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ELECTRIC CORPORATION

FINAL REPORT

FOR

PHASE III OF GROOVE ETCH STUDIES
OXIDE BARRIER ISOLATION

Contract No. NAS 5-3758 Procurement No. 670-WA6712
Westinghouse G.O. 51248AN1A

Prepared By

WESTINGHOUSE ELECTRIC CORPORATION
DEFENSE AND SPACE CENTER
AEROSPACE DIVISION

For

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND

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ABSTRACT AND SUMMARY

15987

The object of this report is to summarize Phase I, Controlled Groove Etching and Phase II, The Chemical Deposition of Silicon Dioxide and Polycrystalline Silicon in these Grooves as well as a report on Phase III, The Construction of Oxide Isolated Regions of Single Crystalline Silicon of a quality suitable for device manufacture.

A process whereby these isolated regions may be fabricated is given. Essentially, the process followed is one which produces clean contaminant-free oxide barrier isolated regions. The method is compatible with existing processes of producing functional electronic blocks.

Author

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1.0 INTRODUCTION

This report covers a three phase program investigating processes and methods of providing isolated "islands" of a semiconductor in a dielectric matrix. The need for the investigation was established by the undesirable presence of "parasitic" capacitance resulting from presently used methods of electrical isolation, i.e., p-n junction isolation.

Phase I deals with the study and development of controllable techniques for chemically cutting grooves in silicon wafers. Phase II experimental work was undertaken to develop techniques and establish a tentative process to chemically deposit silicon dioxide and polycrystalline silicon in these grooves in the silicon. The goals and processes developed were described in detail in these reports; Contract No. NAS 5-3758, Procurement No. 670-190-5 Westinghouse G. O. 51248AHIA (Phase I) and Contract No. NAS 5-3758, Procurement No. 670-W46374; Westinghouse G. O. 51248AQIA (Phase II).

Phase III reports the completion of the program, that of developing techniques and processes to produce oxide barrier isolated islands of silicon suitable for device manufacture. Some of the problems which still offer difficulty are discussed as well as the advantage of this method of isolation. An alternative approach dealing with work in Phase I is discussed, as well as experimental results.

2.0 EXPERIMENTAL PROCEDURE

2.1 Material Preparation (Slice Preparation)

The silicon material used in these experiments were processed by standard lapping and polishing techniques. The slices were lapped (both sides) on a Dallons Planetary Lapper with 12 μ grit size Al_2O_3 to remove damage from the prior slicing operation. The slices were then mounted on stainless steel holders and lapped with 3 μ grit Al_2O_3 to give a smoother surface. Following this a 1 μ grit compound was used for the final polishing operation. After removal from the work holders residual preparation materials were removed from the slices by using solvents and high temperature H_2SO_4 cleaning baths followed by deionized water rinses.

2.2 Specification for Epitaxial Processes

2.2.1 Generally, slices were prepared for experiments by the methods already described in Phase I and Phase II reports, i.e., trichloroethylene swab, HCl high temperature etch, deposition of an opposite type conduction epitaxial layer; this in turn was followed by deposition of an insulating layer of silicon dioxide. The silicon dioxide was formed by introducing CO_2 into the reactor upon completion of the deposition of the desired thickness of the epitaxial layer. The silicon dioxide layer was then treated with N_2 at 1150°C to produce nucleation sites. Following this polycrystalline material was deposited as a backing for use during subsequent operations.

At this point, the slices are removed from the reactor and the initial substrate is removed by standard lapping - polishing techniques. This operation leaves a very thin single crystalline layer (which was the original epitaxial layer) upon an oxide which is in turn supported by a polycrystalline backing material.

A second epitaxial operation then deposited a silicon dioxide mask over the exposed single crystalline epitaxial layer. This oxide was heat treated in nitrogen to insure tenacity of the photoresist chemicals. The slices were then processed by standard photoetching methods to open windows in this protective oxide.

Grooves were then etched in the exposed silicon in a third expitaxial operation by passing anhydrous HCl over the slices at 1200°C. This in turn was followed by another deposition of silicon dioxide dielectric within the grooves. This in turn was follwed by the deposition of a polycrystalline silicon layer sufficiently thick for mechanical strength during subsequent device fabrication.

The original polycrystalline material is then removed by a wet chemical etching process exposing the original deposition of oxide covering the initial epitaxially deposited layer of silicon.

An Appendix "Specification for Epitaxial Processes" is included as Appendix A to this report.

Material produced by this method has certain inherent limitations, i.e., the useful single crystalline silicon layer must of necessity be very thin. This limiting factor has a two fold reason: 1) the oxide protective mask has certain time limitations in contact with anhydrous HCl at 1200°C beyond which its integrity will not remain intact, and 2) the depth of etch into the silicon as well as being geometry dependent is also time dependent. Therefore, in order to insure good grooves and an intact oxide, the ultimate thickness of the single crystal layer must be limited.

Another method of achieving a greater layer thickness of silicon was through use of a wet chemical etch as reported in Phase I. Essentially all other processes except the anhydrous HCl etch at 1200°C were used. (The wet chemical etch was used instead.) The drawback of this process is that the polycrystalline silicon filled groove at the surface of the slice is now much wider than the anhydrous HCl high temperature groove.[1]

Present state-of-the-art indicates that the wet chemical process will probably be more useful in device fabrication until methods of improving the HCl high temperature etch are developed.

3.0 DISCUSSION AND EXPERIMENTAL DATA

3.1 General

As explained in the Phase I report, groove etching by ca. 4% HCl in Hydrogen at 1200°C was used in conjunction with deposition techniques developed during Phase II to provide oxide barrier isolated areas. Although the epitaxial processes are straight forward there are still some material preparation procedures which need improvements. The two main drawbacks to this method are: 1) the rounding of the surface of the slice (produced during the vapor etching step) which engenders problems of parallelism in later processing operations, and 2) the difficulty in mounting these curved surfaces such that material removal processes will maintain flat surfaces parallel to the original epitaxial layer.

Various experiments were run during Phases I and II which established: Etch rates of silicon; deposition rates of both silicon dioxide and silicon; groove etching rates; and the effects of temperature and concentration variations upon etch rates.

In Phase III all the above information was used to plan and coordinate a series of experiments to establish a tentative process for producing isolated islands of single crystalline silicon in a silicon dioxide matrix.

Figure 1 thru 6 shows graphically the methods used to produce these islands.

The cleaned slices of silicon were placed in the epitaxial reactor (3.1)*
on a quartz protective envelope covering a graphite susceptor. (3.2)
After proper purging with nitrogen and then hydrogen, the slices were (3.3.1)
heated to 1200°C and then were exposed to a mixture of anhydrous HCl in H_2 for a time sufficient to remove all residual surface damage

$$4\ HCl_{(g)} + Si_{(s)} \rightleftharpoons SiCl_{4(g)} + 2\ H_{2(g)} \qquad \text{Eq. (1)}$$

caused by material polishing operations. Then (See Figure 1) the slices
received a deposition of N-type doped silicon by passing a mixture of (3.3.2)
$SiCl_4$ and H_2 at 1150°C through the reactor.

$$SiCl_{4(g)} + 2\ H_{2(g)} \rightleftharpoons 4\ HCl_{(g)} + Si_{(s)} \qquad \text{Eq. (2)}$$

After the required thickness of silicon has been deposited CO_2 is (3.3.3)
introduced into the reactor to deposit a layer of silicon dioxide.

$$2\ H_{2(g)} + SiCl_{4(g)} + 2\ CO_{2(g)} \longrightarrow 2\ CO_{(g)} + SiO_{2(s)} + 4\ HCl_{(g)} \qquad \text{Eq. (3)}$$

Following this, a layer of polycrystalline silicon is deposited on the (3.3.4)
surface at an accelerated rate.

* Marginal numbers indicate Process Specification steps in Appendix A.

The slices are now ready for removal of the original substrate material. Two methods have been used: 1) electrochemical etching and 2) the standard lapping-polishing techniques used to originally prepare the slices. To date the best results are obtained from the lapping-polishing method. Care must be taken to lap the surface of the polycrystalline layer to remove all spurious growth. This insures a more nearly perfect parallelism between the original epitaxial layer and the lapping plate to which the slices must be mounted for subsequent lapping-polishing operations. The slices are then lapped and polished by standard material preparation mechanical methods. Final polishing is completed when the original substrate material has been removed. (See Figure 2).

For the second epitaxial operation, the slices are again loaded into the reactor and a layer of silicon dioxide is deposited, (see Figure 3) in the same manner as shown by Eq. (3). (3.3.3)

Windows are cut through this oxide by standard photoengraving techniques (see Figure 4) thus exposing the n-layer of silicon through which grooves will be etched in the third epitaxial process (See Figure 5a). These grooves are cut as was explained in Phase I report, i.e. (3.3.1)

$$4\ HCl_{(g)} + Si_{(s)} \rightleftharpoons SiCl_4 + 2\ H_{2_g} \qquad \text{Eq. (4)}$$

While yet in the reactor a third layer of silicon dioxide is deposited (see Figure 5b) which laterally isolates individual areas from each other. (3.3.3) Immediately, a layer of polycrystalline silicon is deposited (see Figure 5c) which becomes the substrate for the slice during subsequent device manufacturing operations. (3.3.4)

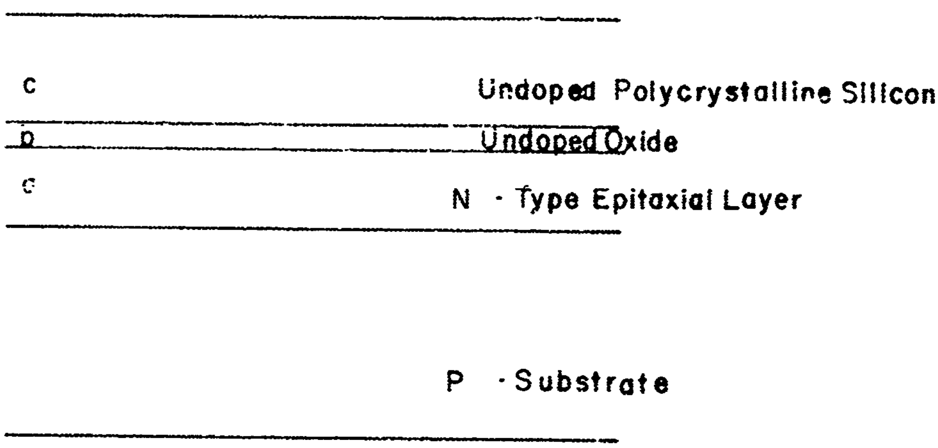

Figure 1

First Epitaxial Operation

(a) After vapor etching the p-type substrate an n-type epitaxial layer is deposited. (b) Over this an undoped layer of silicon dioxide is deposited. This in turn covered with (c) a layer of polycrystalline material to be used for mechanical stability during subsequent handling.

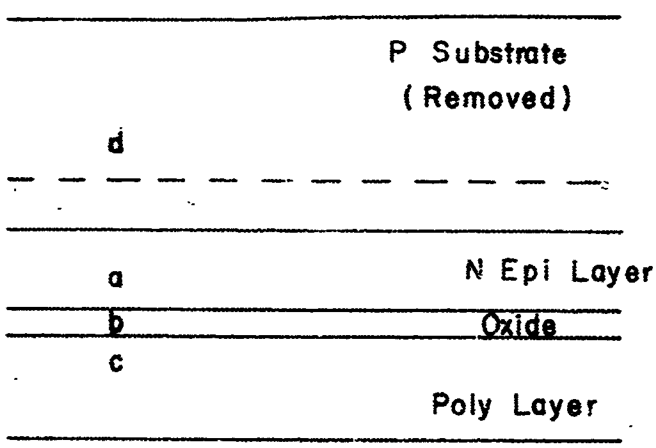

Figure 2

Lapping-Polishing Operation

(d) To remove p-type substrate (slice has been inverted)

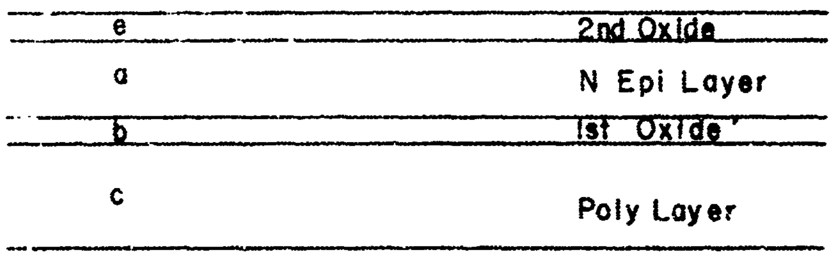

Figure 3

Second Epitaxial Operation

A second silicon dioxide layer (e) is deposited over the exposed N epitaxial layer.

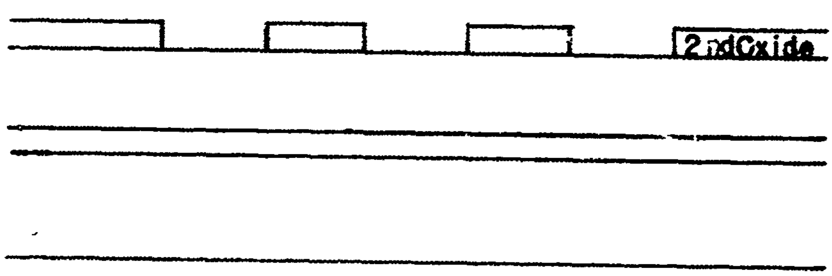

Figure 4

Windows cut through second oxide by standard photoresist methods.

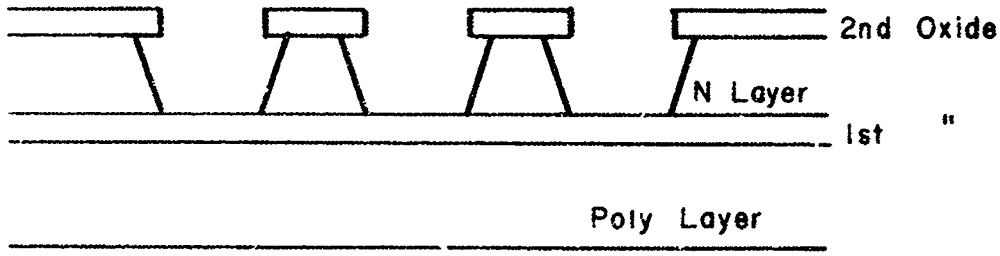

Figure 5a Grooves Etched

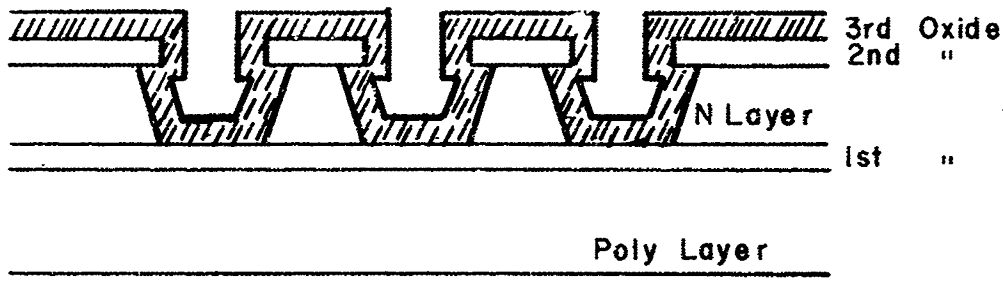

Figure 5b Third Oxide Deposited

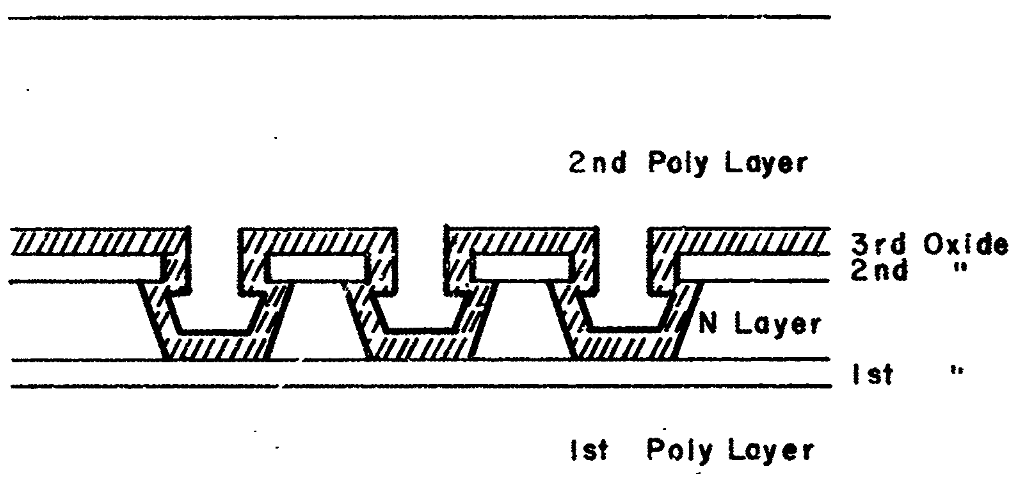

Figure 5c Second Poly Layer Deposited

Figure 5

Third Epitaxial Operation

a. Grooves are etched through silicon to first oxide layer. b. Third or isolation oxide is deposited. c. Second polycrystalline silicon layer is deposited.

The original polycrystalline layer is then removed by etching thus exposing the silicon dioxide protective coating over the islands of N type single crystal silicon of the original epitaxial layer. See Figure 6 and 7.

Figures 8 and 9 show the silicon N-type single crystalline layer sandwiched between layers of silicon dioxide. Figure 10 shows the lateral isolation oxide barrier deposited at the periphery of the "island."

Inasmuch as the silicon single crystalline layer thickness has limitations in the HCl high temperature etching process, an alternate method to remove these limitations was also used. This alternate method involved the use of a wet chemical etch as has been used in many standard processes. After the second epitaxially (thermally) deposited layer of silicon dioxide has had windows opened, the exposed silicon is then etched with a mixture of HNO_3:HF:HAc (in the ratio of 84:8:8). This cuts away silicon in the open window through to the original thermally deposited oxide. Subsequently, the overhang of the silicon on the islands is removed by HF. Thereafter, the operations proceed exactly as stated above, i.e., the slice is subjected to a deposit of silicon dioxide by the CO_2 + (3.3.3)
$SiCl_4$ + H_2 method, which is then covered by polycrystalline silicon. (3.3.4)

This method produces a more useful slice at the present state-of-the-art. The thickness of the useful area has no device limiting characteristics (see Figure 11). There is, however, a loss of useful area at the surface of the slice. (See Figure 12).

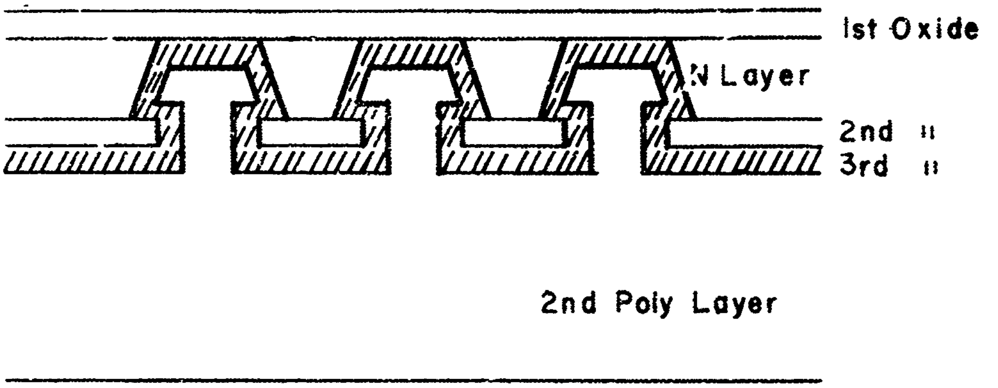

Figure 6

Final Isolation Diagram (Slice Re-inverted)

Showing silicon islands isolated by oxide barrier after first polycrystalline silicon layer is removed by etching.

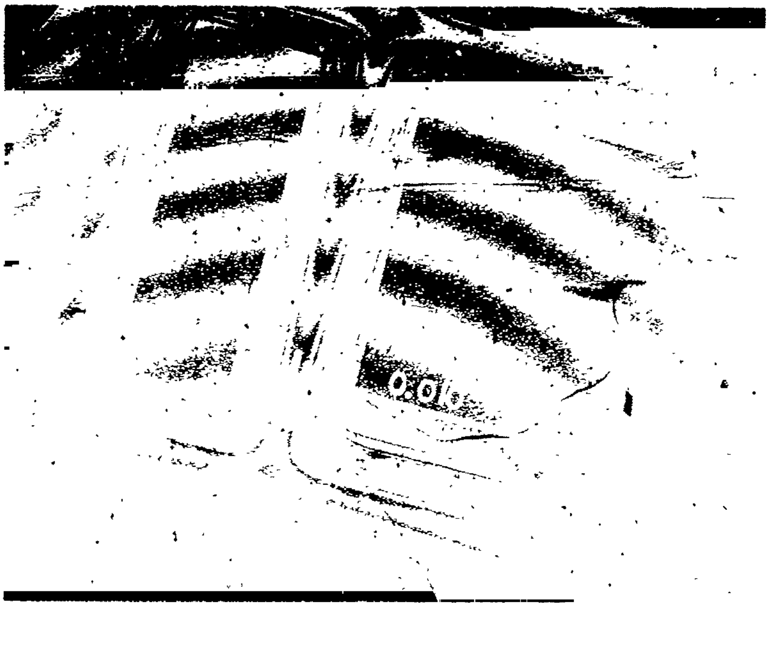

Figure 7

Photomicrograph of isolated island surrounded by oxide barrier and polycrystalline silicon.

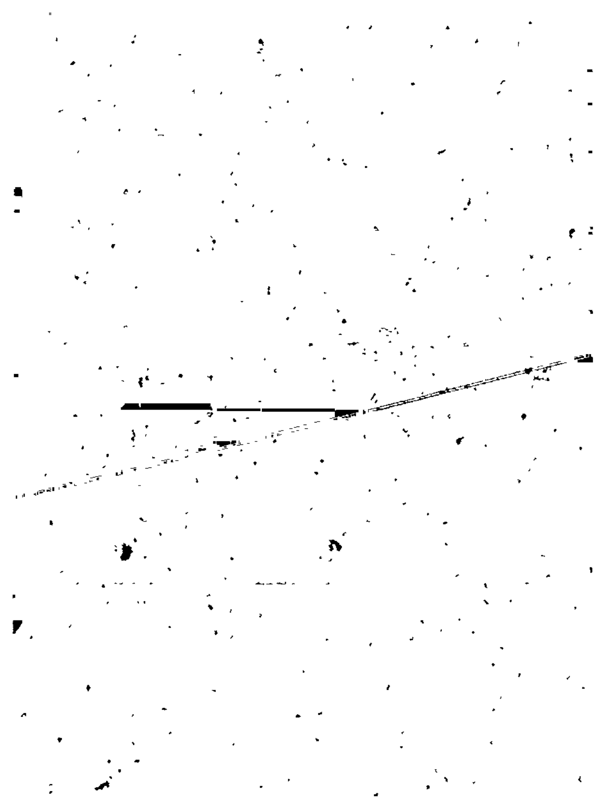

Figure 8

N-type single crystalline silicon layer sandwiched between layers of silicon dioxide.

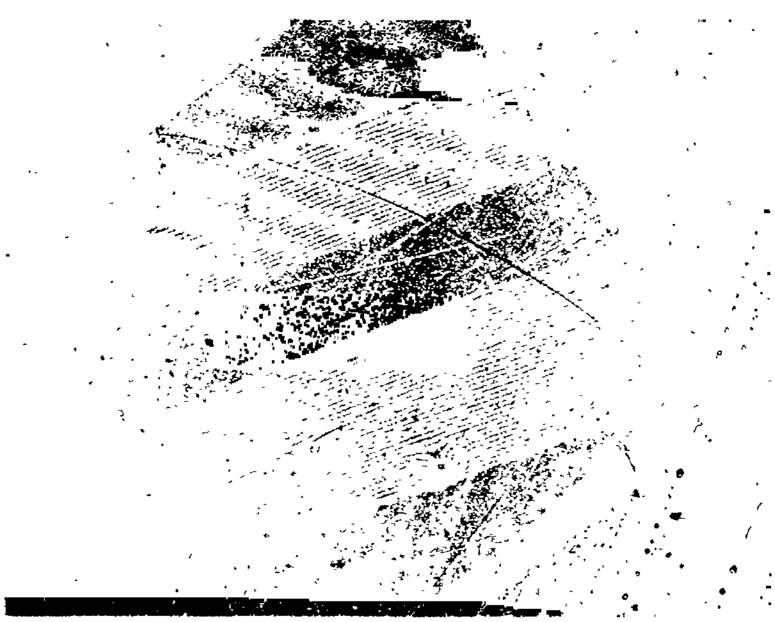

Figure 9

Silicon sandwiched between oxide layers.

Figure 10

Photo showing oxide barrier at periphery of island. (oxide)

Figure 11. Photo showing island lateral isolation oxide barrier as well as sandwiched single crystalline silicon between top and bottom poly-crystalline and oxide layers (wet chemical process).

Figure 12. Photo showing top surface of wet chemical process slice.

4.0 CONCLUSIONS AND RECOMMENDATIONS

It is feasible to produce oxide barrier isolated regions suitable for integrated circuit device manufacture by the high temperature HCl groove etching techniques. However supporting techniques of material removal methods at present are inadequate to assure high yield for subsequent steps in the manufacturing processes. A second process used - the wet chemical etching of the silicon grooves is also feasible and preferable to the high temperature anhydrous HCl groove etching.

Present methods of electrochemical polishing tried in material removal have not been adequate to assure device quality surfaces. More experiments should be planned in this area.

A set of specifications for epitaxial processes are included as an appendix to this report.

5.0 REFERENCES

1. A. F. McKelvey, C. G. Thornton and G. L. Schnable
   New Techniques for Reduction Parasitic Resistance and Capacitance in Integrated Circuits. Conference paper, Fourth Annual Microelectronics Symposium. May 1965, St. Louis, Mo.

2. M. V. Sullivan, D. L. Klein, R. M. Finne, F. A. Pompliano and G. A. Kalle
   Journal of the Electrochemical Society Vol. 110, No. 5, May 1963.

APPENDIX A

Specification for Epitaxial Processes

1. Equipment
    - 1.1 Gas control panel
    - 1.2 Epitaxial reactor
    - 1.3 RF generator
    - 1.4 Optical pyrometer
    - 1.5 4-point probe
    - 1.6 Angle lapping equipment
    - 1.7 Interference fringe apparatus
    - 1.8 Surface hydrogen purifier
    - 1.9 Tweezers
2. Material
    - 2.1 Silicon tetrachloride
    - 2.2 Diborane in H_2(100 PPM)
    - 2.3 Silane in H_2 (100 PPM)
    - 2.4 Arsine in H_2 (100 PPM)
    - 2.5 Hydrogen
    - 2.6 Nitrogen
    - 2.7 Carbon dioxide (Coleman grade)
    - 2.8 Graphite susceptor
    - 2.9 Quartz envelope

2.10 Quartz sled

2.11 Silicon slices (previously polished and cleaned)

2.12 Petri dishes Pyrex

2.13 Lint free paper

2.14 Trichloroethylene

2.15 HF

2.16 HNO_3

2.17 HAc

2.18 Cotton balls

2.19 Anhydrous HCl

3. Procedure

3.1 Cleaning Process

3.1.1 Place slices of silicon in petri dish.

3.1.2 Cover slices with Trichloroethylene (TCE). Note: Slices must not be allowed to become exposed to air by Trichloroethylene evaporation; must be kept covered until removal.

3.1.3 Remove a slice; place on at least three thicknesses of lint free paper.

3.1.4 With plastic squirt bottle apply a small amount of TCE.

3.1.5 Swab slice with cotton swab or ball to physically remove any trace of foreign particle.

3.1.6 Place slice in clean petri dish (bottom of dish to be covered by disc of lint free paper.)

3.1.7 Repeat steps 3.1.3 thru 3.1.6 until all slices have been cleaned.

3.2 Loading Boat and Reactor

3.2.1 Assemble graphite susceptor into quartz envelope.

3.2.2 Place assembly on sled.

3.2.3 Place slices of silicon on boat centered properly along midline.

3.2.4 Introduce sled and boat assembly with slices in reactor tube and center boat within extremes of RF load coil.

3.2.5 Replace end cap and start purge of reactor tube with N_2.

3.3 Epitaxial Processes

3.3.1 Vapor Etching by HCl

3.3.1.1 Purge reactor tube of all atmosphere by nitrogen flow. (At least 3 minutes).

3.3.1.2 Purge reactor tube of all nitrogen by hydrogen. (At least 3 minutes).

3.3.1.3 Turn on RF generator and allow temperature to reach 1200°C. Temperature is checked by Optical Pyrometer.

3.3.1.4 Set H_2 flow to desired rate.

3.3.1.5 Start HCl flow to desired rate and set timer to desired etch time; allow etch to proceed for this time.

3.3.1.6 Stop HCl flow after completion of time, allowing only H_2 to flow through reactor. If HCl etch only desired, move to step 3.3.2.5.

3.3.2 Epitaxial Deposition of Silicon

3.3.2.1 Set temperature to 1150°C.

3.3.2.2 Set gas flow rates (according to desired doping levels) for H_2 flow through $SiCl_4$ bottle 'H_2 bypasses $SiCl_4$ bottle) and for doping gases as desired. (Arsine or phosphorus for N type and diborane for p type) the gas flows of doping gases are directed to exhaust.

3.3.2.3 Start flow of H_2 thru $SiCl_4$ bottle and direct doping gas flow from exhaust to reactor. (Set timer for desired length of time.) Allow deposition to continue for length of time necessary to deposit desired thickness of layers.

3.3.2.4 Stop H_2 flow thru $SiCl_4$ and direct doping gas from reactor to exhaust.

3.3.2.5 Allow reactants to purge from reactor by H_2 flow. (At least 2 minutes).

3.3.2.6 Turn off RF generator and allow reactor to cool. Turn off dopant supplies.

3.3.2.7 Purge H_2 from reactor with nitrogen (at least 2 minutes).

3.3.2.8 Slices may be removed from the reactor by removing sled and boat assembly.

3.3.2.9 Place slices in clean petri dish on clean lint free paper.

3.3.2.10 Evaluate test slices for layer thickness and resistivity. By 4-point probe and thickness evaluation equipment.

3.3.3 Oxide Deposition - If an oxide layer is desired for masking or protection, follow procedure of epitaxial deposition 3.3.2 thru step 3.3.2.3, then proceed with the following:

3.3.3.1 Allow H_2 flow to continue through $SiCl_4$ bottle; divert doping gas from reactor to exhaust; start and set CO_2 flow to reactor and start timer for desired time and thickness.

3.3.3.2 Allow to proceed for desired time.

3.3.3.3 Stop H_2 flow through $SiCl_4$, stop CO_2 flow to reactor, maintain temperature (1150°C)

3.3.3.4 Stop all H_2 flow to reactor and introduce nitrogen flow.

3.3.3.5 Allow nitrogen to flow for time required.

3.3.3.6 If this is final step, proceed according to the following:

3.3.3.7 Turn off RF generator and allow reactor to cool.

3.3.3.8 Remove slices per 3.3.2.8 thru 3.3.2.10.

3.3.4 Polycrystalline silicon deposition (one oxide). If a polycrystalline layer is desired over the oxide continue oxide deposition (3.3.3) up to step 3.3.3.4 and then proceed with the following.

3.3.4.1 Continue nitrogen flow through the reactor for at least three minutes minimum.

3.3.4.2 Stop nitrogen flow; start H_2 flow and purge nitrogen from the reactor.

3.3.4.3 Start H_2 flow through $SiCl_4$ at the setting desired to deposit silicon at the proper rate. Set timer.

3.3.4.4 Allow deposition to proceed for time necessary.

3.3.4.5 Stop H_2 flow through $SiCl_4$.

3.3.4.6 Allow H_2 to purge reactor. (At least 2 minutes).

3.3.4.7 Turn off RF generator.

3.3.4.8 Proceed to cool down and remove slices according to steps 3.3.2.7 thru 3.3.2.9.

3.4 Groove Cutting by Wet Chemical Method

3.4.1 Slices with windows cut through the second epitaxially grown (thermal) oxide are mounted on a glass slide by apiezon wax (black wax). Care must be taken to keep wax from face of the wafer.

3.4.2 A mixture of HNO_3, HF and HAc is prepared in the ratios of 84:8:8 respectively.

3.4.3 The mounted slice is introduced to the acid mixture and etched (with constant agitation) until the original oxide layer is exposed. (This will be noted by the reflection being very clear).

3.4.4 The slice is now removed from the acid mixture and cleaned in D.I. water for at least 5 separate rinses.

3.4.5 The slices are submerged in HF (48%) until all the overhanging silicon dioxide has been removed. (This also can be detected visually).

3.4.6 Slices are removed from glass slide and cleaned by organic solvents prior to continuing subsequent operations.