Westinghouse

ELECTRIC CORPORATION

FINAL REPORT

FOR

EPITAXIAL PROCESS FOR DEVELOPMENT FOR MONOLITHIC COMPLEMENTARY MOS-FET STRUCTURE WITH OXIDE BARRIER ISOLATION

W.O. 670-W46784 Contract No. NAS 5-3758
Westinghouse G.O. No. 51248-BD

15 March - 15 September 1965

Prepared By

WESTINGHOUSE ELECTRIC CORPORATION
DEFENSE AND SPACE CENTER
AEROSPACE DIVISION

For

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND

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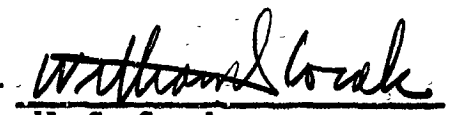
Approved By 
W. S. Corak

ABSTRACT AND SUMMARY

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This report summarizes the results of work done on experiments to provide oxide barrier isolation between areas of different conductivity type silicon. These areas are suitable for use in manufacturing complimentary MOS-FET devices. The process is essentially a combination of the groove-refill, and the oxide isolation processes developed and explained in prior reports.

A process is provided along with specifications and directions whereby these results may be evaluated and/or duplicated. Photos and diagrams are provided to show typical results obtained.

Author

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1.0 INTRODUCTION

This report covers a program investigating process and methods of using epitaxy and allied integrated circuit operations to provide oxide barrier isolated islands of both p and n conductivity type. Such islands have been successfully made by utilizing and combining methods previously reported[1,2]. A combination of etch and groove refill was used both for the oxide barriers and the pad formation. Opposite type conductivity silicon was deposited within the grooves in the original island formed by the oxide barrier isolation method. The problems encountered are discussed.

The processes used are described and a detailed specification is provided in an appendix.

Electrical tests and chemical staining evaluation indicated that the goal of the study is accomplished.

2.0 EXPERIMENTAL PROCEDURE

2.1 Slice Preparation

The silicon material used in these experiments was processed by standard lapping and polishing techniques. The slices were lapped (both sides) on a Dallons Planetary Lapper with 12 μ grit size Al_2O_3 to remove damage from the prior slicing operations. The slices were then mounted on stainless steel holders and lapped with 3 μ grit Al_2O_3 to give a smoother surface. Following this, 1 μ grit compound was used for the final polishing operation. After removal from the work holders, residual organic and preparation materials were removed from the slices by using organic solvents and high temperature H_2SO_4 cleaning baths followed by de-ionized water rinses.

2.2 Specification for Epitaxial Processes

2.2.1 Generally, slices were prepared for these experiments by these methods: Trichloroethylene swab; HCl high temperature etch; deposition of an opposite conductivity epitaxial layer; this in turn was followed by the deposition of an insulating layer of silicon dioxide. The silicon dioxide was formed by introducing CO_2 into the reactor upon completion of the deposition of the desired thickness epitaxial layer. This silicon dioxide layer was then subjected to a high temperature heat treatment in dry nitrogen gas to improve nucleation of subsequent layers. A polycrystalline silicon layer was deposited directly on this oxide layer. This polycrystalline layer is used as a backing to give strength during handling in subsequent operations.

The major portion of the original substrate was then removed by mechanical lapping-polishing techniques and the polished underside (inverted slices) covered by silicon dioxide (CO_2 method). Windows were opened through this second oxide in the desired locations by standard photoetching techniques. Grooves were then etched through the remaining portion of the original substrate and the epitaxially deposited layer exposing the first oxide. (This oxide separates the epitaxial layer from the polycrystalline backing material).

The slice was then subjected to a deposition of oxide (CO_2 method) which partially fills the grooves. This process was followed immediately by a polycrystalline silicon deposition which is thick enough to offer mechanical strength and support for ensuing operations during device manufacture.

The original polycrystalline backing material was then removed from the slice by etching. This exposed isolated islands of the original epitaxial silicon surface which was still protected by the original silicon dioxide layer.

The next steps were undertaken to provide opposite type conductivity pads on these islands: Windows were cut through the protective oxide by standard photo-engraving techniques and grooves (pockets) were etched into the silicon by the previously reported wet chemical etching process.

The pockets were then refilled by a standard epitaxially deposited layer of opposite type conductivity silicon. Spuriously nucleated silicon growth on the oxide protective mask was removed by etching in HF with ultrasonic agitation.

An appendix "Specification for Epitaxial Processes" which describes in detail the operational procedures is included as Appendix A to this report.

3.0 DISCUSSION AND EXPERIMENTAL DATA

3.1 General

The goals of this project were to develop a procedure and provide an epitaxial process specification to provide oxide isolated islands of both P and N type silicon suitable for fabrication of complimentary MOS-FET devices on a monolithic substrate.

Two programs which have been previously reported[1,2] gave results that if compatible would solve the problems and provide a method to achieve the goals of this program. From information and data generated in these programs an approach to the solution of the problems in the present program was formulated. Attempts have been made to utilize a two-sided approach but front to back registration of masks on the same slice was inadequate for device fabrication requirements. Therefore an approach using the groove filling technique[2] was used after the island of silicon had been formed by the oxide barrier isolation[1] method.

3.2 Experimental

Cleaned polished P type slices of silicon were placed in the epitaxial reactor on a quartz protective envelope covering a graphite susceptor. After proper purging with nitrogen and then hydrogen, the slices were heated to 1200°C and then exposed to a mixture of anhydrous HCl in H_2 for a time sufficient to remove all residual surface damage caused by material polishing operations. (3.1)* (3.2) (3.3)

*Margin numbers indicate Process Specification steps in Appendix A.

$$4\ HCl\ (g) + Si\ (s) \rightleftharpoons SiCl_4\ (g) + 2H_2(g) \qquad (1)$$

The slices then received a deposition of N type doped silicon by passing a mixture of $SiCl_4$, PH_3 and H_2 through the reactor and over the slices which were maintained at a temperature of 1150°C. (3.3.2)

$$SiCl_4\ (g) + 2H_2\ (g) \rightleftharpoons 4HCl\ (g) + Si\ (s) \qquad (2)$$

After the required thickness of doped silicon has been deposited, the dopant flow is stopped and CO_2 is introduced into the reactor and a layer of silicon dioxide is pyrolytically deposited on the surface of the slice. (3.3.3)

$$2H_2\ (g) + SiCl_4\ (g) + 2\ CO_2(g) \rightleftharpoons 2CO(g) + 4\ HCl\ (g) + SiO_2(s) \qquad (3)$$

The slices were then heat treated in N_2 for 3-10 minutes. Immediately following this heat treatment the nitrogen is purged from the reactor tube and a layer of polycrystalline silicon is deposited over the silicon dioxide. This layer is used as a mechanical back-up for physical strength during subsequent operations during device fabrication. See Figure 1. (3.3.5) (3.3.4)

Inasmuch as spurious nucleation can and usually does occur at the periphery of the slices it is imperative to remove such growths prior to further mechanical operations on the slices. This operation is carried out by hand lapping the upper surface using a medium size grit and a glass plate. (grit size = 12-15 μ). The slices were then cleaned and mounted on a lapping holder with the now smooth polycrystalline layer facing the holder. This leaves the original substrate material exposed for subsequent mechanical lapping and polishing operations.

The slices were then machine lapped with 12-15 μ grit alumina lapping compound until the major portion of the original substrate material was removed. Care must be taken to insure adequate removal while keeping enough of the original slice and the epitaxial layer to insure sufficient

material for device fabrication. Subsequently the slice is lapped with 3 micron alumina grit and then polished with 1 micron grit polishing compound. This leaves a slice of silicon with a layer of polycrystalline silicon, a silicon dioxide isolation/insulation layer, an epitaxial layer of silicon, and a minute portion of the original substrate. (If desired, the entire original substrate may be removed; however, this is a much more exacting mechanical engineering problem.)

The polished slice is then cleaned to remove all residual mechanical preparation contaminants and is then subjected to a deposition of a second silicon dioxide layer by the CO_2 process. The layer is deposited (3.3.3) thick enough to mask the silicon single crystal during deep wet chemical etching processes. See Figure 2.

Windows are then cut through this second oxide layer at the desired locations by standard photoengraving methods. See Figure 3.

Following the window opening operation isolation grooves are etched through the single crystalline silicon thus exposing the original (3.4) silicon dioxide layer deposited. The slice is then replaced into the epitaxial reactor and after proper purging, a layer of silicon dioxide (3.3.3) is grown on the surface and in the grooves. This layer is also grown by the CO_2 method. Immediately following this third oxide layer operation a (3.3.4) second polycrystalline layer is deposited. Inasmuch as this layer will be the ultimate support of the slice, it is grown somewhat thicker so as to offer support for all subsequent operations. See Figure 4.

The slice is then removed from the reactor and mounted protectively on a glass slide by apiezon wax exposing only the original polycrystalline layer which is removed by etching. When this layer is removed

the exposed surface (the original silicon dioxide layer) is seen. Through this may be seen the gridwork which indicates isolated islands of single crystal silicon are present on the slice. See Figure 5.

The islands on the slice are now all n type and it is necessary to perform the operations which will give both p and n type areas upon which complimentary MOS-FET structures may be fabricated.

Windows are now cut through the original oxide at the desired locations by standard photoengraving methods. Another method considered but not attempted was to remove all the original oxide, regrow another oxide in its place and then cut windows through it. This would be necessary only if the originally deposited oxide were no longer suitable for protective reasons during subsequent operations.

Following the window opening operation, a wet chemical etch (3.4) mixture composed of HNO_3, HF, and HAc in the volumetric ration of 84:8:8 was used to etch pockets or grooves in the exposed silicon.

Following the pocket etch, the slices are again placed into the reactor and a layer of silicon is deposited upon the exposed silicon. There (3.3.2) is some spurious growth of silicon on the surface of the silicon dioxide which is removed by exposing the slice to 48% HF with ultrasonic agitation. See Figure 6.

Figures 7 and 8 show 10° and 20° respectively beveled and stained photomicrographs of finished structures.

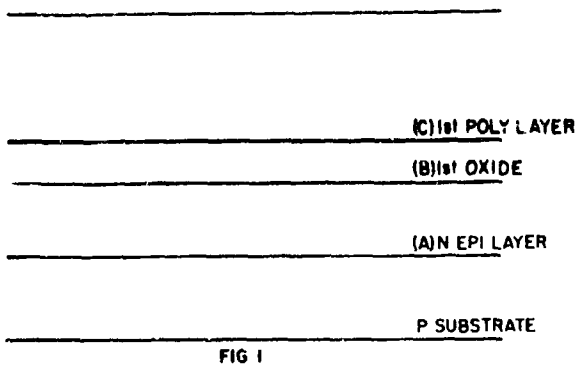

FIG 1

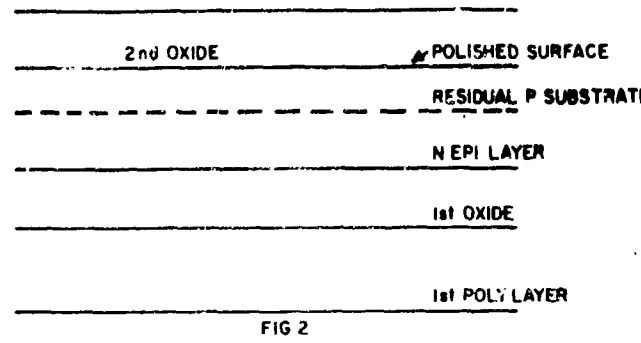

FIG 2

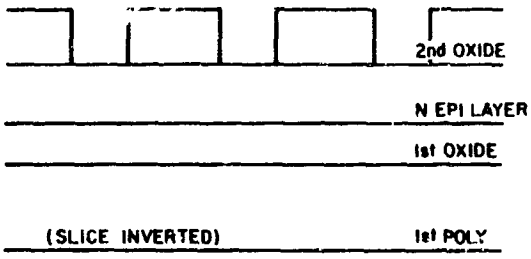

FIG 3

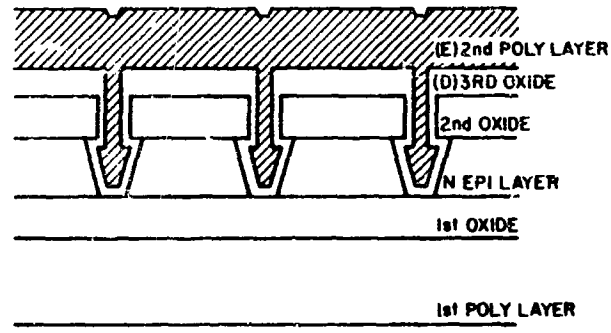

FIG 4

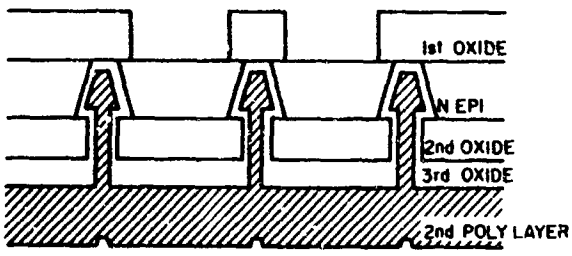

FIG 5

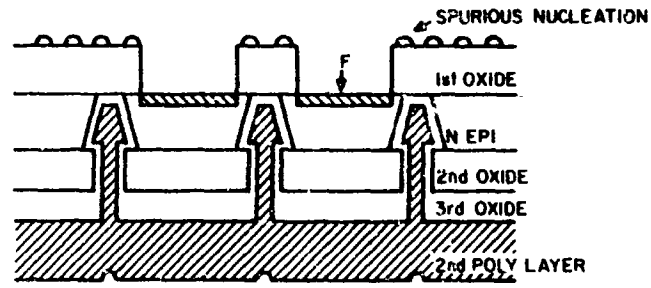

FIG 6

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Figure 1. First Epitaxial Operation (A) N Type Epitaxial Layer (B) Pyrolytically Deposited SiO_2 (C) Polycrystalline Backing Layer
Figure 2. Slice After Deposition of Second Oxide Layer
Figure 3. Windows Cut Through 2nd Oxide by Photoresist Techniques
Figure 4. Grooves Etched Through Epitaxial Layer and (D) 3rd Oxide Layer is Deposited. (E) Second Polycrystalline Layer Deposited.
Figure 5. Slice After Removal of 1st Polycrystalline Layer and Windows Cut Through 1st Oxide for Pad Formation Groove Etch.
Figure 6. Slice After Groove Etch (Pad) and (F) Pad Refilled with P Type Silicon.

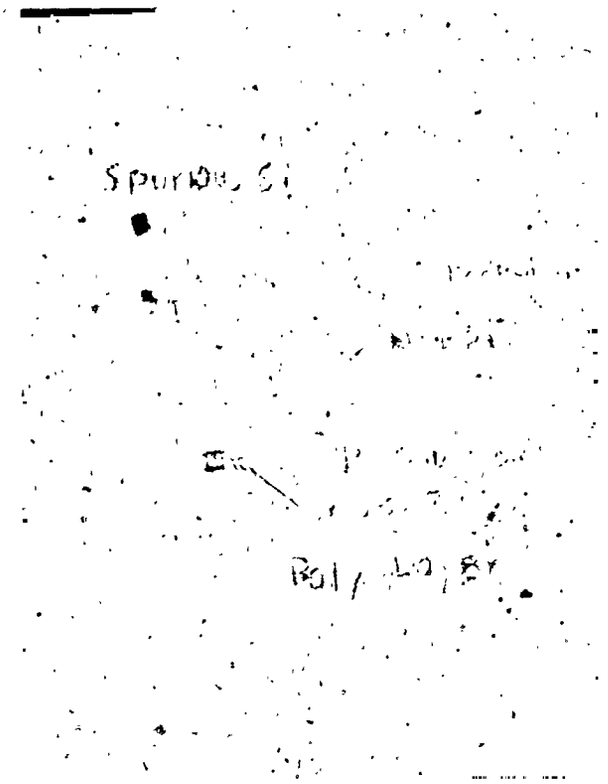

Figure 7 Photo Showing Finished Structure, Note 3 Oxide Layers. 10° Bevel

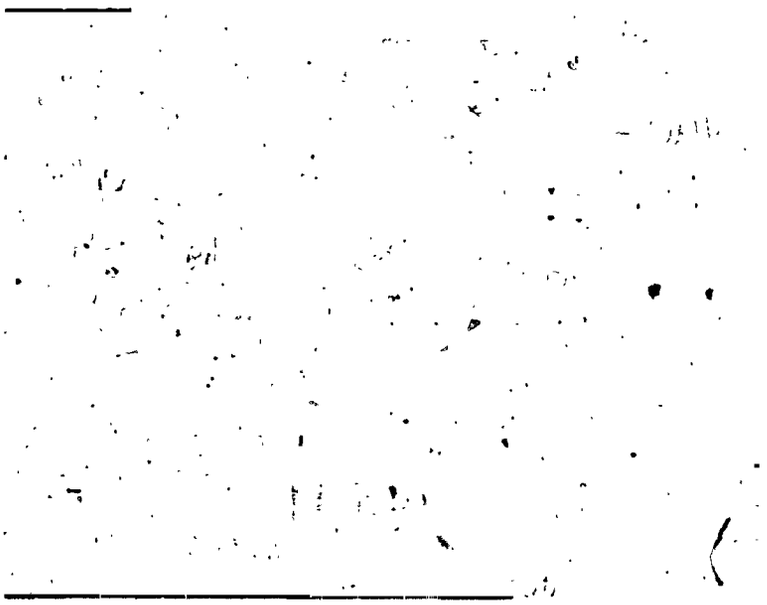

Figure 8. Photo Showing Finished Structure. 2° Bevel.

4.0 CONCLUSIONS AND RECOMMENDATIONS

It is possible to form a checkerboard of alternating n and p type exposed areas of single crystalline silicon on the surface of a slice of silicon. These areas are isolated from each other by silicon dioxide which is deposited by pyrolytic decomposition of $SiCl_4$ and CO_2. The use of this material is compatible with existing previous and subsequent device fabrication operations.

There are certain areas that offer engineering and development problems, however. The major problem is the curved surface of the final layer deposited in the etched groove (pad). This problem would only be detrimental in the metallized interconnect operation. Most other problems are minor in nature and involve becoming familiar with the new techniques used.

It is recommended that continued investigation be carried out to improve surface matching at the edge of the pads deposited in the etched grooves. These edges are adequate to make individual devices, however, inasmuch as metallic interconnections are desirable, improved surface conditions would make them more reliable.

5.0 NEW TECHNOLOGY

A method and process for providing material for monolithic complimentary MOS-FET structures with oxide barrier isolation is defined in this report.

Isolated P and N type pads or areas are produced and tests indicate their capability of being used for device fabrication. This method is a combination of the groove-refill and the oxide isolation processes previously reported. The sequence of operations and their control are explained.

6.0 REFERENCES

1. Final Report for Phase III of Groove Etching Study, Oxide Barrier Isolation, Westinghouse Electric Corporation, Contract No. NAS5-3758, Procurement No. 670-WA6712, Westinghouse G. O. 51248AN1A, 1 June 1965.

2. Final Report for Epitaxial Process Development for Monolithic Complementary MOS-FET Structures with P-N Junction Isolation. Contract No. NAS5-3758, Procurement No. 670-W46754, Westinghouse G. O. 51243AX1A, 15 July 1965.

APPENDIX A

Specification for Epitaxial Processes

1. Equipment
   - 1.1 Gas control panel
   - 1.2 Epitaxial reactor
   - 1.3 RF generator
   - 1.4 Optical pyrometer
   - 1.5 4-point probe
   - 1.6 Angle lapping equipment
   - 1.7 Interference fringe apparatus
   - 1.8 Surface hydrogen purifier
   - 1.9 Tweezers
2. Material
   - 2.1 Silicon tetrachloride
   - 2.2 Diborane in H_2(100 PPM)
   - 2.3 Silane in H_2 (100 PPM)
   - 2.4 Arsine in H_2 (100 PPM)
   - 2.5 Hydrogen
   - 2.6 Nitrogen
   - 2.7 Carbon dioxide (Coleman grade)
   - 2.8 Graphite susceptor
   - 2.9 Quartz envelope

2.10 Quartz sled

2.11 Silicon slices (previously polished and cleaned)

2.12 Petri dishes Pyrex

2.13 Lint free paper

2.14 Trichloroethylene

2.15 HF

2.16 HNO_3

2.17 HAc

2.18 Cotton balls

2.19 Anhydrous HCl

3. Procedure

3.1 Cleaning Process

3.1.1 Place slices of silicon in petri dish.

3.1.2 Cover slices with Trichloroethylene (TCE). Note: Slices must not be allowed to become exposed to air by Trichloroethylene evaporation; must be kept covered until removal.

3.1.3 Remove a slice; place on at least three thicknesses of lint free paper.

3.1.4 With plastic squirt bottle apply a small amount of TCE.

3.1.5 Swab slice with cotton swab or ball to physically remove any trace of foreign particle.

3.1.6 Place slice in clean petri dish (bottom of dish to be covered by disc of lint free paper.)

3.1.7 Repeat steps 3.1.3 thru 3.1.6 until all slices have been cleaned.

3.2 Loading Boat and Reactor

3.2.1 Assemble graphite susceptor into quartz envelope.

3.2.2 Place assembly on sled.

3.2.3 Place slices of silicon on boat centered properly along midline.

3.2.4 Introduce sled and boat assembly with slices in reactor tube and center boat within extremes of RF load coil.

3.2.5 Replace end cap and start purge of reactor tube with N_2.

3.3 Epitaxial Processes

3.3.1 Vapor Etching by HCl

3.3.1.1 Purge reactor tube of all atmosphere by nitrogen flow. (At least 3 minutes).

3.3.1.2 Purge reactor tube of all nitrogen by hydrogen. (At least 3 minutes).

3.3.1.3 Turn on RF generator and allow temperature to reach 1200°C. Temperature is checked by Optical Pyrometer.

3.3.1.4 Set H_2 flow to desired rate.

3.3.1.5 Start HCl flow to desired rate and set timer to desired etch time; allow etch to proceed for this time.

3.3.1.6 Stop HCl flow after completion of time, allowing only H_2 to flow through reactor. If HCl etch only desired, move to step 3.3.2.5.

3.3.2 Epitaxial Deposition of Silicon

3.3.2.1 Set temperature to 1150°C.

3.3.2.2 Set gas flow rates (according to desired doping levels) for H_2 flow through $SiCl_4$ bottle (H_2 bypasses $SiCl_4$ bottle) and for doping gases as desired. (Arsine or phosphorus for N type and diborane for p type) the gas flows of doping gases are directed to exhaust.

3.3.2.3 Start flow of H_2 thru $SiCl_4$ bottle and direct doping gas flow from exhaust to reactor. (Set timer for desired length of time.) Allow deposition to continue for length of time necessary to deposit desired thickness of layers.

3.3.2.4 Stop H_2 flow thru $SiCl_4$ and direct doping gas from reactor to exhaust.

3.3.2.5 Allow reactants to purge from reactor by H_2 flow. (At least 2 minutes).

3.3.2.6 Turn off RF generator and allow reactor to cool. Turn off dopant supplies.

3.3.2.7 Purge H_2 from reactor with nitrogen (at least 2 minutes).

3.3.2.8 Slices may be removed from the reactor by removing sled and boat assembly.

3.3.2.9 Place slices in clean petri dish on clean lint free paper.

3.3.2.10 Evaluate test slices for layer thickness and resistivity. By 4-point probe and thickness evaluation equipment.

3.3.3 Oxide Deposition - If an oxide layer is desired for masking or protection, follow procedure of epitaxial deposition 3.3.2 thru step 3.3.2.3, then proceed with the following:

3.3.3.1 Allow H_2 flow to continue through $SiCl_4$ bottle; divert doping gas from reactor to exhaust; start and set CO_2 flow to reactor and start timer for desired time and thickness.

3.3.3.2 Allow to proceed for desired time.

3.3.3.3 Stop H_2 flow through $SiCl_4$, stop CO_2 flow to reactor, maintain temperature (1150°C)

3.3.3.4 Stop all H_2 flow to reactor and introduce nitrogen flow.

3.3.3.5 Allow nitrogen to flow for time required.

3.3.3.6 If this is final step, proceed according to the following:

3.3.3.7 Turn off RF generator and allow reactor to cool.

3.3.3.8 Remove slices per 3.3.2.8 thru 3.3.2.10.

3.3.4 Polycrystalline silicon deposition (one oxide). If a polycrystalline layer is desired over the oxide continue oxide deposition (3.3.3) up to step 3.3.3.4 and then proceed with the following.

3.3.4.1 Continue nitrogen flow through the reactor for at least three minutes minimum.

3.3.4.2 Stop nitrogen flow; start H_2 flow and purge nitrogen from the reactor.

3.3.4.3 Start H_2 flow through $SiCl_4$ at the setting desired to deposit silicon at the proper rate. Set timer.

3.3.4.4 Allow deposition to proceed for time necessary.

3.3.4.5 Stop H_2 flow through $SiCl_4$.

3.3.4.6 Allow H_2 to purge reactor. (At least 2 minutes).

3.3.4.7 Turn off RF generator.

3.3.4.8 Proceed to cool down and remove slices according to steps 3.3.2.7 thru 3.3.2.9.

3.4 Groove Cutting by Wet Chemical Method

3.4.1 Slices with windows cut through the second epitaxially grown (thermal) oxide are mounted on a glass slide by a piezon wax (black wax). Care must be taken to keep wax from face of the wafer.

3.4.2 A mixture of HNO_3, HF and HAc is prepared in the ratios of 84:8:8 respectively.

3.4.3 The mounted slice is introduced to the acid mixture and etched (with constant agitation) until the original oxide layer is exposed. (This will be noted by the reflection being very clear).

3.4.4 The slice is now removed from the acid mixture and cleaned in D.I. water for at least 5 separate rinses.

3.4.5 The slices are submerged in HF (48%) until all the overhanging silicon dioxide has been removed. (This also can be detected visually).

3.4.6 Slices are removed from glass slide and cleaned by organic solvents prior to continuing subsequent operations.