Westinghouse

ELECTRIC CORPORATION

FINAL REPORT

FOR

EPITAXIAL PROCESS DEVELOPMENT FOR MONOLITHIC COMPLEMENTARY MOS-FET STRUCTURES WITH P-N JUNCTION ISOLATION

1 FEBRUARY 1965 - 15 JULY 1965

W.O. 670-W46754 Contract No. NAS 5-3758

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Prepared by

WESTINGHOUSE ELECTRIC CORPORATION
DEFENSE AND SPACE CENTER
AEROSPACE DIVISION

For

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND

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ABSTRACT AND SUMMARY

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This report summarizes the work done on and the results of the p-type silicon back filling of grooves or pockets etched into n-type silicon slices. Two methods of etching pockets are discussed, gaseous high temperature and the wet chemical method. Comparisons are noted of each.

A process is provided along with specifications and directions whereby these results may be evaluated and/or duplicated. Photos and diagrams show general usefulness of the methods discussed.

Author

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1.0 INTRODUCTION

This report covers a program investigating processes and methods of providing "p" type pockets of silicon regrown epitaxially into cavities etched into "n" type silicon. Two methods of cavity etching were used: One involving the use of high temperature anhydrous hydrogen chloride in a carrier gas of hydrogen; the other utilized a wet chemical mixture of nitric, acetic and hydrofluoric acid. The manner of depositing silicon within the pockets thus formed is discussed.

The processes used as well as a detailed specification is provided.

Electrical tests have indicated device quality material is provided by this process.

2.0 EXPERIMENTAL PROCEDURE

2.1 Slice Preparation

The silicon material used in these experiments was processed by standard lapping and polishing techniques. The slices were lapped (both sides) on a Dallons Planetary Lapper with 12μ grit size Al_2O_3 to remove damage from the prior slicing operations. The slices were then mounted on stainless steel holders and lapped with 3μ grit Al_2O_3 to give a smoother surface. Following this, a 1 grit compound was used for the final polishing operation. After removal from the work holders, residual organic and preparation materials were removed from the slices by using organic solvents and high temperature H_2SO_4 cleaning baths followed by de-ionized water rinses.

2.2 Specification for Epitaxial Processes

2.2.1 Generally, slices were prepared for the experiments by these methods: trichlorethylene swab; HCl high temperature etch, deposition of an opposite conductivity epitaxial layer; this in turn was followed by the deposition of an insulating layer of silicon dioxide. The silicon dioxide was formed by introducing CO_2 into the reactor upon completion of the deposition of the desired thickness of the epitaxial layer. This dioxide layer was then subjected to a high temperature heat treatment in dry nitrogen gas to improve tenacity of the photoresist chemicals. The slices were then subjected to standard photoengraving methods to open windows in this protective oxide.

2.2.2 Groove etching. Grooves or pockets were then formed by either of these two methods.

2.2.2.1 Anhydrous HCl high temperature etch. Subjecting the slices with windows cut through the protective oxide mask to a mixture of approximately 4% HCl in H_2 resulted in the etching of pockets into the silicon. This generally is a very short time etch, (between 25-50 seconds.)

2.2.2.2 Wet chemical etching process. The slices with windows cut through the protective oxide are mounted face side up on a glass microscope slide with Apiezon wax. They are subsequently exposed with continuous agitation to an etching mixture of HNO_3, HF, H_2O in the ratios of 84:8:8 respectively. This cuts pockets or grooves into the silicon slices. The slices are then cleaned in solvents and other proper methods and introduced into the epitaxial reactor. The ensueing process is then the same as for the Anhydrous HCl Etching Method.

2.2.3 Groove (Pocket) refilling. Immediately following the etch the reactor is allowed to purge and then an epitaxial layer is deposited within the pockets. By controlling the time of both etch and re[illegible] very nearly perfect surfaces are produced. Sample evaluations are carried out by standard methods of angle lapping and staining techniques. Spuriously nucleated silicon growth on the oxide mask may now be removed by HF etching with ultrasonic agitation. This also removes all previously deposited silicon dioxide. Electrical measurements indicated that p-n junction isolation is achieved.

An appendix "Specification for Epitaxial process" which describes in detail the operational procedures is included as Appendix A to this report.

Present state-of-the-art indicates that the Wet Chemical Process is probably more applicable in providing device quality material than the HCl high temperature etching techniques. However, both methods are useful.

3.0 DISCUSSION AND EXPERIMENTAL DATA

3.1 General

The goals of this project were to develop a procedure and provide an epitaxial process specification for back filling with p type material pockets etched into an n type silicon layer.

A further possible goal in conjunction with this program would be to ascertain the compatibility of the process with prior and subsequent operations of MOS-FET device fabrication. This goal will be covered more fully in subsequent tasks of the overall MOS-FET program.

Various experiments were reported previously[1,2,3] which established etch rates and growth rates of silicon by epitaxial methods. Essentially this information was used in organizing a series of experiments to evaluate methods and achieve the goals of the present program.

3.2 Experimental

Cleaned polished slices of silicon were placed in the epitaxial reactor on a quartz protective envelope covering a graphite susceptor. After proper purging with nitrogen and then hydrogen, the slices were heated to 1200°C and then exposed to a mixture of anhydrous HCl in H_2 for for a time sufficient to remove all residual surface damage caused by material polishing operations. (3.1)* (3.2) (3.3)

$$4\,HCl(g) + Si(s) \longrightarrow SiCl_4(g) + 2H_2(g) \qquad \text{Eq. (1)}$$

The slices then received a deposition of N type doped silicon by passing a (3.3.2)

*Marginal numbers indicate Process Specification steps in Appendix A.

mixture of $SiCl_4$, PH_3 and H_2 through the reactor and over the slices which were maintained at a temperature of 1150°C. (See Figure 1)

$$SiCl_4(g) + 2H_2(g) \rightleftharpoons 4\ HCl(g) + Si(s) \qquad \text{Eq. (2)}$$

After the required thickness of doped silicon has been deposited, the dopant impurity is stopped and CO_2 is introduced into the reactor and a layer of (3.3.3) silicon dioxide is pyrolytically deposited on the surface of the slice. (See Figure 1).

$$2\ H_2(g) + SiCl_4(g) = 2\ CO_2(g) \rightleftharpoons 2\ CO(g) + 4\ HCl(g) + SiO_2(s)$$

Eq. (3)

The slices are then heat treated in N_2 for 3 - 10 minutes. (3.3.3.4)

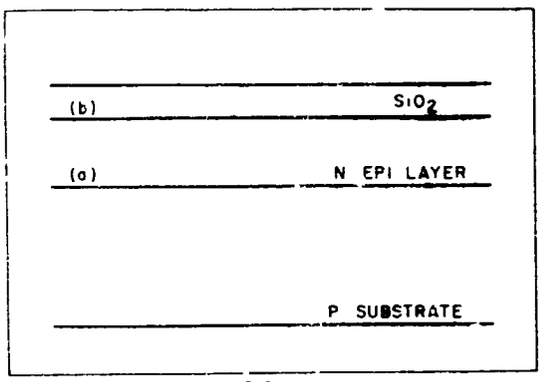
Windows are then cut through this oxide at the desired locations by standard photoengraving methods. (See Figure 2).

Following the window opening operation, either of two methods are used to etch pockets into the exposed silicon: 1) the use of HCl in H_2 at 1200°C (3.3.1) and 2) the use of a wet chemical etch mixture composed of HNO_3, HF, and HAc (3.4) in the volemeteric ratios of 84:8:8. The latter method has thus far proven most effective. (See Figure 3). The high temperature HCl pocket etching has certain inherent associated problems. The bottom of the pocket or the groove assumes a convex lens-shaped cross-sectional profile. The reason for this is probably heat flow difficulties and is geometry dependent as explained in a prior report to NASA (1). Subsequent regrowth of silicon on this surface is single crystalline in structure. However, growth is approximately uniform (3.3.2) and therefore the upper surface of the regrown pocket is a replica of the bottom of the groove and is unsuitable or at least of dubious value for device fabrication.

The wet chemical process using HNO_3, HF and HAc in the volumetric (3.4) ratios of 84:8:8 respectively has proven more useful in etching the pockets into the silicon. Although the cross-sectional geometry is still lenticular in nature, it is not as pronounced as with the anhydrous HCl high temperature etching. The upper surface of the regrown area is therefore of better quality and capable of being used for device fabrication.

Following the pocket etch, the slices are again placed intc the reactor and a layer of silicon is deposited over the exposed silicon. (3.3.2) (See Figure 4). There is spurious growth of silicon on the surface of the oxide. However, this is removed by exposing the slice to HF at 48% with ultrasonic agitation. (See Figure 5). Tests of Breakdown Voltage from pad to pad indicate that electrical isolation is achieved.

Figures 6, 7, and 8 show the actual groove etched, and the surface quality respectively of slices prepared in this manner.



FIG

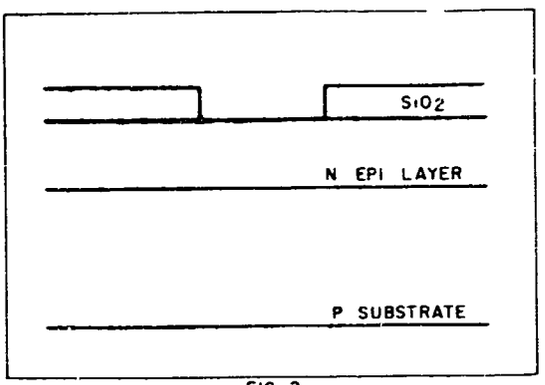


FIG 2

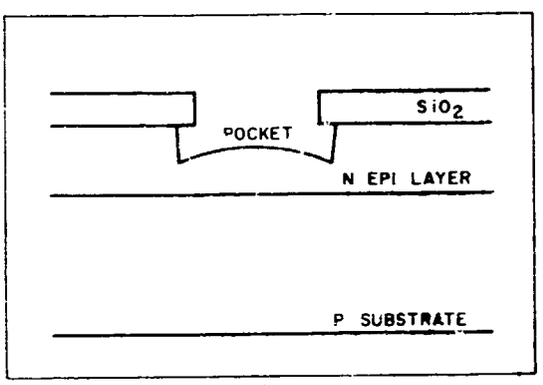


FIG 3

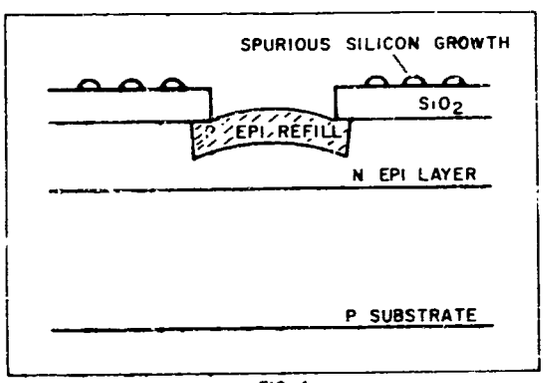


FIG 4

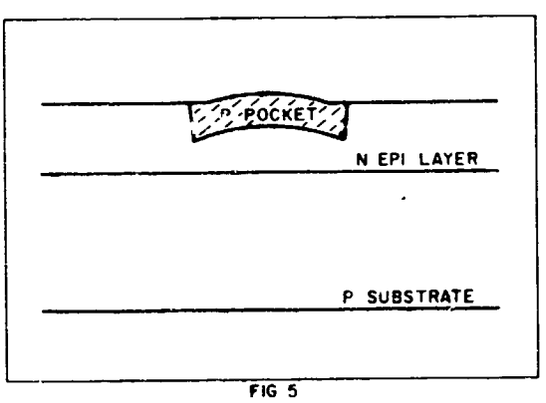


FIG 5

Figure 1. Epitaxial Layers of Silicon (a) and Silicon Dioxide (b) Deposited on Substrate that has been Polished and Etched in HCl Gas at 1200°C.

Figure 2. Windows Cut Through SiO_2 Layer Exposing Silicon.

Figure 3. Pocket Etched into Silicon.

Figure 4. Pocket Refilled with Single Crystalline Silicon. Silicon is P Type.

Figure 5. Pocket Remaining After Removal of Silicon Dioxide and Spuriour Silicon Deposition.

Figure 6. Photo Showing Pocket Etched Through Oxide Mask Into N-Type Silicon. Pocket = 0.020" wide

Figure 7. Photo Showing Pocket Refilled With P Type Silicon. Pocket = 0.020" wide

Figure 8. Photo Showing Top Surface of Pocket Refill After Deposition. (0.020" x 0.020")

4.0 CONCLUSIONS AND RECOMMENDATIONS

It is feasible to provide pockets of "p" type silicon in n-layers of silicon such that the overall slice is capable of being used to make complementary MOS-FET devices. A wet chemical etch is considered to be preferable to a high temperature HCl etching procedure.

A set of specifications for etching and epitaxial processes is included as an appendix to this report.

5.0 NEW TECHNOLOGY

A method and process for providing material for monolithic complimentary MOS-FET structure with P-N junction isolation is defined in this report.

6.0 REFERENCES

1. First Interim Report for Phase I Groove Etching Study, Westinghouse Electric Corporation, Contract No. NAS 5-3758, W. O. No. 670-190-5, January 1965.

2. Interim Progress Report for Phase II of Groove Etching Study, Westinghouse Electric Corporation, Contract No. NAS 5-3758, Procurement No. 670-W46374 Westinghouse G. O. 51248-AQ1A, 1 April 1965.

3. Final Report for Phase III of Groove Etching Study, Oxide Barrier Isolation, Westinghouse Electric Corporation, Contract No. NAS 5-3758, Procurement No. 670-WA6712, Westinghouse G.O. 51248-AN1A, 1 June 1965.

APPENDIX A

Specification for Epitaxial Processes

1. Equipment
   - 1.1 Gas control panel
   - 1.2 Epitaxial reactor
   - 1.3 RF generator
   - 1.4 Optical pyrometer
   - 1.5 4-point probe
   - 1.6 Angle lapping equipment
   - 1.7 Interference fringe apparatus
   - 1.8 Surface hydrogen purifier
   - 1.9 Tweezers
2. Material
   - 2.1 Silicon tetrachloride
   - 2.2 Diborane in H_2(100 PPM)
   - 2.3 Silane in H_2 (100 PPM)
   - 2.4 Arsine in H_2 (100 PPM)
   - 2.5 Hydrogen
   - 2.6 Nitrogen
   - 2.7 Carbon dioxide (Coleman grade)
   - 2.8 Graphite susceptor
   - 2.9 Quartz envelope

2.10 Quartz sled

2.11 Silicon slices (previously polished and cleaned)

2.12 Petri dishes Pyrex

2.13 Lint free paper

2.14 Trichloroethylene

2.15 HF

2.16 HNO_3

2.17 HAc

2.18 Cotton balls

2.19 Anhydrous HCl

3. Procedure

3.1 Cleaning Process

3.1.1 Place slices of silicon in petri dish.

3.1.2 Cover slices with Trichloroethylene (TCE). Note: Slices must not be allowed to become exposed to air by Trichloroethylene evaporation; must be kept covered until removal.

3.1.3 Remove a slice; place on at least three thicknesses of lint free paper.

3.1.4 With plastic squirt bottle apply a small amount of TCE.

3.1.5 Swab slice with cotton swab or ball to physically remove any trace of foreign particle.

3.1.6 Place slice in clean petri dish (bottom of dish to be covered by disc of lint free paper.)

3.1.7 Repeat steps 3.1.3 thru 3.1.6 until all slices have been cleaned.

3.2 Loading Boat and Reactor

3.2.1 Assemble graphite susceptor into quartz envelope.

3.2.2 Place assembly on sled.

3.2.3 Place slices of silicon on boat centered properly along midline.

3.2.4 Introduce sled and boat assembly with slices in reactor tube and center boat within extremes of RF load coil.

3.2.5 Replace end cap and start purge of reactor tube with N_2.

3.3 Epitaxial Processes

3.3.1 Vapor Etching by HCl

3.3.1.1 Purge reactor tube of all atmospheres by nitrogen flow. (At least 3 minutes).

3.3.1.2 Purge reactor tube of all nitrogen by hydrogen. (At least 3 minutes).

3.3.1.3 Turn on RF generator and allow temperature to reach 1200°C. Temperature is checked by Optical Pyrometer.

3.3.1.4 Set H_2 flow to desired rate.

3.3.1.5 Start HCl flow to desired rate and set timer to desired etch time; allow etch to proceed for this time.

3.3.1.6 Stop HCl flow after completion of time, allowing only H_2 to flow through reactor. If HCl etch only desired, move to step 3.3.2.5.

3.3.2 Epitaxial Deposition of Silicon

3.3.2.1 Set temperature to 1150°C.

3.3.2.2 Set gas flow rates (according to desired doping levels) for H_2 flow through $SiCl_4$ bottle (H_2 bypasses $SiCl_4$ bottle) and for doping gases as desired. (Arsine or phosphorus for N type and diborane for p type) the gas flows of doping gases are directed to exhaust.

3.3.2.3 Start flow of H_2 thru $SiCl_4$ bottle and direct doping gas flow from exhaust to reactor. (Set timer for desired length of time.) Allow deposition to continue for length of time necessary to deposit desired thickness of layers.

3.3.2.4 Stop H_2 flow thru $SiCl_4$ and direct doping gas from reactor to exhaust.

3.3.2.5 Allow reactants to purge from reactor by H_2 flow. (At least 2 minutes).

3.3.2.6 Turn off RF generator and allow reactor to cool. Turn off dopant supplies.

3.3.2.7 Purge H_2 from reactor with nitrogen (at least 2 minutes).

3.3.2.8 Slices may be removed from the reactor by removing sled and boat assembly.

3.3.2.9 Place slices in clean petri dish on clean lint free paper.

3.3.2.10 Evaluate test slices for layer thickness and resistivity. By 4-point probe and thickness evaluation equipment.

3.3.3 Oxide Deposition - If an oxide layer is desired for masking or protection, follow procedure of epitaxial deposition 3.3.2 thru step 3.3.2.3, then proceed with the following:

3.3.3.1 Allow H_2 flow to continue through $SiCl_4$ bottle; divert doping gas from reactor to exhaust; start and set CO_2 flow to reactor and start timer for desired time and thickness.

3.3.3.2 Allow to proceed for desired time.

3.3.3.3 Stop H_2 flow through $SiCl_4$, stop CO_2 flow to reactor, maintain temperature (1150°C)

3.3.3.4 Stop all H_2 flow to reactor and introduce nitrogen flow.

3.3.3.5 Allow nitrogen to flow for time required.

3.3.3.6 If this is final step, proceed according to the following:

3.3.3.7 Turn off RF generator and allow reactor to cool.

3.3.3.8 Remove slices per 3.3.2.8 thru 3.3.2.10.

3.3.4 Polycrystalline silicon deposition (one oxide). If a polycrystalline layer is desired over the oxide continue oxide deposition (3.3.3) up to step 3.3.3.4 and then proceed with the following.

3.3.4.1 Continue nitrogen flow through the reactor for at least three minutes minimum.

3.3.4.2 Stop nitrogen flow; start H_2 flow and purge nitrogen from the reactor.

3.3.4.3 Start H_2 flow through $SiCl_4$ at the setting desired to deposit silicon at the proper rate. Set timer.

3.3.4.4 Allow deposition to proceed for time necessary.

3.3.4.5 Stop H_2 flow through $SiCl_4$.

3.3.4.6 Allow H_2 to purge reactor. (At least 2 minutes).

3.3.4.7 Turn off RF generator.

3.3.4.8 Proceed to cool down and remove slices according to steps 3.3.2.7 thru 3.3.2.9.

3.4 Groove Cutting by Wet Chemical Method

3.4.1 Slices with windows cut through the second epitaxially grown (thermal) oxide are mounted on a glass slide by apiezon wax (black wax). Care must be taken to keep wax fror face of the wafer.

3.4.2 A mixture of HNO_3, HF and HAc is prepared in the ratios of 84:8:8 respectively.

3.4.3 The mounted slice is introduced to the acid mixture and etched (with constant agitation) until the original oxide layer is exposed. (This will be noted by the reflection being very clear).

3.4.4 The slice is now removed fr m the acid mixture and cleaned in D.I. water for at least 5 separate rinses.

3.4.5 The slices are submerged in HF (48%) until all the overhanging silicon dioxide has been removed. (This also can be detected visually).

3.4.6 Slices are removed from glass slide and cleaned by organic solvents prior to continuing subsequent operations.