X-611-65-489

NASA TM X-55406

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GPO PRICE $ _____

CFSTI PRICE(S) $ _____

Hard copy (HC) 1.00

Microfiche (MF) .50

ff 653 July 65

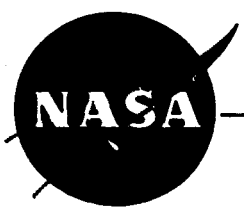
FACILITY FORM 602

N66-17239 (ACCESSION NUMBER) (THRU)

23 (PAGES) 1 (CODE)

(NASA CR OR TMX OR AD NUMBER) 14 (CATEGORY)

OCTOBER 20, 1965



GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND

A Digitized Spark Chamber for Gamma Ray Astronomy

by
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N66172 39

Abstract

A digitized spark chamber has been developed for balloon borne and satellite gamma ray astronomy. The detector is a multi-array wire, plate chamber utilizing magnetic cores for buffer storage and magnetic tape for data logging. The high voltage system consists of a set of gas krytrons triggered by avalanche transistor pulsers. Track information is stored in parallel into a ferrite core array mounted to the chamber face and buffered via a linear select memory system into a sixteen track sub miniature tape recorder for bulk storage.

Also included is a 16 channel rate meter and housekeeping multiplexer which interleaves data with track information onto the tape recorder. The package is designed to operate for long periods of time on a single charge of neon-helium gas in a free balloon environment.

Author

Introduction

A digitized spark chamber has been developed for balloon borne gamma ray astronomy by the method of electron positron pair productions. This paper will present a brief description of the detector array and high voltage system and a thorough treatment of the associated data acquisition and data handling systems.

Detector

The detector (figure 1) consists of two sixteen section plate-wire grid chambers, a thin central Pilot B scintillator and a quartz Cerenkov radiator housed in a gas tight vessel and covered by a large Pilot B anticoincidence dome [1].

The detector will be flown in an oriented gondola using a fluxgate magnetometer for direction sensing and gas reaction jets for propulsion. The pointing accuracy requirement of the gondola and detector configuration are implicit in the physics of the experiment and are beyond the scope of this paper.

The chambers are six inches square, the plate consists of a .02 radiation length gold aluminum sandwich absorber and the grid of 128 .007" diameter beryllium copper wires on .047 inch centers, with plate grid spacing approximately .093 inches, and operating at one atmosphere in 90% neon and 10% helium, with argon added for Penning effect.

The plates are formed by annealing the aluminum stock between flat stainless steel plates, and then plating .002 inches of gold onto either side. They are held flat by riveting stretcher bars to each of the four edges

while the plate is held under tension in a fixture, a tab being left on one corner for the high voltage feed point.

The wire grids are made on machined glass bonded mica frames by cementing copper pins, positioned by glass bonded mica locator jigs, into grooves in the frame, and then ultrasonically welding the wires to them.

Glass bonded mica[2] was chosen as a frame material for its low outgassing rate, high dielectric strength, and relative ease of machinability.

The chamber is assembled by clamping wired frames, plates, and appropriate filler bars, to maintain proper electric field distribution, in a steel fixture.

The memory cores [3] are located directly at the ends of the spark wires and are supported in small shelves which also contain current limiting resistors and the readout sense wires. (Figure 2)

The coincidence system consists of the plastic anticoincidence dome (A) viewed from the base by six RCA CF 7151 PM tubes whose outputs are summed, a 1/8" thick central plastic scintillator edge viewed, through a curved lucite light pipe, by an RCA CF 7151 PM tube positioned beside the chamber (B) and a 5" diameter EMI 9530 QA photomultiplier with a ¼" thick quartz Cerenkov radiating face coated to make it unidirectional (C).

The chamber may be fired on either an $\bar{A}BC$ or $\bar{A}C$ event through a fast coincidence system with a time resolution of 200 nsec and a total delay time of less than 50 nsec. The coincidence output is fed to both the high voltage pulsers and to the memory scan electronics. The coincidence system also provides counting rate and coincidence rate outputs to the housekeeping data multiplexer.

The high voltage system consists of a set of avalanche transistor drivers transformer coupled to the grids of the thyratron high current[4] pulsers. Eggerton, Germeshausen and Grier KN 2 krytrons are used with an 800 volt grid driving pulse and 2.4 KV plate supply to give a 20 ns rise time 2.2 KV negative going pulse at the plate, with a total of 50 nsec delay time. These tubes, though quite satisfactory for balloon work, have useful lives of only several weeks making them unsuitable for satellite experiments. Work is under way to perfect a solid state pulser which will not be troubled by lifetime problems.

Data System

The data system consists of a buffered memory scan system, a housekeeping data handling system, and a tape multiplexer and recorder.

The core memory is arranged as a 256 word linear select memory with a sixteen bit word length. This arrangement was chosen as the minimal hardware configuration, while providing a high readout rate and good output S/N ratio[5].

A memory addressing system may be built of n selecting devices, where n is m times the mth root of the number of cores and m is the dimension of the selecting matrix, that is if each core is described by three co-ordinates the number of selecting devices which must be utilized is equal to 3 times the cube root of the number of cores in the set. In our case there are four thousand ninety six cores so for a three dimensional select matrix forty-eight select devices are needed. For a conventional coincident current memory which is a two dimensional system 256 select devices would have been required.

Each core in the system is threaded by 3 wires; the first being a spark wire which threads one core only and carries current of polarity to set the core, the second is a reset wire threading 16 cores, one per chamber plate, and carrying current to reset the core, and the third is a sense wire, threading all 256 cores associated with each x-y plate pair, which senses core change of state. The reset wires are further arranged in a matrix (figure 3) with 16 shockley diode current sources, which provide 0.8 ampere, 1 μsecond, pulses and 16 current sinks constituting the select elements, thus by firing one source with only one sink conducting a single reset wire may be selected, reading the contents of 16 cores into their associated sense wires. These wires are thansformer coupled to tunnel diode thresholded, single ended, sense amplifiers which detect the 0.5 volt output pulses from the set cores (figure 4). At pulse time the states of these amplifiers are strobed into a 16 bit shift register forming the third dimension of the select system.

A coincident current memory in the same application would have required four wires per core; one spark wire and a sense wire serving the same purpose as their counterparts in the existing system, and two drive wires each carrying half the core reset current, to read out a single core. This would have produced two hardware inefficiencies; first an extra wire would have had to have been threaded through each core; and second, since the reset current would have been only slightly larger than minimum switching current, and since core output is a strong function of drive current, much more sophisticated sense amplifiers would have been required.

A 12 bit scaler is used to decode the core location (figure 5). The first four bits decode the contents of the last bit of the shift register, the second four the current pulser last fired and the third four the current sink selected thus defining the core being read out.

In operation, a delay is initiated on coincidence to allow spark transients to die away, all scalers are reset to zero, the shift register is cleared, and the first reset wire is fired. Shift pulses are counted until a set core is found, inhibiting counting and shifting until the address of the set core is recorded. Shifting then resumes. After each 16th shift pulse the contents of the next column of cores is loaded into the shift register. The process continues in this manner until all cores have been examined, freeing the chamber for the next event. This method of scanning was chosen over simply recording the contents of all cores because in any single event the number of fired cores will be small, and only 12 bits of data need be stored for each fired core, as against 4096 bits if all cores were fired.

Further recording efficiencies could have been implemented by recording only the first of a group of adjacent set cores and the number of such cores in the group, and by immediately firing the next readout wire if all cores strobed by any wire had been zero. It was determined however, that with the existing scan and counting rates dead time would be low at balloon altitude, chamber scan time being $(1 + n/16)$ seconds, where n is the number of set cores.

Housekeeping Data System

It is also desirable to monitor counting rates of the coincidence detectors, chamber live time, and such parameters as pointing accuracy and direction of the balloon gondola, power and orientation fuel consumption, chamber gas pressure and temperatures. To this end a 16 channel digital and analog data handling assembly has been constructed (figure 6).

The system provides 8 channels of digital pulse counting and an 8 position analog multiplexer and ADC.

The binary accumulators are 8 bits in length providing counting accuracy of one part in 256. Digital prescalers are provided to scale down counting rates so that the accumulators will not overflow during the counting interval. Individual detector, double, and triple coincidence rates are monitored. In addition the coincidence conditions for any analyzed event are stored in three fixed core locations and recorded during memory scan.

One of the accumulators serves as a live time counter accumulating time in minutes with a 1/16 second precision.

The analog to digital converter also accurate to 1 part in 256, is used to moniter voltage transducers for recording the other housekeeping parameters.

The housekeeping multiplexer, memory scan system, live time clock, ADC, and tape recorder all operate from a common frequency source consisting of a 16 kc crystal oscillator and digital countdown chain. Memory scan frequency being 4 kb, ADC rate 1 kb and record rate 32 bps.

Data is logged in parallel onto a 16 track write only recorder developed at GSFC. Recording rate is 32 words per second and tape speed is .375 ips. The recorder system interleaves housekeeping information with core information when available. Two tracks are used as selective strobes, one firing when core information is present, the other for housekeeping data (figure 7).

The core words are 13 bits in length - twelve for core address and one for a scan-ready mode indicator.

The housekeeping words are 12 bits in length - 8 data bits and 4 bits of channel address. It was decided to record all channel addresses rather than decode them to simplify ground data reduction.

The housekeeping multiplexer is run synchronously with the recorder and completes a scan of all 16 channels in one second. Core data is recorded whenever available and a signal is returned to the scan electronics when recording is complete so that scanning may continue.

The system is completed by a compact ground data handling console small enough to be carried into the field which produces strip chart records of housekeeping data and either an oscilloscope display or photographic facsimile of individual chamber events.

Acknowledgement

It is a pleasure to acknowledge the participation of the many GSFC personnel who contributed to the design of the detector instrumentation, in particular Mr. R. W. Ross for the high voltage and coincidence systems, Mr. R. L. Smith for his assistance with the logic design, and Messrs. J. O'Conners, L. Martinez and L. Himmelstein for the mechanical design.

Footnotes

1. T. L. Cline, C. E. Fichtel, GSFC Proposal, February 1965.
2. General Electric Company's Mycalex.
3. Electronic Memories Inc. Type 51-114.
4. R. W. Ross, unpublished.
5. Bownin, Newman, Miller and Sherrard, Institute for Computer Research, University of Chicago Report.

Figure Captions

Figure 1 - Gamma Ray Telescope - Detector Array

Figure 2 - Wire Grid and Core Shelf Structures

Figure 3 - Spark Chamber Memory Arrangement

Figure 4 - Sense Amplifier

Figure 5 - Memory System Block Diagram

Figure 6 - Data Multiplexer Block Diagram

Figure 7 - Tape Format

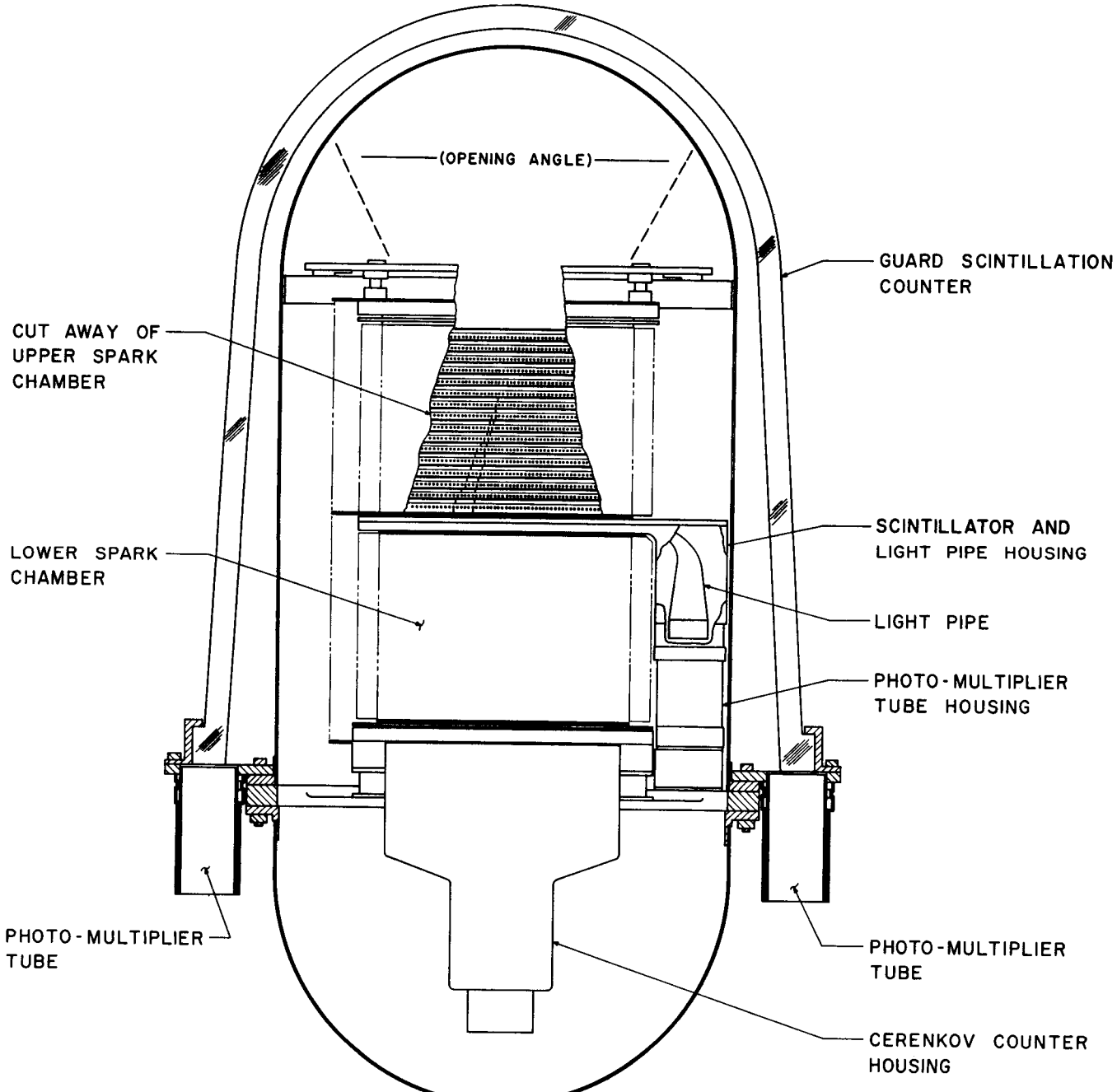

(OPENING ANGLE)
GUARD SCINTILLATION COUNTER
CUT AWAY OF UPPER SPARK CHAMBER
LOWER SPARK CHAMBER
SCINTILLATOR AND LIGHT PIPE HOUSING
LIGHT PIPE
PHOTO-MULTIPLIER TUBE HOUSING
PHOTO-MULTIPLIER TUBE
PHOTO-MULTIPLIER TUBE
CERENKOV COUNTER HOUSING

Figure 1

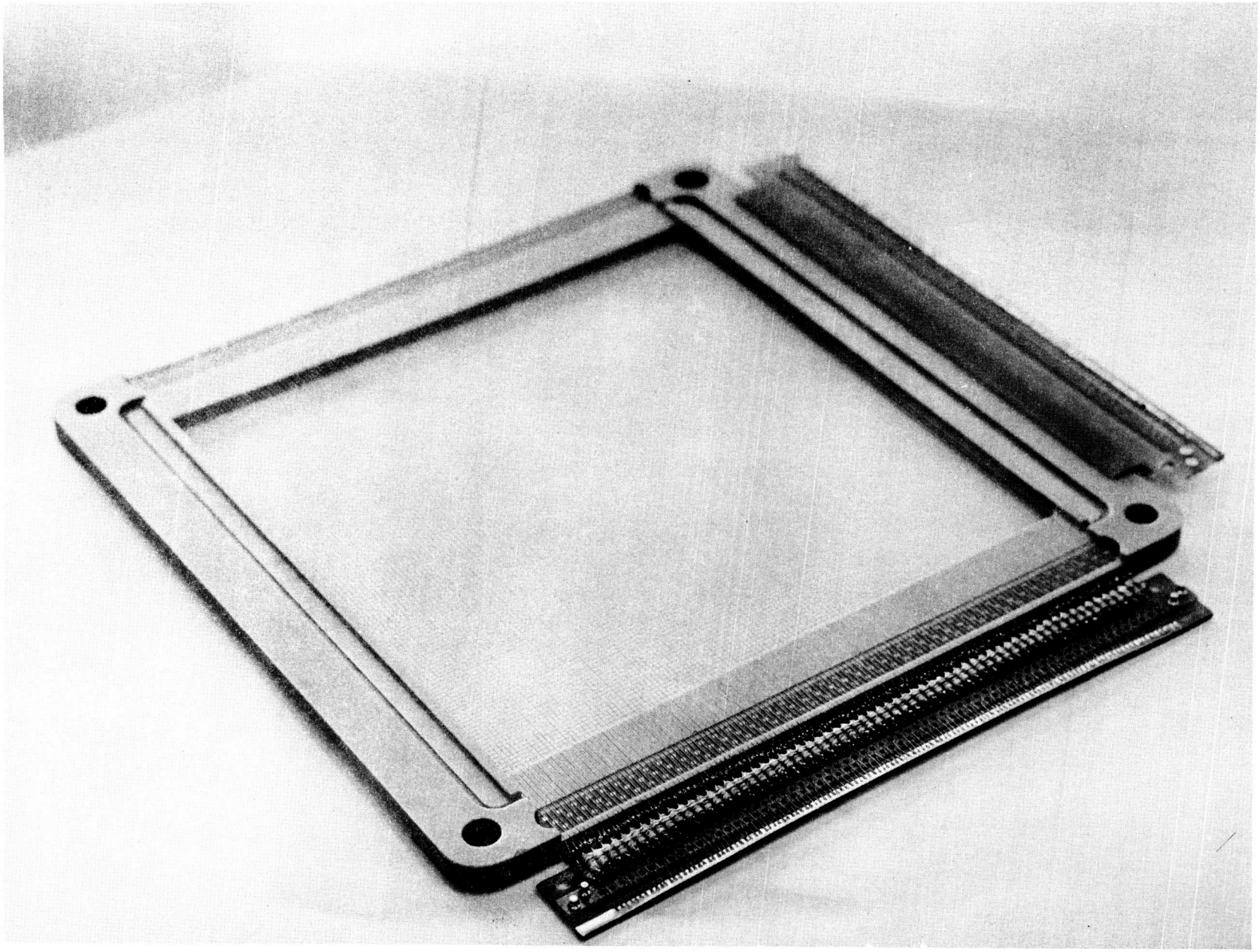


Figure 2

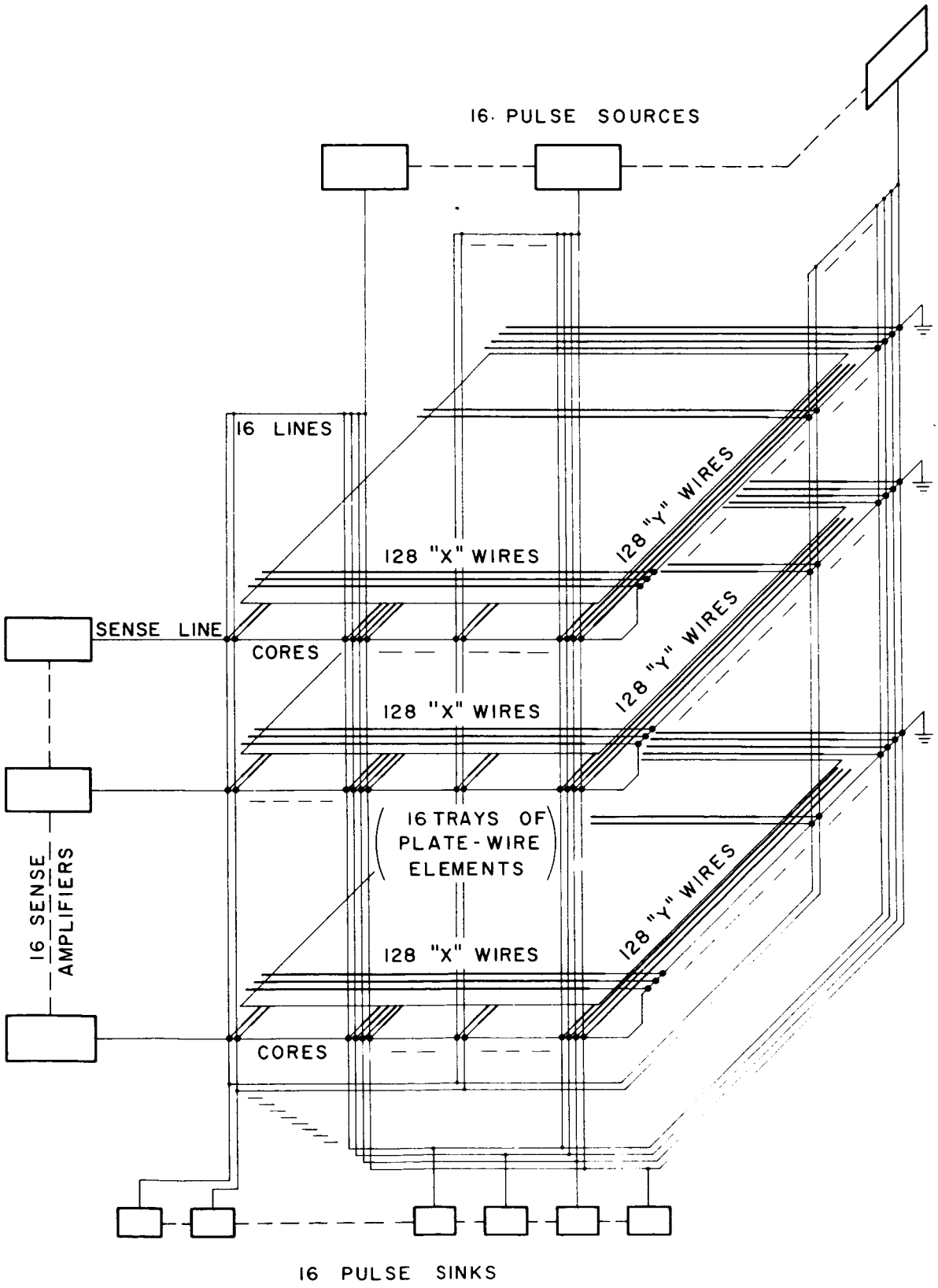
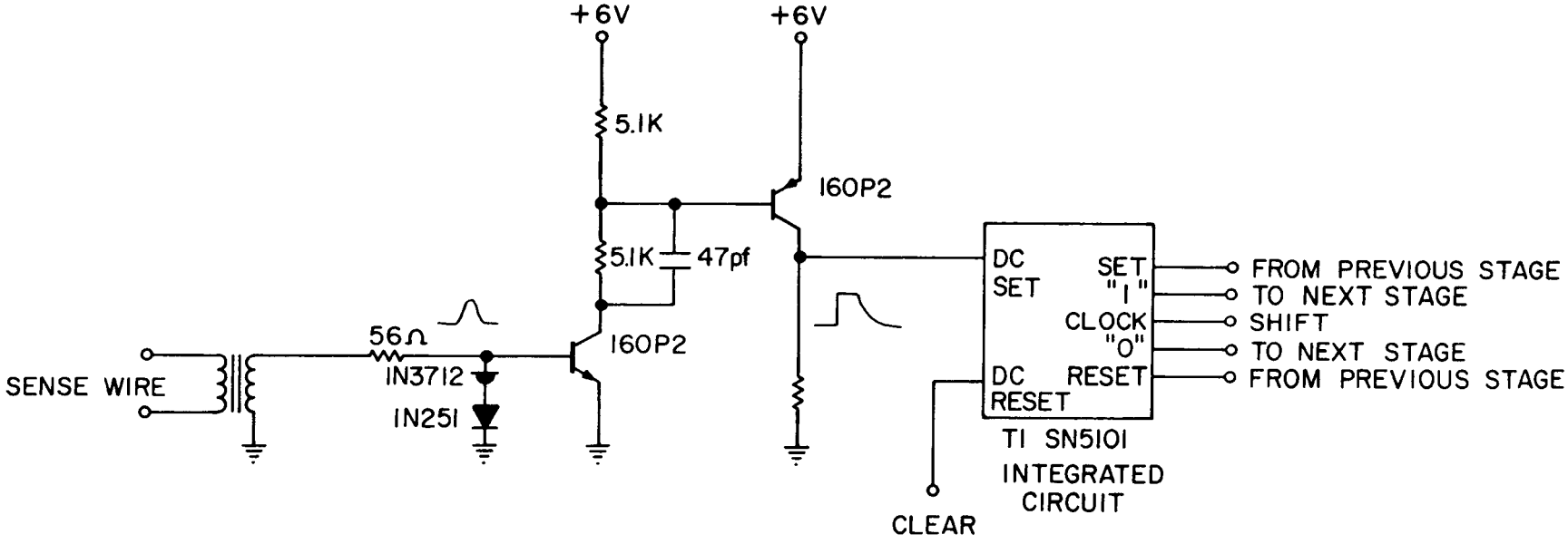
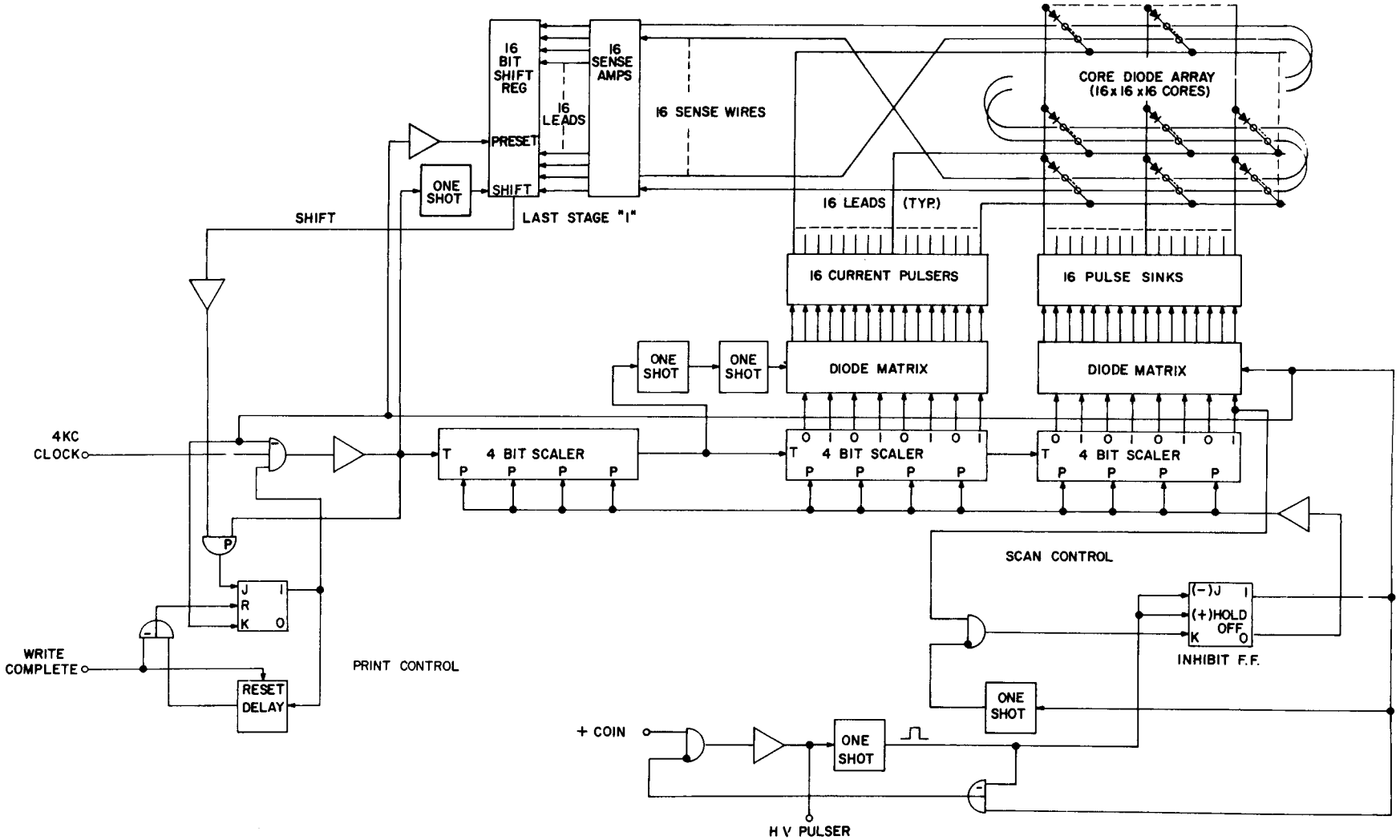

16 PULSE SOURCES
16 LINES
128 "Y" WIRES
128 "X" WIRES
SENSE LINE
CORES
128 "Y" WIRES
128 "X" WIRES
16 TRAYS OF PLATE-WIRE ELEMENTS
16 SENSE AMPLIFIERS
128 "Y" WIRES
128 "X" WIRES
CORES
16 PULSE SINKS

Figure 3



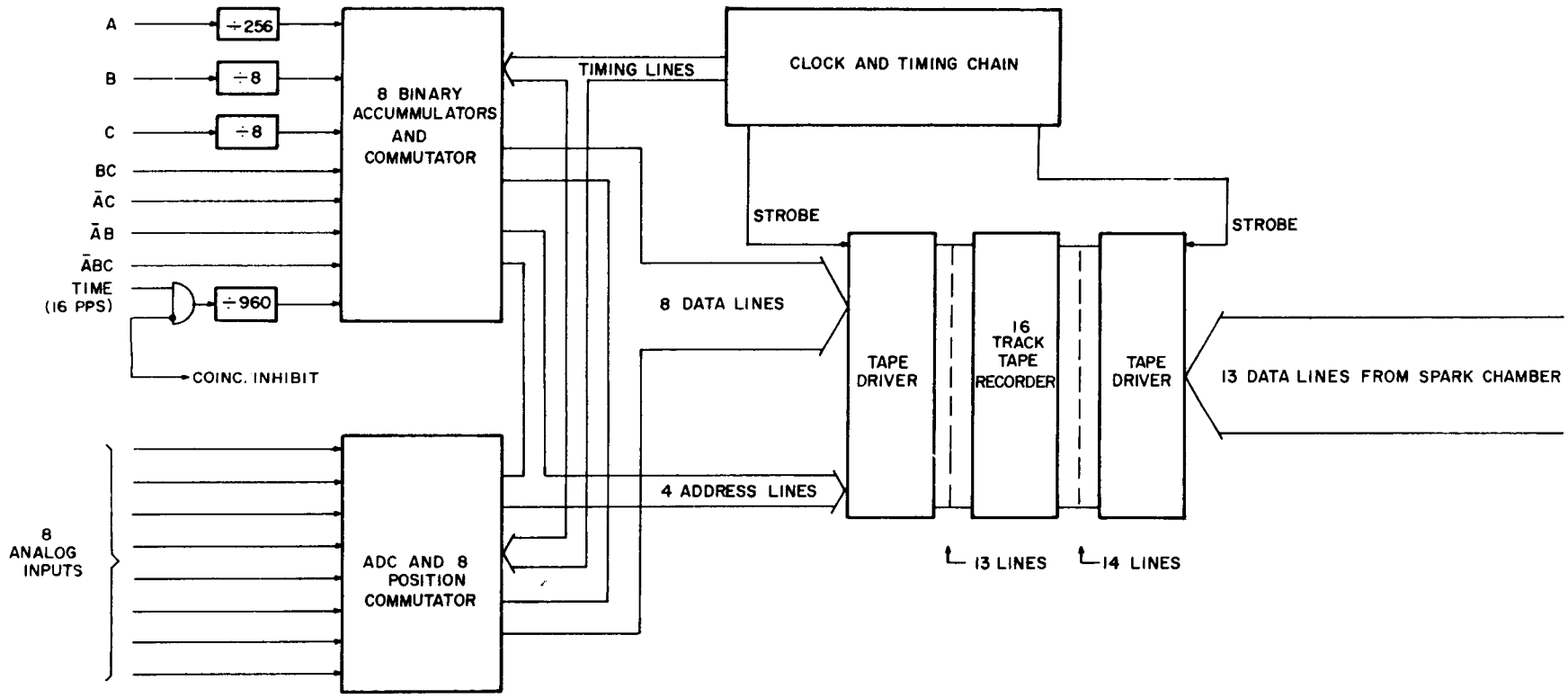
SENSE AMPLIFIER

Figure 4



SCAN ELECTRONICS BLOCK DIAGRAM

Figure 5



MULTIPLEXER BLOCK DIAGRAM

Figure 6

DATA BIT #1	ADDRESS BIT #1		TRACK #1	
DATA BIT #2	ADDRESS BIT #2		TRACK #2	
DATA BIT #3	ADDRESS BIT #3		TRACK #3	
DATA BIT #4	ADDRESS BIT #4		TRACK #4	
DATA BIT #5	ADDRESS BIT #5		TRACK #5	
DATA BIT #6	ADDRESS BIT #6		TRACK #6	
DATA BIT #7	ADDRESS BIT #7		TRACK #7	
DATA BIT #8	ADDRESS BIT #8		TRACK #8	
HOUSEKEEPING STROBE			TRACK #9	
	CORE STROBE		TRACK #10	
PARAMETER BIT #1	MODE FLAG		TRACK #11	
PARAMETER BIT #2	ADDRESS BIT #9		TRACK #12	
PARAMETER BIT #3	ADDRESS BIT #10		TRACK #13	
PARAMETER BIT #4	ADDRESS BIT #11		TRACK #14	
	ADDRESS BIT #12		TRACK #15	
			TRACK #16	
HOUSEKEEPING WORD	CORE WORD	HOUSEKEEPING WORD	CORE WORD	

TAPE FORMAT

Figure 7