FINAL REPORT ON

NASA CR70591

S-BAND ODOP TRANSPONDER

Prepared for

GEORGE C. MARSHALL SPACE FLIGHT CENTER

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

HUNTSVILLE, ALABAMA

CONTRACT NO. NAS8-11509

CONTROL NO. TP 3-83548

RESDEL ENGINEERING CORPORATION

990 SOUTH FAIR OAKS AVENUE, PASADENA, CALIFORNIA

REC-TR-15

FINAL REPORT ON

S-BAND ODOP TRANSPONDER

Prepared For

GEORGE C. MARSHALL SPACE FLIGHT CENTER

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

Huntsville, Alabama

CONTRACT NO. NAS8-11509

CONTROL NO. TP 3-83548

Prepared By

James R. Pourtales

OF

RESDEL ENGINEERING CORPORATION

Pasadena, California

ABSTRACT

18426

This document is the final report on an S-Band ODOP Transponder, Resdel Model 91242, with offset input and output frequencies of 2113 5/16 to 2295 mc. This transponder was developed by Resdel for the Marshall Space Flight Center, Huntsville, Alabama, under contract No. NAS8-11509 (Control No. TP 3-83548). The major effort of the program was the study, design, and development of a prototype transponder intended primarily for booster tracking. The design included advancements in the state-of-the-art in high temperature design with small size, high power at 100 mc frequencies, efficient VHF to UHF varactor multiplications, extremely low dynamic phase shift IF amplifiers, fast acquisition capabilities, and increased system response with stability by elimination of AGC signal loops. The end-product is a transponder from which future units can be directly manufactured.

The report contains a description of the equipment and its theory of operation with schematic diagram, block diagram, drawings, photographs, and test procedures. A bibliography of applicable specifications, drawings, and references is included. A two weeks course with a prepared text on Phaselock Techniques was also given at Huntsville, Alabama. This included the preparation, literature research, and presentation to NASA engineers and scientists.

TABLE OF CONTENTS

TABLE OF CONTENTS (con't.)

LIST OF ILLUSTRATIONS

SUMMARY

The primary result of this contract has been the design and development of an advanced prototype S-band phase-coherent transponder primarily intended for Booster tracking purposes in the Saturn Missile Program.

The design and construction is quite versatile so that additional features can be added without a completely new design concept required. This is extremely important from the standpoint of follow-on work in the Saturn program wherein mission requirements are liable to change and fast reaction to these changes is mandatory. As an example, in the latter stages of this contract the mission requirement changed to add ranging, increased sensitivity, and certain telemetry features. By simply combining two housings physically together these requirements could be handled expeditiously without a great deal of basic redesign.

The accomplishments under this contract have represented significant advances in the state-of-the-art. Among these are:

1. Novel IF Amplifiers with excellent limiting characterisitics and small dynamic phase shifts.

2. Elimination of AGC loops in the transponder system design and thereby eliminating dependence of acquisition and acceleration capabilities on AGC response.

3. Improved self-acquisition capability where automatic lock-on over a wide signal range is possible in 1/10 second. This is especially important in Booster tracking since large signal fluctuations are liable to cause loss of signal and it is mandatory to reacquire in as short a time as possible.

4. High temperature design where this rather complicated transponder system operates at 100°C. All components are also safely derated in most instances by 50% or more.

5. The almost complete elimination of interior connectors. The entire transponder has only three interior cables with connectors. This materially increases the reliability.

6. Ability to handle large input signals. The transponder will handle +5 dbm signals.

Included in the efforts is a report dealing with AGC versus limiting as a means for gain control (see Section 7). An exceptional portion of this report is the section written by Mr. Richard Jaffe where an extensive theoretical analysis is made of limiting and AGC gain con-

trols and their relationships with possible false lock conditions.

The transponder prototype included a separate housing enclosing all of the power supply. (See Section 3 for further discussions of the power supply).

A significant portion of this contract was the preparation and delivery of a phaselock course to MSFC personnel. This represented an achievement that for the first time to our knowledge, phaselock techniques were gathered together in one volume. In the past, phaselock literature has been quite selective into very narrow applications.

Section 1

INTRODUCTION

1.1 Scope of Report

This document is the final report on an S-Band ODOP Transponder developed by Resdel Engineering Corporation for the Marshall Space Flight Center, Huntsville, Alabama under contract no. NAS8-11509 (control no. TP3-83548) dated 29 June 1963. The report is comprised of: detailed descriptions of the transponder system; procedures for testing of the transponder; discussions of unique areas; a bibliography listing specifications, drawings, reports and other data pertinent to the program (the items in the bibliography are not supplied as part of this report).

1.2 Scope of Program

The program began as an effort to undertake two phases: I. preliminary design and calculations necessary to determine an optimum system to meet the requirements as stated in the contract, II. detail design and fabricate one engineering prototype transponder and three final transponders. The results of the preliminary design effort of phase I are contained in "Preliminary Study Report". (See the bibliography). This resulted in modification 2 to the contract outlining the specifications and some desing goals. (Modification 1 added in-process design and end-item inspection requirements). Modification 3 was added incorporating a change of scope and adding Phase III: to develop and conduct a course in Phaselock Techniques. One of the results of Phase III is the book "Theory of Phaselock Techniques as Applied to Aerospace Transponders".

Phase II of the contract was continued based on the specifications of the preliminary study. The essential history and program of phase II is contained in "Progress Reports 1 through 16" and "Special Technical Report No. 1". In the latter stages of phase II the fabrication of the three final transponders was cancelled as a requirement of the contract. The end product of phase II was the prototype transponder incorporating several state-of-the-art features with advanced capabilities intended primarily for Booster tracking.

Section 2

SYSTEM DESCRIPTION

2.1 General Description and Specifications

This transponder is a phaselocked offset frequency type with an offset frequency ratio of 221/240 and an input frequency of 2113-5/16 mc. It is completely transistorized and is constructed to provide long term reliability, minimum weight, volume, and power consumption, and construction for very rugged missile environments. The characteristics of the transponder are listed below.

2.1.1 Electrical Specifications (Resdel Model 91242)

Input Frequency: 2113-5/16 mc
Output Frequency: 2295 mc
In/Out Freq. Offset Coherent Frequency Ratio: 221/240
Minimum Input Sensitivity for Phase Tracking error of 30°: -120 dbm
Maximum Input Signal: +5 dbm
Minimum Power Output: 1 watt
Primary Input Voltages: 25 to 31 volts DC, isolated from case ground
RF Input and Output Impedance: 50 ohms nominal
Load: 2295 mc output shall oeprate into a VSWR of 1.5:1.
RF Input and Output VSWR: 1.5:1 maximum
Telemetry Test Points:
1. Input Signal Level
2. Static Phase Error Voltage
3. Lock Indication

Outputs are double ended and isolated from case ground such that either end may be grounded. Outputs are 5 volts maximum when operating into a 100 kilohm load. The operation of the transponder is not affected by short circuits on the outputs.

Threshold Loop Bandwidth: approximately 1000 cycles.
Lock-On Bandwidth: $\pm$ 250 kc
Reacquisition Time: approximately 0.5 seconds maximum
RFI: MIL-I-6181D
Input Tuning Range (Factory Tuned): 2113-5/16 $\pm$ 5 mc
Primary Power: approximately 85 watts

2.1.2 Mechanical Specifications

Volume: approximately 250 in^3
Weight: approximately 11 pounds
Construction:
1. Serviceable by competent Engineering personnel
2. All solid state

3. Solid mounting to Heat Sink with no shock mounts.
4. Pressurized with Dry Nitrogen

2.1.3 Environmental Specification

Temperature: -20°C to +85°C with capability of operation to +100°C
Vibration: 21g rms random noise for 4 seconds, 12g rms for 3 minutes, 7.5g rms for 6 minutes, in three mutually perpendicular planes.
Shock: 50g peak for 6 to 11 millisecond duration of half sine wave.
Altitude: Space vacuum.

2.2 General Technical Discussion and Theory of Operation

A block diagram is shown in Figure 2-1 disclosing the essentials of the S-Band Transponder system. A brief explanation of the operation is as follows: The interrogating frequency, 2113-5/16 mc is converted to 47-13/16 mc at the 1st mixer whose L.O. is derived from a stable VCXO at 19-1/8 mc multiplied by 108. The 47-13/16 mc IF is then converted to a 9-9/16 mc IF at the 2nd mixer whose L.O. is derived from the same VCXO frequency multiplied by 3. The 9-9/16 mc IF frequency is phase compared with 1/2 the VCXO frequency. Any phase difference outside the quadrature reference will produce an error signal output. This error signal is then processed in a loop filter whose output controls the VCXO, thereby completing a multiple loop phaselock system. The VCXO frequency is therefore phaselocked to the interrogating signal and will follow its change due to doppler shift by the multiplication of 1/108th. The VCXO frequency then is multiplied by 120 to produce a transmitter frequency of 2295 mc.

A unique feature of the Resdel transponder is the elimination of the AGC loop. Normally, an AGC loop is utilized to prevent objectionable phase shifts from occurring under overdrive conditions. Although coherent AGC loops have been successfully employed, there are secondary effects which make their elimination quite desirable, especially in narrow band phaselocked loops. In order to prevent a coherent AGC loop from following the phase perturbations of the main loop, a long AGC filter time constant is required, making the system response to signal variations quite slow. Thus, for rapid signal fluctuations, the AGC cannot respond rapidly enough and overdrive can occur producing inneraction between the AGC loop and the phase loop.

As an answer to the problem of requiring signal limiting, an IF amplifier has been developed at Resdel which exhibits excellent limiting features. Limiting itself is not objectionable as long as noise limiting with resulting signal suppression does not occur in early stages where the signal suppression is not desired. That is, as long as the early IF stages do not limit on noise, the signal suppression that occurs in the second IF can be predicted, and the threshold design can be achieved through the use of a linear or quasilinear model.

The device used in the IF design is an integrated circuit consisting of two active devices connected in a differential amplifier configuration. Due to the circuit configuration, little fractional detuning (i.e., phase shift) occurs when the device is overdriven. Signal levels higher than 0 dbm have been handled by the first IF with 70 db limiting range and extremely little fractional detuning. These features made possible the elimination of the standard AGC loop.

Attention should also be drawn to the provisions for automatic lock-on using a sweep generator technique. This provides a lock-on time capability of less than 0.5 seconds with up to 250 kc "off frequency" conditions prevailing.

Provisions are incorporated for telemetering of phase error, signal level, and lock indication as shown in Figure 2-1. The power supply is designed to be self-contained within the transponder housing.

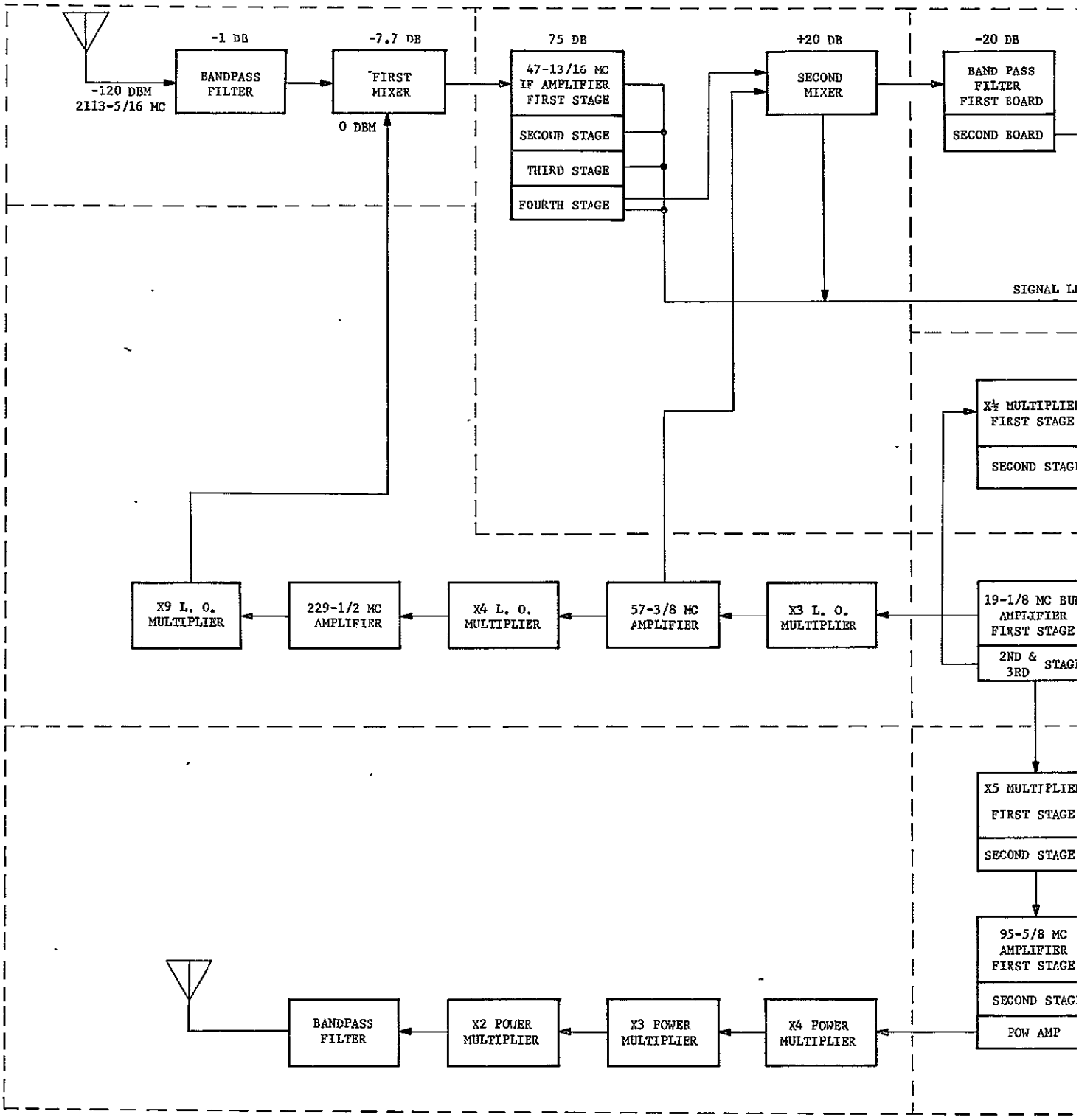
2.3 Packaging and Construction

The basic system packaging concept used in the transponder is depicted in Figures 2-2 and 2-3. Figure 2-4 is a photo of the existing Resdel Model 91242 transponder prototype.

Ease of production and servicing is assured by the design by allowing simple insertion or removal of all board modules. As can be seen in Figure 2-3, the individual boards are fitted into their respective slots. The slots in the bottom of the chassis are tapered so that the bottom section of the boards form a tight fit. The Allen screws at the side of the chassis slots are tightened after the board insertion. This locks the board tightly against the sides and bottom of the chassis slots, thus giving a good RF ground condition between the chassis and the boards.

This packaging concept is especially ideal for RF circuitry in that it affords:

(1) Effective shielding between stages
(2) Point-to-point wiring, eliminating long leads or cable runs.
(3) Ease of maintenance.
(4) Straightforward production and quality control, i.e., all boards can be fabricated, tested and inspected prior to insertion into the chassis.
(5) Eliminates internal connectors, enhancing reliability.
(6) Reduction of feedback problems.
(7) Excellent structural and vibration characteristics.
(8) High density packaging
(9) Demonstrated environmental, electrical, and reliable performance.


-1 DB
-7.7 DB
75 DB
+20 DB
-20 DB
-120 DBM
2113-5/16 MC
BANDPASS FILTER
FIRST MIXER
0 DBM
47-13/16 MC IF AMPLIFIER FIRST STAGE
SECOND STAGE
THIRD STAGE
FOURTH STAGE
SECOND MIXER
BAND PASS FILTER FIRST BOARD
SECOND BOARD
SIGNAL LI
X½ MULTIPLIEI FIRST STAGE
SECOND STAGI
X9 L. O. MULTIPLIER
229-1/2 MC AMPLIFIER
X4 L. O. MULTIPLIER
57-3/8 MC AMPLIFIER
X3 L. O. MULTIPLIER
19-1/8 MC BU AMPLIFIER FIRST STAGE
2ND & 3RD STAGI
X5 MULTIPLIEI FIRST STAGE
SECOND STAGE
95-5/8 MC AMPLIFIER FIRST STAGE
SECOND STAGI
POW AMP
BANDPASS FILTER
X2 POWER MULTIPLIER
X3 POWER MULTIPLIER
X4 POWER MULTIPLIER

2-3A

(1)

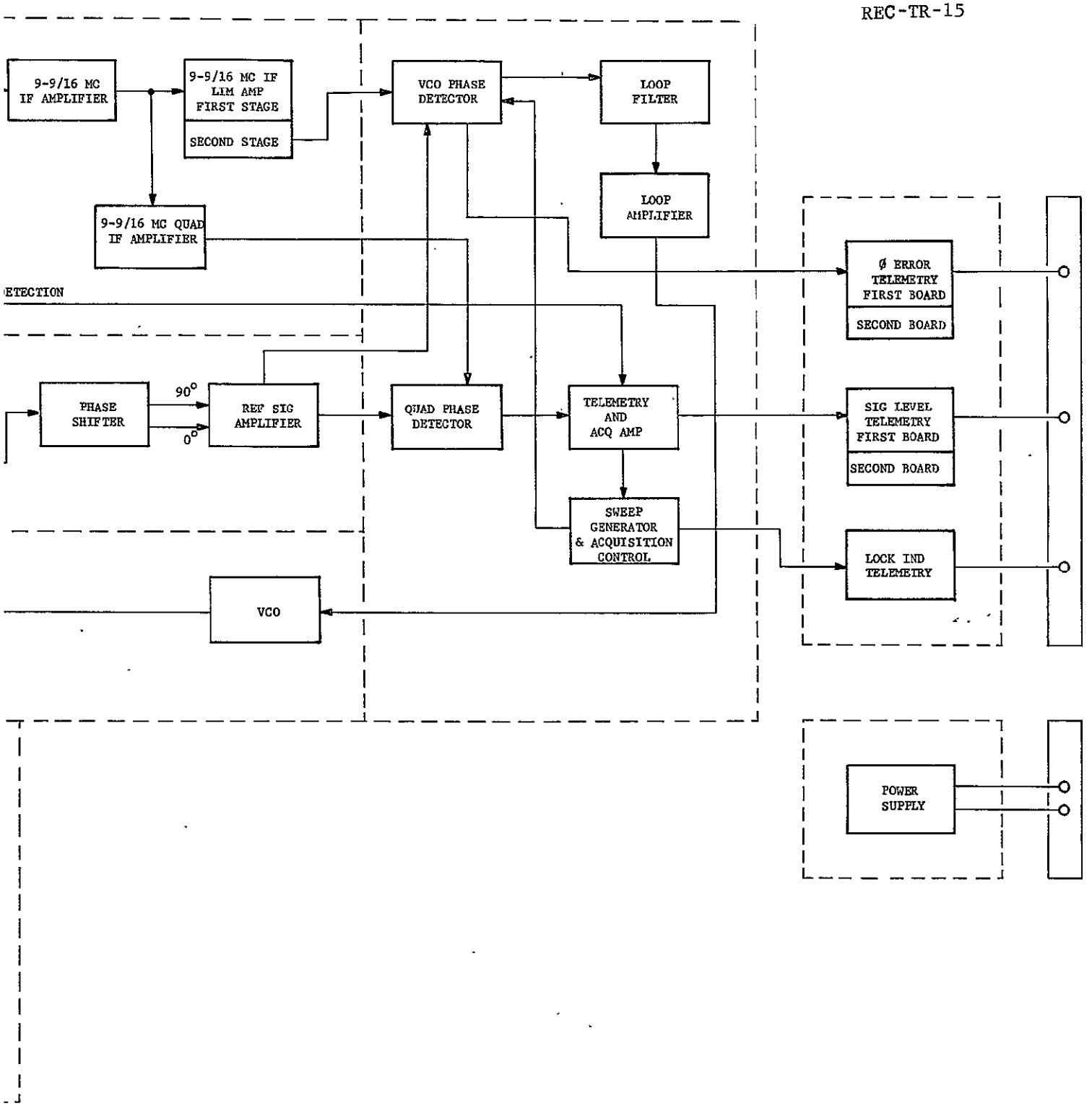


FIGURE 2-1

BLOCK DIAGRAM - S-BAND TRANSPONDER

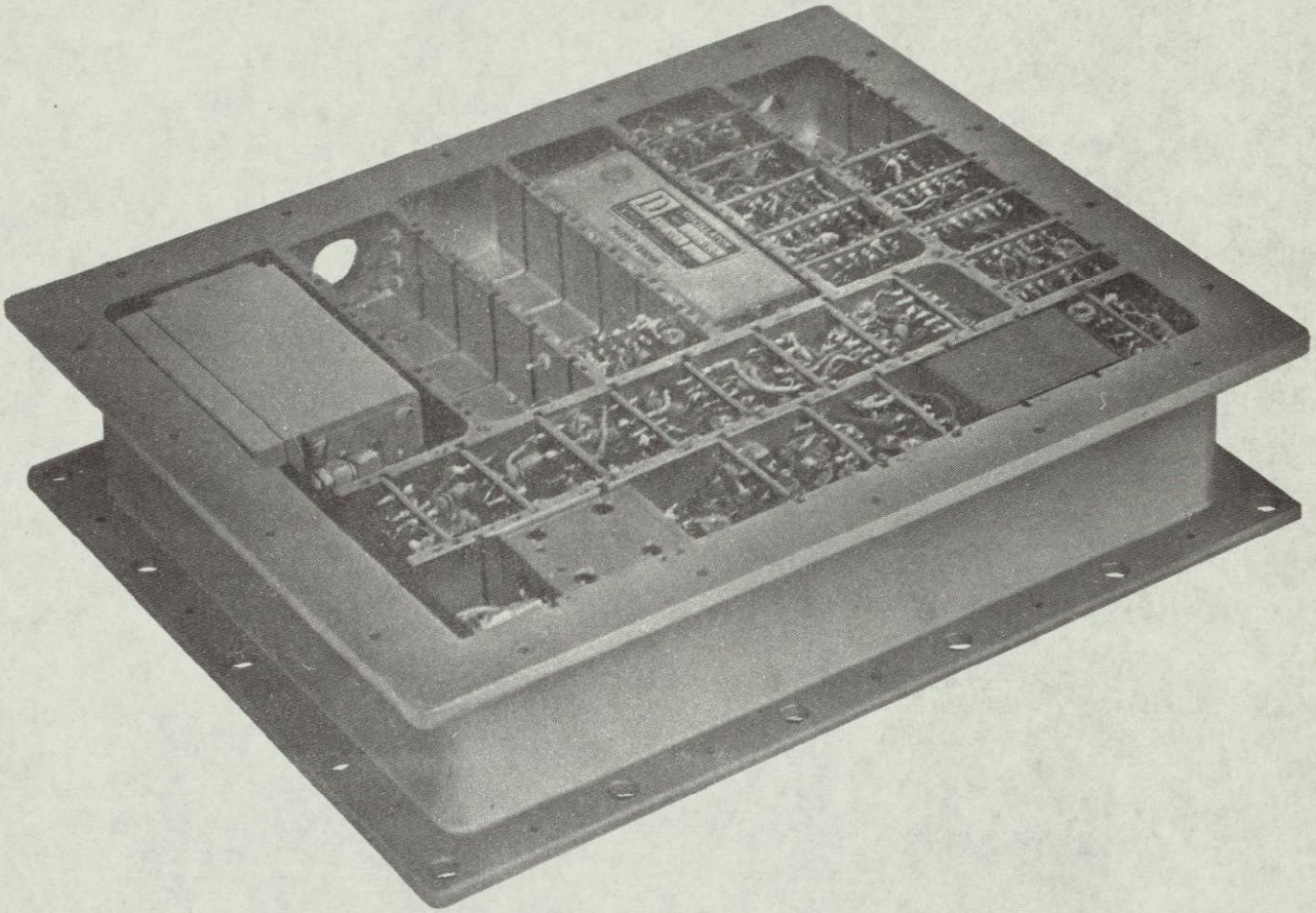


FIGURE 2-2 COMPARTMENTED PACKAGING DESIGN

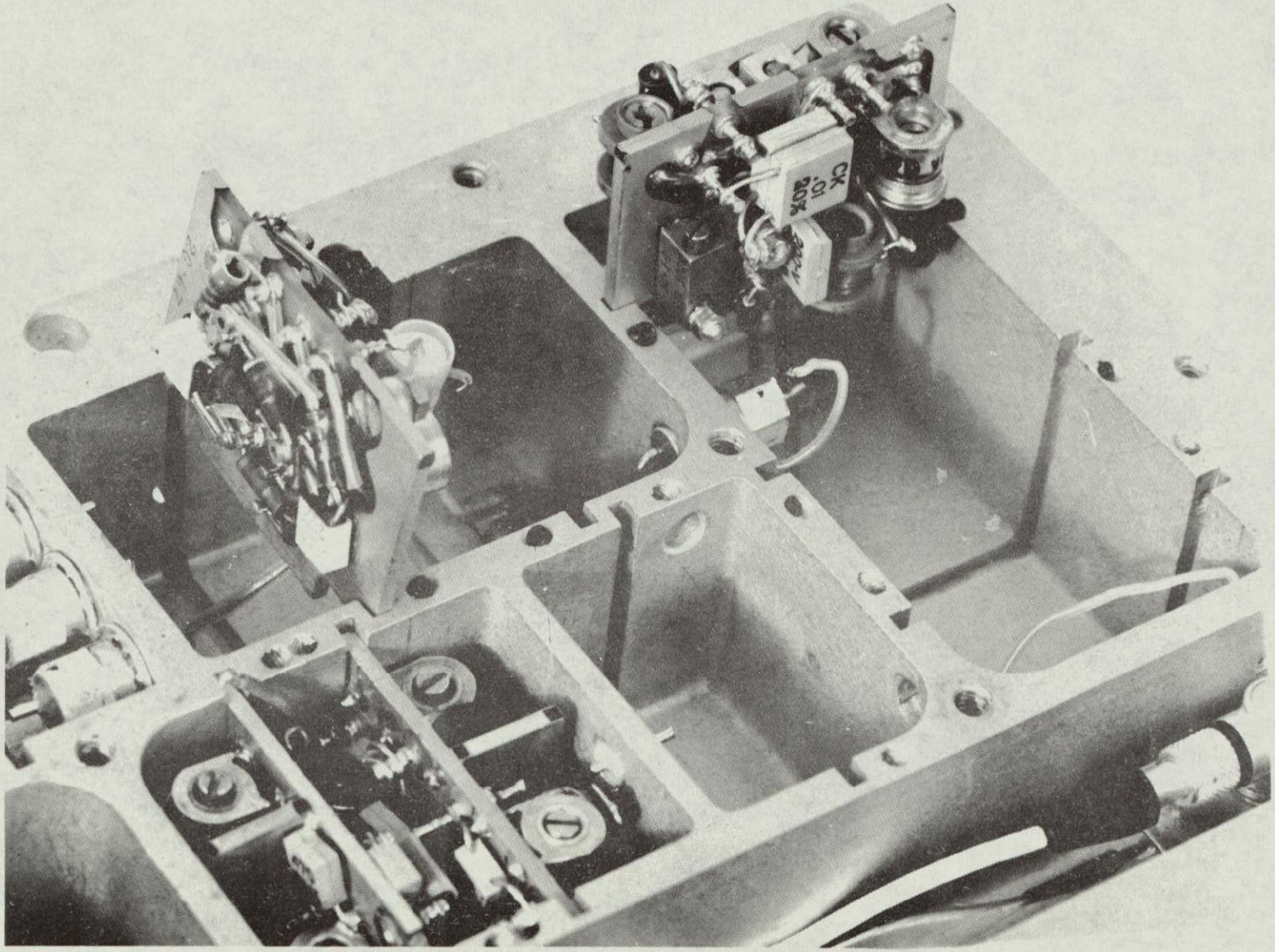


FIGURE 2-3 DETAIL OF COMPARTMENTED PACKAGING DESIGN

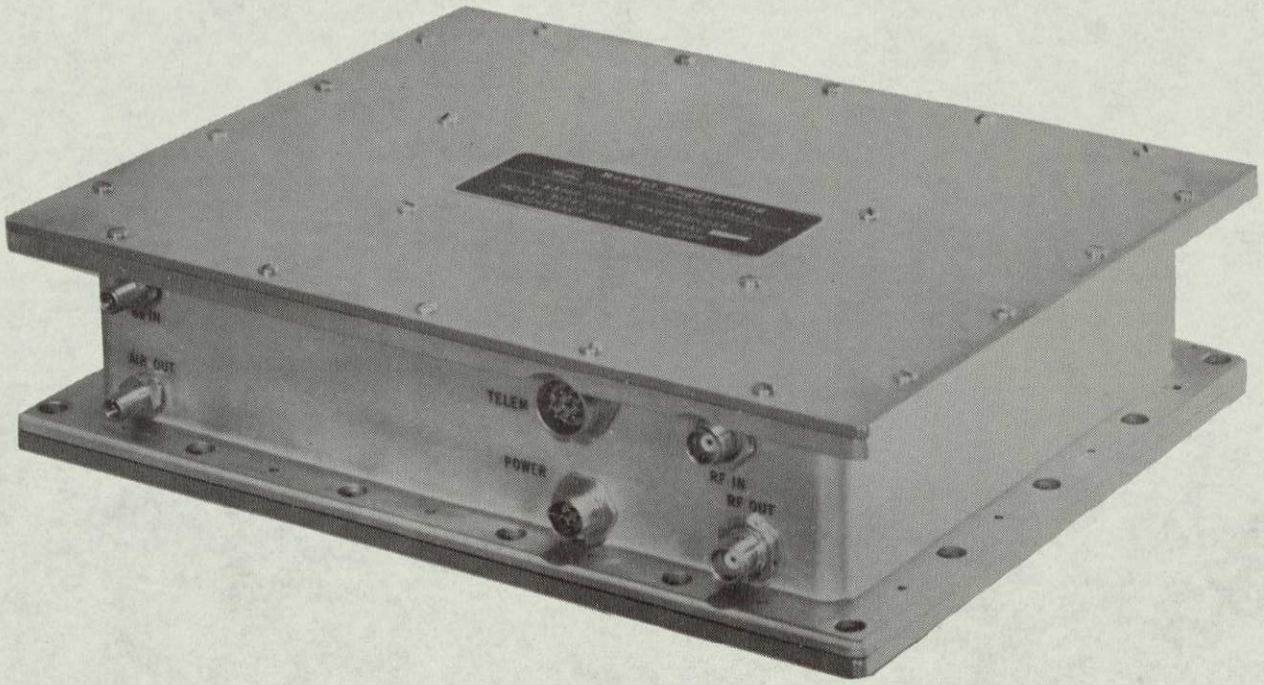


FIGURE 2-4 EXISTING RESDEL MODEL 91242 TRANSPONDER PROTOTYPE

The housing is made of cast aluminum including the slots. It is entirely gold plated, both inside and out. It is designed for pressurized operation. Resdel has also perfected an impregnation technique after gold plating which absolutely insures pressurization capability above 25 psi.

This impregnation process minimizes pressurization problems after assembly since no further mechanical or plating operation on the housing is performed after gold plating.

Pressurized mating of the covers and housing is accomplished by the use of "0" rings around the entire periphery of the covers. The "0" ring technique permits pressurization with an excellent metal-to-metal contact over relatively large surfaces, thereby assuring very good RF shielding. This minimizes possibilities of RF leakage and subsequeny undesired radiation of internal frequencies.

Each board module is designed for individual potting with compounds especially selected for their RF characteristics and repairability. In those areas where high impedance and/or RF considerations are paramount, a solid foam is used. In other places a transparent rubber-like silicone compound is used, which provides ease of repair.

The boards are copper plated with solder and ground terminals installed. Boards are plated around the edges to insure RF ground plane consistency. The connection from one mounting board to another are soldered wires thus reducing to an absolute minimum the connectors to be used.

In order to insure corrosion resistance where RF circuitry is involved, gold plating is the only choice to be made. Therefore, all boards and mechanical components are gold plated to insure non-corrosive contacts.

2.4 Receivers Description

2.4.1 Phase Lock Loop

The transmitted signal from the transponder is phase coherent with the received signal and is related by the ratio of 240/221. Phase coherence is accomplished by a phase locked loop. The following is a summary of the system parameters of the loop.

The System Phase Transfer Function at threshold is:

$$K_{CL}(S) = \frac{1 + \frac{3}{4B_L} S}{1 + \frac{3}{4B_L} S + \frac{9}{32B_L^2} S^2}$$

where s = complex La Place operator

B_L = loop bandwidth (one sided)

$$B_L = \frac{1}{2\pi} \int_0^\infty / K_{CL} (j\omega) /^2 \, d\omega = 1200 \text{ cps}$$

$$T_2 = \frac{3}{4B_L} = 0.625 \times 10^{-3} \text{ seconds}$$

$$T_1 = \frac{9}{32B_L^2} KoT = 1.44 \text{ seconds}$$

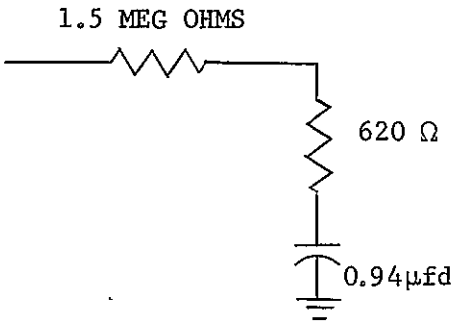
Velocity Lag Error $\leq 12^o$

Sweep Acceleration Lag Error $\leq 18^o$

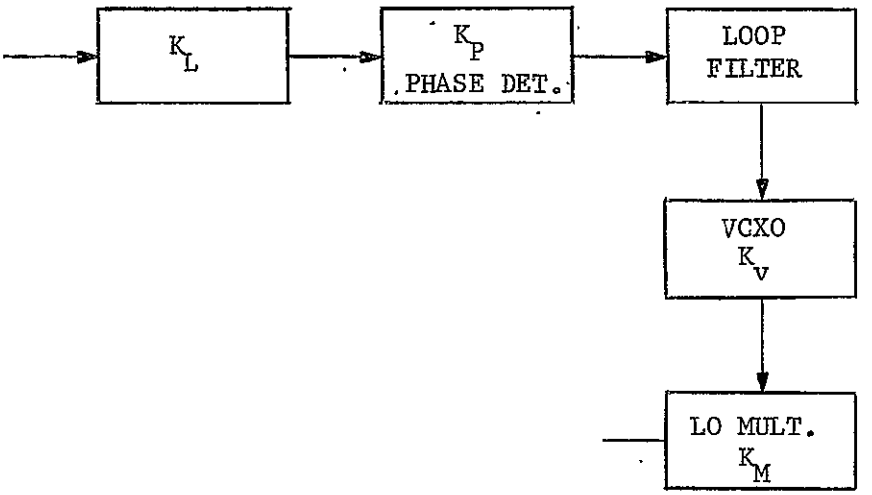
Sensitivity = -120 dbm

Lock Confidence Factor $\geq 95.5\%$

Loop Filter



A functional block diagram is as follows:



The total gain at the threshold is given by:

$$K_{OL} = K_L\ K_P\ K_f\ K_v\ K_M = 7.4 \times 10^6$$

where,

K_L = 0.125 = Limiter Gain (actual voltage suppression factor)

K_P = 14.3 volt/rad = Phase Detector Gain

K_f = 2.0 = Loop filter and DC amplifier gain

K_v = 18,700 $\frac{\text{rad}}{\text{volt sec}}$ = VCO Gain

K_M = 110.5 = Local Oscillator Multiplication ratio

2.4.2 Receiver Discussion

A block diagram of the S-Band Transponder is shown in Drawing 20675. It details the gains, impedances, frequencies, and signal levels at threshold. A brief discussion of each block follows below. Since gains, power levels, etc. are designated on the block diagram these will not be spelled out in these discussions. The receiver consists of sections 200, 300, 400, 500, 600, 700 as called out on the block diagram. The schematic drawing numbers are shown with the section designation on the block diagram.

2.4.2.1 Section 200

Input Bandpass Filter

This is a three section bandpass filter purchased from Telonic Engineering Corporation. It is intended as a preselecter to reject any off channel interfering frequencies. Its dimensions are specifically tailored to the transponder housing.

First Mixer

This is a balanced microwave diode mixer purchased from Sanders Associates Inc. It is fixed tuned but is able to operate over a relatively broad range of frequencies. It has a noise figure of 8.7 db when operated with an If amplifier noise figure of 2.5 db. It utilizes strip-line techniques.

47-13/16 mc If Amplifier

The 47-13/16 mc IF Amplifier consists of four stages of amplification. It has an input noise figure of 4.0 db and a 3 db bandwidth of 7 mc. The amplifier uses "limiting" action as a means of gain control. It can handle up to +5 dbm input signal levels without degradation of the input signal.

All stages are very similar and use a differential amplifier design. This amplifier provides the required system gain and also prevents any overloading of the 2nd mixer by means of its excellent limiting action. It is shielded internally to prevent ground loop instabilities. See Section 2.8.1.2 for further discussion on this amplifier.

Second Mixer

This is a single transistor stage. Its primary purpose is to provide frequency conversion to the second IF, but it also gives 20 db of gain.

2.4.2.2 Section 300
9-9/16 mc Bandpass Filter

This filter consists of two double tuned circuits. It is intended to provide the required system predetection noise bandwidth. Its 3 db bandwidth is 70 kc. Because of the extremely high Q's involved it is shielded internally so that RF radiation from other areas cannot enter and cause loop instabilities.

9-9/16 mc 2nd IF Amplifier

The second IF amplifier provides linear gain for the Quad Phase Detector and a limited output for the loop phase detector. The linear amplifier consists of LC tuned amplifier and a wideband RC coupled isolation amplifier. The isolation amplifier is required to prevent signals from the Quad phase detector from getting back into the 2nd IF limiter and producing false locks onto the reference. The present amplifier consists of seven transistors and has a compression of a ¼ db at +16 dbm output.

The limiter in the 2nd IF amplifier holds the output constant (within .5db) over the input signal range.

Limiting is accomplished at low level of +2 mw and the limited signal is then amplified by a linear amplifier. This allows limiting to only occur at one place providing easy and precise control of the limit level. Four transistors are used in the limiting function.

2.4.2.3 Section 400
Phase Detectors

The phase detectors are diode circuitry. The diodes are DC matched to provide good temperature stability.

Loop Filter and Amplification

The loop filter is a lead-lag network used to give phase and gain margins for stability and to set the post-detection loop bandwidth. The loop amplifier consists of transistor circuitry to provide the required DC gain and impedance isolation and matching of several megohms from the loop filter output and VCXO input of 50 K ohms. It has extremely small drift with temperature.

Sweep Generator and Acquisition Control

This circuit provides the sweep for acquisition purposes. It gives the varying voltage necessary to vary the VCXO frequency to search for the incoming signal. It also provides the control for determining when to sweep and when the signal has been acquired. See Section 2.8.4 for further discussion of this operation.

Telemetry and Acquisition Amp

This is a combination amplifier for providing the acquisition control voltage and also the signal level voltage that is produced by the Quadrature phase detector. It consists essentially of a nine-transistor integrated circuit.

2.4.2.4 Section 500
VCXO

The VCXO is purchased from Damon Engineering Corporation and is specially constructed for this transponder. Its frequency control input impedance is 50,000 ohms and RF output impedance is 50 ohms. It has a frequency deviation capability of $\pm$ 12.5 kc. It is temperature stabilized.

19-1/8 Buffer Amps

These consist of three conventional transistor stages used to provide buffering and power to the reference signal section, to the transmitter string, and to the local oscillator multiplier string.

2.4.2.5 Section 600
X½ Multiplier

This is a parametric divider consisting of a unique balanced arrangement using a single varactor. Also included is a conventional buffer amplifier at the input to the divider. This is further discussed in Section 2.8.5.

Phase Shifter

This is a 90° phase shifter and buffer amplifier. It provides the proper phase shift for the operation of the quadrature phase detector.

Reference Signal Amplifiers

These amplifiers give the required Ref signal power level for efficient operation of the phase detectors. They give an output of 100 mw each.

2.4.2.6 Section 700
X3 L.O. Multiplier and 57-3/8 Amplifier

This consists of an X3 transistor type multiplier and a 57 mc power amplifier for the power required for further LO multiplication and for the 2nd Mixer LO port. This multiplier is further discussed in Section 2.8.5.

X4 LO Multiplier and 229½ Amplifier

This consists of an X4 varactor type multiplier utilizing an idler circuit at the 3rd harmonic for efficiency. The power amp is a conventional grounded emitter type. Further discussion of the multiplier is in Section 2.8.5.

X9 LO Multiplier

This uses a step-recovery diode as the non-linear device. The multiplication of 9 is obtained without the use of idlers, thus improving stability with temperature. This is further discussed in Section 2.8.5.

2.5 Transmitter Description

The transmitter portion consists of sections 800 and 900 as shown on the Block Diagram 20675.

2.5.1 Section 800
X5 Multiplier

This is a varactor type multiplier utilizing three idler circuits at the 2nd, 3rd, and 4th harmonics. It also contains a conventional input buffer amplifier. This is discussed further in Section 2.8.5.

Power Amplifier

This is a four stage power amplification chain consisting of two intermediate power amplifiers followed by a driver and then two paralleled high power transistor amplifiers. It supplies approximately 25 watts at 95-5/8 mc for driving the transmitter multiplier string. The intermediate amplifiers are conventional Class C amplifiers. The driver and power amplifiers are integrally matched and are discussed further in Section 2.8.3.

2.5.2 Section 900 X24 Power Multiplier

This section consists of first an X4 power varactor multiplier utilizing a single idler at 3rd harmonic. It is completely a lumped-constant design. It is then followed by an X3 power varactor multiplier with a single idler at 2nd harmonic. This multiplier input is also lumped constant but the output circuitry is a coaxial cavity. The X3 is then followed by a power varactor X2 multiplier supplying nominally 2 watts at S-Band. It is completely cavity circuitry.

All the power multipliers are thermally rugged by derating. Further discussion of these multipliers is in Section 2.8.5.

Output Bandpass Filter

This bandpass filter is intended to help reject unwanted spurious signals emanating from the power multiplier string. It is almost identical to the input bandpass filter and is also purchased from Telonic Engineering Corporation.

2.6 Telemetering

The telemetering functions consist of Section 1100 of the Block Diagram 20675. The outputs are voltages suitable for modulation of a subcarrier VCO of the standard IRIG specifications.

Phase Error Telemetry

The phase error telemetry receives the indicated static phase error voltage from the VCO phase detector, amplifies it, and then by means of a chopper amplifier provides the required double ended output isolated from ground.

Lock Indicator Telemetry

This is again an amplifier-chopper circuit providing isolated, double ended output voltages. It receives a voltage from the acquisition control and processes it to give a go-no-go type of output to indicate whether the transponder is locked or not.

Signal Level Telemetry

This is essentially identical to the phase error telemetry circuit. It processes and combines the voltages from the signal sensing amplifiers and the telemetry and acquisition amplifier to give an isolated, double ended output.

Signal Sensing Amplifiers

The signal sensing amplifiers samples a 47-13/16 mc signal from the output of the 1st stage of the 47-13/16 IF amplifiers. It then amplifies this signal, detects it, and then uses the detected signal as a pseudo AGC voltage. This AGC voltage is then fed to the signal level telemetry amplifiers as a measure of signal level. The entire amplifier is quite simple and straightforward and does not require any particualr temperature compensation since it is not within the main receiver signal path.

2.7 Power Supply

The power supply is section 1000 on the block diagram 20675. It consists essentially of input RFI filters, 10 kc square wave oscillator-regulator, high frequency ripple filters, and electronic ripple regulator. It supplies the chopper voltage for operation of the telemetering amplifiers. The DC voltages generated are 50V @ 1.2 amp, +15 volt @ 0.5A, and -15 volt @ 0.3A. The output ripple on the $\pm$ 15 volts is less than 50 μv.

2.8 The following are discussions of the more unique and interesting areas of this transponder.

2.8.1 Design Considerations of Bandpass Limiting Versus Synchronous AGC and Non-Synchronous AGC

At the onset of this project it was decided that synchronous AGC should be used in the system design. It was realized however, that conflicting requirements made the use of synchronous AGC undesirable in some respects. First, a requirement existed for handling a -7 dbm input signal level at the system input. This signal level attenuated by the insertion loss of the input filter and conversion loss of the first mixer gave approximately a -16 dbm input level to the first IF stage.

The device used in the first IF design is a MC1110 integrated device. It was chosen primarily because its output and input susceptance variations are quite small for changes in collector voltage and emitter current. One of the main problems in the design of phase locked systems

is preventing fractional detuning in the IF amplifiers under overdrive conditions or during AGC loop operation.

Digressing briefly from the device discussion, the synchrous AGC control of the IF gain is present only when the loop is lock on. Also the noise bandwidth of the AGC loop must be several orders of magnitudes narrower than the tracking loop. The AGC response time therefore is considerably longer than the tracking loops. This presents a problem in trying to acquire the signal. If for example a loss of signal occurred for a period of time sufficiently long for the loop filter to discharge upon return of signal the loop would be out of lock until the external sweep voltage could pull the VCXO into the loop bandwidth. During this time however, no coherent AGC would be available to control the IF gain and if the signal level were sufficiently high the IF would be overdriven. In a very narrow band transponder for deep space application the system memory (energy storage of the loop filter) would be considerably longer than that of this transponder. In this case it might be reasonable to assume that signal loss would not occur for periods of time sufficiently long for the system memory to be lost and that if it did a signal level sufficiently large to overdrive the IF would not be present upon signal return. Such, however, is not the case, for the presently discussed system. Loop bandwidth has been purposely increased since the system usage is for relatively short ranges and the acceleration ramp handling capability is the determining factor as to how fast the system can reacquire signal which in turn dictates loop bandwidth.

Thus, in the case of the Resdel S-band transponder, coherent AGC alone would be inadequate in that overdrive of the IF would still occur and the response time could limit how fast a signal could be reacquired.

An alternate approach would be to use in addition to the coherent AGC, non-coherent AGC. The non-coherent AGC would control IF gain with the system out of lock while the coherent AGC would control the gain while the system was in lock. This approach was not used since the additional system complexity was considered unwarranted.

During the development of the first IF a very unique feature of the MC1110 transistor was noted. It was found that if the device was driven from a certain source impedance, that very little difference between its small signal and large signal response occurred. Practically no fractional detuning occurred and the normal response flat topping along with generation of spurious outputs did not occur. It was felt intuitively that this unique behavior was due to several factors. First the device is connected in such a manner that as one stage was being driven on harder, the other was being turned off so that some cancellation of susceptance variations could occur. Also the output collector resonant circuit is driven from a common base stage which is a relatively high impedance current source. Thus, as the stage is cut off for a portion of the cycle or driven into saturation the collector circuit can continue ringing since during nonlinear operation very little energy is fed back into the source.

Predicting the behavior of the device in its small signal region is easily accomplished by usage of the Linvill analysis or other circuit models. Analysis of the large signal behavior however, requires a more intimate knowledge of the device parameters than can be obtained from manufacturer data sheets or simple tests. Also, the complexity of a non-linear analysis lends credence to an empirical approach rather than a rigorous analytical approach to the IF's large signal behavior.

The excellent limiting features of the first IF were illustrated by putting a sweep generator on the input to the first IF stage and varying the input from 0 dbm to -110 dbm. The output varied from 0 dbm to -25 dbm. For a +110 dbm input signal level variation, the response was altered very little and practically no fractional detuning occurred. The limit level is 0 dbm and the limiting range is in excess of 70 dbm (output remains within .25 db of limit level).

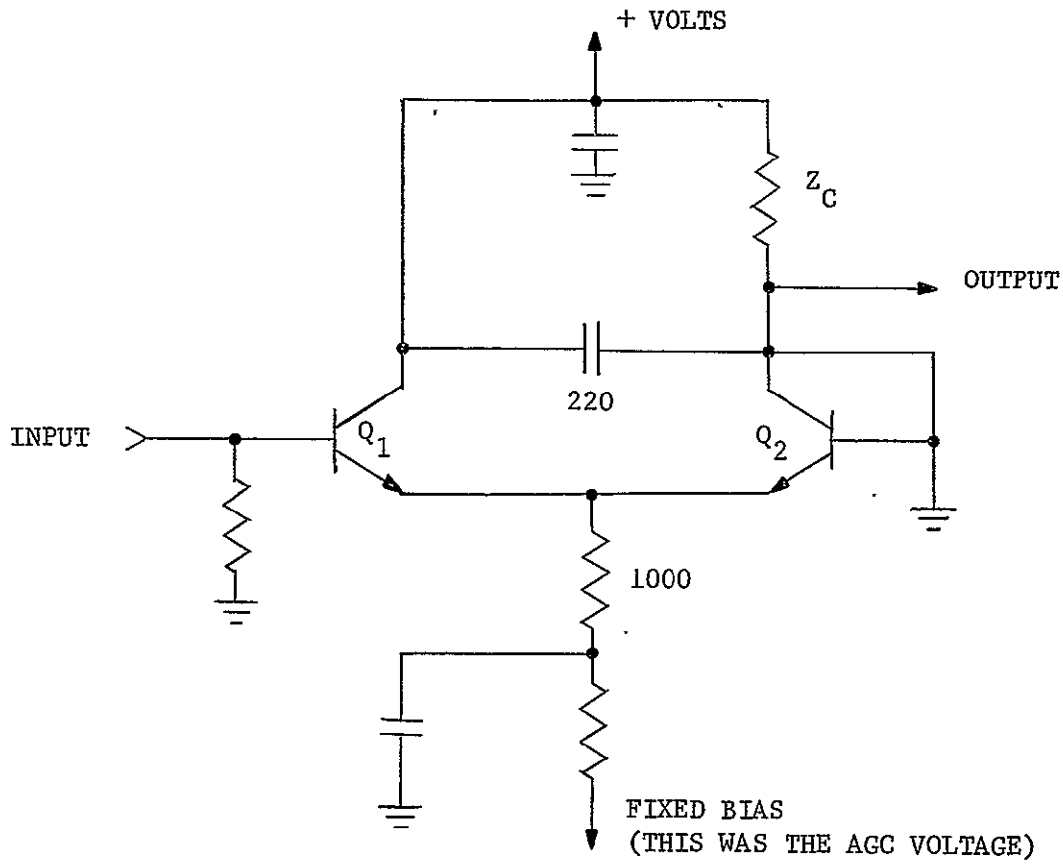
With this type of limiting the question arises as to the necessity of an AGC loop at all. Certainly the elimination of the AGC loop is attractive for the previously mentioned reasons and for elimination of any possible two loop oscillations between the AGC and the carrier tracking loop. The type of limiting provided in this S-band transponder will approximate a variable loop filter that is continually adjustable for optimum performance for each change of input signal level.

2.8.2 IF Amplifier

One of the major technical problems was possible phase shift that would be encountered over the large dynamic AGC characteristic in the first IF amplifier. (Later eliminated by using limiting). A breadboard of the JPL approach was built up and tried along with some other proposed methods. These all yielded too much phase shift for this application.

It is self-evident that in order for any phaselock receiver to faithfully follow the incoming signal, the receiver should introduce no incremental phase shifts over the entire dynamic range of signal input and environmental variations. Phase shift variations in the receiver are one of the most difficult problems the designer must solve.

The incremental phase shift requirements are in the order of 10^{o} and additional techniques must be used to meet these stringent requirements. Many types of AGC circuits have been tried in order to minimize phase shift over dynamic ranges of 80 to 100 db. The types have ranged from various combinations of "forward" and "reverse" AGC to the use of diode-type attenuators between stages. Each of these methods has had some success but has not really been completely satisfactory. The method developed for the S-Band Transponder employs an integrated circuit of two transistors in a differential amplifier as shown in the following diagram.



I-F AMPLIFIER STAGE WITH AGC AMPLIFIER

This configuration provides a relatively high input impedance, good isolation from input to output, low base to emitter capacitance, plus capacitance cancellation with current changes. The stage operates similar to any differential amplifier. Gain control is accomplished by varying the emitter current.

Tests made on this unit indicated an excellent limiting characteristic. Due to system requirements being hard to meet with synchronous AGC, this amplifier was studied as a possible solution of providing the required gain without overloading on strong signal causing spurious responses and system study and the S-Band Transponders mission. (From launch to some 15000 KM) indicated that limiting IF amplifiers was a better approach.

Tests conducted on this type of configuration have indicated the phase shift to be less than 5^o over a dynamic range of 30 db.

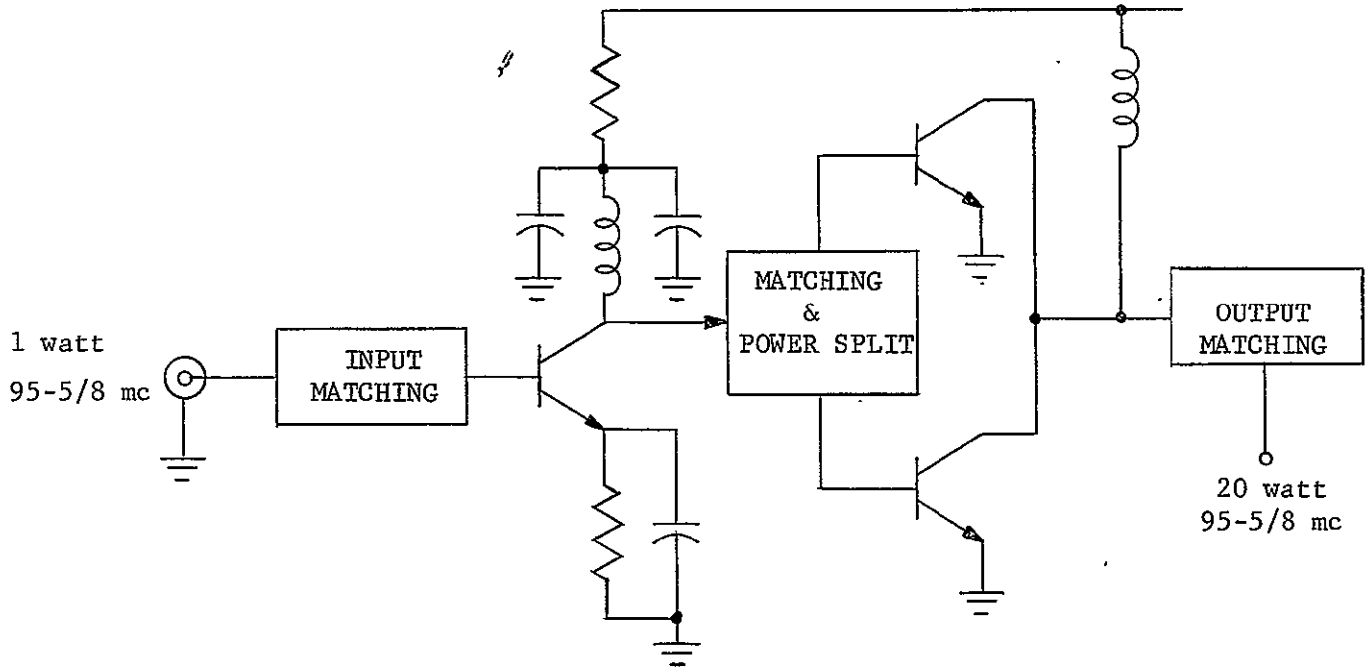
Incremental phase shift due to temperature changes are also minimized through the use of the circuitry shown. Incremental phase shift due to Doppler frequency excursions are reduced by using broadbanded tuned circuits with a small L/C ratio. This amplifier configuration is used in both

1st and 2nd IF amplifiers where power output is not of primary importance.

2.8.3 95 Mc Power Amplifier

To supply the required power output of the transmitter it is required to provide considerable power at a sub-multiple of the output frequency. The choosing of the frequency to do this depends on the dissipation capabilities of the varactors to be used in the multipliers. Considering component capabilities it was decided to do this at 95 mc (following the X5 Multiplier).

The power amplifier for this requirement consists of a driver and parallel connected final amplifier. It receives one watt at 95-5/8 mc from the Intermediate Power Amplifier and delivers in excess of 20 watts to the X4 multiplier. A simplified schematic of the power amplifier is as follows.



2.8.4 Acquisition

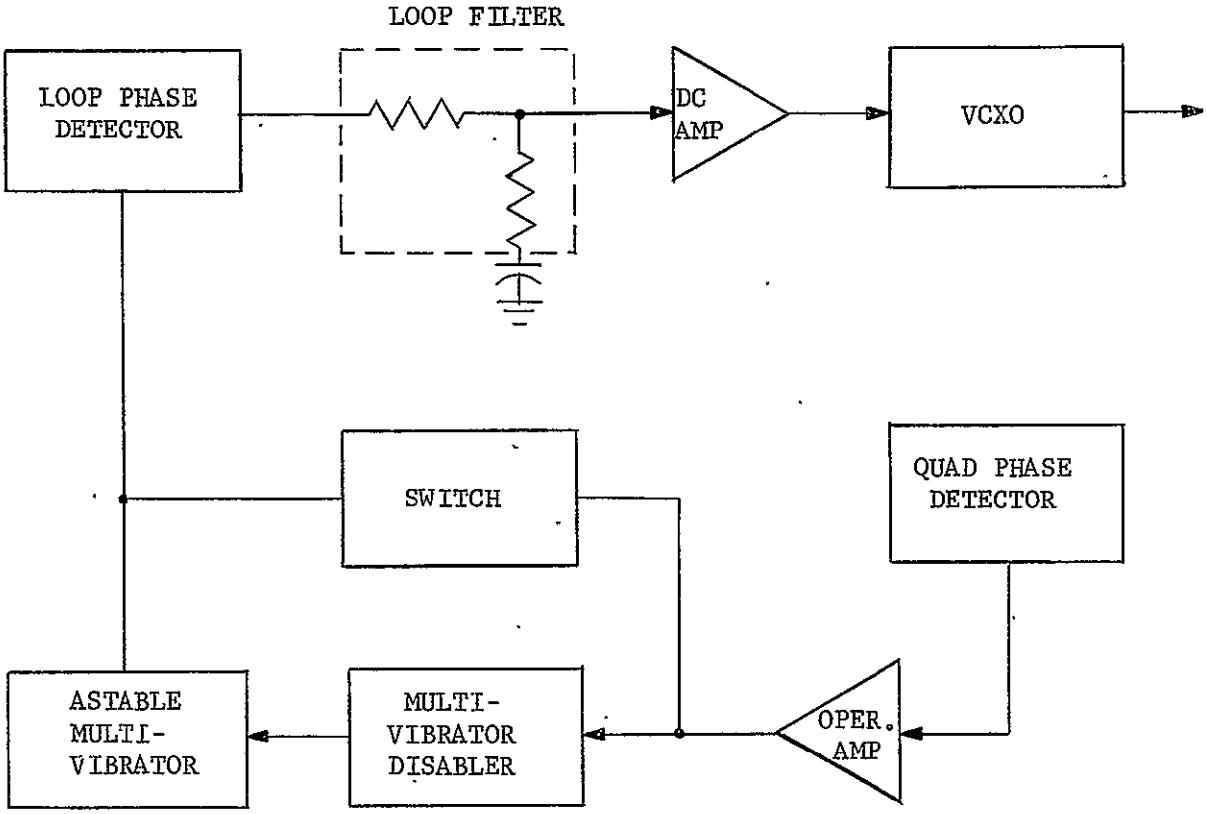
A questionable area was the acquisition requirements of the transponder. A study of the requirements for this system and a search for best and most reliable circuitry for this job was conducted. Early philosophy to the problem of acquiring the signal as fast as possible without degrading threshold performance was to sense the beat frequency produced by the quadrature phase detector. This signal was then filtered and rectified and used to control a sweep generator. Several limitations to this approach became evident as the development program progressed. One drawback was that the acquisition bandwidth was set by the acquisition filtering configuration and since the sensing was occurring before the sweep had brought the VCXO into the loop bandwidth, the maximum sweep rate was limited by the charge rate of the sensing filter. This resulted in an acquisition time in the order of 5 seconds. Another limitation was that the sweep voltage could not be coupled into the loop filter without causing DC transfer loss of the loop filter which reduced overall loop gain.

Presently the sweep voltage is a square wave generated by an astable multi-vibrator. This signal is coupled through the phase detector into the loop filter in such a way that the loop filter is not loaded. The square wave sweep voltage appears as a triangular sweep voltage at the VCXO due to the integration of the square wave by the loop filter. As the VCXO is swept, the output of the quadrature phase detector is sampled to determine if signal of usable level is present. As the VCXO is pulled by the sweep voltage so that it is closer to the incoming signal frequency the voltage out of the quadrature phase detector increases. This voltage is amplified in a DC amplifier which actuates the acquisition control circuitry. The acquisition control circuitry disables the astable multi-vibrator and switches the sweep input to the phase detector to very near ground through a reverse connected transistor, thus preventing an "offset" voltage on the phase detector.

One advantage of this acquisition is that the loop voltage now opposes the sweep voltage in such a way that the system remains within the acquisition bandwidth for a longer period of time. The acquisition bandwidth can now be made narrower, thus reducing the effects of noise near threshold levels.

The limitation on acquisition time is also now only dependent on the loop bandwidth and a more reliable operation is assured since the sensing does not activate until it is within the "range" of the loop bandwidth, the loop will lock up itself. This has resulted in a maximum acquisition time of 0.5 sec.

A simplified schematic of the acquisition circuitry is shown for illustration of the operation.



2.8.5 Multipliers

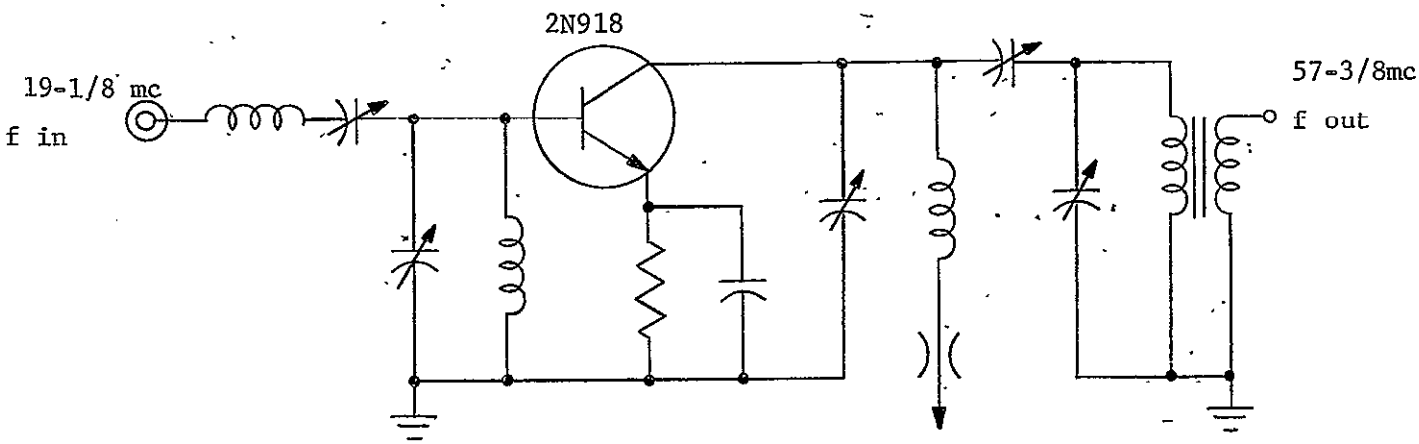
All frequency multipliers used in the transponder are Resdel designs. They may be categorized into three types: (1) ordinary transistor frequency multipliers, (2) reactance diode frequency multipliers, and (3) passive multipliers.

Transistor Frequency Multiplier

Only one of the several multipliers in the transponder is of the usual transistor, active multiplier design. This stage is the multiply-by-three circuit in the S-band mixer injection chain. It takes the 19-1/8 mc drive signal from one of the VCXO buffers and triples the frequency up to 57-3/8 mc. Active multiplication was chosen, since both frequency and power are commensurate with efficient transistor usage. The 2N918 high

frequency silicon planar epitaxial transistor was chosen and provides optimum phase coherence through the multiplier. The efficiency is maintained near maximum with this type of device, and the power level at the input makes the 2N918 an excellent choice. The non-linearity required for multiplication is attained by using a Class C mode. Constant output is maintained across the thermal excursion by desing specification requiring excessive drive signal. Conduction angle for the stage is controlled by use of a by-passed emitter resistor.

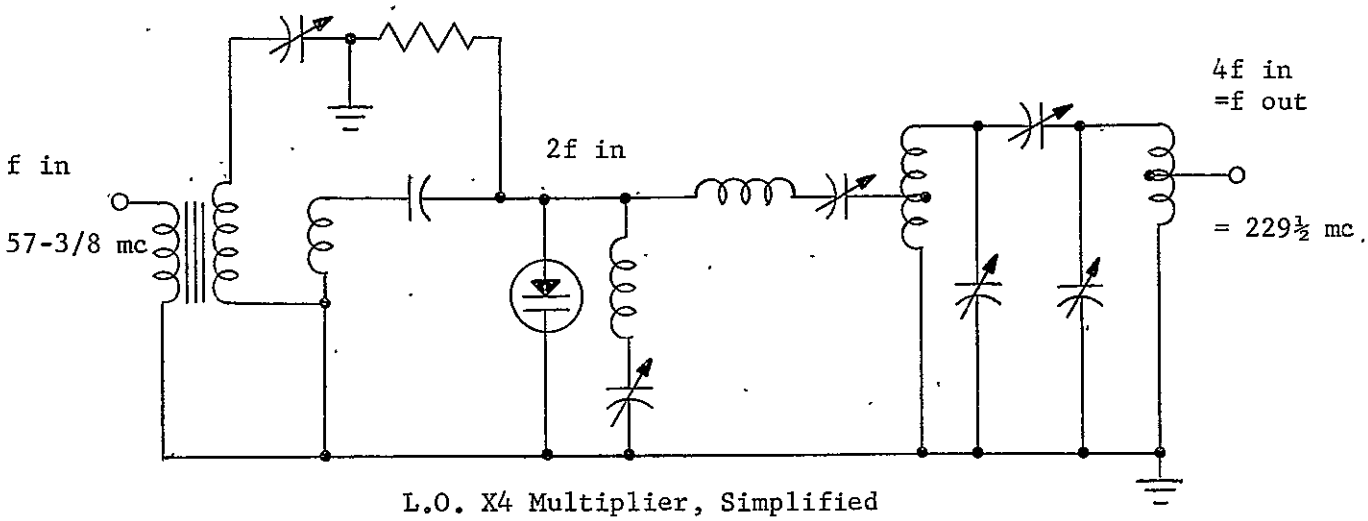
A simple input impedance transformation drives the common emitter configuration, and a double-tuned, critically coupled output circuit provides adequate harmonic rejection.



X3 Multiplier Simplified Schematic

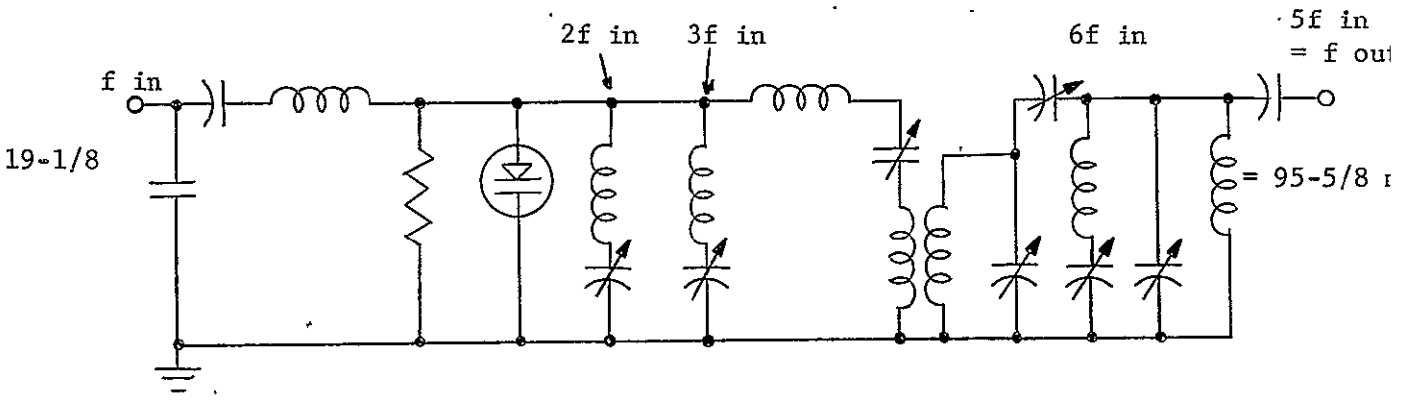
Varactor Frequency Multipliers

A total of five varactor frequency multipliers are used at various locations in the transponder. Both the multiply-by-4 circuit in the S-band local oscillator chain, and the multiply-by-5 circuit in the transmitter chain are typical low level design.



L.O. X4 Multiplier, Simplified

Both of these multipliers utilize the current pumped or shunt configuration, and also employ double-tuned harmonic suppression filters on their outputs. The diodes used are the lead connected, square-law type. The thermal safety margin is extremely high-being well over 200% at the maximum operating temperature for the system. The power efficiencies are

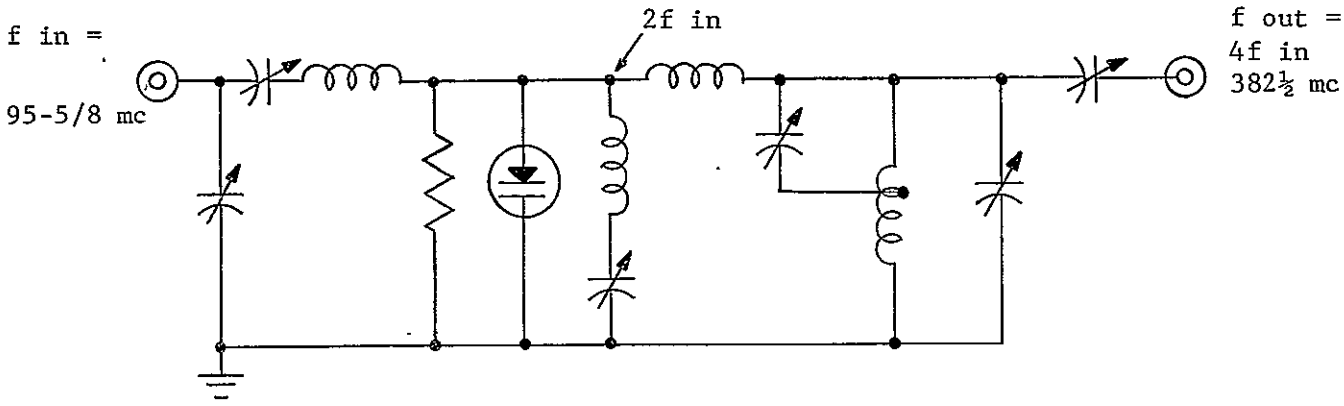


X5 Transmitter Multiplier, Simplified

quite high and the spurious output content is well below the requirements for their location within the entire system. Differences between the two multipliers (other than power level, frequency, and multiplication order) are as follows. The X4 uses a parallel tuned, link-coupled transformer for matching in and the parallel tap method for output matching. The X5 uses a tunable L-Section and has a negative reactance output to the next stage to resolve any series, residual inductance at the interface. Additionally, the X5, because of the high order of multiplication, uses two idler circuits and requires a 6f trap at the high impedance point of the output filter. Both multipliers are fully self biasing to insure smooth operation when subjected to input power variations and thermal environment.

The nature of the multipliers used in the transmitter power chain differ in power level, frequency, and mechanically. However, their electrical equivalent is quite standard.

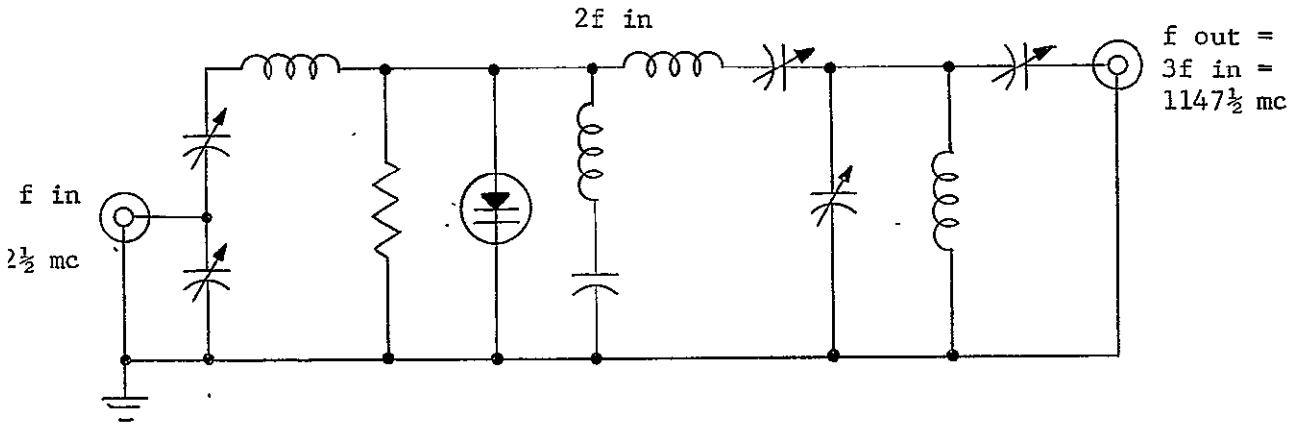
The high power X4 which converts 20 watts minimum from the power amplifier at 95-5/8 mc to about 12 watts at 382½ mc is shown in the following simplified schematic.



Transmitter VHF X4 Multiplier

A tunable L-Section matches the X4 input to the Power Amplifier output. A single idler at 2f is used. An efficiency of 50% is obtained in this multiplier. A parallel-tap resonator provides a match for the diode, and the load is transformed capacitively for the sake of tuning out any series inductance which could remain. The output system employs a double tuned resonant circuit. A series tuned element at 4f provides a high impedance to f and other harmonic energy. Lumped parameters are used throughout, and self-bias provides smooth operation over an input power variation well in excess of 13 db. Spurious content is well below -20 db in reference to f_{out}. The varactor diode itself is a stud-mounted, hermetic-sealed device having a very high Q-factor. The non-linearity law is low, approximately 0.2, as opposed to the more usual 0.33 to 0.5. This low non-linearity law would result in poor efficiency, except that a current-step-recovery is also prevalent. This raises the efficiency greatly, and the result is that a much smoother response is made possibel. The unique type of depletion layer profile also contributes to the excellent thermal performance. This X4 was actually tested with 50 watts input and the efficiency remained nearly 40%. The diode is capable of tolerating over 75 watts at 25°C stud temperature. A rugged, machined, module houses this quadrupler.

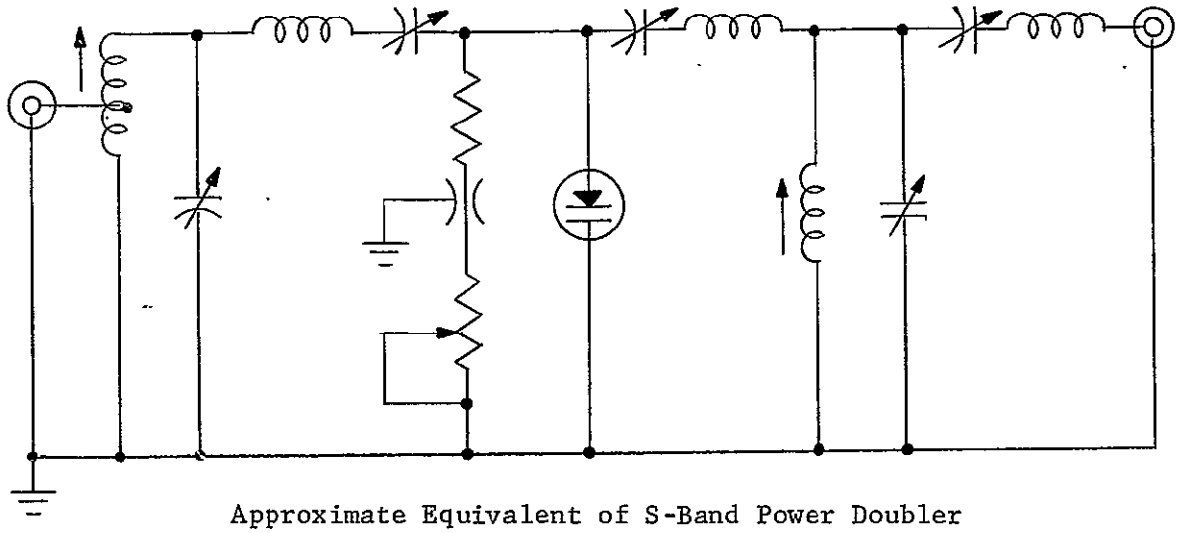
The next multiplier in the transmitter power chain is the 382½ mc to 1147½ mc tripler. The same type of diode element is employed as was used in the previous quadrupler. Only the electrical parameters differ due to the frequency/power situation. A similar thermal margin exists. About 100% safety factor is present at 85°C heat sink temperature. The circuitry is similar to the X4, except that the output system utilizes distributed parameters due to the elevated frequency. The electrical equivalent is as follows.



Transmitter L-Band X3

Once again, self-bias is used to promote stability. The output cavity is of the foreshortened, TEM Mode coaxial design. Rigid micro-coax is used to interconnect to the last doubler. Output power is in the order of 4.5 to 5 watts at 25°C. The related multiplier efficiency is approximately 40%. The mechanical construction is again that of a machined module which allows operation independent of the system housing.

The S-Band output power is developed in the final frequency doubler. Distributed-parameter TEM Mode Coaxial cavities prevail for both input and output circuits. The closest electrical equivalent is shown.



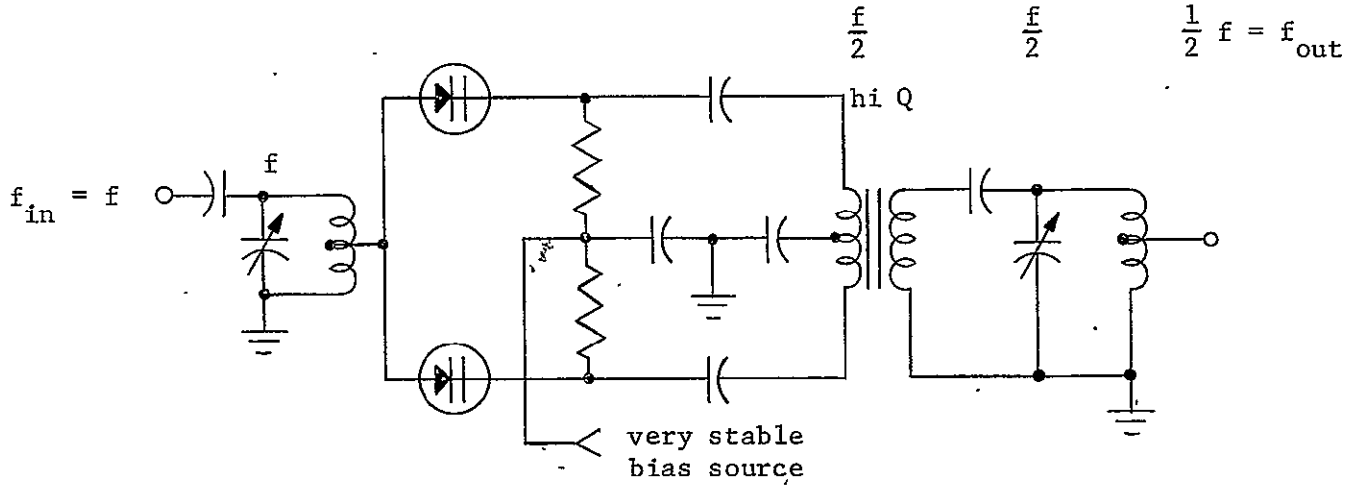
Approximate Equivalent of S-Band Power Doubler

Input impedance is transformed by a short conductive tap on the input cavity line. The input resonator loaded Q is set by the series capacitor, and at the same time provides a high impedance to the 2f current preventing it from flowing out the input port. Second harmonic power developed in the diode is coupled into the output resonator by a similar (but smaller) series capacitor. Both resonators are parallel tuned with end loading plugs which increase the capacity and reduce the equivalent inductance at the same time. These plugs yield rigid support to the cavity center pins and preclude large amounts of phase variance due to vibration influence. S-Band power is finally transformed to 50 ohms by a similar capacitive transformation. The output power is passed through a three section output filter. Bias is provided to a 10 kilohm resistor for isolation and then to a potentiometer to the cavity. This vernier bias is available for fine tuning of the doubler, and results in a means of final envelope shaping after all modules are mounted in the system housing. The diode is a reversible welded microwave cartridge. It is secured into the doubler housing by means of locked set screws, and has an intimate thermal path to the major assembly. This diode is of the conventional graded junction type possessing a good history of S-Band applications.

Unusual Passive Multipliers

Two frequency multipliers employed in the transponder should be classified as being somewhat unusual in regards to the method used. The multiply by one-half (or divide by two) module is a passive rational fraction generator. It is used in the reference channel to feed the phase detectors. The other unusual multiplier is the multiply by nine circuit employed in the first mixer (S-Band) local oscillator chain. This module uses a step-recovery diode in a triple-tuned cavity. No idler circuits are required.

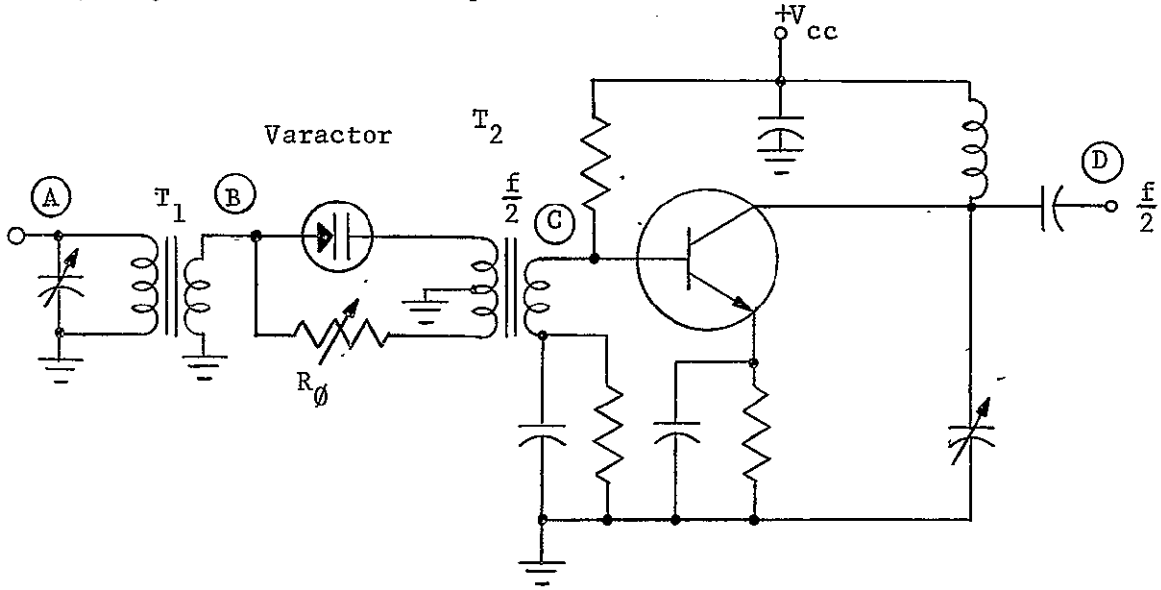
The X½ multiplier is an outgrowth of the more common, bi-phase divider circuits presented in other literature and as used by JPL. These divide-by-two circuits perform as follows:



ORTHODOX VARACTOR DIVIDE BY TWO

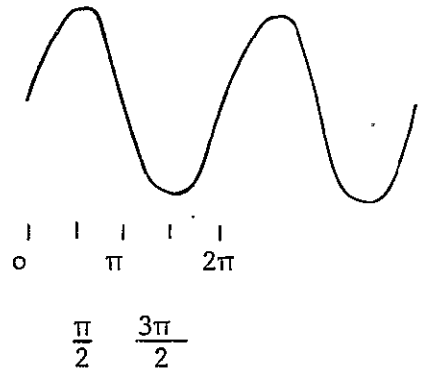
The input signal (f.) is introduced in phase to a push pull varactor configuration. The output includes of a tuned bridge with a rather high Q, carefully balanced and resonant at ½ f. The varactors are selected, and the driving power established such that the diodes are driven into the negative resistance region as utilized in the operation of parametric amplifiers. When the negative resistance exceeds the loop resistors loss, the ½ f loop oscillates and output is available at ½ f. The output is phase synchronous for the divide-by-two case as shown by Penfield and Rafuse in the text "Varactor Application". It may be seen that these circuits are quite sensitive to minor fluctuations in the following: (1) drive level, (2) device parameters, (3) load impedance, (4) bias setting, and (5) Q-factor of the oscillatory arm in particular.

These reasons engendered another approach. A single diode, reactive frequency divider was developed as shown:



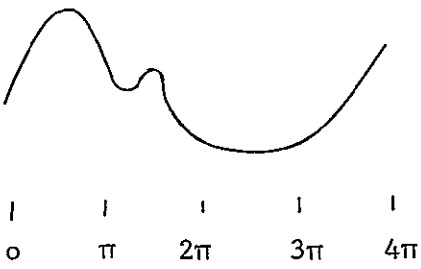
Power is applied to the circuit by T_1 at frequency f. The energy drives the varactor in the resistor-varactor bridge toward the forward biased direction. (See Sine Wave A) from 0 to π/2.

SINEWAVE A



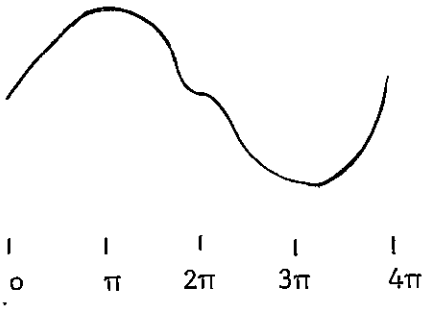
Increasingly large amounts of charge are stored, the reverse bias disappears and forward contact potential $\emptyset$ is approached. The input sin at f reverses, ($\pi/2$ to $3\pi/2$) and the diode essentially disconnects from the energy source. The varactor capacity had increased sufficiently to tune the resonant circuit to ½ f. The stored change is now available in the ½ f resonant circuit. The period of occurrence is quite short, but it is long enough to produce sub-frequency distortion on the drive frequency wave across the varactor. (See Wave Form B).

WAVEFORM B



The bridge resistor is adjusted to approximately the value of effective R_{in} for the varactor at f. This balance helps to cancel out the drive frequency at the output terminals of the bridge transformer T_2. This transformer is very tightly coupled (bi-filar wound) and must also be carefully balanced. The output wave form T_2 is a much cleaner wave comprised largely of ½ f. (shown as waveform C)

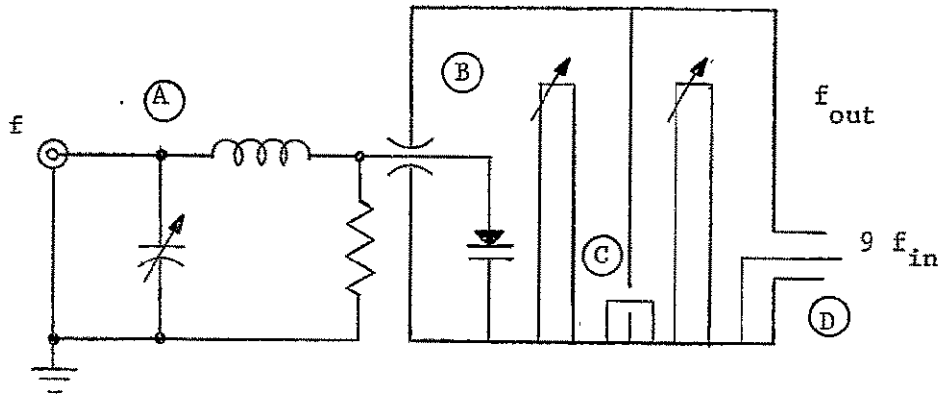
WAVEFORM C



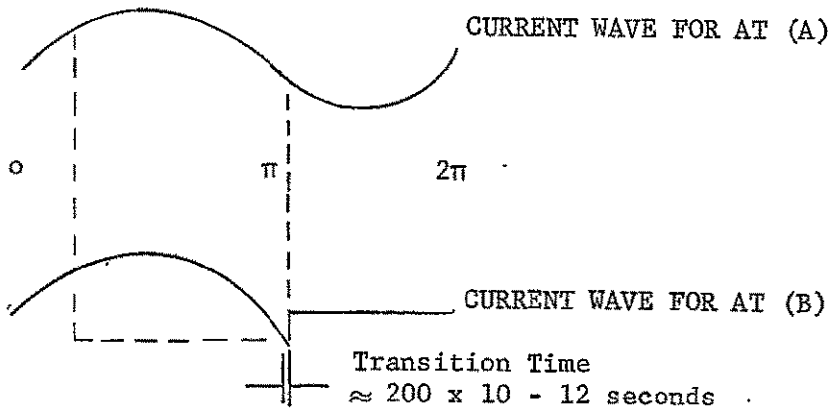
The new frequency is truly generated in the varactor T_1 circuit, and is not an apparent infraction of the Fourier analysis which predicts that no sub-harmonic power is available in any given sine wave. A filtering amplifier produces the final wave required at ½ f.

This divider is by far less critical in regards to drive level, complex impedance at the terminals or even the diode itself. An input variation of 10 db simply produces linear output level variations, and not an off or on situation as with the other approach. This provides considerably more reliability.

The high-order, multiply-by-nine module required for the first mixer S-Band Local Oscillator is a step-recovery diode. This type of multiplier attains quite high harmonic conversion efficiency without the use of any idler circuits. An X9 varactor would require three idlers in addition to the impedance matching and filtering requirements. Circuit stability and bandwidth are both improved by using the non-idled step-recovery diode approach.



The simplified schematic shows an input matching network, the diode imbedded in a resonant cavity which in turn selects and filters the desired output signal for S-Band LO injection. The wave at A simply shows the sinusoidal driving current ($I_1 . \sin \omega_1 t$) which is supplied at 228 mc from a buffer amplifier. A study of wave B exhibits a very rapid current change which occurs in something like 200 picoseconds or less.



From a study of the Fourier expansion of a sawtooth wave with a step transition, that all harmonics of the fundamental current, through and including the n^{th} harmonic are present. It is simply a matter of impedance matching and extracting this 9th harmonic.

The cavity design is very similar to those of the microwave power miltipliers used in the transmitter chain. It is a separate module, physically and operationally independent of the major housing. Output power is loop coupled to a miniature coax cable which interconnects with the first mixer.

Section 3

RECOMMENDATIONS ON TRANSPONDER PROTOTYPE MODEL

3.0 The prototype transponder for which this report is written met almost all of the intended specifications and was quite successful in the areas of basic operations, such as sensitivity. However, there are areas in which further efforts could result in improved specifications.

3.1 Power Supply

In order to facilitate the redesigns and testing that was required to eliminate the high frequency voltages associated with square wave ripples on the power lines, the prototype transponder's power supply has been mounted in a separate housing. By using smaller components, and using shielded cables on the internal power leads, it could be repackaged into the main transponder housing.

The ripple on the power supply output has been reduced below 50 μv, thereby effectively eliminating the phase noise previously caused by these ripple frequency components entering into the receiver system.

3.2 Telemetering

The phase error telemetry output has phase noise caused by reverse feedthrough of the 10 kc chopper frequency components passing through the telemetry amplifier to the VCXO. By placing a filter between the VCXO and telemetry circuits, this could be eliminated. The lock indicator telemetry has an inaccuracy caused by the Quad phase detector and the acquisition amplifier having an impedance mismatch that can be corrected by a simple isolation amplifier.

The signal level telemetry has an interface impedance mismatch between the signal sensing amplifier output and its telemetry amplifier that can also be corrected by a simple isolation amplifier.

Section 4

BIBLIOGRAPHY

4.0 The following is a list of references intimately associated with this contract during the course of progress. They are not included as deliverable items of this final report.

4.1 NASA Contract NAS8-11509 dated 29 June 1963 with modifications 1 dated 23 July 1963; modification 2 dated 15 December 1963; modification 3 dated 4 May 1964; TWX from NASA (Mr. McKinney) dated 8 October 1964.

4.2 Progress Reports 1 through 16 (Particularly Progress Report No.15)

4.3 Special Technical Report No. 1 dated July 1964.

4.4 Preliminary Study Report dated March 1964.

4.5 "Theory of Phaselock Techniques", by Gardner and Kent - Contract NAS8-11509.

4.6 Resdel Engineering Bid Request Quotation BR 2171.

4.7 Resdel Engineering Internal Report TR-13 on W.O. 101130 D "Considerations of AGC versus Limiting as a Means for Gain Control" dated 12 November 1964.

Section 5

APPLICABLE DRAWINGS

5.0 The following drawings are included as a part of this report.

5.1 Drawings Identification 91242 (sheet 2 of 3)

5.2 Schematics

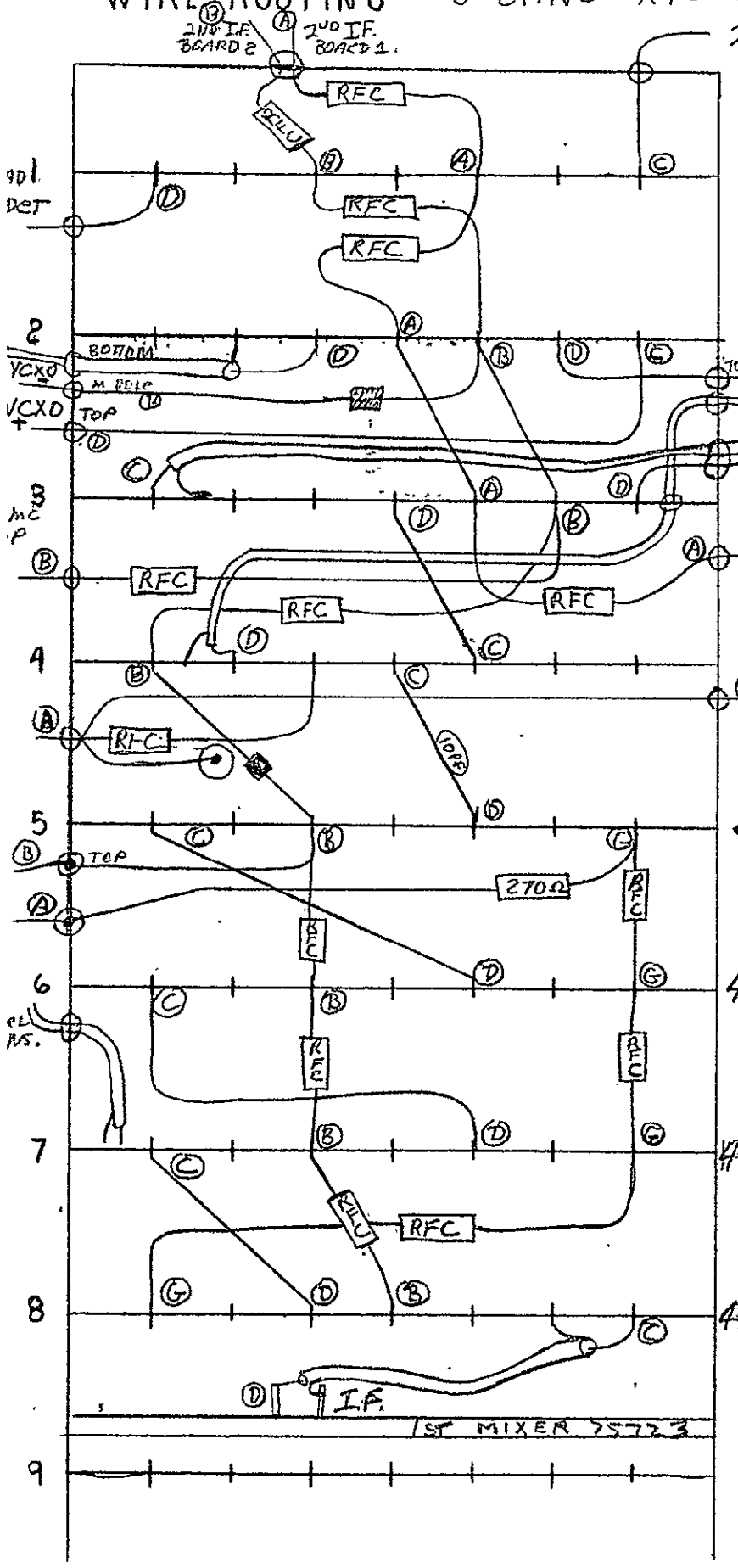
System Block Diagram	20675
RF Input and 1st IF (Section 200)	20667
2nd IF Amplifiers (Section 300)	20666
Loop and Sweep (Section 400)	20670
VCXO (Section 500)	20671
Reference Signal Amps (Section 600)	20673
Local Oscillator String (Section 700)	20692
X5 and Power Amp (Section 800)	20690
Transmitter Multipliers (Section 900)	20691
Power Supply (Section 1000)	20695
Telemetry Amps (Section 1100)	20694

5.3 Miscellaneous

Outline Drawing	91242 (sheet 3 of 3)
Wire Routing	76353
Electrical and Board Assembly (Photo)	76133
1st Mixer	75723
Input/Output Bandpass Filters	75212
VCXO	75725

WIRE ROUTING - S-BAND XPONDER

NO. 76353



9 9/16 QUAD AMP 76067

19MC BUFFER 75745

47 13/16 I.F., 4th 75991

47 13/16 I.F. 3RD 75990

47 13/16 I.F. 2nd 75989

47 13/16 I.F., 1st 75988

A = +15 VDC
B = -15 VDC
C = INPUT
D = OUTPUT
E = -5.6 VDC
F = +12 VDC
G = +6 VDC
H = +28 VDC
I = -28 VDC
J = +50 VDC
K = -50 VDC
L =
M =
N =
O =
P =
Q =
R =
S =
T

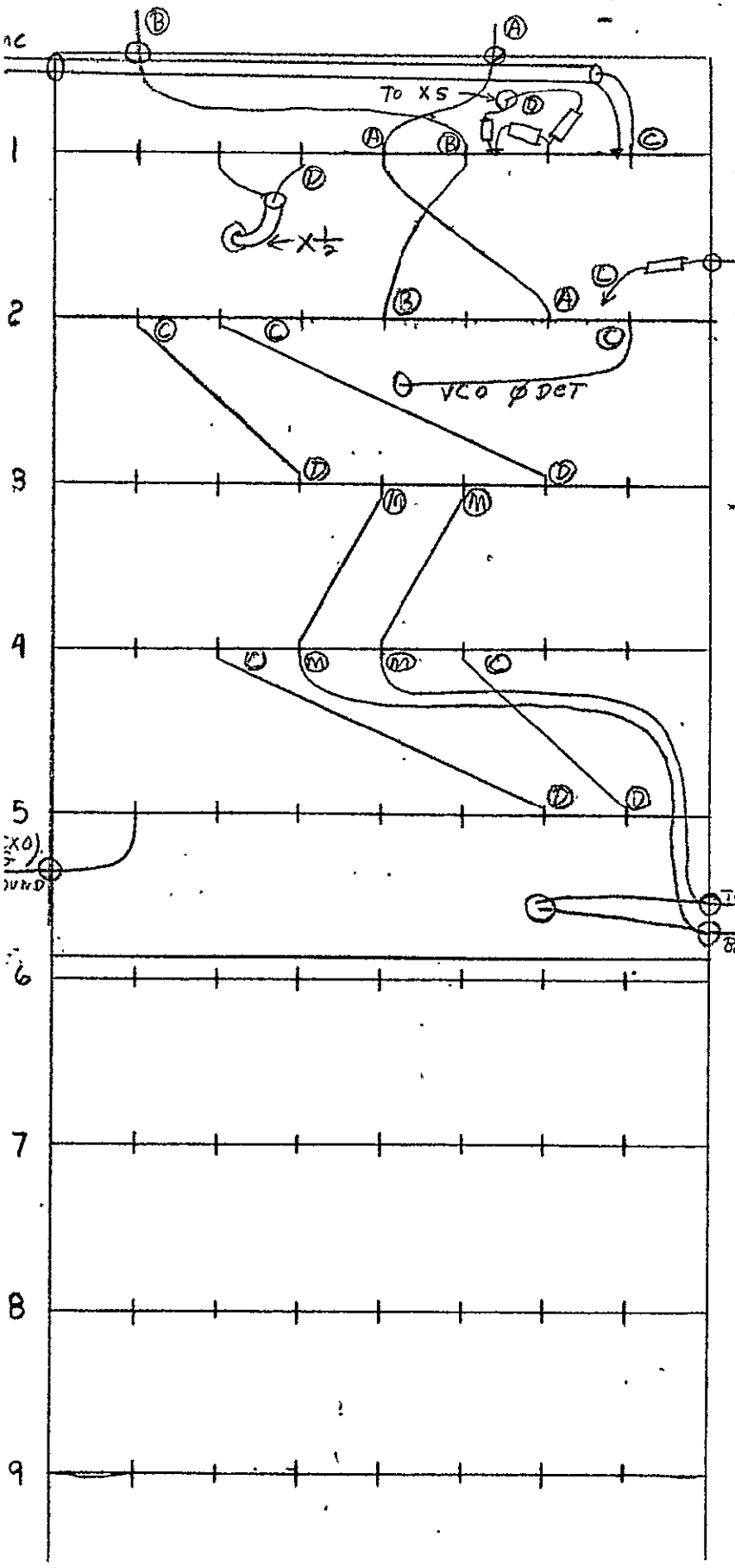
⊙ = AB FEED THRU

⊙ = HOLE FEED

T. O'Hara
12-31-64

WIRE ROUTING - S-BAND TRANSPONDER

NO. 76353



19 MC BUFFER 75766

SIG. SENS

SIG. LEV. TELEM. 75997

SIG LEV TEL 75998

ϕ ERROR TEL 75994

ϕ ERROR TEL 75995

TO QUAD TELEM.

A = +15 VDC
B = -15 VDC
C = INPUT
D = OUTPUT
E = -5.6 VDC
F = +12 VDC
G = +6 VDC
H = +28 VDC
I = -28 VDC
J = +50 VDC
K = -50 VDC
L =
M = 10 KC
N =
O =
P =
Q =
R =
S =
T

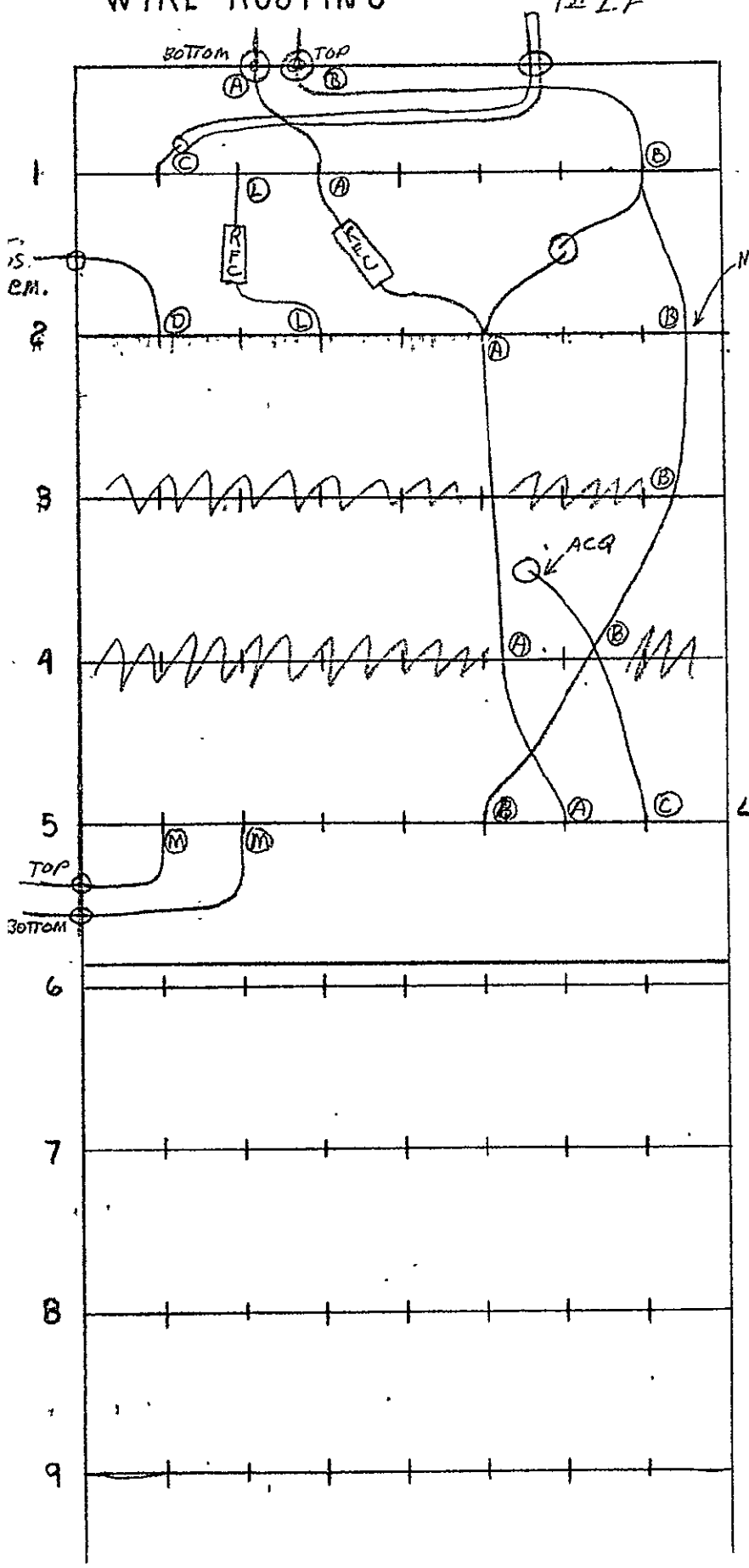
= AB FEED THRU

= HOLE FEED

T. D'Hara
12-31-64

WIRE ROUTING -

NO. 76353



LOGIC
SIG. SENS. 1ST
76248

SIG SENS. 2ND
76249

LOGIC/IND. TELEMETRY
75996

A = +15 VDC
B = -15 VDC
C = INPUT
D = OUTPUT
E = -5.6 VDC
F = +12 VDC
G = +6 VDC
H = +28 VDC
I = -28 VDC
J = +50 VDC
K = -50 VDC
L = AGC
M = 10 KC
N =
O =
P =
Q =
R =
S =
T

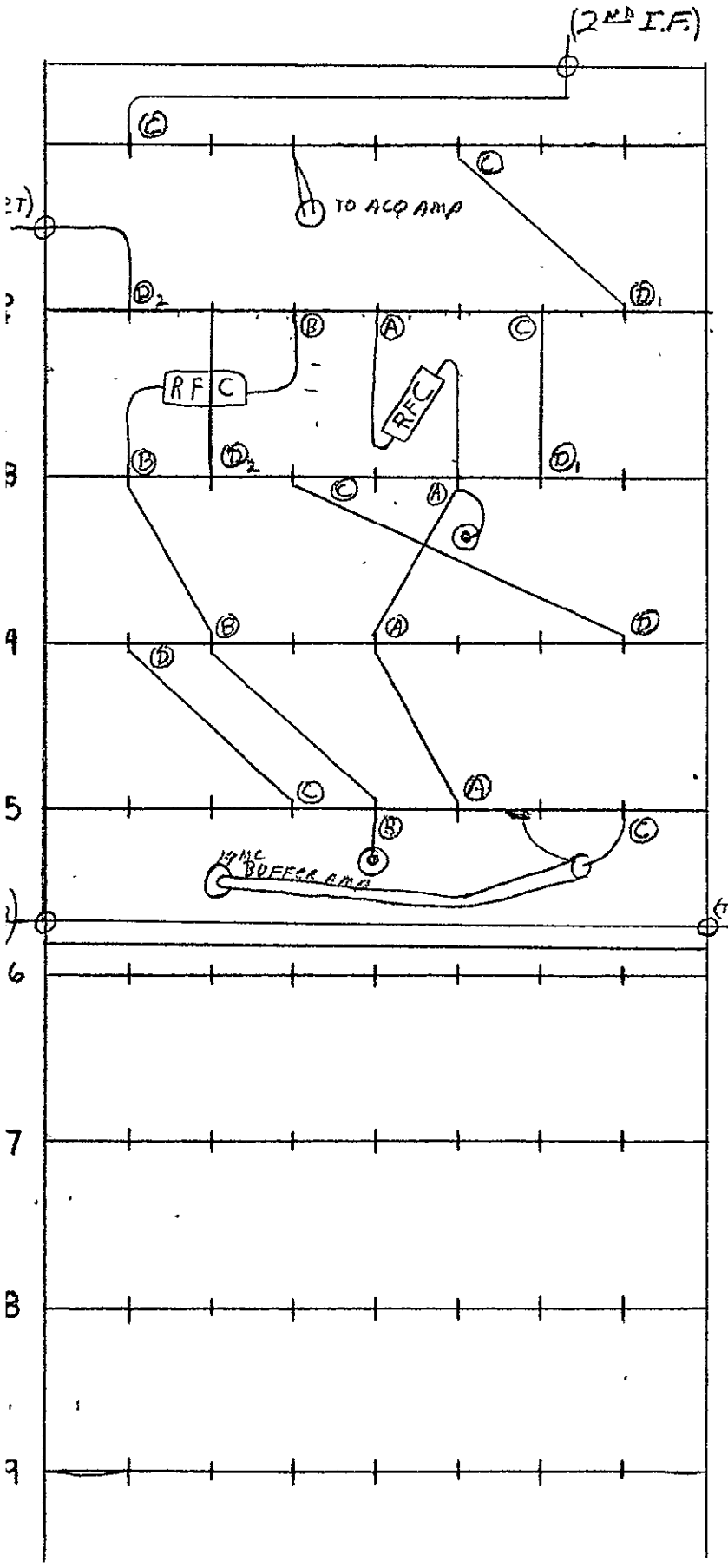
= AB FEED THRU

= HOLE FEED

T. O'Hara
12-31-64

WIRE ROUTING - S-BAND XPONDER

NO. 76353



QUAD Ø DET
75786

REF AMP
75782

Ø SHIFTER 90°
75783

X½, 2nd
75762

X½, 1ST
75761

A = +15 VDC
B = -15 VDC
C = INPUT
D = OUTPUT
E = -5.6 VDC
F = +12 VDC
G = +6 VDC
H = +28 VDC
I = -28 VDC
J = +50 VDC
K = -50 VDC
L =
M =
N =
O =
P =
Q =
R =
S =
T

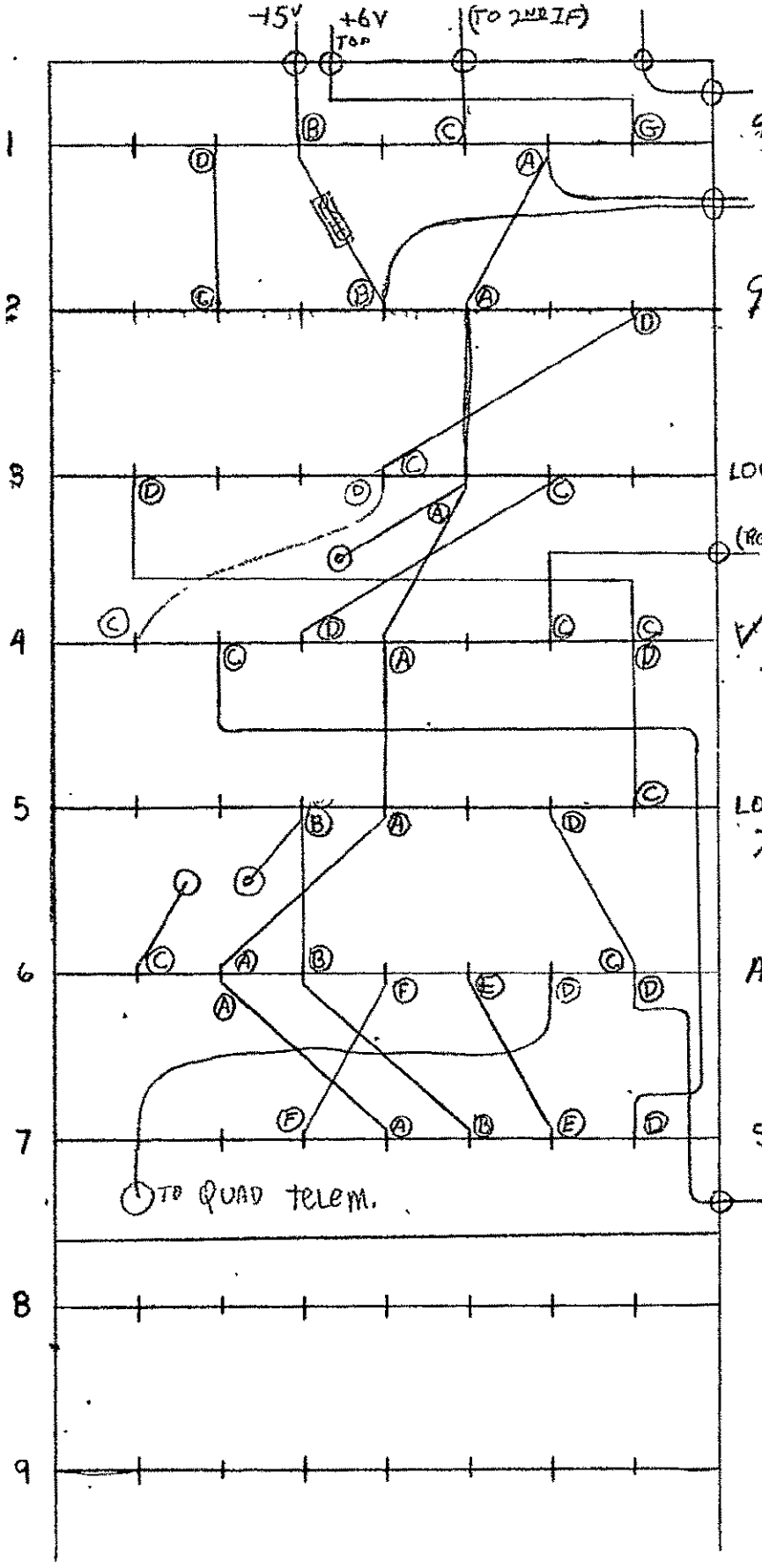
= AB FEED THRU

= HOLE FEED

T. O'Kane
12-31-64

WIRE ROUTING - S-BAND XPONDER

NO. 76353
PAGE 5 OF 7



Red A = +15 VDC
Orange B = -15 VDC
Yellow C = INPUT
D = OUTPUT
Blue E = -5.6 VDC
Violet F = +12 VDC
Green G = +6 VDC
White H = +28 VDC
Black I = -28 VDC
J = +50 VDC
K = -50 VDC
L =
M =
N =
O =
P =
Q =
R =
S =
T

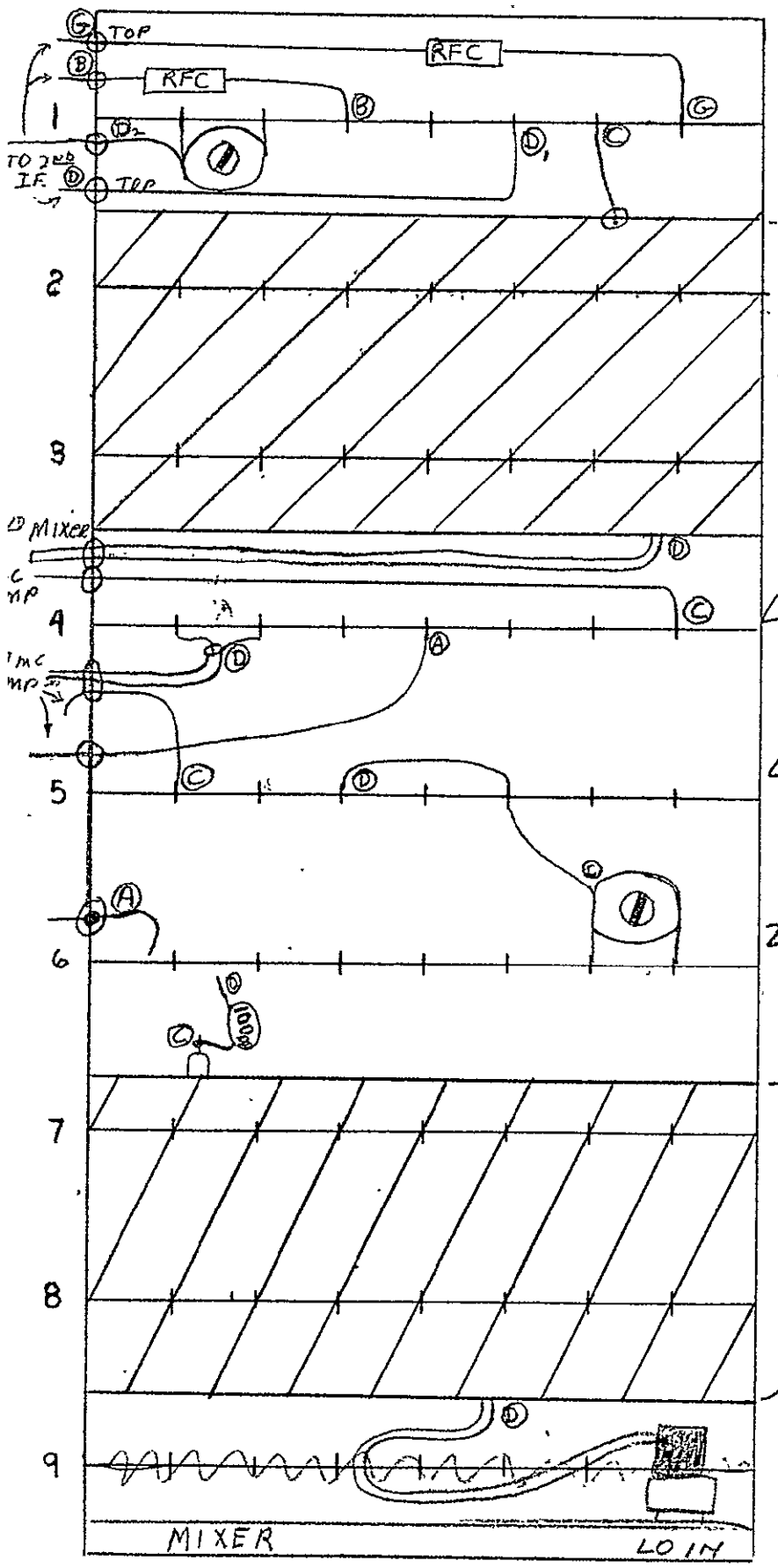
= AB FEEDTHRU

= HOLE FEED

T. O'Hara
12-31-64

WIRE ROUTING - S-BAND XPONDER

NO. 76353



9/16 AMP
75726

BP FILTER
76032

BP FILTER
75992

LO X3
75750

LO X4
75897

229 POWER AMP
75899

X9 MULTIPLIER
75898

A = +15 VDC
B = -15 VDC
C = INPUT
D = OUTPUT
E = -5.6 VDC
F = +12 VDC
G = +6 VDC
H = +28 VDC
I = -28 VDC
J = +50 VDC
K = -50 VDC
L =
M =
N =
O =
P =
Q =
R =
S =
T

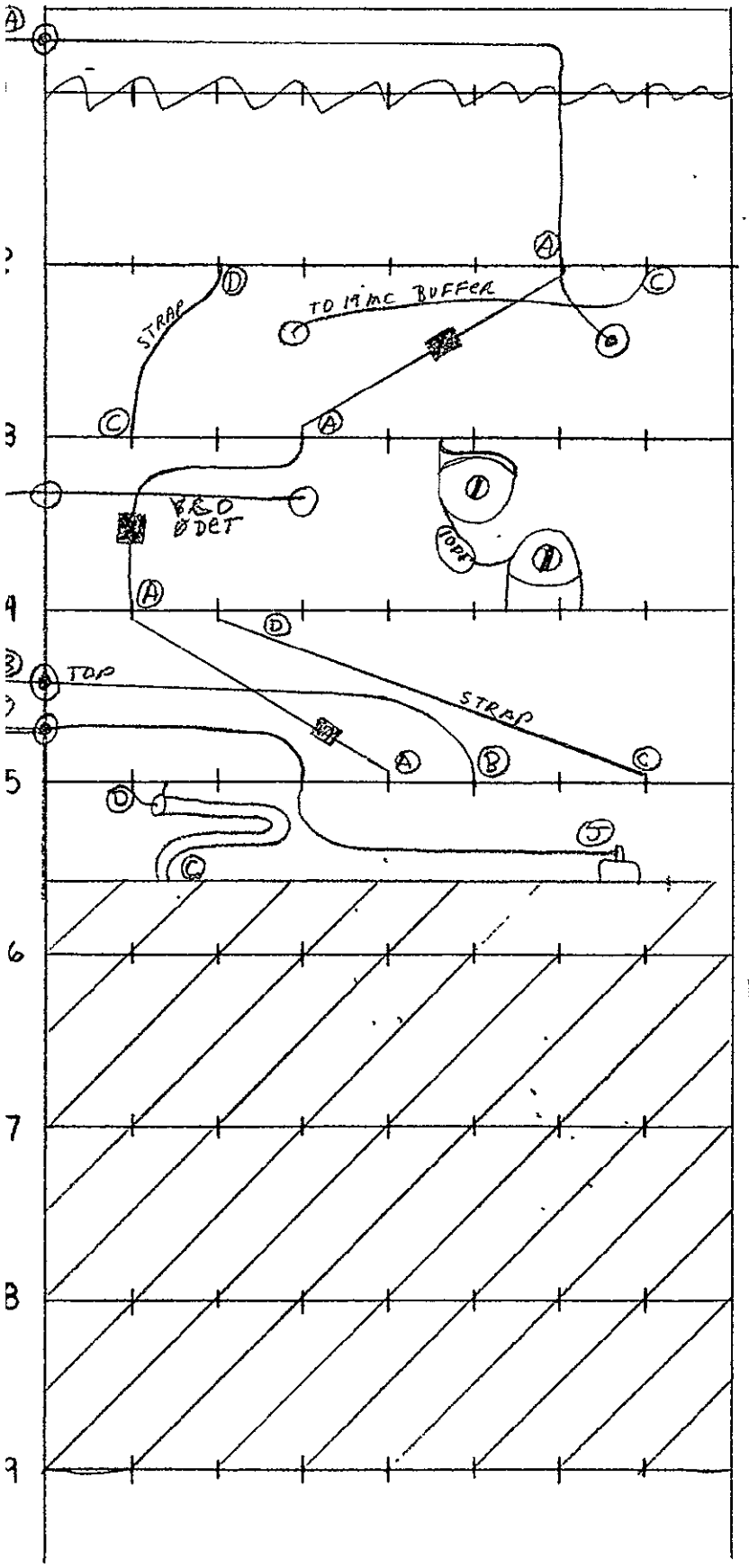
= AB FEED THRU

= HOLE FEED

T. O'Hara
12-31-64

WIRE ROUTING - S-BAND XPONDER

NO. 76353



X5, 1ST
75849

X5, 2nd
75864

95AMP, 1ST
75902

95AMP, 2nd
75903

POWER
AMPLIFIER
75904

A = +15 VDC
B = -15 VDC
C = INPUT
D = OUTPUT
E = -5.6 VDC
F = +12 VDC
G = +6 VDC
H = +28 VDC
I = -28 VDC
J = +50 VDC
K = -50 VDC
L =
M =
N =
O =
P =
Q =
R =
S =
T

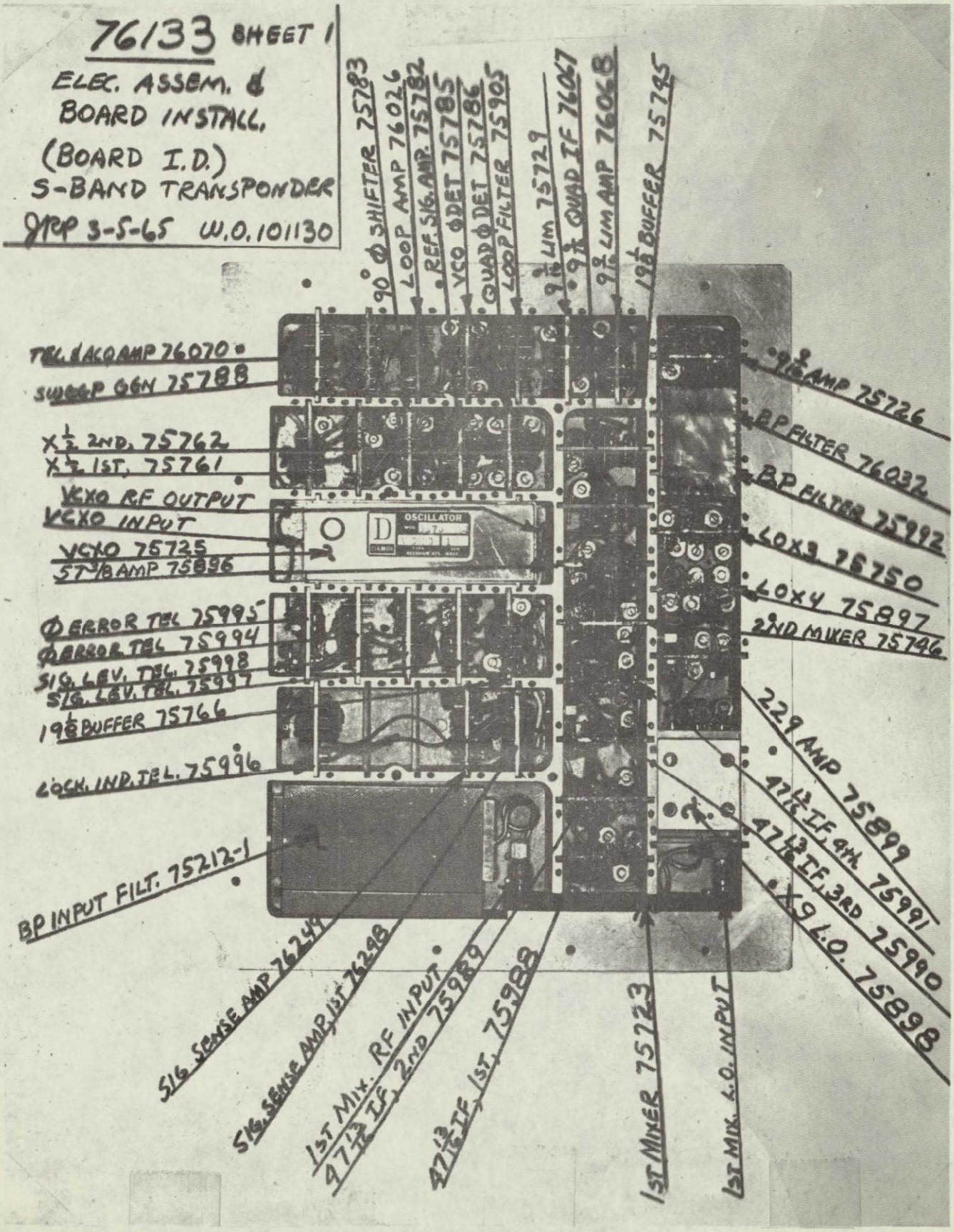
⊙ = AB FEED THRU

⊙ = HOLE FEED

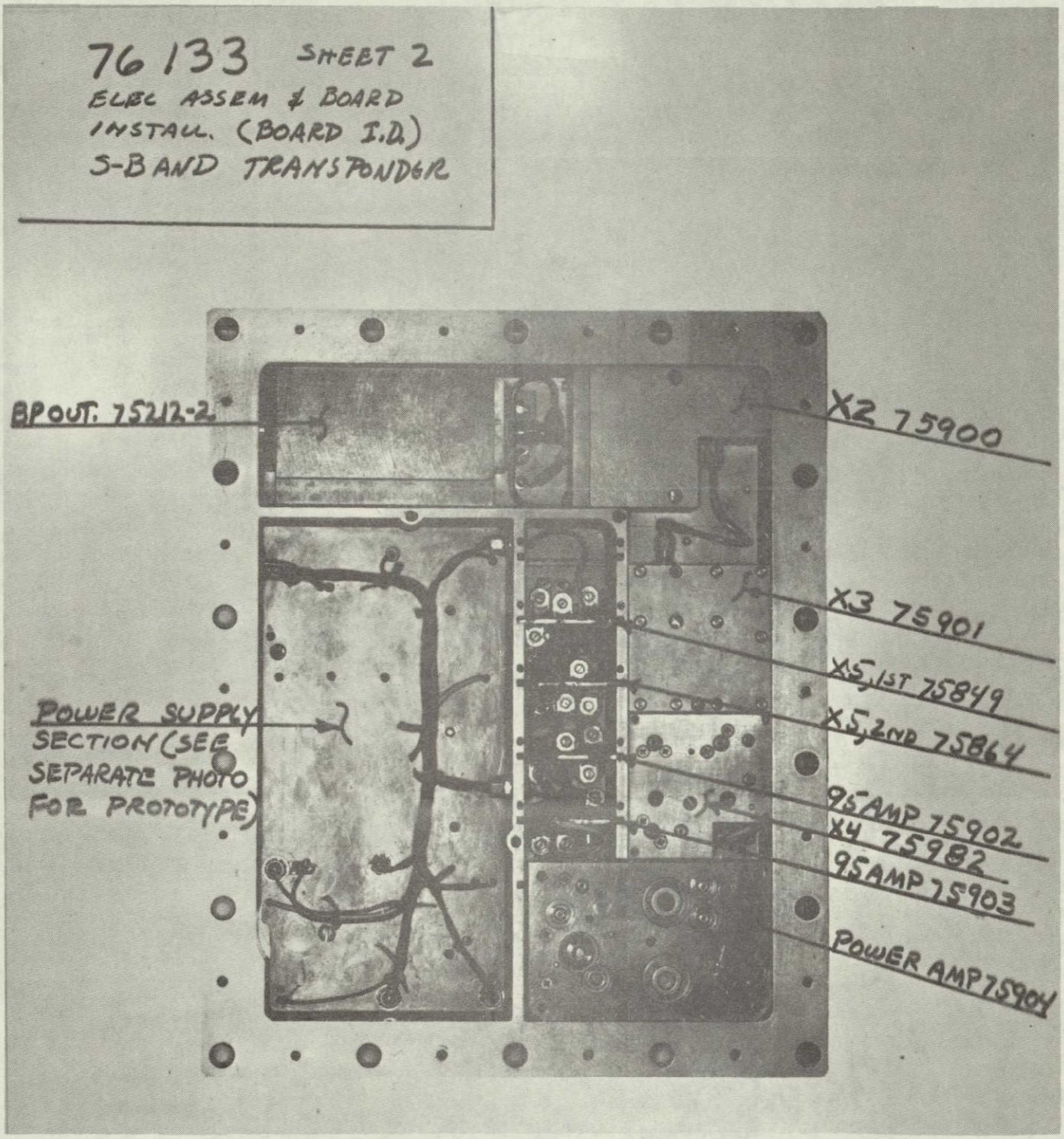
T. O'Hara
12-31-64

76133 SHEET 1

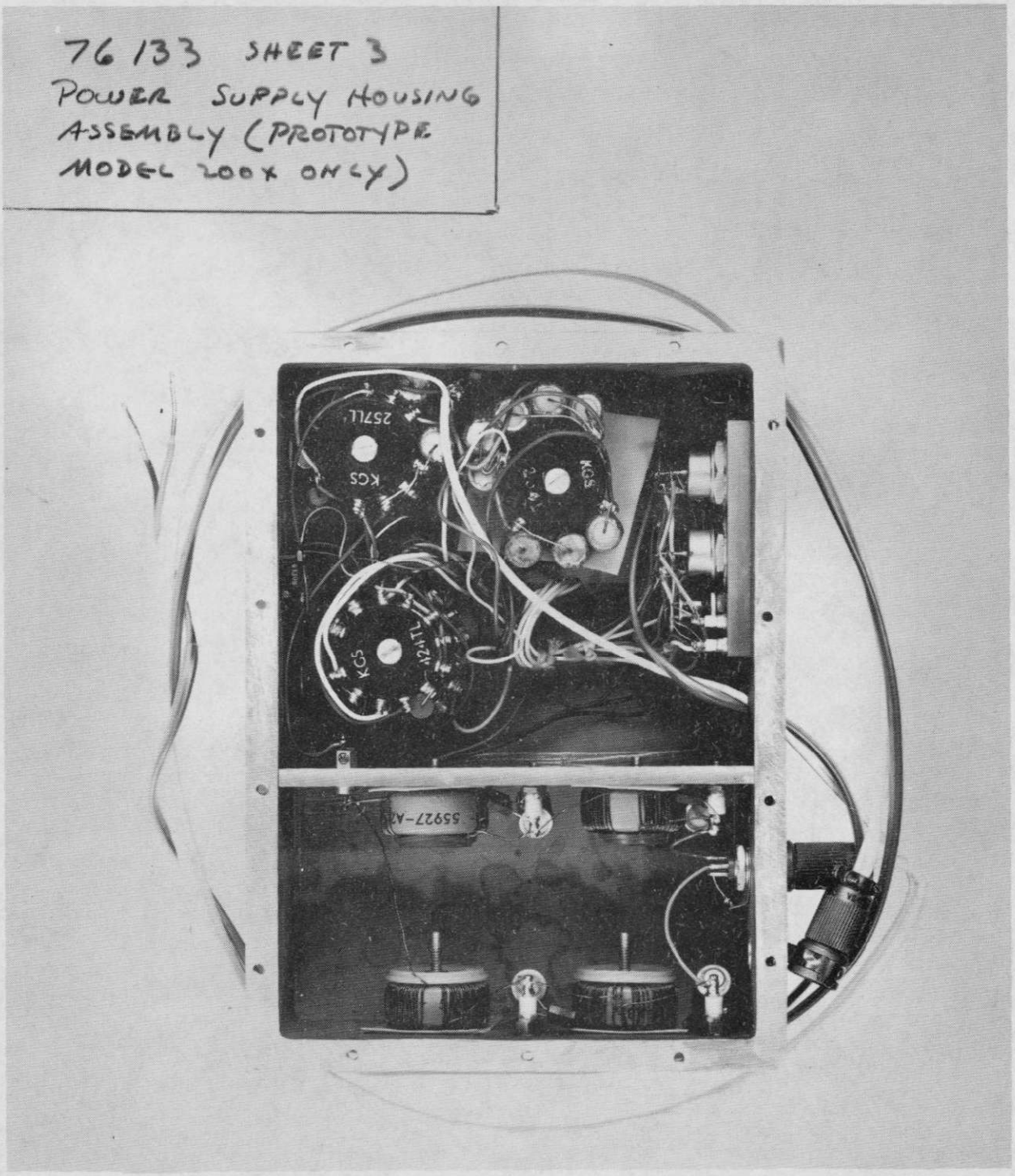
ELEC. ASSEM. & BOARD INSTALL. (BOARD I.D.)
S-BAND TRANSPONDER
JPP 3-5-65 W.O. 101130



76133 SHEET 2
ELEC ASSEM & BOARD INSTALL. (BOARD I.D.)
S-BAND TRANSPONDER



76 133 SHEET 3
POWER SUPPLY HOUSING ASSEMBLY (PROTOTYPE MODEL 200X ONLY)



Section 6

PROTOTYPE MEASUREMENTS & DATA

6.0 The following section consists of the Final Test Procedures 61148 and data taken on the prototype transponder S/N 100X.

DWG NO. 61148

The final tests for the S-Band transponder Resdel Model 91242 are intended to demonstrate the conformance to the design parameters of contract NAS8-11509.

Portions of the tests will be conducted with false covers on the transponder since no provisions for external test points have been made. Certain internal connections will have to be made at different steps in the testing procedure.

1.1 Sensitivity

1.11 Dropout Threshold Sensitivity

Hookup as in figure 1.

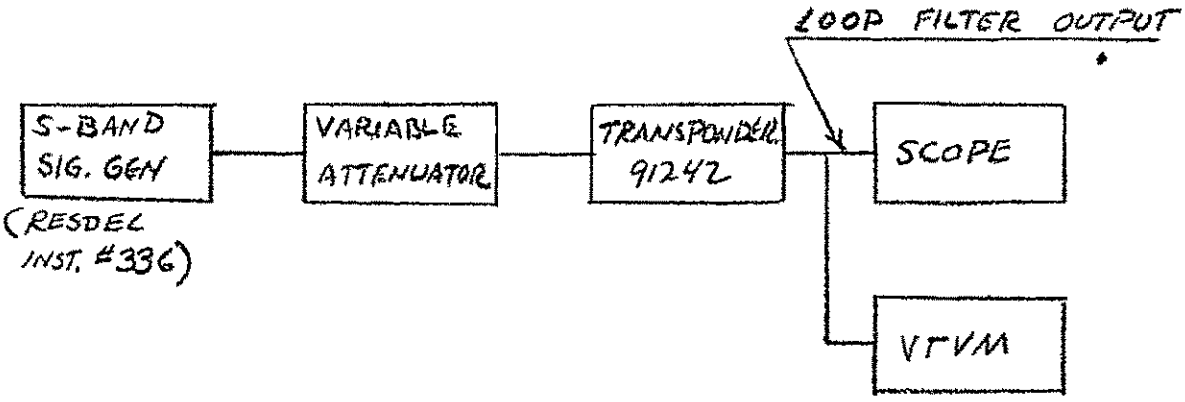


FIGURE 1

Obtain a locked on signal condition at center frequency by setting the sig gen at its calibrated center frequency and increasing signal level input. Decrease sig gen input until lock is lost. This is noted by observing the VTVM as a sudden variation in voltage from that voltage value noted in the locked condition or by observing the scope as a sudden increase in noise signal. Record the value of input signal in DBM as "absolute threshold sensitivity".

Adjust frequency of sig gen to +250 kc off center frequency. Increase signal level until lock is again obtained. Decrease signal level until lock is just lost. Record as "plus dropout threshold sensitivity".

Repeat for -250 kc off center frequency and record as "minus dropout threshold sensitivity".

1.12 Acquisition Sensitivity

Adjust frequency of sig gen to center frequency. Decrease signal level until lock is lost. Now slowly increase signal level until automatic acquisition is accomplished. Record as "absolute acquisition sensitivity".

Repeat for +250 kc off center frequency and record as "plus acquisition sensitivity".

Repeat for -250 kc off center frequency and record as "minus acquisition sensitivity".

1.2 Lock-On Range

Use same hookup in Figure 1. Adjust signal level input to -110 DBM and center frequency. Adjust frequency in a plus direction until lock is lost. Record frequency.

Repeat for minus frequency at -110 DBM.

Repeat plus and minus frequency lock on measurements for -80 DBM, -60 DBM, -40 DBM, -20 DBM, and 0 DBM.

1.3 Tracking Rate (Acceleration Capability)

Use same hookup as figure 1 except provide for an injection of ramp modulation into the sig gen.

Adjust sig gen frequency for center frequency and -120 DBM signal level and obtain a locked signal condition.

Adjust the ramp modulation for the correct voltage to produce a frequency swing of approximately 20 kc. Use the calibrated chart for the signal generator and the scope to make this adjustment.

Increase the ramp frequency until an unlocked condition occurs. Record as center tracking rate.

Repeat for plus 250 kc from center frequency.

Repeat for minus 250 kc from center frequency.

1.4 Acquisition Time

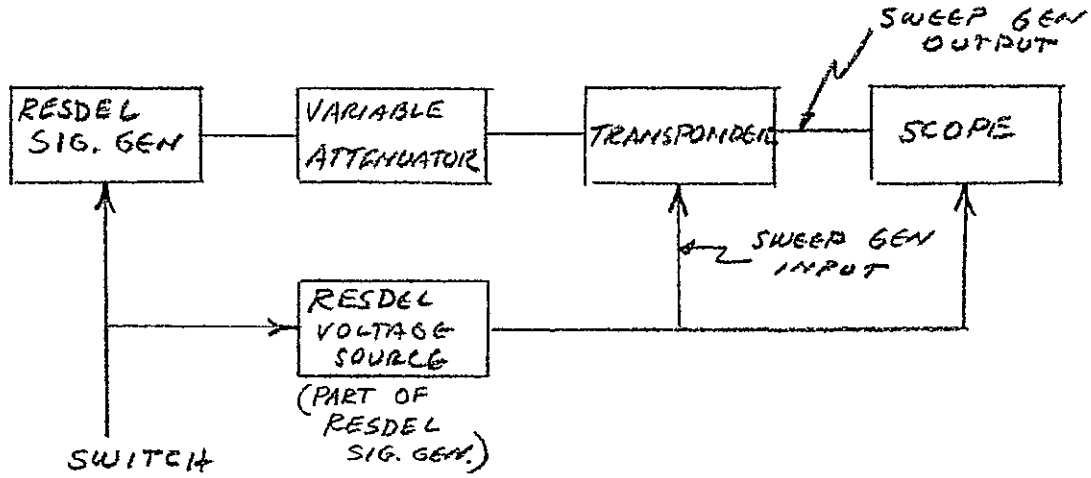


FIGURE 2

Hookup as in Figure 1. Set sig gen at center frequency and -60 DBM and obtain a lock condition. Hookup as in Figure 2. Throw switch to on position and measure the time in seconds from the start of the sweep to the stop of the sweep.

Repeat for plus and minus 250 kc from center.

Repeat for -100 DBM and -120 DBM.

1.5 Maximum Input Signal

Hookup as in Figure 1 and obtain locked condition at center frequency. Increase input signal level until "deterioration" of output starts. Record as maximum center frequency input signal.

Repeat for plus and minus 250 kc from center.

1.6 Output Power

Hookup in Figure 3.

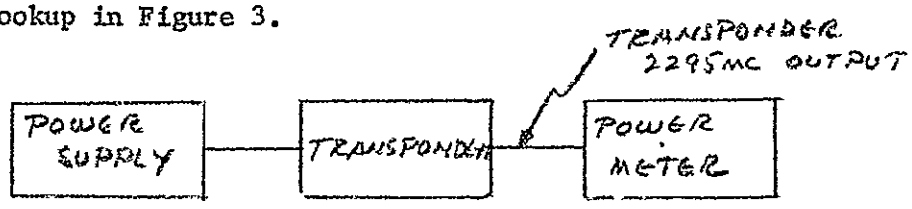


FIGURE 3

DWG NO. 61148

Set power supply for +28 volts. Read power output. Repeat for +25 and +31 volts.

1.7 Primary Power

Hookup in Figure 3. Measure primary power current at +25, +28, +31 v.

1.8 Telemetry Test Points

1.8.1 Lock Indication

Hookup in Figure 4.

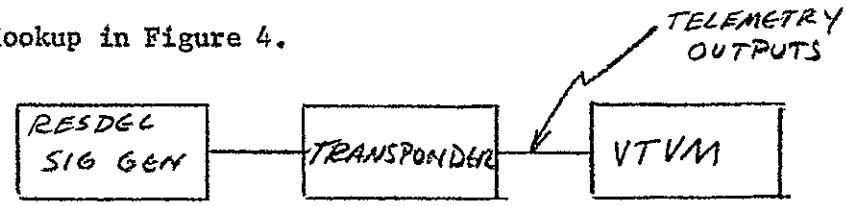


FIGURE 4

Measure telemetry voltages at input signal levels of -120 DBM, -100 DBM, -60 DBM.

1.8.2 Phase Error

Repeat 1.8.1.

1.8.3 Signal Level

Repeat 1.8.1 for every 10 DBM from -120 DBM to 0 DBM.

TEST DATA SHEET

Unit S-BAND TRANSPONDER By UBRon

Model 91242 Date 2-25-65

S/N 100X (PROTOTYPE) Approved JKP

Paragraph

1.1.1 Threshold Sensitivity

Absolute Dropout Threshold Sensitivity -121 DBM (>120)

Plus Dropout Threshold Sensitivity -120 DBM (>120)

Minus Dropout Threshold Sensitivity -119 DBM (>120)

1.1.2 Acquisition Sensitivity

Absolute acquisition sensitivity -110 DBM (>110)

Plus acquisition sensitivity -109 DBM (>110)

Minus acquisition sensitivity -110 DBM (>110)

1.2 Lock on Range

Signal Level	Plus Lock on Range (>250 kc)	Minus Lock on Range (>250 kc)
-110 DBM	2113.9093	2112.6548
-100	↓	↓
-80		
-60		
-40		
-20		
0		

1.3 Tracking Rate

Center Frequency tracking rate ___>1000___ Cycles (>50)

Plus 250 kc tracking rate ___>1000___ Cycles (>50)

Minus 250 kc tracking rate ___>1000___ Cycles (>50)

1.4 Acquisition Time

	-60 DBM	-100 DBM	-120 DBM
Center Frequency	sec.(<.3) 0.1	sec.(<.3) 0.1	sec.(<3) 0.2
Plus 250 kc Frequency	0.1 sec.(<.3)	0.1 sec.(<.3)	0.2 sec.(<.3)
Minus 250 kc Frequency	0.1 sec.(<.3)	0.1 sec.(<.3)	0.2 sec.(<.3)

1.5 Maximum Input Signal

	Maximum Input Signal
Center frequency	DBM (>-7DBM) > -4
Plus 250 kc Frequency	DBM (>-7DBM) > -4
Minus 250 kc Frequency	DBM (>-7DBM) > -4

1.6 Output Power

	+25V	+28V	+31V
Power	1.6 W (>1W)	1.7 W (>1W)	1.7 W (>1W)

1.7 Primary Power

	+25	+28V	+31V
Current	4.8 amp	4.0 amp	3.9 amp
Watts	W.(95) 110	W.(95) 110	W.(95) 100

1.8 Telemetry Test Points

1.8.1 Lock Indication

	Volts
-120 DBM	Not Measured
-100	
-60	

1.8.2 Phase Error

	Volts
-120	Not Measured
-100	
-60	

1.8.3 Signal Level

	Volts		
-120	Not Measured	-60	
-110		-50	
-100		-40	
-90		-30	
-80		-20	
-70		-10	
		0	

DWG NO. 61148

Temperature Test

1. Start at ambient of 25°C. At primary voltage of +28V, measure:
   a. Threshold V and acquisition sensitivity at center frequency
   b. Power output (repeat for +25V & +31V)
   c. Primary power (repeat for +25V and +31V)
   d. Lock-on Range
   e. Maximum input signal
   f. Telemetry test points at -100 DBM sig level
2. Repeat at +50°C, +70°C, +85°C, +100°C, 0°C, -20°C.

		-20°C	0°C	+50°C	+70°C	+85°C	+100°C	+25°C
Threshold Sensitivity		-119dbm	-120	-118	-115	-110	-105	-121
Acquisition Sensitivity		-109	-110	-107	-105	-105	-105	-110
Power Output	25	1.6	1.6	1.1	0.6	0.7	0.25	1.6
	28	1.7	1.7	1.1	0.6	0.7	0.25	1.7
	31	1.7	1.7	1.1	0.6	0.7	0.25	1.7
Primary Power	25							
	28	110w.	110	110	110	110	110	110
	31							
Lock On Range	Plus	2113.9	→	→	→	→	→	→
	Minus	2112.6	→	→	→	→	→	→
Maximum Inp. Signal		7-4	→	→	→	→	→	→
Telemetry	Lock on	Not Measured						
	Error							
	Sig Level							

Section 7

TECHNICAL REPORT

7.0 This appendix includes an outstanding Resdel internal report TR-13 on "Consideration of AGC versus Limiting as a means for Gain Control" dated 12 November 1964. Of special interest is the portion including a memorandum from Mr. Richard Jaffe, a well known and recognized expert in the phase-lock field to Mr. Donald Gehlke, Vice President in charge of Engineering and manufacturing at Resdel Engineering Corporation. This memo includes an excellent theoretical treatment of probability of false lock conditions in phase lock systems.

RESDEL ENGINEERING CORPORATION INTERNAL REPORT REC-TR-13
"CONSIDERATIONS OF AGC VERSUS LIMITING AS A MEANS FOR GAIN CONTROL"

By James Pourtales, November 12, 1964

This report is a gathering of various data and extractions from other pertinent reports. It deals specifically with applications to the Resdel 91242 transponder of AGC, limiting, and other considerations involving Booster Tracking Transponders. It includes the following:

1. Resdel Internal Report "Considerations of Limiting versus AGC as a means for gain control in Phase Lock Systems" by J. Pourtales dated November 12, 1964.

2. Extract of pages 8-18 through 8 - 21 of "Theory of Phaselock Techniques as applied to Aerospace Transponder" by Gardner and Kent, Contract NAS8-11509.

3. Extract of pages 4 - 1 through 4 - 4 and Figures 1 through 12 of Program Report No. 15, Contract NAS8-11509

4. Memo to D. A. Gelke of Resdel from Dick Jaffe, "A Comparison of the Relative Merits of Bandpass Limiters and AGC Systems for use in a Phase-Locked Transponder", November 1965.

J. M. Fowler
Nov 12, 1964

Considerations of Limiting versus AGC as a means for gain control in Phase Lock Systems.

INTRODUCTION

This report outlines the problems encountered in phase lock systems relating to the development of spurious signals causing false lock-on conditions. It also shows the advantages to be gained by using a strictly limiting type of gain control rather than AGC.

PHASE LOCK SYSTEM

The following block diagram, fig 1, shows the elements of a phase lock system as used in an S-Band transponder developed by Resdel.

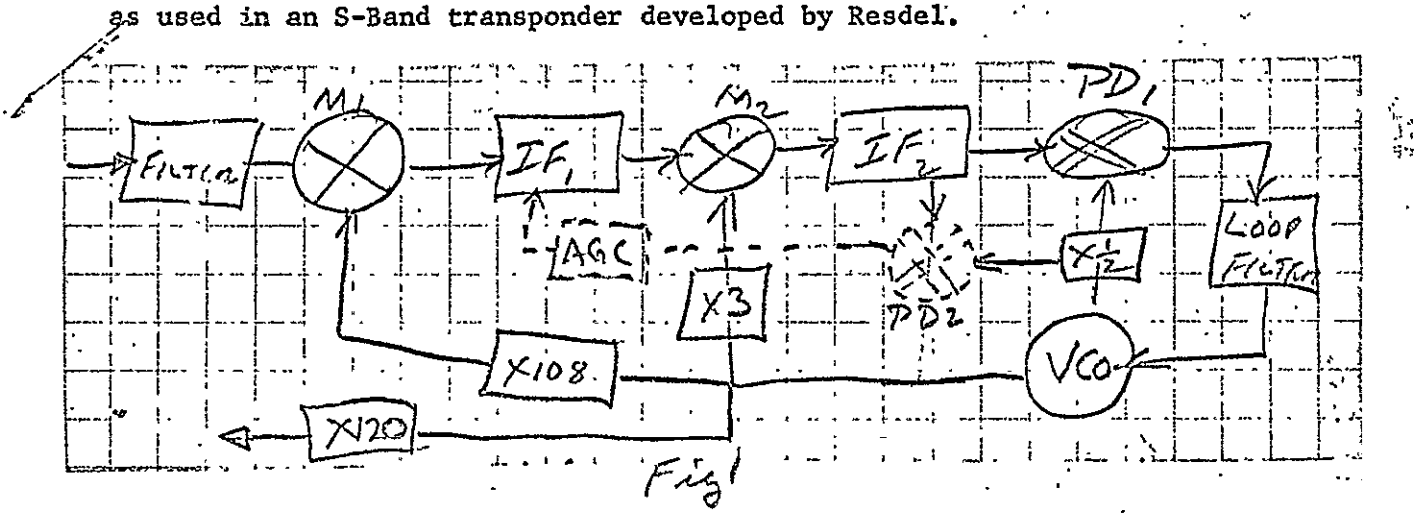


Fig 1

The dotted portion represents the synchronous AGC system commonly used. The Resdel design utilizes only limiting in the IF amplifier for gain control.

CONSIDERATIONS OF ~~PROBLEMS COMMON TO BOTH~~ AGC AND LIMITING SYSTEMS.

There are certain problems that would be present whether AGC or limiting is used:

1. BW of input filter. The narrower this can be made, the better the REJECTION to off chanel interference. The insertion loss must be kept reasonable, however, and since the loss is a function of BW (and skirt selectivity) the discrimination against close off-channel interference at S-Band is not feasible. Therefore, it can be expected that close off-channel

interference will get to the first mixer.

2. 1st Mixer non linearity. Normally, on low signal levels the 1st mixer is a linear device and does not produce spurious signals. At signal levels approaching ODBM the mixer now becomes non-linear, starts to reach the saturation point and produces strong harmonics and mixing of these harmonics takes place. It is also possible to produce extraneous spurious signals under certain conditions. If the combination of harmonics of interfering and on-frequency signals is just right, a false-lock condition will take place and the transponder will lock-on the false signal (if the false signal is approximately 10DB stronger than the on-frequency signal).

The 1st mixer used in the Resdel transponder will withstand input signals to +4DBM before non-linearity occurs, and +10DBM before severe saturation takes place.

3. 1st IF Bw. The bandwidth of the 1st IF will dictate how far off frequency interfering signals will penetrate to the 2nd mixer. Ideally, a bandpass filter at the input to the 1st IF would prevent much of the signals from getting into the IF at all. However, ~~problem of noise figure now would be present because of the probable inability to properly match the 1st mixer and 1st IF~~. It is mandatory for some applications, such as ranging with pseudo-noise, that this BW be wide also, the difficulty of proper matching, plus filter loss would degrade the figure. In the Resdel limiting system an interfering signal of sufficient magnitude within the 1st IF passband will cause stable, non-spurious limiting of the 1st IF, thus assuring no large signal ever reaching the 2nd. mixer. A synchronous AGC system, on the other hand, has no such assurance, since the only gain control is by an on-frequency signal. It is emphasized that because of the large gain in the 1st IF it is essential that no extraneous signals ever penetrate to the 2nd mixer since it then would be very susceptible to generation of spurious and harmonic combinations.

It should also be pointed out that since stable limiting is designed into the Resdel IF it is not susceptible to generation of spurious signals as a normal IF amplifier might be that had not been designed to handle large saturating type signals.

4. 2nd IF BW. The second IF Bandwidth is primarily determined by the allowable noise level to the phase detector. Obviously the narrower this bandwidth the less chance for generation of spurious signals in the 2nd IF amplifier stage. The limitation on this BW is the aforementioned noise consideration and the ability to construct the filter with minimum phase shift across the band of interest. The latter consideration precludes the use of crystal filters since they cannot be built with assured minimum phase difference across their bandwdth. The filter used in the Resdel transponder is a 4pole double tuned, slightly overcoupled, bandpass filter constructed with high Q toroids tuned to give essentially zero phase shift over a much greater frequency than that necessary to handle the expected doppler shift. The bandwidth is 60 kc at 3 db down and the noise bandwidth is approximately 120 kc. Center frequency is 9-9/16 mc.

5. Loop problems. For adequate stability the AGC loop must be several orders of magnitude narrower than the tracking loop. The AGC response time is therefore considerably longer than that of the tracking loop. This presents a problem when automatic aquisition is required, wherein full input signal is delivered to the IF's when the loop is out of lock, since no AGC is being developed. If the signal is large enough to overdrive the IF's the "reaction" time of the AGC could cause serious delay in acquisition, and the design for automatic acquisition would of necessity have to incorporate the consideration of slow-reacting AGC systems. It is questionable if acquisition much under 5 seconds could be obtained over the specified lock on range of $\pm$ 250 kc.

In addition to the problems of acquisition there are possibilities of two loop instabilities occurring, especially under very heavy signal conditions and also when signal level changes rapidly (accelleration). The Resdel limiting type system eliminates all signal AGC loops, thus providing absolute loop stability plus a fast reacting gain control thus assuring the fastest possible acquisition.

References to Resdel limiting

Theory of Block Techniques - pg 8-20

Progress Report #5 - pg 4-1

limiting

extracted from Status Report

and

$G > +15 \text{ dbm} - (-105 \text{ dbm}) \geq 120 \text{ db.}$

To insure solid limiting, the gain was set so it equalled 135 db in the absence of noise. Thus, the system has "15 db of limiting" on noise alone.

8-4.8 Phase-Stable I-F Amplifiers

It is self-evident that in order for any phaselock receiver to faithfully follow the incoming signal, the receiver should introduce no incremental phase shifts over the entire dynamic range of signal input and environmental variations. Phase shift variations in the receiver are one of the most difficult problems the designer must solve. Circuit designers and component manufacturers are continually working to reduce phase shift problems and much has been accomplished with solid-state designs in recent months.

The main causes of phase shift in the I-F amplifiers are:

1. Internal feedback in the amplifier.
2. AGC variations
3. Temperature variations
4. Frequency changes due to Doppler excursions
5. Saturation on strong signal levels

Causes of phase-shift 2, 3 and 4 can be reduced considerably by simply employing wide-band tuned circuits with a low L/C ratio. This technique is almost universally used in all phaselock equipments and has proved very effective. Internal feedback effects are overcome by the use of mismatching techniques. The necessary narrow-bandwidth is obtained though the use of passive filters.

Because the incremental phase-shift requirements are in the order of 10°, the above techniques are not satisfactory in themselves. Additional techniques must be used to meet these stringent requirements. Many types of AGC circuits have been tried in order to minimize phase shift over dynamic ranges of 80 to 100 db. The types have ranged from various combinations of "forward" and "reverse" AGC to the use of diode-type attenuators between stages. Each of these methods has had some success but has not really been completely satisfactory. One of the latest methods

developed employs two transistors in a differential amplifier form as shown in Fig. 8-3

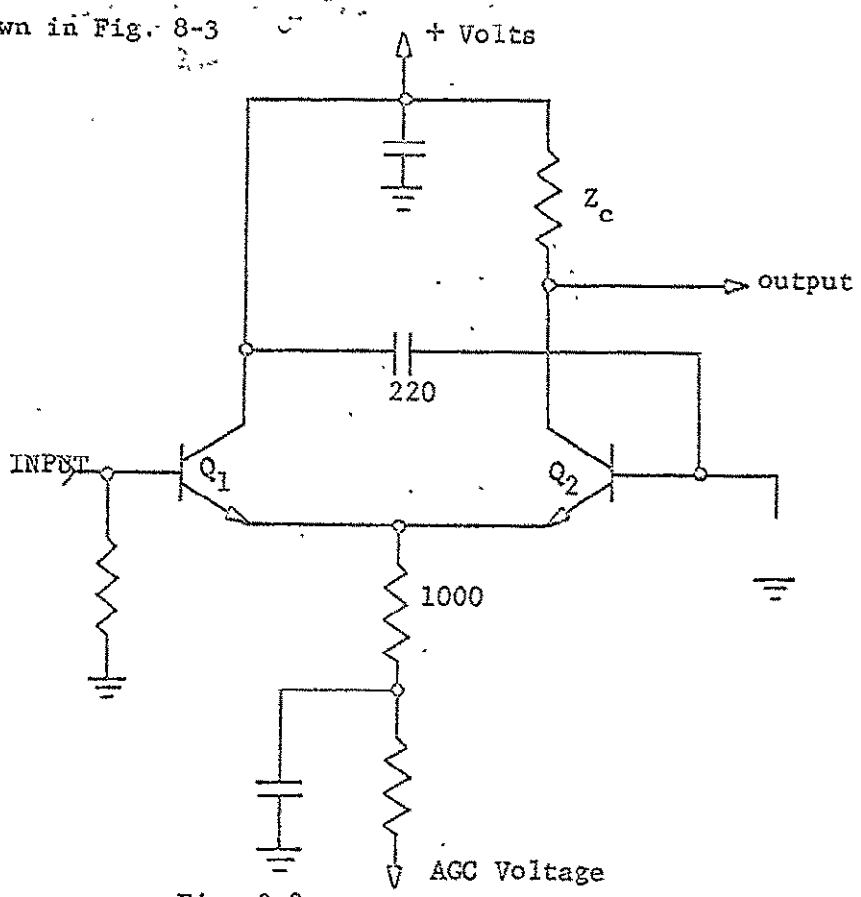


Fig. 8-3

I-F Amplifier Stage With AGC Applied

This configuration provides a relatively high input impedance, good isolation from input to output, low base to emitter capacitance, plus capacitance cancellation with current changes. The stage operates similar to any differential amplifier. Gain control is accomplished by varying the emitter current with the AGC voltage.

Tests conducted on this type of configuration have shown the phase shift to be less than 5° over a dynamic range of 30-db.

Incremental phase shift due to temperature changes are also minimized through the use of the circuitry shown. In addition, temperature-stable components (especially capacitors) must be used. Some temperature compensation devices may also be required. Incremental phase shift due to Doppler frequency excursions are reduced by using broadbanded tuned circuits with a small L/C ratio. Large capacity values are used to improve phase shift due to temperature and AGC variations.

Saturation of amplifier stages causes signal distortion with attendent phase shifts. In a system that employs AGC in the I-F amplifiers, saturation (or limiting) on noise in the I-F string is undesirable because it results in signal suppression due to the limiting action. The designer must take the necessary precautions to eliminate this particular problem (this is discussed further in paragraph 8-5.1.2).

8-4.9 AGC versus Limiting

Jaffe and Rechtin (JAF-1) have shown that the use of a limiter provides a near optimum phase-lock loop because the system self-compensates for signal level changes near threshold. This effect has been proved both in the laboratory and in the field. Thus, as far as theoretical operation is concerned, AGC is not a system necessity.

Besides the incremental phase-shift problems associated with the use of AGC, there are several other good reasons for eliminating AGC, if possible. The problems associated with interaction between the AGC loop and the phase-lock loop are not clearly understood because of second-order effects that do not lend themselves to easy analysis. Since the problem of "threshold" is not clearly understood, it would seem advisable not to complicate it further by the inclusion of the AGC loop.

A third problem, associated with the use of coherent AGC, is the generation of spurious signals within the equipment due to receiver overload prior to locking on strong signals. This problem can be solved, but it generally requires the use of two additional non-coherent AGC detectors - one before and one after the I-F bandpass filter.

All of the above problems can be eliminated if an amplifier can be designed that will limit, as the signal increases, without causing phase-shift. Transistor circuitry has recently been developed that will limit without introducing undersirable phase shift. The circuit diagram for such a single stage amplifier is shown in Fig. 8-5.

This circuit is identical to Fig. 8-4 except the emitter resistor is returned to a fixed voltage.

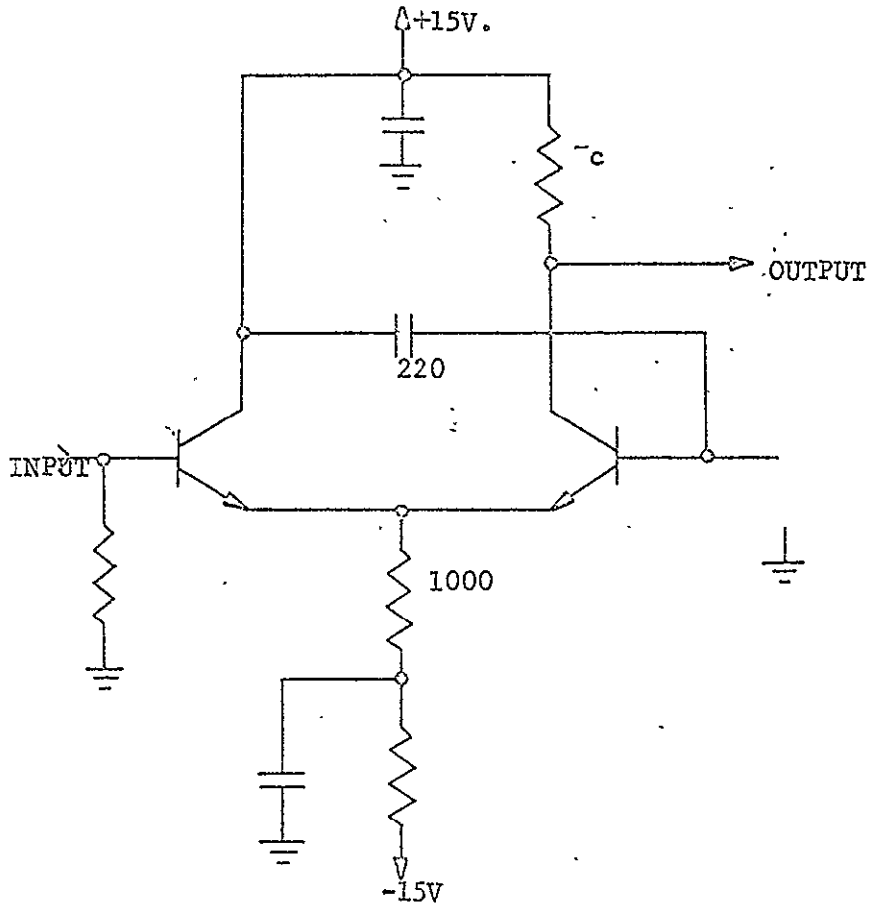


Fig. 8-5

Limiter/Amplifier Stage

A simplified explanation of the operation is as follows: For low level inputs the stage operates as a linear differential amplifier. As the signal level increases a point is reached where the output stage is not conducting any current during a portion of the input signal. Beyond this point then, no more energy can be transferred to the output circuit - the output power is limited by the maximum current available in the output stage. In effect, then, the output stage is switched on and off by the incoming signal.

The circuitry shown has been assembled in a four stage amplifier and, from low-level to full saturation of all four stages, the total measurable phase-shift is in the order of 5^{o}. This is equal to, or better, than most of the AGC circuits developed to date. The amplifier shown provides 20 db of gain, at 50 mc, and can safely handle up to 0-dbm (50 ohm) input levels without affecting the operation.

Attached from P. 15

4.0 DESIGN CONSIDERATIONS OF BANDPASS LIMITING VERSUS SYNCHRONOUS AGC AND NON-SYNCHRONOUS AGC

At the onset of this project it was decided that synchronous AGC should be used in the system design. It was realized however, that conflicting requirements made the use of synchronous AGC undesirable in some respects. First, a requirement existed for handling a -7 DBM input signal level at the system input. This signal level attenuated by the insertion loss of the input filter and conversion loss of the first mixer gave approximately a -16 DBM input level to the first IF stage.

As mentioned previously the device used in the first IF design is a MC1110 integrated device. It was chosen primarily because its output and input susceptance variations are quite small for changes in collector voltage and emitter current. One of the main problems in the design of phase locked systems is preventing fractional detuning in the IF amplifiers under overdrive conditions or during AGC loop operation. ~~Please refer to~~ Appendix D for first IF schematic. Minimizing fractional detuning has been accomplished in other designs by using diode attenuators and susceptance variation cancellation which has only been partially successful in solving the detuning problem.

Digressing briefly from the device discussion, the synchrous AGC control of the IF gain is present only when the loop is locked on. Also, it is desirable that the noise bandwidth of the AGC loop must be several orders of magnitudes narrower than the tracking loop. The AGC response time therefore is conderably longer than the tracking loops. This presents a problem in trying to acquire the signal. If for example a loss of signal occurred for a period of time sufficiently long for the loop filter to discharge upon return of signal the loop would be out of lock until the external sweep

voltage could pull the VCXO into the loop bandwidth. During this time however, no coherent AGC would be available to control the IF gain and if the signal level were sufficiently high the IF would be overdrawn. I a very narrow band transponder for deep space application the system mem ory (energy storage of the loop filter) would be considerably longer tha that of the subject transponder. In this case it might be reasonable to assume that signal loss would not occur for periods of time sufficiently long for the system memory to be lost and that if it did a signal level sufficiently large to overdrive the IF would not be present upon signal return. Such, however, is not the case, for the presently discussed sys tem. Loop bandwidth has been purposely increased since the system usage is for relatively short ranges and the acceleration ramp handling capa- bility is the determining factor as to how fast the system can reacquire signal which in turn dictates loop bandwidth.

Thus, in the case of the Resdel S-band transponder, coherent AGC alone would be inadequate in that overdrive of the IF would still occur and the response time could limit how fast a signal could be reacquired.

An alternate approach would be to use in addition to the coherent AGC, non-coherent AGC. The non-coherent AGC would control IF gain with the system out of lock while the coherent AGC would control the gain while the system was in lock. This approach was not used since the addi tional system complexity was considered unwarranted.

During the development of the first IF a very unique feature of the MC1110 transistor was noted. It was found that if the device was driven from a certain source impedance, that very little difference between its small signal and large signal response occurred. Practically no fractio

detuning occurred and the normal response flat topping along with generation of spurious outputs did not occur. It was felt intuitively that this unique behavior was due to several factors. First the device is connected in such a manner that as one stage was being driven on harder, the other was being turned off so that some cancellation of susceptance variations could occur. Also the output collector resonant circuit is driven from a common base stage which is a relatively high impedance current source. Thus, as the stage is cut off for a portion of the cycle or driven into saturation the collector circuit can continue ringing since during non-linear operation very little energy is fed back into the source.

Predicting the behavior of the device in its small signal region is easily accomplished by usage of the Linvill analysis or other circuit models. Analysis of the large signal behavior however, requires a more intimate knowledge of the device parameters than can be obtained from manufacturer data sheets or simple tests. Also, the complexity of a non-linear analysis lends credence to an empirical approach rather than a rigorous analytical approach to the IF's large signal behavior.

The excellent limiting features of the first IF are best illustrated in Figures 1 to 12. These photographs were made by putting a sweep generator on the input to the first IF stage and varying the input from 0 DBM to -110 DBM. The output varied from 0 DBM to -25 DBM. The discontinuity appearing at the top of the response on some of the pictures is caused by the marker and is not in the IF amplifier. As can be seen for a +110 DBM input signal level variation, the response is altered very little and practically no fractional detuning occurs. The limit level is 0 DBM and the limiting range is in excess of 70 DBM (output remains within .25 DB of limit level).

With this type of limiting the question arises as to the necessity of an AGC loop at all. Certainly the elemination of the AGC loop is attractive for the previously mentioned reasons and for elimination of any possible two loop oscillations between the AGC and the carrier tracking loop. The type of limiting provided in this S-Band transponder will approximate better than any previous developed method, a variable loop filter that is continually adjustable for optimum performance for each change of input signal level. This has been discussed at length by Jaffe and Rechtin*. The bandpass limiter they describe is improved with the circuit developed for this application due to excellent hard limiting characteristics without creating spurious responses or increasing bandwidth. Without increasing bandwidth.

This is not true. Spurious responses are inevitably generated with a limiter.

* Jaffe and Rechtin. "Design and performance and phase lock circuit capable of near optimum performance over a wide range of input signal and noise levels." From RIE Transactions on Information Theory IT-1, March, 1955.

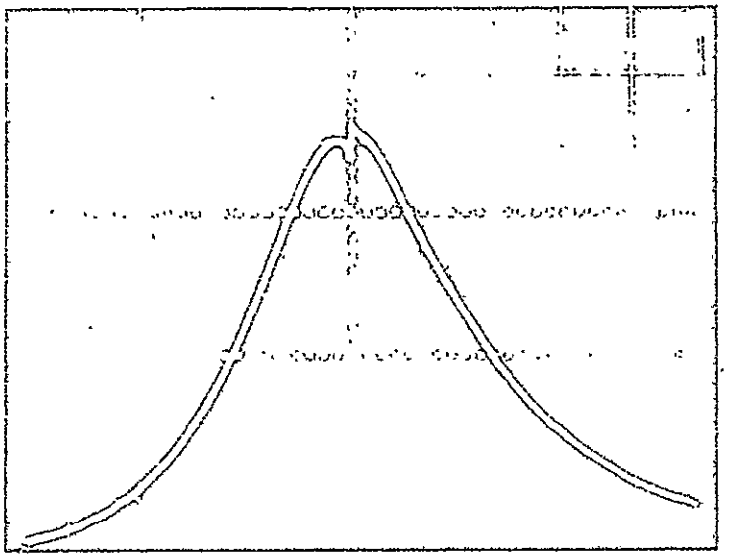


FIG. I

Input 0 dbm

Output 0 dbm

B.W. 9 mc

f_o 47.8125 mc

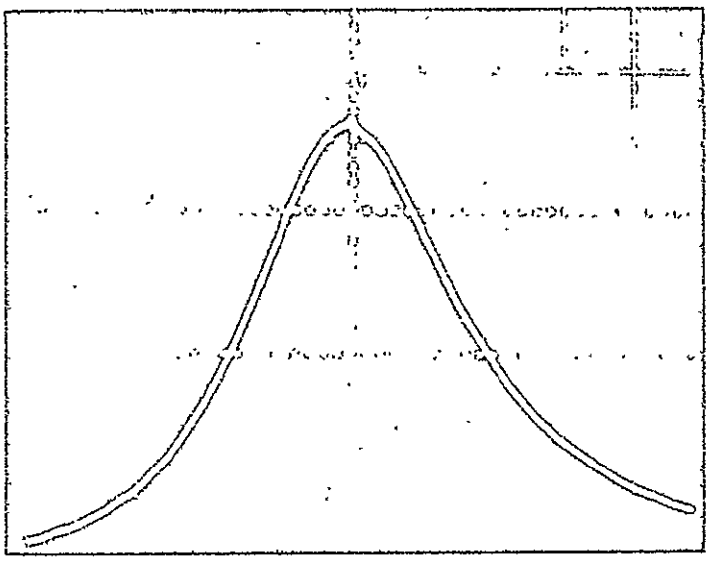


FIG. 2

Input - 10 d

Output 0 dbm

B.W. 9 mc

f_o 47.8125

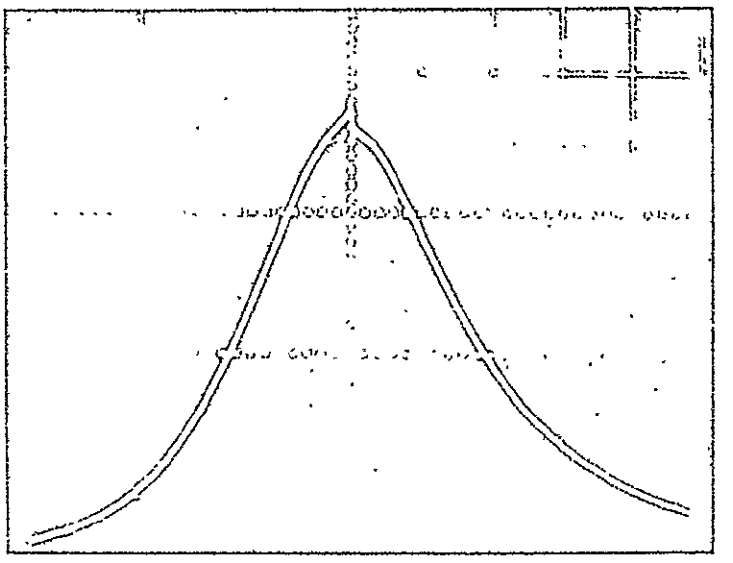


FIG. 3

Input - 20 dbm

Output 0 dbm

B.W. 9 mc

f_o 47.8125

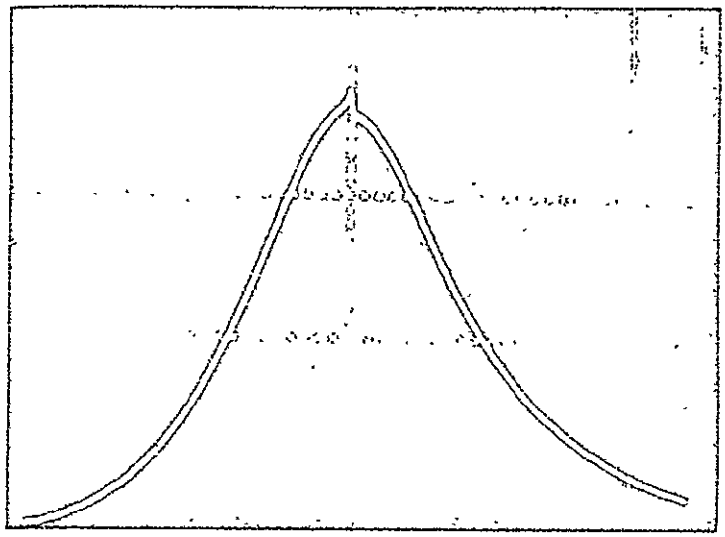


FIG. 4

Input - 30 dbm

Output 0 dbm

B.W. 9 mc

f_o 47.8125

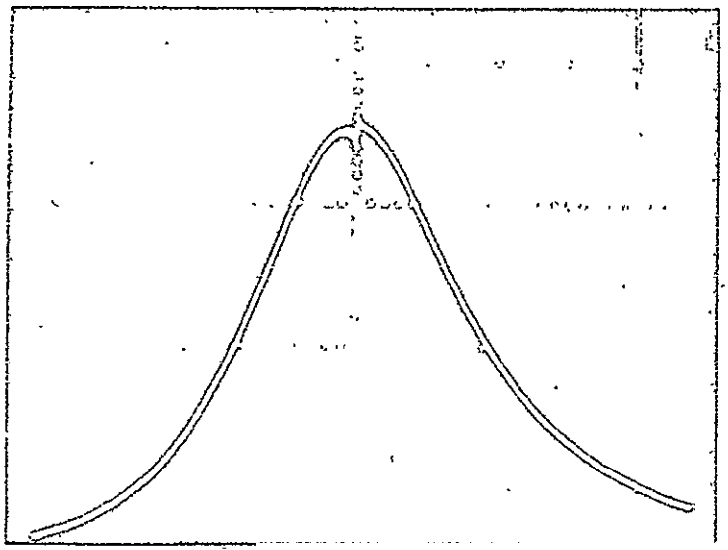


FIG. 5

Input - 40 dbm

Output 0 dbm

B.W. 9 mc

f_o 47.8125

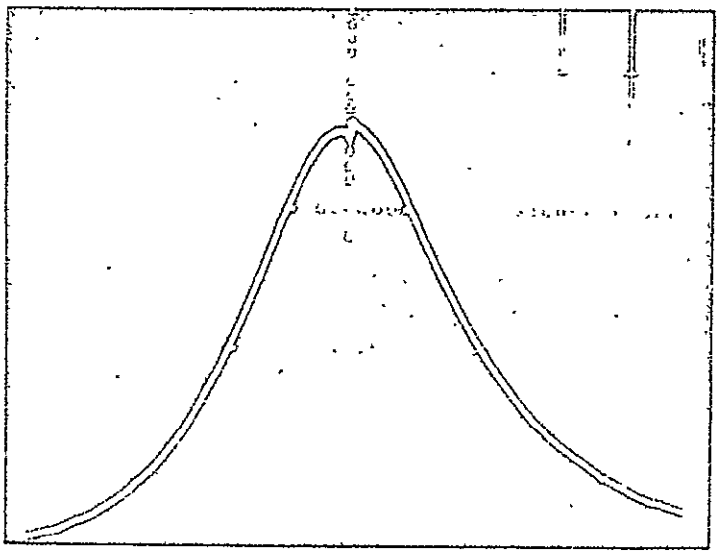


FIG. 6

Input - 50 dbm

Output 0 dbm

B.W. 9 mc

f_o 47.8125

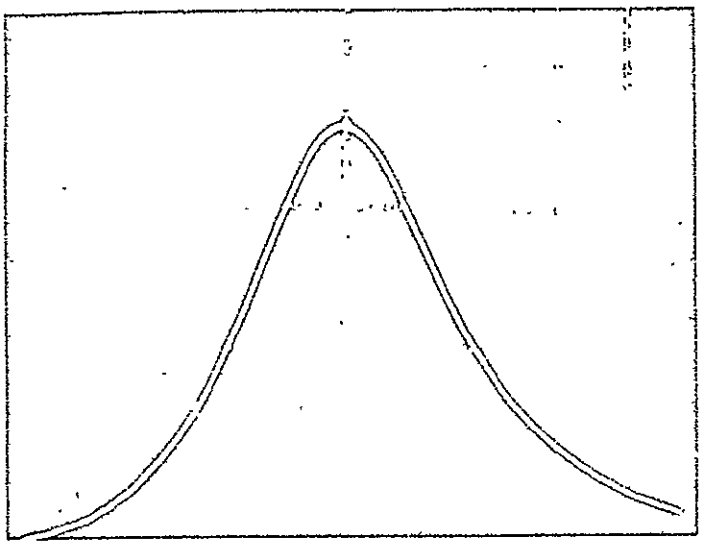


FIG. 7

Input - 60 dbm

Output 0 dbm

B.W. 8 mc

f_o 47.8125

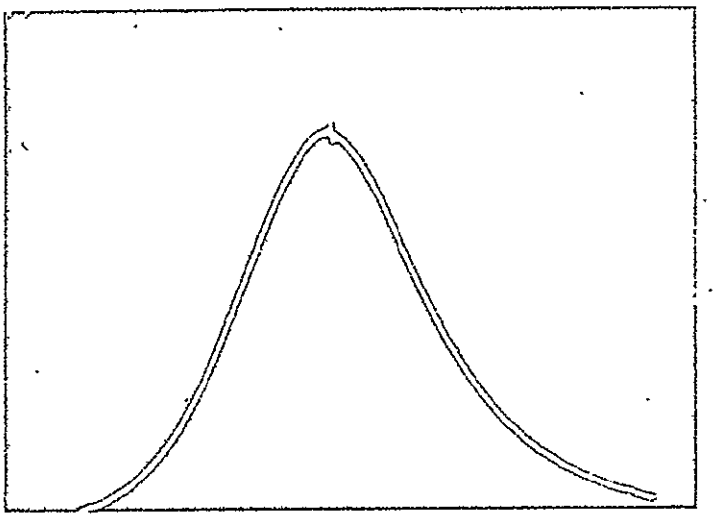


FIG. 8

Input - 70 dbm

Output 0 dbm

B.W. 8 mc

f_o 47.8125

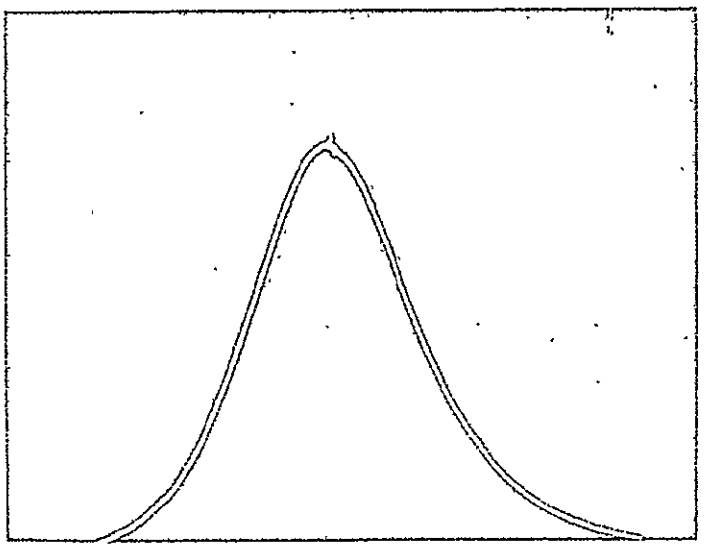


FIG. 9

Input - 80dbm

Output - 1 dbm

B.W. 7 mc

f_o 47.8125

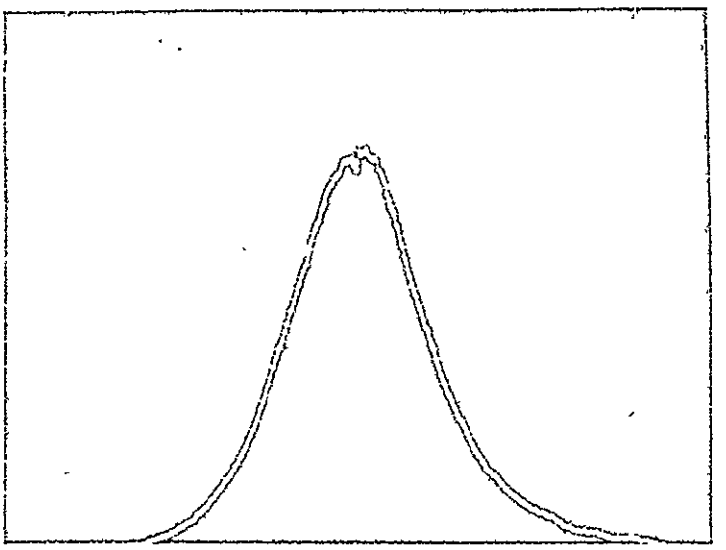


FIG. 10

Input - 90 dbm

Output - 5 dbm

B.W. 7 mc

f_o 47.8125

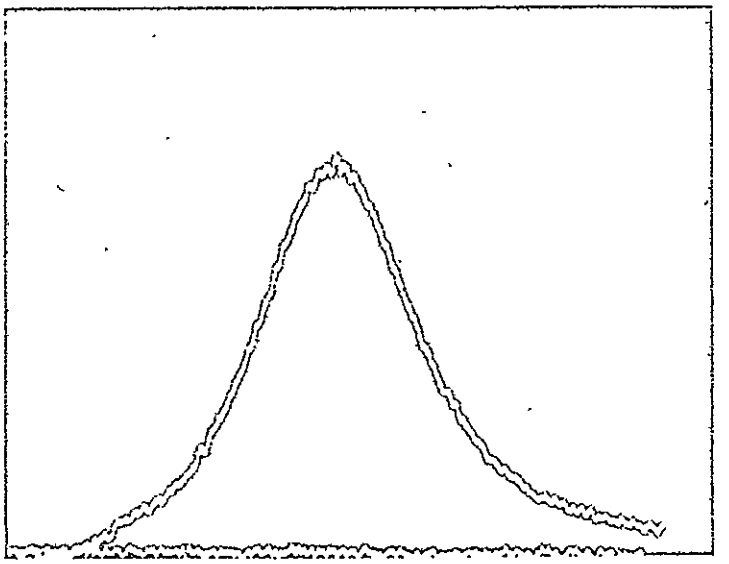


FIG. 11

Input - 100 dbm

Output - 15 dbm

B.W. 7 mc

f_o 47.8125

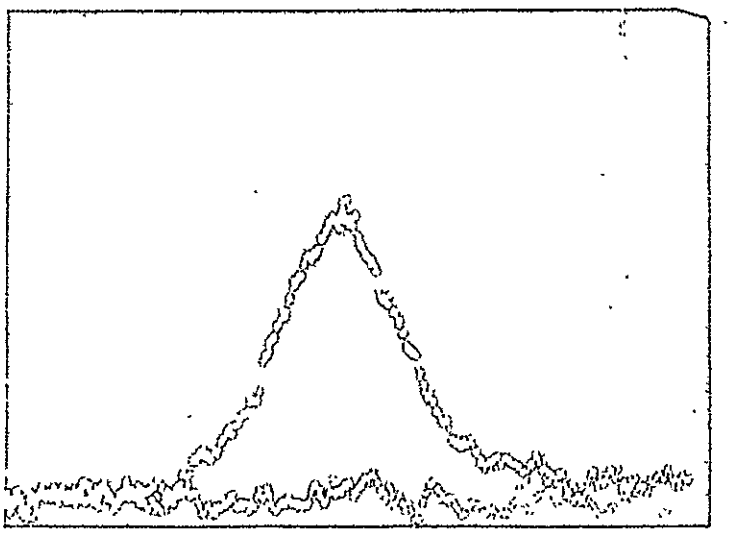


FIG. 12

Input - 110 dbm

Output - 25 dbm

B.W. 7 mc

f_o 47.8125

November, 1965

TO: D. A. Gehlke

FROM: Dick Jaffe

SUBJECT: A COMPARISON OF THE RELATIVE MERITS OF BANDPASS-LIMITERS AND AGC SYSTEMS FOR USE IN A PHASE-LOCKED TRANSPONDER

I. Introduction

The receiver gain of a phase-locked transponder must be controlled in order to accommodate a wide range of input signals and input interference. There are 4 common methods by which this gain-control can be effected:

1) Employing a bandpass-limiter, prior to the loop phase-detector.
2) Using a coherent AGC system to control amplifier gain.
3) Using a non-coherent AGC system to control amplifier.
4) Using a non-coherent AGC system to control amplifier gain until the loop has locked on, and then controlling the amplifier gain by means of a coherent AGC system.

The following definitions are applicable:

1) A bandpass limiter consists of a hard-limiting limiter which is preceded and followed by narrowband filters. These filters have sufficient bandwidth to pass the frequency components of the input signal, but do not pass any frequencies in the region of d-c, or twice the center-frequency of the input. The definition of a bandpass limiter is adequately satisfied if the filters have effective Q's of 10 or greater.
2) A coherent AGC system (in a phase-locked receiver) generates AGC voltage by phase-detecting the input signal to the phase-locked loop with a 90^{o} phase-shifted output from the loop VCO (voltage-controlled-oscillator).

3) A non-coherent AGC system generates AGC voltage by envelope detecting the input signal to the phase-locked loop. Envelope detection is usually accomplished with a diode detector.

The purpose of this memo is to evaluate the relative merits of these 4 methods for controlling gain; the 4 methods will be evaluated in connection with their suitability for use in the Resdel S-band transponder.

II. Block Diagram of the Transponder:

A block diagram of the receiver portion of the Resdel S-band transponder is shown below in Figure 1.

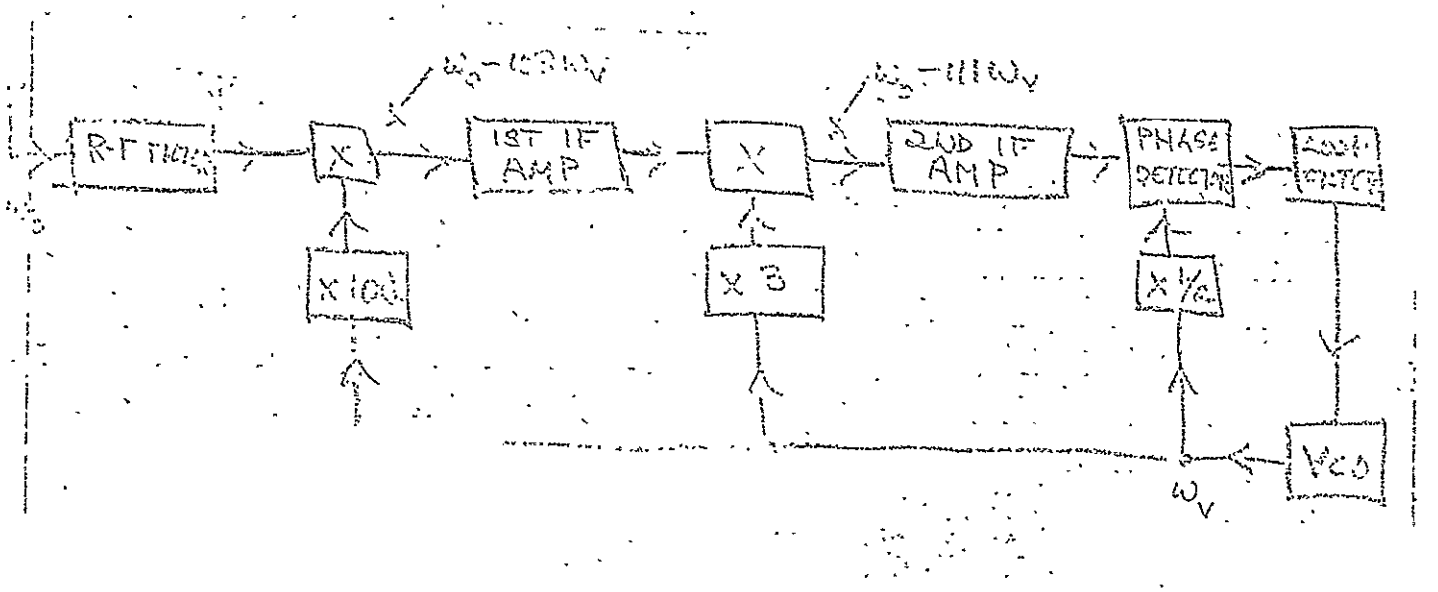


Figure 1. BLOCK DIAGRAM OF RECEIVER PORTION OF RESDEL S-BAND TRANSPONDER

The input S-Band signal (at frequency W_o) is passed through a band-pass R-F filter, and then heterodyned with an X108 version of the VCO output (at frequency W_v). The mixer output is passed through a 1st. i-f amplifier (gain = 75 db, center frequency $\cong$ 47 Mc) to the second mixer. The 1st i-F is heterodyned to a 2nd i-F of approximately 9.5 Mc.

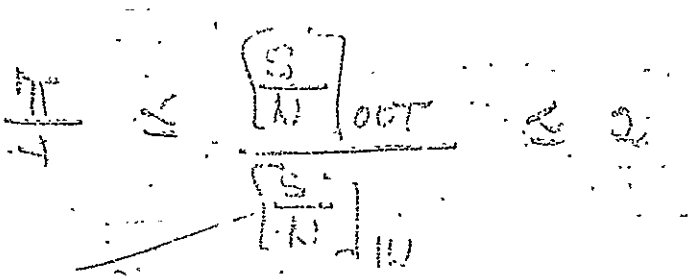
in the second mixer; the heterodyning signal is an X3 version of the VCO output. The output of the second mixer is passed through a 2nd i-F amplifier (bandwidth $\cong$ 120 Kc) and phase-detected with a X1/2 version of the VCO output. The VCO control-voltage consists of the phase-detector output as filtered by the loop filter.

The receiver also contains an automatic-acquisition circuit (not shown in Figure I), which sweeps the VCO frequency until the phase-lock loop locks on.

The present configuration of the transponder obtains gain control by employing a hard limiter (which limits on thermal noise alone) in the 2nd i-F bandwidth filter.

III. Noise-Interference Considerations

As shown in Reference 1, the relationship between input and output signal/noise ratios for a bandpass limiter fed by a sinusoidal signal and Gaussian noise, is



(1)

where S = signal power

N = noise power

In equation (1), the lower limit on the ratio is for $S/N_{in} \ll 1$, while the upper limit is for $\left[S/N\right]_{in} \gg 1$.

Furthermore, as shown on p.288 of reference 2, the output power from a bandpass limiter is constant* . Consequently,

$$\overline{[S+N]}_{OUT} = K^2 \quad ; \quad K = \text{constant} \tag{2}$$

Combining equations (1) and (2) shows that, for small input S/N (the case usually of interest), the output signal power will be

$$S_{OUT} \cong \frac{1}{1 + \frac{4}{\pi}\left(\frac{N}{S}\right)} \tag{3}$$

This variation of signal power will cause a change (proportional to S_{out}) in the gain of a phase-locked loop which follows the limiter.

This effect is not generally detrimental, and may sometimes be helpful (c.f. Reference 3).

In conclusion, when the input to a bandpass limiter is a sinusiodal signal and Gaussian noise, the limiter introduces an essentially insignificant (1db maximum) degradation of signal/noise ratio; and causes a generally non-detrimental change in the gain of a phase-locked-loop subsequent to the limiter.

* A hard-limiter, <u>without</u> any filtering following the limiter will obviously have a constant, total-power output. However, it must be <u>proved</u> that a limiter followed by a narrowband filter, will deliver constant total power. The proof of this only holds if the limiter is also preceded by a narrowband filter, similar to the output filter.

IV. Analysis of the Response of a Bandpass Limiter to an Input of 2 Sine Waves:

As shown in the preceding section, a bandpass limiter provides a satisfactory method of gain-control when the only interference to a sinusoidal signal is that generated by Gaussian noise.

However, in the application of the Resdel transponder, another potential source of interference is an additional sine wave. Consequently, in this section we will consider the response of a bandpass limiter to an input of two sine waves.

Consider the following input to a bandpass limite

$$V_{in}(t) = \cos at + \beta \cos bt \qquad (7)$$

where both a and b lie within the bandwidth of the filter preceding the limiter.

It may be shown that the output of the bandpass limiter contains the following frequencies

$$W_n = (2n+1)A$$

$$A = b - a$$

and where n can have any positive or negative value such that W_n lies within the bandwidth of the filter following the limiter.

The amplitudes of the various frequency terms, for general values of β, are given in terms of hypergeometric functions and must be calculated by series expansions. However, some special cases of the results can be calculated with relative ease, and two of these cases will now be presented to illustrate the general results.

Case I: Equal-Amplitude Inputs

In this case, = 1 in equation (4), yielding

$$V_{IP}(t) = \cos at + \cos bt \qquad (5)$$

The amplitude spectrum of the input consequently looks like

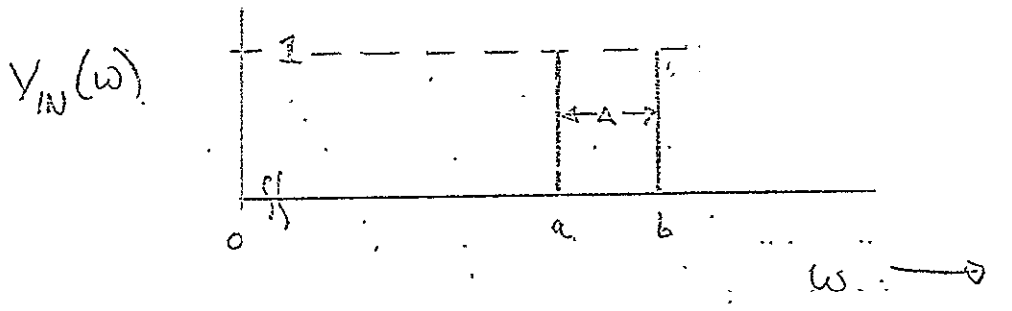


Figure 2: AMPLITUDE SPECTRUM OF LIMITER INPUT FOR EQUAL-AMPLITUDE SINUSOIDAL INPUTS

where we have defined $\Delta = b - a$

and where the areas of the delta-functions in frequency are represented by their amplitude (this convention will be followed in the remainder of this report).

In appendix I, it is shown that the spectrum of the output of a bandpass limiter, fed by the input shown in Figure 2, may be represented (normalized to a unity maximum) as in Figure 3.

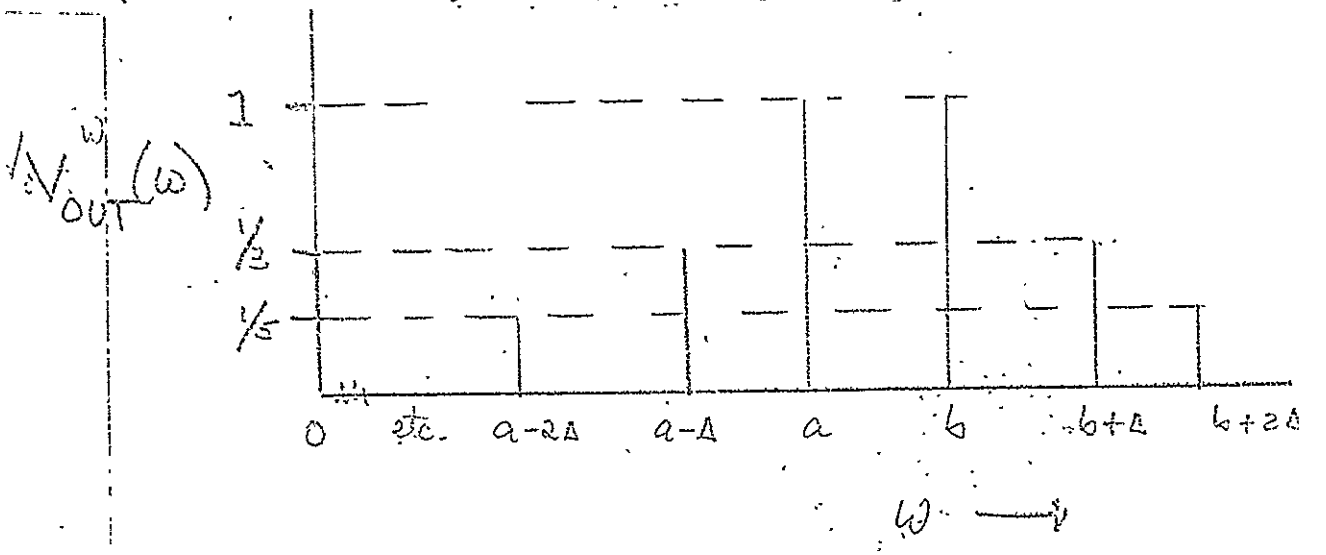


Figure 3: AMPLITUDE SPECTRUM OF LIMITER OUTPUT FOR EQUAL-AMPLITU SINUSOIDAL INPUTS

As seen in Figure 3 above, and described in equation (A12) of appendix A, the output frequencies at $W_n = a - n\Delta$ and $\Omega_n = b + n\Delta$ have amplitudes equal to $\frac{1}{2n+1}$ times the amplitude of the terms at $W = a$, and $W = b$.

Case II: Inputs Having a Large Amplitude Ratio

In this case

$$V_{IN}(t) = \cos at + \beta \cos bt \qquad (6)$$

where

$$\beta^2 << 1 \qquad (7)$$

Equation (7) is satisfied by $\beta^2 \leq 0.1$ (i.e., the sure wave at radian frequency, a, is 10 db or more greater than the sine wave at radian frequency, 6). The amplitude spectrum of the input consequently looks like

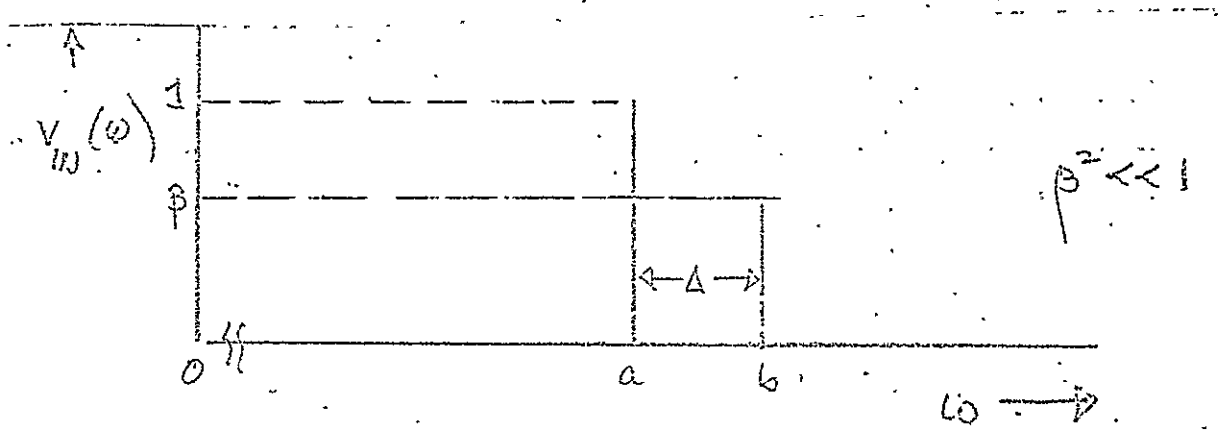


Figure 4: AMPLITUDE SPECTRUM OF LIMITER INPUT FOR SINUSOIDAL INPUTS HAVING A LARGE AMPLITUDE - RATIO

where we have again defined Δ.

The corresponding amplitude spectrum of the limiter output is derived in appendix II, and is plotted (normalized to a unity maximum) in Figure 5,:

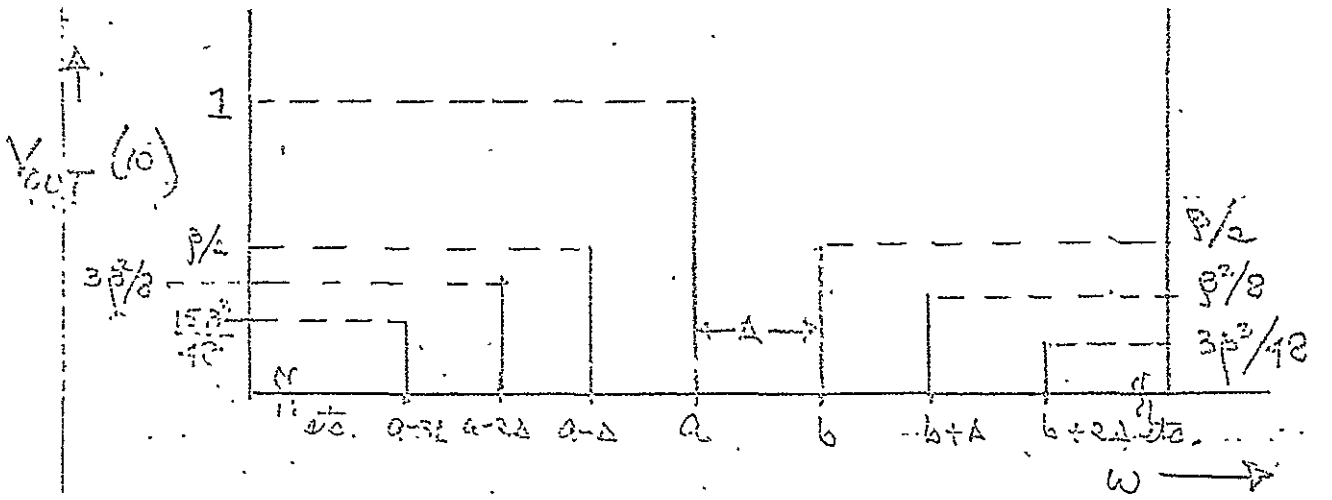


Figure 5: AMPLITUDE SPECTRUM OF LIMITER OUTPUT FOR SINUSOIDAL INPUTS HAVING A LARGE AMPLITUDE-RATIO

It is shown in Appendix II, that in general, there are output frequencies at $W = a$, and $W_n = a - n\Delta$ $n = 1, 2,$ and $W_m = a + m\Delta$ $m = 1,2$ with the amplitudes of these terms respectively given by (cF. equations B10 and B11 in appendix II)

$$\text{Amplitude at } \omega_n = \alpha_n \beta^n \qquad (9)$$

$$\text{Amplitude at } \omega_m = \left[\frac{1}{2m+1}\right]\left[\alpha_m \beta^{2m}\right] \qquad (10)$$

where (cF. equation B8 in appendix II)

$$\alpha_K = \frac{1 \times 3 \times 5 \times 7 \times \cdots (2K-1)}{2 \times 4 \times 6 \times 8 \times \cdots (2K)} \qquad (10)$$

Note from Figure 5 and equations (8) and (9), that the Kth. sideband about the strong input (i.e., the input signal at $W = a$) falls off with β^k.

Also note that, while the output spectrum is roughly symmetric about $W = a$, the sideband at $W = a + K\Delta$, is generally weaker than the corresponding sideband at $W = a - K\Delta$; this indicates that the centroid of the output spectrum has a slight bias away from the frequency of the weaker input-signal.

V. DISCUSSION OF THE EFFECTS OF SINUSOIDAL INTERFERENCE ON THE RESDEL TRANSPONDER= IF A BANDPASS LIMITER IS EMPLOYED:

In the previous section, we have seen that, if the input to a bandpass limiter consists of 2 sine waves, at radian frequencies, respectively of $W = a$ and $W = b$, then the limiter output will contain frequencies at $W_n = a \pm n\Delta$ where $n = 0, 1, 2, \quad \Delta = b - a$, subject only to the restriction that the output will contain no W_n terms lying outside of the bandwidth of the limiter-output filter.

The magnitude of these terms are, in general, a complicated function of the order of the sideband and the ratio of the amplitudes of the input sine-waves. For specialized values of this input amplitude-ratio, results have been derived and presented in the previous section.

The significance of this, in a transponder using a bandpass limiter, is not serious, provided that the transponder phase-locked loop has locked onto the desired signal. Once lock-on has been achieved, there is little probability that a radian-frequency interfering sine-wave will be so close in frequency to the desired signal, that the frequency-difference between the ? input sine-waves will be within the very small bandwidth of the phase-locked loop. Obviously, if the original interfering signal lies outside the bandwidth of the phase-locked loop, the sidebands generated by the limiter will fall even farther outside of the bandwidth of the phase-locked loop, and will cause no problem.

However, a potential problem does exist in a transponder, such as the Resdel S-band unit, which contains an automatic acquisition circuit. The problem is that the limiter-induced sidebands may increase the probability of false lock-on from the probability that existed without the limiter.

However, in appendix C it is shown that the increase in false lock on probability is not very great. The results are summarized in the next section.

VI. SUMMARY OF THE INCREASE IN FALSE LOCK-ON PROBABILITY CAUSED BY THE LIMITER.

In section IV of appendix C it is shown that, assuming

1) The signal-frequency, the interference-frequency, and the receiver-center-frequency-at-the-start-of-the-sweep, are equally likely to be anywhere within the acquisition bandwidth, W.

2) There is sufficient signal/noise ratio on the limiter-induced sidebands, to allow loop acquisition to these sidebands (the criteria for this requirement will be given subsequently)

then the ratio of probabilities of false lock-ons, with and without the limiter is

$$\frac{[P_F]_{\text{WITH LIM}}}{[P_F]_{\text{NO LIM}}} < \left\{1 + \frac{B}{2W}\left[1 + \frac{B}{8W}\right]\right\} \qquad (11)$$

where B = 2nd IF bandwidth

W = range of sweep acquisition circuit

This increase of false lock-on probability will only occur if there is sufficient signal/noise ratio. In section III of appendix C it is shown that the requirements on signal/noise ratio necessary for (11) to be valid are:

either:

$$\left[\frac{S}{N}\right]_{in} \geq 1 \qquad (12)$$

$$\left[\frac{J}{S}\right]_{RF} \geq 1$$

or

$$\left[\frac{S}{N}\right]_{in} \geq \frac{6.4}{\left[\frac{J}{S}\right]_{RF}} \qquad (13)$$

$$\left[\frac{J}{S}\right]_{RF} \leq 0.1$$

where

$\left[\frac{S}{N}\right]_{in}$ = signal/noise power ratio in 2nd IF passband before limiter

$\left[\frac{J}{S}\right]_{RF}$ = $\frac{\text{power of interfering sinusoid}}{\text{power of desired sinusoid}}$ AT RF

when

$$0.1 \leq \left[\frac{J}{S}\right]_{RF} \leq 1.0 \qquad (14)$$

then the required S/N_{in} is somewhere between the values given in (12) and (13), but the exact value of the required S/N_{in} is exceedingly difficult to compensate.

In conclusion, since B is always less than W, equation (11) shows that the increase of false lock-ons caused by the limiter is 50%. If the original probability of false lock-on was 10-3, the increase of this probability to 1.5 X 10-3 should be a matter of no great concern. Furthermore, when it is realized that the interference-power considerations of equations (12) and (13) further restrict the increase of limiter induced false lock-ons, by imposing constraints on the power for effective interference it appears that use of a limiter introduces an essentially insignificant degradation of system performance.

APPENDIX I

RESPONSE OF A BANDPASS LIMITER TO AN INPUT OF TWO EQUAL-AMPLITUDE SINE WAVES

Get the input to the limiter

$$V_{IN}(t) = \cos at + \cos bt \tag{A1}$$

Expanding (1) yields

$$V_{IN}(t) = 2\left[\cos\left(\frac{a+b}{2}\right)t\right]\left[\cos\left(\frac{b-a}{2}\right)t\right]$$

$$= 2\left[\cos\left(a+\frac{\Delta}{2}\right)t\right]\left[\cos\left(\frac{\Delta}{2}\right)t\right] \tag{A2}$$

Where we have defined

$$\Delta = b-a \tag{A3}$$

For an "ideal" limiter (i.e., a limiter whose output is either $\pm$ volt), the output voltage is determined by the polarity of the input voltage. Consequently, the unfiltered output of the limiter is

$$V_{OUT}(t) = \left[V_{IN}(t)\right] \text{ SQ.WV.} \tag{A4}$$

where the notation "SQ.WV." implies that the function is made into a unit-amplitude square wave having the same zero crossings as the original function.

Using (A2) in (A4) yields

$$V_{OUT}(t) = \left\{\left[\cos\left(a+\frac{\Delta}{2}\right)t\right]\left[\cos\left(\frac{\Delta}{2}\right)t\right]\right\}_{SQ.WV.} \tag{A5}$$

Now note that the limited version of a product, is equal to the product of each of the limited versions. Consequently, (A5) can be written as:

$$V_{OUT}(t) = \left[\cos\left(a+\frac{\Delta}{2}\right)t\right]_{SQ.WV} \times \left[\cos\left(\frac{\Delta}{2}\right)t\right]_{SQ.WV} \qquad \text{(A6)}$$

It is now possible to express (A6) as the product of two Fourier-series expansions. In general, if

$$X(t) = \left[\cos\alpha t\right]_{SQ.WV} \qquad \text{(A7)}$$

then, the Fourier expansion of X(t) is

$$X(t) = \frac{4}{\pi} \sum_{p=0}^{\infty} \frac{(-1)^p}{(2p+1)} \cos\left[(2p+1)\alpha t\right] \qquad \text{(A8)}$$

Consequently, using (A8) in (A6) we obtain:

$$V_{OUT}(t) = \frac{16}{\pi^2}\left[\sum_{p=0}^{\infty} \frac{(-1)^p}{(2p+1)} \cos\left[(2p+1)\left(a+\frac{\Delta}{2}\right)t\right]\right] \times \left[\sum_{q=0}^{\infty} \frac{(-1)^q}{(2q+1)} \cos\left[(2q+1)\frac{\Delta t}{2}\right]\right] \qquad \text{(A9)}$$

For the bandpass limiter we are only interested in those terms centered around frequency, a (as contrasted with those terms centered around 2a, 3a, etc.). Therefore, the bandpass limiter output is obtained by letting p = o in (A9) above, yielding

$$\left[V_{OUT}(t)\right]_{BANDPASS} = \frac{16}{\pi^2}\left[\cos\left(a+\frac{\Delta}{2}\right)t\right] \times \sum_{q=0}^{\infty} \frac{(-1)^q}{(2q+1)} \cos\left[(2q+1)\frac{\Delta t}{2}\right] \qquad \text{(A10)}$$

low note that,

$$\left\{\cos\left(a+\frac{\Delta}{2}\right)t\right\}\left[\cos(2q+1)\frac{\Delta t}{2}\right]$$

$$= \frac{1}{2}\left\{\cos\left[a+(q+1)\Delta\right]t + \cos\left[a-q\Delta\right]t\right\}$$

$$= \frac{1}{2}\left\{\cos\left[b+q\Delta\right]t + \cos\left[a-q\Delta\right]t\right\} \qquad (A11)$$

here the last equality has made use of the fact that $b = a + \Delta$.

Substituting (A11) into (A10) yields the final expression for the output f a bandpass limiter, having an input of two equal-amplitude sine waves:

$$\left[V_{OUT}(t)\right]_{BANDPASS}$$

$$= \frac{2}{\pi}\sum_{q=0}^{\infty}\frac{(-1)^q}{(2q+1)}\left\{\cos\left[b+q\Delta\right]t + \cos\left[a-q\Delta\right]t\right\} \qquad (A12)$$

APPENDIX II

RESPONSE OF A BANDPASS LIMITER TO AN INPUT OF TWO SINE WAVES HAVING A LARGE AMPLITUDE RATIO

Let the input to the limiter be

$$V_{IN}(t) = \cos at + \beta \cos bt \qquad \text{(B1)}$$

where

$$\beta^2 << 1 \qquad \text{(B2)}$$

Equation (B2) will be satisfied if $\beta^2 \leq 0.1$ (i.e., the two sine waves have a power ratio of 10 db or more). All subsequent approximations will involve ignoring terms of magnitude β^2 relative to terms of unit magnitude.

Davenport & Root (reference 2, p-288) have shown that the normalized output of a bandpass limiter is obtained by dividing the input by the instantaneous amplitude of the input. Consequently, the normalized output of the bandpass limiter is

$$\left[V_{OUT}(t)\right]_{BANDPASS} = \frac{\cos at + \beta \cos bt}{\left|\cos at + \beta \cos bt\right|} \qquad \text{(B3)}$$

The denominator of (B3) can be expressed as

$$\left|\cos at + \beta \cos bt\right| = \left|e^{jat}\left[1 + \beta e^{j\Delta t}\right]\right|$$

$$= \sqrt{1 + 2\beta \cos \Delta t + \beta^2} \qquad \text{(B4)}$$

where we have defined $\Delta = b - a$.

Substituting (B4) into (B3), and ignoring terms in β^2 relative to 1, yields

$$\left[V_{OUT}(t)\right]_{BANDPASS} = X\left[\cos \omega t + \beta \cos \omega t\right] \qquad (B5)$$

where

$$X = \frac{1}{\sqrt{1+2\beta \cos \Delta t}} \qquad (B6)$$

expanding X in a power series yields

$$X = 1 - \alpha_1 (2\beta)\cos \Delta t + \alpha_2 (2\beta)^2 \cos^2 \Delta t + \alpha_3 (2\beta)^3 \cos^3 \Delta t + \cdots$$

$$\cong 1 - 2\beta\alpha_1 \cos \Delta t + 2\beta^2 \alpha_2 \cos 2\Delta t - 2\beta^3 \alpha_3 \cos 3\Delta t + \cdots \qquad (B7)$$

where the α_n are the coefficients of the ex ? and are given by (CF. p.3 of reference 4)

$$\alpha_n = \frac{1 \times 3 \times 5 \times 7 \times \cdots (2n-1)}{2 \times 4 \times 6 \times 8 \times \cdots (2n)!} \qquad (B8)$$

and where the approximation in the second equality of (B7) has ignored terms in β^2 relative to 1.

Substituting (B7) into (B5) yields, (after expansion of the products of cosine terms, and deletion of terms in β^2 relative to 1) =

$$\left[V_{OUT}(t)\right]_{BANDPASS} = \cos at + [\alpha_1\beta]\cos(a-\Delta)t + [(1-\alpha_1)\beta]\cos(a+\Delta)t + [\alpha_2\beta^2]\cos(a-2\Delta)t + [(\alpha_1-\alpha_2)\beta^2]\cos(a+2\Delta)t - [\alpha_3\beta^3]\cos(a-3\Delta)t + [(\alpha_2-\alpha_3)\beta^3]\cos(a+3\Delta)t + \ldots \quad (B9)$$

The above results can be generalized to state:

1. Amplitude of sideband at frequency = a $-\Delta n$, is

$$\alpha_n \beta^n \quad (B10)$$

2. Amplitude of sideband at frequency = a $+\Delta m$, is

$$\left[\alpha_{m-1} - \alpha_m\right]\beta^m = \left[\frac{1}{\beta^{m-1}}\right]\left[\alpha_{m-1}\beta^{m-1}\right] \quad (B11)$$

where the α_k are defined by (B8), and where the last equality of (B11) has made use of the relationship expressed by (B8).

Evaluation of the first few terms is accomplished by using (B8) to calculate=

$$\alpha_1 = 1/2$$

$$\alpha_2 = 3/8$$

$$\alpha_3 = 15/48 \qquad \text{(B12)}$$

Substituting (B12) into (B9) yields the output of the bandpass limiter:

$$\left[V_{OUT}(t)\right]_{\text{BANDPASS}} = \cos at - \left[(1/2)B\right]\cos(a-\Delta)t + \left[(1/2)B\right]\cos(a+\Delta)t + \left[(3/8)B^2\right]\cos(a-2\Delta)t - \left[(1/8)B^2\right]\cos(a+2\Delta)t - \left[(15/48)B^3\right]\cos(a-3\Delta)t + \left[(3/48)B^3\right]\cos(a+3\Delta)t + \cdots \qquad \text{(B13)}$$

APPENDIX III

PROBABILITY OF FALSE LOCK-ON WITH AND WITHOUT A BANDPASS LIMITER

As described in Section II of the text, the Resdel transponder has an automatic-acquisition circuit that sweeps the VCO frequency ($=W_v$) until a sinusoidal input signal is heterodyned to a 2nd i-F frequency of $W_v/2$, at which time the phase-locked loop locks on to the signal.

The purpose of this appendix is to consider the probability of locking on to an undesired sinusoid, when the input to the transponder consists of an interfering sinusoid as well as the desired signal.

We will consider a number of different possible cases for different relationships of:

1) The $\wedge$-F frequency of the desired signal = W_s
2) The $\wedge$-F frequency of the interfering signal = W_I
3) The $\wedge$-F frequency to which the transponder is tuned, prior to the start of the acquisition cycle:; = W_o

We will then assume probability distributions for these functions, and determine the increase in probability of false lock-on resulting from the use of a bandpass limiter (as contrasted with a non-limiting system).

Besides the definitions of frequency listed above, the following additional definitions will be employed:

$E = (W_s - W_o)$

$\Delta = (W_s - W_I)$

W = frequency range of acquisition search

B = bandwidth of 2nd IF (where limiter may be present)

I. Case I: Transponder Center Frequency Closer to Interference that to Signal

This situation may be pictured as

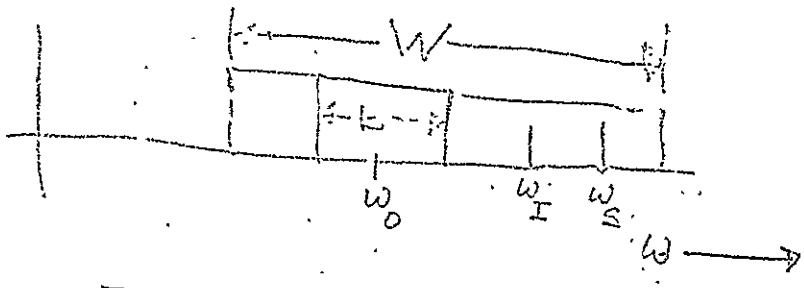


FIGURE C1

where this (and all subsequent charts) show the relative configurations of the sweep range (=W), the 2nd i-F bandpass (width = B, centered at W_o), and the interference and signal frequencies (W_I and W_S).

Although there are other possible picutres for this case (e.g. with B encompassing W_I, even though $W_o < W_I$), there is a fundamental result that pertains in this case, in the absence of a limiter:

The transponder will always acquire the interfering signal, rat... than the desired signal.

This result is obvious from inspection of Figure C1. As the receiver center-frequency (=W_o) sweeps (in an assumed continuous fashion) the first signal it will enocunter will be the interference at W_I, and the transponder phase-lock-loop will lock on.

Now consider what will happen with a limiter. As discussed in Section IV of the test, there will be sidebands generated about W_I a intervals of every Δ cycles ($\Delta = W_S - W_I$). Consequently, the transponder may lock on to one of these sidebands, depending on the relative position of W_o and W_I. However, with a bandpass limiter =

The transponder will lock on to either the interfering signal, or a sideband of the interfering signal, rather than the desired signal.

Consequently, for this case, the probability of false lock-on is unity regardless of whether a limiter is used

II. Case II Transponder Center Frequency Closer to Signal than to Interference

Subcase A: Interference Initially Outside 2nd IF Passband

The situation may be pictured as

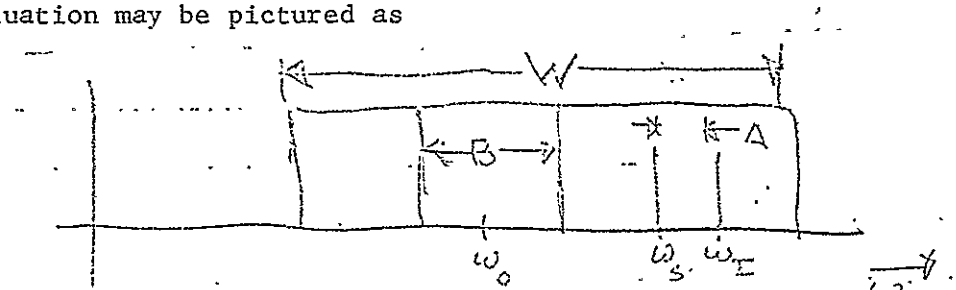


FIGURE C2

If no limiter is employed, the transponder will lock to the desired signal. This is obvious since a continuous sweep will first encounter W_s, rather than W_I.

If a limiter is employed, there will be sidebands about the signal at every rad/sec. In particular, there will be a sideband at $(W_s-\Delta)$.

At this point in the discussion, we will assume that the sideband at $(W_s-\Delta)$ has sufficient amplitude to permit transponder lock-on. Subsequently, we will investigate the criteria necessary to validate this assumption.

We will also ignore the possibility of the transponder locking on to a different sideband (e.g., one at $W_s-2\Delta$). The chance for this happening is smaller than the chance to capture the sideband at $(W_s-\Delta)$: a sideband at $W_s-2\Delta$ will have less amplitude, and its capture imposes more severe restrictions on the relationship between W, W_o, B and Δ, as can be seen by extending the subsequent argument. The important point is that, even if the transponder does lock on to a different sideband (e.g., at $W_s-2\Delta$), it will still be a false lock-on.

Put succintly: 1) the transponder will not lock-on to a sideband different from $(W_s-\Delta)$ unless it is also capable of locking on to the

sideband at $(W_s-\Delta)$ is the probability of false lock-on.

Referring again to Figure C2, it is seen that no limiter-generated sideband will be available until the VCO has swept Figure C2 into the configuration of Figure C3, below:

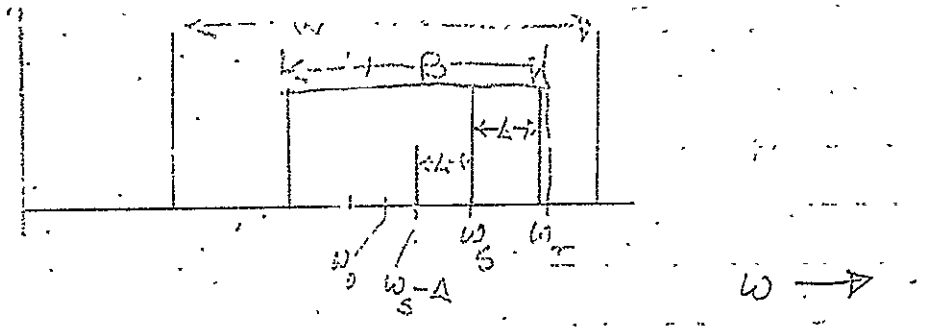


FIGURE C3

Specifically, both W_s and W_I must be encompassed by B to generate sidebands in the limiting process. Once this happens, Figure C3 shows that, if

$$2\Delta \leq \frac{B}{2} \tag{C1}$$

then the sideband at $(W_s-\Delta)$ will be picked up by the loop (centered at W_o), and a false lock-on effected. (note that we have conservatively assumed a zero probability of the loop pull-in mechanism opposing the sweep and pulling B to the left in order to pick up $(W_s-\Delta)$ first pops up closer to W_o (but in the left of W_o) then is W_s. This conservatism is warranted because of the narrow pull-in range of the loop especially when fighting the push-to-the-right of the sweep circuit.)

Therefore, in this subcase, equation (C1) shows that the limiter will cause false lock-on if

$$\Delta \leq B/4 \tag{C2}$$

whereas, without the limiter, no false lock-on would be effected.

Subcase B: Interference Initially Inside 2nd IF Passband

This situation may be pictured as

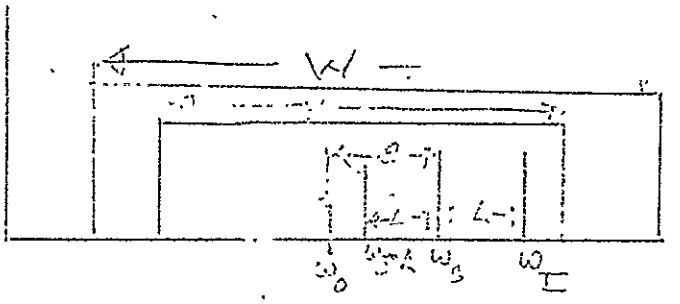


FIGURE C3

It is seen that, for this subcase, not only must the condition for the previous subcase ($\Delta \leq b/4$) be satisfied to cause false lock-on, but also

$$E \geq \Delta \qquad \text{(C3)}$$

for false lock-on to occur.

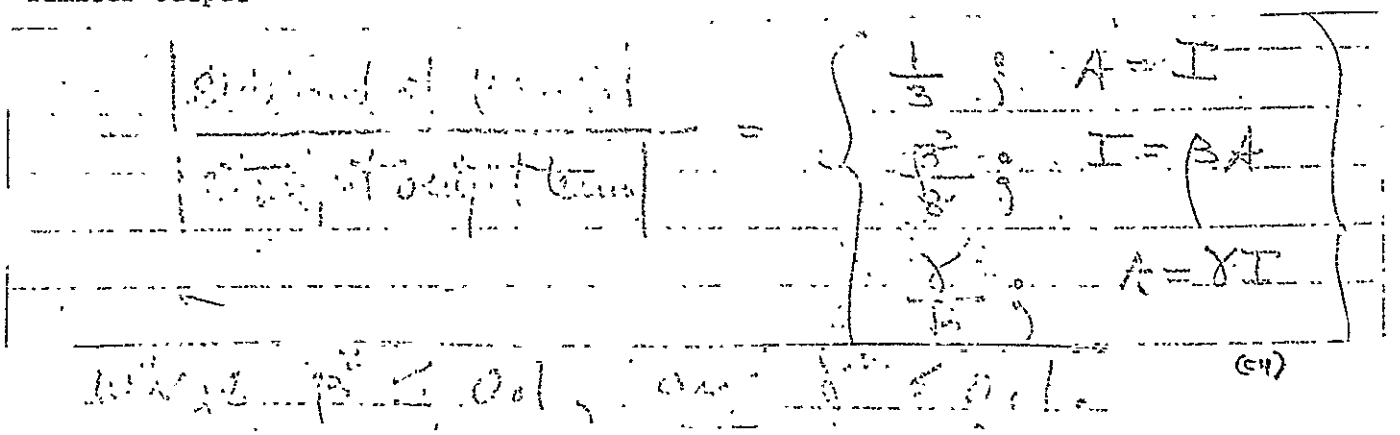
III. Amplitude Considerations

It is now necessary to consider what amplitudes are required in order for the false lock-on situations described above to actually occur.

We define A = signal amplitude at limiter input

I = interference amplitude at limiter input

Referring to Figures 3 and 5 in the text, we then see that, at the limiter output



(C4)

It is to be noted, however, that the resilts in equation (C4) pertain to the noise-free case. Analysis of the case, inclusing noise, in quite involved. However, according to work done by I. S. reed at the Rand Corporation, it appears that the sideband magnitudes for the case with noise, are essentially the same as the magnitudes in the noise-free case, provided that the signal/noise ratio in the limiter passband is greater than unity. (If the signal/noise ratio is less than unity, the sideband magnitudes apparently fall off extremely rapidly with the noise/signal ratio).

Consequently, we will assume that the signal/noise ratio in the limiter passband is greater than unity, and employ (C4) to obtain the magnitude of the desired sideband. Since Reed has also shown that, under the assumed ligh signal/noise condition, the signal/noise ratio for the original input frequencies (one of which has to be the strongest output term in C4), is preserved, in the limiter, we obtain from C4:

$$\left[\frac{S}{N}\right]_{\text{Post L.}} = \begin{cases} \frac{1}{9}\,\frac{B_{IF}}{B_L}\left(\frac{S}{N}\right)_{IN}; & A = I \\ \frac{B^4}{64}\,\frac{B_{IF}}{B_L}\left(\frac{S}{N}\right)_{IN}; & I = BA \\ \frac{\gamma^2}{4}\,\frac{B_{IF}}{B_L}\left(\frac{S}{N}\right)_{IN}; & A = \gamma I \end{cases} \qquad (C5)$$

Where B_{IF} = bandwidth of bandpass limiter

B_L = one-sided looo noise bandwidth

$\left[\frac{S}{N}\right]_{loop}$ = signal/noise power ratio in one-sided loop bandwidth

$\left(\frac{X}{N}\right)_{in} = \left[\frac{\text{power of strongest signal}}{\text{noise power in } B_{IF}}\right]$ BEFORE LIMITING

≥ 1

A conservative figure for acquisition of a phase-locked loop is

$$\left[\frac{S}{N}\right]_{loop} \geq 1o \qquad \text{(C6)}$$

Therefore, conbining (C5) and (C6) we see that acquisition to the sideband at W = a - Δ can be effected if

$$\left[\frac{B_{IF}}{B_L}\right]\left[\frac{S}{N}\right]_{IN} \geq 9.0 \; ; \quad A = I$$

$$\left[\frac{B_{IF}}{B_L}\right]\left[\frac{S}{N}\right]_{IN} \geq \frac{640}{B^2} \; ; \quad I = BA$$

$$\left[\frac{B_{IF}}{B_L}\right]\left[\frac{S}{N}\right]_{IN} \geq 10 \; ; \quad A \leq 0.1I \qquad \text{(C7)}$$

Where $\left[\frac{S}{N}\right]_{in} = \left[\frac{\text{power of desired signal}}{\text{noise power in } B_{IF}}\right]$ Before Limiting

and where $\left[\frac{S}{N}\right]_{in} =$ [illegible] for $A = \gamma I$

The results in (C7) are predicated on the assumption that:

1) The signal/noise power ratio in the i-F passband, before limiting, is ≥ 1 for the stronger of the two sinusiodal inputs.

2) $\beta^2 \leq 0.1$

Finally, if we make the almost always valid assumption that

$$\frac{B_{IF}}{B_L} \geq 100$$

then (C7) shows that lock-on to the sideband at $W = a - \Delta$ can be effected under the simple conditions that

1) $\left[\frac{S}{N}\right]_{in} \geq 1$

2) $\left[\frac{J}{S}\right]_{RF} \geq 1$

or

3) $\left[\frac{S}{N}\right]_{in} \geq \frac{6.4}{\left[\frac{J}{S}\right]_{RF}}$

4) $\left[\frac{J}{S}\right]_{RF} \leq 0.1$ (C8)

where $\left[\frac{J}{S}\right]_{RF} = \left[\frac{\text{power of interfering sinusoid}}{\text{power of desired sinusoid}}\right]_{\substack{AT \\ RF}}$

IV. Probability Considerations

We will now calculate the probability of a false lock-on, assuming that: 1) The receiver center-frequency ($=W_o$) prior to lock-on

2) The frequency ($=W_I$) of the interfering sinusoid.

3) The frequency ($=W_S$) of the desired sinusoid.

have equal and independent probabilities of lying any where in the sweep range W_o, and that the limiter sideband at $W = a - \Delta$ has sufficient amplitude (CF section III of this appendix) to permit loop lock-on if the

loop is centered at W = a - Δ.

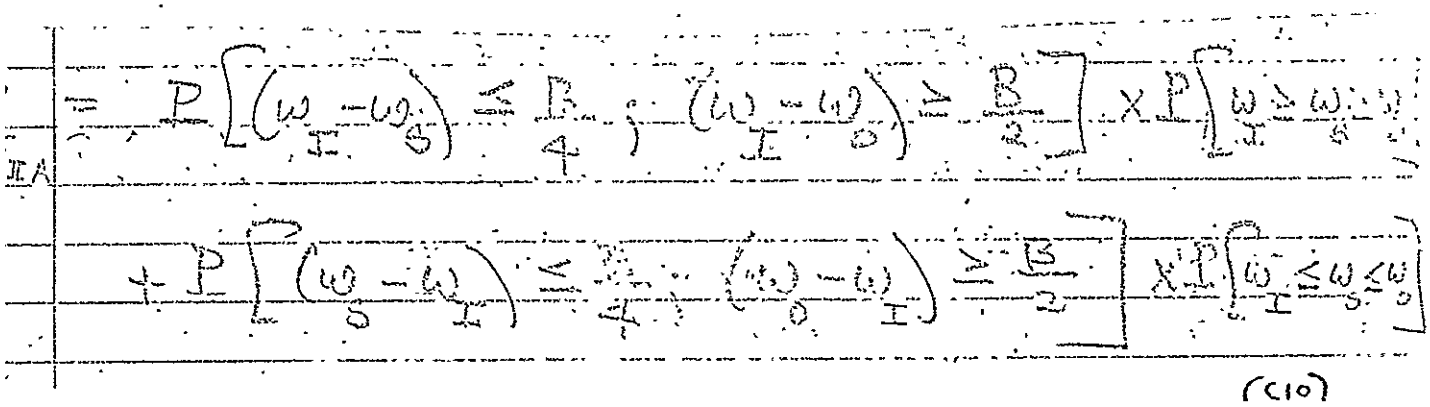
Without a limiter the probability of false lock-on is obviously

$$P/F = 1/2 \qquad \text{(C9)}$$

Since there is equal probability that the loop will first encounter either the signal or the interference.

With a limiter, the probability will be 1/2, plus the probability of the false lock-on conditions of case II (in this appendix) occuring.

The probability of limiter-induced false lock-on for subcase IIA is, from equation (C2) =



(C10)

The first term of (C10) represents the configuration of Figure C2, where the receiver is sweeping from left to right , to pick up W_s. The second term of (C10) represents the minor image of Figure C2, where the receiver is sweeping from right to left to pickup W_s (and where W_s W_I). The internal arguments of the probabilities of (C10) represent the respective requirements of that =1) Equation C2 be satisfied, and that

2) the interference be initially outside the 2nd IF passband.

Since all functions are uniformly distributed, the two terms in (C10) are equal and we can write

$$P_{F_{IIA}} = 2P\left[(\omega_I - \omega_s) \le \frac{B}{4} \, ; \, (\omega_I - \omega_o) \ge \frac{B}{2}\right] \times P\left[\omega > \omega_s\right] \qquad (C11)$$

Examination of (C11) shows that we can reqrite it as:

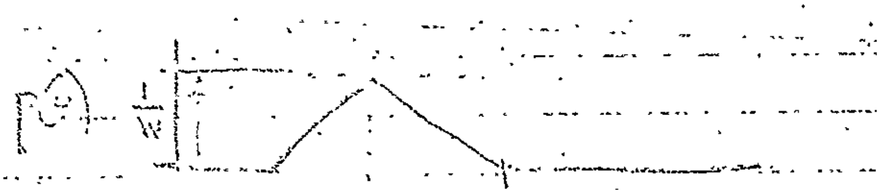
$$P'_{F_{IIA}} = 2P\left[0 \le (\omega_I - \omega_s) \le B/4 \, ; \, (\omega_I - \omega_o) \ge \frac{B}{2}\right]$$

$$= 2P\left[\omega_s \le \omega_I \le \left(\frac{B}{4} + \omega_s\right) ; \; \omega_o \le \omega_s - \frac{B}{2}\right]$$

$$= 2P_1\left[\omega_s \le \omega_I \le \left(\frac{B}{4} + \omega_s\right)\right] P_2\left[\omega_o \le \omega_s - \frac{B}{2}\right] \qquad (C12)$$

where the last equality has made use of the fact that the probability of W_s and W_I are independent, regardless of where W_s happens to be.

The probability density function of $\Xi = \omega_1 - \omega_2$ can be shown to be a triangle like



where W_1 and W_2 are any of the independent variables we have mentioned, all having density functions.

$$p(\omega) = \frac{1}{W} \qquad 0 \le \omega \le W$$

Consequently:

$$P\left[0 \le (\omega_2 - \omega_1) \le \frac{B}{4}\right] = \int_0^{B/4} p(z)\,dz$$

$$= \frac{1}{W}\int_0^{B/4}\left(1 - \frac{B}{W}\right)dz$$

$$= \frac{B}{4W}\left[1 - \frac{B}{4W}\right] \qquad (C13)$$

Similarly,

$$P\left[\frac{B}{2} \le (\omega_2 - \omega_1)\right]$$

$$= \frac{1}{W}\int_{B/2}^{W}\left(1 - \frac{B}{W}\right)dz$$

$$= \frac{1}{2}\left[1 - \frac{B}{W}\left(1 - \frac{B}{4W}\right)\right] \qquad (C14)$$

Consequently, from (C12) through (C14)

$$P_{\text{error}} = \frac{1}{2}\left[\frac{B}{4W}\left(1 - \frac{B}{8W}\right)\right] + \frac{1}{2}\left\{1 - \frac{B}{W}\left(1 - \frac{B}{4W}\right)\right\}$$

$$= \frac{B}{4W}\left(1-\frac{B}{8W}\right)\left[1-\frac{B}{4W}\left(1-\frac{B}{4W}\right)\right]$$

$$< \frac{B}{4W} \qquad \text{since } \frac{B}{W} < 1 \qquad (C15)$$

Now consider case IIB. Examination of Figure C3 shows that the false lock-on probability of this case is (including a factor of 2 for the minor image terms)

$$P_{FL(IIB)} = 2P\left[(\omega_1-\omega_0)<\frac{B}{2} \text{ and } (\omega_2-\omega_0)\leq\frac{B}{2}\right] \times P\left[\omega_2 \text{ is the}\right.$$

$$= 2P\left[0\leq(\omega_1-\omega_0)<\frac{B}{2};\ 0\leq(\omega_2-\omega_0)\leq\frac{B}{2}\right]$$

$$= 2\sum_{i=1}^{3} P_i\left[0\leq(\omega_1-\omega_0)<\frac{B}{2}\right] P_i\left[0\leq(\omega_2-\omega_0)\leq\frac{B}{2}\right]$$

$$(C13)$$

Using (C13) as an analogy we now find

$$P_1 = \frac{1}{W}\int_0^{B/4}\left(1-\frac{\omega}{B}\right)d\omega = \frac{B}{4W}\left[1-\frac{B}{8W}\right] \qquad (C17)$$

$$P_2 = \frac{1}{W}\int_0^{B/4}\left(1-\frac{\omega}{B}\right)d\omega = \frac{B}{8W}\left[1-\frac{B}{16W}\right]$$

$$(C18)$$

Consequently, from (C13), (C14), and (C15) we obtain

$$P_{FEB} = \frac{B^2}{32W^2}\left[1+\frac{B}{8W}\right]\left[1+\frac{B}{16W}\right]$$

$$< \frac{B^2}{32W^2} \qquad (C16)$$

Combining (C15) and (C16) we obtain the extra probability of false lock-on induced by the limiter

$$P_{FE} < \frac{B}{4W} + \frac{B^2}{32W^2} = \frac{B}{4W}\left[1+\frac{B}{8W}\right] \qquad (C17)$$

Finally, noting, that without the limiter, we already had a 50% probability of false lock-on, we find the ratio of false lockon with and without a limiter to be

$$\frac{[P_F]_{LIM}}{[P_F]_{NO\ LIM}} < \frac{1/2 + \frac{B}{4W}\left[1+\frac{B}{8W}\right]}{1/2}$$

$$= 1 + \frac{B}{2W}\left[1+\frac{B}{8W}\right] \qquad (C18)$$

FINAL REPORT

S-BAND ODOP TRANSPONDER

Prepared By

J. P. Pourtales
Project Manager

Approved By

D. A. Gehlke
Vice President Engineering and Operations

29243
3/5/66
2cy