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SURVEY/STUDY OF THE INTERCONNECTION PROBLEM IN MICROELECTRONICS

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IN MICROELECTRONICS

for

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

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FINAL REPORT OF FIRST PHASE (NASw-919)

CONCLUSION AND MANAGEMENT CONSIDERATIONS

July 20, 1965

1. INTRODUCTION

This report contains the conclusions and management

considerations that have resulted from the survey/study con-

ducted under NASA contract NASw-919.

The purpose of this survey/study was to evaluate the state

of the microelectronics art with emphasis on the interconnection

problem, particularly as it relates to systems reliability.

During the course of this study, pertinent groups and individuals

were contacted in the NASA Centers, in Military facilities, and

in the plants of both systems and components manufacturers.

Our visits were made with, and coordinated by, the manage-

ment personnel in the organizations which were contacted. We

wish to express our appreciation for the wholehearted cooperation

received from the NASA Centers, from the Military, and from the

many industrial organizations visited. A survey of this type

would be impossible without the full cooperation of all of

these organizations.

From these interviews we have endeavored to determine the

trends in the microcircuitry field and, from these trends, the

weak spots or areas where further attention is warranted at

this time. It is believed that as special attention is given

to these areas, the state-of-the-art of microelectronics will be advanced in a manner that will particularly help NASA and other procurement agencies. Further, the field of microelectronics as a whole would be strengthened.

It is realized that in any technology as dynamic as the microelectronics field, there are many strong and quite valid, and frequently diverse, opinions regarding future developments. Our recommendations are based, to a large degree, upon the talks we have had with persons engaged in the day-to-day task of designing, developing, manufacturing and packaging deliverable hardware. When we have not found agreement among those interviewed, we have had to make a decision as to what course of action seemed most reasonable and most likely to improve the microelectronic systems to be required by future NASA programs -- we trust that the majority of these conclusions are valid.

During the course of our interviews, we have become aware of the acute need for a concise statement of those particular aspects of microcircuitry which are, in a sense, critical with respect to the making of proper management decisions. A vast amount of information and data are available on the subject of microcircuitry. Too often, however, management personnel are so pressed for time that it is not possible for them to always acquire sufficient knowledge of the state-of-the-art at any given time to confidently make the decisions which are required of them.

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In that portion of this report entitled, "Management Considerations", we have tabulated those points regarding the current state-of-the-art of microcircuitry which we feel should be most valuable to management officers and personnel.

The microcircuitry industry is going through a period of tremendous change, caused to a large degree by economic pressure to obtain profitable plant operation. This pressure has resulted in an overall tightening up of plant operations and processes. More exacting design, tooling, and production control have resulted in integrated circuit yields which would have been thought impossible to obtain a year or so ago. These substantially higher yields have caused production costs to tumble, and have made feasible the consideration of multiple function chips of a high order of complexity. When properly applied, these complex chips will improve systems reliability by orders of magnitude. Within a very few years, complex chip costs will be reduced to pennies per function. This cost reduction potential has yet to be fully realized and appreciated by the electronics industry. Its impact has yet to be evaluated. There can be no question but that it will cause a drastic reappraisal of the market potential for electronic equipment.

The electronic industry is already highly developed and there are definite trends which in all probability cannot now be changed. Where possible, these trends should be augmented on

a selective basis to further the state-of-the-art in a manner
to favor the requirements of NASA advanced systems hardware.
At this time we would not recommend the sponsorship of radically
new concepts and approaches. The industry needs a period of
stability - one in which yields and reliability can be brought
under proper control, and in which the low cost potential of
microcircuitry can be fully realized.

The industry is rapidly gravitating toward the multiple
function chip - chips which may have as many as 100 functions
today and, in all probability, thousands of functions in a few
years.

Since the majority of the packaging concepts now in use
have been conceived for single function chips, this multiple
function progress has placed the packaging of microcircuitry
in a state of instability and change. While it is fully realized
that standardization, per se, is premature for the microcircuitry
industry, it is strongly recommended that the industry be guided
by NASA and other major procurement agencies so that the multiple
function packaging, at least, develops in such a manner as to
provide some degree of interchangeability. During the course of
this study, a number of individual approaches to the packaging
of multiple function chips, and of multiple chip assemblies,
have been seen. All of these have been only slightly different
from each other, but sufficiently different to preclude any

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degree of interchangeability, particularly because of lead configuration. The industry would be substantially helped by some degree of uniformity in the packaging of multiple function chips and multiple chip assemblies.

The multiple function chip represents a direct method of substantially reducing the number of interconnections. For this reason alone, the multiple function concept is particuarly interesting from the standpoint of reliability. As the single silicon chip includes sub-systems, and even rather involved systems, the overall systems reliability will increase by orders of magnitude. This is so because the complex chip can be considered as a monolithic structure from the reliability standpoint and should have substantially the same failure rate as a chip with only a single function. While, to our knowledge this concept has yet to be proven experimentally, it would appear to be valid because the major failure rates on current integrated circuits are mainly associated with the interconnections to the chip rather than with the circuitry diffused into the chip. Therefore, efforts to increase the complexity of the monolithic structure are directly improving the interconnection picture.

We have noticed considerable concern on the part of systems manufacturers as to whether to make or buy the microcircuitry required for the systems which they manufacture. This matter will be discussed in the section, "Management Considerations".

There is an apparent trend, however, away from the manufacture
of integrated microcircuitry by systems manufacturers. The
cost picture is probably one main reason for this, as is also
the fact that only by fabricating large quantities of micro-
circuitry can the manufacturing processes be brought under
sufficient control to approach reasonable yield and accurate
reliability figures.

A great deal of controversy exists regarding the relative
merits of soldering versus welding. Our own appraisal of this
situation would be that it is apparently easier to obtain a
reliable soldered connection than a reliable welded connection.
Proponents for soldering also stress its redundant nature and
the ease with which large complex arrays can be handled. On
the other hand, if absolute control can be maintained over
lead materials and processes, welding appears to be quite
satisfactory; but this absolute control is mandatory. More
information regarding the physics of interconnection bonds is
obviously needed to insure that maximum reliability is achieved.

We have also noticed a decided reluctance to use plug-in
connectors. The consensus is that the plug-in connectors
themselves represent a major failure mode and therefore adversely
affect the reliability of any microcircuitized system in which
they might be used. There is a definite trend toward the use of
soldering or wire-wrap techniques for interconnecting circuit
modules into a system.

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There is more and more evidence of systems manufacturers being more cognizant of the need for so designing individual integrated circuits that they can be easily manufactured by the semiconductor houses. This is critical to the obtaining of good yields, reasonable cost, on time delivery, and reliable operation.

There is need for more management awareness of the basic problems inherent in the manufacture and use of integrated circuitry. Too often there is an attempt to fit problem solutions into existing budgets rather than to obtain management support for the total amount of work which actually has to be done.

Chip mounting, chip packaging, and interconnections to the chip are in a state of flux. The importance of chip mounting and of making better connections to the chip have been brought to the forefront by the trend toward multiple chip packaging. Chips are being mounted to thin film substrates which contain the interconnections for the sub-system being prepared. Flip chip techniques are somewhat of an enigma. Some manufacturers claim to be able to satisfactorily mount chips by this technique. The large quantity manufacturers seem to be more conservative regarding the flip chip mounting method. Planar chip mounting methods are being developed in a number of companies. Others are resorting to more conventional mounting arrangements with flying leads and attempting to perfect the processes so that

they will be highly reliable. All aluminum and all gold systems are being studied to overcome bi-metallic problems such as purple plague.

There is interest in unorthodox bond forming methods such as electron beam welding, laser welding and conducting "epoxy-like" materials. It would now appear that these processes will be only used where they provide some special advantage. The station costs for electron beam and laser welding are quite high.

Probably the most significant change in packaging will be the transferring of the hermetic seal from the package, where it is now, to the chip where it belongs. This is particularly important with multiple function packages where the package size is larger and more leads are required, making the case seal that much more difficult. Also, the case costs are being evaluated and new designs will stress cost reduction. This cost reduction is necessary because the cost of the chips is falling so rapidly that chips are now being installed in cases which are considerably more expensive than the chips which they are protecting. As the costs of the chips continue to fall, this disparity will become even more pronounced.

The validity of some process specifications has been questioned by many of the manufacturers we have visited, and it is apparent that every effort must be taken to insure that specifications which control production practices be as realistic

as possible, particularly from the standpoint of manufacturing costs. The fact must not be overlooked, in any facet of work in the microelectronics field, that this field is now cost controlled to a very large degree. Manufacturers are looking for ways to reduce manufacturing costs to stay competitive, and any hindrance to their being able to reduce their costs will not be tolerated if any alternative is available.

There are emerging large array concepts which will tend toward standardized matrices with very low function costs. These concepts are termed cellular logic, planar logic, large area MOS arrays, etc. Function costs are now considerably less than a dollar in some configurations and will be a few cents per function in two or three years. This is a concept to keep in mind, for the cost situation is going to revolutionize the industry.

Reliability assurance is another difficult area of micro-circuitry. The failure rates are now so low that it is practically impossible, with any reasonable expenditure of time and money, to determine level of reliability before the circuits being evaluated are obsolete. As these failure rates become still lower, the classical reliability methods will not be practical at all. We have mentioned the improvement of reliability inherent in the complex array chip containing many interconnected functions. This is the most significant area of gain in the area of reliability

because the complex chip has, potentially at least, the same failure rate as the simple chip. The major failure modes with integrated circuitry, however, are involved with the making of connections to the chip. These failure modes are practically all associated with the control of production processes. Since these processes are controllable, better on-line inspection, more comprehensive employee training, and a general tightening up of the semiconductor lines will make significant progress in the reliability of the basic chip. The semiconductor manufacturers seem to be in agreement with this objective, and every effort is being made to improve production processes.

Following is a listing of areas of the field of micro-circuitry which are particularly pertinent at the present time. We sincerely feel that guidance in these fields by NASA and by other large users of microcircuitry will be extremely helpful and that, if such guidance is wisely managed, significant state-of-the-art improvements can be realized.

LOGIC CONSIDERATIONS

THE MULTIPLE FUNCTION CHIP

THE MULTIPLE CHIP ASSEMBLY

THE MICROCIRCUIT PACKAGE

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THE INTERCONNECTION BOND

THE CONNECTOR

THE SYSTEMS DESIGN

COMPONENT AND SYSTEMS RELIABILITY

MANAGEMENT CONSIDERATIONS

The remaining sections of this report will deal with these topics in the order noted.

2. LOGIC CONSIDERATIONS

There can be no question but that the multiple function chip represents the direction toward which the microcircuitry industry is heading, and that chips of greater and greater complexity will be produced by all of the suppliers who remain in this field. This is an unmistakable trend and it will have a more significant effect on both the reliability and cost of integrated circuitry.

As these chips become more complex, and particularly as they contain larger segments of "on chip" connected circuitry, the overall system interconnection problem will be greatly alleviated. This is actually the only way that real inroads can be made in the interconnection problem. In the future there can be no question but that sub-systems and systems of some complexity will be diffused into a single silicon chip.

As the multiple function chip technology progresses, however, the problem of what to put on the chip must be solved. If this problem is not solved, the large array concept will revert back toward customized circuitry and away from potential standardization. As a complex array becomes a sub-system, it, by definition becomes less of a universal item and more of a segment of circuitry tailored for a specific application.

To realize the full potential of the complex chip for cost reduction, the technology must be developed around widely

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usable arrays. This is a problem which is currently with us. Now that large arrays can be made, of what shall they consist? Unfortunately, many of the complex chip programs are merely solving in-house requirements for marketable hardware and the longer-range need is being apparently neglected.

Some manufacturers are considering universal matrices and this effort should be encouraged.

It is felt that insufficient consideration is being given to the critical analysis of the multiple function package situation from the standpoint of universal computer requirements. Perhaps the problem goes back even farther to the development of a computer language that would be acceptable to those organizations engaged in producing computer systems.

Once such a universal computer language is available, it could then be broken down into function packages which would be capable of handling any anticipated logic problems. These function packages could then be manufactured by those microcircuitry manufacturers who had an interest in so doing and who had the capability to manufacture multiple function packages.

This procedure would appear to minimize the problems of developing a standard set, or a usable set, of multiple function microelectronic packages. First, would come the task of developing a computer language which would be as universal as possible.

Then it would be a relatively manageable task to divide this computer language into multiple function packages which could then be used to develop whatever logic might be required for a given computer application. In this way, a standard set of multiple function logic packages would evolve which would have some real meaning and utility. Such a program is urgently needed at this time to give some tangible direction to the rapidly developing multiple-function technical capability. Complex arrays are becoming a practical reality much earlier than had been initially anticipated.

A carefully directed program effort would serve as a catalyst for the industry recognition and effort needed if a family of usable multiple function packages is to materialize within a reasonable time. If such development guidance is not presented to the industry, the multiple function capability will just "grow" as required by various hardware applications, and the likelihood of any substantial degree of universal application will be remote. In situations like this it is usual to let nature take its course, and it is perfectly true that in time a usable set of multiple function modules would evolve. However, there can be no question but that careful planning at this stage could advance the availability of universal multiple function packages by years. It would seem an unfortunate waste

to have to wait for a trial-and-error process of attrition to obtain maximum utility from the multiple function package concept. The potential merit of this concept is too significant for this.

It is recommended that the possibility of developing a computer language (that would be, to a large degree, universal) be considered together with the manner in which such a computer language could be broken down into a series of widely applicable multiple function components. This would be the first step toward a family of multiple function modules that would have some basis for orderly establishment and that would be widely applicable throughout the computer industry.

3. THE MULTIPLE FUNCTION CHIP

The multiple function chip, in complex form, is a recent technological achievement that has been made possible by improvements in semiconductor process control which, in turn, have resulted in yield improvements that had not been anticipated as a practical reality for some time to come. During the course of our study, chips have been seen with as many as 600 transistors and associated circuitry diffused into them. This represents a current manufacturing capability for chips of considerable complexity.

We believe that the current capability in complex chip technology should be exploited for those applications where a widely usable component can be produced. So-called cellular logic and planar logic are perhaps the best known examples of complex chip arrangements which can have an immediate potential of some degree of wide application. For simplicity we will refer to logic schemes of this type as "matrix logic". Basically this type of logic has been devised to minimize the interconnection problem.

Matrix logic consists of a matrix of, ideally, identical logic blocks or cells in which all connections (in idealized form) are made only from one cell to its neighbor. In function with two input connections (top and left side) and two output connections (right side and bottom). This generates a single

layer interconnection pattern. Practically, other connections are usually employed, but the ideal arrangement can be approximated.

In its most advanced form, matrix logic would have the entire matrix of interconnected functions diffused into a single chip of silicon thereby creating a monolithic sub-system.

Within the next five years it should be possible to practically diffuse matrices as large as 50x50 functions (2500 functions total) onto a single silicon chip. With the yields rising as rapidly as they are, and with techniques available to by-pass inoperative functions, there is no reason why such large arrays will not soon be possible to manufacture with a practical yield.

Arrays of this type would be responsible for drastic reductions in electronic function costs.

It is felt that work could be profitably done at this time on a universal matrix logic chip. Computer manufacturers have suggested that an integrator slice might be the most practical initial effort and one which could be widely used in DDA type computers. The objective would be to have a complete integrator on a single silicon chip. This would not only test the multiple function chip capability, but also provide a usable complex chip sub-system.

Since the integrator chip would have universal application in DDA computers it is believed that it would be economically sound to proceed with this application to both obtain a needed

component and, at the same time, enable the advancement of the state-of-the-art of multiple function technology by directing it toward a reasonably complex application.

On the surface, the matrix form of complex chip would seem to be an ideal method of minimizing interconnections and for making an approach to the involved problem of sub-system standardization. We have noted, however, that some of the semiconductor manufacturers feel that the conventional complex chip will be less expensive for a given application because of the added functions required for the matrix array approach. Here again, is appreciation for the economic factors coming to the fore as it will continue to do in the microcircuitry field.

We believe that a universal type of complex chip array should be developed, and that the integrator chip be one consideration - the main objective being to develop a complex chip with as wide a utility as possible.

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4.   THE MULTIPLE CHIP ASSEMBLY

The multiple chip assembly is made up of a number of silicon chips of more or less complexity mounted onto a suitable substrate and interconnected on this substrate. The substrate is usually glass or alumina, and the interconnections are typically made through a thin film pattern deposited onto the substrate prior to mounting the individual silicon chips.

Through the use of the multiple chip assembly technique, it is possible to develop a microcircuitized sub-system of substantial complexity with a minimum of tooling costs. The tooling costs are minimized because the complex sub-system can be produced by suitably interconnecting available silicon chips of moderate complexity.

The multiple chip assembly is of particular interest because it provides a method for making small quantities of complex electronic circuitry without the expense of time delay of making a special complex array. It is an exceedingly flexible process and one which should be developed further.

During the course of this survey/study a number of examples of the multiple chip assembly process have been inspected. From what has been seen, the average current state-of-the-art multiple chip assembly would comprise 16-25 integrated circuit chips mounted onto a substrate onto which had been deposited the thin film interconnection pattern required for the desired sub-system

configuration. The average substrate size has been 3/4" to 1" square.

When it is appreciated that the individual silicon chips can be multiple function chips, the possible complexity of the multiple chip assembly becomes apparent. It is feasible for the 3/4" square substrate to contain a complex electronic sub-system and at the same time have a high degree of flexibility because the sub-system is made up of a plurality of silicon chips, each individually attached to the thin film substrate.

The basic problems which have yet to be adequately solved are those involved with the mounting of the silicon chips onto the substrate. There are several methods for doing this.

The chips can be bonded by a soldering, eutectic, or other fastening process with the required connections being made by flying wire leads to the thin film connection pads. This is a widely used process and one which can be perfected to the point where reliability is very good. At this writing, this is in all probability the preferred process, even though it would be highly desirable to eliminate the flying wire leads. However, it would not be desirable to remove the flying wire leads if by so doing other complications were introduced which would adversely affect reliability.

There is also the widely publicized flip-chip chip mounting process. With this process, the integrated circuit chips are

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mounted face down onto the substrate and connections are made to the thin film interconnection pattern through special soldering or ultrasonic techniques. On the surface, at least, this would appear to be an excellent approach for mounting silicon chips to thin film substrates. When the size of the silicon chips is carefully considered, the flip chip problem is brought into focus. The making of the ten or more connections to a chip less than 0.01" square is a severe alignment task. It is especially severe because the connections are not readily accessible and are therefore not easily inspected. Several companies indicated that they have the flip chip process under adequate control. Others have become cautious about using the flip chip technique for production programs. It might be fair to say that the flip chip process is marginal for integrated circuit chips, and possible for transistor chips at this time. The difference is, of course, in the number of interconnections which must be transferred to the substrate. In any event, the potential advantages of the flip chip approach are so great that every effort should be made to develop a technology that is satisfactory.

Another process which is becoming used to a somewhat larger degree is the so-called planar method. In this, the silicon chips are inserted into holes, or cut outs, in the thin film substrate so that the top surface of the chip is flush with the top surface of the thin film substrate. In other words, the silicon chips are recessed into the thin film substrate and after this is done

the surface of the integrated circuit chip is on the same plane
as the surface of the thin film substrate. Bridging connections
are then applied from the thin film interconnection pads on the
thin film substrate to the interconnection pads on the silicon
integrated circuit chip. These interconnection jumpers can be
applied by evaporation techniques, _provided_ that any void between
the integrated circuit chip and the thin film substrate is filled
with a suitable material which will wet both the silicon chip
and the substrate material. The importance of this material
for filling the void is such that companies working in the field
of planar multiple chip assemblies consider this material to be
a proprietary product. Any void at all in this filling material
will produce a weak area in the thin film bridging connectors.
The planar method for mounting chips onto thin film substrates
is perhaps the most complex of the three processes to work with,
simply because of the difficulty of so embedding the silicon
chip into the substrate that the surface of the chip is in the
same plane as the surface of the substrate and all voids between
the chips and the substrate are properly filled. The connections
are accessible, however, and this is the reason for using the
planar approach in lieu of the flip chip approach.

  With each of these three methods for making connections
between the silicon chips and the thin film interconnection
substrate, the validity of the interconnection on the silicon

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chip interconnection pads and on the thin film substrate inter-connection pads determines the reliability of the completed multiple chip assembly. Since a large number of such bonds will be required for any complex multiple chip assembly, the nature of these bonds is of utmost importance. As a goal, the integrity of the bonds should be such that the entire multiple chip assembly can be realistically considered a monolithic structure. We have seen developments which would lead one to believe that this is possible.

It is suggested that the multiple chip assembly technology be pushed with a goal of highly reliable structures with bonds having monolithic characteristics.

5. THE MICROCIRCUIT PACKAGE

The major reliability problems with integrated circuitry are associated with the packaging of the silicon chips. Such factors as the bonds to the chip, the bonds to the case leads, purple plague, the hermetic seal - are all packaging problems.

The microcircuit package is in a state of flux primarily because the present packages were designed for single function chips and for chips which were relatively expensive. However, the conventional flat pack and the TO-5 can are too expensive for the low cost single and multiple function chips which are now being produced.

The hermetic seal, which has been more troublesome in the flat pack because of the geometry of this form of package, will tend to become more so as the flat pack type of package becomes larger to accomodate multiple function chips. This is due to the longer seal lengths and the larger number of leads into the package. A definite trend in silicon chip packaging is to remove the seal from the package and to put it on the silicon chip where it belongs.

The transferring of the seal onto the chip requires the avail-ability of suitable sealing materials which can be deposited direct-ly onto the silicon chip and which will form a suitable hermetic seal. The most satisfactory sealants will, in all probability, be types of low melting point glass that will have to have a tempera-ture coefficient of expansion compatible with silicon and at the

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same time be non-hygroscopic. Such glasses can probably best be applied by sputtering.

It can be appreciated that if suitable lead attachment techniques are worked out, the glass encapsulated chip could be used "as is" and the glass would form a very inexpensive package. This is a promising form of future packaging. In any event, a package of this general type is a "must" if the low cost potential of integrated circuitry is to be fully exploited; it would be ludicrous to package a chip costing pennies in an enclosure costing a dollar or more.

The internal bonding problems can best be solved by careful quality control and on-line inspection. The bonds to the silicon chip and the bonds to the package terminals are made by hand, and improvements here can only be made by more careful work and by better tooling arrangements. It has been pointed out to us that the cheapest production tool by far, for high-accuracy assembly, is a girl and a microscope. This high-accuracy is what we are dealing with in practically all integrated circuit assemblies. The girl-microscope combination must not become tired or careless, and means must be available for careful inspection before shipment to customers. It would seem to be a simple matter to pick up bad connections, but defective units are occasionally shipped by even the best of manufacturers which is testimony to the difficulty of maintaining sufficiently close quality control over these tiny

assemblies. The quality of workmanship is steadily improving
due to continuous improvement of process control. It is felt
that significant reliability improvements are being made particu-
larly in the areas of connections to the silicon chip.

We have received every possible, opinion on purple plague,
from its not being a problem at reasonable temperatures to the
opinion that it is always a problem in a gold-aluminum system
where very low failure rates are required. The consensus would
seem to be that below 200°C purple plague is no problem, whereas
at temperatures in excess of 200-250°C it should be cause for
concern.

An all-aluminum or all-gold system would eliminate the
bi-metal problems, but they must be approached cautiously. The
problems of the gold-aluminum system are well known through many
million device hours of environmental testing. The all-aluminum
system will have other problems which at this writing are not well
known; such will also be the case with the all-gold system. Any
sudden change to another system, therefore, would not be wise.

Companies have also pointed out that even when purple plague
is in evidence to a substantial degree (the figure quoted was the
amount produced by 200°C for seven years), the bond would still
not fail if it were properly made initially. Bonds which will
stand high shock and acceleration loads initially (typically 500g

shock and 20,000g acceleration) should not be adversely affected by purple plague.

One facet of the purple plague problem is the high temperature storage requirements which have been part of some specifications. These high temperature storage specifications should be evaluated to determine their validity. We understand that this is being done and in some cases, this requirement is being modified.

Since the bond to the silicon chip connection pad is the most critical aspect of silicon chip packaging, some means for checking this bond in a non-destructive manner is highly desirable. RF and IR radiation from faulty bonds are being evaluated as effective means for detecting bond faults.

Considering the package situation as a whole, we recommend that work be continued in the area of getting the hermetic seal onto the silicon chip. This is the most promising aspect of the packaging problem and one where substantial inroads can be made on both the cost and reliability of integrated circuits. This will require the development of satisfactory sealants and suitable means for attaching lead wires to the silicon chips so that, in connection with the sealant, adequate mechanical strength can be achieved to permit the sealant to be used as the chip package. We believe that as much progress can be realized in this area of the packaging problem as in any other, and suggest that every effort be made to solve the encapsulation problem.

6. THE MULTI-LAYER BOARD

Much more effort is now being expended during the design of microcircuitized systems to minimize the required number of interconnection layers. The multi-layer interconnection board, however, will undoubtedly continue to be used for the foreseeable future.

It is our opinion that the multi-layer board manufacturing technology is coming along satisfactorily. There is, though, an urgent need for education among systems manufacturers on the limitations and design parameters of multi-layer boards.

It would appear that the majority of multi-layer circuit board problems have been caused by a lack of understanding, or a lack of transfer of knowledge between the manufacturers of printed circuit boards and systems designers. The multi-layer board manufacturers believe that it is always desirable for the systems manufacturer to consult with them before the dimensions for any multi-layer board are firmed up. Too often the multi-layer board dimensions are established by designers who are not familiar with the inherent design limitations of these boards. When this is done, the multi-layer board usually has to be squeezed into too little space and the manufacturing processes (for these boards) modified to the extent that production difficulties are encountered, thus necessitating late deliveries, excessive costs, etc. If, on the other hand, these multi-layer board design limitations

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are thoroughly understood by the systems designers, the boards can be adequately fabricated with no serious manufacturing problems and/or delays.

We recommend that an effort be made to improve the coordination between multi-layer circuit board manufacturers and systems manufacturers so that the mutual problems of these two groups will be thoroughly understood by each. When these problems are better understood, the systems design can be developed so that the multi-layer boards can be manufactured without undue process modification, which invariably seems to lead to fabrication difficulties. When this is done the multi-layer board should not continue as a production problem.

7. THE INTERCONNECTION BOND (EXTERNAL TO PACKAGE)

The problem of how to make the best type of interconnection bond has yet to be solved. It has been somewhat surprising to see the widely differing opinions on welding vs. soldering, for example. Radically differing opinions on this subject are expressed by reputable systems manufacturers.

It is our understanding that both Western Electric and RCA recently evaluated, for their own use, interconnections made with welding, soldering and by using wire-wrap techniques. The result of both of these programs was that each of the technologies proposed produced interconnections which were satisfactory for their intended uses. Care has to be exercised in accepting findings such as these and applying them to too wide a base. They may point, however, to the crux of the explanation -- that soldering, welding, and wire-wrap are all capable of producing satisfactory interconnection bonds. This may be the reason why there are such strongly differing opinions. It is possible to produce a very good bond by soldering and it is also possible to produce a very good bond by welding. Therefore the manufacturer that has had success over a number of years with soldering is apt to feel that, for his use, soldering is satisfactory and preferable. Similarly in the case of welding. Each manufacturer has a good reason for favoring the process which he has been using, but he obviously does not have adequate basis for condemning a process which he has

not used or worked with sufficiently to master.

There is no question but that welding is more difficult to master than soldering. Welding requires absolute control over the lead materials and over the processes used. Deviations in lead material are critical, and deviations in process are critical. One large systems manufacturer who is successfully using welding for his systems interconnections stated that nickel and kovar were used exclusively for welds, and that if any other materials were inadvertently obtained on the components they were using, defective welds would result.

A great deal of trouble with welding has undoubtedly been caused by a lack of understanding of the critical nature of the materials problem.

Those manufacturers favoring soldering stress the redundant nature of a soldered connection. The soldered joint is a large area connection especially when compared to a welded bond. They also stress the production characteristics of soldering which can handle literally thousands of connections in a single pass through a wave solderer or similar machine. For example, one systems manufacturer revealed that he could make 30,000 connections by batch soldering processes in less than 10 minutes. This was for a very successful aerospace binary machine which is well thought of in the industry.

With regard to welding, it appears that the welding machines

which have been available for making microcircuitry bonds have not been as satisfactory as the manufacturers may have hoped. Many of the successful users of the welding processes have modified the machines they have purchased to provide especially greater rigidity in the welding head. It is our understanding that the newer welding machines are now much more satisfactory.

There is a great deal to be learned about the techniques and processes involved in making the more common types of interconnection bonds. Conflicting reports are made about the utility and uniformity of practically all of the widely used bonding processes and one can only attribute this diversity to a difference in technique and, in part, to a lack of availability of basic information on the physics of interconnection bonds. For the most part, bonding technology has developed on an empirical basis and it would appear that some of the newer techniques have to be more completely defined. A survey was made of several groups who were investigating the physics of welding and who were attempting to more adequately define the important process variable. More work of this type should be done and, if a coordinated comprehensive program could be worked out, it would be much more effective than the several limited individual efforts now going on. More knowledge is obviously required to stabilize particularly the welding process. This is quite evident when those who are most successful with welding are using different approaches to the process technology.

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In the future continuing emphasis will be placed on the cost of the interconnections as well as on the technical excellence of the interconnections. It is obvious that if it can be shown, for example, that for a given application either welding or soldering would be adequate, the choice should and will be made on the basis of cost. Regardless of the application, there should never be the feeling that costs are unimportant -- costs are always important. Especially in the future the costs of micro-circuitized functions promise to become so low that all systems manufacturing costs will have to be accordingly minimized so that the user of the systems will be able to take full advantage of the cost reduction. This should be just as valid for NASA and Military applications as for commercial developments.

A concerted effort should be made to disseminate the knowledge that is available for the making of microcircuitry interconnections and for developing the basic theory to the point where adequate background data are available to establish dependable production techniques.

8.   THE CONNECTOR

The plug-in connector was originally developed to enable the modularizing of electronic equipment to minimize service difficulties particularly in the field. This led to the replacement of electronic modules in the field and their repair at suitably equipped depots. Such design, particularly for military applications, became routine and was expected. For this concept to be feasible, however, it is mandatory that the connector be considerably more reliable than the electronic modules being interconnected.

Most of the systems manufacturers surveyed are concerned about the reliability of miniature connectors when used in microcircuitized systems. The reliability of integrated circuitry is now so high that the connector appears more likely to fail than the circuitry. In other words, would there be any reason to design a microcircuitized system with plug-in modules if the servicing problems would be largely associated with the connectors? A substantial number of systems manufacturers appear to be going to permanently connected modules which could only be replaced by remaking either soldered or welded connections.

It would seem that insufficient thought is often given to connector design for microcircuitry modules. Catalog connectors are usually selected and, while such connectors are highly tooled and very reasonably priced, they may not be suited for the intended use.

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As with multi-layer interconnection boards, the systems manufacturer should work closely with the connector manufacturer in the selection, or development, of a high reliability connector for a microcircuitized electronic system. Again, close cooperation between the connector manufacturer and the systems manufacturer will enable the best possible answer to the plug-in connector requirement.

The physics of the reversible electrical contact also needs to be much better understood so that small pins can be used with assurance that the ultimate in reliability is being obtained. This is a very important area and one which should be pushed if connectors are going to be able to keep pace with the reliability requirements of microcircuitized systems.

9. THE SYSTEMS DESIGN

In the microcircuitized electronic system, the basic system mechanical design consists for the most part of suitably interconnecting flat packs, or TO-5 type cans, containing the integrated circuitry required. Numerous instances have been observed of similar systems designs being worked out by different groups each apparently working independently of the other.

From the standpoint of systems reliability, if for no other reason, it is important that as much of the presently available information as possible be used rather than undertake to develop assembly and interconnection methods which are only slightly different from ones already developed and thoroughly tested.

For example, there are manufacturers of multi-layer boards and manufacturers of semiconductor products who have highly developed the skills necessary to mount flat packs onto circuit boards by soldering and by welding. Use of these available technologies should be made before time and effort is expended to develop these processes all over again. By so doing, substantial development costs can be saved and better reliability information obtained.

It is becoming increasingly apparent that the wisest use of the talents of the systems manufacturer is to develop highly refined methods for using the low-cost integrated circuitry which is now available to him. Never before in the history of the

electronic industry has so much electronics been available for so little cost. For this reason the real challenge to the systems manufacturer is how he can use these available functions in his current and new equipment, and how he can expand his markets to cover new fields which are being made accessible to him because of the new low cost functions.

Since cost is now so important and since it is going to become more and more important in the future, the systems manufacturer should make increasingly wider use of the available techniques for assemblying his electronic systems. This is becoming more critical because the assembly costs are the high costs in the system. The systems manufacturer should not develop his own techniques unless by so doing he can achieve overall systems advantages which are worth the costs involved. This is an obvious statement, but more attention to this phase will be quite helpful to the systems manufacturer in minimizing systems development and manufacturing costs.

10. COMPONENT AND SYSTEMS RELIABILITY

During the survey of the MIT Instrumentation Laboratory, where the Apollo Guidance and Navigation Computer work is being conducted, the following information on reliability was obtained and is considered particularly pertinent.

In the guidance computer for the Apollo Project, 4100 circuit functions are used. For the purpose of standardization, and to enhance reliability, the circuit functions are all three-input NOR gates. These NOR gates are specified by NASA Specification 101-6771.

The initial computers for the Apollo Project were designed around the use of the three input NOR gates in TO-47 cans. Later design changes are based upon the use of flat packs, with two three-input NOR gates in each flat pack. The opinion was expressed that packaging was definitely improved by going from the TO-47 can to the flat pack. Other users have indicated similarly.

The MIT Apollo Guidance Computer is completely welded; this is one of the few groups surveyed who are welding their systems. One important reason given for the success with welding was that sufficient quantities of components were required for the Apollo work that lead material could be specified in every case. Nothing but nickel and Kovar leads are used throughout the system. MIT/IL indicated that only by this strict specifying of lead material could a reliable system be assembled by welding. This point of

complete material control was stressed as a prerequisite for welding. From this it can be concluded that many of the problems associated with welding are no doubt due to lack of materials control. It was also pointed out that only the substantial quantities involved in the Apollo work made such strict materials control practical.

The necessity for demonstrating reliability of a system, such as the Apollo computer, before field use was stressed by the Instrument Laboratory. This is a major problem, because the demonstration of reliability to the extent required for space and military applications requires the obtaining of many tens of millions of operating hours of element operation without failure. If large samples are not available, the time required to obtain the operating hours required exceeds the time after which the system, parts, and the parts processing become obsolete. For example, even a year (in the semiconductor field) is sufficient time to so change processes that reliability could be significantly affected.

To circumvent this time problem in making reliability checks, the following methods have been proposed:

. Use of Mathematical Models for Reliability Prediction

. Step Stressing

. Redundancy Techniques

. Reliability through Standardization

The efficiency of the Mathematical Model is obviously dependent upon the use of past data for the prediction of the operation of a future system. In a field which is changing as rapidly as the semiconductor field, the mathematical model technique is highly questionable. It does not appear that the generation of a useful mathematical model for the prediction of IC failure rates is promising, at least at this stage of the development of ICs. Even if such a model were developed in the future, the efficacy of the method would have to be demonstrated by life testing which, in itself, would require a stable period of several years in the development of IC manufacturing methods. When such a stable period will appear in the IC field is impossible to predict at this writing.

Step Stressing is a process for hopefully accelerating the aging process and, while it is sometimes helpful in other fields, it has been shown to be erroneous in predicting the life of ICs. Step Stressing must be followed by extended life testing to prove its accuracy; therefore, the main reason for the Step Test in the first place has largely been defeated.

The Redundancy Technique depends upon a knowledge of the various failure modes and the variation of failure modes among different parts suppliers to be successful. However, even assuming such information were known about ICs (and such information is not known), redundancy techniques sacrifice weight, power, size, and

increase the complexity of the system. In the case of ICs, not enough is known about the failure modes of <u>currently manufactured</u> functions to make the redundancy assumptions valid.

Standardization is a very effective method for improving reliability if for no other reason than that it minimizes the number of different components in any given system. This minimizing of the different numbers of components also minimizes the production line process control which effectively improves the reliability of the assembly process. Also, by using a minimum number of component types, the component numbers can be maximum for any given system which, in itself, helps in the evaluation of system reliability. The development of a reliable IC must be stressed, because no amount of design or assembly work will produce a reliable system if the basic ICs are not adequately reliable. Standardization helps to maintain the volume of individual components at a maximum and so aids in improvements in production techniques as well as in reliability evaluation.

Reliability depends upon vendor control over proven processes with rapid feedback to the vendor when new failure modes are detected.

Purchasing of large quantities of a part aids in the development and maintenance of high reliability. Purchasing of large quantities also results in lower prices which allow funds to be allocated to evaluation programs. Large volumes permit a continuous

production flow where manufacturing control is facilitated.

The Standardization approach, which is particularly adaptable to computers, has been demonstrated with the Polaris flight computer and extended with the integrated circuits used in the Apollo Guidance Computer. Both computers were designed to use a three-input NOR gate as the only logic element. All logic functions are generated by interconnecting the three-input NOR gates with no additional logic blocks of external passive components.

This is yet another instance where the use of a slightly increased number of functions permits the enhancing of other considerations which can be more important than just minimizing the number of functions. Another example of this was in the planar systems layout, where the number of interconnection layers was minimized at the cost of a small percentage of additional circuit functions. With the MIT work, the use of a small additional number of circuit elements enables the standardizing of the circuit function and the reduction of the function failure rate and element cost.

The following summary of integrated circuit failure modes detected to November 1964 has been reported by the MIT Instrumentation Laboratory:

    a. <u>Open Nail Head (or Ball) Bonds Using Gold Wires Making</u>

         <u>Contact to Aluminum Pads</u>. This open bond type of failure

was in some instances caused by the gold-aluminum eutectic formation known as "purple plague". These were traced to uncontrolled bonding procedures. The failures may be triggered by mechanical shock, thermal shock, acceleration, or vibration testing. "Purple plague" does not appear to be created during extended bakes at 200°C or less. Visual internal inspection often indicates that a weakened bond already exists in a bond which has failed and in which "purple plague" has been found to exist. This would corroborate the similar findings of the NASA Marshall Center.

Another cause of this type of failure is the poor adhesion of the aluminum film to the silicon dioxide. This failure is always triggered by mechanical stresses. This type of failure mode is a production process problem and can be cured by more careful process control.

Insufficient pressure or temperature (underbonding) is another cause of the ball-bond failures. This is usually caused by lack of adequate bond between the gold and the aluminum, a result of no real metallurgical bond between the gold and the aluminum. This type of failure is again the result of poor process control.

In some instances, a peripheral "purple plague" caused open circuits when the aluminum film was thin, or

when the bond was misplaced so that it did not make

contact to the proper portion of the bonding pad. This

again is a process control problem.

Overbonding (too much heat or pressure, or both)

also caused bond failures which usually resulted in the

pulling up of the aluminum and silicon dioxide. Only one

example of this failure mode was experienced by MIT.

b. Opens in the aluminum interconnects are normally caused

by the formation of hydrated alumina at the dissimilar

metal contacts in the presence of excessive moisture.

This failure mode, which can form at room temperature,

may be accelerated by baking.

It should be noted that opens in the aluminum inter-

connects can also be caused by electrical overheating

which usually results from the reduction of the cross

section of the interconnect by scratches or by other

defects in the deposition of the aluminum film and by

its subsequent etching.

c. Faulty oxide removal at the windows may cause the build

up of a dielectric layer between the silicon and the

aluminum film. This type of failure mode is difficult

to prove because the film can sometimes be broken down

by testing.

d. Bulk shorts due to secondary breakdowns are failure modes

which can usually be eliminated by proper specification of the electrical characteristics.

e. Chip scratching caused a base-to-base type of shorting which would permit the unit to pass most operational tests as well as operate in a ring oscillator circuit, and yet not perform properly in a computer circuit where logic operations are required.

f. Aluminum interconnect shorts to the silicon through the silicon dioxide have been detected. This is a voltage dependent failure mode and is attributed to the poor dielectric strength of the silicon dioxide. Pin holes, entrapped impurities, etc. cause weak SiO_2 dielectric.

g. Poor chip layout. Shorts have also been observed due to the bonds being made too close to the oxide edge because of poor chip layout. The remedy here is obvious.

h. Improper surface preparation can result in surface problems which result in the long term change in IC characteristics such as the degradation of gain and leakage currents under reverse bias. Better surface preparation will eliminate this type of long-term drift.

i. Cracked chips. The occasional failures due to cracked chips can usually be traced to strains which were set up in the die during the attaching process. Silicon-gold eutectic attachment procedures are preferable.

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j. Internal lead wires. Many types of shorts were caused by internal lead wires and the method of making contact from the aluminum pads on the chip surface to the posts of the package. Such shorts are always process problems which can be remedied by better chip and package layout or by more careful process controls.

k. Faulty handling, processing and bonding can cause opens to occur in lead wires. Nicks and cuts can cause opens during mechanical stressing. Another processing problem.

l. Loose material and particles within a package are always a potential cause of failures. The presence of free conducting material (extra length of leads which have been cut off, etc.) are the most troublesome cause of failures. Non-conducting particles can cause mechanical damage during vibration and shock testing.

We feel that the most significant part of this work is the use of circuit standardization as a means for minimizing system failure rates. The IC failure modes listed are process problems which all reputable manufacturers of ICs are striving to bring under better control and upon which progress will be made purely as a function of time and production diligence.

11. <u>MANAGEMENT CONSIDERATIONS</u>

Management personnel frequently do not have a full apprecia-
tion of the scope of the impact of microcircuitry on the production
of electronic systems for NASA, military and commercial uses.

Following is a brief resume of some facts concerning micro-
electronics which should be recognized by every person having the
responsibility for making management decisions affecting electronic
programs:

11.1 <u>Is microcircuitry readily available?</u>

Standard and special forms of microcircuitry are readily
available. There is far more than enough microcircuitry pro-
duction capacity in the United States for all of the systems
requirements in the foreseeable future. Any electronic system
can be designed with a full assurance that adequate production
capacity will be available regardless of the production volume
anticipated.

11.2 <u>Is microcircuitry expensive?</u>

Any standard form of microcircuitry is by far the least
expensive form of electronic packaging. Standard digital
functions for NASA and military-type environments can be
purchased for as low as $1.50 per chip to an average of less
than $10. for fully-housed units. Integrated circuit chips
for commercial uses are approaching 50¢.

No process for producing electronic circuitry has had

the low cost potential of the integrated circuit. In the
near future, multiple functions will be produced on a single
substrate for substantially the same cost as the single func-
tion currently is being produced. This is so because the
multiple function is produced by exactly the same number of
production steps as is the single function -- the only dif-
ference being the production yield. Yields are improving so
that today four functions on a single silicon chip cost only
20 percent more than one function on the same silicon chip.
The cost savings in microcircuitry are now substantial, but
these savings will increase very greatly with the advent of
multiple-function packaging in large electronic systems.

11.3 Is microelectronics reliable?

All tests have shown that microelectronics is by far
the most reliable form of electronic packaging ever developed.
In fact, microelectronic reliability has so increased that
the whole concept of plug-in replaceable modules is being
reevaluated.

While, at this writing, single microelectronic functions
are more reliable than their counterpart in any other form of
electronic assembly, the real breakthrough in reliability is
coming with the multiple-function chip which will be as
reliable as the single-function chip. This is so because of
the nature of the microelectronic failure modes which are in

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the interconnection areas rather than in the silicon chip
itself. Also, since the failure modes are in the inter-
connection area, these failure modes can be minimized by
careful in-line inspection and quality control. This is
currently being done, and the now very high reliability of
microcircuitry will be improved by orders-of-magnitude within
the relatively near future.

11.4 <u>Can any electronic problem be handled with microcircuitry?</u>

The state-of-the-art of microcircuitry is such that any
form of electronic system requirement can now be handled.
Low power applications, especially those of a computing
nature, are perhaps the ones most suitable for the applica-
tion of standard integrated circuitry. Power circuits can
best be handled by hybrid arrangements which combine the
characteristics of integrated circuits and thin film circuits,
and which can be coupled with high power devices, such as
silicon controlled rectifiers where very high output powers
are required. It is safe to state that there are applica-
tions for microcircuitry for any type of electronic system.
It would not be wise to ignore these possibilities.

11.5 <u>Should I make my own microcircuits?</u>

There is more than enough (by far) production and devel-
opmental capacity for microcircuitry in the United States.
It would not be economical to set up at this date to make

microcircuitry, even on the basis of becoming aware of the limitations of the various microcircuitry processes. There are far less expensive methods for becoming aware of the limitations of microcircuitry than by trying to produce microcircuitry in small quantities. The microcircuitry failure modes are such that they can only be adequately controlled and evaluated by well-established production procedures which emanate from lines handling substantial microcircuitry production. Microcircuitry yields can only be controlled adequately by carefully set-up production lines, with adequate inspection and control, and by handling large quantities which enable the lesser failure modes to be detected and controlled.

There has been a tendency in the past to set up in-house facilities just to keep abreast of the state-of-the-art. This is a very expensive method of staying abreast of the state-of-the-art and one which does not permit one to actually stay abreast because a small microcircuitry facility with inconsistent runs, and with low quantity production, is bound to be behind, particularly in the area of reliability where consistent high quantity runs are mandatory to train personnel and to permit inspection and process control facilities which are adequate. This factor alone can affect reliability by orders of magnitude.

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Other factors of a small in-house facility (yield, cost, capability, etc.) can be highly misleading.

11.6 <u>What is the most critical area of microcircuitry?</u>

There is no question but that the most critical area of microcircuitry is in the interconnections. The interconnection area is critical from the standpoint both of system reliability and cost. The major expense of any substantial microelectronic system is in the interconnection portion of the system, and much effort and attention must be given to this phase of system development. Many organizations are now using computer layout techniques to minimize the number of interconnection layers. Also, there is a trend toward considering the use of additional microelectronic circuit functions if, by so doing, the number of interconnection layers can be reduced. Multi-layer interconnection boards are more expensive than are the 10 - 20 percent additional circuit functions which at times can be used to reduce the layers in a multi-layer board or to eliminate it completely. This represents a new stage of thinking in systems layout - the minimizing of interconnection costs through the use of more circuitry. This would not have been a valid consideration with conventional electronic packaging. Integrated circuit functions are now so reasonable in cost, however, that a small additional quantity of circuit functions is

not a substantial expenditure and, if the interconnection costs can be lowered by using more circuit functions, there often can be an appreciable reduction in the overall systems costs.

11.7 <u>If I am to produce microcircuitized electronic systems, will I have to have a staff of microcircuitry experts?</u>

It now appears that it would be better of have competent systems personnel and to rely on the microcircuitry suppliers for technical excellence in the specifics of microcircuitry design. Overall management appreciation of the potentialities and general limitations of microcircuitry is essential, but the details of microcircuitry development and design can best be left with the semiconductor manufacturers who will be called on to supply the circuit functions. The systems manufacturer should develop his systems capability to the point where he can accurately specify the microelectronic functions he requires. He should not try to "expert" the microcircuitry phases.

11.8 <u>How can I be sure of getttng the best possible circuit functions?</u>

The technology for producing integrated circuits is now highly developed and there is no problem in getting highly reliable and economical functions from the well-established microelectronic manufacturers. There is very definitely a buyers' market in microelectronics, and every manufacturer is

doing all he can to properly service his accounts. Adequately

specifying what is required and procuring from established

vendors will assure getting the best possible circuit functions.

12. SURVEY PARTICIPATION

The wholehearted cooperation of government laboratories,

microcircuitry manufacturers, microcircuitry users, connector

manufacturers, university laboratories, non-profit organizations

and others is acknowledged. Without such assistance surveys of

this nature would not be possible.

Because of time limitations, it was not possible to visit

all of the numerous companies and laboratories that expressed a

willingness to participate. It is hoped, however, that such visits

can be scheduled as the study progresses.