NASA CONTRACTOR REPORT

NASA CR-398

LAMINATED FERRITE MEMORY

PHASE I

by R. Shahbender

Prepared under Contract No. NAS w-979 *by*
RADIO CORPORATION OF AMERICA
Princeton, N. J.
for

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION • WASHINGTON, D. C. • MARCH 1966

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ABSTRACT

This report describes the research performed for the period June 1, 1964 to May 30, 1965 in developing fabrication techniques to permit the assembly of a laminated ferrite stack of 4096 x 64 bits. For the assembled stack, a density in excess of 10^5 bits per cubic inch was demonstrated.

Test data on individual arrays indicate bipolar sense signals of 1.5 mV for drain currents under 50 mA.

Nuclear radiation studies conducted on ferrite samples indicate insignificant changes in magnetic and dielectric characteristics for dosages as high as 10^{19} nvt.

For MOS transistors, the radiation studies indicate carrier mobility changes for dosages of 10^{16} nvt. Other changes, related to metallurgical processing, were observed as a result of the high ambient temperatures in the testing reactor.

TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Continued)

LIST OF ILLUSTRATIONS (Continued)

LIST OF TABLES

I. INTRODUCTION

The limited capacity of random-access memories available in today's computing systems -- of the order of 10^6 bits -- severely limits the capability of these systems. For the commercial environment, economic considerations primarily limit the capacity of core stores, the most widely used form.[1] With the recent introduction of novel electronic selection schemes and the adoption of simplified core wiring and stacking, capacities in excess of 10^7 bits have become economically feasible.[2]

For space and military environments, the maximum usable core capacity is determined by considerations other than economics. Size, weight, power consumption, reliability, etc., are, in general, more important than the exact cost per bit. A number of devices in addition to ferrite cores are under intensive development for space and military environments.

Laminated ferrite memory stacks[3] operated with integrated Metal-Oxide-Semiconductor (MOS) transistor[4] circuits are eminently suited to a space or military environment. The memory stacks, as described in this report, offer bit densities unmatched by other techniques. Operation with low drive currents (low power) yields relatively high sense signals. The combination of low drive power and high output is essential for the successful use of integrated semiconductor circuits.

Integrating laminated ferrite stacks with integrated MOS circuits is expected to yield a memory system with a capacity in excess of 10^7 bits operating at a few microseconds cycle time. Low power, small size, tolerance to severe environments, as well as low bit cost, will be attained by these systems. This follows from the already well-established characteristics of ferrite cores[5] coupled with the results achieved on this program. However, continued research and development, especially in the area of integrated MOS circuits, is required to attain these desirable characteristics.

Briefly, a laminated ferrite array is a monolithic sheet of ferrite with an embedded matrix of conductors fabricated by a batch process. The embedded conductors form two sets of insulated, mutually orthogonal windings. Operation is in a word-organized mode with one set of windings used for read-write energization, and the other set for the sense digit function.

An MOS transistor is formed by diffusing and metallizing two isolated n-type regions in a p-type crystal to form the source and drain electrodes. An oxide layer is formed on the crystal surface between the source and drain regions and a metal layer, the gate electrode, is deposited on top of the oxide. These transistors can be fabricated as integrated arrays and can be used either for switching applications or as amplifying units. Further, complementary types (p-regions diffused in n-crystals) can also be fabricated.

Preliminary estimates indicate that a random access memory system with the following characteristics specified may be realized by integrating laminated arrays with integrated MOS circuits.

Memory Capacity	1.3×10^7 bits
Number of words	65,536
Number of bits per word	200
Ferrite stack bit density	10^4 bits per square inch 2×10^5 bits per cubic inch
Ferrite stack volume	65 cubic inches
Memory system volume (Ferrite stack and electronics)	130 cubic inches
Memory system weight	15 lbs.
Average power consumption for a 2-μsec random access cycle	100 watts

For the above-specified memory, the equivalent serial information rate is 10^8 bits/second. Reducing the equivalent serial information rate reduces the power consumption. For a maximum rate of 10^6 bits/second, the estimated average power consumption is less than 10 watts.

For a number of projected space applications, the use of associative memory techniques results in important system advantages. A magnetic associative memory is attractive for such applications since it can store information indefinitely without the expenditure of standby power.

The realization of a magnetic associative memory requires a magnetic nondestructive readout (NDRO) storage element. Feasibility of such an element in laminated ferrite arrays has been demonstrated at RCA Laboratories as part of the company-funded research. A magnetic associative memory requires a considerable amount of electronic circuitry. Economic feasibility of such systems hinges on the use of integrated circuits.

Combining integrated MOS circuits with laminated ferrite NDRO arrays may well be the optimum solution to the realization of associative memories for space applications.

The scope of the present R and D program is to develop the ferrite technology to permit the fabrication of an operable memory stack of 4096 words, and to determine the damage effects produced by nuclear radiation for both the ferrites and semiconductors to be used in the memory. The progress accomplished in the fourth quarter, together with that of the first three quarters, is described in the following sections.

The work described in this report was pursued at RCA Laboratories, Princeton, New Jersey, in the Computer Research Laboratory under the general supervision of Dr. Jan A. Rajchman. Dr. Rabah Shahbender was the Project Engineer. The following members of the RCA Laboratories' staff contributed to the program: Dr. Wolfram Bosenberg, Mr. Stuart Hotchkiss, Dr. Anthony Robbi, Dr. Rabah Shahbender, Mr. James Tuska, Mr. Joseph Walentine, and Mr. Chandler Wentworth.

II. ARRAY FABRICATION

A. FABRICATION TECHNOLOGY

The basic operations involved in the fabrication of a laminated memory array are[6]:

1. Ferrite powder preparation
2. Doctor blading of ferrite sheets
3. Conductor fabrication
4. Laminating and sintering of memory arrays

1. Ferrite Powder Preparation

The metal oxides, carbonates, or other compounds, which are to form the ferrite by a solid-state reaction, are mixed homogeneously and wet-milled in a steel ball mill. The dried powder is pressed into cakes and prefired at a temperature between 1000°C and 1100°C to bring about the initial chemical reaction between constituents. To produce a chemically homogeneous sample, the prefired powder is again intensively milled and mixed. This powder, after the addition of a binder, is formed into a slurry by suspending it in a volatile solvent.

Conventionally, the prefired powder is dry pressed into cores after the addition of the binder. The pressed cores which are in the "green" state, i.e., unsintered state, are sintered to form the finished product.

2. Doctor Blading of Ferrite Sheets

The ferrite slurry is used to prepare sheets of green ferrite by the "doctor blading" technique. In this technique the slurry is spread in an even layer on a glass substrate by the sweeping action of a blade (called a "doctor blade") held at a constant distance above the glass surface, as shown in Fig. 1. The bladed slurry is air-dried, at which time the solvent evaporates, resulting in a sheet of green ferrite on the glass surface. The ferrite particles in the sheets are held firmly together by the binder. After drying, the sheet is easily peeled from the glass surface.

The distance of the blade from the glass surface, which is accurately set by means of a micrometer attached to the blade, is nominally adjusted to 5 to 7 times the desired thickness of the green ferrite sheet. The ratio of the blade height to green sheet thickness is determined by a number of factors, the most important of which are:

1. Amount of solvent and binder used in the slurry.
2. Ferrite powder particle size
3. Desired sheet thickness

3. Conductor Fabrication

Conductors are formed as an integral part of a green ferrite sheet by means of a modified "silk screening" process. A photoformed metal mask is

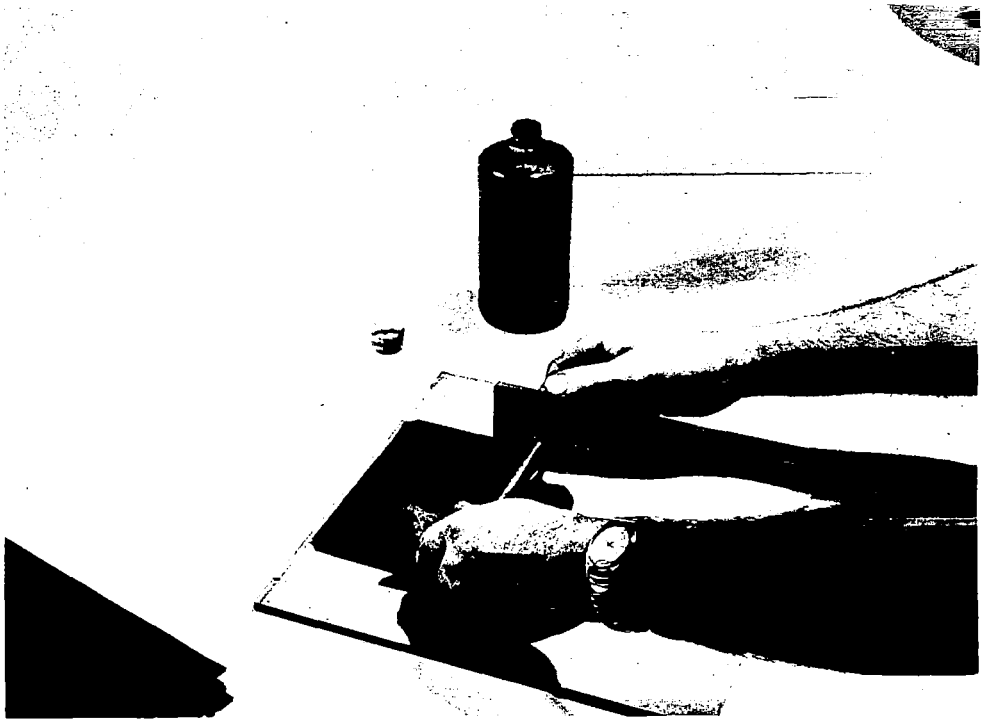


Fig. 1. Doctor blading of ferrite sheets.

laid on a glass substrate and a paste consisting of the required metal powder and a binder is squeegeed through the mask onto the glass substrate. The mask is removed leaving a conductor pattern on the glass. A ferrite slurry is next doctor bladed over the conductor pattern and allowed to dry. On peeling, the ferrite sheet retains the conductor intimately embedded in it and flush with its surface.

The photoformed masks are made from commercial grade beryllium-copper. This is coated with KPR (Kodak photoresist) and exposed through a photomaster according to well-established photoforming techniques. The mask is etched in a ferric-chloride bath.

The conductor materials employed are basically the refractory metals, such as platinum, palladium, rhodium, iridium, and gold. Alloys of these metals and mixtures have also been tried as described later.

4. Laminating and Sintering of Memory Arrays

A memory array, such as the 256-bit plane shown schematically in Fig. 2, is fabricated by laminating together and sintering three sheets of green ferrite in the order shown in Fig. 3. The top and bottom sheets, with a green thickness of 2.5 mils contain conductors spaced 12 mils apart. The center sheet is 0.5 mil thick and contains no conductors.

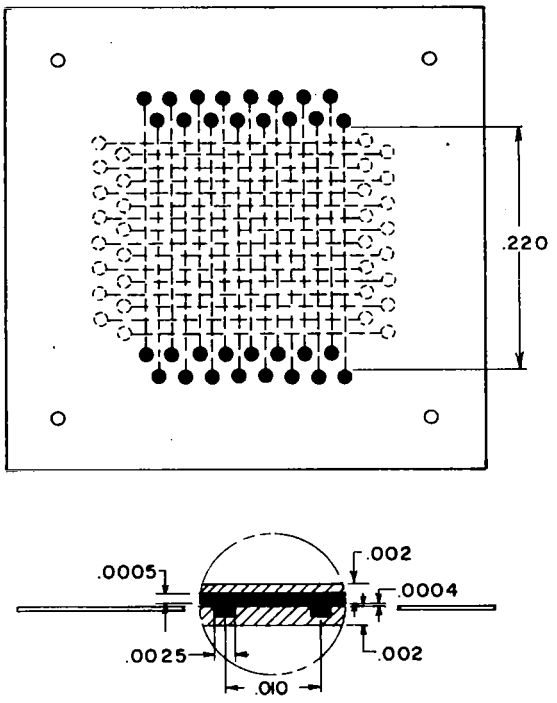


Fig. 2. Laminated array structure.

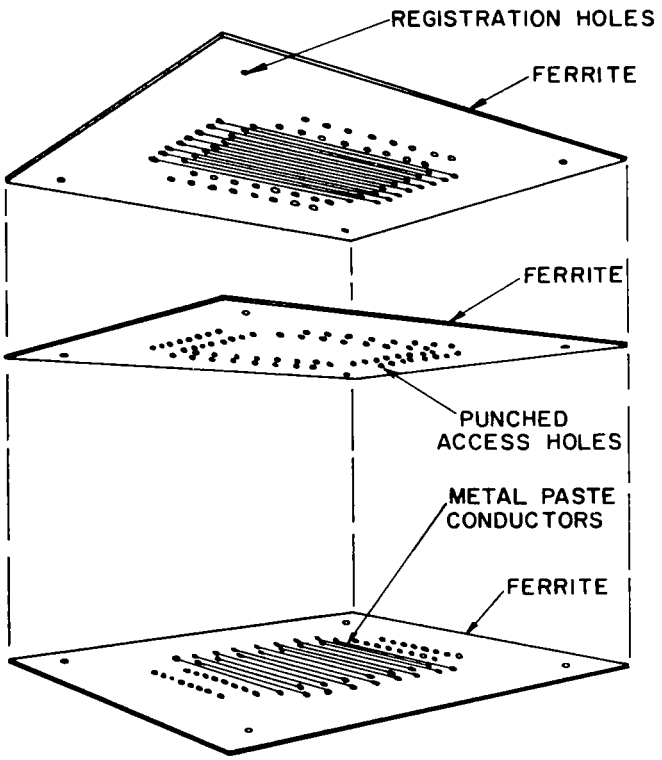


Fig. 3. Laminate details.

Laminating is accomplished by pressing the green sheets together at moderate pressures and temperatures (1000 psi and 100°C, respectively). The ferrite sheets are sandwiched between two optically flat, polished aluminum blocks, which are placed between the heated platens of a hydraulic press. Pressure is applied for a few minutes after the temperature of the blocks, as monitored by a thermocouple, has stabilized. The laminated sheets are next sintered in a controlled temperature furnace.

Following sintering, the laminates are air-quenched to produce the required magnetic characteristics. Experimental data indicated that quenching results in excessive mechanical distortion of the laminates as well as internal stresses which affected the magnetic performance. To alleviate these problems a nitrogen-annealing procedure following sintering was adopted. A gas-tight quartz muffle is used in the nitrogen-annealing furnace to control the atmosphere during annealing. Considerable improvements were achieved in both the magnetic and mechanical characteristics of fabricated sample planes.

On sintering, a ferrite laminate shrinks by approximately 20% in linear dimensions. The embedded conductors likewise sinter and shrink. The shrinkage of the embedded conductors is determined primarily by the binder content of the paste. Excessively high binder content results in porous, high-resistance conductors, whereas insufficient binder causes the ferrite laminate to crack as a result of unequal shrinkage.

B. KILO-BIT ARRAYS

To effectively achieve bit capacities in excess of 10^7, it is anticipated that individual laminated arrays containing thousands of bits as an integral unit must be used to form a stack. The fabrication technology described above was used to produce experimental memory arrays with conductors spaced 10 mils apart and having the number of crossovers indicated below:

1. 16 x 16
2. 256 x 64
3. 256 x 100
4. 512 x 200
5. 1024 x 200

The smaller planes (16 x 16) were mainly used to determine the effect of fabrication parameters on magnetic characteristics. Planes with 256 x 64 crossovers were used to obtain most of the data presented in this report. Several hundred planes were fabricated and 16 of these were assembled into a 4096-word stack. A number of planes with 256 x 100 crossovers were also fabricated. These, as expected, showed the same characteristics as the 256 x 64 planes.

To investigate the feasibility of fabricating larger sized arrays, a few sample planes, each containing 512 x 200 crossovers, were produced. These had mechanical characteristics similar to the 256 x 64 planes. Magnetic testing of these planes was not attempted. A few sample planes, each containing 1024 x 200 crossovers, were also fabricated. Difficulties were encountered in producing these arrays as a result of temperature gradients in the sintering furnace.

Mechanically, the samples were not as good as the 256 x 64 planes. Magnetic testing was not attempted.

The data obtained indicate that fabrication of planes with 256 x 100 crossovers or 512 x 200 crossovers is feasible and practical. The sintering and handling of the large arrays necessarily requires care but is not unduly difficult or complicated.

Figure 4 is a magnified radiograph of a 256 x 64-bit plane, and Fig. 5 is a partial cross section showing the embedded conductors. The overall dimensions of the shown laminate are: 2.94 x 0.84 x 0.005 inches. The conductor spacing in both lateral directions is nominally 10 mils, and the conductor cross-sectional dimensions (Fig. 5) are approximately 2.5 x 0.7 mils.

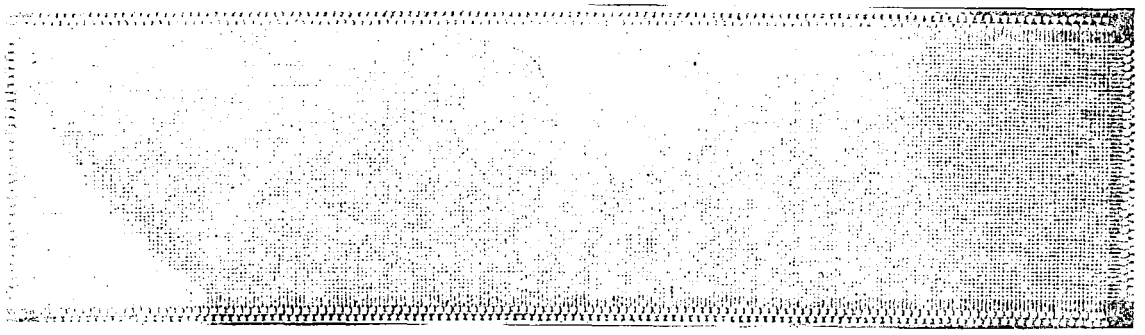


Fig. 4. Magnified radiograph of a 256 × 64-bit plane.

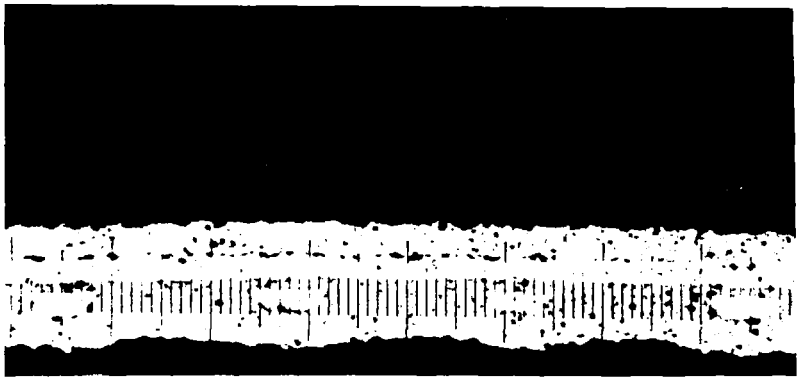


Fig. 5. Partial cross section showing the embedded conductors in the 256 × 64-bit plane.

Sample planes containing 64 x 64 crossovers were obtained from RCA Ferrite Memory Operations, Needham Heights, Mass., and were used for the preliminary investigations of stacking and interconnecting techniques. For these planes, the conductor spacing is 15 mils, and the conductor cross-sectional dimensions are approximately 5 x 1 mils.

C. CONDUCTOR MATERIAL INVESTIGATIONS

Various metals and alloys[7,8] beside platinum were considered for use as embedded conductors in the laminates in an effort to reduce the winding resistance. For the word windings, reduction of the resistance is of secondary importance since the back voltage is predominantly due to flux-switching rather than resistive drops. On the other hand, the attenuation of the sense signal is largely due to the resistance of the sense digit windings. Thus, a reduction in this resistance permits sensing of larger memory blocks. Table I lists the metals that were tried as embedded conductors and gives the resistivity and melting temperatures. Other metals, e.g., silver or copper, are known to interact with ferrites and were not tried. The results obtained with the metals listed in Table I, their alloys and mixtures, are summarized below.

TABLE I

CONDUCTOR MATERIAL CHARACTERISTICS

Material	Resistivity ($\mu\Omega$-cm)	Melting Temp. (°C)
Platinum	11	1773.5
Palladium	10	1555
Rhodium	5	1966
Gold	2.4	1063
Iridium	5.3	2454
Aluminum	2.7	660.2

Platinum: The data show that platinum may be safely used. It does not interact with the ferrite and does not oxidize during sintering. The paste conductors sinter with the ferrite and yield a resistance of approximately 3 Ω/inch length for a conductor cross section of 2.5 x 1.5 mils.

Palladium: The metal forms an oxide that is unstable at temperatures above 600°C. The oxide is very tenacious. Palladium is very similar to platinum and yields the same resistance values.

Rhodium: Extensive testing indicated that rhodium conductors have a deleterious effect on the magnetic characteristics of ferrite laminates. The main effect is a loss of squareness in the hysteresis characteristic. This was confirmed for two different ferrite compositions. Embedded rhodium paste conductors sintered with the ferrite and yielded resistance values of approximately 1.5 Ω/inch length. A relatively tenacious oxide film formed on the surface of the conductors.

Gold: The low resistivity and freedom from oxidation obviously make gold a suitable conductor material. A great deal of effort was spent in attempting to utilize gold for conductors. For either paste conductors, or solid wires embedded in ferrite, open circuits develop in the conductors at the melting temperature of gold. The conductors remain open as the temperature is raised to the final sintering temperature. They do not re-form into continuous strips after the sample is cooled. The above was determined by monitoring the resistance of embedded gold conductors during sintering. Radiographs of sample planes show a "balling up" of the gold within the sample. Samples partially sintered at temperatures below the melting point of gold and, hence, without the desired magnetic characteristics, had continuous conductors. Thus, the possibility exists of alloying gold to raise its melting point or developing sintering schedules at temperatures below the melting point of gold.

By selecting sections of ferrite containing usable lengths of continuous conductors, it was found that gold does not interact with the ferrite and has no deleterious effects on the magnetic characteristics. Resistance measurements indicate values under 0.5 Ω/inch length.

Iridium: The metal is mechanically strong as compared with platinum which is soft and ductile. As a result, paste conductors of usable density cause the ferrite laminates to crack and distort. Increasing the thickness of the laminates alleviates the difficulty. The material does not seem to interact with the ferrite and yields conductors with a resistance of 1.5 Ω/inch length.

Aluminum: Solid aluminum wires of 5-mil diameter embedded in ferrite completely oxidized on firing. It was assumed that an oxide film would form on the conductor surface which would prevent further oxidation of the wires or interaction with the ferrite. This was not the case and aluminum may not be used.

Gold Alloys: Gold forms an alloy with any percentage (0 to 100 percent) of platinum, palladium, and rhodium. The melting point of any of these alloys can be made higher than the sintering temperature of the ferrite. However, the resistivity of the alloys with sufficiently high melting point is slightly less than that of the pure refractory metal, i.e., platinum, palladium, or rhodium. A gold-palladium alloy of (90-10 percent) composition was used to form foil conductors that were next embedded in a laminate. The resistivity of the alloy is 7 μΩ-cm and the conductor resistance as measured in the ferrite correlated with it. Paste conductors made with gold-palladium powders of (95-5 percent) composition were attempted. For this composition, the melting point is slightly lower than the ferrite sintering temperature. The conductors melted and did not re-form continuously as can be seen in the radiograph of Fig. 6.

Gold-Iridium: Gold will alloy with only a few tenths of a percent of iridium. The alloy has a melting temperature that is lower than the sintering temperature of the ferrite. Figures 7 and 8 are radiographs of samples containing foil conductors made from ingots of gold - 0.1 percent iridium, and gold - 2.5 percent iridium, respectively. The conductors melted during sintering and re-formed discontinuously as can be seen in the figures.

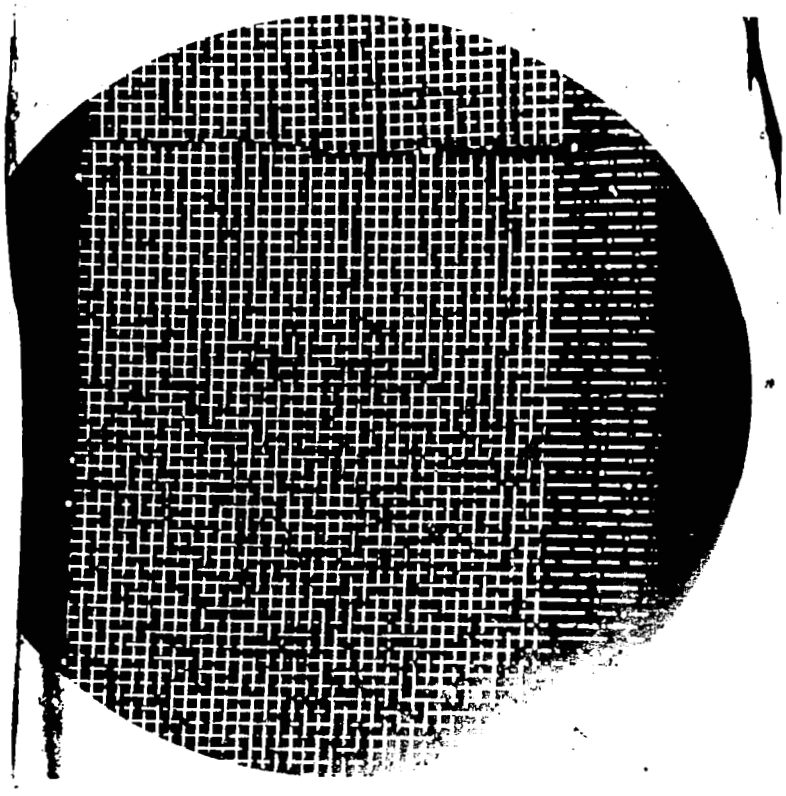


Fig. 6. Magnified radiograph of Au-Pd conductors.

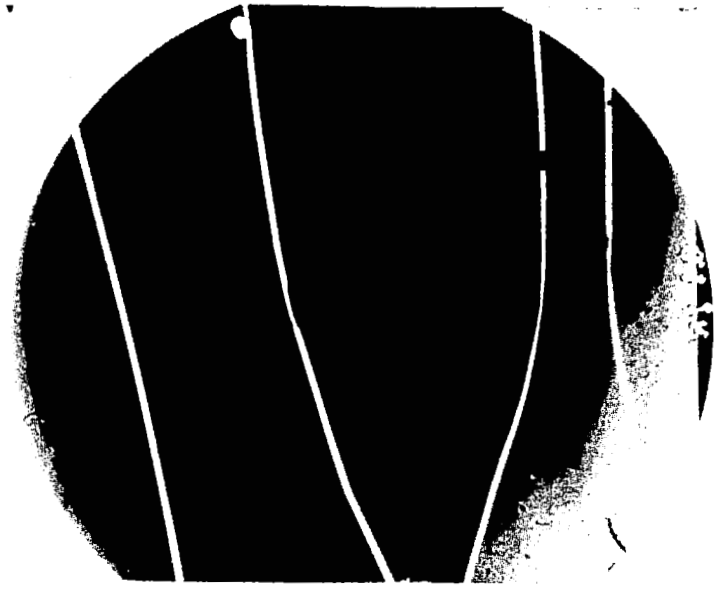


Fig. 7. Radiograph of laminated conductors. Alloy: Gold – 0.1% iridium.

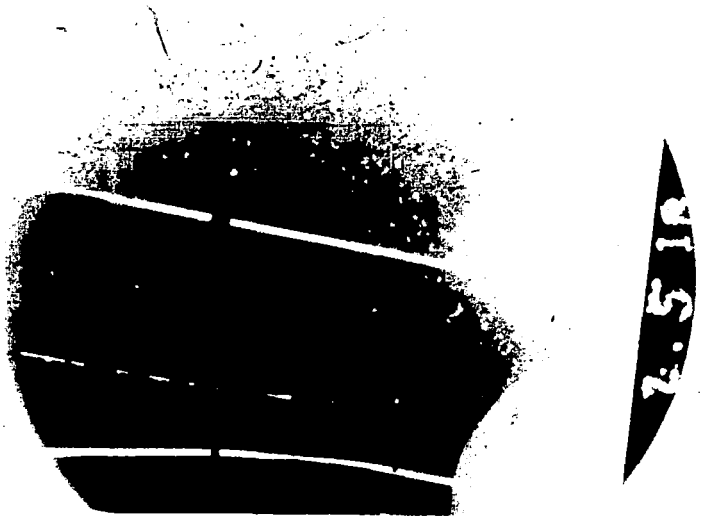


Fig. 8. Radiograph of laminated conductors. Alloy: Gold – 2.5% iridium.

Paste conductors made with gold-iridium powders of (50-50) percent composition and (25-75) percent composition appear to have the desired characteristics. The conductors are continuous for both of the above compositions and exhibit a resistance of under 1 Ω/inch length. The effect of these compositions on the magnetic characteristics of the ferrite has not been completely tested. However, the data available indicate an increase in coercive force. Ferrite cracking and warping has not been observed for both compositions. Additional effort is required to determine the optimum composition and suitable methods for forming the combined powder paste.

For the 4096-word stack described later, platinum conductors were used exclusively. This was necessary to insure an adequate number of laminates for stack assembly.

III. STACK ASSEMBLY AND CONNECTIONS

Utilization of laminated ferrite planes in the construction of a mass memory hinges on developing stacking and mass interconnecting techniques. Interconnecting the planes to one another to form a stack and interconnecting the stack to integrated semiconductor circuitry must be accomplished. Obviously, both stack assembly and mass interconnections are simplified, if the overall mechanical dimensions and conductor spacings are reproducible from sample to sample. The work performed and the results achieved in assembling a 4096-word stack are described in this section.

A. DIMENSIONAL MEASUREMENTS ON 256 x 64 SAMPLE PLANES

A measurement program was undertaken to determine the uniformity and reproducibility of laminate dimensions and conductor spacings. The measurements were restricted to planes having 256 x 64 crossovers. To reduce the labor involved, the spacing of every tenth conductor (of the 256 conductors) was measured using an optical comparator. The spacings were measured on both edges of the laminate which were arbitrarily labeled A and B.

In one series of experiments, the conductor spacings were measured after each step in the fabrication process.[6] Dimensional changes occurred as a result of the mechanical handling of the ferrite sheets. The predominant change occurred, as was expected, following sintering of the laminate.

Nonuniform shrinkage in the lateral dimensions of a laminate lead to distortion and nonuniform conductor spacing. Deviation of a conductor from its desired position is defined as the cumulative error (computed as the measured distance between a conductor and a reference point minus the computed distance of the same conductor from the reference point assuming a standard conductor spacing). Figure 9 is a plot of the cumulative error for both edges of a sample plane[7] assuming a standard conductor spacing of 10.26 mils. Points of maximum deviation, i.e., points at which the cumulative error has maximum magnitude, are indicated in Fig. 9 and occur at different locations for the two sample edges.

In a series of eleven sample planes, identified as the second-numbered series, the sintering conditions were closely controlled in an effort to reproduce mechanical dimensions.[8] The planes were quenched following sintering. The mechanical tolerances and uniformity for this series of planes is considerably better than had been previously accomplished. Table II gives the maximum cumulative errors and their locations for the 22 sample edges. The largest error is 27 mils (edge 26B). This is a tolerance of approximately 1%. The tolerance for four of the samples is 0.4 percent or better in both sample edges. A histogram of the average spacing between adjacent word conductors for the eleven samples is shown in Fig. 10. Both edges of each sample are measured, resulting in two bars for each sample.

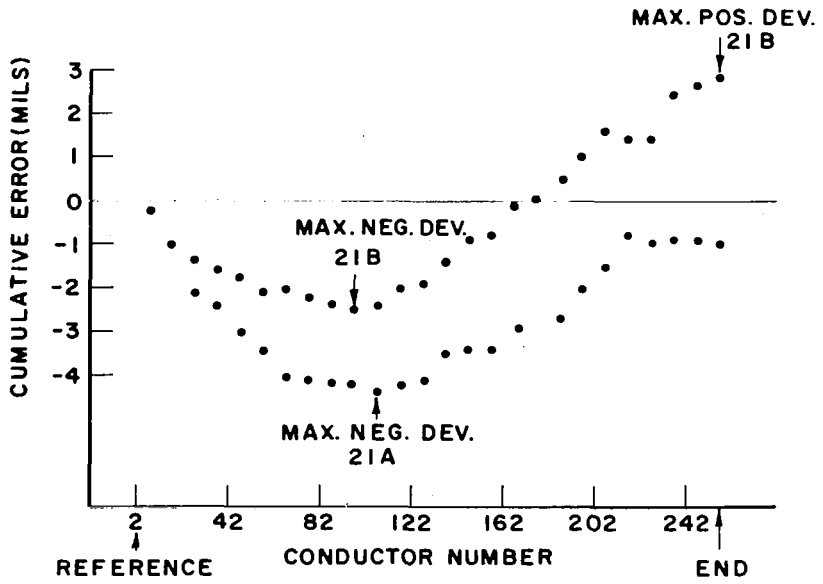


Fig. 9. Maximum deviations from standard vs. conductor location in Sample 21.

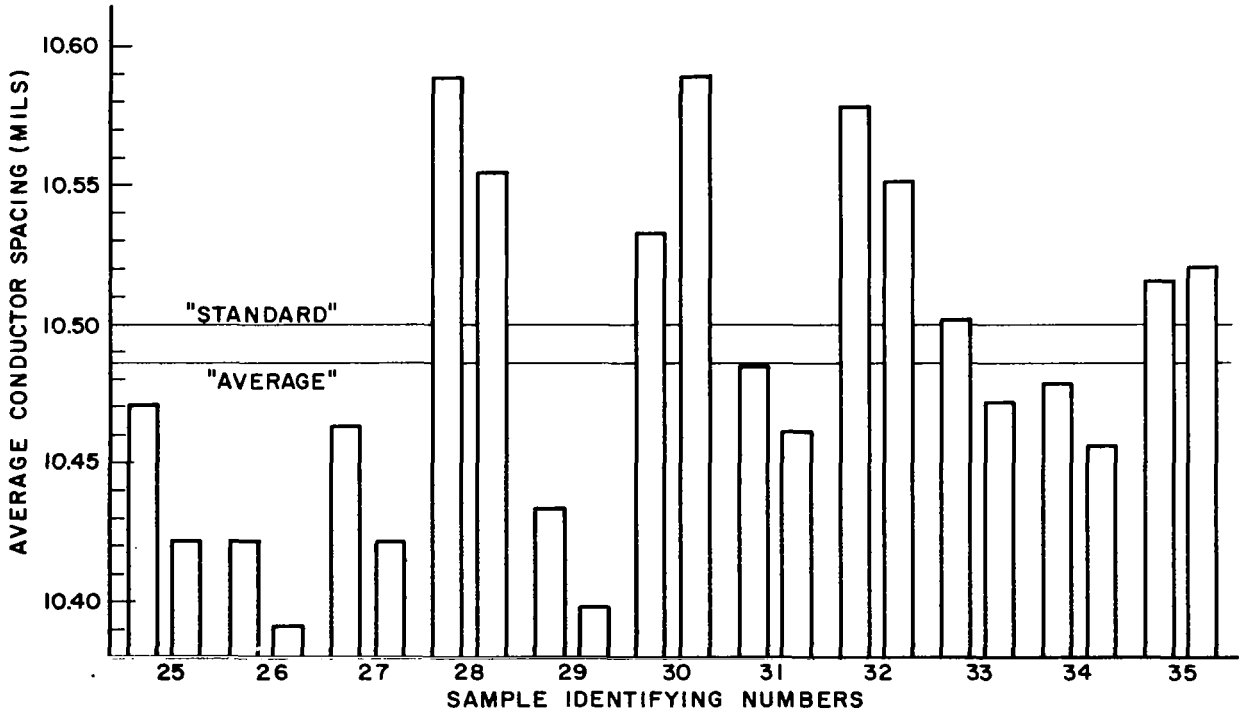


Fig. 10. Histogram of average conductor spacings for eleven sample planes (second-numbered series).

TABLE II

MAXIMUM CUMULATIVE ERRORS AND THEIR LOCATIONS IN SECOND-NUMBERED SERIES SAMPLES (BOTH EDGES)

Sample Number	Maximum Pos. Deviation	Conductor Number	Maximum Neg. Deviation	Conductor Number
25A	4.4	102	7.3	END
25B	0.2	10	19.5	END
26A	0.7	22	19.5	END
26B	---	---	27.0	END
27A	1.5	32	9.0	END
27B	0.3	32	19.8	END
28A	24.2	212	---	---
28B	17.8	212	---	---
29A	---	---	16.4	END
29B	---	---	25.6	END
30A	8.2	END	---	---
30B	22.2*	END	---	---
31A	1.9	22	3.8	END
31B	---	---	9.6	END
32A	19.5	END	---	---
32B	13.0	END	---	---
33A	1.2	52	0.3	172
33B	---	---	7.0	END
34A	0.4	12	8.2	142
34B	---	---	10.6	END
35A	5.6	202	---	---
35B	5.6	END	---	---

* This edge "hung up" on the setter plate during sintering.

The achievement of even better tolerances requires closer control over all the fabrication steps, particularly the sintering process and the density of the doctor-bladed sheet. Nitrogen-annealing of sample planes resulted in improved flatness and linearity. However, conductor spacing reproducibility and uniformity has not been measured on nitrogen-annealed sample planes.

B. STACK ASSEMBLY

After a study of factors involved in packaging, it was decided to position laminated ferrite planes in a surface-to-surface configuration rather than an edge-to-edge arrangement. Such a design permits maximum density with the most convenient inter- and intraconnection techniques. To approach an optimum reliability factor, a maximum of eight planes would be grouped in an individual substack with initial efforts directed to the use of only four planes per substack. Consequently, four substacks of four planes each could provide 262,144 bits in the interconnected stack (4096 words of 64 bits).

1. Packaging

Packaging considerations were evaluated -- keeping in mind inter- and intraconnections, a necessary relationship in dealing with an integrated type of assembly. Interconnections are connections between substacks, and intraconnections are connections within a given substack.

Early in the program, relatively uniform mechanical specimens approximately one inch square and containing 64 x 64 orthogonal conductor arrays were used. These were obtained from the RCA Ferrite Memory Operation, Needham Heights, Mass. A specially designed frame, molded from castable epoxy* was made such that one laminate per frame would be used and four such subassemblies would constitute a stack.[7] The frames were made to physically interlock, and the laminates were isolated by thin silicone rubber** gaskets. Samples of this technique are shown in Figs. 11 through 14, and the overall schematic is seen in Fig. 15. Although several stacks were fabricated in this manner, the difficulties in fabrication together with the very poor mechanical strength thus obtained, resulted in an investigation of a second packaging method.

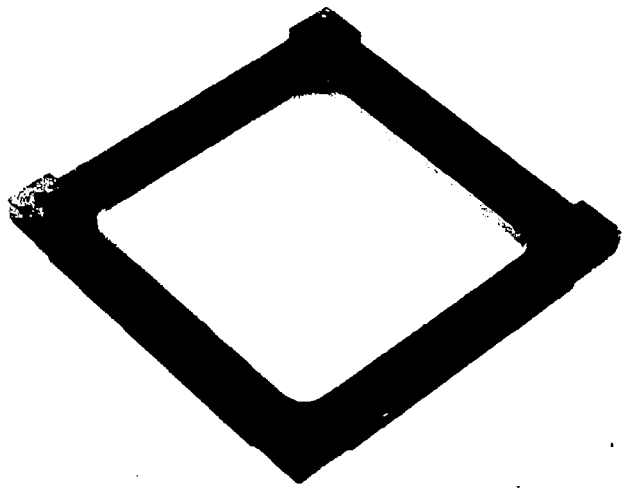


Fig. 11. Frame as cast.

* Stycast 2651-40, black epoxy, Emerson and Cuming, Inc., Canton, Mass.

** RTV-11 Room Temperature Vulcanizing Silicone Rubber, General Electric Company, Silicone Products Dept., Waterford, New York.

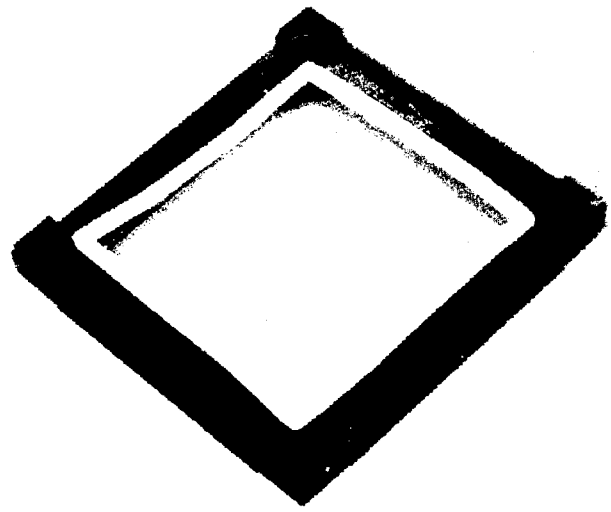


Fig. 12. Frame with gasket partially in place.

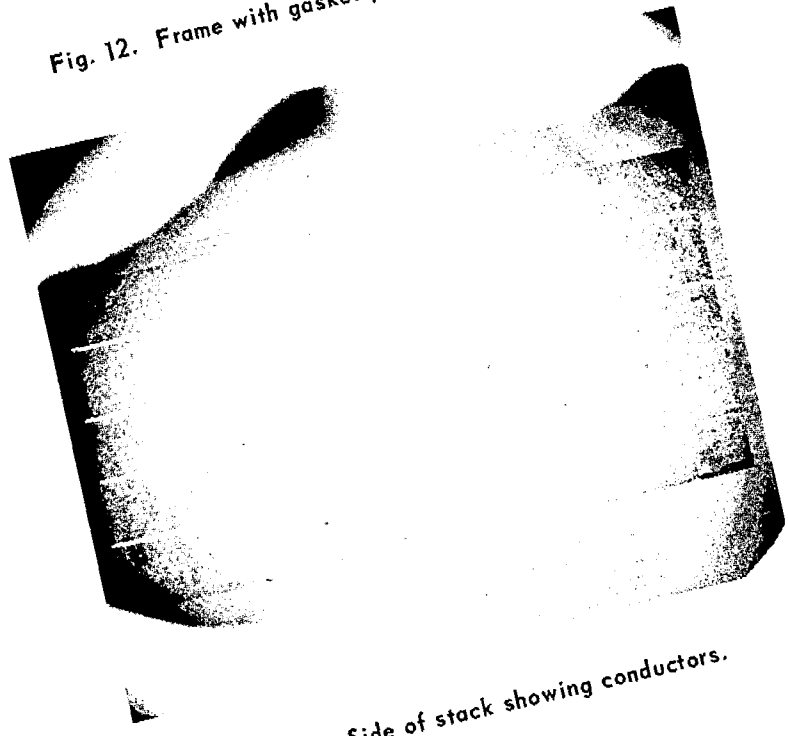
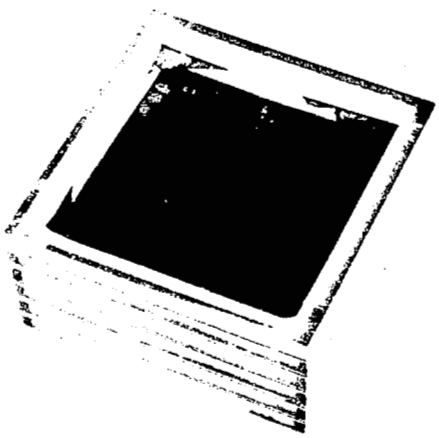
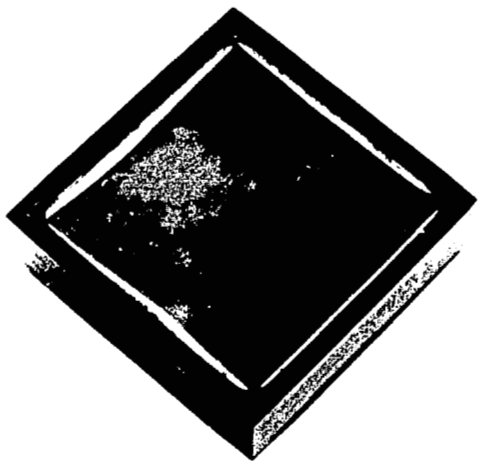


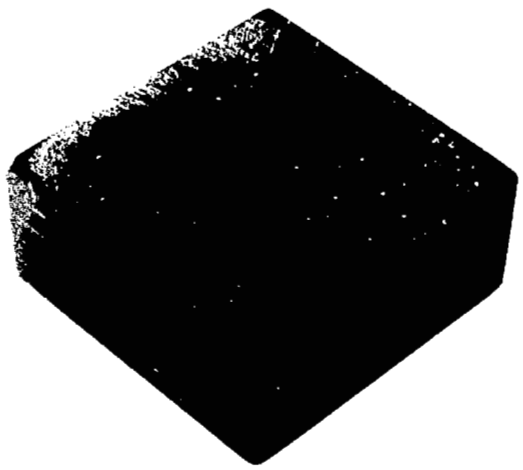
Fig. 13. Side of stack showing conductors.



EARLY STACK WITH PORTIONS OF TOPMOST FERRITE REMOVED



LATER STACK WITH EXPOSED PLANE



ENCLOSED STACK WITH POLISHED SIDES SHOWING CONDUCTORS

Fig. 14. Typical 4- and 5-plane stacks.

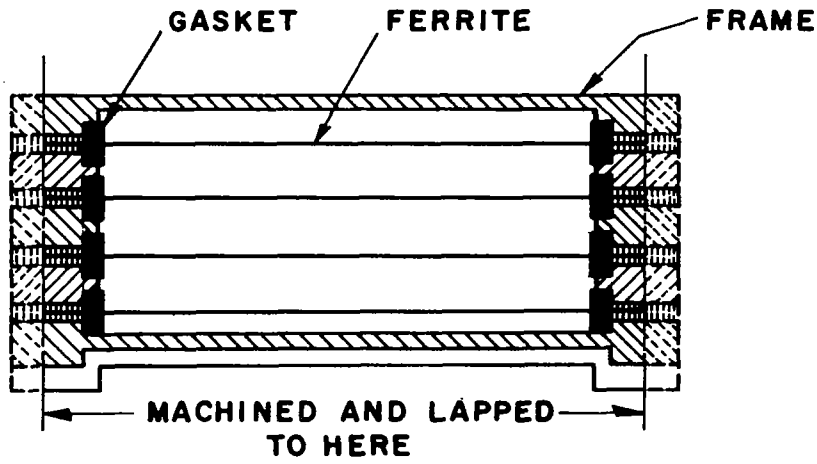


Fig. 15. Cross section of 4-plane stack.

A silicone rubber mold reinforced with aluminum[8] was made which would permit casting a completely epoxy-filled rectangular solid stack configuration. Parts of this mold and a finished 4-plane stack are shown in Figs. 16 and 17. The epoxy used is Emerson and Cuming, Inc., Stycast 2651-40-white with 4% by weight of Stycast 2651-40-blue added. Emerson and Cuming 24LV catalyst is added to the mixture (18% by weight) to produce a sufficiently low viscosity to permit pouring. Room temperature (23°C) curing for approximately 16 hours is recommended for complete dimensional stabilization. Dimensional measurements made on a block cast in a Teflon mold indicate a shrinkage of 10^{-4} inches per inch after a 48-hour cure.

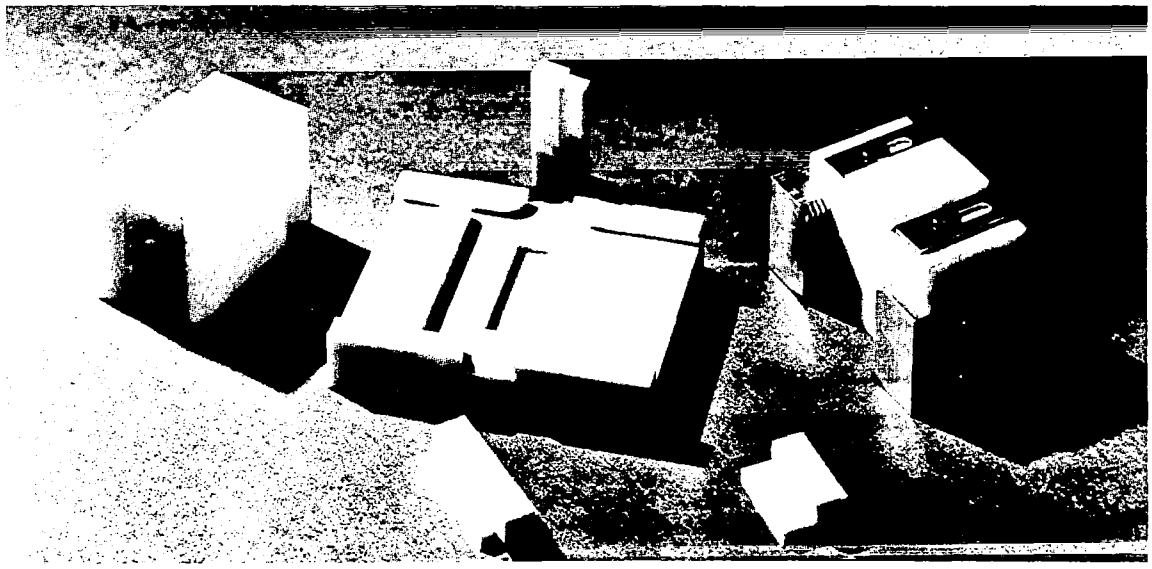


Fig. 16. Separate parts of assembly jig.

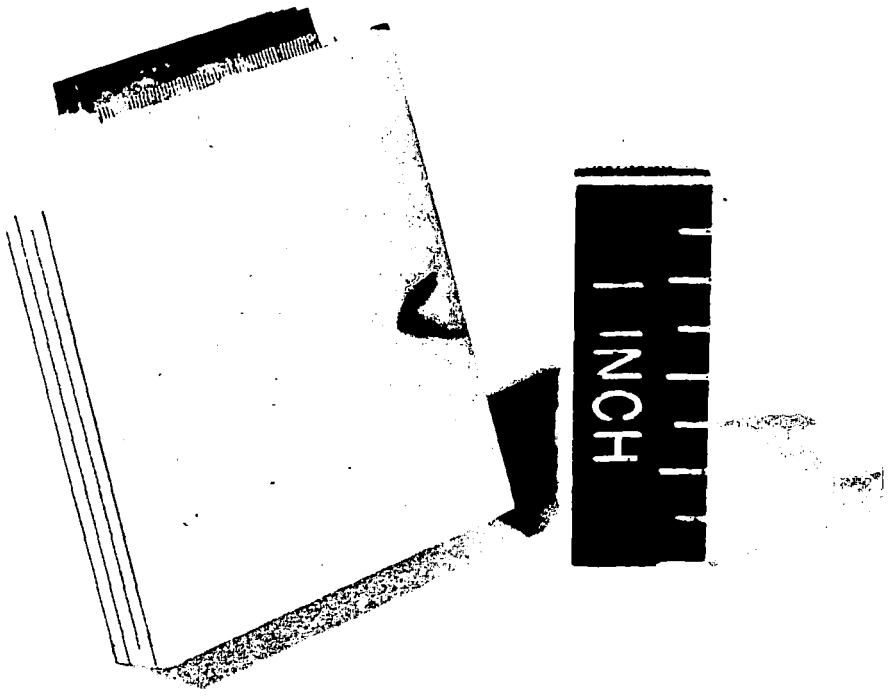


Fig. 17. Block with ground sides.

A strip of chemically milled copper conductors is soldered to one edge of each plane in this stack as a first effort toward inter- or intraconnection.

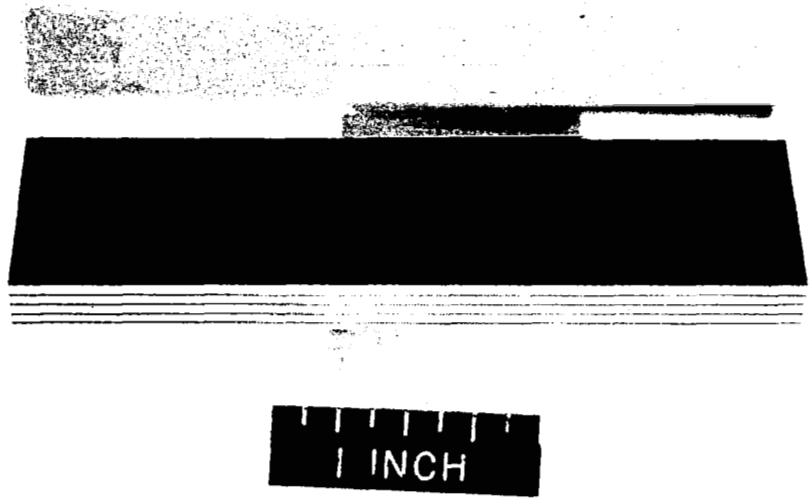
The techniques learned were next applied to larger laminates containing 64 digit and 256 word conductors which by this time had become available. A similar silicone rubber and aluminum mold of larger dimensions and incorporating several improvements to facilitate removal of the cast block was then made.

At this point, we decided to delete the hand-soldered chemically milled copper fingers in favor of other methods of inter- and intraconnection described under the respective headings. However, two sets of such fingers were cast concurrently with the ferrite in the block as a provision for future interconnection of digit conductors. Finished assemblies of this type are shown in Figs. 18(a) and 18(b).

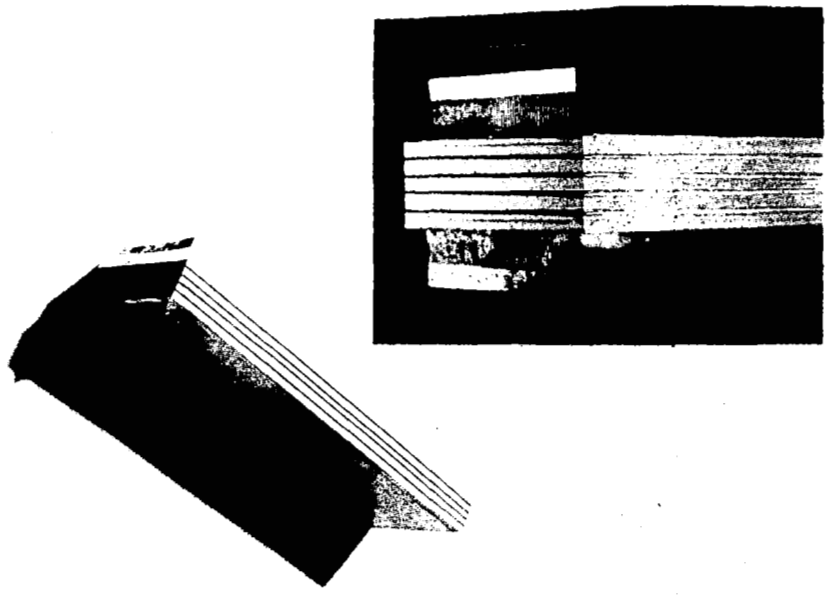
Preliminary tests of this type package indicate some adverse characteristics, especially in the form of apparent stresses on the ferrites, probably due to shrinkage of the epoxy. Quantitative data are given in Section IV.

2. Intraconnection

The original concept of locating planes in a surface-to-surface arrangement was selected in part because it was believed that intraconnection problems



(a)



(b)

Fig. 18. Four-plane assembly. (a) Plane without digit-interconnecting fingers. (b) Plane with fingers.

could be minimized. A plan of connecting the digit conductors of one plane to corresponding digit conductors of adjacent planes included the use of evaporated "bridges" of conductive metal. This plan, however, required that essentially a continuous uniform surface including laminate edges with exposed conductors could be fabricated. The epoxy cast block was elected as one means of achieving this surface.

When hand lapping of the surface was found to produce a smooth but slightly convex surface on the block edges, a final finish by grinding was introduced. The flatness is required to assure good contact between the surface and the evaporation mask.

Because of the irregular spacing between center lines of conductors in the laminates and, even more important, the difficulty of precisely locating each of the four planes relative to one another, it was necessary to devise a method for fabricating photographic negatives which would exactly match these small dimensional variations. From such photonegatives it would then be possible to make evaporation masks or permit application of other methods as might be desired for intraconnection or interconnection.

The technique[8] described below was developed. A finished casting, after being ground, is placed in the normal film plane of an accurate camera. By means of special lighting, its image is projected at about a 12 times magnification onto a sheet of unexposed film mounted on the copy board of the camera. After exposing and developing of the film sheet, an exact magnified duplicate of the exposed conductor ends in all four planes is obtained. This negative is then over-laid with a thin sheet of clear Mylar and appropriate intraconnecting lines are "drawn" with black flexible printed-circuit tape. This pattern is then located at the copy board and photographed through the same optics as used for the original projection. By making contact negatives from these reduced negatives, a final negative is produced which has essentially a zero error with the exposed laminate conductor ends. A schematic presentation of this arrangement is seen in Fig. 19, while the actual elements involved are shown in Fig. 20.

A special positioning jig for the evaporation of "bridge" patterns (see Fig. 21) was prepared and several materials were attempted as bridging conductors. Silver alone was found to have poor adhesion to both the epoxy and the ferrite. The addition of a chrome flash prior to silver evaporation improved this shortcoming, but aluminum alone was found to provide the best adhesion coupled with lowest resistance. In addition, aluminum could be easily removed by etching in the event of a poor evaporation or in the case of a misaligned mask.

Preliminary tests of the evaporated aluminum bridges indicate abnormally high resistance as compared with a similar evaporation on a glass slide used as a reference. Figure 22 is a diagram of resistance measurements made with average values shown. The exact reason for the high resistance is presently unknown.

A related technique also attempted was the vacuum plating, or "sputtering" of a copper layer over the entire end of the block followed by photoetching of all areas other than the desired bridges.

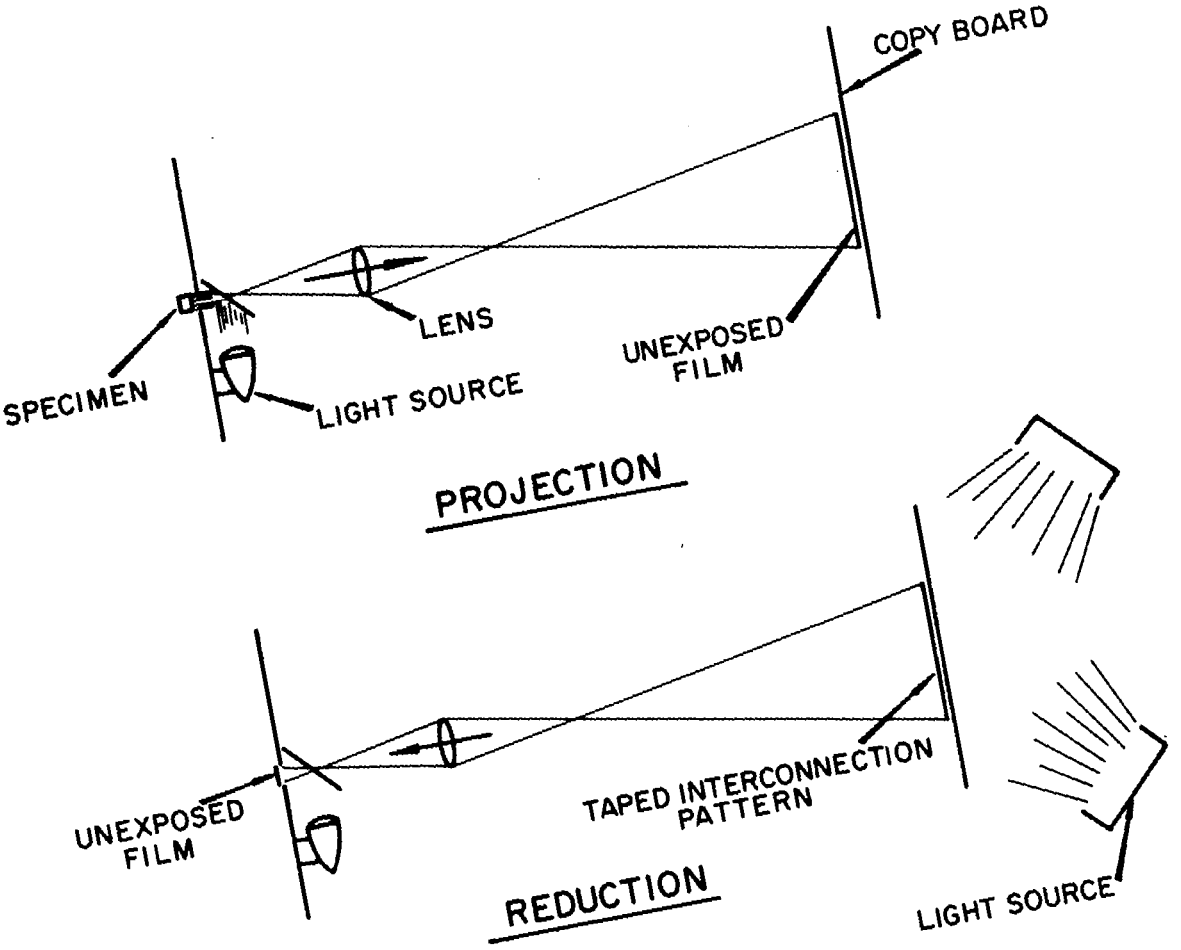


Fig. 19. Optical system.

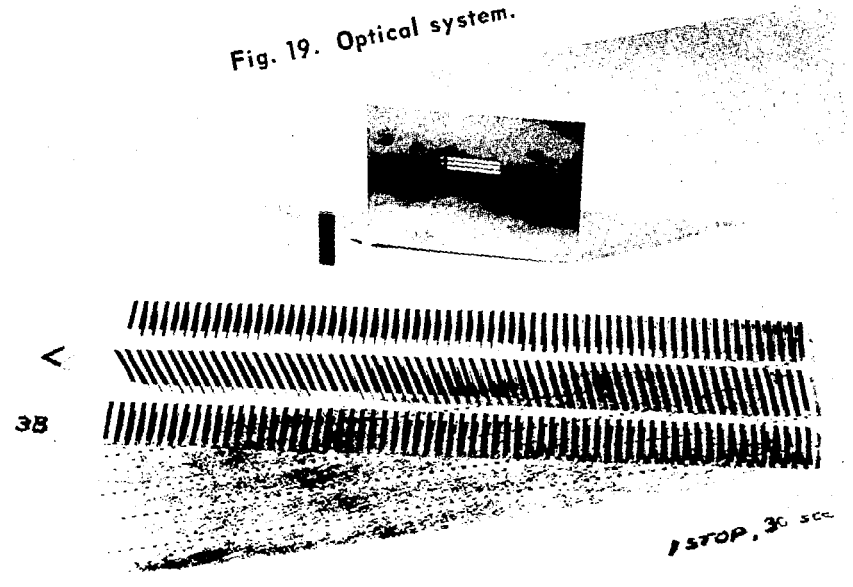


Fig. 20. Projected negative, taped overlay, and resulting mask.

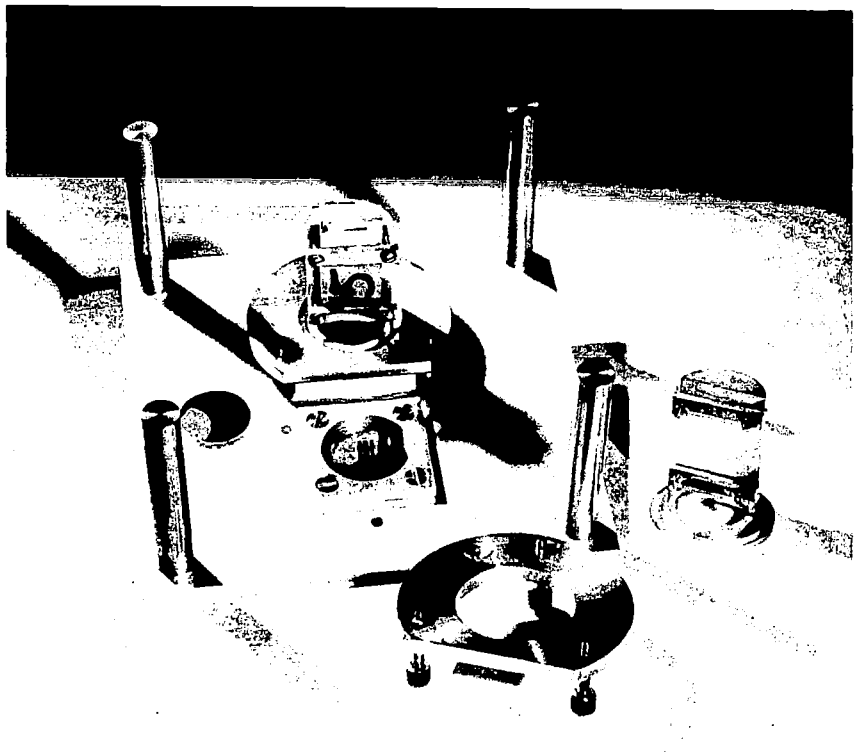


Fig. 21. Evaporation jig for producing digit conductor intraconnections.

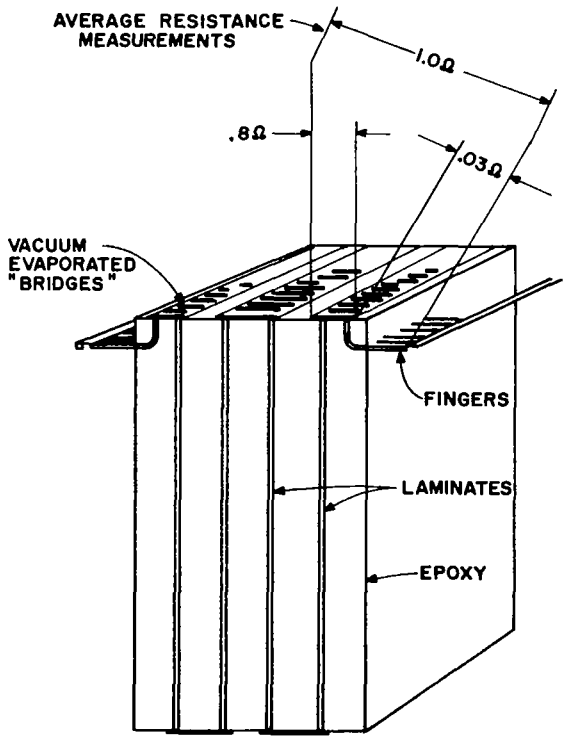


Fig. 22. Typical average resistances and block schematic.

Adhesion was found to be poor, resulting in loss of some bridges and, in addition, registration of the negative was more difficult.

Two other methods were also tried. Ultrasonic bonding of 1.5-mil aluminum wires and 0.5-mil gold wires was found to produce unacceptable bonds. Electronic (resistance) welding using a demonstration machine made by Hughes was reasonably good but the unavailability of the welding equipment precluded further test or actual use of this method.

Since the word driving system requires one termination of each word conductor to be bussed in common to ground, a single evaporation of chrome-silver is provided on one "word" edge of each block which electrically intraconnects all word conductors.

3. Interconnection

As was mentioned under the heading of packaging, a series of chemically milled fingers were successively embedded in pairs together with the four ferrite planes. These fingers, after milling, were left with a temporary buss for alignment and support and were then bent at a right angle. They were positioned in the casting mold such that the unbussed ends lay in a line parallel to the line of conductors on both the first and fourth laminates. The bussed ends protruded from the completed block to permit ultimate removal of the buss and joining to a similar set of fingers in the next block by soldering. The unbussed ends, because of their positioning in the casting, were then further exposed at the time the edge of the block was ground and, hence, appeared as a row of dots much the same as the ferrite conductors in the photographic process described under "Intraconnection". These ends were then joined to the first or fourth laminate by evaporated bridges, thereby completing the access to each individual digit conductor series string.

Interconnection of word conductor common grounds may be achieved by soldering a buss from block to block on the chrome-silver evaporated busses. A photograph of a block (substack containing 1024 x 64 bits) fully intraconnected with digit conductor projecting fingers (busses not removed) and the evaporated word-conductor common buss is shown in Fig. 23. Four such substacks have been assembled.

The techniques described above need to be modified and refined to permit the assembly of laminates without deteriorating the magnetic characteristics. Evaporated bridges appear to be a suitable means for intraconnecting the embedded conductors.

4. Assembled Stack

Four substacks were assembled using the techniques described above. Interconnection of the four substacks results in a stack of 4096 words of 64 bits -- a total of 262,144 bits.

Each substack consists of four laminated arrays (4 x 256 x 64) packaged with protruding fingers for interconnection to adjacent substacks. Pertinent data relating to the assembled substacks are summarized in Table III.

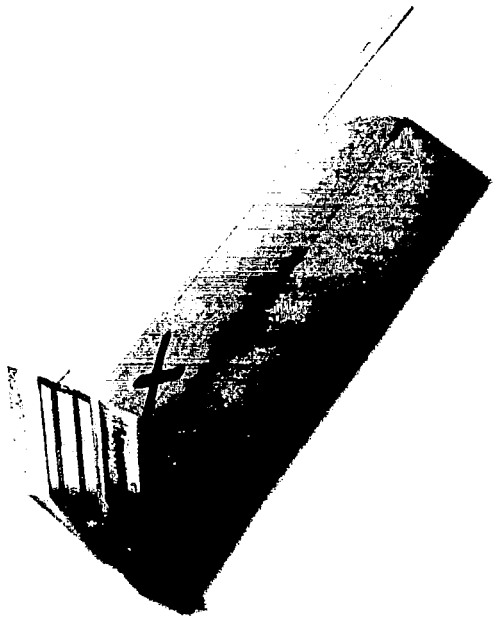


Fig. 23. Completed 4-plane assembly.

TABLE III

SUBSTACK CHARACTERISTICS

Number of bits	65,536
Number of words	1024
Number of bits per word	64
Overall dimensions in inches	2.85 x 0.78 x 0.25
Array spacing in inches	0.05
Bit density per cubic inch	1.18×10^5
Weight in lbs.	0.04
Embedded conductors	Platinum
Evaporated bridges - sense-digit windings	Aluminum
Evaporated ground - word windings	Chrome-Silver
Interconnecting fingers	Copper

IV. OPERATING CHARACTERISTICS OF LAMINATED FERRITE MEMORY PLANES

A. GENERAL DESCRIPTION

Operation[6] of the memory array in a word-organized mode may be understood with the aid of the vector diagrams shown in Fig. 24. The flux switched by a current is represented by a vector in the direction of that current. Because of the mutual orthogonality of word (x-directed) and digit (y-directed) conductors, the flux switched by word currents does not link a digit conductor unless digit current is applied. A digit pulse, overlapping in time a write pulse, switches components of flux linking both x and y conductors at the crossover point. The application of a read pulse removes that component of flux linking the digit conductor and thus induces an inelastic sense voltage. The polarity of the sense signal is dependent only on the polarity of the digit current.

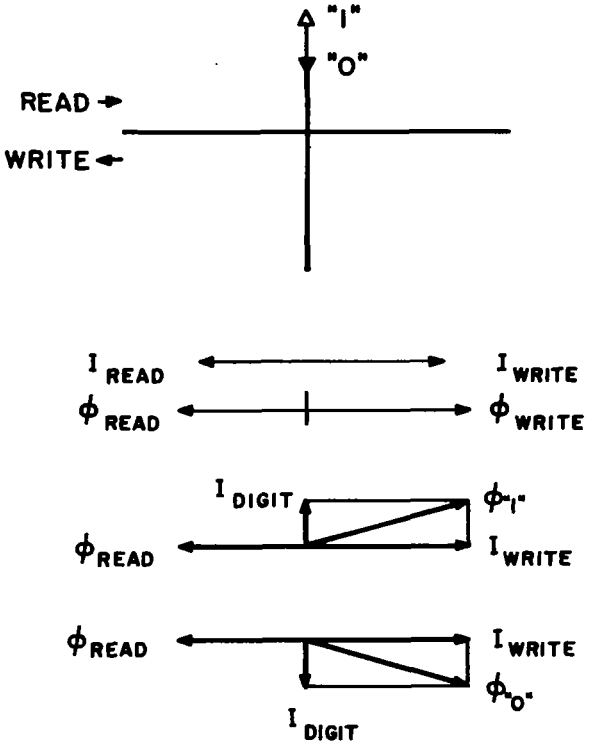
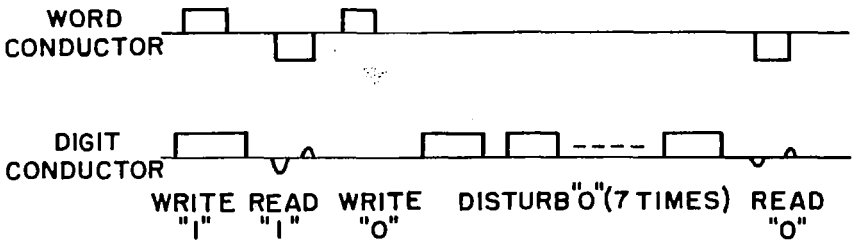


Fig. 24. Vector diagram of flux patterns at crossover point.

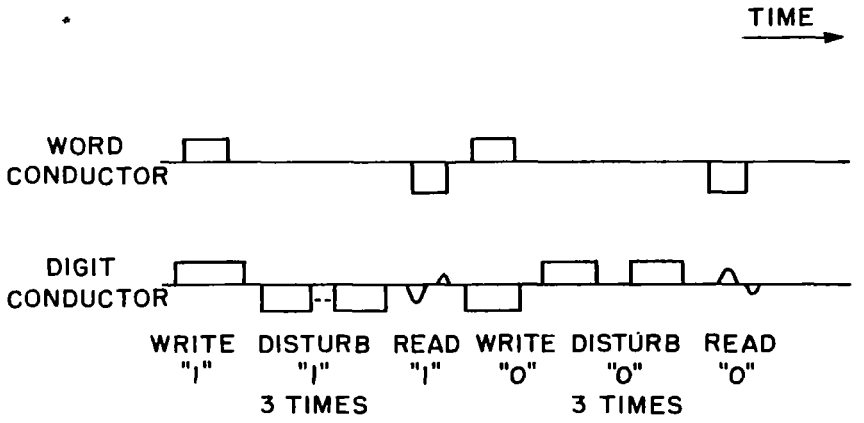
The array can be operated in a one crossover per bit mode using bipolar or unipolar digit currents. For the bipolar digiting a binary 1 is entered by applying a write current pulse and a positive digit pulse in time coincidence. A binary 0 is entered by applying a negative digit pulse. The vector diagram shown in Fig. 24 corresponds to this case. For unipolar digiting, a digit pulse (of either polarity) is applied to enter a 1 and no digit to enter a 0.

B. TEST PROCEDURE

The programmed pulser used for obtaining the test data to follow can deliver as many as 10 trigger pulses per clock cycle to each of four current drivers, two positive and two negative. The pulse programs used to test arrays in unipolar digit and bipolar digit modes are shown in Figs. 25(a) and 25(b), respectively.



(a) UNIPOLAR DIGIT



(b) BIPOLAR DIGIT

Fig. 25. Memory test pulse programs.

Test data for laminated arrays of three sizes, 16 x 16 crossovers, 256 x 64 crossovers, and 256 x 100 crossovers, are reported below. These laminates are operated with both word and digit lines grounded at one end, as shown in Fig. 26. Sense outputs are monitored with a Tektronix 1121 amplifier feeding an oscilloscope. The output data for a given plane are taken at a fixed strobe time. The strobe time is optimized on the basis of the peaking times for a few randomly selected bits.

Two different magnesium-manganese-zinc ferrite compositions have been considered for use in the low drive memory. Their characteristics and sense outputs obtained from 16 x 16 planes are given next.

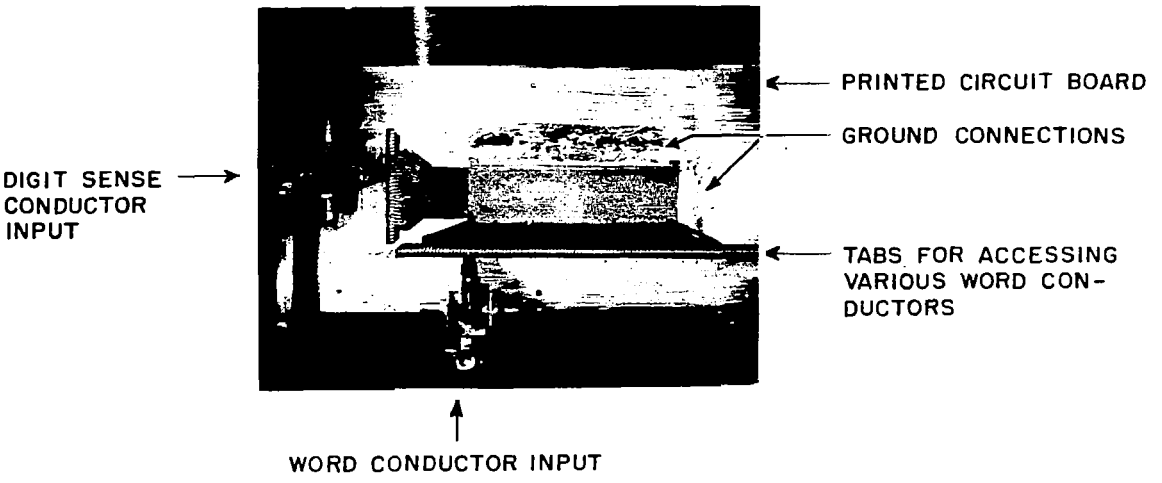


Fig. 26. 256 × 64-bit memory array mounted for test.

C. OPERATING DATA

1. Ferrite A

Ferrite A has the following magnetic properties:

Coercive force (H_c)	1.1 Oe
Remanent flux density (B_r)	1000 gauss
Switching coefficient (S_w)	0.3 Oe μsec
Squareness	0.7 (estimated)
Curie Temperature (T_c)	250°C

Its dc resistivity at 20°C is 2.1×10^6 Ω-cm when air quenched and 2.8×10^6 Ω-cm when nitrogen-annealed.

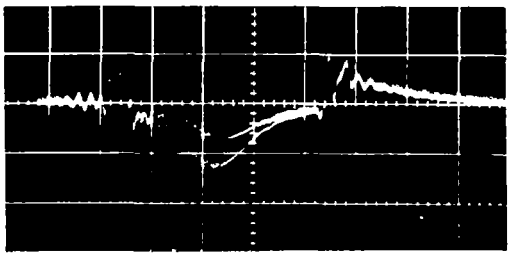
A 16 x 16 laminate was tested using unipolar digit currents. The various drive current magnitudes and durations (at the 50% points) are as follows:

I_R (read current)	80 mA	0.5 μsec
I_W (write current)	50 mA	0.7 μsec
I_D (digit current)	22 mA	0.8 μsec

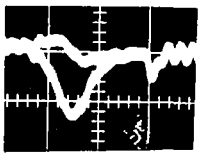
Typical peak signal outputs are:

"1" signal - v1 - 1.2 mV
Disturbed "0" signal - dv0 - 0.6 mV

The signals are 0.5 μsec wide at the base as shown in Fig. 27(a). This switching time and signal level are insufficient to utilize Ferrite A in a low drive memory application. All the remaining work reported in this section is with sample arrays composed of Ferrite B.



(a)



(b)

Fig. 27. Experimental laminate operation.

2. Ferrite B

Ferrite B has the following magnetic properties:

H_c = 0.4 Oe
B_r = 1200 gauss
S_w = 0.3 Oe μsec
Squareness = 0.9
T_c = 110°C

Its dc resistivity at 20°C is 8.6×10^7 Ω-cm for air-quenched samples and 1.1×10^8 Ω-cm for nitrogen-annealed samples.

A number of 16 x 16 laminates incorporating Ferrite B have been evaluated using a unipolar digit program [Fig. 25(a)]. The drive currents and their duration at the 50% points are:

I_R (read current)	40 mA	0.5 μsec
I_W (write current)	35 mA	0.3 μsec
I_D (digit current)	3 mA	0.5 μsec

Typical peak signal outputs are:

"1" signal - v1 = 1.4 mV
Disturbed "0" signal - dv0 = 0.4 mV

The signals are about 0.3 μsec wide at the base as shown in Fig. 27(b).

A series of 256 x 64 and of 256 x 100 sample planes composed of Ferrite B have been fabricated and evaluated using one or both of the pulse programs of Fig. 25. Their characteristics and performance are given in the next section.

3. Kilo-Bit Array Performance

All of the tested arrays are composed of Ferrite B; their sintering terminates with either an air quench (air Q) or a nitrogen anneal (N_2 anneal). The sample physical characteristics are given in Table IV.

The sample number "OS" in Table IV refers to all four 256 x 64 planes of the "O" series utilized to fabricate the prototype memory stacks described in Section III.

The operating characteristics of the kilo-bit arrays are presented in Table V. The test pulses had the nominal durations at the 50% points given below:

I_R = read current = 0.5 μsec
I_W = write current = 0.4 μsec
I_D = digit current = 0.7 μsec

Bipolar digiting is denoted by the presence of both + and - signs in the I_D column; for that case both the 1 and 0 signals are disturbed according to the program of Fig. 25(b). The read current risetime is 0.3 μsec for 256 x 64 samples and 0.4 μsec for 256 x 100 samples.

It is clear from the data of Table V that in the one-crossover-per-bit mode of operation, the arrays require bipolar digit currents for reliable sensing.

The uniformity of bit outputs from planes with a high percentage of bipolar outputs under conditions of the bipolar digit program is shown in the histograms of Figs. 28, 29, and 30 for samples M7, JK3, and JK12, respectively. For these figures, the output signals are quantized in 0.2-mV steps.

D. EFFECTS OF LAYER THICKNESS VARIATION ON ARRAY PERFORMANCE

Two of the kilo-bit arrays described in the previous section have significantly different layer thickness arrangements. All of the samples through the "M" series except for M5 and M6, are symmetrical about the center layer, i.e., the ferrite sheets containing the word conductors are equal in thickness to those containing the digit conductors. Sample M5 has an extra 2-mil layer of ferrite covering the word lines whereas sample M6 has an additional 2-mil covering over its digit lines. The superior performance of M5, obvious from Table V, is attributed to the fact that switching due to word currents now extends all the way to the surface of the sample, as illustrated in Fig. 31.

TABLE IV

SAMPLE PHYSICAL CHARACTERISTICS

Sample Number	Number of Crossovers	Conductor Material	Conductor Cross Section in mils	Sinter Process	Number of Tested Bits
Z1	256 x 64	platinum	1.1 x 0.7	air Q	48
Z2	256 x 64	platinum	1.1 x 0.7	air Q	24
Z4	256 x 64	platinum	1.1 x 0.7	air Q	18
Y1	256 x 64	rhodium	1.1 x 0.7	air Q	18
E2	256 x 64	platinum	1.1 x 0.7	air Q	134
D4	256 x 64	platinum	1.1 x 0.7	air Q	41
G7	256 x 64	rhodium	1.1 x 0.7	air Q	96
10	256 x 64	platinum	2.5 x 1.0	air Q	13
11	256 x 64	platinum	2.5 x 1.0	air Q	73
13	256 x 64	platinum	2.5 x 1.0	air Q	18
K2	256 x 64	platinum	2.4 x 1.0	N_2 annealed	280
K17	256 x 64	platinum	2.4 x 1.0	N_2 annealed	29
K18	256 x 64	platinum	2.4 x 1.0	N_2 annealed	236
M0	256 x 64	platinum	2.4 x 1.0	N_2 annealed	256
M5	256 x 64	platinum	2.4 x 1.0	N_2 annealed	210
M6	256 x 64	platinum	2.4 x 1.0	N_2 annealed	91
M7	256 x 64	platinum	2.4 x 1.0	N_2 annealed	280
M9	256 x 64	platinum	2.4 x 1.0	N_2 annealed	220
O6	256 x 64	platinum	2.4 x 1.0	N_2 annealed	150
O7	256 x 64	platinum	2.4 x 1.0	N_2 annealed	110
O11	256 x 64	platinum	2.4 x 1.0	N_2 annealed	119
OS	256 x 64	platinum	2.4 x 1.0	N_2 annealed	936
JK0	256 x 100	platinum	2.3 x 0.7	N_2 annealed	112
JK3	256 x 100	platinum	2.3 x 0.7	N_2 annealed	234
JK9	256 x 100	platinum	2.3 x 0.7	N_2 annealed	150
JK12	256 x 100	platinum	2.3 x 0.7	N_2 annealed	168

TABLE V

SAMPLE OPERATING CHARACTERISTICS

Sample	I_R	I_W	I_D	Best		Typical		Percent Bipolar Outputs	Peak Back Voltage per bit - mV
				v1	dv0	v1	dv0		
Z1	36	16	2.3	0.7	0.2	0.8	0.4	--	11.0
Z1	36	16	±2.3	±0.35	-0.4	+0.2	-0.4	37%	11.0
Z2	36	12	1.8	0.8	0.3	0.9	0.5	--	9.4
Z4	36	19	1.9	0.6	0.1	0.8	0.3	--	11.7
Y1	36	20	5.5	1.5	0.6	1.5	1.0	--	13.3
E2	40	16	1.8	0.6	0.1	0.7	0.3	--	15.5
E2	40	20	±2.4	+0.4	-0.4	{+0.1 / +0.5}	{-0.5 / -0.1}	51%	15.5
D4	40	20	2.2	0.7	0.2	0.8	0.4	--	--
D4	40	20	±2.2	+0.4	-0.4	+0.2	-0.5	86%	--
G7	40	17.5	±3.3	+0.2	-0.3	-0.1	-0.4	30%	--
10	63	37	±6.5	-0.4	+0.2	+0.3	-0.1	67%	15
11	50	17	11	1.0	0.4	1.3	0.6	--	6.3
11	50	20	-12.5 +4	+0.9	+0.3	+1.0	+0.4	--	6.5
13	52	26	±7.2	+0.5	-0.1	+0.3	-0.1	78%	--
K2	50	18	±5.5	+2.2	-2.0	+1.4	+0.4	44%	18.0
K17	42	26	7.5	0.8	0.3	0.9	0.5	--	--
K18	45	30	4.0	1.8	0.8	1.6	1.2	--	14.5
K18	47	34	±3.3	+2.2	-1.2	+0.8	-0.6	80%	14.5
M0	52	23	±6.0	+2.2	-2.6	+1.5	-1.5	85%	17.2
M5	48	20	±5.5	+2.8	-2.4	+2.0	-2.0	97%	19.5
M6	48	18	±5.0	+1.0	-1.2	+1.0	-1.0	75%	17.2
M7	50	20	±6.0	+2.0	-2.2	+1.5	-1.5	99%	22.0
M9	50	20	±5.0	+0.8	-1.0	+1.0	+0.2	47%	--
06	50	20	±5.0	+2.2	-1.6	+1.0	-1.0	99%	--
07	50	24	±5.1	+2.0	-3.2	+2.0	-2.0	98%	21.1
011	50	26	±5.0	+2.0	-2.4	+1.7	-1.7	92%	20.3
JK0	50	18	±5.0	+1.4	-1.8	+1.3	-1.3	94%	--
JK3	48	20	±5.0	+2.8	-1.8	+1.6	-1.6	98%	28.0
JK9	50	20	±5.0	+1.2	-1.2	+0.8	-1.0	56%	19.0
JK12	50	20	±5.0	+2.8	-2.0	+2.0	-2.0	100%	26.0

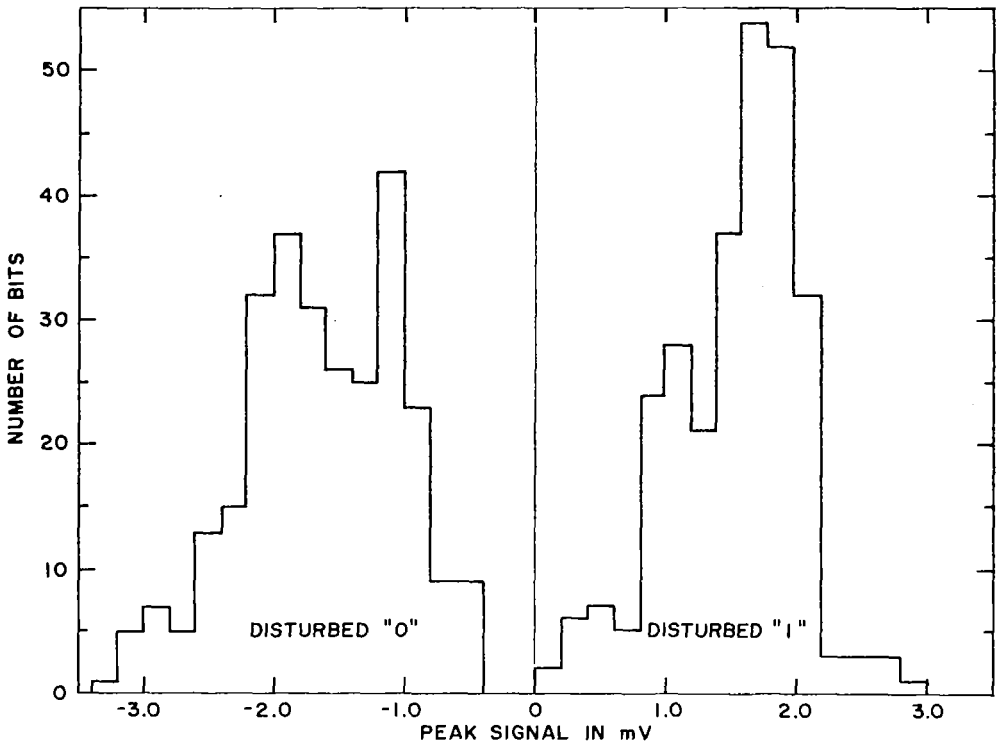


Fig. 28. Histogram of outputs – Sample M7.

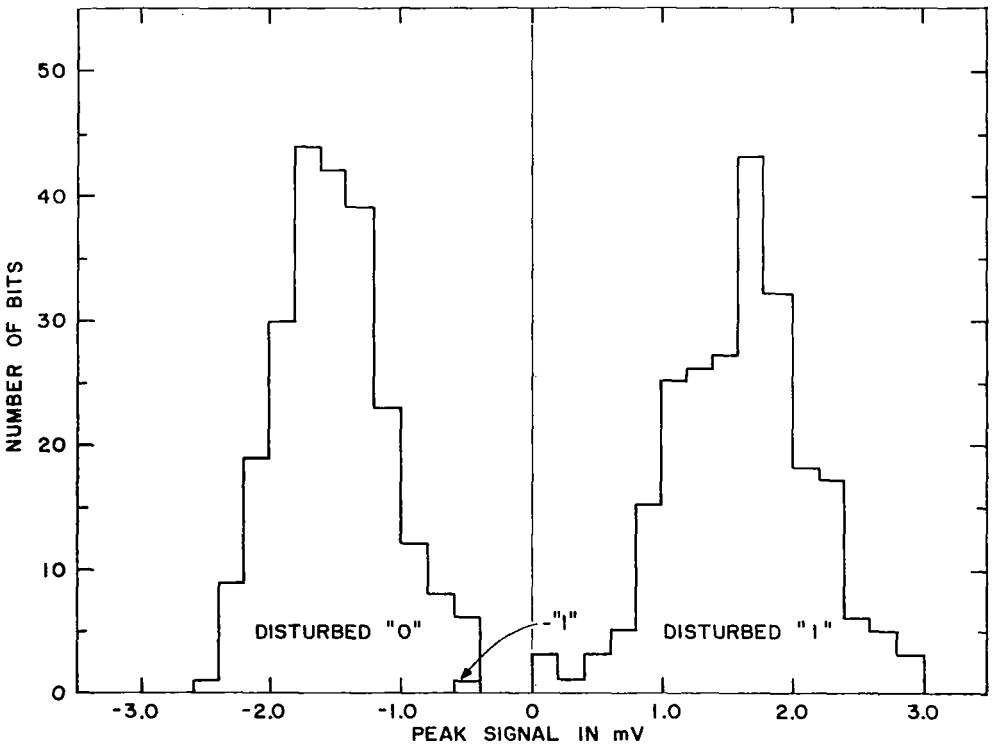


Fig. 29. Histogram of outputs – Sample JK3.

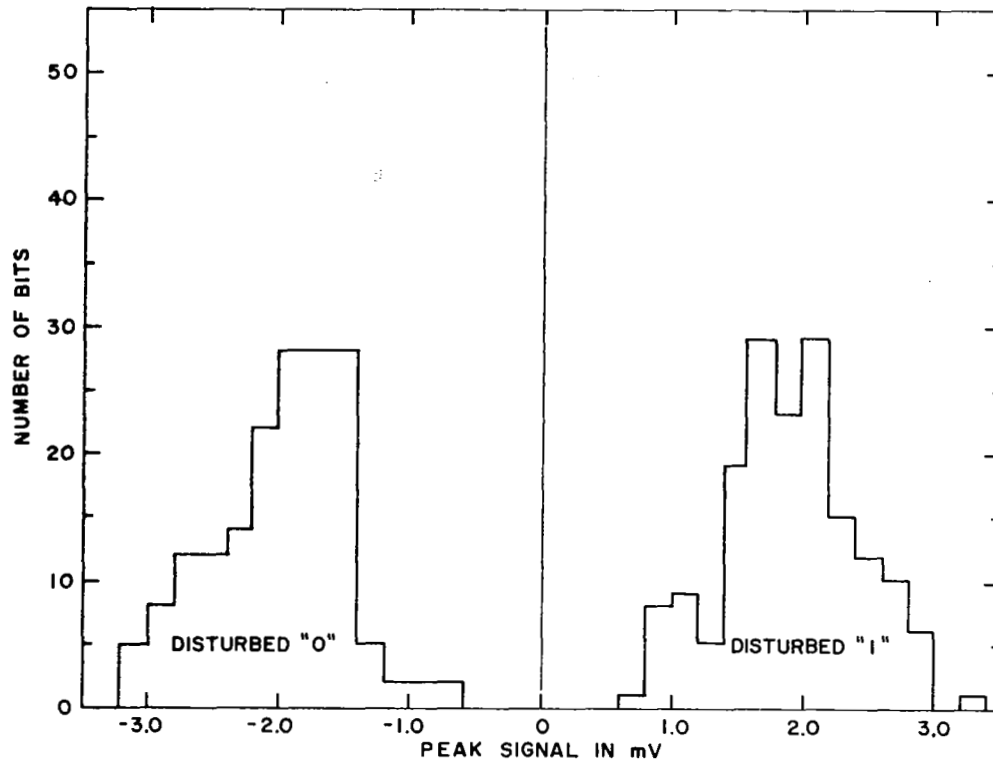


Fig. 30. Histogram of outputs – Sample JK12.

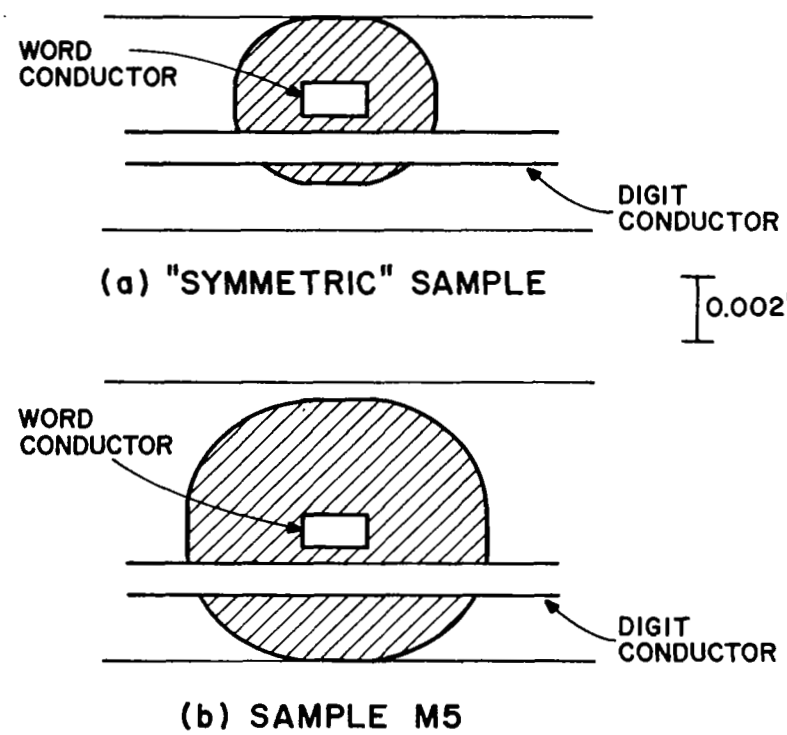


Fig. 31. Flux-switching regions (shaded) vs. layer thickness.

E. SOLID EPOXY STACK PERFORMANCE

1. 16 × 16 Array

To determine whether a stack assembly technique involving a complete embedding of the ferrite sheets degrades memory operation, a 16 x 16 array composed of air-quenched Ferrite B was tested before and after encapsulation in epoxy. The test drive currents (unipolar digiting) are given below:

I_R . . . . 40 mA $\quad \tau_R = 0.3$ μsec
I_W . . . . 22 mA
I_D . . . . 4.6 mA

These currents were reproduced within ± 5 percent for testing the sample after it was encapsulated in epoxy.

A comparison was made of the 1 and disturbed 0 signals (v1 and dv0) at the same scattered bit locations before and after encapsulation. With the exception of four bits along one edge of the sample, the 1 signal amplitudes decreased between 13 and 21 percent and the corresponding disturbed 0 signal amplitudes decreased between 10 and 50 percent. Of the four edge bits, one had identical outputs, two had increases of signal and noise, and one had a decrease of 10 percent in both signal and noise. In general, the v1:dv0 ratio was improved by encapsulation, but not uniformly.

2. Four-Plane Stack

The four-plane (256 x 64) substack described in Section III was mounted and tested. The ferrite planes used for the stack were drawn from the "0" series; see entry OS in Table IV. No intraconnections were formed on this stack, necessitating individual testing of the four planes. As in the testing of unencapsulated planes, one end of both the digit and the word conductor array is commonly grounded. The ground here was formed by sputtering of copper layer on the stack face and backing this with silver paste. Electrical connections to selected bits are made utilizing probes mounted in micromanipulators, as shown in Figs. 32 and 33. In each of the four planes, numbered 1 to 4 from top to bottom (Fig. 32), a grid of 26 word lines (every tenth) by 9 digit lines (every eighth) was tested, 234 bits in all. The test currents were individually optimized for each of the four planes. Their nominal widths are as in Section C-3. The amplitudes are given in Table VI.

TABLE VI

STACK CURRENT AMPLITUDES

Plane No.	Read Current (mA)	Write Current (mA)	Digit Current (mA)
1	50	22	± 4
2	50	24	± 2.6
3	50	20	± 5
4	50	22	± 4

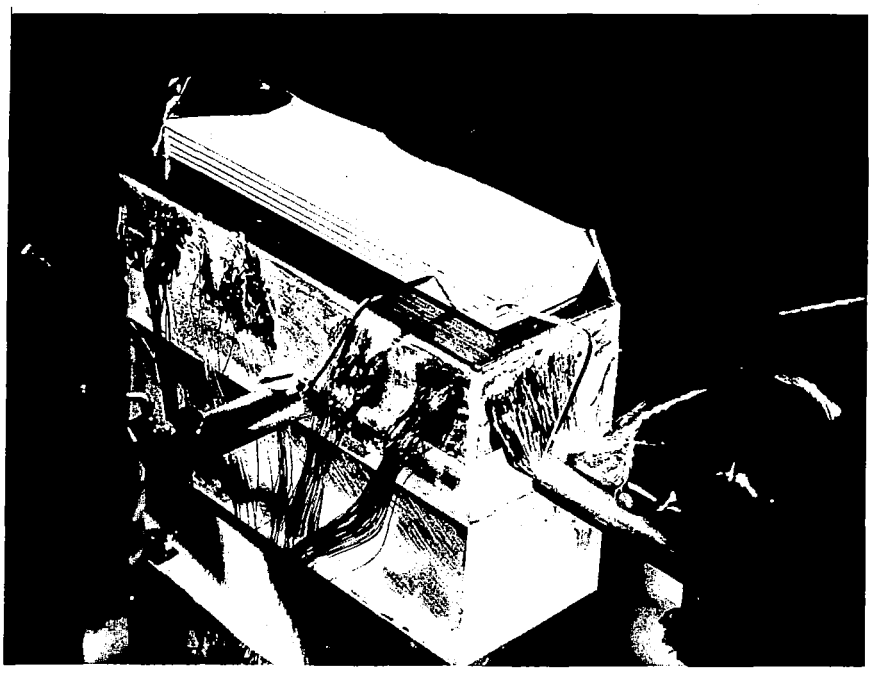


Fig. 32. Four-plane stack mounted for test.

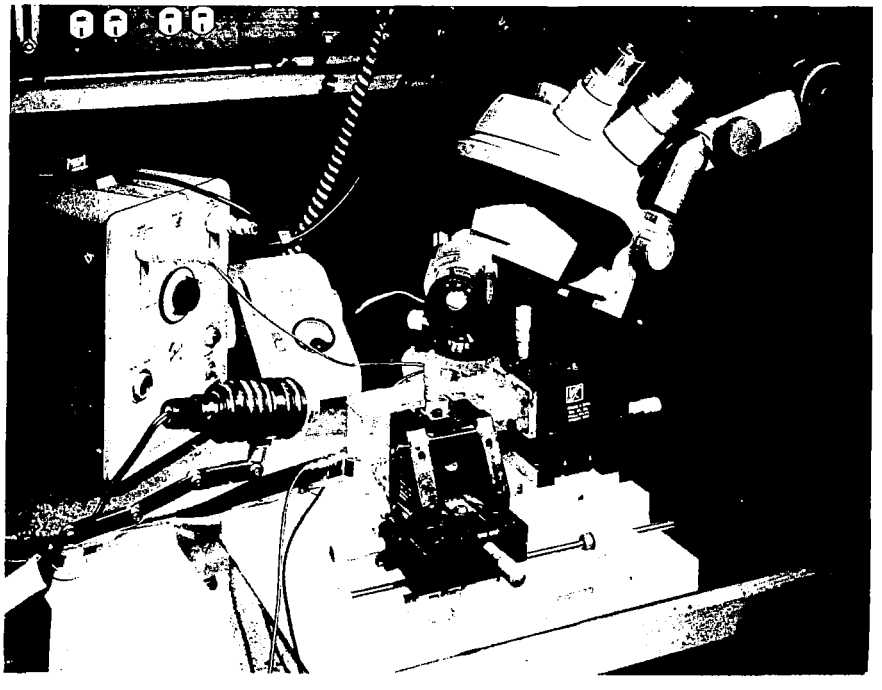


Fig. 33. Test apparatus for 4-plane stack.

The percentage of disturbed bipolar kit outputs for the four planes is 57%, 63%, 64%, and 56% for Planes 1, 2, 3, and 4, respectively. Note that the three singly tested planes of the "0" series had in excess of 90% bipolar outputs (Table V). The physical regions where unipolar outputs are observed in each of the four planes are denoted by shading in Fig. 34.

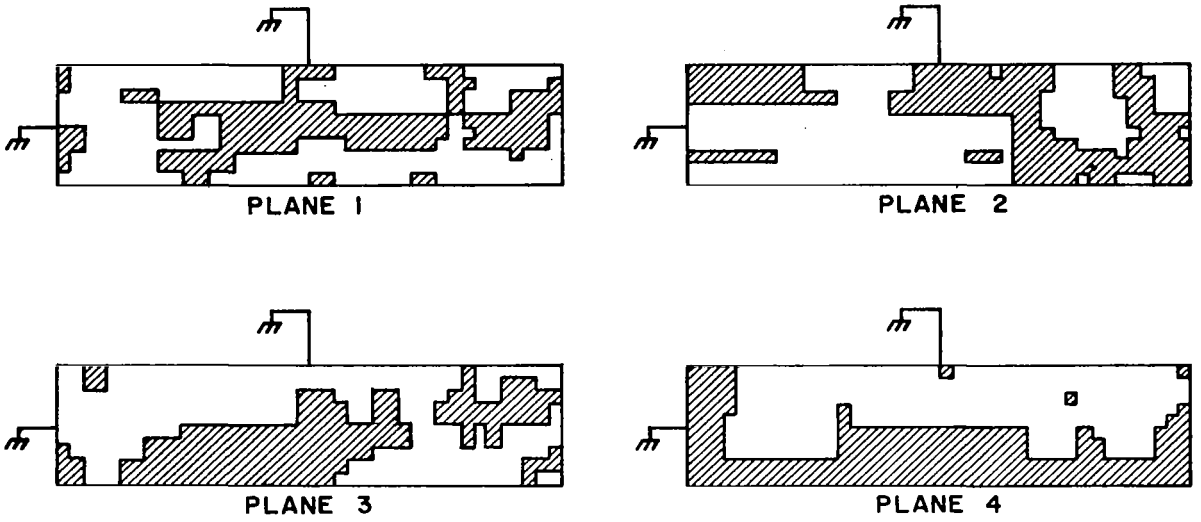


Fig. 34. Regions of unipolar outputs in prototype stack.

One explanation for the data is the presence of nonuniform stress in the planes due to nonuniform adherence of the epoxy to the laminated ferrite sheets. This nonuniform adherence is due, at least in part, to the heating cycles suffered by this prototype stack during the copper sputtering experimentation. Microscopic inspection of the stack faces after sputtering revealed regions of nonadherence between epoxy and ferrite at the stack edges. A less likely alternative explanation is that the planes were inherently nonuniform.

F. EFFECT OF READ CURRENT WAVESHAPE ON SENSE SIGNALS

One of the bits in sample K2 with relatively high sense output was selected to check the effect of read current amplitude and risetime on the sense signal and back voltage.[8] To separate the effects of risetime and amplitude, two experiments were performed: (1) The risetime was held fixed at 0.3 μsec and the read current amplitude varied from 20 to 80 mA. (2) The read current amplitude was fixed at 50 mA and the risetime varied from 0.03 to 0.4 μsec. In both experiments the bipolar digit currents were held fixed. The write current was optimized for maximum sense signal in the first experiment in which the read current amplitude was varied.

Figure 35 shows the dependence of sense signal amplitude (solid curve) and switching time, τ_S (defined as time from beginning of read pulse to end of sense output), on read current amplitude. The anomalous dip in τ_S at 30 mA is due to a decrease in optimum write current which in turn results in higher peak sense signal but lower sense flux. Note the gradual leveling off of sense signal amplitude as the switching time τ_S approaches the risetime of the read pulse. The back voltage due to flux-switching climbs from 9.4 mV/bit at 50-mA read current to 18 mV/bit at 80-mA read current whereas the sense signal goes from 4.7 mV to 6 mV, a marked drop in "efficiency".

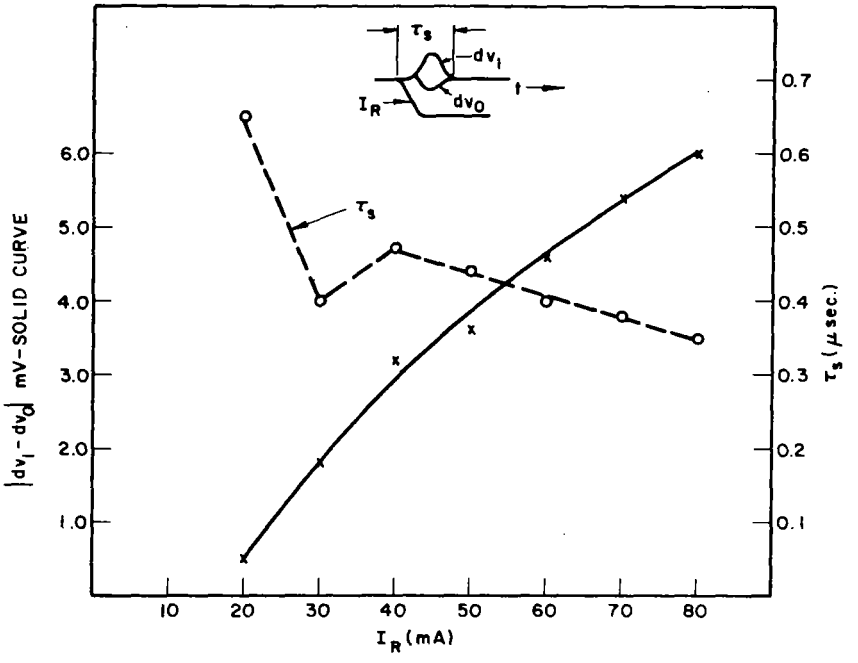


Fig. 35. Effect of read amplitude on signal.

Figure 36 shows that the signal magnitude is relatively insensitive to the risetime, only doubling for a 4:1 change in τ_R. Concurrently, the bit back voltage increases fivefold.

G. DISTURB SENSITIVITY

One of the bits in Sample 07 was utilized to check the disturb characteristics of the samples for disturb bursts of length greater than the three which are used in the standard bipolar digit program of Fig. 25(b). The pulse program is shown in Fig. 37. The test current data are given below:

Current	Amplitude	Duration	Risetime
I_R	50	0.8	0.2
I_W	20	0.6	0.2
I_D	varies	1.5	---

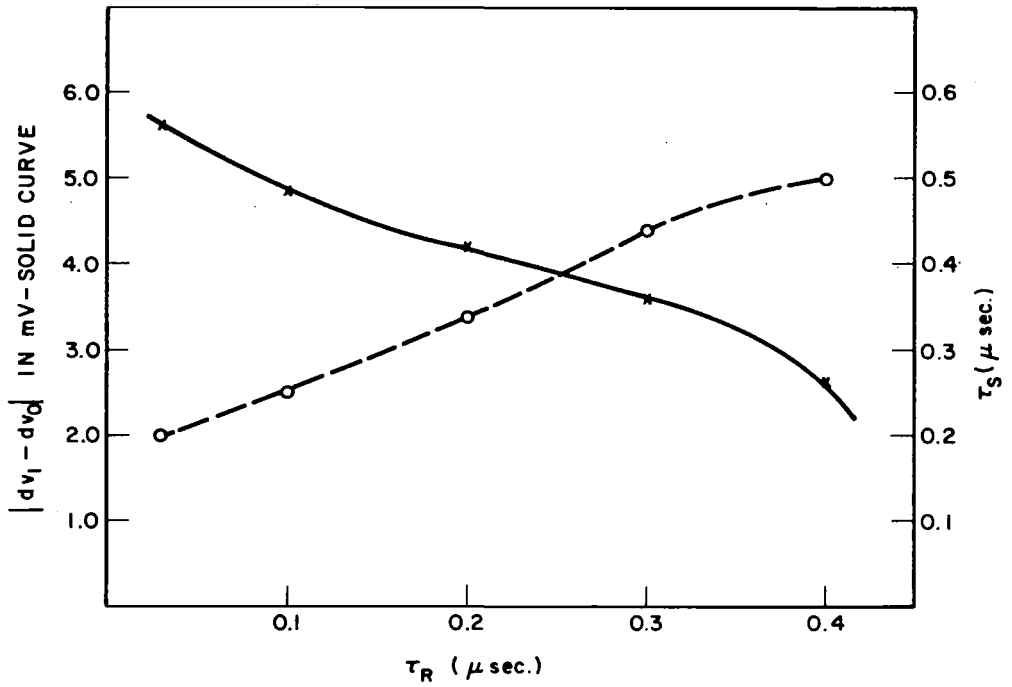


Fig. 36. Effect of read risetime on signal.

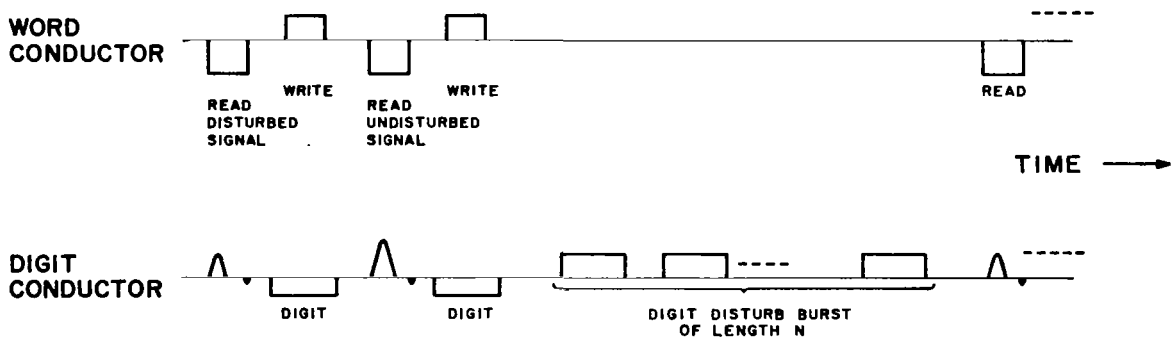
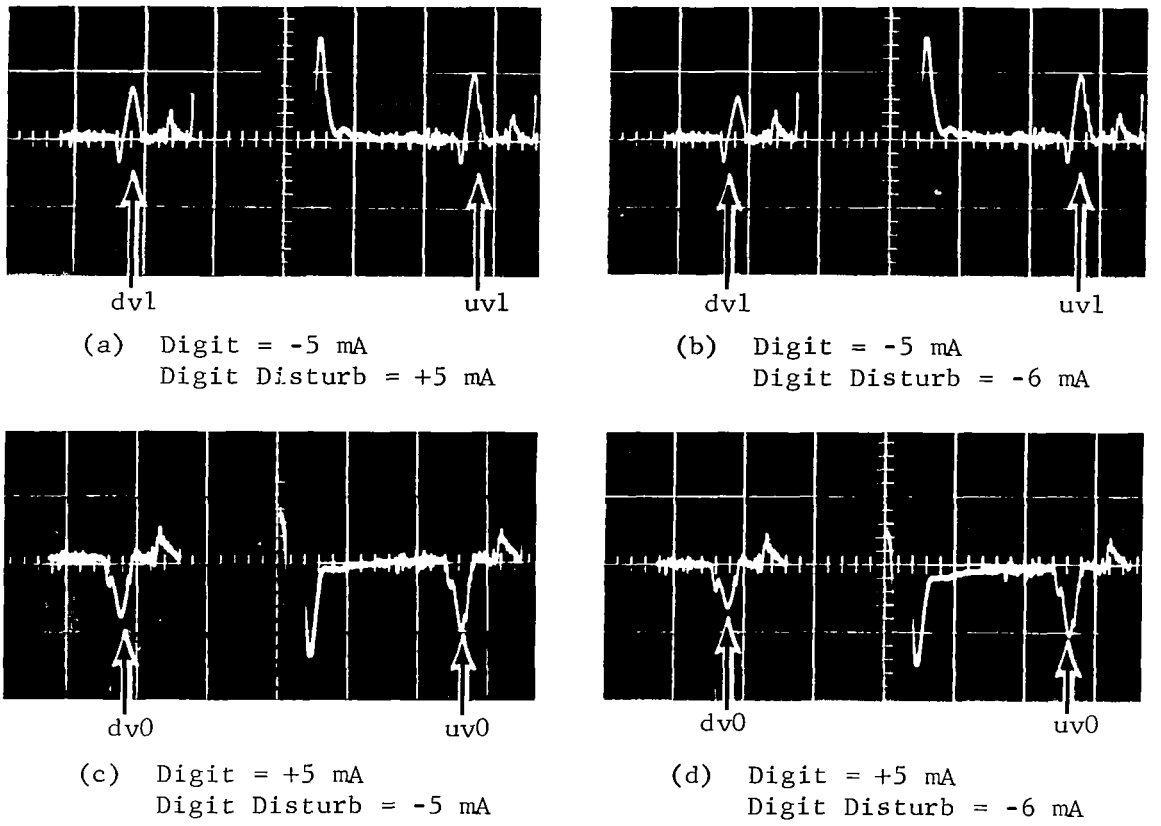


Fig. 37. Disturb burst program.

Oscillograms of the disturbed and undisturbed signal waveforms are shown in Fig. 38 for a long disturb burst, N = 170,000 pulses. The polarities and amplitudes of the digit pulses used for writing ("digit") and the digit pulses used for disturbing ("digit disturb") are given in Fig. 38. A single digit disturb, N = 1, degrades the undisturbed signal by one half as much as the long



(a) Digit = -5 mA
Digit Disturb = +5 mA

(b) Digit = -5 mA
Digit Disturb = -6 mA

(c) Digit = +5 mA
Digit Disturb = -5 mA

(d) Digit = +5 mA
Digit Disturb = -6 mA

Horiz. Scale: 1.0 μsec/div.
Vert. Scale: 5 mV/div.

Fig. 38. Disturb behavior of Sample 07.

burst. Note that in Figs. 38(b) and (d) the disturbing digit is 20 percent greater in magnitude than the nominal digit used for writing (5 mA). However, a discernable signal remains. A 50 percent greater disturb (i.e., 7.5 mA) is sufficient to "kill" the signal.

H. NOISE CHARACTERISTICS [6]

Ohmic, capacitive, and inductive coupling between the word drive and the digit-sense conductors result in extraneous noise during read time.

1. Ohmic Coupling

The coupling resistance between a word conductor and a sense-digit conductor ranges from 2.5×10^7 Ω to 250×10^8 Ω (computed for an assumed ferrite resistivity ranging from 10^5 to 10^8 Ω-cm). These coupling resistors lead to

current leakage which is highest at the ungrounded end of the word conductor. Even there this leakage induces negligible noise.[6]

2. Capacitive Coupling

During the risetime of the read pulse, the capacitive coupling between the word and digit conductors, on the order of 0.1 pF, leads to a noise voltage an order of magnitude below signal level for read current risetimes of 0.2 μsec or greater.[6] For high-speed laminated ferrite memories this noise requires a two-crossover-per-bit mode of operation.

3. Inductive Coupling

If the ferrite sheets were infinite in their lateral dimensions, perfectly uniform in thickness and magnetic characteristics, and the conductors were perfectly orthogonal, the only inductive coupling between word and digit conductors would be that due to the digit current. In practice, none of these idealizations hold, and the amount of undesired inductive coupling depends on the extent of the departure from the ideal. With reasonable care, extraneous inductive coupling is held an order of magnitude below signal level.

V. RADIATION STUDIES

A. FACILITIES

A five-megawatt, pool-type nuclear reactor at the Industrial Reactor Laboratories, Inc. (IRL), in Plainsboro, New Jersey (approximately two miles northeast of RCA Laboratories) has been used to study the effect of neutron radiation on both ferrite materials and field-effect transistors. IRL is jointly owned by RCA and nine other corporations, and the reactor is operated by Colombia University. Normally, the reactor is in operation for a 90-hour period each week.

The primary purpose of the IRL reactor is to provide a source of neutrons, gamma rays and radioactive isotopes for experimentation. It provides a number of locations where specimens may be placed or experiments conducted to utilize the radiations. These include:

1. One 12-inch square and one 8-inch diameter beam tube, and four 6-inch diameter beam tubes, extending from the outside vertical walls of the pool to the face of the core, which may be used in water- or air-filled conditions with appropriate shield plugs. Two beam tubes are currently in use by RCA. They have a working diameter of 1-1/8 inch and are 14-1/2 feet long. For tests during radiations, fiber-glass-insulated aluminum leads at least 14-1/2 feet long are required.

2. A horizontal thermal column, four feet square in cross section, filled with stringers of high-purity graphite, which makes available a wide range of fluxes of "slow" or "thermalized" neutrons.

3. Two pneumatic "rabbit" tubes which pass alongside the core for convenient short exposures of small samples.

4. Space in the water around the reactor and unused positions in the core grid plate which may be used for specimen irradiation.

5. Gamma irradiation facilities outside the pool area using the reactor fuel elements as the source of radiation.

6. Gamma irradiation in the pool from fuel elements which have been in the reactor core.

RCA has its own laboratory facilities at IRL, and a staff of its own personnel carries out its individual research program.

In addition to various heavily shielded facilities for the storage and handling of radioactive materials that have been exposed in the reactor, the "hot" laboratory accommodations include three special cells in which experiments can be handled by "master-slave" mechanical manipulators. Each of these cells is constructed of high-density concrete, 3 feet thick, faced with steel skins, with access through doors weighing 13 tons each.

Characteristics of the two locations where the experiments were carried out are given in Table VII, where "fast" neutrons are defined here as those having an energy greater than 500 eV.

TABLE VII

IRRADIATION CONDITIONS

	Neutrons $cm^{-2} sec^{-1}$		Max. Exposure per Run
	Fast	Thermal	
Hydraulic Rabbit	10^{13}	1×10^{13}	1 hour
At Core (in water)	10^{13}	1.5×10^{13}	90 hours

B. FERRITE COMPONENTS

1. Introduction

Experiments were conducted to determine the effect of neutron radiation on the fundamental physical properties of ferrites A and B (described in Sect. IV). The basic properties studied before and after irradiation are: coercive force H_c, remanent flux density B_r, hysteresis loop squareness, electric resistivity ρ, and dielectric ϵ.

2. State of the Art

Ceramics (ferrites belong to the ceramic family) are quite radiation-resistant.[9] The damage mechanism in ferrites is thought to be displacement of the metal ions, thus causing vacancies and interstitials in the spinel structure.

Some work has been done on square-loop ferrites suitable for memory applications.[10-12] Sery et al.[10] studied 50-50 Ni ferrite and found small changes (10 percent at most) in the coercive force H_c and the flux density B_r. Moss et al.[11] investigated fast-switching magnesium-manganese ferrites after exposures up to 3×10^{18} nvt (fast neutrons). They found changes in the hysteretic properties (H_c increased and B_r decreased) after 10^{18} nvt but no change in the switching speed. Taimuty and Mills[12] measured the radiation sensitivity of two magnesium-manganese memory cores (Ferramic S1 and S3) as well as a variety of microwave ferrites. The memory cores exhibited slight (almost within experimental error) increases in H_c and even smaller increases in B_r. In a previous study on ferrite resistivity changes after irradiation, a variety of nickel-zinc and manganese-zinc commercial ferrites were exposed to a simulated nuclear burst.[13] Although the momentary neutron dose had high intensity the integrated flux was low, up to 10^{13} nvt including thermals, and no measurable effect on resistivity was found.

3. Experimental Procedure

a. Radiation Conditions - The ferrite samples to be irradiated were placed in watertight aluminum cans weighted with lead which were lowered into the pool to a position near the reactor core face. Five cans were exposed for the times shown in Table VIII to achieve the indicated integrated neutron dosages (the 10^{19} can also contained toroids already exposed for 300 hours so that the total dosage for those samples is 2 x 10^{19} nvt).

TABLE VIII

EXPOSURE TIMES

Dosage (nvt)	10^{15}	10^{16}	10^{17}	10^{18}	10^{19}
Time	100 sec	16.6 min.	3 hrs.	30 hrs.	300 hrs.
Condition of Lead Weights	unaffected	partially melted	completely melted	partially melted	slightly melted

The dosage numbers are accurate to ± 15 percent. The neutron energy spectrum is given in Fig. 39. Besides the neutron dosage the samples were exposed to a gamma irradiation flux amounting to 10^8 to 10^9 rads/hour. The temperature of the samples during exposure was not monitored.

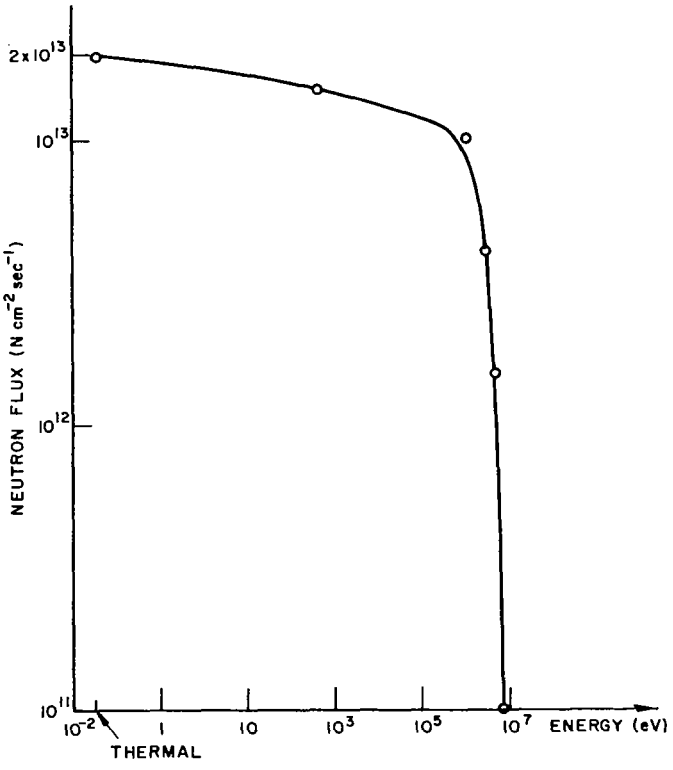


Fig. 39. Neutron energy spectrum.

The pool ambient is approximately 40°C. However, the contents of the sample cans are at much higher temperatures, in the range of 200°-300°C as previously experienced with a variety of samples. This temperature rise is primarily due to gamma irradiation. Small samples with high surface-to-volume ratio are more efficient radiators of heat and will tend to run cooler than larger samples. This is seen in the behavior of the lead weights in the sample cans. The weights in the 10^{15}, 10^{16}, and 10^{17} cans were larger than those in the 10^{18} and 10^{19} cans, and, thus, melting of the lead was most severe in the case of the 10^{17} exposure as seen in Table VIII. The melting point of lead is 327.4°C so that the weights reached that temperature in all cases except the 10^{15} case where the exposure time is only 100 sec. The ferrite samples were not in good thermal contact with the outer can because they were in small individual cans. On the other hand, their surface-to-volume ratio is much better than the weights so that they radiate more efficiently.

b. Magnetic Properties - Forty-five toroidal samples, cut with a "cookie cutter" from two sheet laminates, have been fabricated. Their green dimensions are 190 mils OD, 140 mils ID, and 6 to 8 mils thick. Upon sintering, all dimensions shrink by approximately 20 percent. The 400-cps hysteresis loops, at room ambient, were photographed before and after irradiation, and comparisons were made between the coercive force H_c, the remanent flux density B_r, and the general appearance of the loops. Figure 40 defines the quantities of H_c and B_r.

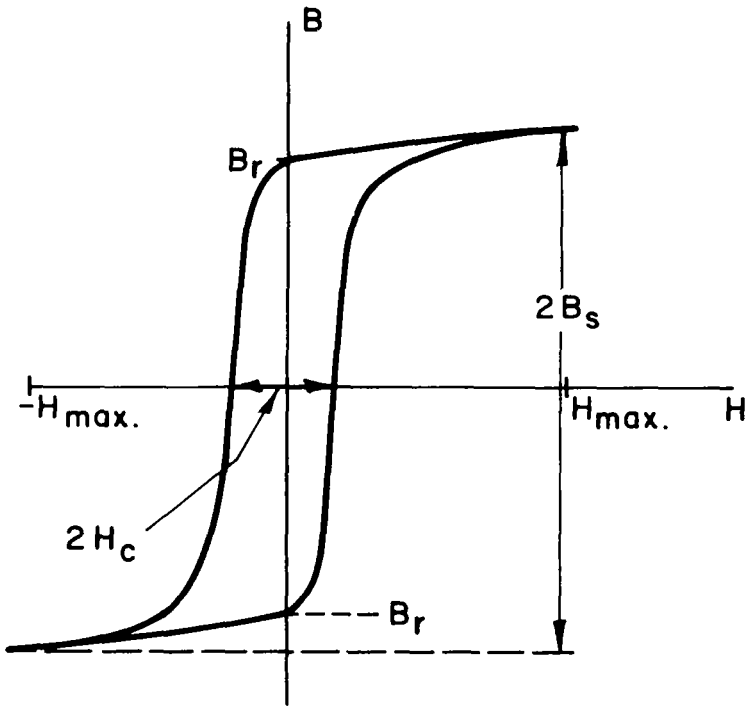


Fig. 40. Hysteresis loop.

The ferrite materials used are ferrites A and B (see page 28 for a description), both air-quenched and nitrogen-annealed.

c. Electric Properties - To determine resistivity and dielectric constant changes, samples in the form of capacitors were fabricated. Sintered sheets of ferrite 3 in. x 1 in. x 2-3 mils thick were coated with an aluminum evaporated layer 2000-3000 Å in thickness. Samples approximately 0.2 in. x 0.2 in. were cut from the sheets, giving a pre-irradiation capacitance of roughly 50 pF.

The dc conductivity was determined by measuring the current drawn by the sample from a 6-V dry cell with a Boonton microammeter. The capacitance was measured by a General Radio type 716-C impedance bridge. To get sufficient Q to operate the bridge accurately, the measuring frequency was set at 100 kc/sec (the highest conductivity ferrite required 300 kc/sec). To insure constant and reproducible temperature and a high Q the measurements are made with the sample cooled in a double thermal bath as shown in Fig. 41.

Two separate runs were made with the capacitor samples. In Run I the leads were attached to the sample (using a tin-zinc solder), initial measurements made, leads removed, samples irradiated, leads re-attached, and samples re-measured. Also, the inner thermal bath contained silicone oil rather than n-hexane as shown in Fig. 41. In Run II the aluminum leads were left attached throughout and the inner thermal bath was changed to the n-hexane.

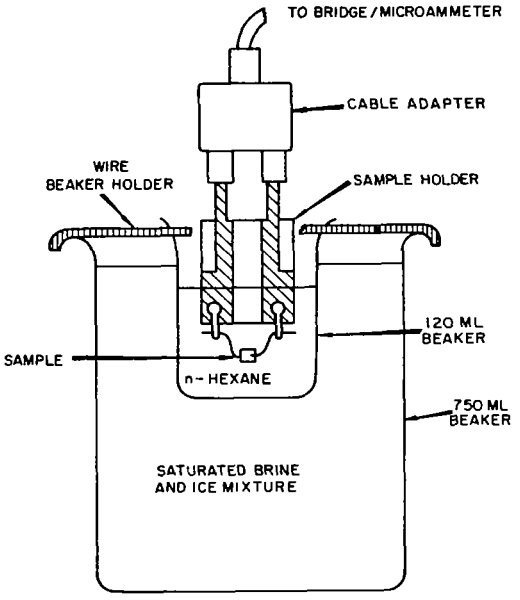


Fig. 41. Double thermal bath.

4. Experimental Results and Discussion

a. Magnetic Properties - Percentage changes in the hysteretic properties B_r and H_c (see Fig. 40) are presented in Figs. 42 to 49 for the four ferrites, namely ferrite A air-quenched and nitrogen-annealed, respectively, and ferrite B air-quenched and nitrogen-annealed, respectively. The percentage changes are computed according to the relationship:

$$\frac{B_r' - B_r}{B_r} \times 100 \qquad (1)$$

where B_r' is the remanent flux density after irradiation and B_r is the remanent flux density before irradiation. An analogous relationship is used for H_c.

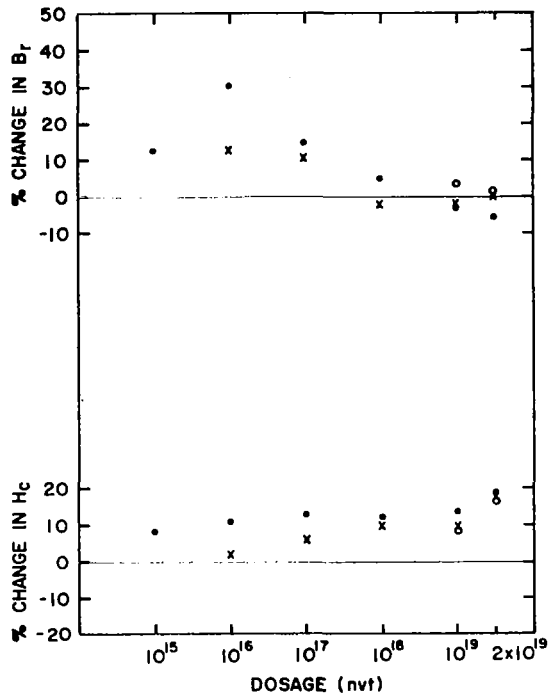


Fig. 42.
Changes of B_r and H_c in Ferrite A (air-quenched) as a function of irradiation.

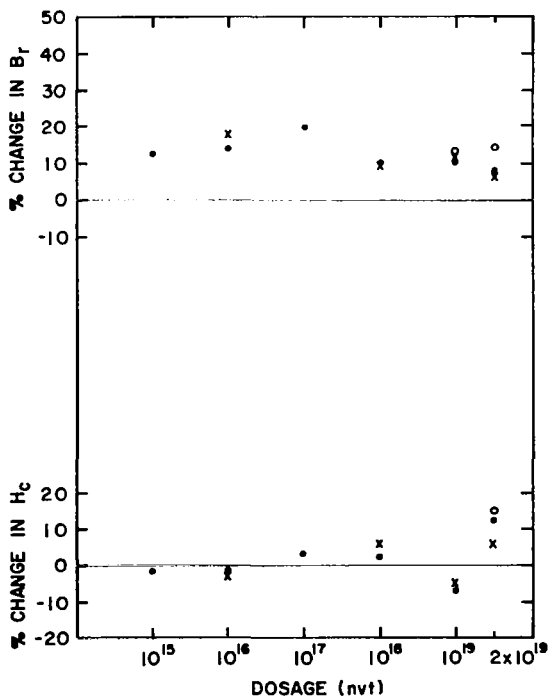


Fig. 43.
Changes of B_r and H_c in Ferrite A (nitrogen-annealed) as a function of irradiation.

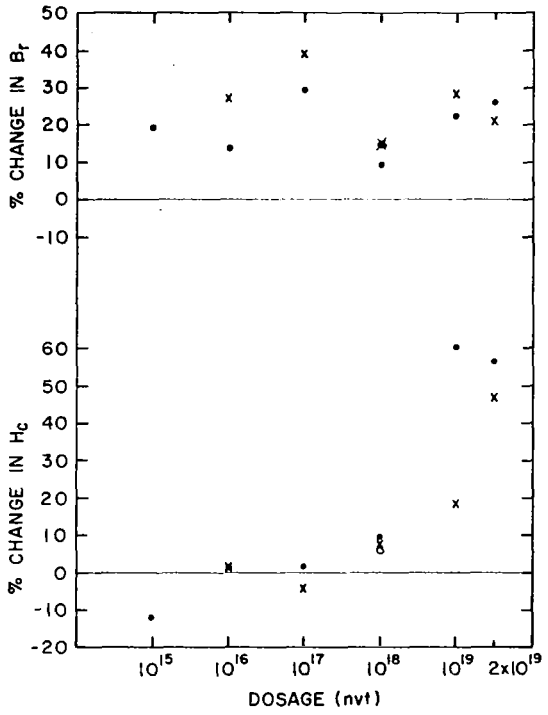


Fig. 44.
Changes of B_r and H_c in Ferrite B (air-quenched) as a function of irradiation.

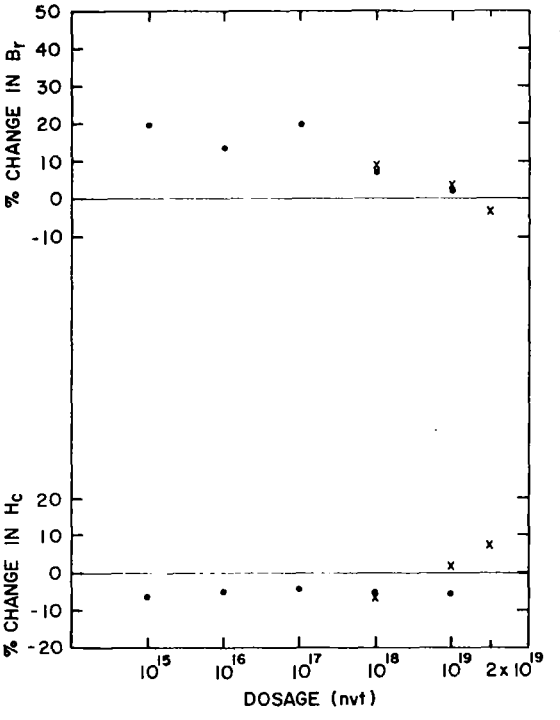


Fig. 45.
Changes of B_r and H_c in Ferrite B (nitrogen-annealed) as a function of irradiation.

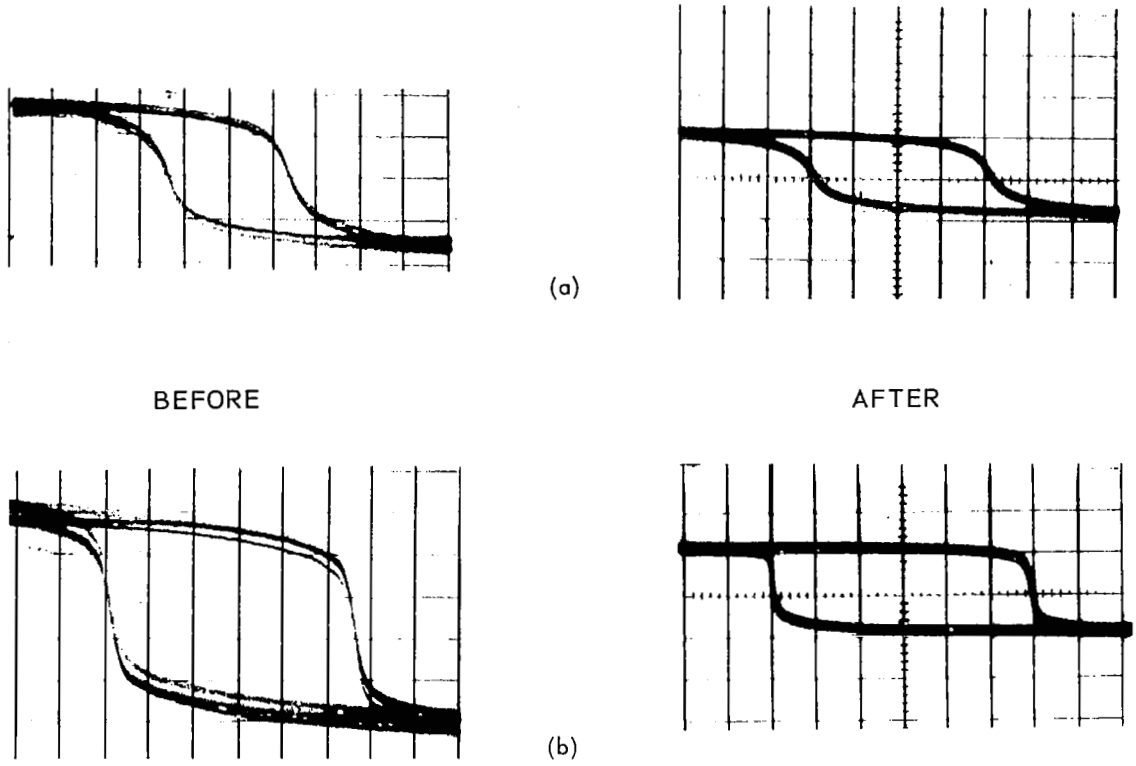


Fig. 46. Hysteresis loops for Ferrite B before and after irradiation to 2×10^{19} nvt.
(a) Air-quenched, drive = 0.88 A-turns rms.
(b) Nitrogen-annealed, drive = 0.77 A-turns rms.
Vert. scales: 20 mV/div except where noted.

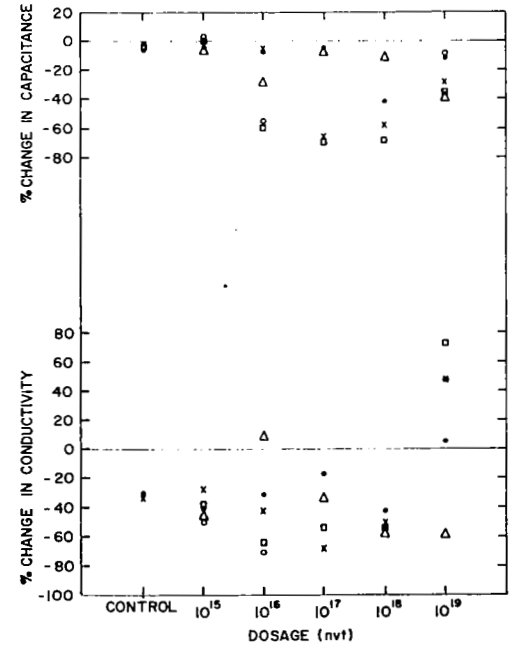


Fig. 47.
Changes in conductance and capacitance in Ferrite A (air-quenched) as a function of irradiation.

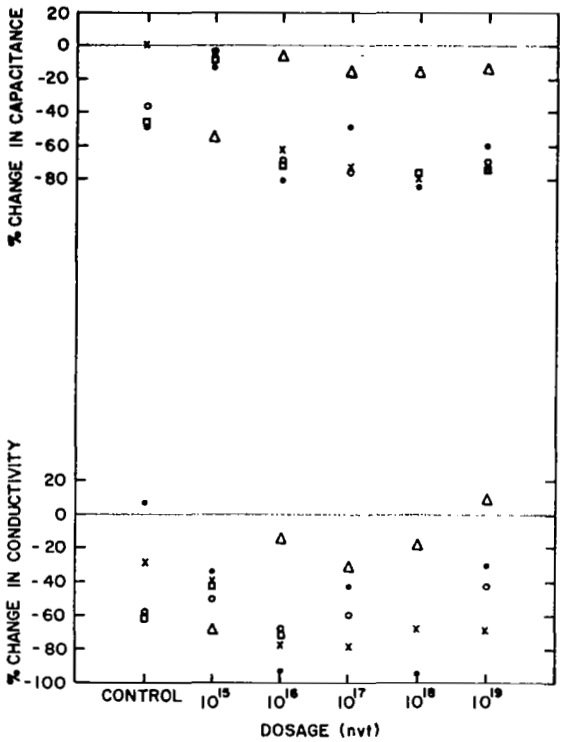
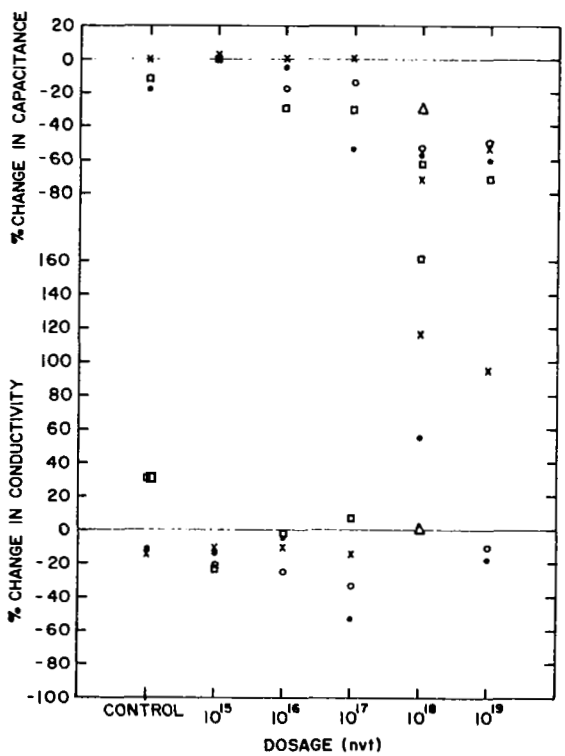


Fig. 48.
Changes in conductance and capacitance in Ferrite A (nitrogen-annealed) as a function of irradiation.

Fig. 49.
Changes in conductance and capacitance in Ferrite B (air-quenched) as a function of irradiation.



The numbers corresponding to the data points in Figs. 42 to 50 are given in Tables IX and X. The data points in the figures are indicated by black

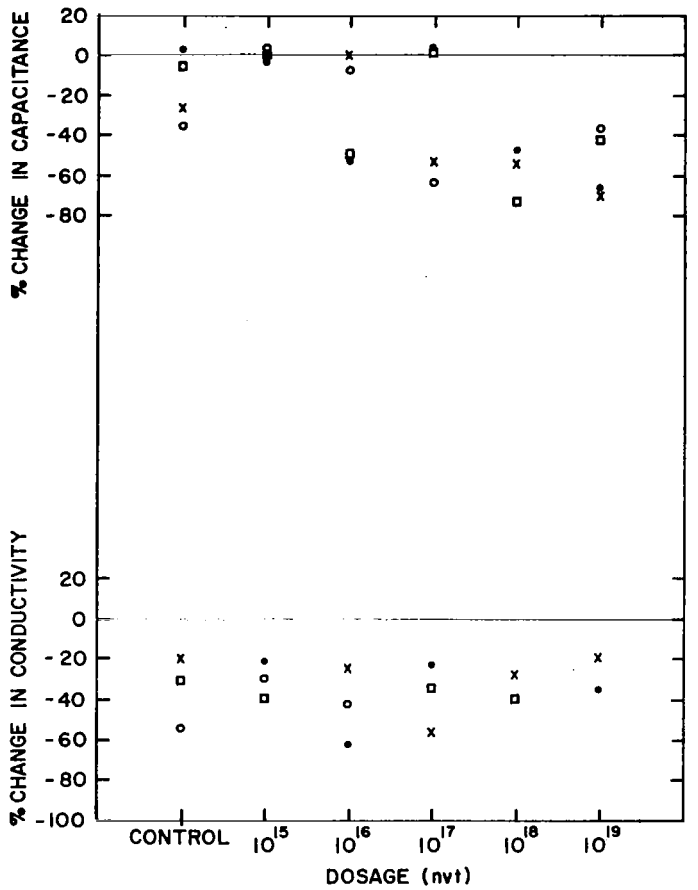


Fig. 50. Changes in conductance and capacitance in Ferrite B (nitrogen-annealed) as a function of irradiation.

dots, circles, and crosses to differentiate between the different toroidal samples subjected to the same neutron exposure. For instance, on the graphs of Fig. 42 the two crosses at 10^{18} nvt correspond to the change in B_r and H_c in one sample and the dots at 10^{18} nvt correspond to the changes in another sample. A given symbol at the dosage 2 x 10^{19} nvt is for the same sample as the corresponding symbol at 10^{19} nvt, (e.g., the four black dots at 10^{19} nvt and at 2 x 10^{19} nvt are for the same sample exposed in two separate runs of 10^{19} each). This correspondence does not hold at any of the other dosages.

The possible sources of error in this experiment are:

1. Numerical interpretation of oscillograms
2. Changes in room ambient temperature
3. Gain drift in electronic circuitry
4. Error in reproducing driving currents

TABLE IX

RADIATION EFFECTS ON FERRITE A - MAGNETIC PROPERTIES

	Sample #	Dosage nvt	%Change B_r	%Change H_c
Air-Quenched	10	10^{15}	12.8	8.5
	8	10^{16}	30.6	11.0
	9	10^{16}	12.5	2.1
	6	10^{17}	15.3	12.8
	7	10^{17}	10.8	6.2
	4	10^{18}	5.0	12.2
	5	10^{18}	-2.4	9.8
	1	10^{19}	3.6	12.8
	2	10^{19}	-3.3	13.7
	3	10^{19}	-2.3	9.6
	1	2×10^{19}	1.2	17.0
	2	2×10^{19}	-5.5	17.9
	3	2×10^{19}	0	18.0
Nitrogen - Annealed	30	10^{15}	12.3	-1.3
	28	10^{16}	17.8	-2.5
	29	10^{16}	14.3	-1.3
	27	10^{17}	20	3.6
	24	10^{18}	15	2.4
	25	10^{18}	14.6	6.3
	21	10^{19}	11.7	-5.7
	22	10^{19}	12.5	-5.9
	23	10^{19}	10	-6.3
	21	2×10^{19}	5.9	5.7
	22	2×10^{19}	14.3	15.3
	23	2×10^{19}	8.3	12.5

TABLE X

RADIATION EFFECTS ON FERRITE B - MAGNETIC PROPERTIES

	Sample #	Dosage nvt	%Change B_r	%Change H_c
Air-Quenched	45	10^{15}	19	-11.9
	43	10^{16}	27.5	1.5
	44	10^{16}	13.6	1.5
	41	10^{17}	29.4	1.3
	42	10^{17}	38.9	-4.4
	14	10^{18}	14.8	7.4
	15	10^{18}	14.8	5.4
	17	10^{18}	9.5	9.3
	12	10^{19}	28.3	17.8
	13	10^{19}	22.2	60.4
	12	2×10^{19}	20.8	46.5
	13	2×10^{19}	25.9	56.6
Nitrogen - Annealed	39	10^{15}	20.5	-6
	38	10^{16}	13.9	-4.9
	37	10^{17}	20	-4.1
	35	10^{18}	8.4	-6.5
	36	10^{18}	7.5	-4.9
	32	10^{19}	2.5	-5.5
	33	10^{19}	3.6	1.8
	33	2×10^{19}	-3.6	7.3

Individually, none of these errors would be expected to exceed ± 5 percent. According to the literature one would expect insignificant changes at least over the range of 10^{15} - 10^{17} nvt. Thus, these points serve as a rough calibration.

Figures 42 and 43 indicate insignificant changes in the flux density B_r of ferrite A after exposures as high as 2×10^{19} nvt.* Its coercive force H_c increases by roughly 10 percent at 2×10^{19} nvt. Ferrite B also shows significant changes in B_r over the full dosage range, as seen in Figs. 44 and 45. The coercive force of the air-quenched form of ferrite B increases by about 50 percent at 2×10^{19} nvt while the H_c of the nitrogen-annealed form remains essentially constant. This difference may be due to neutron-induced stress relief in the quenched ferrite.

The shapes of the loops before and after irradiation were remarkably similar, as illustrated by Fig. 46.

To summarize, integrated neutron dosages as high as 2×10^{19} nvt can be tolerated by these ferrite without significantly altering the magnetic properties, with the sole exception of the air-quenched form of ferrite B.

b. Electric Properties - Percent changes in the capacitor terminal properties--capacitance C, and dc conductivity G are given in Figs. 47 to 50 for the four ferrite types. The percent changes are computed analogously to Equation (1). Numbers corresponding to the data points in Figs. 47 to 50 are given in Tables XI, XII, XIII, and XIV. The data include control samples all of which were produced at the same time as the irradiated samples. Some of these controls were heated at 225°C for 90 hours.

Most of the data in the figures correspond to Run II where the leads were left attached. The data points corresponding to Run I are indicated by triangles. The remaining symbols are used simply to differentiate between the various samples of the same ferrite type subjected to the same neutron exposure.

The possible sources of error in this experiment are:

1. microammeter reading
2. bridge reading
3. null location for capacitance bridge
4. temperature reproducibility
5. sneak conduction paths via sample holder
6. deterioration of aluminum contacts.

The first three should not lead to a total error of more than 5 to 10%. The nominal bath temperature is -8.5°C. The measured variation is -9°C to -7.5°C. The temperature variation of ferrite conductance is approximately 20 percent over the 1.5°C range. The fifth item, sneak conduction, is particularly noticeable in remeasuring irradiated samples. The person moving samples

* The anomalous point at 10^{16} nvt in Fig. 42 is probably due to an error in the number of secondary turns used to obtain the B-H loop. For that sample the original B_r value is considerably lower than for similar samples.

TABLE XI

RADIATION EFFECTS ON FERRITE A (AIR-QUENCHED)
ELECTRICAL PROPERTIES

Sample #	Dosage nvt	%Change C	%Change μA
7	10^{15}	- 3.9	-41.2
18	10^{15}	0	-38.0
20	10^{15}	0	-28.5
22	10^{15}	+ 2.6	-51.0
13	10^{16}	-55.8	-71.2
14	10^{16}	-58.7	-64.5
15	10^{16}	- 4.1	-42.8
19	10^{16}	- 6.9	-32.4
12	10^{17}	- 4	-17.5
28	10^{17}	-65	-69.0
34	10^{17}	-68.7	-53.8
10	10^{18}	-68.5	-53
16	10^{18}	-57.5	-51.1
17	10^{18}	-41	-42.4
5	10^{19}	-11.1	+ 4.9
6	10^{19}	-28	+46.7
9	10^{19}	-35.4	+72.5
11	10^{19}	- 7.8	+45.8
40	control	- 5.9	-31
30	heated control	- 2.8	-34.2
39	heated control	- 4.5	---

TABLE XII

RADIATION EFFECTS ON FERRITE A

(NITROGEN-ANNEALED) ELECTRICAL PROPERTIES

Sample #	Dosage nvt	%Change C	%Change μA
18	10^{15}	-12.8	-34.2
19	10^{15}	- 3.8	-50
23	10^{15}	- 4.9	-41.3
24	10^{15}	- 7.7	-40.5
9	10^{16}	-80.4	-93
22	10^{16}	-62	-76.8
32	10^{16}	-71.5	-70
36	10^{16}	-68	-68.8
10	10^{17}	-48.4	-42.5
25	10^{17}	-72.9	-77.8
27	10^{17}	-72.6	-58.4
13	10^{18}	-84	-95.5
26	10^{18}	-77	---
28	10^{18}	-79	-68
16	10^{19}	-59.5	-30.4
17	10^{19}	-74	---
29	10^{19}	-70.2	-43.5
30	10^{19}	-71.4	-69.6
20	control	-36.2	-58.7
40	control	0	-29.4
34	heated control	-46.1	-60
39	heated control	-47.6	+ 6.7

TABLE XIII

RADIATION EFFECTS ON FERRITE B

(AIR-QUENCHED) ELECTRICAL PROPERTIES

Sample #	Dosage nvt	%Change C	%Change μA
9	10^{15}	0	- 14.3
14	10^{15}	+ 1	- 23.4
17	10^{15}	+ 2.6	- 10.7
25	10^{15}	0	- 22
10	10^{16}	- 4.7	- 3.9
36	10^{16}	-18.2	- 2.5
37	10^{16}	-29.2	- 2.2
39	10^{16}	0	- 10.9
2	10^{17}	0	- 15
6	10^{17}	-53.4	- 52.7
23	10^{17}	-31.2	+ 7
30	10^{17}	-14.3	- 33.4
7	10^{18}	-72.1	+117
12	10^{18}	-56.7	+ 55
16	10^{18}	-61.8	+162
24	10^{18}	-53.2	--
3	10^{19}	-50.7	- 11.1
19	10^{19}	-60.5	- 18
26	10^{19}	70.7	--
29	10^{19}	-52.4	+ 94.5
27	control	-18.1	- 11.1
32	control	0	- 14.7
40	heated control	-11.8	+ 31.3

TABLE XIV

RADIATION EFFECTS ON FERRITE B (NITROGEN-ANNEALED)

ELECTRICAL PROPERTIES

Sample #	Dosage nvt	%Change C	%Change μA
15	10^{15}	- 2.1	-20.9
22	10^{15}	0	---
24	10^{15}	0	-41.4
35	10^{15}	+ 2.1	-30.6
3	10^{16}	0	-25
4	10^{16}	-53.4	-61.8
9	10^{16}	-48	---
13	10^{16}	- 8.2	-42.5
6	10^{17}	+ 4.1	-22.8
8	10^{17}	-53	-57
11	10^{17}	+ 1.8	-34.7
20	10^{17}	-63.5	---
16	10^{18}	-72.6	-39.6
37	10^{18}	-54.5	-27.8
39	10^{18}	-47.6	---
27	10^{19}	-65.7	-35.2
29	10^{19}	-69.6	-19.5
30	10^{19}	-36.4	---
34	10^{19}	-42.6	---
17	control	-26.2	-20
23	control	+ 2.71	---
7	heated control	-35.6	-55
18	heated control	- 6.30	-30.4

in and out of the sample holder wears disposable polyethylene gloves as a precaution against radioactive contamination. These gloves readily pick up contaminants which can be brushed off on to the sample holder leading to sneak currents as high as several microamperes. When this effect was noted during the second run the conductances were remeasured, periodically checking the sneak current to insure that it was well below 0.1 μA. However, it is possible that these sneak currents were present to some extent in the pre-irradiation measurements. They were not large then, however, because some samples had original currents of 0.4 to 0.5 μA. In addition, the samples chosen for irradiation had a high degree of consistency in both their capacitance and conductance.

The last error source, contact deterioration, is by far the most significant. This deterioration is not attributable solely to neutron and gamma flux because samples that were not exposed had the same sort of symptoms, although not as often and not to such extremes. The scope of the effects on unexposed samples is shown in Fig. 51. The sample in Fig. 51(c) has been heated to 225°C in air for 90 hours. The other three were aged at room ambient. As a precaution,

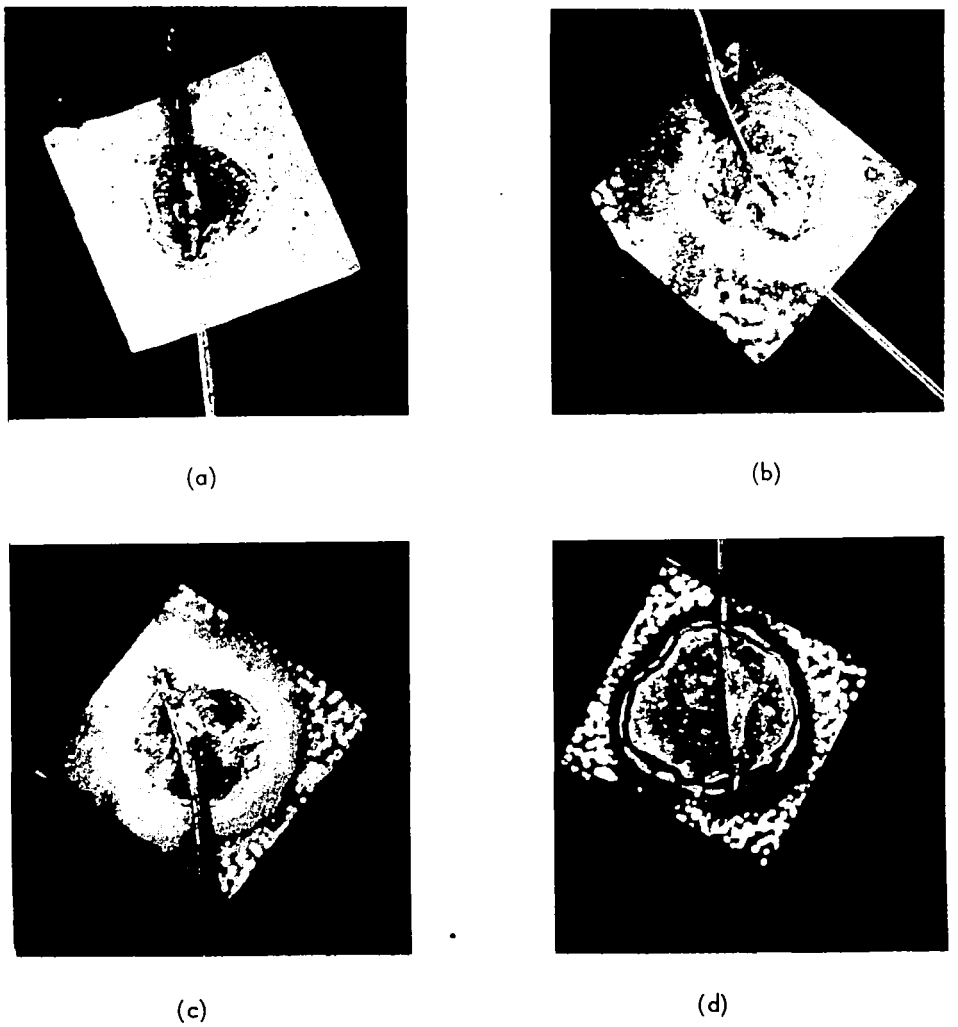


Fig. 51. Aging effects on aluminum contact appearance.

it should be noted that the photos overemphasize the gradations in darkness because of the high contrast prints. The dark regions in Fig. 51 (d) appear visually only as dark as the dark regions in Fig. 51(b). The sample shown in Fig. 51(a) is normal in appearance, i.e., like a freshly made sample. Since the samples have high resistance (200 kΩ and up), the contact can be quite poor before the conductance and capacitance measurements are affected. However, in a case like Fig. 51(d) the dark ring around the solder area can be a total interruption in aluminum continuity, thus reducing the contact area quite significantly. This results in a large percentage drop in both capacitance and conductance. Many of the experimental samples showed such a drop in both capacitance and conductance, as illustrated in Figs. 47 to 50. Since the physical mechanisms for conductance and capacitance in solids are quite different, it is improbable that a given neutron dose would affect both properties by the same percent and in the same direction. It is therefore likely that samples which suffered roughly equal drops in capacitance and conductivity (for example, the "cross" at 10^{17} nvt in Fig. 50) did so because of contact deterioration.

To summarize, large downward changes (> 10 percent) in capacitance can be caused by contact deterioration and/or the effect of neutrons and gamma rays on the material dielectric constant. Downward changes in conductivity can be due to some combination of contact deterioration, temperature change, and the effect of radiation on ferrite conductivity. Upward changes in conductivity can be due to temperature change and/or the effect of radiation on ferrite conductivity.

Figures 47 and 48 indicate insignificant changes in the dielectric constant of ferrite A. The conductance of ferrite A increases by about 50 percent for the air-quenched form and by about 20 percent for the nitrogen-annealed form at 10^{19} nvt.

Figures 49 and 50 indicate downward changes in dielectric constant by 20 to 40 percent for ferrite B at 10^{18} nvt with no further change at 10^{19} nvt. The conductance of ferrite B in air-quenched form roughly doubles at 10^{18} nvt while the nitrogen-annealed version changes little.

The general trend for moderate increases in conductance may be the result of a secondary effect. We do know that the conduction in all these ferrites is n-type, i.e., it is primarily due to electronic transport. For high-resistivity ferrites, such as ferrites A and B, the iron ions present must be ferric. If the neutron and gamma flux cause oxidation of the aluminum film, some of this oxygen may be drawn from the ferric ions, thus changing them to ferrous and thereby increasing the conductivity via the mechanism of electron hopping between ferric and ferrous ions.

To summarize, the changes in electric properties of these ferrites after exposure to 10^{19} nvt are not large enough to affect memory operation, because the memory performance is not very sensitive to moderate changes in these properties.

C. RADIATION STUDIES ON MOS TRANSISTORS

1. State of the Art

Relatively few radiation studies have been conducted on silicon field-effect transistors. Most studies are on the reverse-biased p-n junction gate variety. Comparisons between this type and planar bipolar silicon (conventional) transistors do not give a true picture because of their different constructions.

Most of the performance degradation (current gain reduction) in bipolar transistors is due to a reduction of the minority-carrier lifetime and can therefore be minimized through the use of a thin base region as used in high-frequency diffused-base transistors. Field-effect transistors are majority-carrier devices and do not suffer from minority-carrier lifetime problems. Radiation at high levels ($> 10^{15}$ nvt) reduces the majority-carrier mobility and therefore the transconductance of the field-effect transistor. Metal-oxide semiconductors (MOS) insulated-gate field-effect transistors also suffer from possible charge build-up in the oxide layer thus shifting the transfer characteristic (drain current versus gate voltage). Secondary effects may cause an increase in the leakage of the gate junctions or the insulated gate and the source and drain junctions.

Different types of radiations result in different amounts of damage to the semiconductor devices. Table XV shows the relative effectiveness of the various types of radiations.[14] The accuracy is no better than a factor of 2 to 3. For reasons of easy availability, most radiation studies in the literature use neutron or electron bombardment.

S. M. Christian of RCA Laboratories irradiated several MM765 reverse-biased gate field-effect transistors, which can also be operated as pnp bipolar transistors.* While the field-effect mode is not affected by a dose as high as 10^{14} nvt, the bipolar operation shows degradation at levels as low as 10^{12} nvt. (This does not mean that radiation-resistant bipolar transistors cannot be designed to stand 10^{14} nvt radiation levels.)

Initial neutron radiation studies up to 10^{15} nvt conducted by S. M. Christian on MOS full-gate low-level logic transistors showed data widely scattered. Some performance degradation was noted at doses slightly higher than those tolerated by high-frequency bipolar transistors.

C. Gross and C. Fales[15] have observed a drain current decrease of various degrees on RCA experimental n and p enhancement type MOS transistors. These transistors were exposed to 22-MeV protons, 0.3 and 2-MeV electrons. N-type channel units did not degrade with 0.3 MeV electrons at a dose of 3×10^{16} el/cm^2. However, they degraded to 70 percent I_{drain} with 2-MeV electrons at a dose of 4×10^{15} el/cm^2. Bombardment with 22-MeV protons reduced the drain current to 70 percent of its original value at a dose of 2.5×10^{11} p/cm^2.

* S. M. Christian; to be published a chapter in Field-Effect Transistor Physics, Devices, Fundamental and Applications, Prentice Hall, Inc.

TABLE XV

RELATIVE EFFECTIVENESS OF NUCLEAR PARTICLES AT VARIOUS ENERGIES FOR PRODUCING DISPLACEMENT DAMAGE IN SILICON AND GERMANIUM

Particle	Energy (MeV)	Relative Effectiveness for Silicon	Relative Effectiveness for Germanium
Thermal Neutron	2.5×10^{-8}		3.1×10^{-3}
Fission Neutron	1 to 2	1.0	1.0
Neutron	4.8		1.2
Neutron	14		0.8
Gamma Photon	1.25	4×10^{-5}	4×10^{-5}
Electron	0.3	2.5×10^{-4}	
Electron	1.0	5×10^{-3}	
Electron	4.5	0.02	0.02
Proton	17.6	1.2	
Proton	110	0.4	
Proton	740	0.6	
Deuteron	9.6	1.0	200
Alpha	40	10	

H. L. Hughes and R. R. Giroux[16] recently published degradation results of commercial n- and p-type MOS transistors for $Cobalt^{60}$ gamma irradiation. 10^6 rads absorbed radiation reduced transconductance to less than one third of its original value. In none of the articles mentioned above was the effect of afterexposure annealing studied.

2. Device Geometry and Device Properties

For operating a laminated ferrite memory, driver MOS transistor strips with center-to-center spacings of 10 mils are required. A top view of such a unit is shown in Fig. 52. Several segments of the MOS driver strip were mounted in 10-lead TO5 headers with 4 drain, 4 gate, 1 common source, and 1 substrate contacts. As little gold as possible was used to avoid the radiation of the slowly decaying Au^{198} (half-life 2.70 d). Each can contains four n-type enhancement MOS transistors with a channel width of 120 mils, a channel length between 0.17 and 0.25 mil and a substrate resistivity of 10-Ωcm p-type.

In initial batches indium solder between the nickel-plated posts of the stem and the gold wire was used for thermocompression bonding. A typical drain current/drain voltage characteristic is shown in Fig. 53(a). The silicon dioxide is doped for device stabilization and device characteristics are usually reproducible at temperatures up to 100°C.

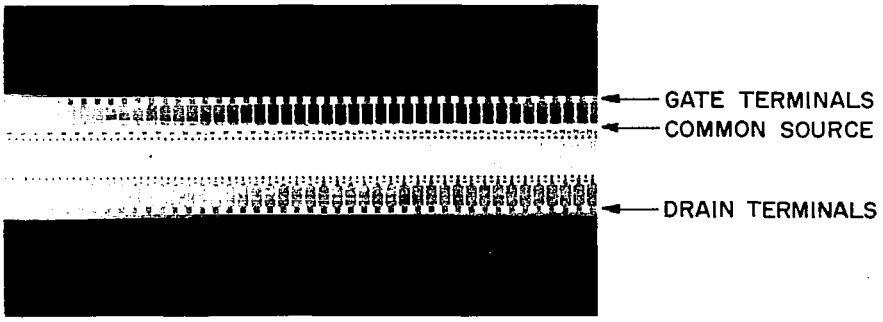


Fig. 52. Photomicrograph of 64-output MOS word switch (44 units shown).

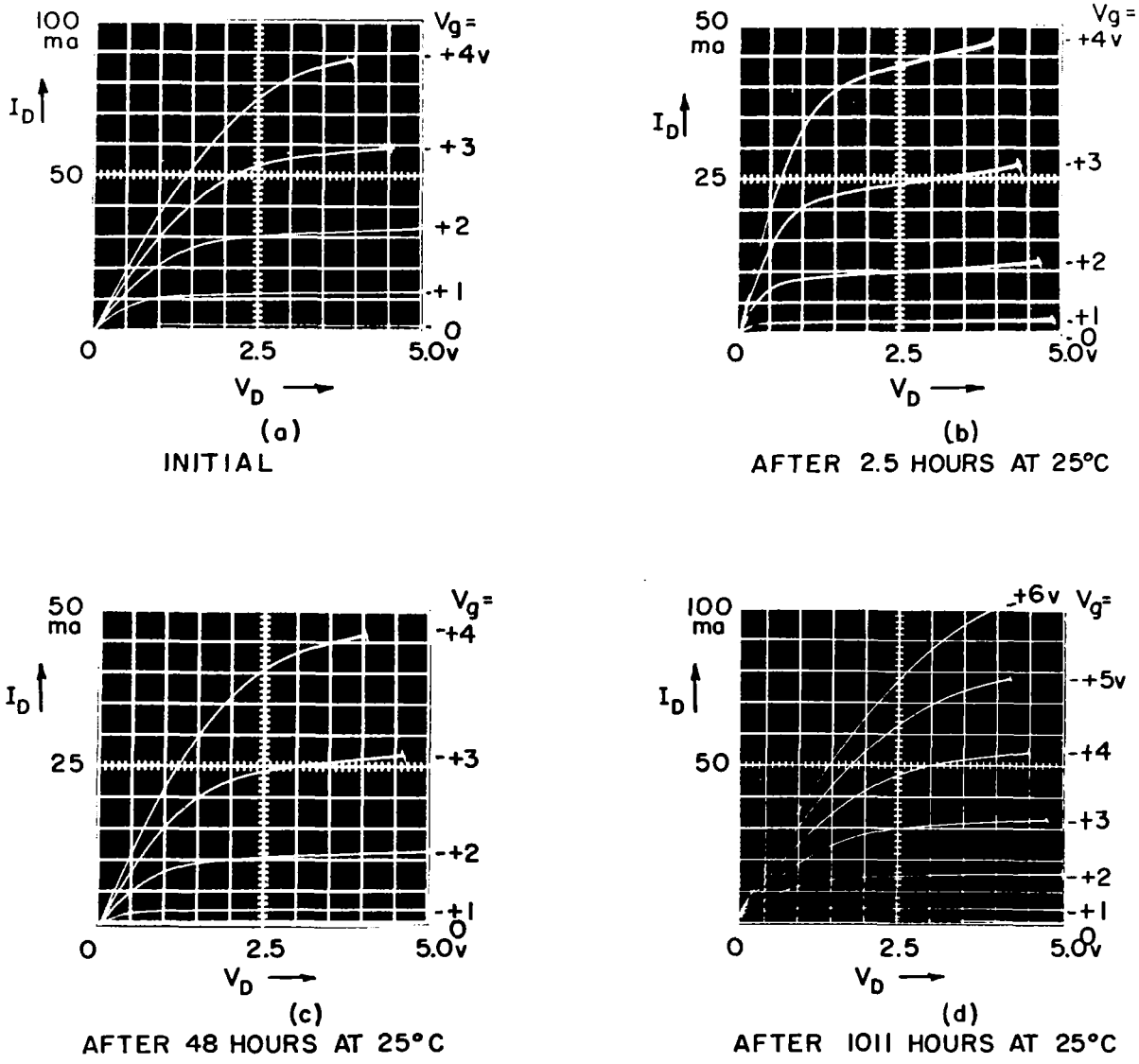


Fig. 53. Recovery of MOS driver transistor No. 8-2 after irradiation at 2×10^{14} neutrons/cm^2. (a) through (d) at room temperature.

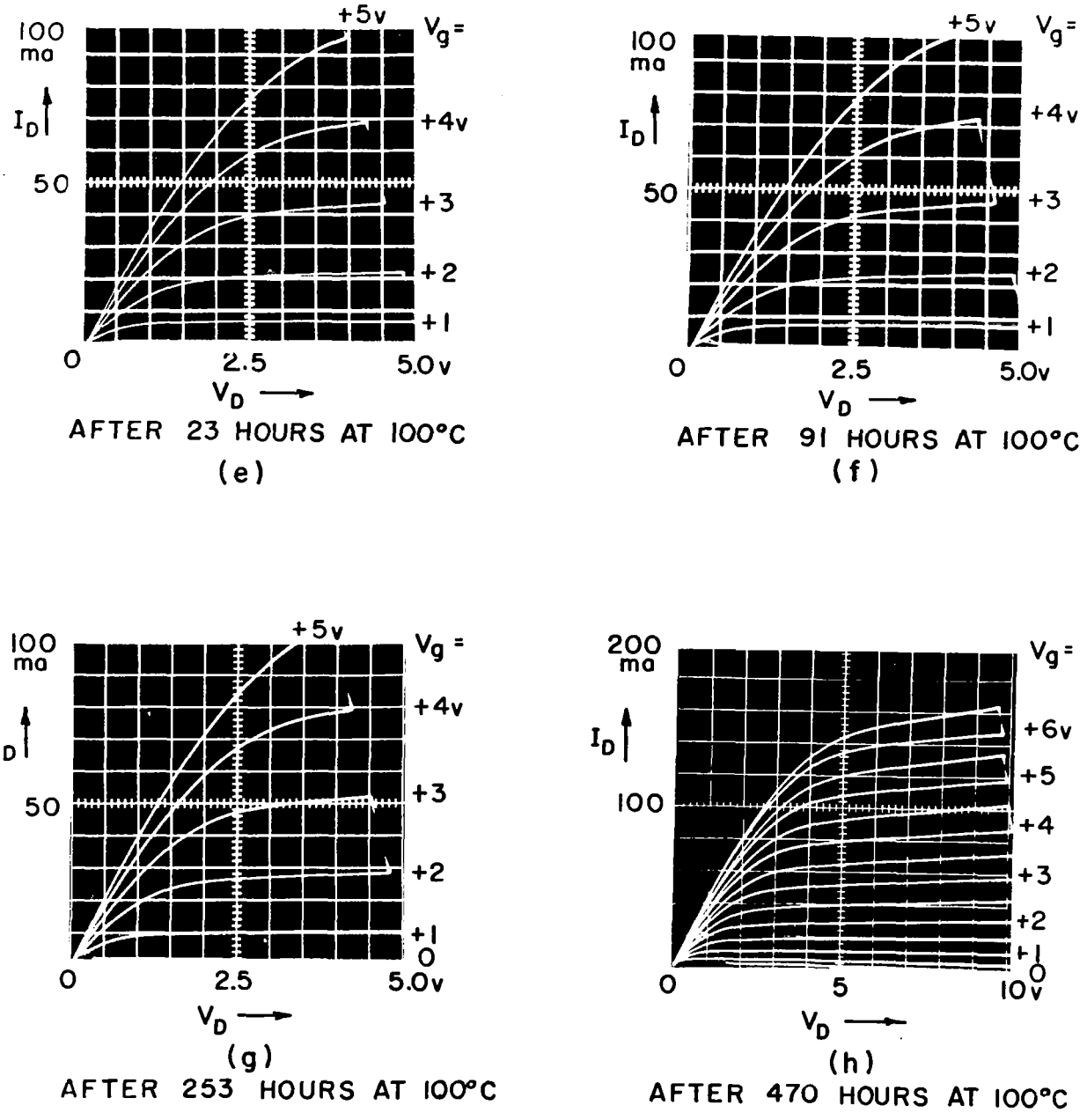
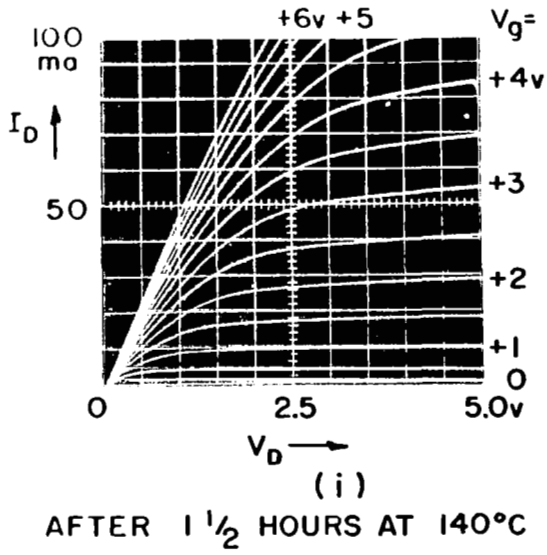
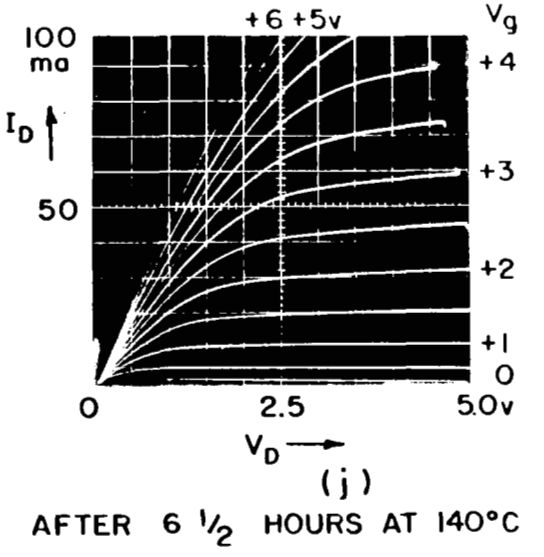


Fig. 53. Recovery of MOS driver transistor No. 8-2 after irradiation at 2×10^{14} neutrons/cm^2. (e) through (h) at 100°C.





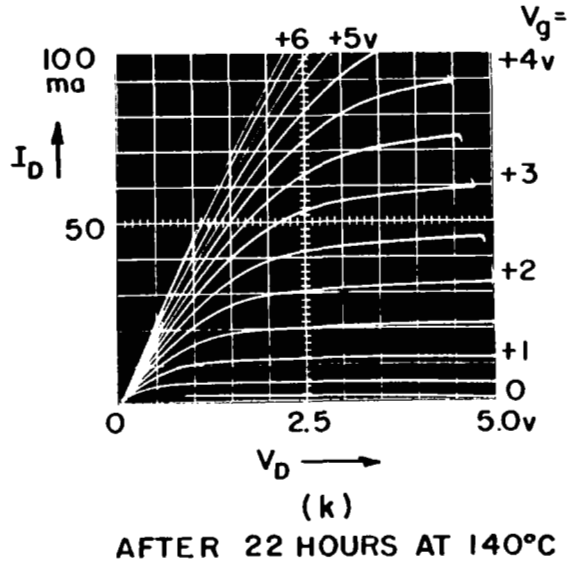


Fig. 53. Recovery of MOS driver transistor No. 8-2 after irradiation at 2×10^{14} neutrons/cm^2 (i) through (k) at 140°C.

3. Neutron-Radiation-Induced Effects

The same MOS transistors were subjected to increasing doses of neutron radiation up to the 3 x 10^{15} neutrons/cm^2. Figure 54 shows the effect of the different doses on the transfer characteristic. The measurements were taken 5 to 16 days after irradiation. The drain current decreases rather drastically with radiation level.

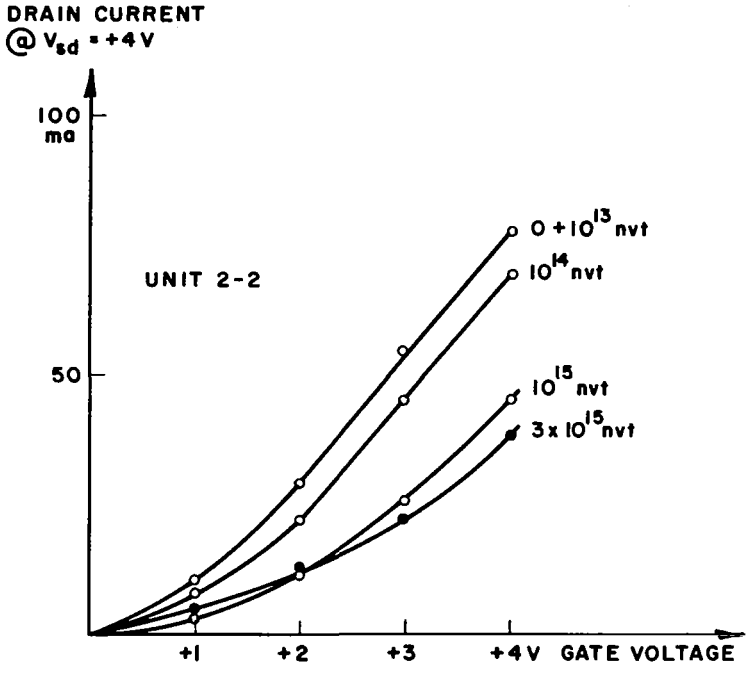


Fig. 54. Change of transfer characteristic of MOS driver as a function of radiation dose.

It soon became apparent that the intrinsic degradation is difficult to measure since annealing takes place after (and even during) exposure. A definite dependence on the location of the samples during irradiation was observed. MOS transistors in the pneumatic rabbit tube get less heating and fewer x-rays and show more degradation than units placed in the swimming pool close to the reactor core face. For the 3 x 10^{15} dose the samples were placed in the pool. The remaining data were obtained using the pneumatic tube.

From then on the device characteristics were measured as soon as it was possible to handle the radioactive units after exposure* and to monitor the data as a function of time at temperatures of 25°C, 100°C, and 140°C. Figure 53 shows the V-I characteristics at various stages of recovery, and Figs. 55 and 56 show the drain current of a typical unit as a function of time and temperature. Relatively fast recovery exists up to 10 hours at room temperature, after which it is very slow. Raising the temperature to 100°C leads to further recovery. A plot of the transfer characteristics (in this case $\sqrt{I_{drain}}$ vs. V_{gate}) is more meaningful and is plotted in Fig. 57. An offset voltage of about -0.9 volt is obtained by linearly extrapolating from large gate voltages. Exposure to 2 x 10^{14} neutrons/cm^2 shifts the transfer characteristic of this particular

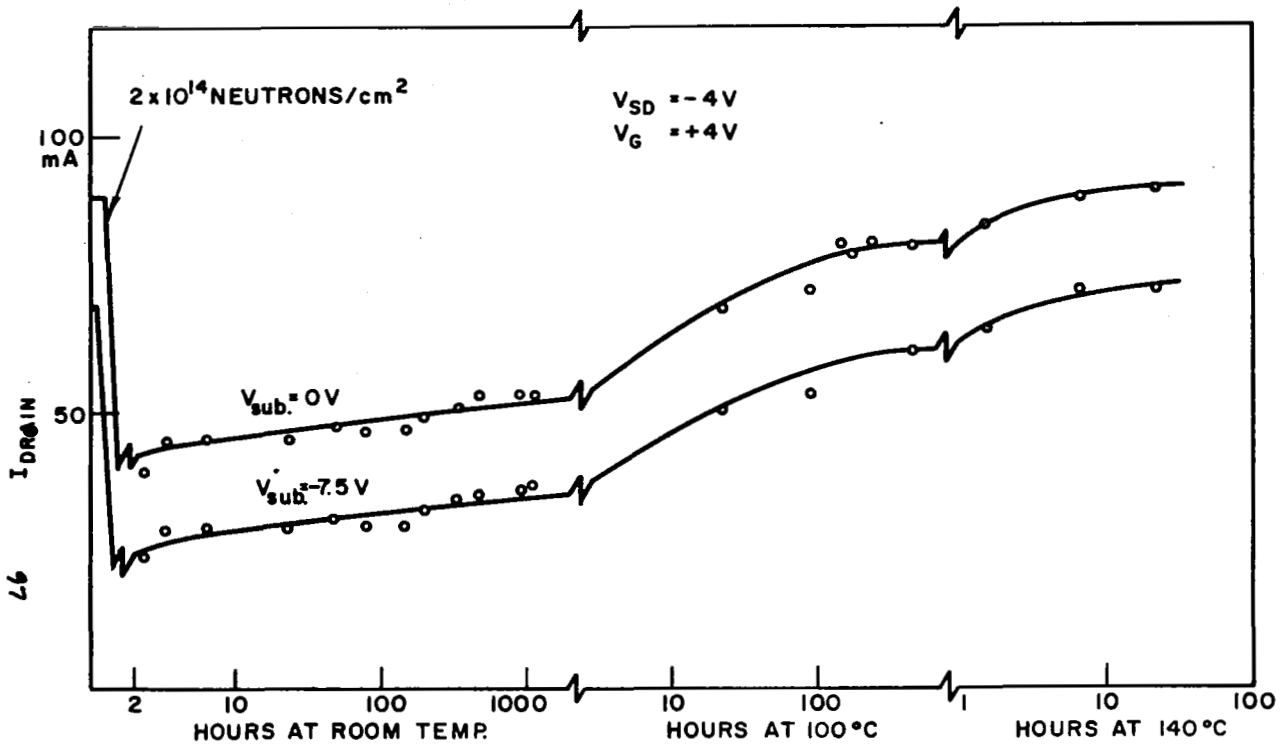


Fig. 55. Drain current of MOS transistor No. 8-2 as a function of time and temperature after 2×10^{14} neutrons/cm^2 irradiation.

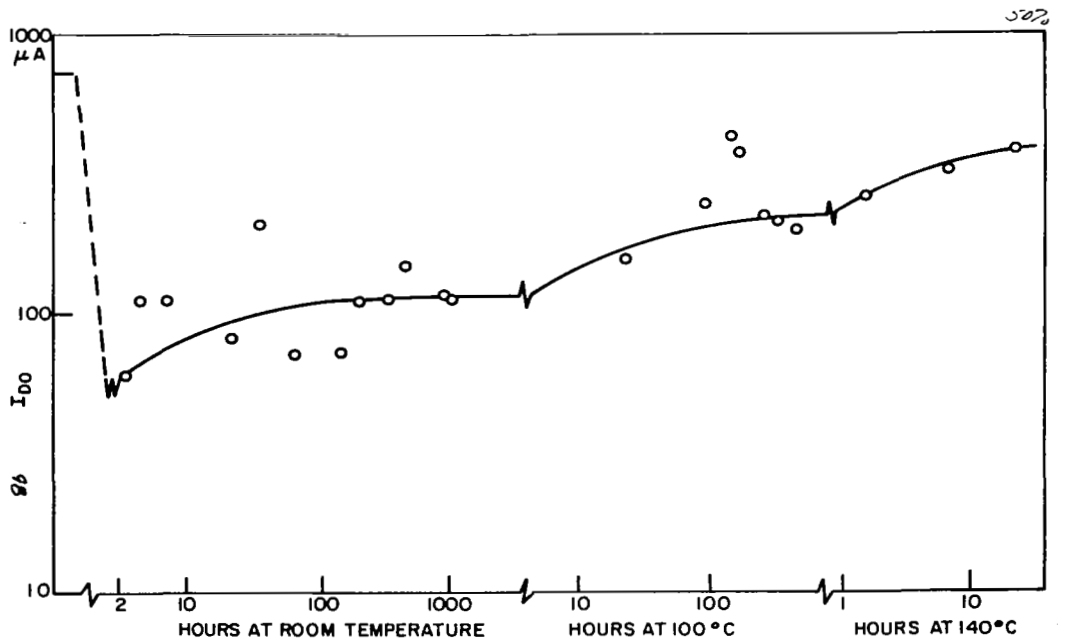


Fig. 56. Drain current at zero gate bias of MOS transistor No. 8-2 as a function of time and temperature after 2×10^{14} neutrons/cm^2 irradiation.

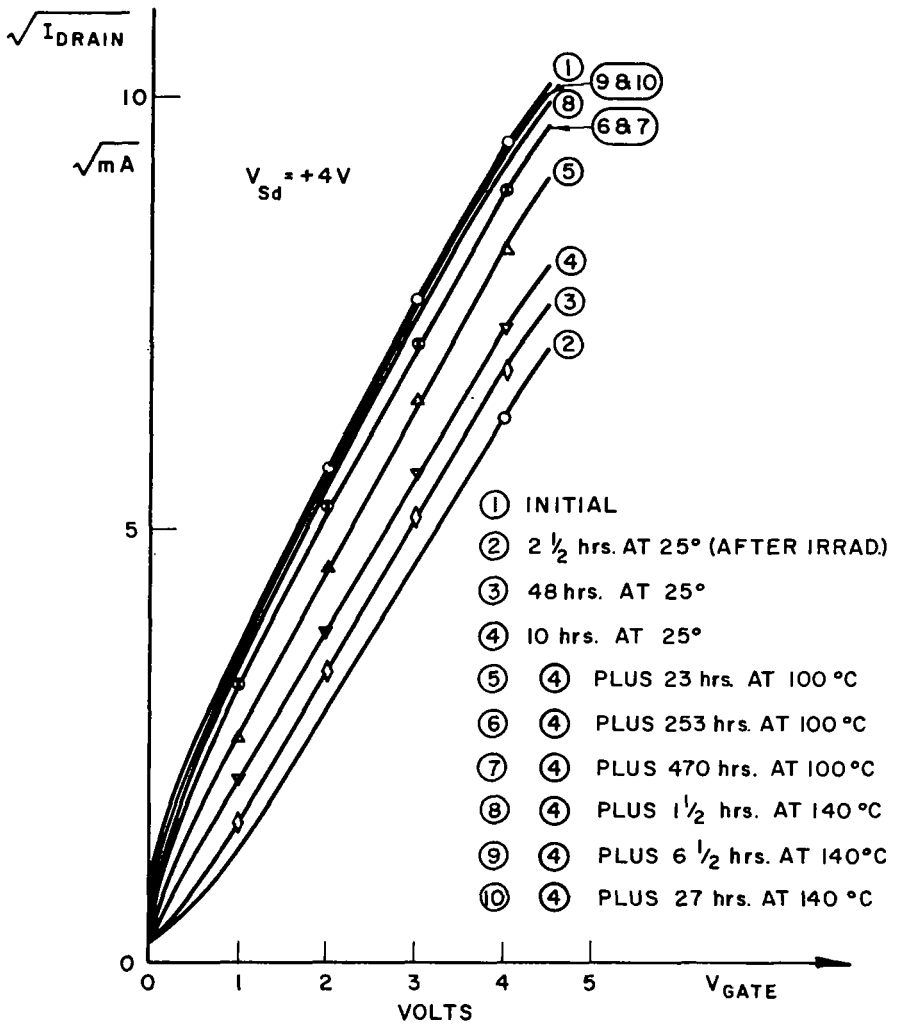


Fig. 57. Transfer characteristic of MOS transistor No. 8-2 as a function of temperature after 2×10^{14} neutrons/cm^2 irradiation.

unit by approximately + 1.6 volts (curve 2 in Fig. 57). Further annealing at room temperature shifts the transfer characteristic back by about -0.5 volt (curves 3 and 4 in Fig. 57). Annealing at 100°C increases the slope of the transfer characteristic, indicating an increase in channel mobility (curves 5-7 in Fig. 57). The MOS transistor improved further (curves 8-10 in Fig. 57). The units tested went through a maximum at 140°C but prolonged heating eventually reduced the drain current. Since this is true for irradiated transistors and nonirradiated control samples, the transistor cans were opened and severe metallurgical degradation was observed.

In Fig. 58, indium migration along the gold wires and onto some of the chromium-silver strip contacts can be seen. Capacitance measurements also confirm that only part of the MOS transistors (1, 3 and 4 shown in Fig. 58)

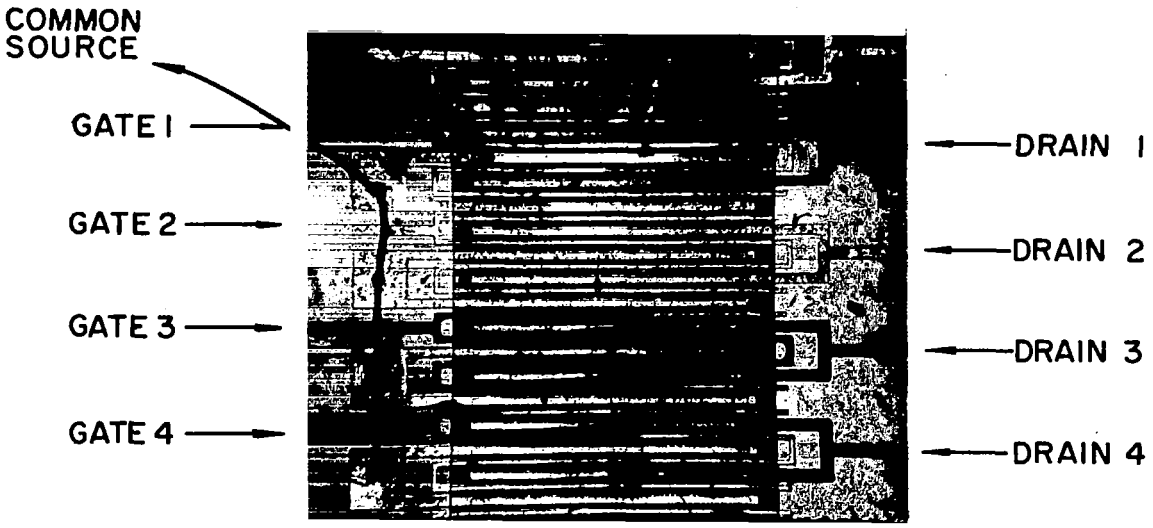


Fig. 58. Top view of MOS transistor No. 8-2 after 2×10^{14} neutrons/cm^2 irradiation and 22 hours at 140°C. Note that indium has migrated along the gold wires and partially along the chromium-silver strips, thus inactivating part of the transistor.

are still operating. During a relatively short annealing cycle at 140°C, the MOS transistors fully recovered (Fig. 57, curves 8-10), and in at least one carefully monitored case an increase in the slope of the transfer characteristic over and above the original value occurred, indicating a mobility increase after irradiation.

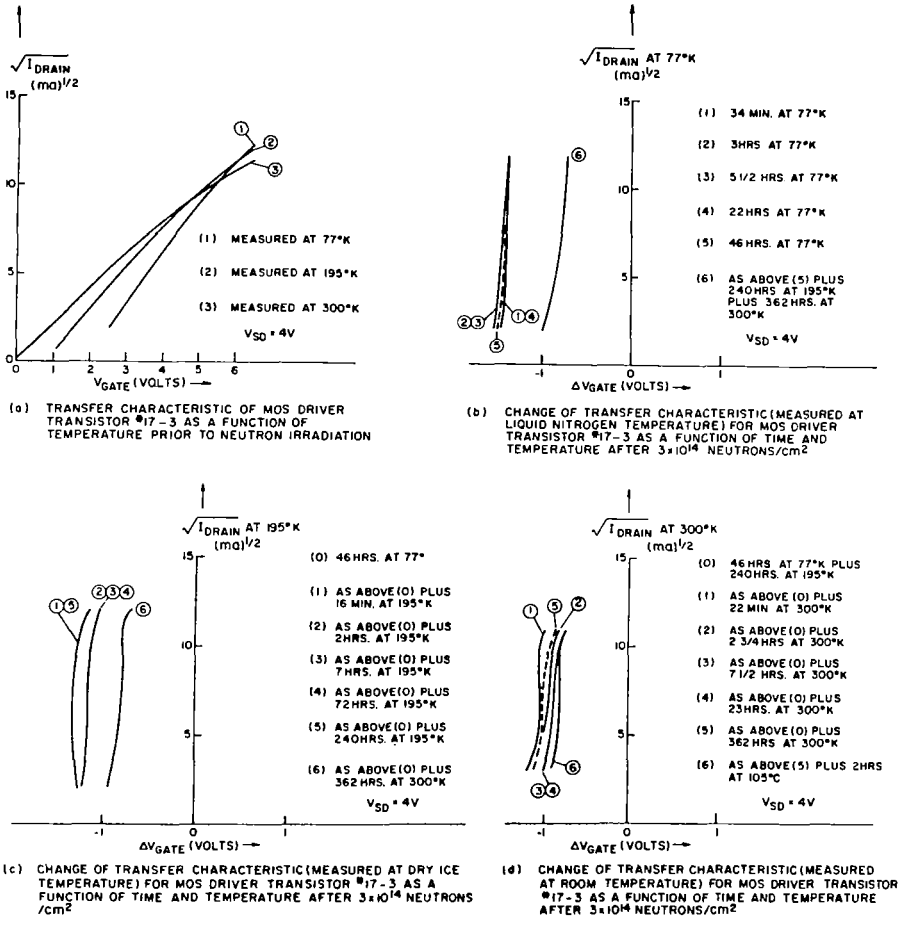
The indium migration was eliminated by partial gold-plating of the header leads and the use of regular thermocompression bonding. From the data presented, it is clear that annealing at room temperature plays an important role in recovering some or all of the electric properties of MOS transistors subjected to neutron irradiation.

By cooling the MOS transistors during and after the irradiation to low temperatures it should be possible to freeze the intrinsic radiation damage. Subsequent time-temperature cycles should give information about the activation energy and kinetics of the annealing process.

Several radiation experiments were run at dry-ice/freon and liquid-nitrogen temperatures. The MOS transistors, embedded in quartz wool for shock absorption and low thermal conductivity during the irradiation, were placed in a polyethylene pneumatic carrier tube. This tube was immersed into the cooling liquid for at least 3 to 4 hours before the irradiation experiment. Then the pneumatic carrier tube was sent into the reactor for a few seconds (to obtain 3×10^{14} neutron/cm^2). The MOS transistors were removed from the carrier tube immediately after the exposure and dropped into the cooling liquid again. As soon as the

radiation level was low enough (approximately 30 minutes after exposure) the first test was taken at the low temperature.

Only one experiment with eight MOS transistors was run at liquid-nitrogen temperature. The polyethylene carrier tube cracked, and two fragments returned from the pneumatic tube instead of one carrier tube. While the neutron irradiation was performed at the desired dose the experiment gave an ambiguous answer. Some samples (No. 17-3, Fig. 59 and No. 18-3, Fig. 60, for example)



(a) TRANSFER CHARACTERISTIC OF MOS DRIVER TRANSISTOR #17-3 AS A FUNCTION OF TEMPERATURE PRIOR TO NEUTRON IRRADIATION

(b) CHANGE OF TRANSFER CHARACTERISTIC (MEASURED AT LIQUID NITROGEN TEMPERATURE) FOR MOS DRIVER TRANSISTOR #17-3 AS A FUNCTION OF TIME AND TEMPERATURE AFTER 3×10^{14} NEUTRONS/cm^2

(c) CHANGE OF TRANSFER CHARACTERISTIC (MEASURED AT DRY ICE TEMPERATURE) FOR MOS DRIVER TRANSISTOR #17-3 AS A FUNCTION OF TIME AND TEMPERATURE AFTER 3×10^{14} NEUTRONS /cm^2

(d) CHANGE OF TRANSFER CHARACTERISTIC (MEASURED AT ROOM TEMPERATURE) FOR MOS DRIVER TRANSISTOR #17-3 AS A FUNCTION OF TIME AND TEMPERATURE AFTER 3×10^{14} NEUTRONS/cm^2

Fig. 59. Transfer characteristic for MOS driver transistor No. 17-3.

did not show any change in transfer characteristic for 46 hours in liquid nitrogen and at least up to 10 hours in a dry-ice bath (thus permitting all further neutron irradiations to be done at the latter temperature); other samples (No. 18-2, Fig. 61 for example) show a significant change in transfer characteristic between the two measurement points of 3 and 6 hours at liquid-nitrogen temperature.

In most samples, however, the maximum shift in transfer characteristic is about 1.5 volts. Predominantly, the shift is in the direction of negative gate bias, especially at low temperatures. There is some recovery (shift in positive

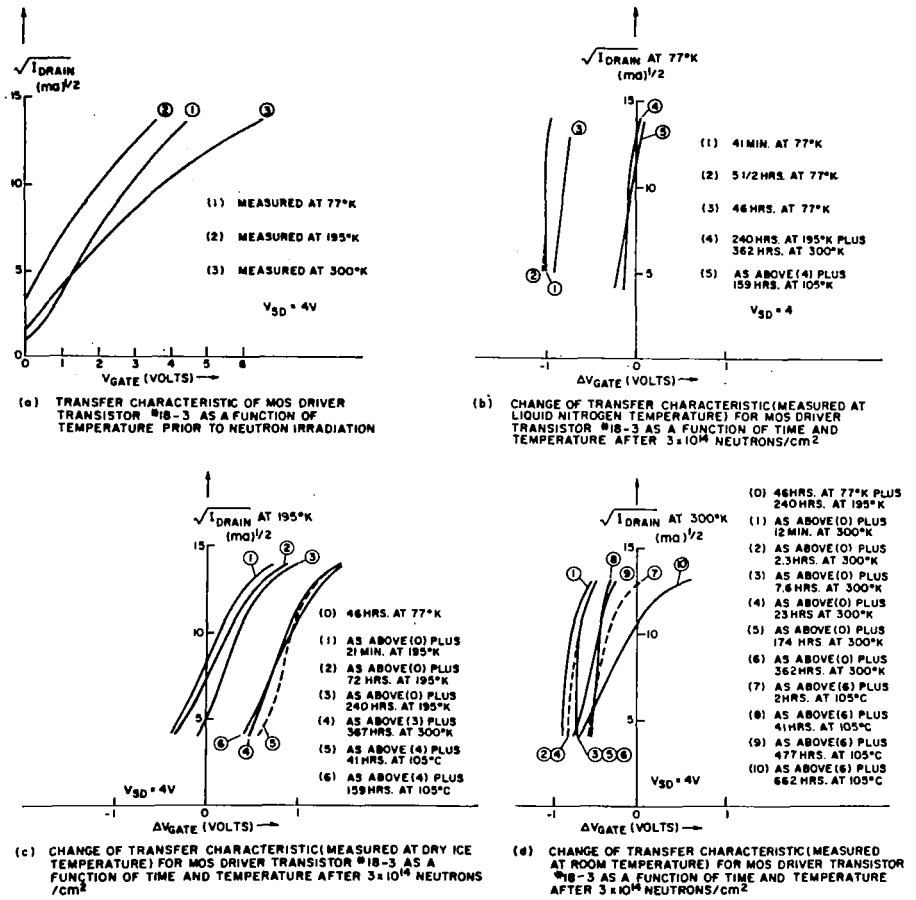


Fig. 60. Transfer characteristic for MOS driver transistor No. 18-3.

direction) for storage at room temperature and elevated temperatures. Similar experiments were performed at radiation levels of 4.5×10^{15} neutrons/cm^2. After 815 hours annealing at room temperature and 360 hours at 110°C some MOS transistors were opened and visually inspected. Severe silver migration was observed (the worst case is shown in Fig. 62). Nonirradiated control samples were heated and showed failure after 331 hours at 100°C and 435 hours at 140°C. Again some silver migration was observed (see Fig. 63). Neutron irradiation seems to aggravate but not solely cause this phenomenon. Therefore, all results obtained by annealing the MOS transistors at high temperatures might have been severely masked by metallurgical degradation of the contacts. It would show up as additional series resistance and reduction in transconductance. In the meantime, MOS transistors have been made using a different metal combination for the source, drain, and gate electrodes. Additional effort is required to determine damage effects in these units.

It appears that an electronic/ionic charge transfer occurs in the annealing of MOS transistors. It has been shown that the electronic state of the oxide-semiconductor system can be widely changed if a gate bias is applied to the

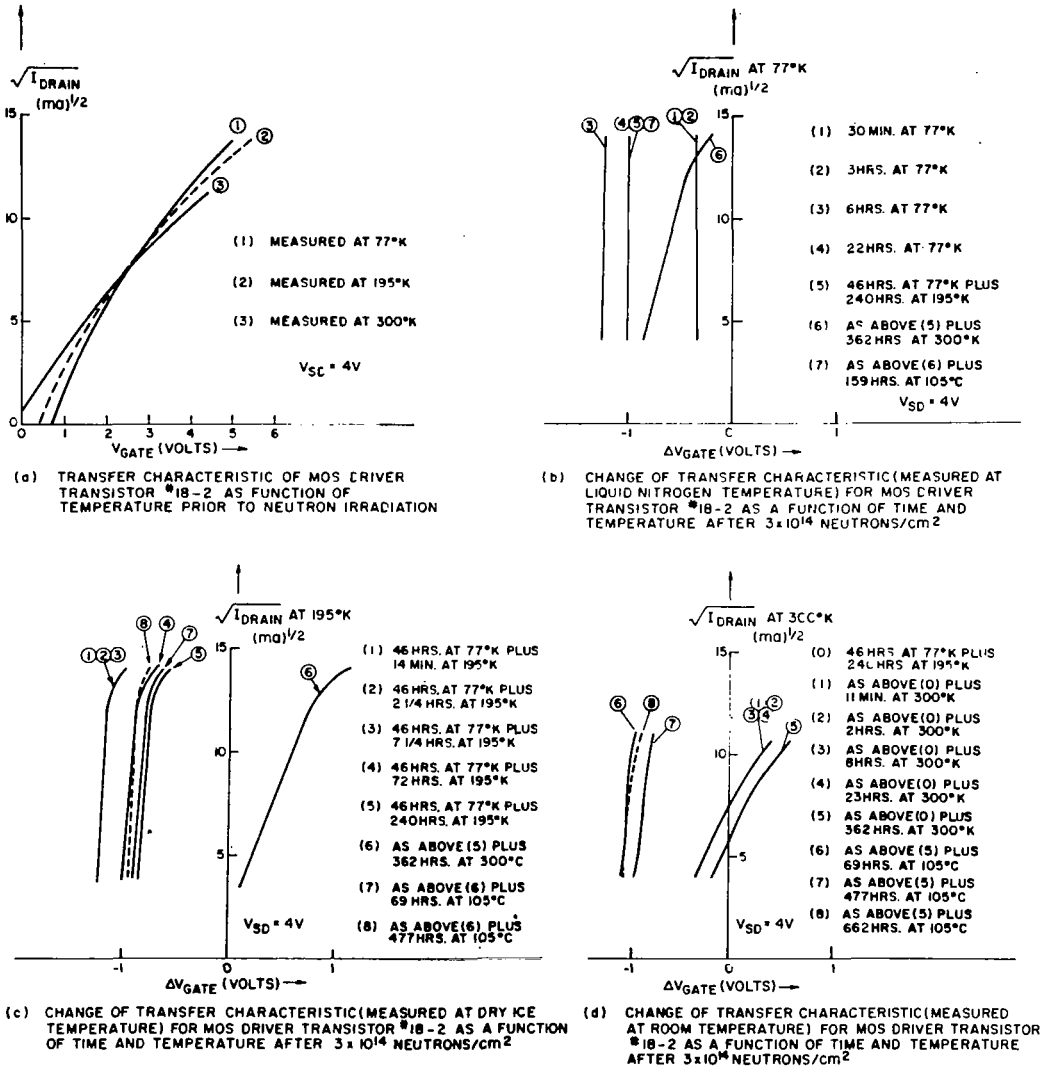


Fig. 61. Transfer characteristic for MOS driver transistor No. 18-2.

MOS transistor at high temperatures. Usually, a shift occurs toward negative gate bias which has been interpreted as a buildup of positive charge in the SiO_2 layer close to the Si-SiO_2 interface. Less positive gate bias is required to reach the previous transfer characteristic. A likely source for this positive charge has been shown to be sodium ions. The best way is to avoid these impurities in the silicon dioxide layer, or to make them immobile by doping the SiO_2 layer.

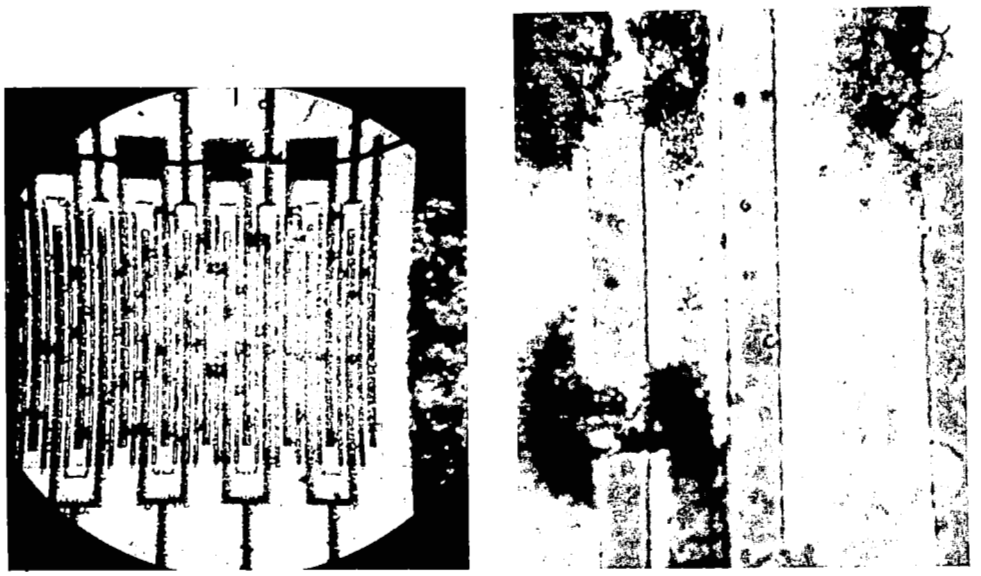


Fig. 62. Slow silver migration caused MOS driver transistor No. 19 to fail after irradiation by 4.5×10^{15} neutrons/cm^2 and annealing 815 hours at 300°K and 360 hours at 110°C.

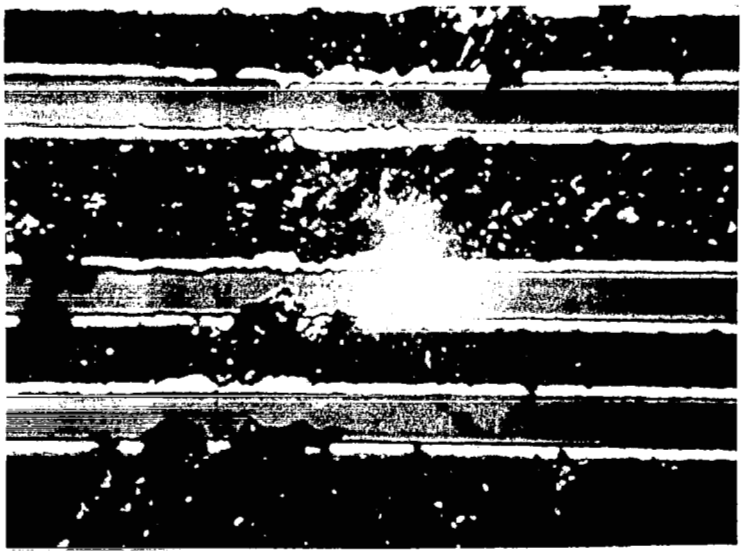


Fig. 63. Silver migration occurred in the nonirradiated MOS driver transistor No. 227 after 331 hours at 100°C and 435 hours at 140°C.

In summary, changes in the transfer characteristic by approximately 1.5 volts in gate bias occurred in the MOS driver transistors studied. The changes were not fully predictable in direction and amplitude even at low temperature where usually a shift toward more negative gate bias prevailed. This shift may be explained by a positive ionic charge which varies with time, temperature, and previous gate bias.

Neutron irradiations up to tested doses of 10^{16} neutrons/cm^2 do not seem to materially affect the MOS performance other than in secondary areas such as accelerated metallurgical contact degradation. True mobility reduction of the majority carriers due to neutron bombardment has not been found so far. Before the intrinsic radiation resistance of MOS transistors can be assessed, technological processing improvements are necessary to prevent the shift of the transfer characteristic that covered up most of the intrinsic radiation resistance.

VI. CONCLUSIONS AND RECOMMENDATIONS

On the basis of the results presented in the previous sections it is concluded that:

1. The fabrication of laminated memory planes with 256 x 100 or 512 x 200 crossovers as single units is feasible and practical.

2. Nitrogen-annealing of laminated planes is necessary to insure uniform and reproducible magnetic and mechanical properties.

3. The use of platinum or palladium conductors with a cross section of 2.5 x 1.5 mils is adequate for memory operation. However, the reduced winding resistance possible with gold bearing conductors will permit reductions in the electronic circuitry for a given memory capacity.

4. The stacking and intraconnecting techniques, described in the report, are feasible and may be used with planes having nonuniform conductor spacing. This relieves the necessity of having planes with highly uniform mechanical properties which is unlikely for large-sized arrays, e.g., 512 x 200.

5. Modifications in the encapsulation techniques are required to prevent nonuniform stressing of the memory planes.

6. The interconnection technique based on chemically milled fingers may be applicable to the interconnection of integrated semiconductor arrays to laminated ferrite stacks.

7. Operation of the laminates with low power is feasible with bipolar digiting techniques in a one crossover-per-bit mode. Read currents of 50 mA with moderate risetimes generate bipolar sense signals in the range of 1 to 3 mV.

8. Peak back voltage at read time is in the range of 10 to 20 mV per bit, permitting a word length of several hundred bits without the need for excessively high voltage supplies.

9. Required digit current amplitudes are in the order of 5 mA, resulting in low digit power consumption even for long words. The digit supply voltage required is of the order of only 1 volt.

10. Expected read-rewrite cycle time for a mass memory is in the range of 2 to 3 microseconds. Faster cycles may be achieved at the expense of increased electronics, i.e., shorter sense-digit lines and increased word currents.

11. For a 2-μsec cycle time the attenuation of the sense signal and digit current is primarily due to the dc resistance of the sense-digit conductor.

12. The magnetic and electrical characteristics (H_c, B_r, ρ, ϵ) of ferrites are sufficiently insensitive to radiation (2×10^{19} nvt and $10^{10} \times 10^{11}$ rads of gamma flux) to permit memory operation in a severe radiation environment.

13. For MOS transistors, carrier mobility changes are not observed for dosages up to 10^{16} nvt. However, other changes, related to metallurgical processing, were observed that led to shifts in device characteristics.

On the basis of these results it is recommended that additional effort, as outlined in Descriptive Specification No. 63-1036E dated April 15, 1965, be pursued to realize a mass-integrated low-power random-access memory suitable for space use.

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