ANALOG-DIGITAL, DIGITAL-ANALOG CONVERTER FOR A DIGITAL CONTROL SYSTEM SIMULATOR

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ABSTRACT

The design and construction of a unit consisting of one

analog-to-digital converter, one digital-to-analog converter, and

digital control logic is described. The unit is used with a GEDA

real time analog computer and a digital logic synthesizer to make

possible the simulation of absolute and incremental digital control

systems having single digital feedback loops. Portions of the GEDA

are utilized in the implementation of the A/D and D/A converters,

thereby making possible a reduction in the unit's overall cost.

The analog-to-digital and digital-to-analog converters

are analyzed, and predicted performance is compared to actual

observed performance. A sample simulation is presented to dem-

onstrate how the unit can be used, and complete operating and

calibration instructions are provided in the form of an operation

manual.

ACKNOWLEDGEMENTS

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ENCODER AND DECODER PERFORMANCE ANALYSIS
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LIST OF LITERAL SYMBOLS

a_0, a_1, $\cdots$, a_n, a_i	binary weights
$\bar{a}_i$	complement of a_i
A	sine wave amplitude (quanta)
β	positive number less than one
D	time increment
δ	voltage increment
E	constant reference voltage
e_o	summing amplifier output voltage
e_i	summing amplifier input voltage
$(e_{on})_i$	portion of summing amplifier output voltage
$(e_{off})_i$	portion of summing amplifier output voltage
ϵ_s	sampling error (quanta)
f	frequency (c.p.s.)
$G(s)$, $G(s')$	transfer functions
i	an integer
I_{CBO}	transistor collector leakage current with emitter open
ΔI_{CBO}	change in I_{CBO}
K_v	velocity gain constant
K	positive number less than one

m	analog voltage slope (quanta/sec.)
n	an integer
ψ	a constant
Q	quanta size (volts)
R_f	summing amplifier feedback resistance
R_i	summing amplifier input resistance
$R_0, R_1, \ldots, R_n$	D/A ladder resistances
R	resistance
R_a	A/D converter input resistance
R_b	bias resistance
s, s'	Laplace operator
θ	controlled variable
$\dot{\theta}$	time derivative of θ
τ	time
T	time constant
τ_A	clock period
$\tau_1, \tau_2, \tau_L, \tau_P, \tau_u, \tau_c, \tau_e$	delay times
V_a	A/D converter input voltage
V_b	bias component of summing amplifier output voltage

V_e	summing amplifier output voltage
V_{c_i}	collector voltage
ΔV_{c_i}	change in collector voltage
V_{ce}	collector-to-emitter voltage
$(\Delta V_{ce})_{sat.}$	change in collector-to-emitter saturation voltage
$(\Delta V_{e_i})_{adj.}$	D/A error voltage component due to bit adjustment
$(\Delta V_{e_i})_{leak.}$	D/A error voltage component due to leakage current variation
V_T	comparator sensing voltage
ζ	damping ratio

LIST OF LOGIC ELEMENT SYMBOLS

Symbol

(logic designed by Case Digital
Systems Laboratory)

Type 202 NOR 2 gate

Type 212 NOR 1 gate
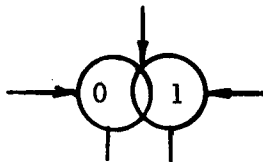
Type 311 RSTT flip flop, or
Type 201 JK flip flop

Type 214 GPG (gated pulse
generator)

Type 308 MIGPG (multi-input
gated pulse generator)
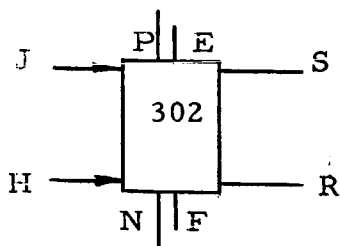
Type 302 BDC (two bit binary
bidirectional counter)

Type 209 Steering gate
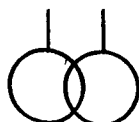
Type 207 FRMV (free running
multivibrator)

LIST OF FIGURES

CHAPTER 1

INTRODUCTION

1.1 Introduction

Digital feedback control, characterized by closed loop systems in which both command and feedback information are in discrete or numerical form, is replacing or supplementing conventional analog (continuous) feedback control in some applications. Advantages in using digital control are primarily those of:

1. Increased accuracy

2. Ease of information storage

3. Greater reliability

4. Compatibility with large general purpose digital computers

5. More reliable data transmission in the presence of noise.

Digital feedback control, however, results in a system which is generally less stable than a corresponding all analog system. Reasons for this are:

1. In order to perform digital computations, continuous signals must be represented by only a finite number of states. When transitions from one state to another occur, loop gain is effectively infinite.

2. Any calculation involving digital information requires

a finite time interval for completion, hence a time
lag will result between the time of measurement of
the desired input and system output and the corre-
sponding application of a corrective control signal.

These two problems due to 1) quantization and 2) sampling are inher-

ent in any digital control system. Much emphasis in digital control

system synthesis is placed on developing methods of compensation

for this decreased stability brought on by quantization and sampling.

The problem of compensator design for a digital control

system is similar to that of designing a controller for a conventional

analog control system. In an analog system, as the process to be

controlled increases in complexity, the analytical design of a suit-

able compensator becomes exceedingly difficult; therefore, an analog

computer is generally used to aid in determining a suitable control

scheme. The methods presently available for analyzing simple dig-

ital control systems, such as graphical convolution, time domain so-

lution on a digital computer, describing function,phase plane, or ac-

tual construction are often slow or tedious to implement and tend to

give the designer information about only a particular class of sys-

tems, not an overall picture. Thus it is even more desirable to be

able to simulate digital system performance than it was for an ana-

log system.

1.2   The Hybrid Simulator

The purpose of this thesis is to design a facility on which a digital control system having a single digital feedback loop and an arbitrary number of analog feedback loops can be simulated. The two main portions of the simulation facility are:

1. The Digital Synthesizer, built by the Case Numerical Control Laboratory, on which can be assembled the digital portions of a digital control system.

2. The Goodyear Electronic Differential Analyzer, (GEDA), a general purpose real-time analog computer, used by the Control Systems Synthesis group. The continuous portion of the system may be simulated this facility.

It is then necessary to provide the interconnecting links---suitable digital-to-analog and analog-to-digital conversion equipment---to combine the Digital Synthesizer and the GEDA into a Control System Simulator. Both the GEDA and the Digital Synthesizer can be rapidly programmed on removable patchboards, hence the complete facility is flexible and can be used both for investigations of the dynamics of digital control systems as well as for classroom demonstration and graduate and undergraduate laboratories. To better explain the aims of this thesis, a brief explanation of the two basic types of digital control systems is in order.

1.3   Absolute Digital Control

A single loop absolute digital control system is shown in Fig. 1. "Absolute" indicates that command and feedback information appear as a coded digital number. In this system, the analog signal representing the controlled variable is converted to a digital form by means of an analog-to-digital (A/D) converter (encoder). This number is compared to a number representing the desired state of the controlled variable command signal. If the two numbers are not equal, a numerical error signal is generated to cause corrective action. This error signal must first be converted back to an analog quantity by a digital-to-analog (D/A) converter (decoder) before it can exercise control on the process. The box marked "LOGIC" includes arithmetic logic for subtraction or comparison, any digital compensation logic, and a register for storage of the latest value of the computed error signal.

1.4   Incremental Digital Control

Fig. 2 shows a single loop incremental digital control system. "Incremental" indicates that command and feedback data are in the form of pulse trains, where each pulse represents an increment of motion. Each time the controlled variable changes by a
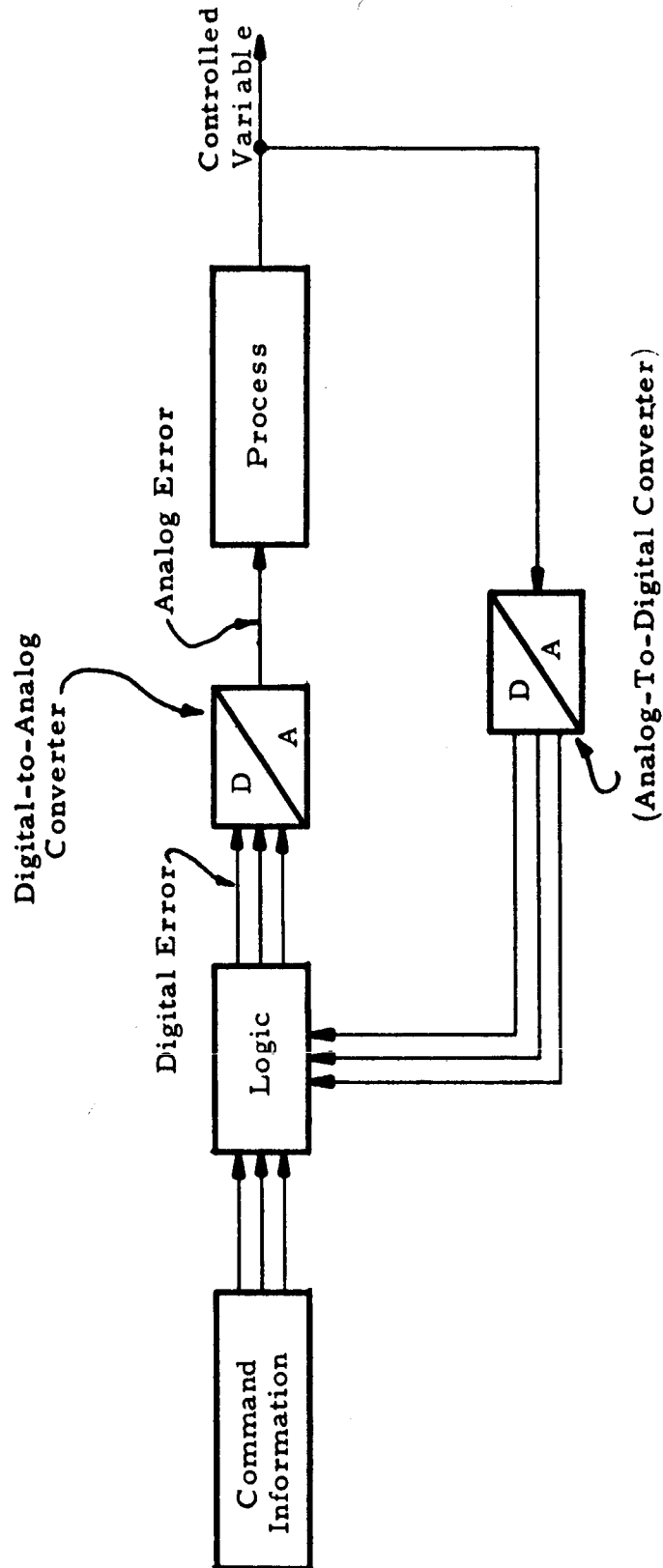
FIG. 1 - ABSOLUTE DIGITAL CONTROL SYSTEM
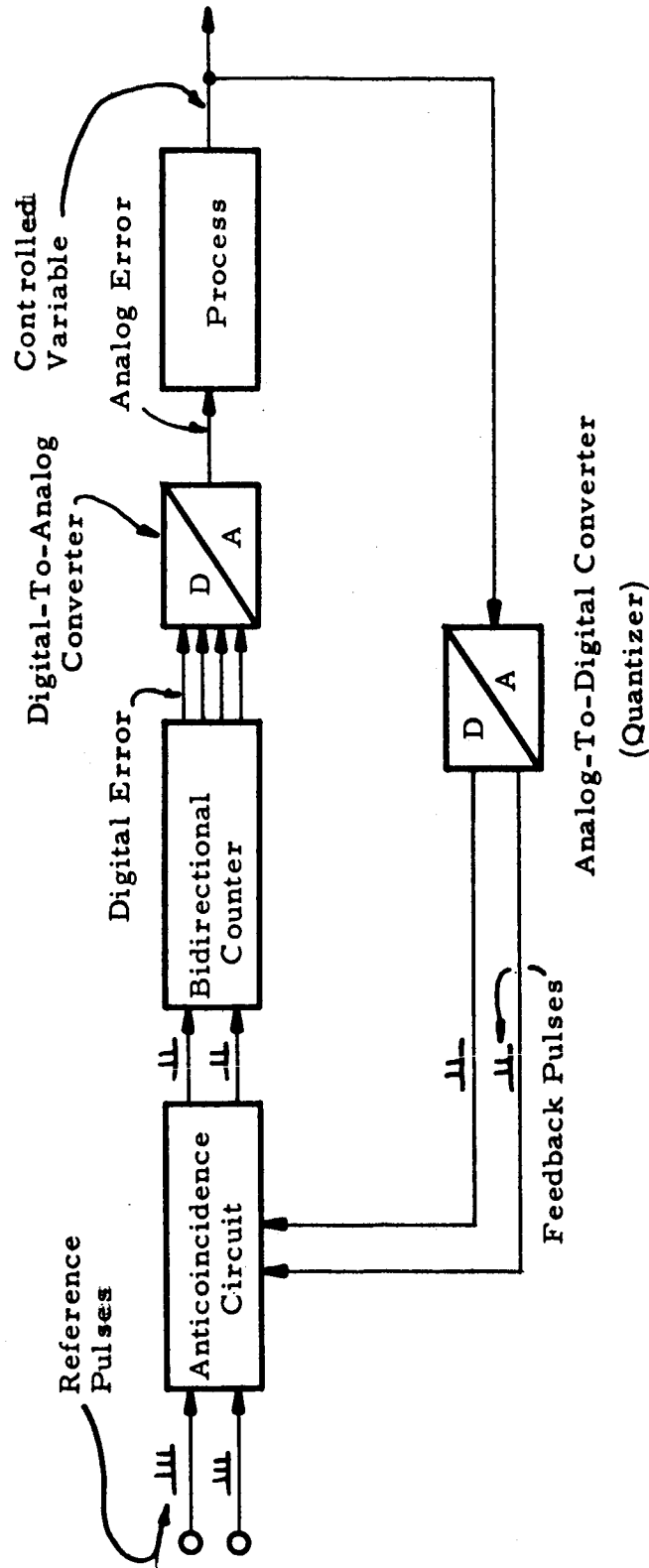
FIG. 2 – INCREMENTAL DIGITAL CONTROL SYSTEM

fixed increment or quanta, the quantizer (A/D Converter) emits a plus or a minus pulse, depending upon the direction of motion, indicating that the output has passed a fixed quanta level. These feedback pulses are summed with reference (command) pulses in a bidirectional counter. The state of the bidirectional counter, usually a binary number, represents the difference between the number of past reference pulses received and the number of feedback pulses emitted by the quantizer. When the number of increments moved by the controlled variable equals the number of increments of desired motion, the number in the error counter is zero. The error number is converted by a converter (decoder) to an analog error signal which is then used to exercise control over the process. Additional digital compensation logic may be employed but is not shown on this simplified schematic.

1.5   Design Specifications for the A/D and D/A Converters

The Digital Control System Simulator should be capable of simulating a single absolute or incremental digital control loop. The main purpose of this thesis work was the design and construction of one D/A converter and one A/D converter, compatible with both the Synthesizer and the GEDA.

The D/A converter designed must meet the following requirements.

1. The digital input must be an eight bit natural binary number. Logic levels are to be 0 and -12 volts d.c.

2. Settling time for the output must be such that the D/A converter is not the limiting factor in total system response.

3. The scale of the analog output must be able to vary so as to have 1, 2, 4, 8, 16, 32, and 64 volts per binary bit. A mid scale input (128 binary) must produce a zero volt output.

Specifications for the A/D Converter are as follows:

1. It must perform as an absolute analog-to-digital converter, simulating transducers such as an absolute shaft-position encoder. It must convert a + 100 volt d.c. signal into a natural binary number, biased such that a zero volt input produces a binary output of 128. The least significant binary bit should correspond to one volt.

2. It must perform as an incremental converter or quantizer, simulating an incremental shaft position encoder. Quanta size must be variable through 1,2, 4, 8, 16, 32, to 64 volts per quanta.

3. Absolute binary outputs must be either 0 or -12 volts. Both asserted and negated forms of the output should be available simultaneously.

4. There must be two incremental (pulse) outputs, one emitting pulses for a positive going input signal, the other for a negative going signal. Each pulse is to have a -12 volt amplitude and a minimum of three microseconds duration.

5. The converter must be able to convert a sine wave with 100 volts half amplitude at a frequency of ten cycles per second.

Additional specifications which apply to both the D/A and the A/D converter are:

1. Both units must be able to be constructed at a substantially lower cost than any similar commercially available items.

2. Reliability must be high. Drift must be low, on the order of that present in the GEDA. Readjustment should not be required more than every six months. The number of different power supplies required should be held to a minimum.

3. Static accuracy should be comparable to that of the GEDA, or ± 0.1 volt.

4. Both the D/A and the A/D should be conveniently packaged for mounting near the GEDA. This insures that any data to be transmitted over an appreciable distance will be in digital form.

Since one of the main areas of use for the simulator will be in the investigation of the dynamics of incremental or pulse-data control systems, the converter package should include in it a four bit binary bidirectional counter and anticoincidence circuit such that a simple pulse-data loop can be programmed without requiring the use of additional logic from the Digital Synthesizer. Thus a great many systems can be studied without using the Synthesizer, thereby

freeing it for other uses.

1.6   Summary

The main purpose of this thesis is to design and construct a unit containing one D/A converter, one A/D quantizer/encoder, and one bidirectional counter plus anticoincidence circuit which when used with the GEDA real time analog computer and the Digital Synthesizer will permit the simulation of digital control systems having single digital feedback loops. The complete facility will make it possible to study the digital control of processes with a wide variety of dynamic characteristics.

CHAPTER 2

ANALOG-TO-DIGITAL AND DIGITAL-TO-ANALOG CONVERSION METHODS

2.1 Introduction

At the present time there are numerous methods of ana-

log-digital conversion (the hyphenated expression "analog-digital"

will be used when referring collectively to D/A and A/D conversion).

Not all of the presently used conversion methods are suitable for the

purposes of this thesis. The main criteria for selecting the A/D and

D/A conversion methods which might be useful were:

1. The D/A converter must operate on parallel input
information and have a high enough output voltage to
accurately function with the analog computer.

2. The A/D converter must simulate the action of both
an absolute shaft-position encoder and an increment-
al shaft-position quantizer.

3. The number of quanta used in the system must be
conveniently variable.

4. The overall design must require a minimum of
equipment, both analog and digital.

With these criteria in mind, various converter types were examined

and the most promising type selected for actual design implementa-

tion.

2.2   Digital-to-Analog Conversion Methods

2.21   Introduction

The criteria restricting the digital input to parallel form eliminated such serial D/A converters as the Shannon-Rack decoder, which would require conversion first from parallel to serial digital form prior to conversion to analog. Thus the types of D/A's considered were either of the weighted resistor type or the resistor ladder type.

2.22   Voltage or Current Ladder Decoder[1,2]*

Resistor ladder networks utilizing either n current or n voltage sources which convert n bit parallel binary numbers to analog voltages are shown in Fig. 3a and 3b. In order to obtain the simplest overall design, all digital (switching) portions of these converters should be transistorized so that they can be operated directly from Synthesizer logic modules. However, use of transistors limits the range of the converter output voltage to about 25 volts, which is near the normal maximum collector-to-emitter voltage of medium speed switching transistors which should be used. Amplification

* Superscripts refer to Bibliography.
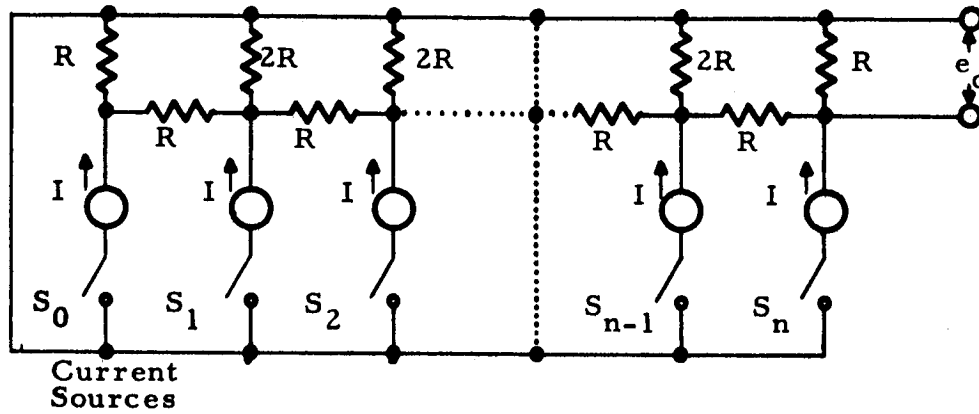
a) Current Source Ladder Decoder
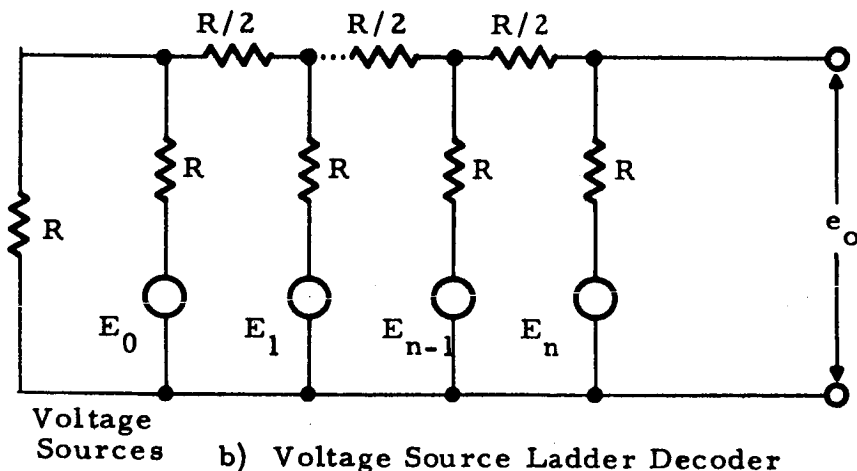
b) Voltage Source Ladder Decoder

FIG. 3 - LADDER TYPE DECODERS

would therefore be needed to boost the output up to 100 v. Very low tolerance resistors would have to be used since adjustable trimming resistors on each resistor leg would result in a circuit which could be theoretically adjusted for the required accuracy but in practice would be unmanageable.

2.23 Weighted Resistor Network[3]

Fig. 4 shows a typical weighted resistor network or "digital potentiometer." The individual resistors can be adjustable so that very low tolerance fixed resistors are not necessary; however, medium speed switching transistors can't withstand the voltages required if the maximum converter output is to be $\pm$ 100 volts. Thus some additional amplification would be required.

2.24 Summing Amplifer with Switched Input Resistors[4]

Fig. 5 depicts a method of decoding which requires the use of a high gain d.c. amplifier and a set of binary weighted input resistors. This circuit has the advantage that low voltage transistors can be used to effectively switch a high reference voltage across a series of weighted resistors. Each bit resistance can be individually adjusted with variable resistors nR $(1-\beta)$. R $(1-\beta)$ must be
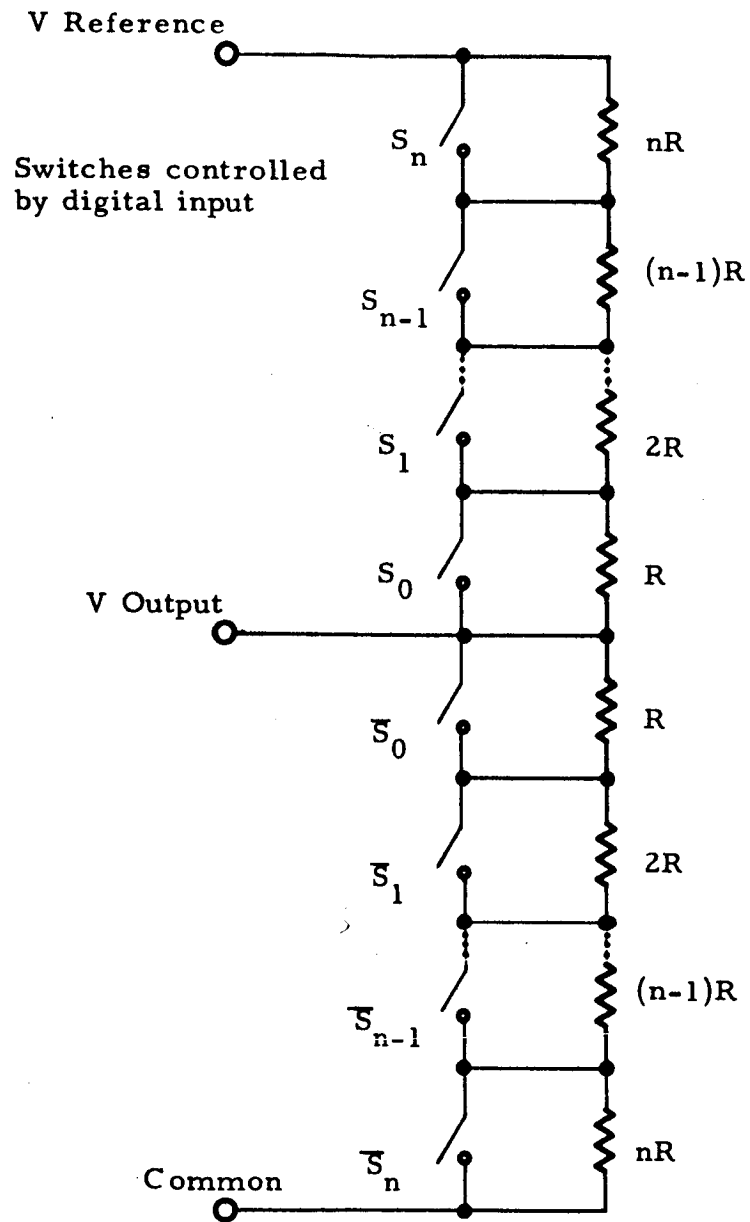
FIG. 4 - WEIGHTED RESISTOR NETWORK
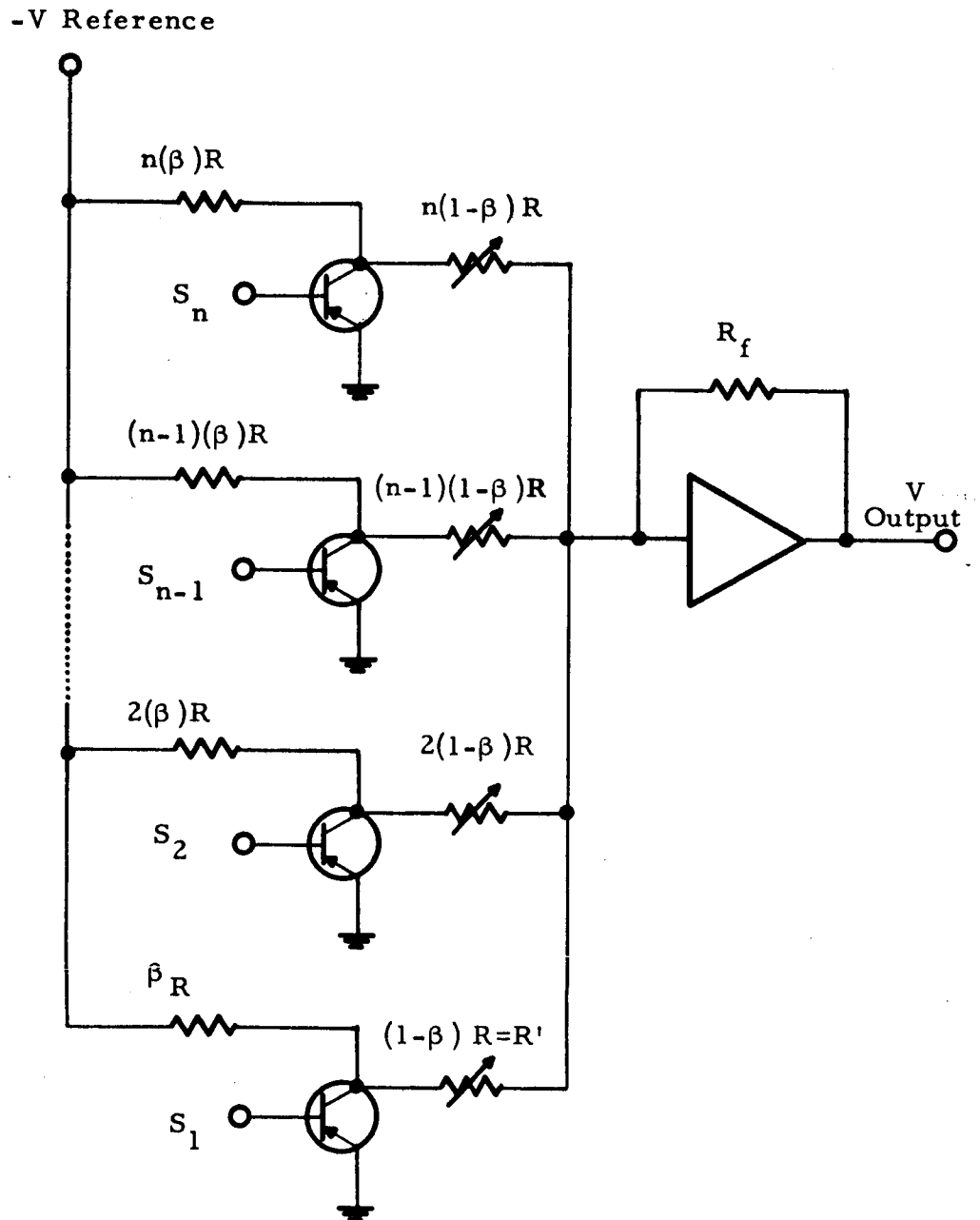
FIG. 5 - SUMMING AMPLIFIER WITH SWITCHED INPUT
RESISTORS

limited by selecting β (where β is a positive number less than 1) so that transistor collector-to-emitter voltages don't ever exceed maximum ratings. The analog computer's reference voltage can serve as $\rightarrow V_{Ref.}$ and an operational amplifier from the analog computer can be used for the summing amplifer. Since the GEDA has a commutator stabilization system which limits d.c. amplifier drift to about 500 microvolts, the problem of decoder drift would also be minimized.

2.25   D/A (Decoder) Selection

The summing amplifier with switched input resistors decoder was selected for implementation because it 1) allows low voltage switching transistors to be used, 2) needs no additional reference voltage supply, 3) can use lower tolerance fixed resistors with adjustable trimming resistors.

2.3   Analog-to-Digital Conversion Methods

2.31   Introduction

There are many A/D converter types that will convert a d.c. voltage to a binary number, therefore the main criteria for selection were not functional but ones of cost, complexity, and re-

liability.

2.32   Electromechanical Position Servo with Shaft Position Encoder

An electromechanical position servo can be used to drive a shaft position-to-digital converter as shown in Fig. 6. By using an encoder with two properly located pickups per bit (encoder tracks), the encoder could also function as a quantizer. Although its performance as an encoder and quantizer would be suitable, such problems as low bandwidth, friction and wear, and relatively high cost of a dual-pickup-per-bit encoder rule it out as a possible solution.

2.33   Time Base Encoder[1]

Fig. 7 shows a typical time base encoder employing a linear sweep generator. A "start" signal from the control logic causes the sweep generator to produce an increasing output and also opens the gate to allow the fixed frequency clock to feed pulses into the counter. The gate is closed when the comparator indicates the linear sweep and the input voltage are equal. The contents of the counter, assuming correct scaling, is a digital representation of the analog input. After some delay, the counter and sweep gen-
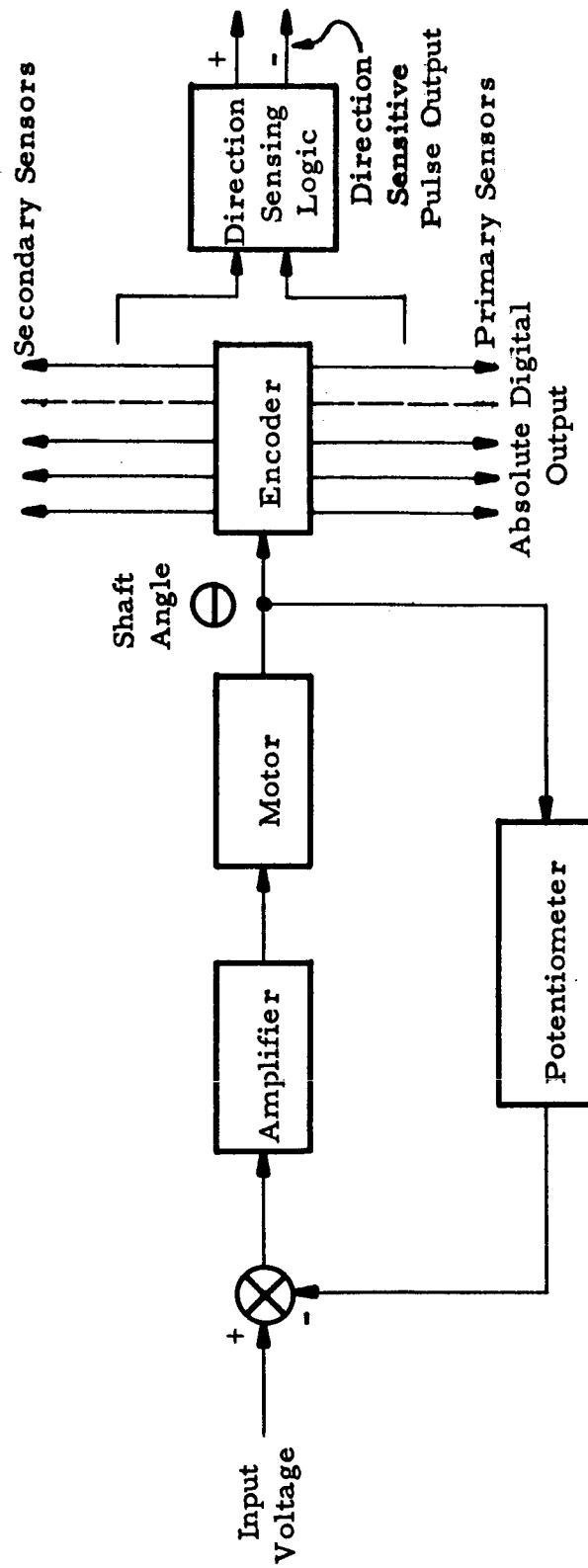
FIG. 6 -- ELECTROMECHANICAL POSITION SERVO WITH SHAFT POSITION ENCODER
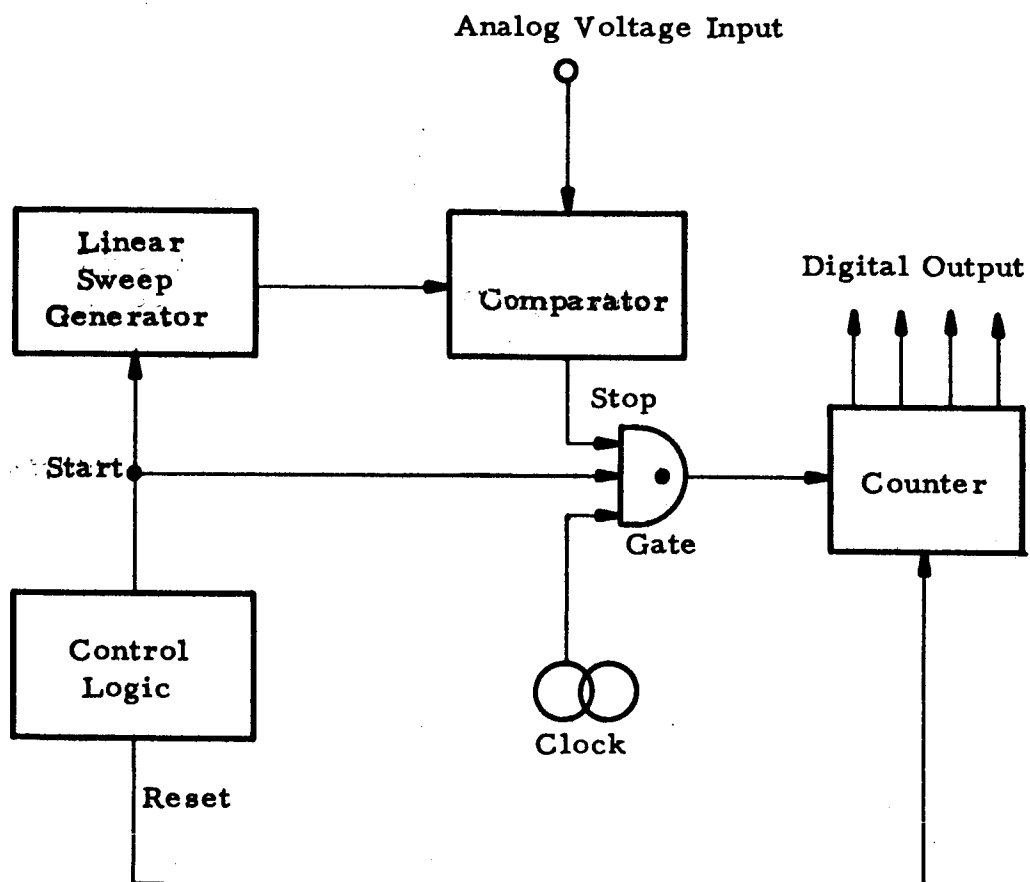
FIG. 7 - TIME BASE ENCODER

erator are reset and the process repeated. There are numerous variations of this method (different comparators, staircase generator instead of the linear sweep generator) but the main drawbacks ⟟ are that the past output must be stored in an additional register while the comparison process is occurring, and the method is relatively slow due to the fact that the counter must be at worst counted through 2^n states if the input corresponds to an n bit binary number. The sweep or staircase generator output is also subject to inaccuracies.

2.34 Cascaded Stages Encoder[5,1]

Fig. 8 depicts an encoder which requires no counter or pulse generator. The analog input voltage is compared first with a fixed reference voltage. If it exceeds the voltage corresponding to the most significant bit (Sn), a true indication is given on line Sn, the equivalent bit voltage is subtracted from the input, the result multiplied by two and used as the input to the next less significant stage. This converter can be quite fast as only n comparisons and subtractions are required as the signal propagates down through to the least significant stage. Problems involved however are the accuracies of the comparators (which could be differential amplifiers or Schmitt triggers) and the implementation of the analog subtract-
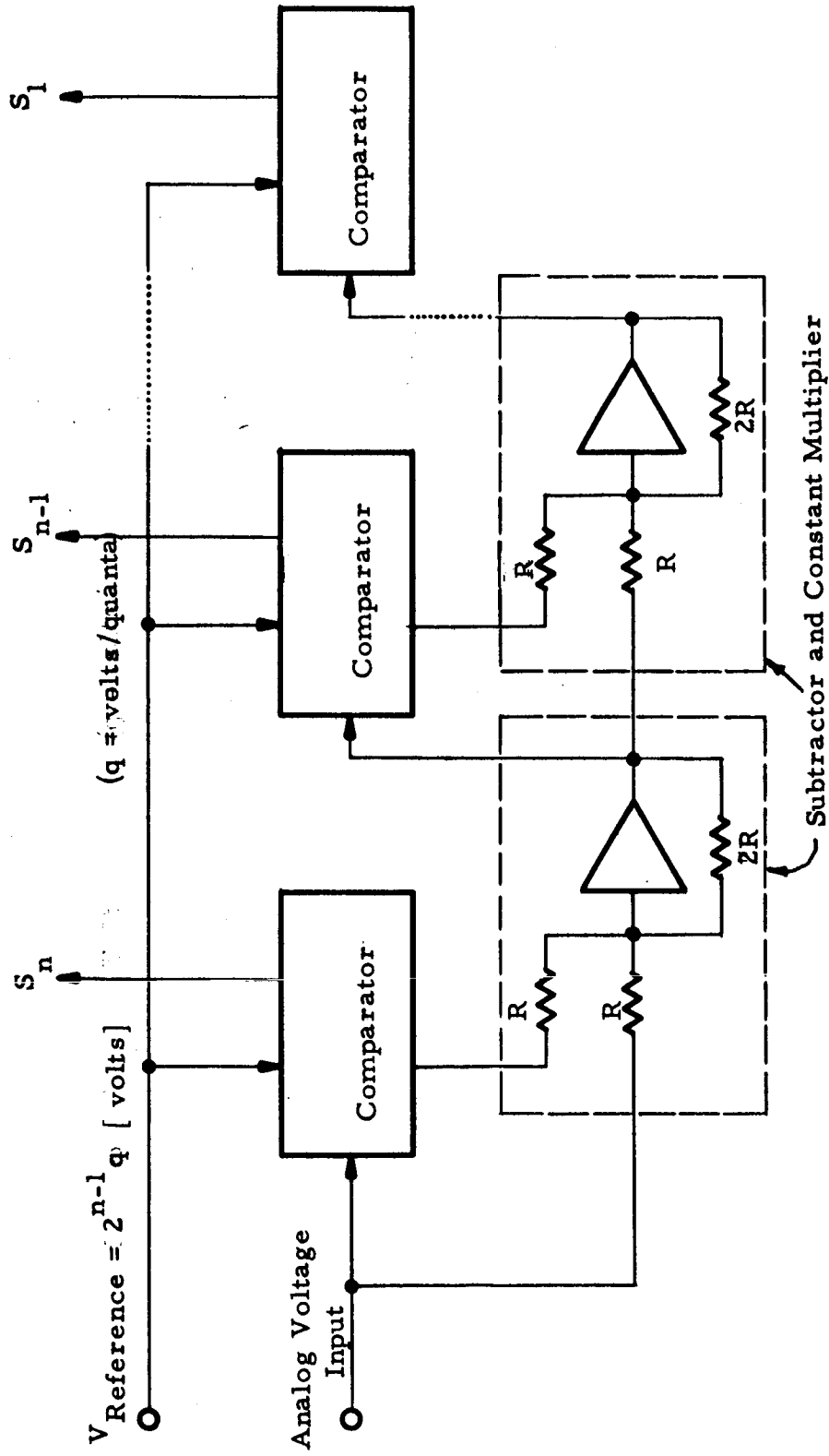
FIG. 8 - CODER WITH CASCADED STAGES

ors. In practice, subtractions and multiplications would be done

using n-1 summing amplifiers. For an eight bit converter, this

would mean tieing up seven GEDA operational amplifiers, which

would be too many in view of the fact that there are only twenty-four

available in all. Note also that this encoder requires no storage re-

gister. This method may be quite advantageous when only two to

four bits of information are required as it can be completely patched

up, including the comparators, on the GEDA. The only external

circuitry required would be Schmitt triggers to convert high voltage

logic levels from the GEDA comparators to low voltage levels suit-

able for Synthesizer logic. Fig. 9 shows a two bit converter capable

of converting positive input voltages only. Note that the sign of the

comparison must alternate with each subsequent stage due to the in-

version in the multiply-subtract amplifier.

2. 35 Successive Approximation Encoder[6,1]

One of the fastest voltage encoders, a member of the

general class of feedback or comparison types is the successive ap-

proximation encoder. Fig. 10 shows a simplified block diagram of

such an encoder. With an analog voltage applied at the input, tim-

ing pulses 1 through 2n are generated by the ring counter. The first

Equations:

$$\frac{R_1}{R_3} \times 200 = V_{Ref} = 2^{n-1} q \text{ Volts}$$

$$R_2 \gg R_1 \dots \dots \quad R_1 \ll R_0$$
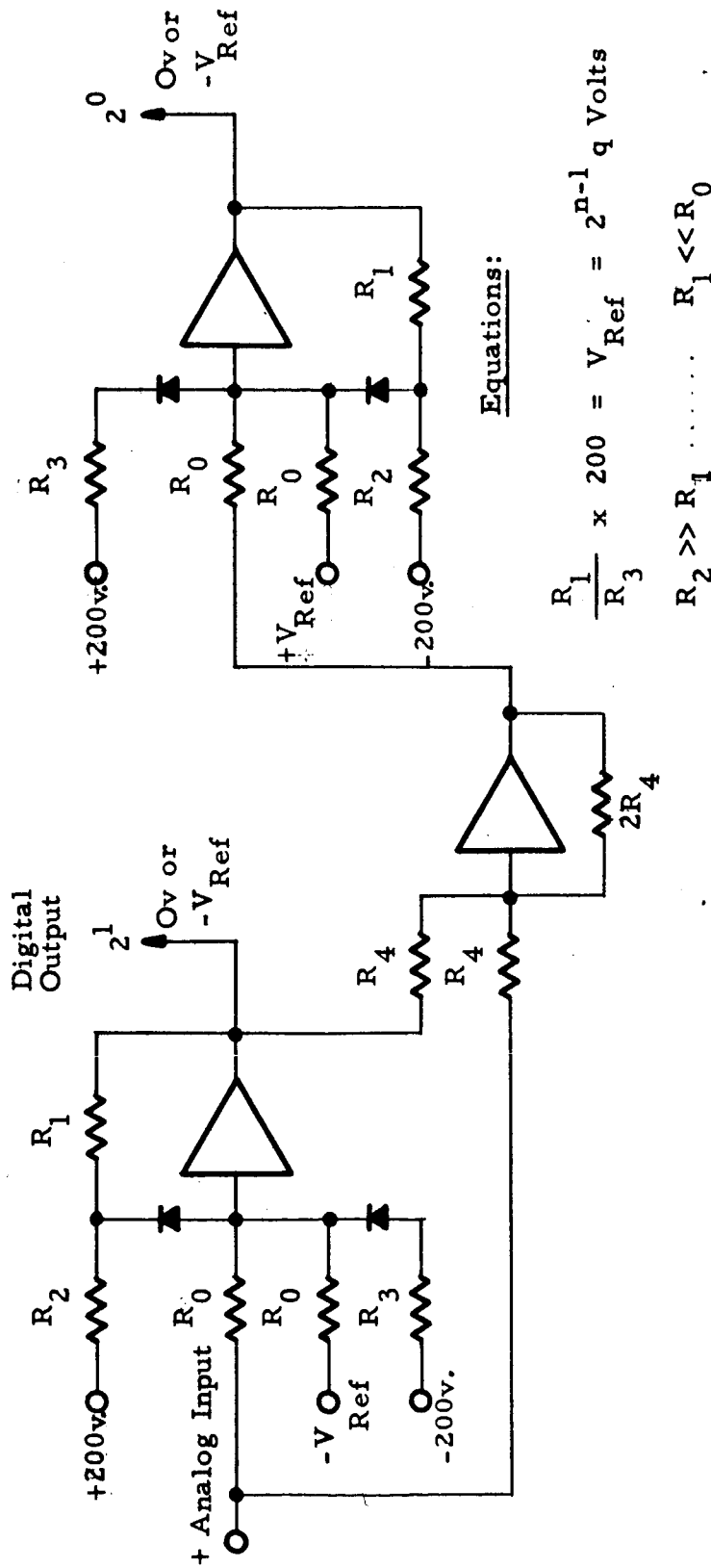
FIG. 9 – ANALOG COMPUTER CIRCUIT FOR A TWO BIT
CASCADED CONVERTER FOR POSITIVE ANALOG INPUT VOLTAGES
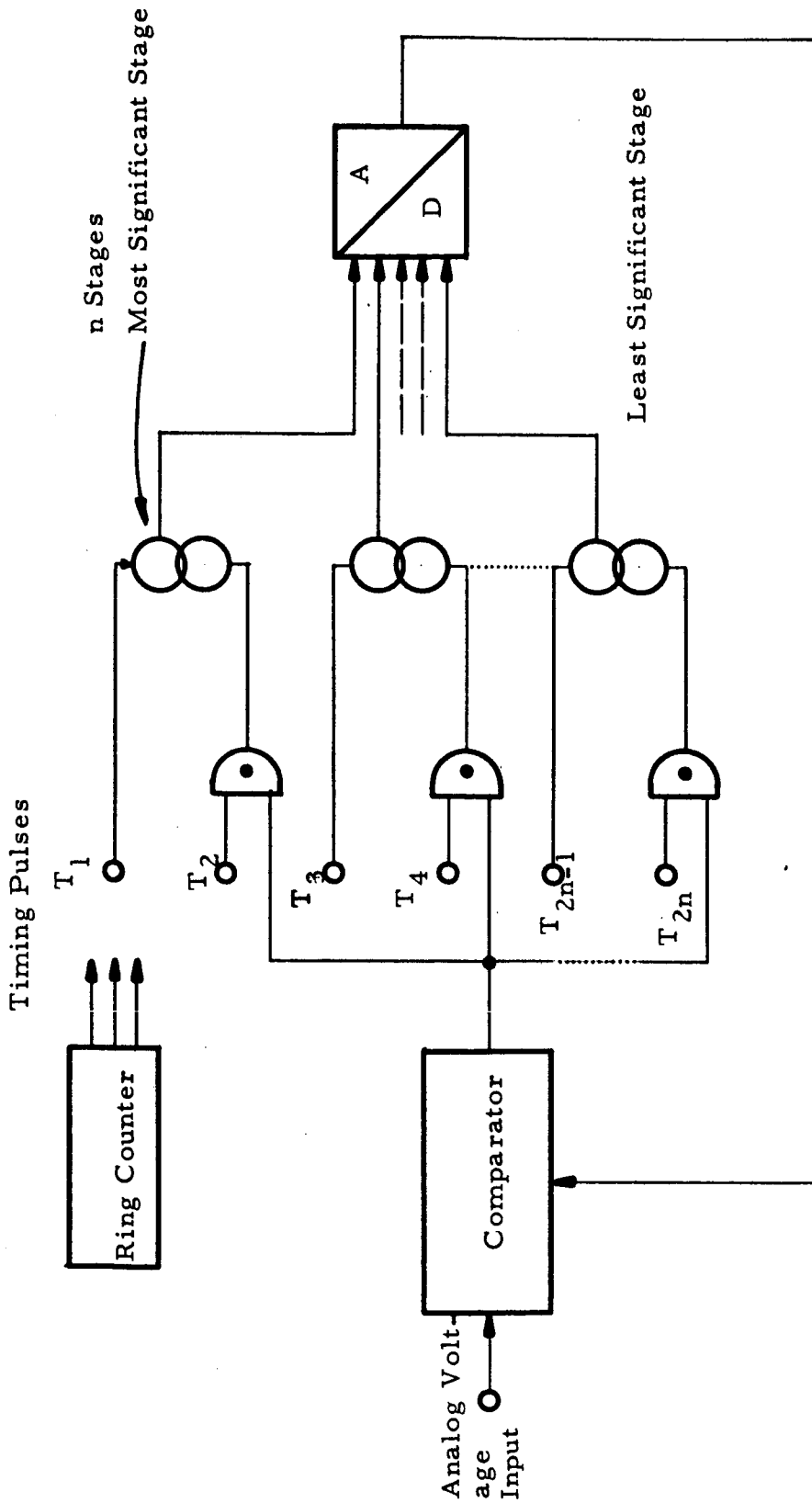
FIG. 10 - SUCCESSIVE APPROXIMATION
ENCODER

pulse (T_1) sets the most significant bit. This bit is converted to an analog voltage by the D/A converter, and the decoder output is compared with the analog input voltage. If the D/A output is greater than the analog input, the "and" gates are enabled and the second timing pulse (T_2) resets the most significant flip flop. If the analog input is greater than the D/A output, the "and" gate is disabled, and the first flip-flop is left in the "set" state. This process is repeated with the lesser significant bits until timing pulse T_{2n} after which the timing cycle is repeated. For a rapid, full-scale change in the analog input voltage, 2n timing pulses will be required before the correct digital output is attained, whereas for the continuous balance method, which will be mentioned next, 2^n-1 pulses will be required. If however, the converter is never required to convert a signal which changes by more than one quanta during the total cycle time (T_1 through T_{2n}) speed of operation of the two types will be comparable. The successive approximation encoder also requires an n-bit ring counter or timing logic which, as will be seen, the continuous balance method does not.

2.36   Continuous Balance Method[6]

The continuous balance encoder is another feedback type

which is known also as the servo or self-balancing encoder. There are two sub-types of continuous balance encoders, asynchronous and synchronous.

2.361 Asynchronous Continuous Balance Encoder

Fig. 11 is a schematic of an asynchronous continuous balance encoder. Starting with zero input voltage, the analog voltage input is increased to +1/2 quanta, the "up" trigger fires and causes the bidirectional counter to count up one. This change in counter state is sensed by the D/A converter, converted to an analog signal, and subtracted from the analog input. The error signal then goes negative, resetting the "up" trigger and settles at a negative voltage slightly more positive than -1/2 quanta. If the input now goes slightly negative, the "down" trigger will fire causing the counter to be counted down one and the error signal to settle at slightly less than +1/2 quanta. The slight difference mentioned is due to hysteresis which must be built into the loop to prevent the encoder from continuously cycling with the input fixed on a quanta line. For proper encoder functioning, the analog input must never move another quanta before the previous pulse has propagated completely around the loop. Otherwise the second pulse will be lost and the encoder
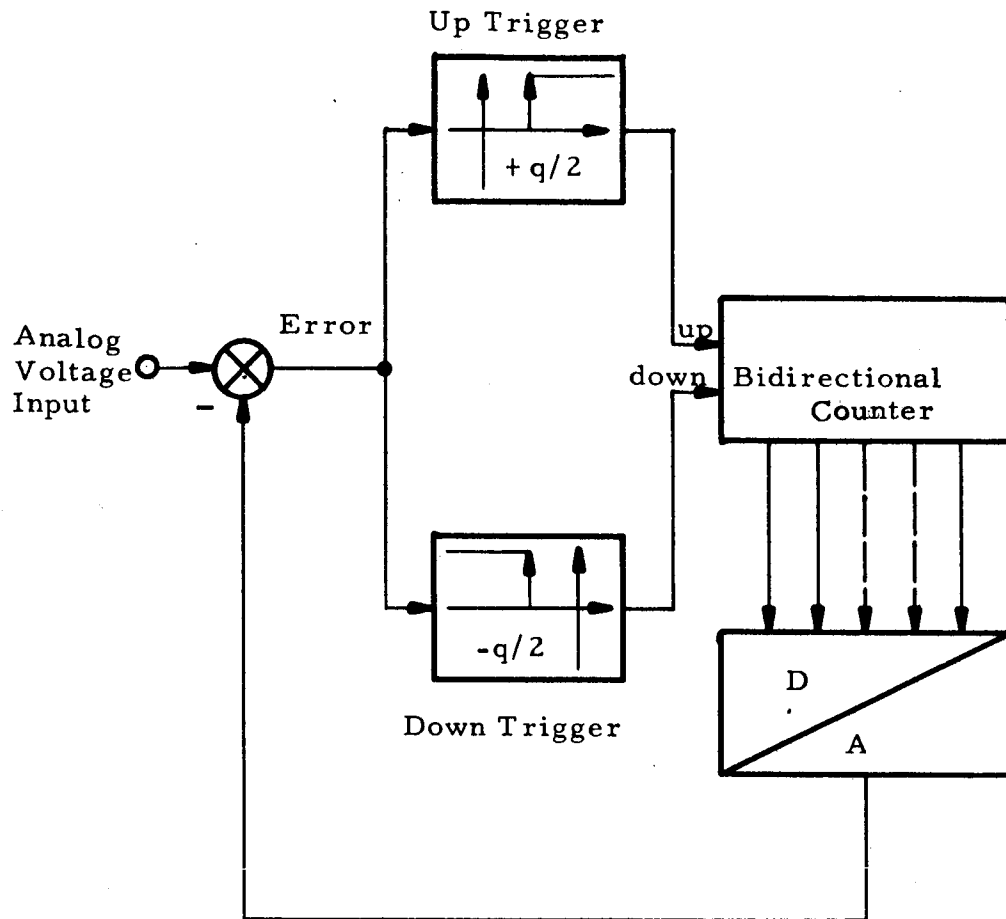
FIG. 11 - ASYNCHRONOUS CONTINUOUS BALANCE
ENCODER

will cease to follow the input. This also means that any noise present in the system or ripple on the analog input must not cause false triggering else the encoder will be in error by one quanta and encoding will stop. This method has the advantages, however, that no timing logic is required and that a change in state of the encoder occurs not at a predetermined clock time but at the instant the input reaches a quanta line. However, if the input signal contains an appreciable noise component, it is preferable to use the synchronous balance encoder which is discussed next.

2.362 Synchronous Continuous Balance Encoder[7]

The synchronous continuous balance encoder, shown in Fig. 12, is quite similar to the asynchronous method. The action of the encoder is the same as the asynchronous encoder except that instead of counting the counter up and down with the trigger transitions directly, the trigger output levels are used to gate constant frequency clock pulses into the counter's "up" and "down" inputs. Therefore, if noise or unusual input conditions cause the input to change more rapidly than the converter can follow, one of the triggers will keep its corresponding "and" gate enabled until equilibrium is reached. However, due to its synchronous nature, counter tran-
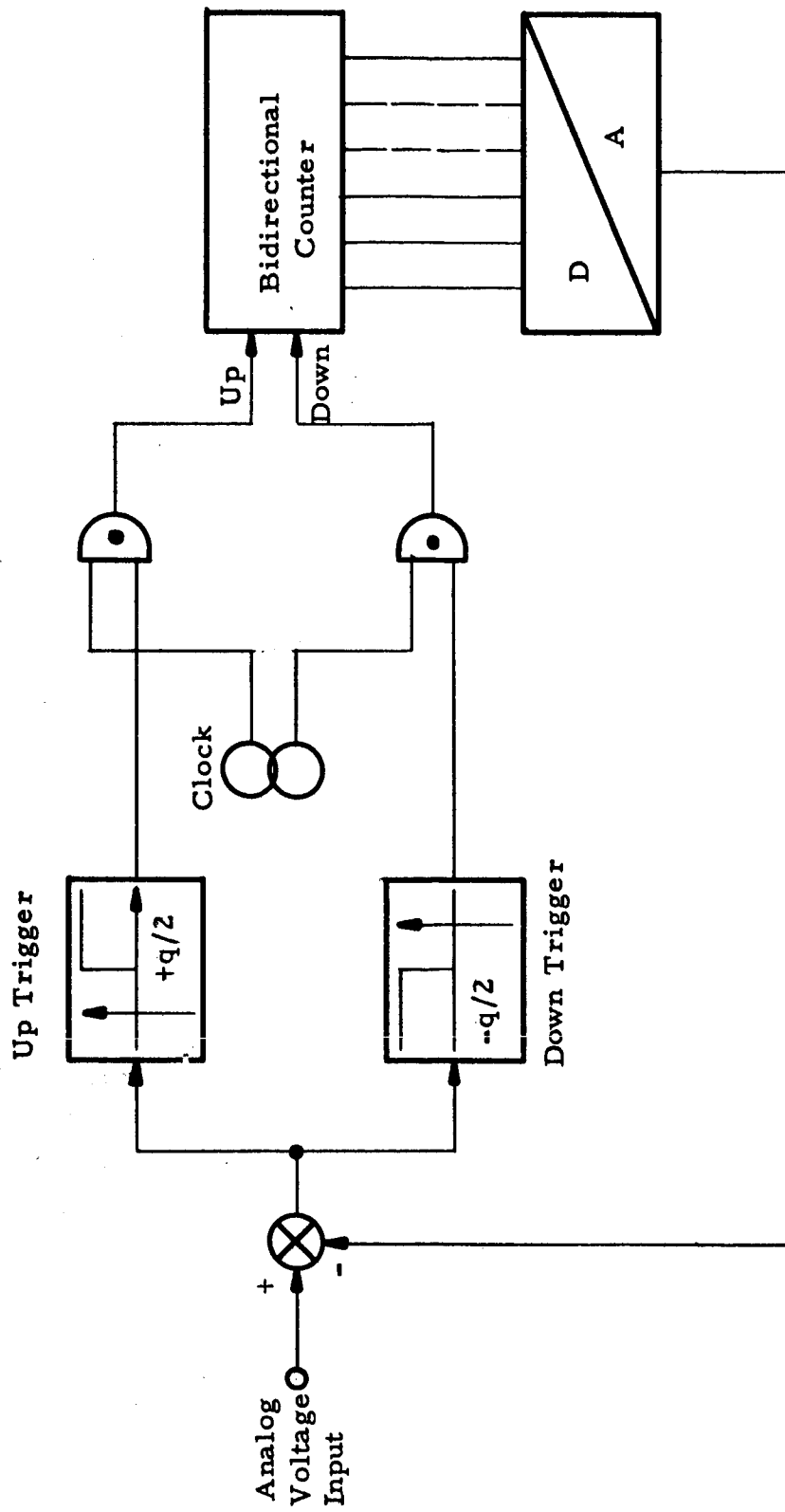
FIG. 12- SYNCHRONOUS CONTINUOUS BALANCE ENCODER

sitions can occur only at clock intervals; hence the converter output is both quantized and sampled, unlike that of a shaft position encoder. If, however, the clock (sampling) frequency is made sufficiently large, sampling effects can be made negligible and the overall encoder performance will very closely approximate that of the shaft position encoder or (quantizer).

2.4   Summary and Conclusions

On the basis of minimum logic requirements and the possibility of avoiding intermediate storage registers, the synchronous continuous balance method was chosen for the final A/D converter design. This method can also be easily converted to asynchronous operation provided that the analog voltage to be converted is sufficiently noise free. This then would eliminate the sampling present in the synchronous version, which might pose a problem, although the sampling rate for the constructed A/D was 10 kc which does not introduce an appreciable delay for most computations.

CHAPTER 3

DETAILED SYSTEM DESIGN

3.1 Introduction

In this chapter, the design of the complete system for interconnecting the GEDA and the Synthesizer will be discussed. The discussion covers three main areas; 1) D/A converter design 2) A/D converter design and 3) Design of an error counter and anti-coincidence logic for use in simulating a pulse-data control system. The final chapters will then be devoted to the analysis and performance of each subsystem as well as examples of overall system performance when simulating a typical control problem.

3.2 D/A Converter Design

The first portion of the system to be designed was the D/A converter since a similar D/A was also required for the synchronous continuous balance method of A/D conversion which was chosen for the encoder design.

3.21 Input-Output Diagram

The desired decoder characteristics are shown in Fig. 13. A zero d.c. voltage appears at the output when the digital input is binary 128 (10000000). The output appears as a series of equally
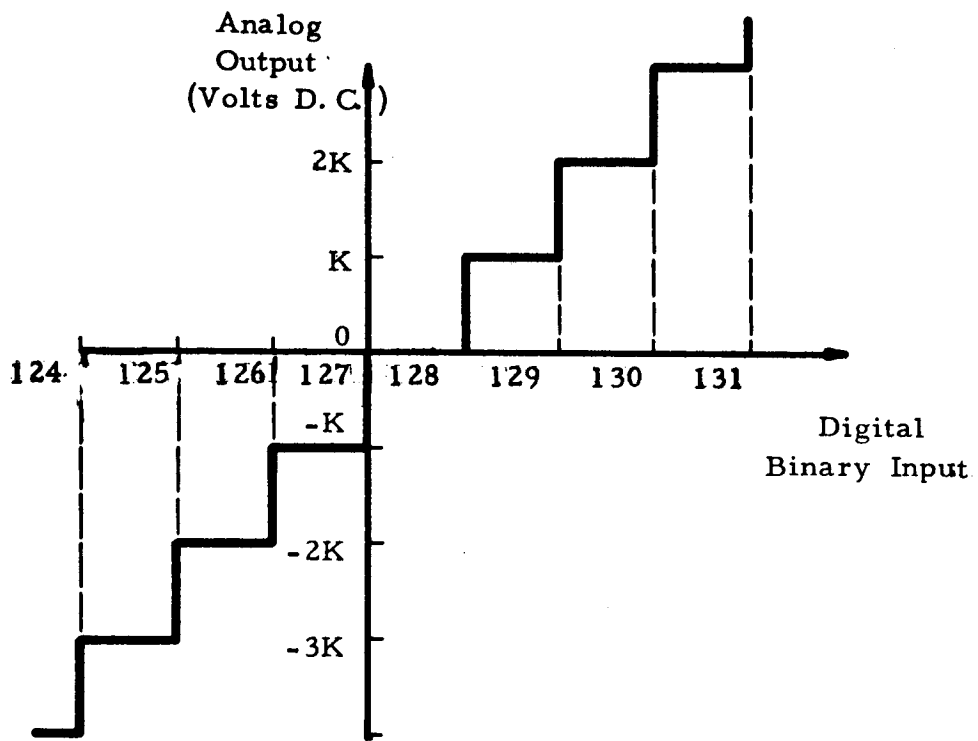
FIG. 13 STATIC INPUT/OUTPUT CHARACTERISTICS
FOR D/A CONVERTER

spaced levels, K volts apart, where K is any positive number less than one. Thus the largest output voltage corresponding to one least-increment (quanta) input is one volt. In order to obtain a larger quanta size, the number of allowable input bits must be reduced. For example, if a one quanta input change must produce a 32 v. output change (32 v. /quanta), set K=1 and use only the three most significant bits of the input, fixing the other five bits at "0". The maximum allowable output voltage range is ± 100 volts, which means that binary input numbers 229 through 255 and 0 through 28 won't normally be used except as extra states to prevent D/A "overflow."

3.22 Typical Bit Design

The switched-input-resistor decoder operates on the same principle as an analog computer summing amplifier; that is, the basic input-output relationship that applies is:

$$\frac{e_o}{e_i} = \frac{-R_f}{R_i} \tag{1}$$

where e_i and e_o are the input and output voltages respectively and R_f and R_i are the feedback and input resistors. This equation assumes the operational amplifier has infinite gain.

Fig. 14a. shows the arrangement for one bit of the de-
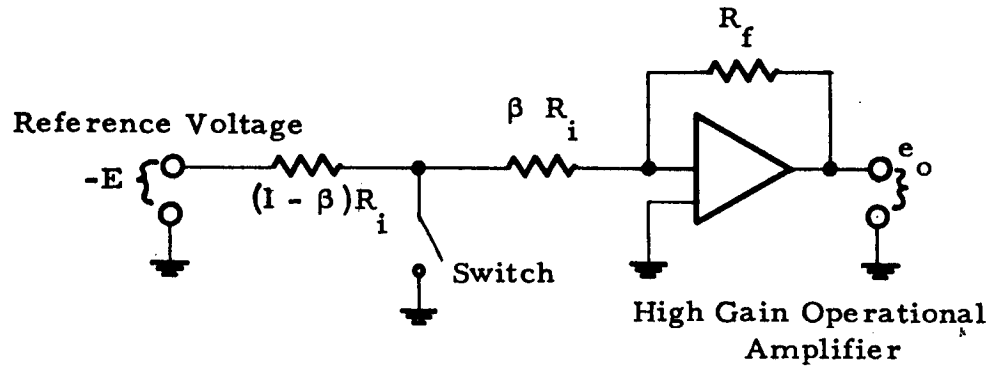
(a)
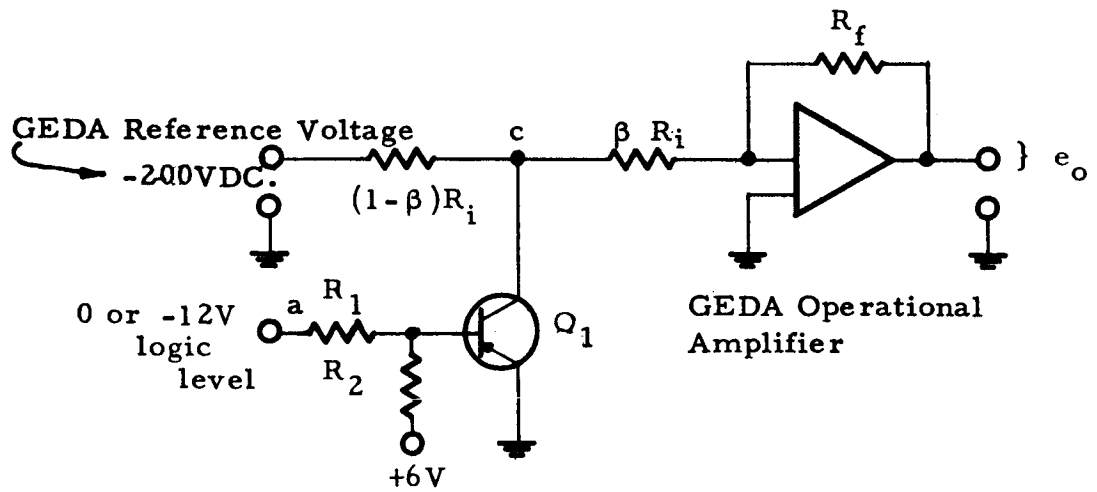
(b)

FIG. 14 TYPICAL DECODER STAGE

coder. With the switch open, the output voltage is:

$$e_o = E \frac{R_f}{R_i} \quad [\text{volts}] \qquad (2)$$

This condition corresponds to the bit being "on", ie., the binary

digit for this particular bit position is a 1. If the switch is closed,

the effective input voltage will be zero (ground); hence the output

voltage must also be zero.

There are many advantages in using this circuit. The

problem is to obtain a simple decoder that will switch high analog

voltages with reasonable speed when actuated by low level digital

voltages. The solution is as shown in Fig. 14b. One requirement

for accurate D/A conversion, a stable, well-regulated reference

voltage, was met by utilizing one of the GEDA's 200 volt reference

supplies. Compatibility with the Synthesizer outputs was insured by

using a medium speed transistor (Q_1), similar to those used in Syn-

thesizer logic cards, for the transistor switch. The 2N1309 was

chosen because of its high beta (80-150), low leakage current (6μa),

relatively high maximum collector voltages (-30v.), and low collect-

or to emitter saturation voltage (-0.1v). β was chosen such that the

voltage at point "c" of the voltage divider formed by resistors $(1-\beta)R_i$

and βR_i never exceeds the maximum allowable collector voltage for transistor Q_1. One GEDA amplifier was used to effectively sum and amplify the weighted digital inputs. Resistors R_1 and R_2 were chosen so that with -12 volts applied to point "a", Q_1 is well into saturation, and the collector very close to ground. Also, with point "a" at ground, the base of Q_1 is biased positively with respect to the emitter to reduce the collector leakage current and make the transistor closely resemble an open switch. It is not necessary that Q_1 have either zero or infinite collector-to-emitter impedance, but only that the collector current be switched between two stable values. If, however, the two states chosen are cutoff and saturation, variations in collector current due to gain and temperature variations will be minimized.

3.23   Actual Bit Design

The equation describing the input-output relationship for the D/A converter is:

$$ e_o = -E R_f \left\{ \frac{a_o}{R_o} + \frac{a_1}{R_1} + \cdots \frac{a_n}{R_n} \right\} \qquad (3) $$

where a_o, a_1, ------ a_n are binary weights 0 or 1, which indicate the presence or absence of a particular bit, and where R_o, R_1, ---- R_n

are a series of binary weighted resistors. For an eight-bit con-
verter, equation (4) becomes:

$$e_o = -E\ R_f\ \{\frac{a_o}{128R_i} + \frac{a_1}{64R_i} + \frac{a_2}{32R_i} + \cdot \cdot \frac{a_7}{R_i}\} \qquad (4)$$

E is specified as -200 v. d. c. from the GEDA reference supply.

With all bits "on", the total resistance seen by the -200 volt supply

to ground is $\frac{128}{255}R \sim \frac{R}{2}$. Total current drain from the -200 supply

was desired to be less than 5 ma, therefore the minimum value for

R is 80K ohms. This requires that the largest input resistance,

128R, be 10.24 megohms.

β (max.) was chosen as 0.1, which limits the voltage at

points "c" (Fig.14b.) to -20 volts when Q_1 is cut off. This is well

within the maximum allowable collector-to-emitter voltage for a

2N1309 (-30 v. d. c.).

To avoid using very expensive low tolerance input resis-

tors, $\beta\ R_i$ resistors are wire wound variable resistors and $(1-\beta)R_i$

are 1% deposited carbon fixed resistors. The 1% tolerance assures

that the fixed resistances will not differ enough from nominal values

to cause difficulty when trimming up the bits with the variable re-

sistors. The nominal total input resistance values were finally sel-

ected as 75K, 150K, 300K, 600K, 1.2M, 2.4M, 4.8M, and 9.6M

ohms, most significant through least significant bit respectively.

3.24 Detailed Converter Diagram

Fig. 15 is the circuit diagram for the actual D/A con-
verter. The ideal desired operation can be described by noting

the most significant bit (marked "128") in Fig. 15. When this bit

is "1" (on), the transistor is cut off and a current flows to the input

of the operational amplifier produced by the -200 volt supply volt-

age impressed across the 68.1K resistor and 10K pot combination.

The operational amplifier thus produces an output voltage propor-

tional to the current flowing into its input. When the first bit

is off, the transistor is conducting in saturation and its collector

is at ground. Therefore no current flows through the 10K pot into

the operational amplifier and its output voltage is zero. Actual

operation may differ from the ideal because a) the transistor can-

not be completely cut off, and b) a finite collector-to-emitter volt-

exists when the transistor is turned full "on". A discussion of the

errors incurred because of these two reasons will be found in

Chapter 4.

Note in Fig. 15 that a +200 volt bias is included. The

bias resistance is made equal to the resistance of bit eight so that

when only bit eight is "on", the positive bias current cancels the
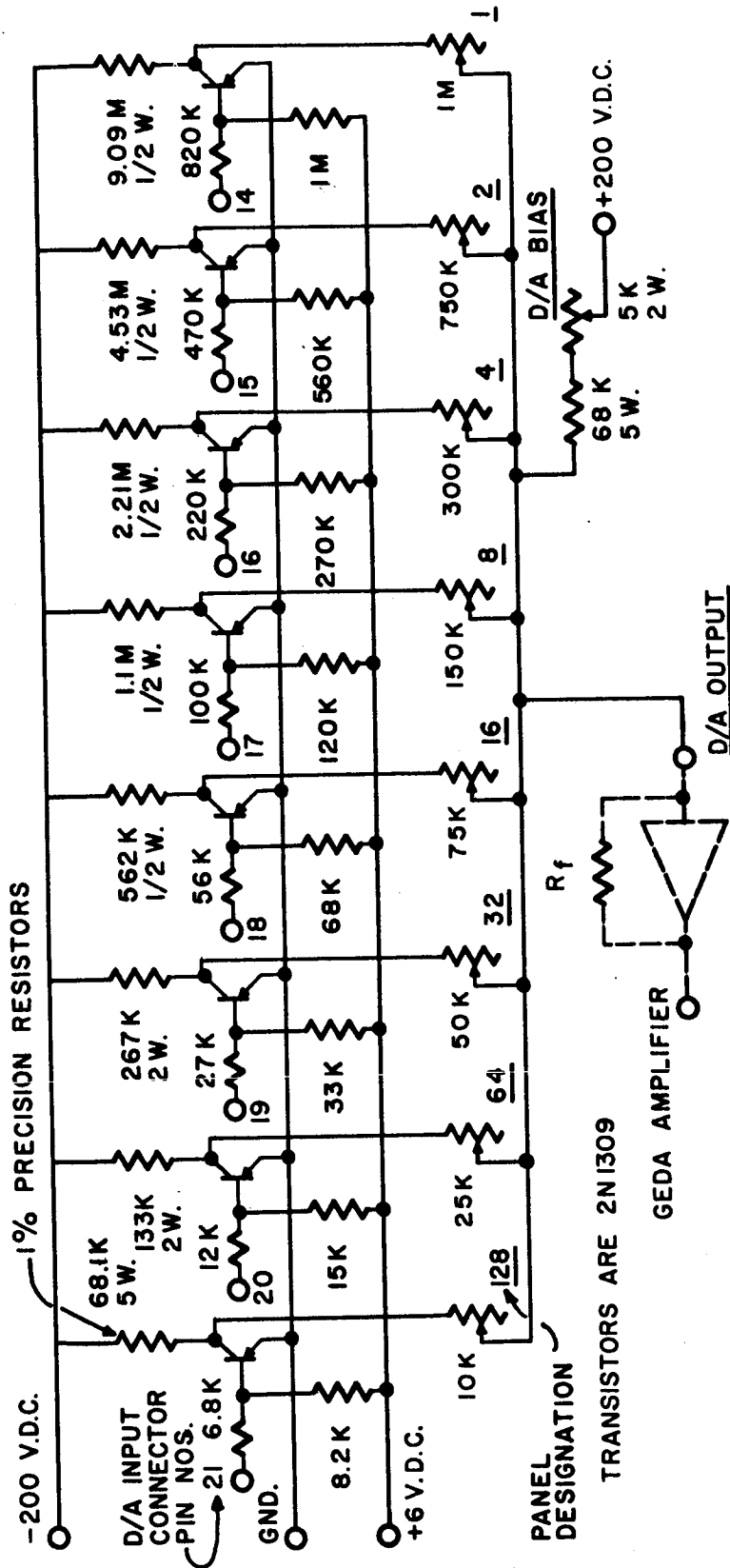
FIG. 15 - DIGITAL-TO-ANALOG CONVERTER

negative bit current and the operational amplifier output is zero.

The operational amplifier feedback resistor, R_f, in Fig. 15, is a plug-in variable decade resistor which is supplied with the GEDA. As indicated previously, for a quanta size of one volt, R_f must be adjusted to approximately 48K, depending upon the actual bit resistor values.

3.3 A/D Converter Design

The synchronous balance A/D converter consists of three basic sections; bidirectional counter, D/A converter and summing amplifier, and comparator. An overall system description will be given and the design of each section then explained.

3.31 Input/Output Diagram

The A/D converter must provide two separate outputs; one incremental and one absolute. Fig. 16 shows the input/output relationships for the converter, both incremental and absolute.

Fig. 16 (a) indicates that when the analog input voltage is zero, the encoder output is 10000000. This number appears both on binary output lines as 0 or -12 volt levels and on a row of display lights where an "on" light indicates a "1", off indicates a zero. Both
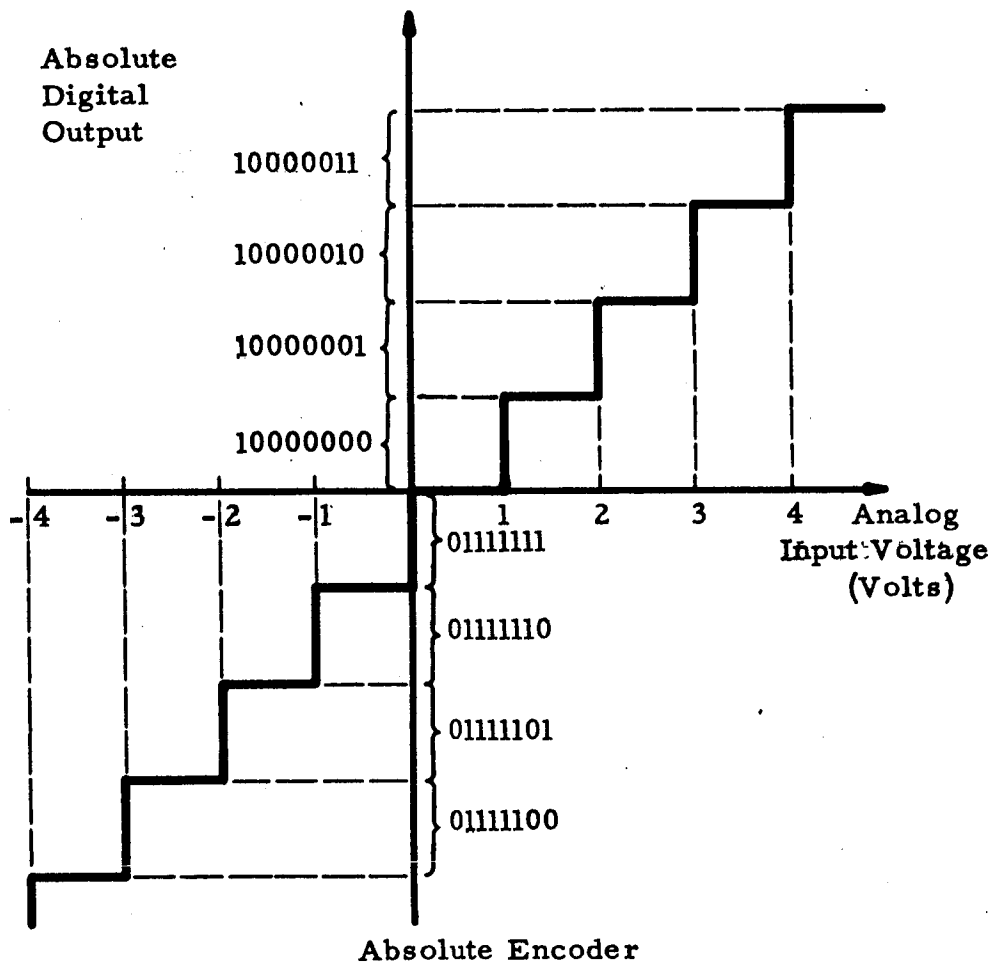
FIG. 16a - ANALOG-TO-DIGITAL
CONVERTER INPUT-OUTPUT DIAGRAM

the complement and asserted form of the number are available.

Note that the digital output changes when the analog input voltage

takes on integer values. This arrangement is arbitrary, and the

actual converter can be altered so that changes occur at one-half

volt points (ie., -0.5, 0.5, 1.5, 2.5, etc.) if so desired.

Fig. 16 (b) shows how incremental (pulse) outputs occur

for a typical analog input voltage variation. Two output terminals

are provided; one for "+" and one of "-" incremental pulses, of -12

volt amplitude and 15 μ sec. duration. A pulse is emitted from the

"+" incremental output terminal each time the analog input voltage

assumes an integer value and is increasing positively. Similarly a

"-" pulse is emitted whenever the analog input voltage passes a

"quanta line" (integer voltage value) increasing negatively.

3.32 Complete System Operation

The overall A/D converter is shown in block diagram

form in Fig. 17. This diagram is an elaboration of Fig. 12, which

showed the basic synchronous continuous balance encoder. The con-

verter consists of an eight bit binary bidirectional counter, a pair

of Schmitt triggers for level sensing, a D/A converter of the type

previously discussed, and provisions for a lighted display, a synch.
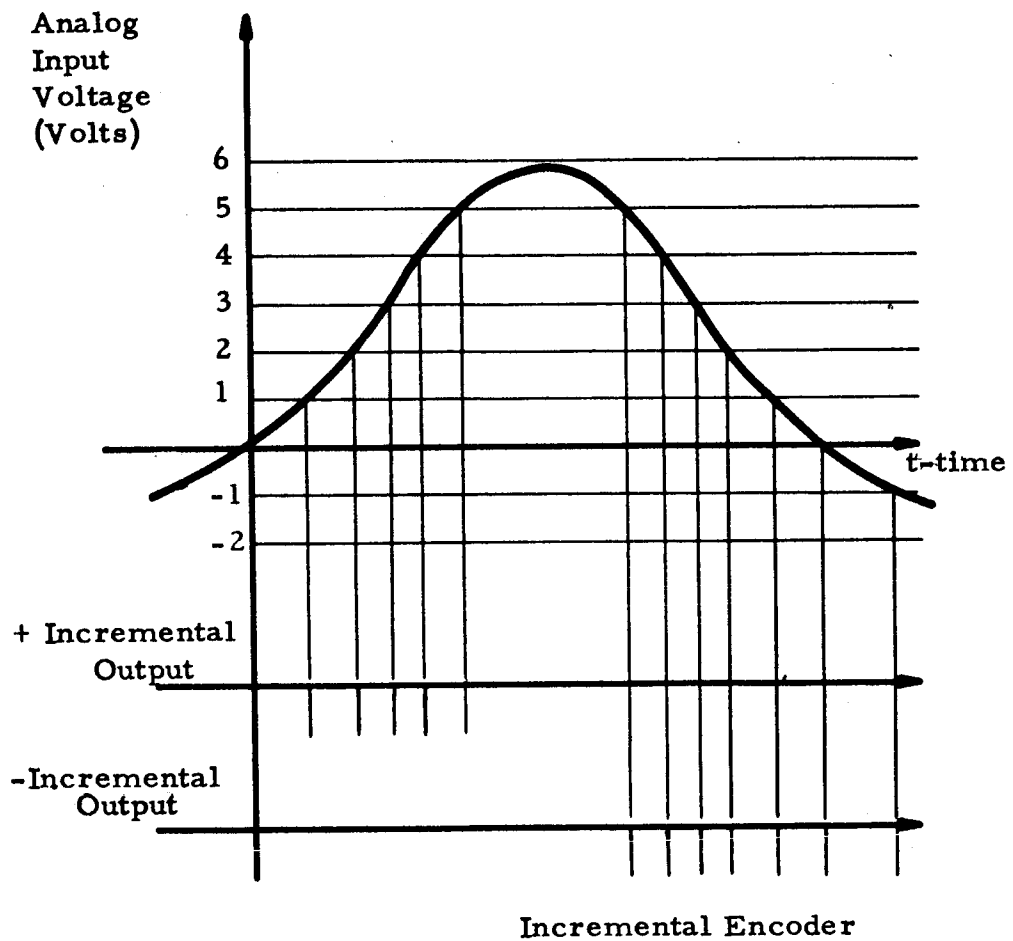
FIG. 16b - ANALOG-TO-DIGITAL CONVERTER
OUTPUT DIAGRAM
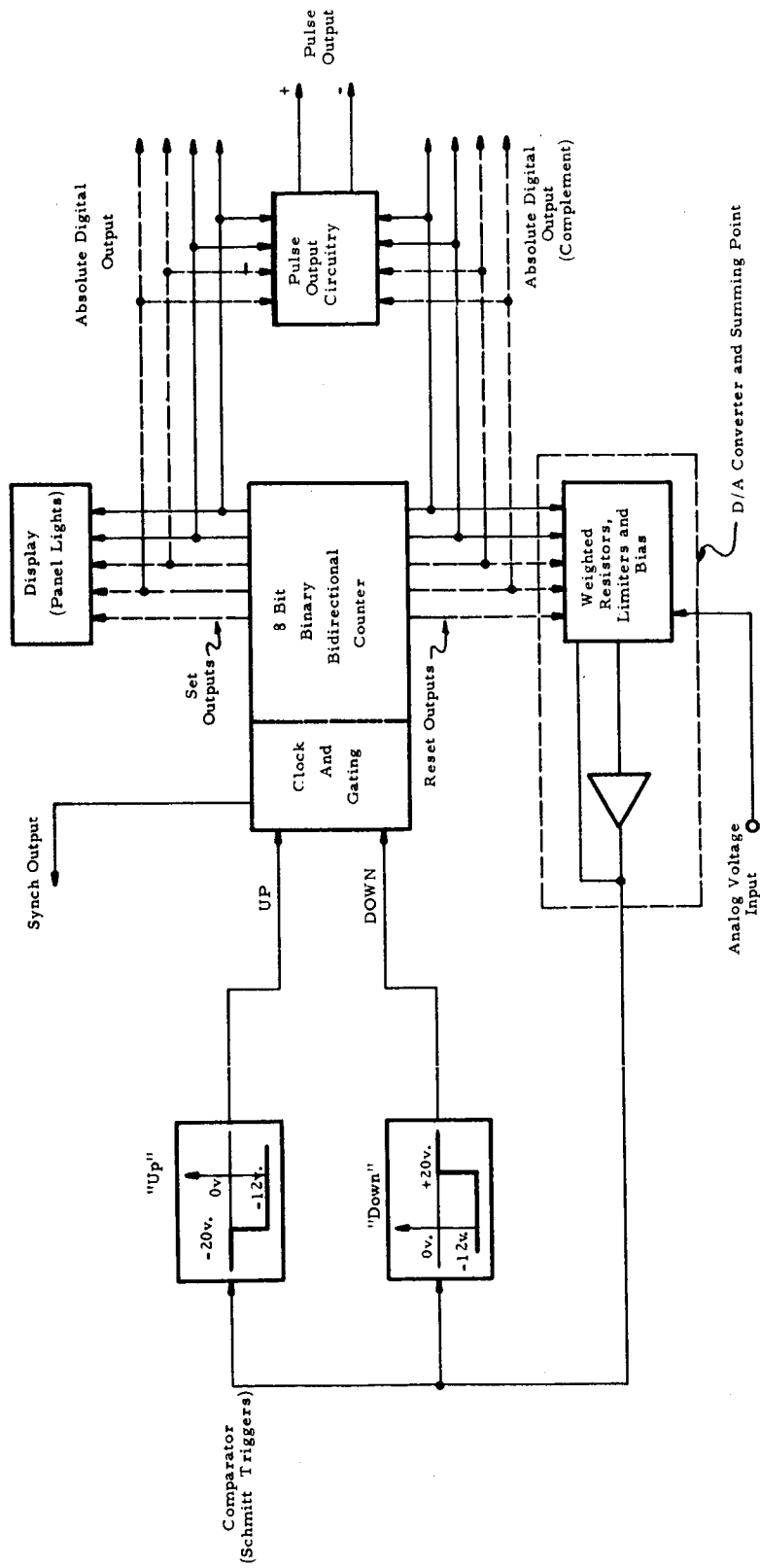
FIG. 17 A/D CONVERTER - BLOCK DIAGRAM

output, absolute outputs and incremental outputs. Overall system

operation can be best understood by referring to the timing diagram

of Fig. 18 and the block diagram of Fig. 17.

A typical triangular-wave analog input voltage is shown,

going from 0 v. to +3.5v. and back to 0v. Quanta size is 1.0 volt,

as indicated in Fig. 16. The D/A converter and summing point am-

plifier is biased such that when the analog input voltage is zero, the

counter contains 10000000 and the amplifier output is +20 volts. The

analog input is amplfied and inverted by the summing amplifier so

that a 1.0v. change at the input appears as a -40.0v. change at the

output. The two Schmitt triggers serve as a comparator, produc-

ing -12 to 0 volt level changes whenever the amplifier output exceeds

± 20.0 volts. Thus the two triggers combined have the characteris-

tics of a dead zone relay. The A/D clock is a free running multivi-

brator, alternately producing "up count" and "down count" pulses

which are gated into the counter by the trigger outputs.

The A/D converter's operation will now be examined

for the given triangular-wave input. As the analog input passes zero

volts, the "up" trigger flips from -12 to 0v., thereby allowing an

"up" pulse to count the counter up by one. As the analog input goes
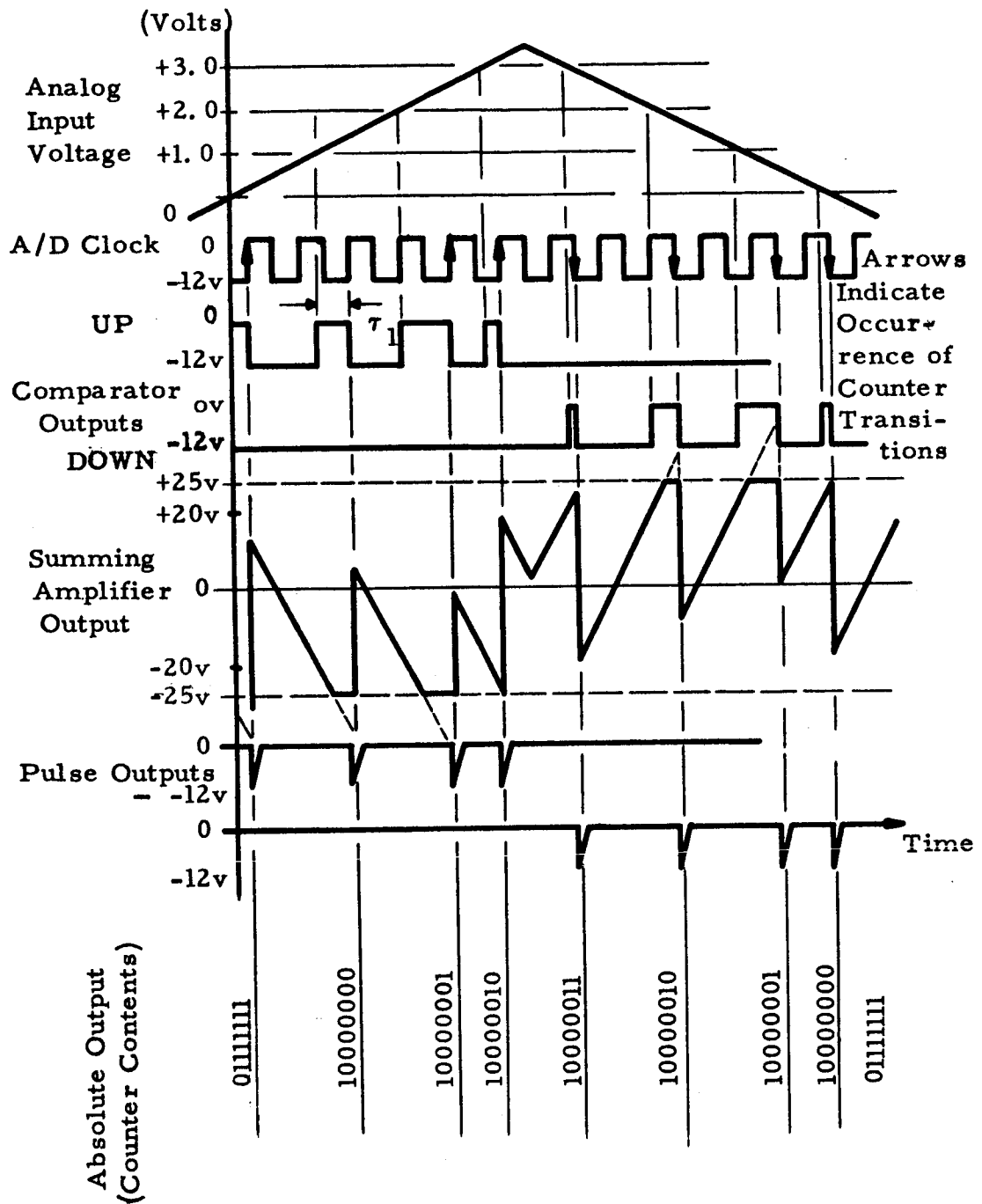
FIG. 18 - TIMING DIAGRAM - IDEAL A/D CONVERTER

from 0 to +1.0 volt, the amplifier output is going from +20v. to -20v.

When it reaches -20v., the "up" trigger changes state once again,

but the counter is not counted up until the next A/D clock transition,

$\tau_1\mu$ sec. later. Note that limiters hold the amplifier output at -25v.

during this delay period so that the triggers aren't overdriven. Af-

ter the clock counts the counter up, the change in counter state is

sensed by the D/A converter, which adds a voltage increment (40

volts) to that appearing at the amplifier output. Thus the amplifier

output rises past -20v. towards ground (to about +6v. in this case)

and resets the "up" trigger. This same action is repeated again as

the analog voltage goes to +3.5v. and back to 0v. The digital out-

put can be taken as the state of the counter (0v. = 10000000) or as

"+" and "-" pulses. Note that these pulses can only occur at clock

transitions and therefore the converter input-output relationship is

not precisely that as shown in Fig. 16(b). The example given for

the timing diagram is typical of the case when the A/D clock fre-

quency is low compared to the slope of the analog input. For further

discussion of this problem, see Chapter 4. Fig. 18 does not truly

describe the actual converter because:

      1)   Finite rise time of the summing amplifier has been
              neglected.

2) Limiters are assumed to be ideal.

3) All signals are assumed to be noise free.

4) Each count, when fed back, is assumed to cause an exact 40 volt change in the summing amplifier output.

Actual converter operation, including the above effects, will be examined in Chapter 4.

3.33 Design of D/A Converter-Summing Point Subsystem

This portion of the A/D converter is quite similar to the D/A converter discussed in sections 3.2-3.24 with a few modifications. Fig. 19 shows the actual D/A and summing point assembly. The D/A is driven from the reset outputs of the bidirectional counter flip-flops.

The GEDA operational amplifier is connected into the circuit by use of patchcords between amplifer input and output and the appropriately marked jacks on the front of the converter. All A/D converter adjustment pots are located on the back panel of the unit. They include pots for bias adjustment, analog input weighting (for minor quanta size variation), operational amplifier feedback resistance (for hysteresis adjustment), and eight pots for D/A bit adjustment. The circuit for limiting the GEDA amplifier output is

-50-

FIG. 19 - 8 BIT D/A FOR A/D CONVERTER
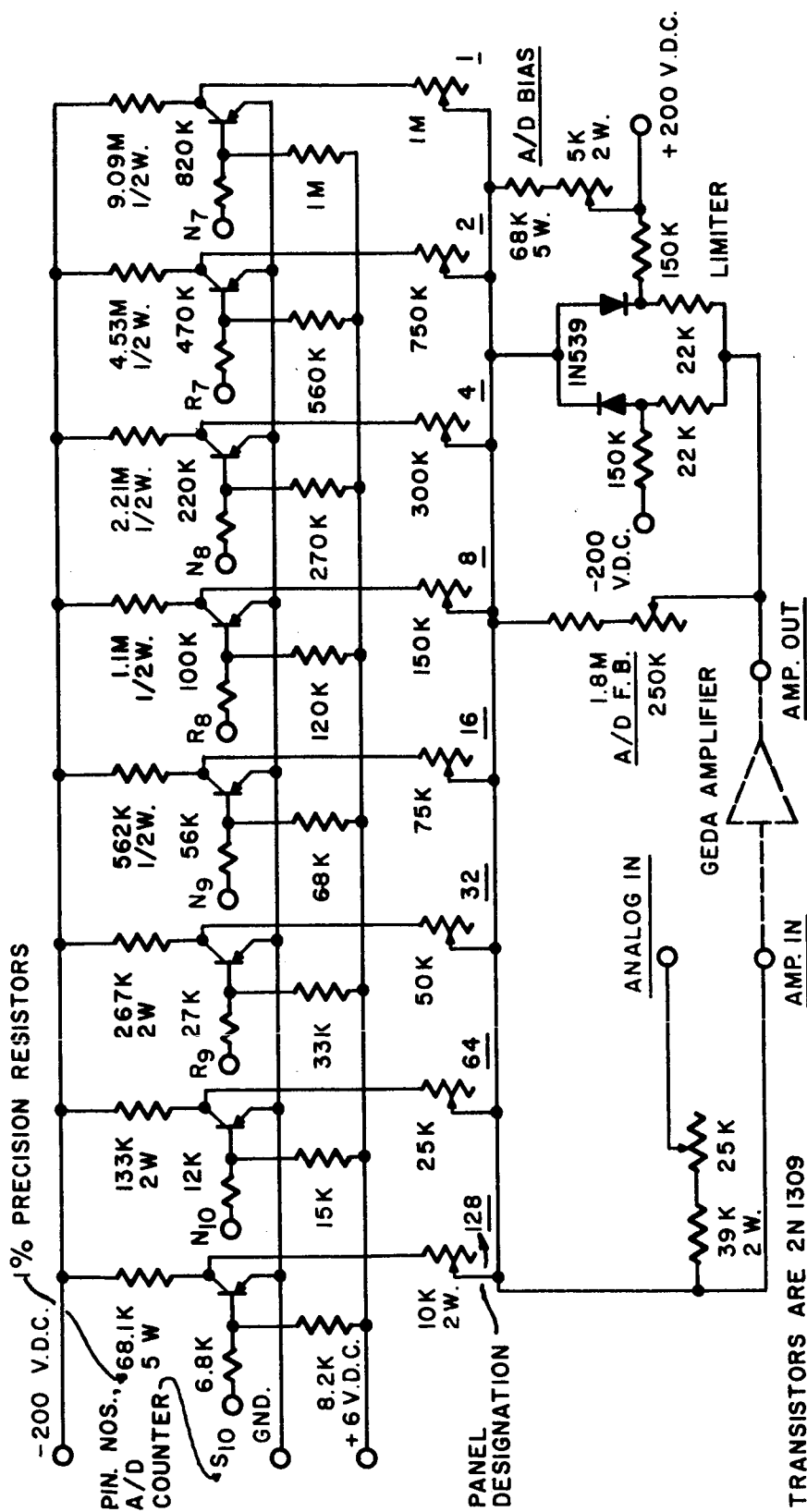
a standard diode limiter circuit and provides limit voltages of about $\pm$ 25 volts.[8]

Since a one count counter change should vary the amplifier output voltage by 40 volts, and the bit resistance for the least significant bit is nominally 9.6MΩ; the feedback resistance can be calculated as:

$$e_o = -e_i \frac{R_f}{R_i}$$

$$= -(-200v.)\frac{R_f}{9.6M\Omega} = 40v.$$

$$\therefore R_f = 1.92M\Omega \text{ nominal.}$$

Now that R_f is specified, R_a, the analog input resistance can be specified, since for a one volt analog input change the amplifier output must change by 40 volts.

$$\frac{e_o}{e_i} = \frac{-R_f}{R_i} = \frac{40v.}{1v.} = \frac{1.92M\Omega}{R_i} \quad;$$

Therefore, R_i = 48K nominal. The bias resistance, R_b, was chosen equal to the resistance of the most significant bit resistance (75K nominal) since both are tied to reference voltages of equal magnitude but opposite polarity ($\pm$ 200v.).

3.34 The Comparator

Choice of the analog comparator was based on the fol-

lowing criteria.

1) Rapidly changing digital output signals (0 to -12v.) must be produced whenever the analog input is greater than a positive reference voltage or less than a negative reference voltage.

2) The detection levels must be sufficiently high so that maximum accuracy and repeatability can be obtained from the GEDA amplifier.

3) The signals indicating positive and negative equality must appear on separate output lines.

Transistorized Schmitt trigger circuits were chosen as the level detection (comparison) means because of their compatibility with Synthesizer logic, good constant-temperature stability, and high speed. Two triggers are used, one changing state when the input reaches some negative reference voltage, and the other doing the same for positively going voltages.

As a compromise, plus and minus 20 volts were selected as the trigger levels, high enough to prevent noise or voltage spikes from causing false outputs and low enough so that the GEDA summing amplifier being used doesn't swing over its entire operating range, thereby reducing bandwidth. (Due to non-linearities, amplifier bandwidth is lower for large output swings.)

The twin trigger circuits are shown in Fig. 20. The

-53-

FIG. 20 - COMPARATOR SCHEMATIC
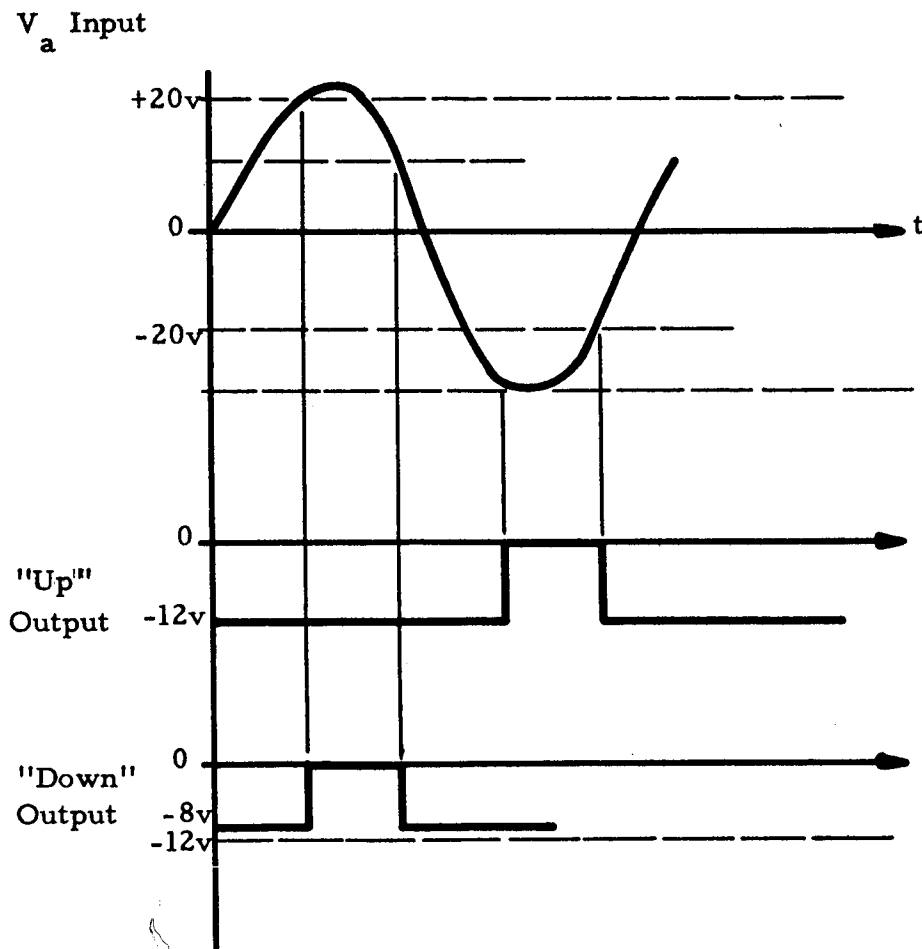
FIG. 21 - COMPARATOR OUTPUTS

circuits are complementary, being identical except for the type of transistor used (PNP or NPN). An inverter is used on the "up" trigger output so that both triggers, when activated, produce output levels of zero volts, which are correct for gating pulses into the bidirectional counter.

The normal -12v. logic supply voltage ($\pm$ 5%) was not accurate enough for the Schmitt trigger negative supply. Therefore, a Zener diode was used to regulate V_{cc} to -11v., $\pm$ 1%. Regulation against load current variations is not critical, because just before either trigger trips, both Q_2's are always on, and the current drain from the -11v. supply is constant.

3.35 Bidirectional Counter and Logic

Fig. 22 shows the bidirectional counter, clock, input gating, and pulse output gating. The operation of this sub-system is quite straight forward, but will be explained briefly.

Count pulse source (A/D clock) is the 10KC. free running multivibrator (FRMV) (5). (Numbers are those on Fig. 22 and refer to logic card locations.) The counter is composed of four Type 302 two bit binary bidirectional counter cards. Being asyn-chronous, the counter is quite simple and requires only 24 transis-
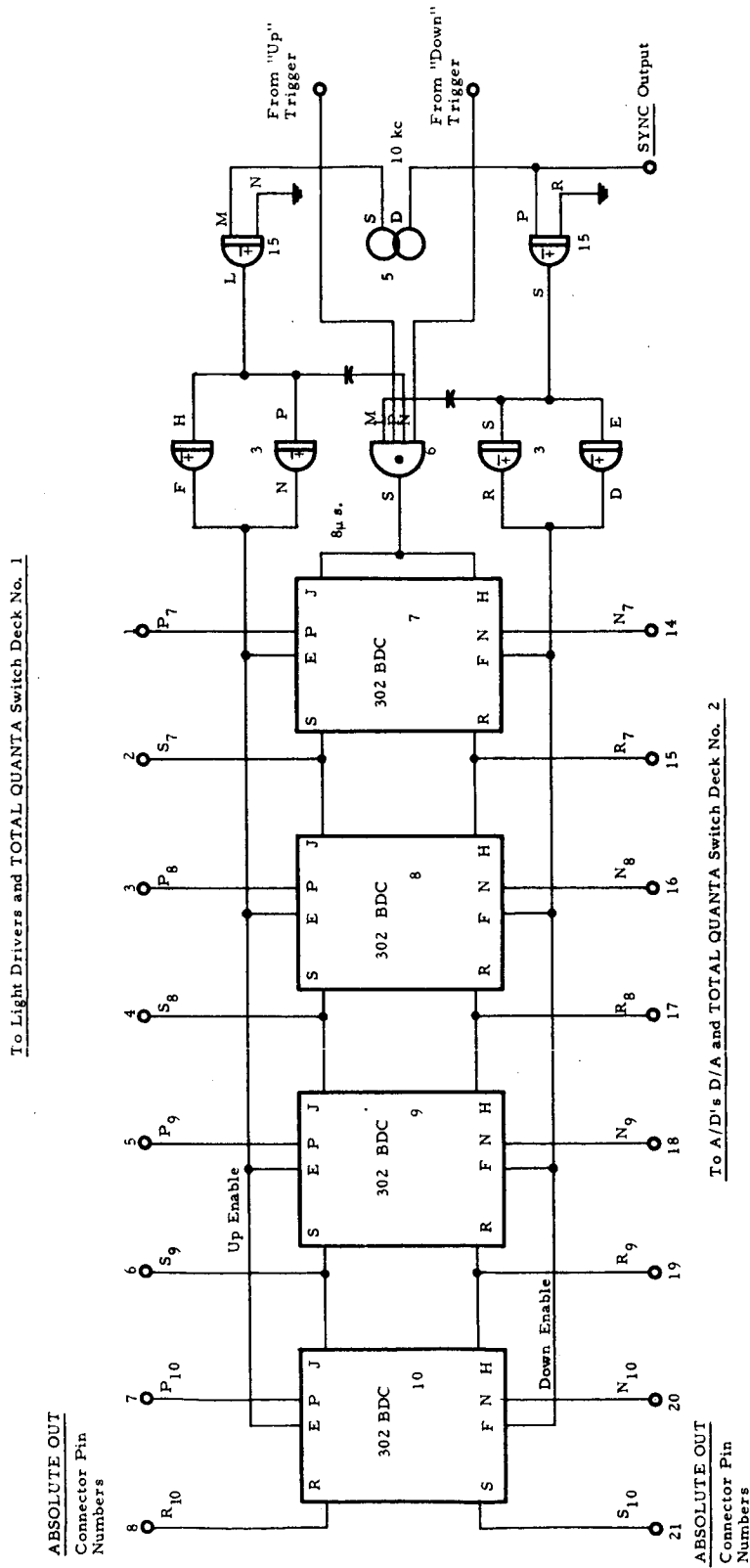
FIG. 22 8 BIT A/D COUNTER

tors. FRMV (5) alternately enables (sets at 0v.) the up enable and down enable lines. Also, suitable -12v. to 0v. transitions are produced on the pulse input lines (M and P) of Type 308 multi-input gated pulse generator (MIGPG) (6). Up count pulses will occur whenever FRMV (5) produces -12v. to 0v. transitions on multi-input GPG (6) line M and GPG (6) line L is held at 0v. by the up output of the comparator. Similarly, the counter will be counted down when positive going transistions appear at MIGPG (6) line P with MIGPG (6) line N enabled by the comparator's down count output. Thus, counter transitions occur only at A/D clock transistions, and the clock frequency is such that a worst-case counter carry propagation can be completed within one-half clock period.

The pulse output gating (Fig. 23) permits the detection of up and down counter transitions at any bit position (flip-flop). The procedure for quanta size variation is simply to trigger "+" or "-" pulse output gated pulse generators from lesser or more significant counter bits. For example, if the finest quantization is desired (1v. per quanta), counter input pulses from MIGPG (6) line S are switched to the pulse inputs of GPG's (4), lines F and K, GPG (4) enable lines, E and J, are permanently connected to counter up
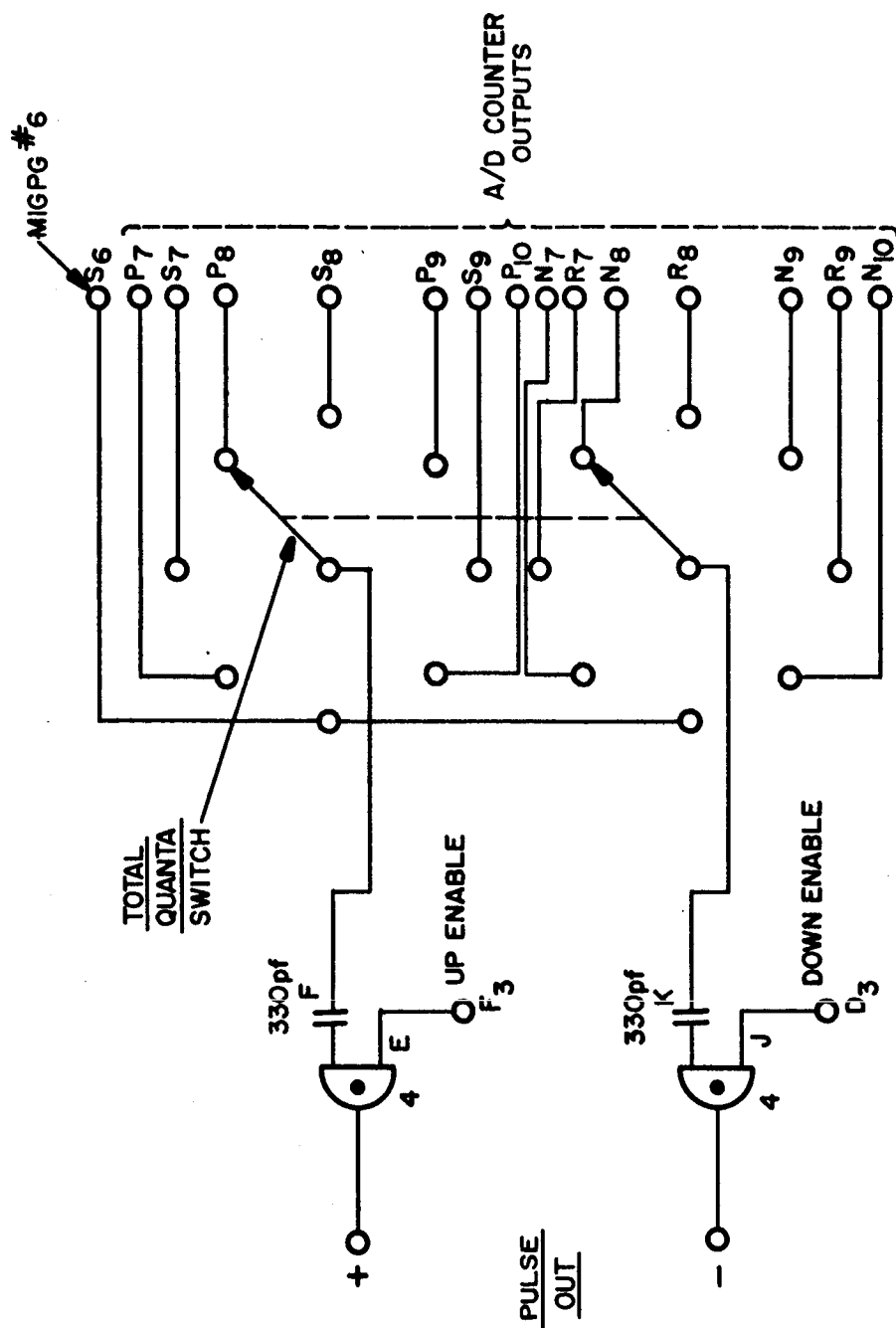
FIGURE 23 A/D CONVERTER PULSE OUTPUT LOGIC

All counter flip-flop outputs (set and reset) are brought out to the front panel in a single connector labeled ABSOLUTE OUT. Also FRMV (5) line D is brought out in front as the SYNC output. Use of these connections is made when constructing an absolute control system. Refer to Chapter 5 for further explanation.

3.4 Pulse Data System

The main use for the D/A and A/D converters designed is in the investigation of the dynamics of discrete (digital) control systems. One of the simplest types of digital control systems to implement is the pulse-data or incremental system (Fig. 2). Although simple, it produces many difficult problems in the area of transient and steady state analysis with regard to stability, quanta size, input type and amplitude, noise, drift, and nonlinearities in the continuous (analog) portions. Thus there is still much to be learned about pulse-data type systems, and more design techniques for such systems need to be developed. It was therefore decided to include the digital hardware for one pulse-data loop (counter and anticoincidence circuit) with the A/D - D/A package.

3.41 Error Counter and Anticoincidence Circuit

Fig. 24 shows the pulse-data system logic. A four bit

enable and down enable lines so that a "+" (up) transition can be differentiated from a "-" (down) transition. If coarser quantization is desired, say 8v. per quanta, the TOTAL QUANTA switch on the front panel is turned to 32 which will connect the outputs of the third counter flip-flop, P_8 and N_8, to pulse output GPG's (4). Now, only every eighth pulse (of the same polarity) at MIGPG (6) line S will effectively appear at the front panel PULSE OUTPUT terminals ("+" or "-" as the case may be).

Additional counter output connections are also noted on Fig. 22 and Fig. 17. The counter state is displayed on eight front panel lights connected through light drivers to the counter "set" outputs (lines S and P). One exception is that "set" and "reset" designations on the most significant flip-flop are interchanged (R_{10} and S_{10}). This is done because when all flip-flops are reset by the manual RESET button provided, the desired counter setting (corresponding to an analog input of zero volts) is 10000000. The "reset" sides of all flip-flops (N or R, except as just noted) are connected to the corresponding D/A converter inputs. This is because the zero volt level present at the "reset" side of a "set" flip-flop is correct for causing the corresponding D/A bit to turn on.
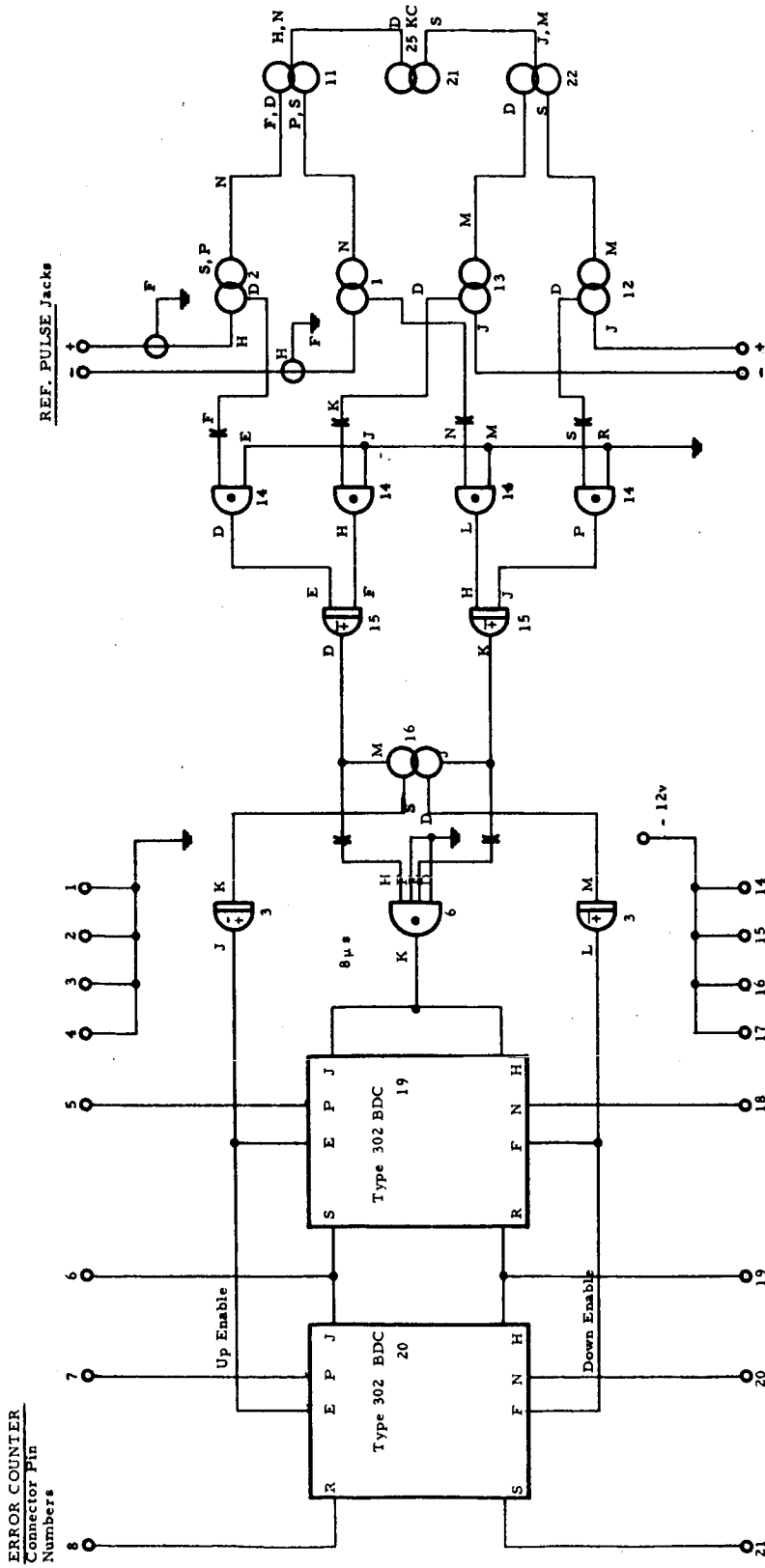
FIG. 24 - ERROR COUNTER AND ANTICOINCIDENCE CIRCUIT

Note:
1) Flip-flops 1, 2, and 11 are Type 201
   Flip-flops 12, 13, 16, and 22 are Type 311.

2) FRMV 21 has J, K and L, M jumped with 33K resistors.

3) Flip-flops 12, 13, and 16 are modified as follows
   a) J input gate resistor connected to C
   b) C is grounded
   c) 16 also has M input gate resistor connected to C.

binary bidirectional counter, composed of two Type 302 two bit

BDC cards, is used as the error counter. Maximum system error

is then limited to +7 or -8 quanta, which is sufficient for almost any

system.

Flip-flop (16) receives up and down count pulses from

the anticoincidence circuit outputs, NOR 2 gates (15), lines D and K,

and controls the counter direction. MIGPG (6) (output K) delays

the input pulses so that count pulses don't enter the counter until

the appropriate enable lines have been enabled.

The anticoincidence circuit is of a standard design and

serves to prevent simultaneous or nearly simultaneous feedback or

reference pulses from causing loss of a pulse. Its operation can be

best understood with the aid of timing diagram of Fig. 25. Anti-

coincidence clock (FRMV (21)) causes reset pulses to be sent to

flip-flops (2), (13), (1), and (12) successively through pulse fre-

quency dividing flip-flops (11) and (22). If a random pulse occurs

on the "+" reference input (see Fig. 25), flip-flop (2) will be set.

At the next clock time at which a -12v. to zero transition occurs on

frequency divider flip-flop (11), line F-D, flip-flop (2) will be reset.

A -12v. to 0v. transition on flip-flop (2) line D causes a negative
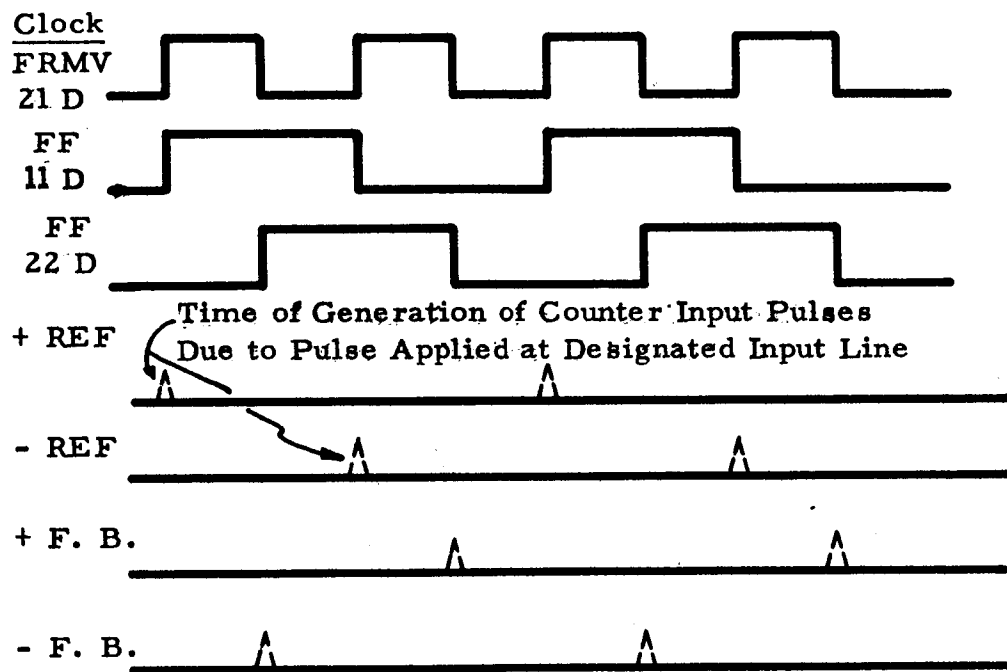
FIG. 25 - ANTICOINCIDENCE CIRCUIT TIMING DIAGRAM

pulse to be emitted from GPG (14), line D, and subsequently the counter is counted up by one.

Simultaneous occurrence of a reset and set pulse on, for instance, flip-flop (2), resulting in a lost pulse, is not a problem. This is because flip-flops (1), (2), (12) and (13) are basically J-K types, thus they will change state upon simultaneous set and reset pulses. The next clock pulse will then reset the flip-flop as desired.

Near coincident set and reset pulses on flip-flops (1), (2), (12), or (13) could conceivably result in the production of "sliver" pulses, whose widths are too narrow or heights too low to properly trigger the gated pulse generators. This does not present a problem because of the manner of attachment of the reset side steering gates' "enabling" resistors. The resistor is tied to the reset output, which is at -12v. when the flip-flop is reset, thereby disabling the steering gate. In order for the steering gate to pass a pulse, its resistor must have been at ground potential for approximately 2 μsec., determined by the RC combination of the gate. This means that the set side must be at -12v. for at least 2μsec. before a reset pulse is allowed to change it back to 0v. Proper op-

eration is thus assured, because a 2 μ sec. pulse is sufficiently wide to trip a GPG. Note that set side steering gate resistors of flip-flops (1), (2), (12) and (13) are permanently grounded, thereby avoiding any steering gate delay and allowing faster operation. Also, the anticoincidence clock frequency must be more than twice as fast as the maximum reference or feedback pulse frequencies to insure that two input pulses never occur on the same line before a resetting clock pulse can occur.

3.5 Summary

The A/D converter, D/A converter, and pulse data system just discussed has been designed with primary attention to low cost, simplicity, flexibility and reliability. Some of the advantages and disadvantages can now be noted before discussion of actual performance data and use in problem simulation.

The two D/A converters are both of the weighted resistor type. This permitted use of less expensive higher tolerance resistors than would have been required had a ladder type decoder been used. The numerous adjustable resistors required, however, pose a real problem in "tuning" the converters for the desired accuracy.

Use was made of both the GEDA ± 200v. regulated d. c.
power supplies and commutator stabilized operational amplifiers,
thereby saving on an added regulated power supply and practically
eliminating any drift introduced in amplification. Of course, the
unit, as designed, is pretty much limited to use with the GEDA, al-
though any similar ± 100v. analog computer will do, provided ± 200v.
regulated supplies are available.

The A/D converter simulates either a shaft position en-
coder or a quantizer. A slight sampling is present, however, but
will be shown to be negligible at normal GEDA operating frequen-
cies. Care must also be taken when using it in the absolute mode to
avoid the ambiguity problem present at counter transitions. The
sample problem in Chapter 5 will show how the ambiguity problem
can be overcome through proper synchronization.

A/D bandwidth will be shown to be primarily a function
of operational amplifier bandwidth, and thus is adequate considering
the required bandwidth of typical systems to be simulated. That is,
a higher bandwidth would not be of any particular advantage.

The adjustable bias adjustment and feedback gain ad-
justment for the A/D permit addition of hysteresis or shifting of

the zero point. Depending upon the accuracy of the A/D's omit D/A adjustment, the A/D may have to have as much as 20% of one quanta hysteresis to avoid undue noise. Such hysteresis is not uncommon to actual encoders, however. All of the above mentioned characteristics will be covered in more detail in Chapter 4 and 5 as the encoder and system operation are discussed.

CHAPTER 4

ENCODER AND DECODER PERFORMANCE
ANALYSIS AND EVALUATION

4.0   Introduction

In this chapter, a few definitions are first made, making

it possible to adequately describe A/D and D/A errors.   Next, anal-

yses of D/A and A/D errors are conducted so that maximum con-

verter errors can be predicted and theoretical error bounds estab-

lished.   Finally, actual operating data is compared to predicted val-

ues of converter error.

4.1   A/D and D/A Performance Parameters

The A/D and D/A are designed primarily for use in sim-

ulating digital control systems where one is interested in the effect

of quanta size (among other things) on stability.   This emphasis on

quanta size and quanta (switching) line placement lead to error defin-

itions based not on the analog input or output but on error as a per-

cent of one quanta.   The following list serves to establish a guide-

line in judging the performance of the A/D and D/A.[9,10]

(A)   Static Error: This is defined as the error (in per-
cent of quanta) between the digital input/output
number and the measured static analog output/in-
put voltage.   For the designed A/D, the "static
analog input voltage" is the value of a very slowly
positively going analog signal when the digital out-

put just changes (see Figure 16a). Thus A/D static accuracy can be made only at quanta lines.

(B) Monotonicity: This is defined as the variation of quanta size from the nominal value (one volt minimum in the designed A/D and D/A). Monotonicity is a measure of the variation in the incremental slope of a converter's input/output relationship, and it is most important that monotonicity be good for accuracy in digital control system stability investigations.

(C) Quantization Uncertainty: This is a measure of the finite width of a quanta line. Due to noise and hysteresis, a band of uncertainty will always surround the quanta lines.

(D) Zero Offset: This is the deviation of the ouput from the desired zero reading when the input is zero. Zero offset is adjusted with the bias control.

(E) Drift: This a measure of permanent changes in the zero offset over a long period of time, excluding variations due to ambient temperature fluctuation.

(F) Dynamic Error: All the previous definitions deal with error occurring when the input is fixed (or slowly changing). Dynamic error is the error incurred when the input is changing at a specified rate. Causes can be sampling or presence of time lags in the converter. Input rate of change is always specified when giving a dynamic error figure.

One term not mentioned above is absolute accuracy. Absolute accuracy implies static accuracy referred to some recognized absolute standard. Absolute accuracy will not be used in describing the designed A/D or D/A, because only accuracy with respect to the

"local" standards, which are the GEDA reference voltages, is important for our purposes. It is this accuracy which determines the overall problem simulation accuracy.

4.2 D/A Converter Error Analysis

The D/A converter, in addition to being used in a servo-system forward loop to convert the digital error signal, appears a part of the designed A/D converter. For this reason, an error analysis applicable to both types will be made first.

4.21 D/A Converter Static Error

The static equation describing the ideal converter and summing amplifier is:

$$V_e = [\sum_{i=1}^{n} a_i \, (e_{on})_i + \overline{a}_i \, (e_{off})_i] - V_b \qquad (5)$$

where:

V_e = D/A (summing amplifier) output voltage.

a_i = Binary weight, 1 or 0, for the i'th bit. 1 indicates the bit is "on", 0 indicates "off".

$\overline{a}_i$ = Complement of $a_i (\overline{0}=1, \overline{1}=0)$.

$(e_{on})_i$ = Voltage contribution of i'th converter bit $(a_i=1)$ to V_e. ($(e_{on})_i$ are weighted by a factor of 2^i).

$(e_{off})_i$ = Voltage contribution of i'th converter bit $(a_i=0)$ to V_e.

V_b = D.C. bias component of V_e.

n = Number of converter bits.

Ideally, V_e is accurately determined once the digital input (the set of a_i) is specified. In actuality, errors in circuit adjustment and random voltage variation will cause V_e to differ from the ideal. Therefore, an analysis will now be made in order to predict the maximum variation of V_e from desired values.

In the static error analysis, errors introduced by reference and logic supply voltages are assumed negligible. Bit resistance changes with temperature are also neglected because ambient temperature changes are small and all bit resistors are oversized to prevent self-heating. The three main error sources considered, which cause $(e_{on})_i$, $(e_{off})_i$, and V_b to vary, are:

1) Bit resistor adjusting tolerance.

2) "Off" transistor switch leakage current variation with temperature.

3) "On" transistor switch saturation voltage variation with temperature.

These three error sources will first be examined and then the maximum error in D/A output will be found.

4.22 Bit Adjusting Errors

Bit adjusting errors are dependent upon the resolution of the bit adjusting potentiometers. Finite potentiometer wire width limits the exactness to which any bit resistance can be set. The error incurred for one bit, expressed as an error component in the summing amplifier output is:

$$(\Delta V_{e_i})_{adj} = \psi \ [\ (e_{on})_i - (e_{off})_i \ ] \qquad (6)$$

where ψ is the ratio of the smallest resistance change which may be made in a bit adjusting pot to the total bit resistance.

4.23 Transistor Switch Leakage Current

Figure 26 shows a typical D/A converter bit, total bit resistance R_i, plus the summing amplifier. Transistor Q_i should ideally behave as an open switch (collector-to-emitter) when this bit is to contribute to summing amplifier output V_e. This is not possible in practice due to the collector leakage current. The base-emitter junction of Q_i is given a slight reverse bias, thereby limiting collector current to slightly less than I_{CBO} (collector leakage current with emitter open and collector-emitter junction reverse biased).[11]
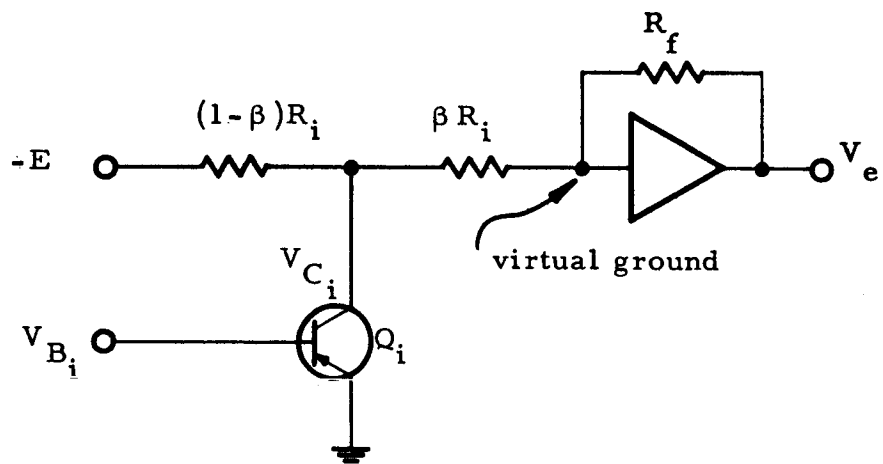
FIG. 26 - TYPICAL D/A CONVERTER
BIT

As a worst case, it is assumed that a collector current equal to I_{CBO} will flow when Q_i is cut off. Then a current summation can be made at the collector, giving:

$$\frac{E - V_{c_i}}{(1 - \beta) R_i} = I_{CBO} + \frac{V_{c_i}}{\beta R_i} \qquad (7)$$

(All currents and voltages will be taken as absolute magnitudes).
Solving for collector voltage V_{c_i}, we obtain:

$$V_{c_i} = \beta [E - R_i I_{CBO} (1 - \beta)] \qquad (8)$$

which is a negative voltage. The voltage produced at the summing amplifier output due to this i'th bit, $(e_{on})_i$, is:

$$(e_{on})_i = \frac{R_f V_{c_i}}{\beta R_i} = \frac{R_f E}{\beta R_i} - R_f I_{CBO}(1 - \beta) \qquad (9)$$

(Note that $(e_{on})_i$ does not refer to the case when transistor Q_i is "on", but rather to Q_i being "off" and the bit being "on").

The term $R_f I_{CBO} (1 - \beta)$ in Equation (9) represents a d. c. bias component of V_e. This fact causes no error in V_e since it is automatically taken into account when the D/A is adjusted. Error can occur, however, due to the temperature-sensitivity of

I_{CBO}, for I_{CBO} increases with temperature. An increase in I_{CBO} drives V_e more positive. The change in $(e_{on})_i$ due to changes in I_{CBO} can be found as:

$$(\Delta V_{e_i})_{leak.} = \frac{\partial \, (e_{on})_i}{\partial \, I_{CBO}} \, \Delta I_{CBO} \tag{10}$$

$$= R_f (1 - \beta) \, \Delta I_{CBO} \tag{11}$$

Equation (11) indicates that an "off" transistor leakage current change produces a change in output voltage that is the same for each bit. Thus for an n bit converter, the maximum total output change due to leakage is:

$$[\, (\Delta V_{ei})_{leak.} \,]_{max.} = nR_f(1-\beta)\Delta I_{CBO} \tag{12}$$

where, m = number of "on" bits $(\le n)$ and all β's are assumed equal.

4.24 Transistor Switch Saturation Voltage

The "on" transistor switch varies from the ideal closed switch model in that an appreciable collector-to-emitter voltage exists for an "on" (saturated) transistor. This saturation voltage is temperature sensitive and thus may vary and cause converter errors. The equation describing the i'th "on" transistor switch

is:

$$\left(e_{off}\right)_i = V_{c_i} \frac{R_f}{\beta R_i} \tag{13}$$

V_{c_i} is now the transistor collector-to-emitter saturation voltage $(V_{c_e} \text{(sat.)})$. A change in V_{c_i} will produce a change in $\left(e_{off}\right)_i$ of:

$$\left(\Delta V_{e_i}\right)_{sat.} = \Delta V_{c_i} \frac{R_f}{\beta R_i} \tag{14}$$

Because collector-to-emitter saturation voltage increases negatively (for PNP transistors) as temperature increases, $\left(e_{off}\right)_i$ will correspondingly go more positive. Note that the error voltage introduced by a bit is inversely proportional to the bit resistance. Assuming the change in saturation voltage, ΔV_{c_i}, is the same for each bit, the most significant bit will cause the largest error voltage to appear at the summing amplifier output.

4.3   A/D Converter Error Analysis

The first thing to be noted about A/D accuracy is that statically, its accuracy is dependent directly on the accuracy of its D/A converter. The A/D's D/A is essentially the same as the other D/A, except that the summing amplifier gain is much higher. However, statically, the A/D's accuracy depends upon two other

factors; the trigger level settings and the summing amplifier gain. The effect of these parameters and how they influence A/D hysteresis is discussed next.

4.31 A/D Static Accuracy

Figure 27 is a time plot of the A/D summing amplifier output (the A/D "error" signal) for a very slowly changing analog input. With the aid of this diagram, an attempt will be made to show the effects of errors in trigger level and summing amplifier gain settings on static and dynamic performance. The main assumptions made are that A/D clock frequency (cps) is much higher than the slope (quanta/sec.) of the analog input voltage and that the D/A is ideal (no error).

Summing amplifer output is shown in Figure 27 for five typical cases of A/D mis-adjustment. For the actual converter, desired comparator levels $(\pm V_T)$ are ± 20v. Quanta lines occur at integer voltages, hence Q is an integer. The five cases can be explained as follows:

> Case I is the way the summing amplifier output should appear for perfect comparator $(\pm V_T)$ and amplifier gain (R_f) adjustment.

> Case II shows both triggers adjusted to trigger high by δ
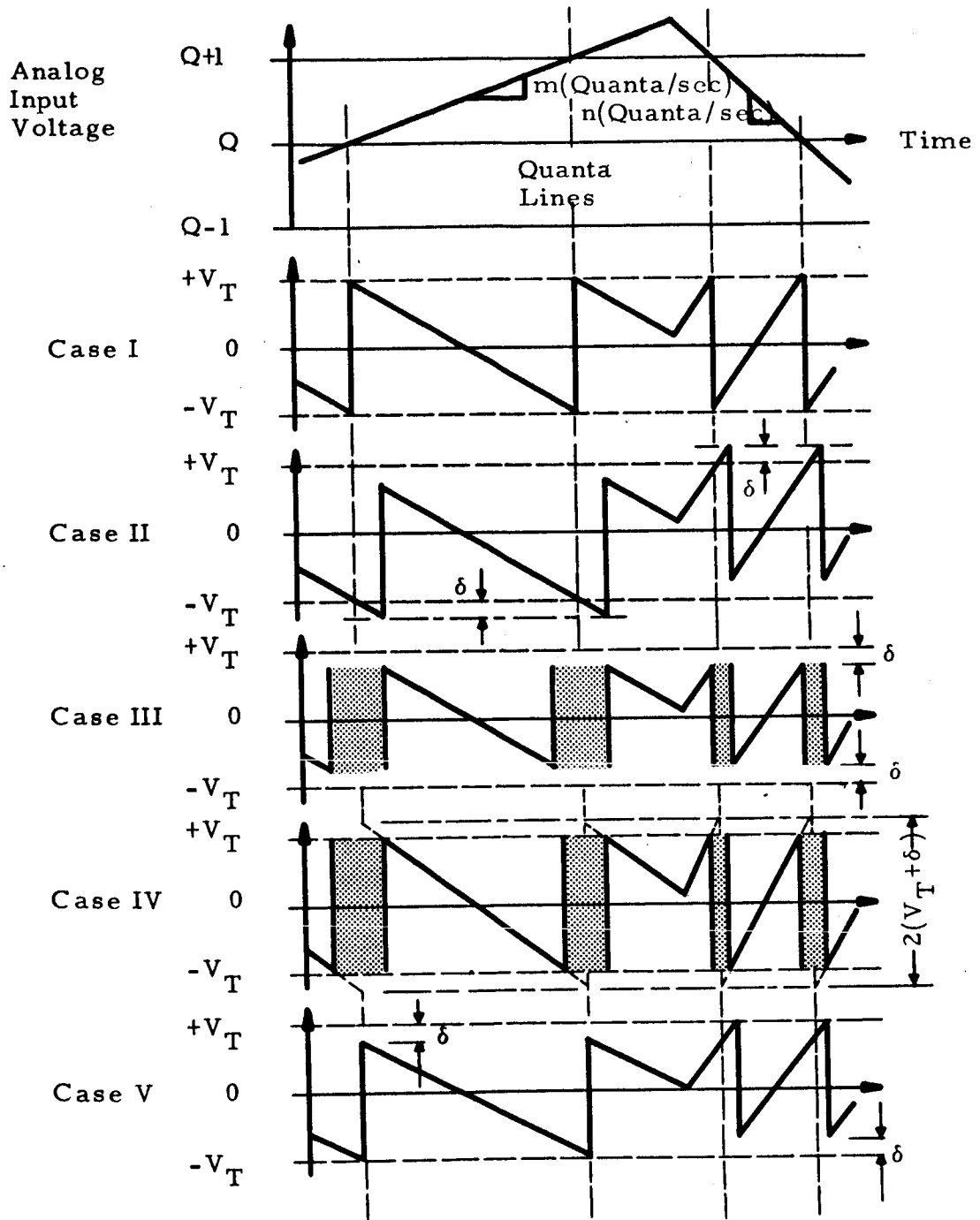
FIG. 27 - A/D SUMMING AMPLIFIER OUTPUTS

volts (absolute magnitudes).

Case III shows both comparator levels adjusted low by δ volts.

Case IV shows amplifier gain (R_f) adjusted high so that the voltage increment fed back due to a one count change in the A/D counter is $2(V_T + \delta)$.

Case V shows amplifier gain adjusted low so that a one count change feeds back $2V_T + \delta$ volts.

Although the above cases are typical examples of A/D misalignment, actual converter error will be caused by a combination of the cases shown. The first step will be to explain what happens in each case, and then the resultant errors will be analyzed.

Assuming exact D/A adjustment, most significant bit resistance R, and least significant bit resistance 128R, the amplifier feedback resistance for the eight bit converter (R_f) must be such that:

$$\frac{E\,R_f}{128R} = 2\,V_T \tag{15}$$

or

$$R_f = \frac{256\,V_T\,R}{E} \tag{16}$$

Also, for correct input scaling, the analog input resistor, R_a, must be sized so that:

$$\frac{E R_f}{128R} = Q \frac{R_f}{R_a} \qquad (17)$$

or

$$R_a = 128 Q \frac{R}{E} \qquad (18)$$

where Q is the quanta size (in volts). If R_a and R_f are adjusted exactly according to Equations (16) and (18) and + and - trigger levels ($\pm V_T$) are equal, the amplifier output will be as shown in Case I. Each positive going discontinuity corresponds to a "+" pulse being emitted on the incremental output and a negative going discontinuity indicates occurrence of a "-" output pulse.

If all adjustments are correct except for comparator level adjustments, summing amplifier outputs are as shown in Cases II and III. Case II shows a converter with hysteresis. The amount of hysteresis is given by:

$$\text{Hysteresis} = \frac{\delta}{V_T} \qquad (19)$$

Case III is characterized by oscillation bands (shaded areas) about the quanta lines. In Case III, comparator levels are set too low. Case IV is essentially the same, except that now R_f (amplifier gain) is too large. In either case, such oscillations are

undesirable, both because they put undue frequency demands on the digital system portions which must accept the A/D output and because accuracy at a quanta line is decreased.

Case V is the proper amplifier output for an actual converter. Since it is impossible to obtain Case I in practice, R_f (amplifier gain) is purposely decreased, causing hysteresis to be added to the converter equal to:

$$\text{Hysteresis} = \frac{\delta}{2 V_T} \quad \text{(Quanta)} \tag{20}$$

The relationship between V_T, R, R_f, E and δ to insure a small amount ($\delta / 2 V_T$) of hysteresis is, for the designed eight bit converter:

$$\frac{E R_f}{128 R} = 2 V_T - \delta \tag{21}$$

which is a minor modification of Equation (15). Solving for R_f, the amplifier feedback resistance:

$$R_f = \frac{128R}{E} (2 V_T - \delta) \tag{22}$$

Presence of hysteresis serves to prevent oscillation near quanta lines when the analog input contains an appreciable noise component. Hysteresis can be considered as an additional

static error component and is the major cause of quantization un-

certainty.

If trigger levels are not set a V_T as desired, the over-

all effect is that of a bias (zero) level shift, which is easily cor-

rected. Assume the negative level is set at $-V_T$, but that the pos-

itive level is set at $V_T -$. This misalignment can be compensated

for by adjusting R_a, the analog input (scaling) resistance and chang-

ing the bias adjustment. After the trigger levels have been ad-

justed, the procedure is to ground the A/D input and adjust the bi-

as pot until the converter is on the verge of reading -1 quanta in-

stead of zero. Then increase the A/D input to full scale (100v.)

and adjust R_a so that just as the input passes 100v., the A/D read-

ing changes to 100. Thus, the trigger level "misadjustment" has

been eliminated. In fact, it is really not imperative that the levels

be $\pm V_T$, but only that their difference be about $2 V_T$. Then R_a and

bias adjustments can compensate for any remaining errors.

In conclusion, A/D static error is primarily dependent

upon D/A accuracy. In addition, some hysteresis must be present

to stabilize operation when converting noisy inputs. Next, high-

speed operation will be examined and bounds on conversion speed

obtained.

4.32 High Speed Operation

Due to the synchronous nature of A/D operation, a change in digital output occurs at a clock time, not at the exact instant the analog input passes a quanta line. The maximum delay which might be incurred in waiting for a clock pulse is termed the aperature time. Another factor influencing high speed performance is the bandwidth of the summing amplifier. These two effects will now be examined.

Figure 28 shows summing amplifier output and A/D clock output for a rapidly changing (ramp) input. When the analog input passes quanta line $Q + 1$, D seconds are required before the correct up count transistion occurs on the A/D clock output and an up count is sent to the A/D counter. Hence the digital output lags the input by D seconds. Supposing D is as large as possible (equal to τ_A, the clock period), the maximum error incurred because of sampling, in terms of quanta is:

$$\epsilon_s = \tau_A m \quad \text{(Quanta)} \tag{23}$$

where m is the maximum allowable input slope. Obviously, ϵ_s can be reduced by either speeding up the A/D clock or by reducing
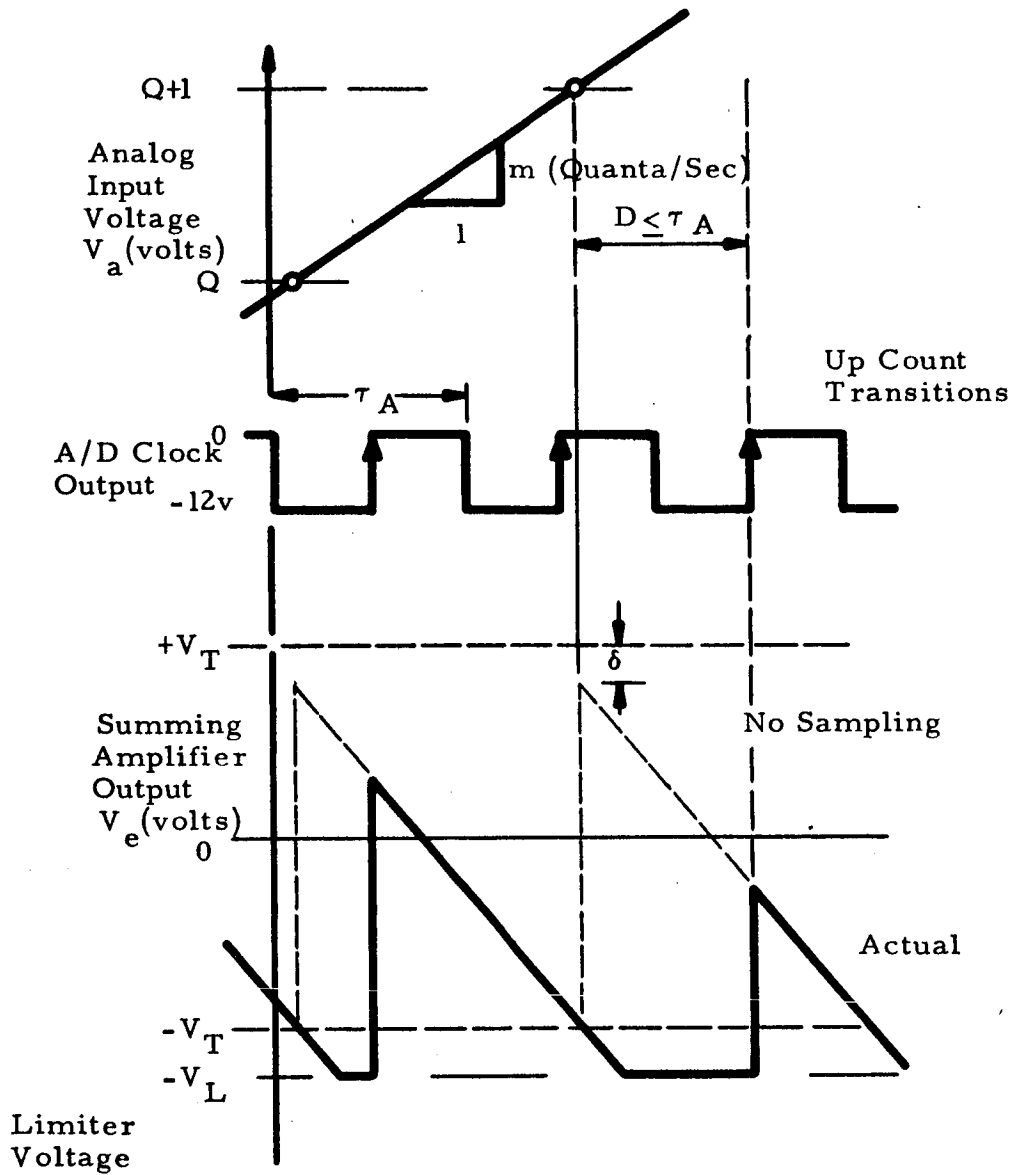
FIG. 28 - A/D AMPLIFIER OUTPUT FOR
RAPIDLY CHANGING INPUT

the maximum allowable input slope.

ϵ_s can also be related to a sinusoidal input. Let the input be:

$$V_a = A \sin 2\pi f t \qquad (24)$$

where: $A = $ Half-amplitude (Quanta)
$f = $ cps

Then, $\dfrac{dV_a}{dt} = $ Input slope $= 2\pi f A \cos 2\pi f t$ (25)

Maximum slope occurs at $2\pi f t = \pm n\pi$ and is equal to $2\pi fA$ (quanta/sec.). Substituting this slope into Equation (24), ϵ_s can be expressed as:

$$\epsilon_s = 2\pi fA\tau_A \quad \text{(Quanta)} \qquad (26)$$

In designing the A/D, clock frequency is made as high as possible. Clock frequency is limited by counter construction and the type of logic used. For the designed A/D, this frequency bound can be found as follows. Refer to Figure 22, the A/D counter schematic. Figure 29 is the A/D timing diagram for a rapidly changing positive going analog input. Assume the bidirectional counter is going through its "worst" positive transition, i.e., 01111111 to 10000000, the one with the most carries. Six time delays
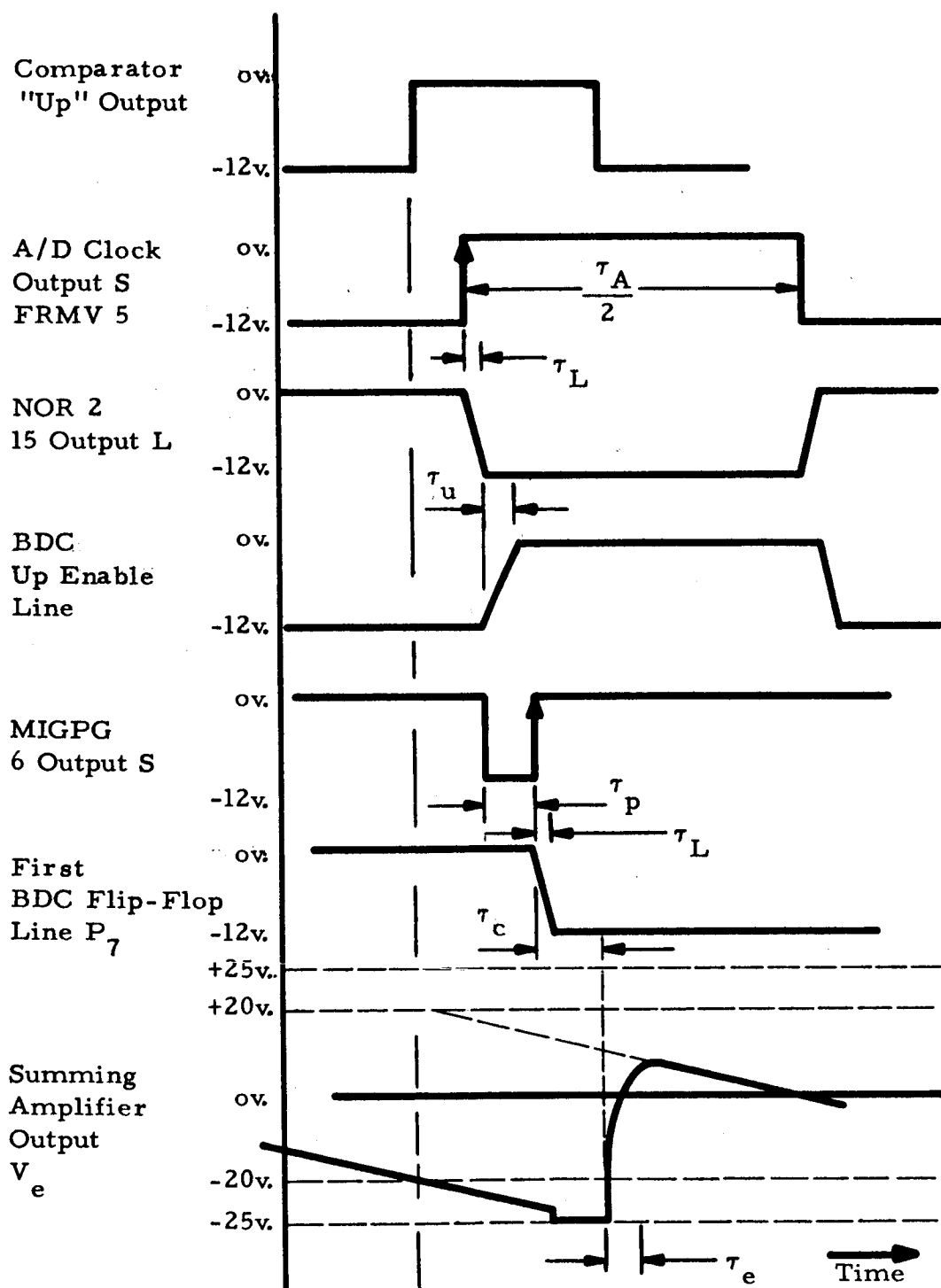
FIG. 29 - A/D TIMING DIAGRAM

encountered are shown in Figure 29. They are

$$\tau_A \quad = \quad \text{A/D clock period}$$

$$\tau_L \quad = \quad \text{Typical logic element transition delay time}$$

$$\tau_p \quad = \quad \text{MIGPG pulse width}$$

$$\tau_u \quad = \quad \text{Delay in settling carry enable lines}$$

$$\tau_c \quad = \quad \text{Bidirectional counter carry propagation time}$$

$$\tau_e \quad = \quad \text{Summing amplifier rise time plus D/A converter settling time.}$$

For the configuration of Figure 22, all but τ_A and τ_p are fixed. τ_p is made greater than τ_u to allow the up enable line to be fixed at ground and the down enable line to be disabled. Once these conditions are established, the MIGPG output goes back to ground and triggers the first counter flip-flop. Let $\tau_{e\,(\text{max.})}$ be the maximum counter carry propagation time. The criteria for choosing τ_A is then:

$$\tau_p \;+\; \tau_{c(\text{max.})} \;+\; \tau_L \;<\; \tau_A/2 \tag{27}$$

If Equation (27) is not satisfied, counter carries won't have time to fully propagate on worst counter transitions, and loss of count can occur when an up pulse is followed $\tau_A/2$ seconds later by a

down pulse.

The counter delay, τ_L, can be measurably reduced by using a synchronous counter. This was not done in the designed A/D because it was felt the additional speed gained in using a synchronous counter wasn't worth the increased complexity and cost. τ_u could be decreased by driving up and down enable lines with one-shots. Both enable lines would be normally disabled, and τ_u would then be the time required to enable one line, not to simultaneously enable and disable both lines.

An additional factor that helps increase operating speed is the action of the $\pm$ 25v. limiters (see Figure 28 and Figure 29). Because the counter is asynchronous, false intermediate states occur during transitions. When going from 01111111 to 10000000 for example, the counter actually takes on the state 00000000 as the carry propagates down the counter before the last flip-flop finally triggers and the counter settles at 10000000. The D/A senses these intermediate states, however, and initially V_e goes the "wrong way" or as shown in Figure 29, more negative. If it weren't for the limiters, the summing amplifier, due to its high gain, would temporarily saturate. Saturation would cause spikes and oscillation in the

amplifier, output as it recovered from this temporary overload con-
dition, thereby effectively increasing τ_e and reducing speed.

4.4 D/A Converter Performance Data

All measurements in analog-digital problem simula-
tions will normally be in terms of quanta. For this reason, all er-
rors, whether for D/A or A/D are expressed as percent of one
quanta. Percentage errors are then larger for small quanta size,
so that choice of quanta size for a particular problem simulation
is quite important.

For the D/A, smallest quanta size is 1 volt. It is now
possible to predict for the designed converter the maximum static
error caused by adjustment inaccuracies and variation of leakage
current and saturation voltage with varying ambient temperature.
On the basis of the following data, conclusions can be made as to
the relative magnitudes of the error introduced by each of these
factors.

1) Transistors: 2N1309

2) Ambient temperature variation: 68°F. to 72°F.
   Transistor data sheet gives; for $\Delta T = 4^\circ$F

   a) $\Delta I_{CBO} = 0.2 \mu a$

b) $\Delta V_{c_e(Sat.)} = 0.6$ mv.

3)   Assume β is 0.1 for each bit.

4)   Potentiometer resolution was found to be one part per thousand for normal manual adjustment; since β is 0.1 (pot resistance is 10 percent of total bit resistance), overall bit adjusting resolution (ψ) is 0.01 percent.

5)   Nominal resistance values are: $R_f = 48K$; bit resistances are 75K, 150K, 300K, 600K, 1.2M, 2.4M, 4.8M, and 9.6M. Reference voltage (E) is -200 volts.

Errors caused by leakage current variation are greatest when the greatest number of ones appear on the D/A input. This occurs at 01111111 (-1 quanta). Error caused by each bit is

$$R_f (1 - \beta) \Delta I_{CBO} = 48K (1 - 0.1) (0.2 \times 10^{-6}) = 0.009 \text{ volts.}$$

At 01111111, the error is $7 \times 0.009 = .063$ v., or 6.3 percent of one least quanta.

Bit adjusting error is maximum at maximum output ($\pm$ 100v.). It is a straight 0.01 percent, 0.01v., or 1 percent of one quanta. This assumes, however, that all bit errors are cumulative. In the normal adjusting procedure, bits are adjusted so that some errors cancel each other. Thus it is safe to assume that the worst error is less than 1 percent.

Saturation voltage variations can account for an error

of: $\Delta V_{c_e(Sat.)} \dfrac{R_f}{BR_i} = \dfrac{(.0006v.)}{(0.1)} \dfrac{(48K)}{R_i}$ for one bit.

This error is a maximum for 01111111 also, where R_i is 75K and error is $\dfrac{(0.6mv.)(48K)}{(0.1)(75K)}$ = .004 volts or 0.4 percent of one quanta. This is small and can be neglected compared to leakage current errors.

Normally, for most problem simulations, no more than five D/A bits will be used (8 volts/quanta). The 6.3 percent error then becomes 0.8 percent which insures good accuracy in the simulation results.

Figures 30 and 31 are plots of actual D/A output for inputs from -100 to +100. The tests were made by connecting the D/A input with the A/D output and driving the A/D with a slow ramp voltage, going from -100v. to +100v. The D/A output vs. the A/D input was then plotted on an X-Y plotter, enabling each D/A output level to be recorded. The maximum quanta size error (change from the desired monotonicity) can be seen to be 0.6v. (.6 quanta) and occurs in changing from +47 to +48 input. Maximum static error was 0.6v. and occurred for +48, +64, and +80 inputs.

The fact that actual D/A error is much greater than predicted error indicates that the main cause of error is poor bit ad-
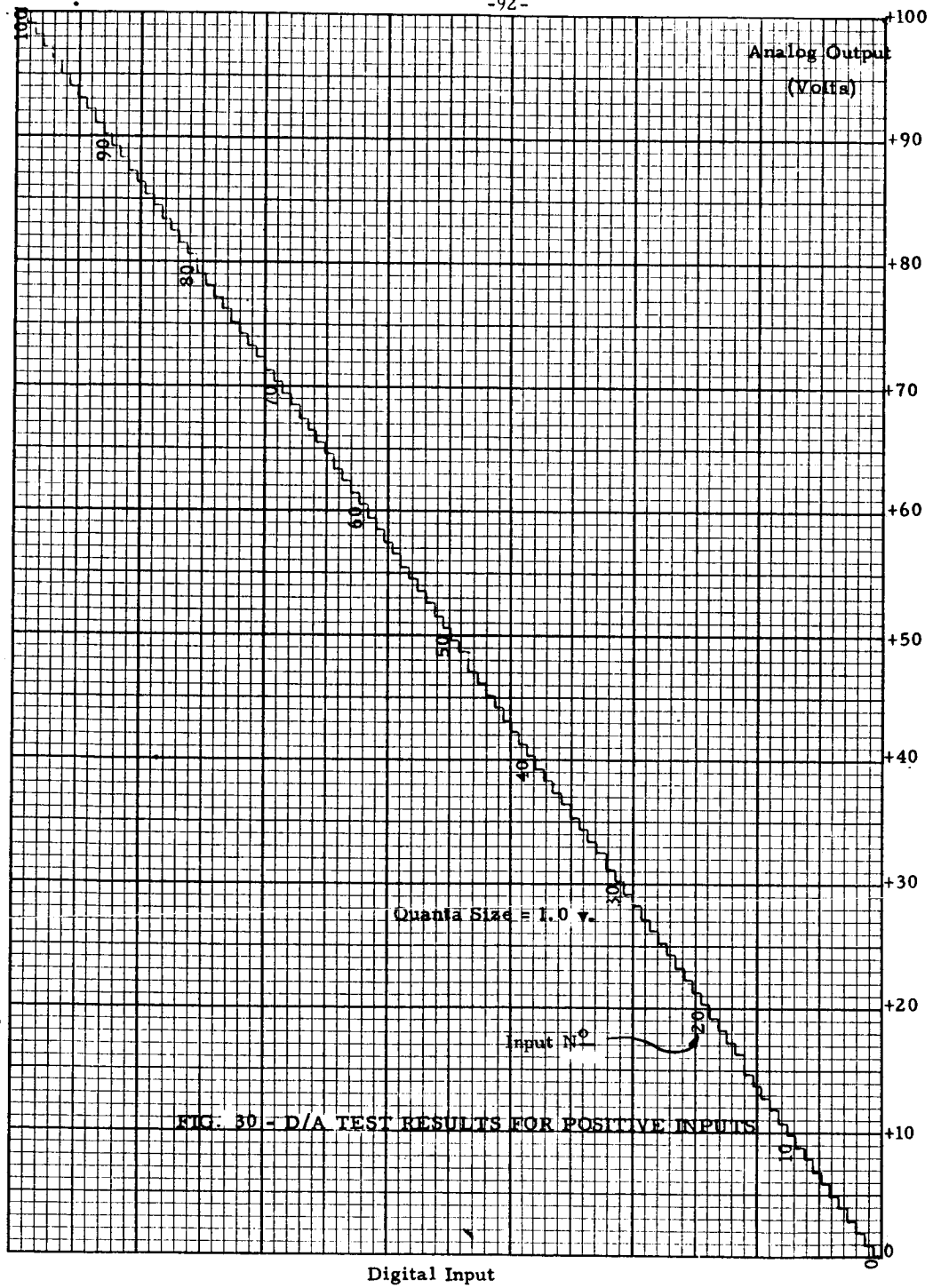
FIG. 30 - D/A TEST RESULTS FOR POSITIVE INPUTS

Digital Input

FIG. 31 - D/A TEST RESULTS FOR NEGATIVE INPUTS

Digital Input
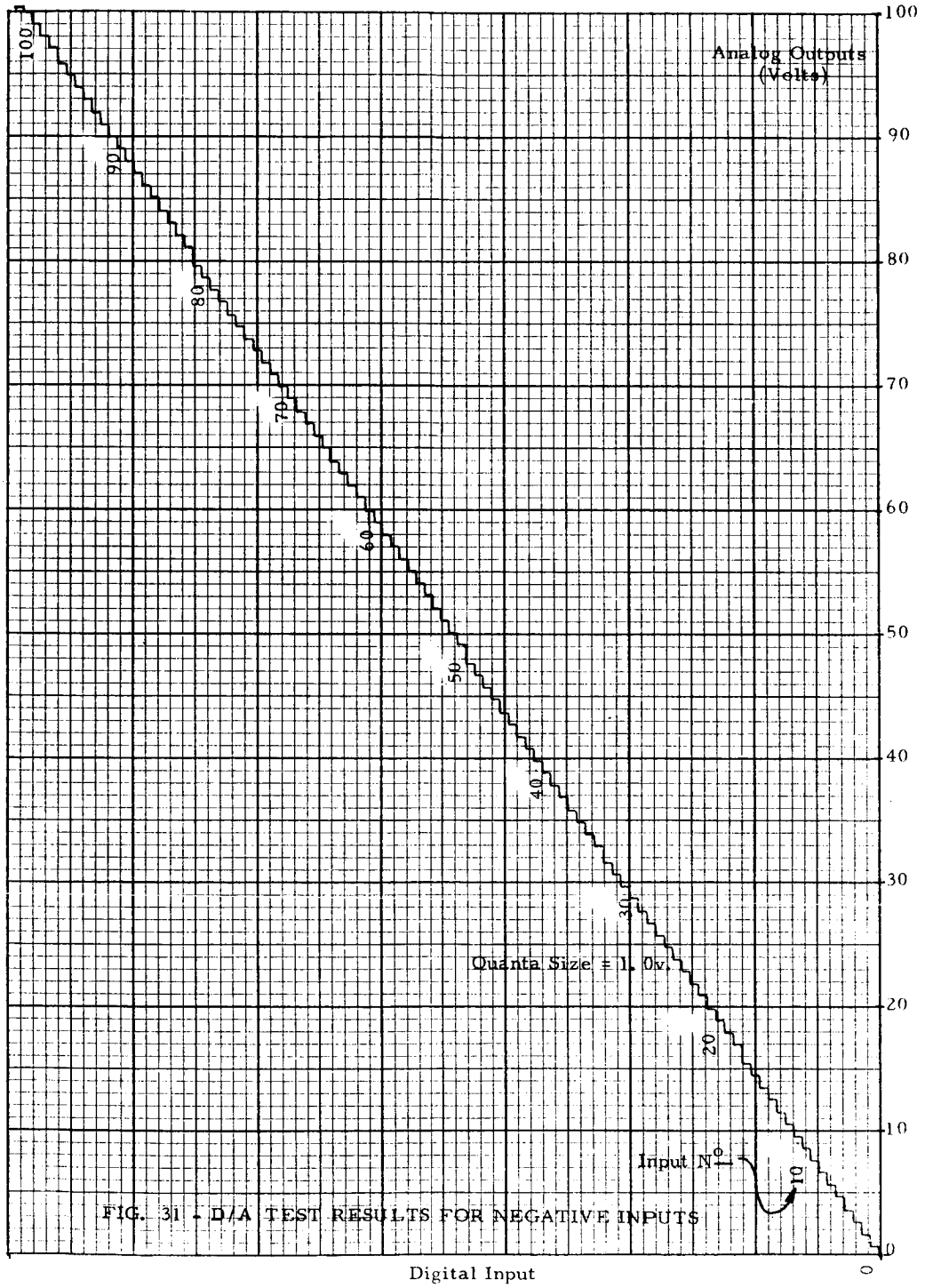
justment. Bit adjusting accuracy was not within theoretical toler-
ances because voltage measurements could only be made to the near-
est tenth of a volt, (or one part per thousand) using the GEDA cali-
brating potentiometer. By use of a 0.01 percent digital voltmeter in
D/A calibration, the bit resistances could be adjusted to within the
theoretical tolerance; however, the accuracy obtained by using the
GEDA potentiometer is sufficient for all immediate applications.

D/A drift was found to be about 0.1 volt per month. This
is possibly due to GEDA reference voltage changes, and in normal
usage both GEDA reference voltages and D/A bias level should be re-
set once a month. D/A rise time is about 50 μ sec., a factor which
should be insignificant since simulated process time constants will
be 10 to 1000 times larger.

4.5   A/D Converter Performance Data

A/D static error should be of the same magnitude as
that of the D/A, except for the contributions due to hysteresis and
noise. Figures 32 and 33 are results of tests identical to those pre-
sented in Figures 30 and 31 except that now along the abscissa are the
analog voltage increments at which the A/D should ideally switch.
The vertical presentation is due to the A/D output being converted

FIG. 32.- A/D CALIBRATION CHECK FOR POSITIVE INPUTS

FIG. 33 - A/D CALIBRATION CHECK FOR NEGATIVE INPUTS
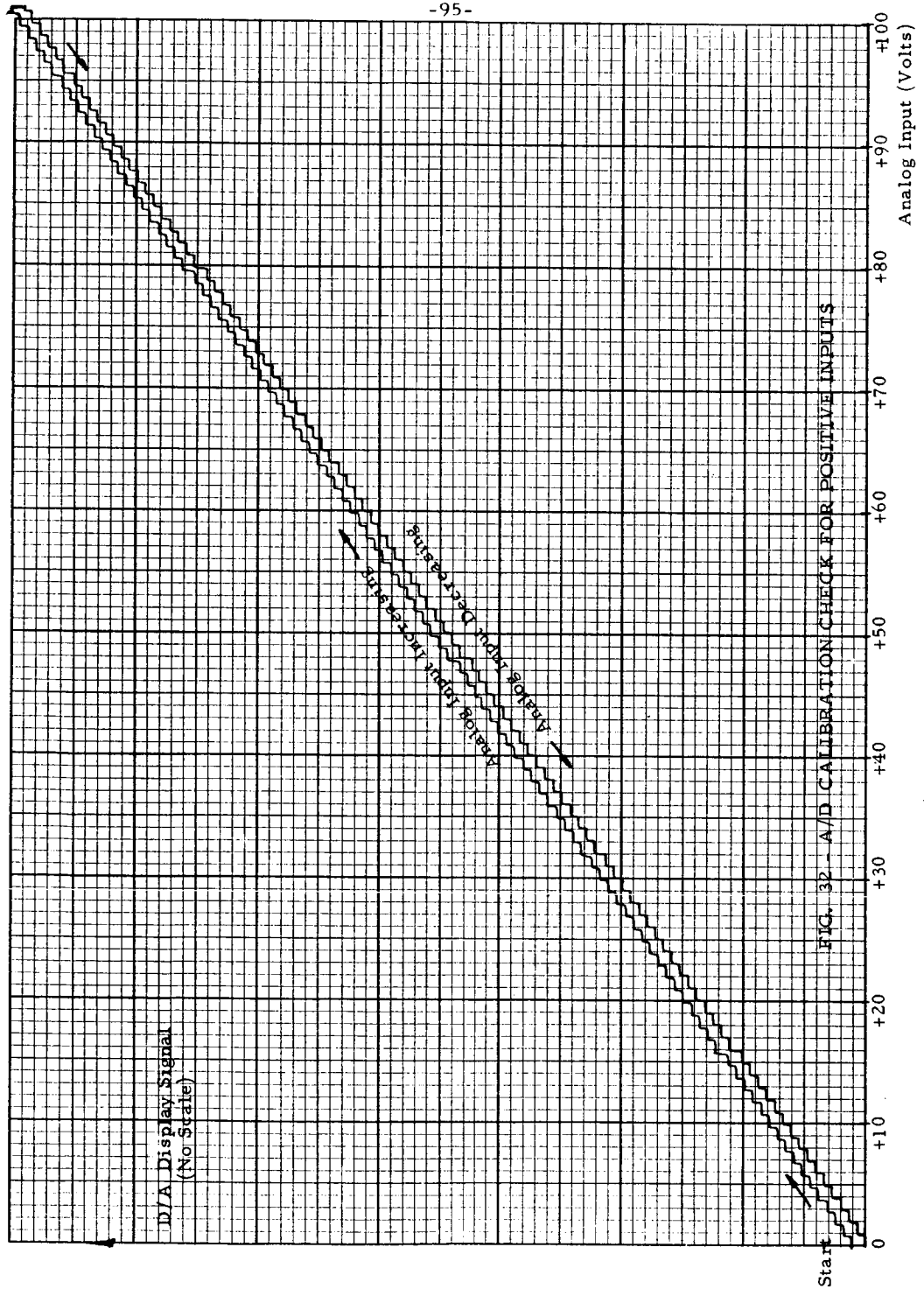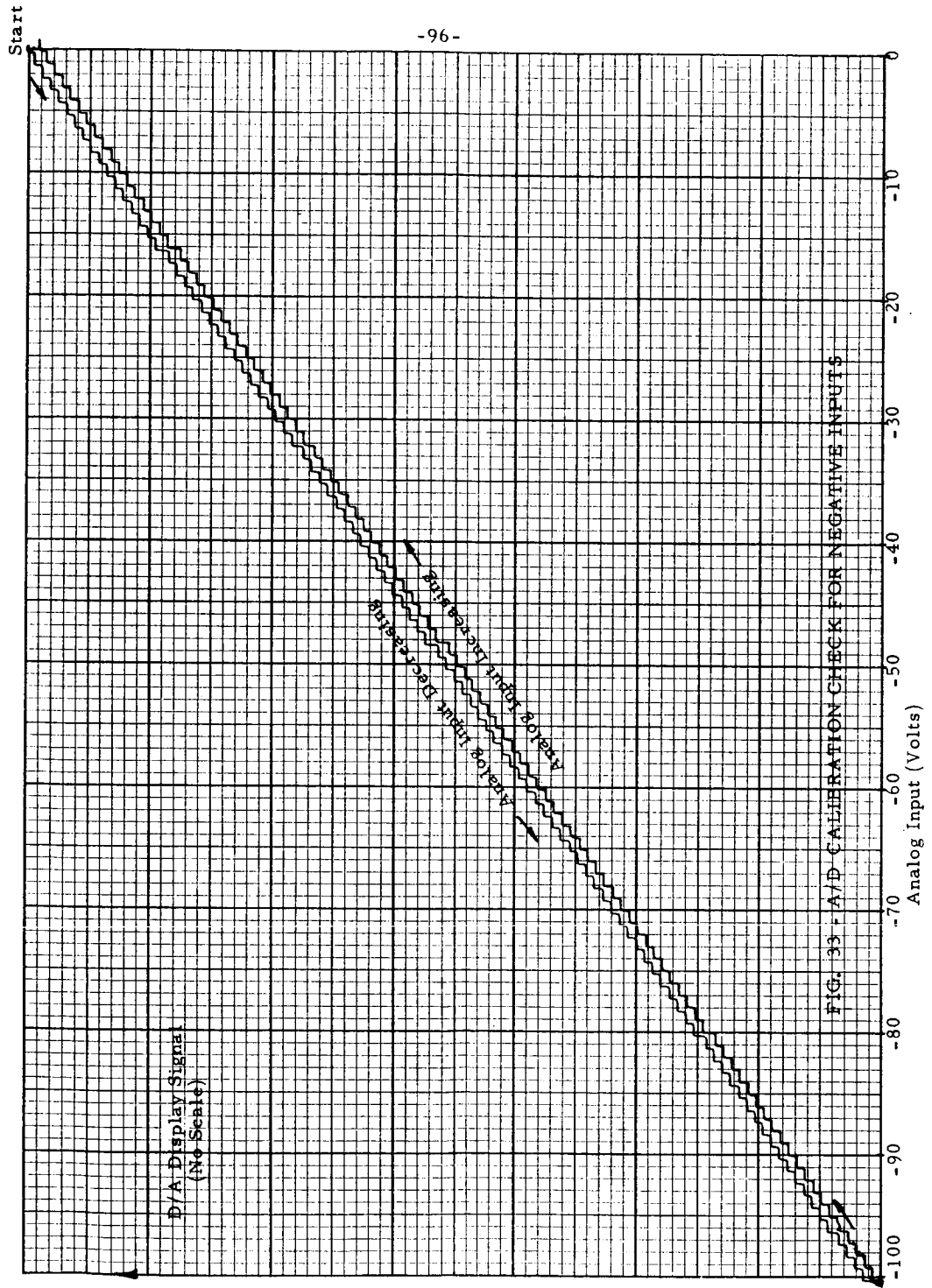
back to analog form by the D/A. This is done to make it easier to see the A/D switching points. The ramp voltage was run up to +100 volts, the plotter manually shifted down slightly, and then the ramp decreased back to zero. A similar procedure was followed for negative inputs. In this way, hysteresis can be detected as the difference in switch point locations for negative and positive going inputs.

Maximum static error for a positively increasing input as seen in Figures 32 and 33 is 0.5 quanta. (Note that a switch should occur at the specified analog input voltage when the input is positively going). Hysteresis can be seen to be about 0.2 volt (quanta), which is enough to prevent noise spikes in the GEDA voltages (A/D input) from causing continuous oscillation near switch points. Figure 34 shows the results of a monotonicity check, in which a carefully calibrated slow speed ramp (1 v./sec.) was applied at the A/D input and the A/D summing amplifier output recorded on a strip chart. Figure 34 indicates that quanta line spacing varied at most by 0.1 volt from the desired value of 1.0 volt. Again, using a more accurate calibrating voltmeter, the above errors could possibly be reduced, but the present performance is adequate for the desired simulations intended.
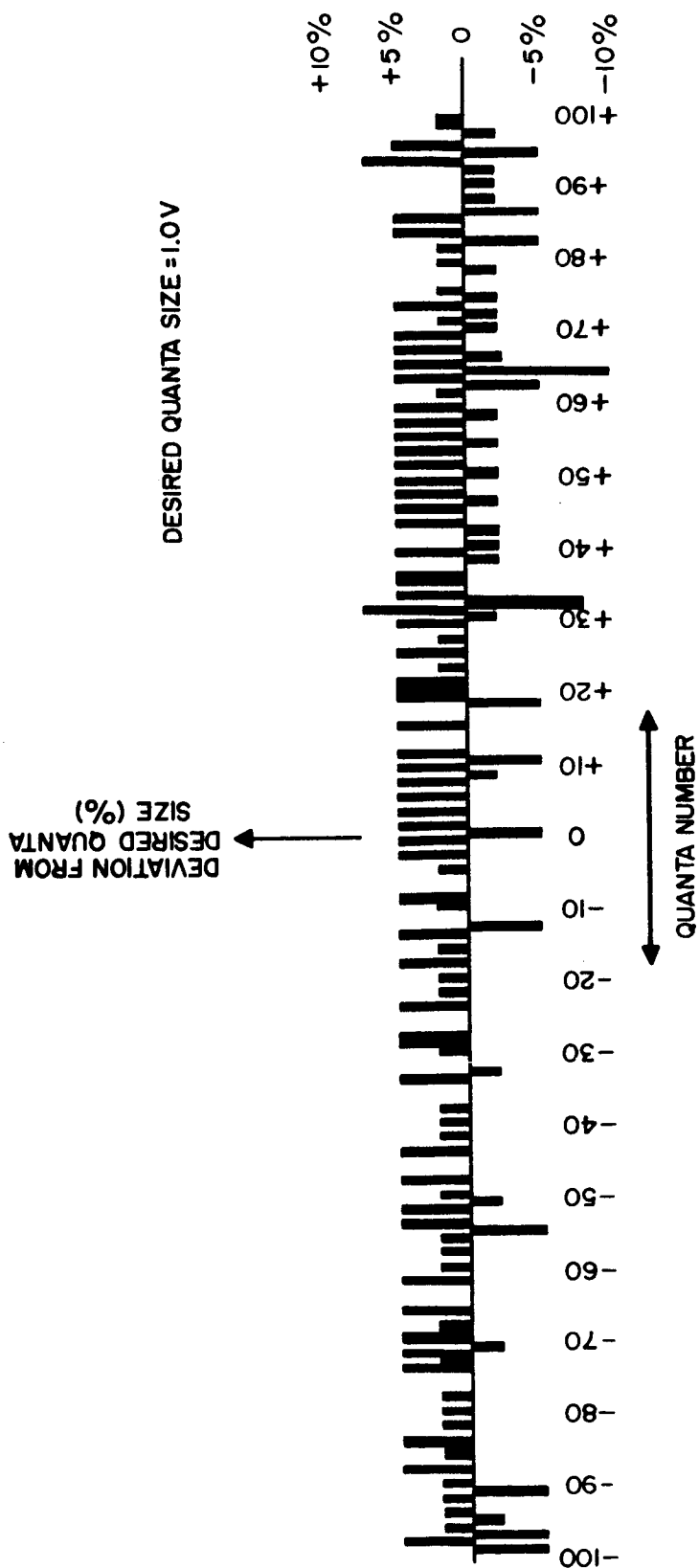
FIGURE 34   A/D MONOTONICITY DATA

the sampling error is:

$$\epsilon_s = 2\pi \, f \, A \, \tau_A$$

$$= 2\pi \, f \, A \, (100 \, \mu s)$$

$$= (628 \times 10^{-6}) \, A \, f \, (\text{Quanta}) \qquad (28)$$

Figure 35 is a plot of ϵ_s vs. A/D input frequency for various input amplitudes. Assuming that dynamic error is desired to be less than 0.05 quanta, problem frequencies must be less than about 0.8 cps if A is allowed to be 100 quanta. For most uses, it is convenient to limit problem natural frequencies to less than 1 cps since at higher frequencies (10 cps and above) care must be taken in problem board patching and inital condition switch manipulation. For $f \leq 1$ cps, dynamic error, at most (A = 100), would be 0.06 quanta. Often, larger quanta size would be selected so that this error (in percent of one quanta) would be even less. For 8 volts/quanta, the maximum error would be $\frac{.06}{8} \approx 0.8$ percent of one (8 volt) quanta. In conclusion, since the GEDA can operate at very low frequency, a time scale can always be selected with the aid of Figure 35 so that dynamic error is made sufficiently small.

4.6 Summary

The error data shown in Figures 30-34 can be summa-

A bound on maximum allowable analog input slope for any desired accuracy can be obtained theoretically. Knowing the dynamic error will then permit selection of appropriate analog computer time scale so as to make such errors negligible.

In designing the A/D counter, the various delay times were taken into account as follows (see Figure 29). τ_u was found to be 5 μ sec. for the designed counter. Thus τ_p was made longer than τ_u and equal to 8 μ sec. $\tau_{c(max.)}$ was found to be 3 μ sec. per stage, or 24 μ sec. total. Thus using Equation(27), $\tau_A > 66 \mu$ sec. However, the PULSE OUT pulses of the A/D may be fed into the four bit ERROR COUNTER (via the anticoincidence circuit). The ERROR COUNTER is able to count bidirectionally with 15 μ sec. minimum pulse spacing. As can be seen in Figure 25, the anticoincidence clock period must be at least twice that, or 30 μ sec. This was increased for safety to 40 μ sec., or a frequency of 25KC. The anticoincidence can then accept pulses at the rate of one every 2 X 40μs = 80 μs or greater, hence the A/D clock period must be longer than 80μs (10 KC for safety). Thus, we see that the A/D sampling frequency is limited by the way in which the A/D is used.

For the designed system (A/D clock frequency 10KC),
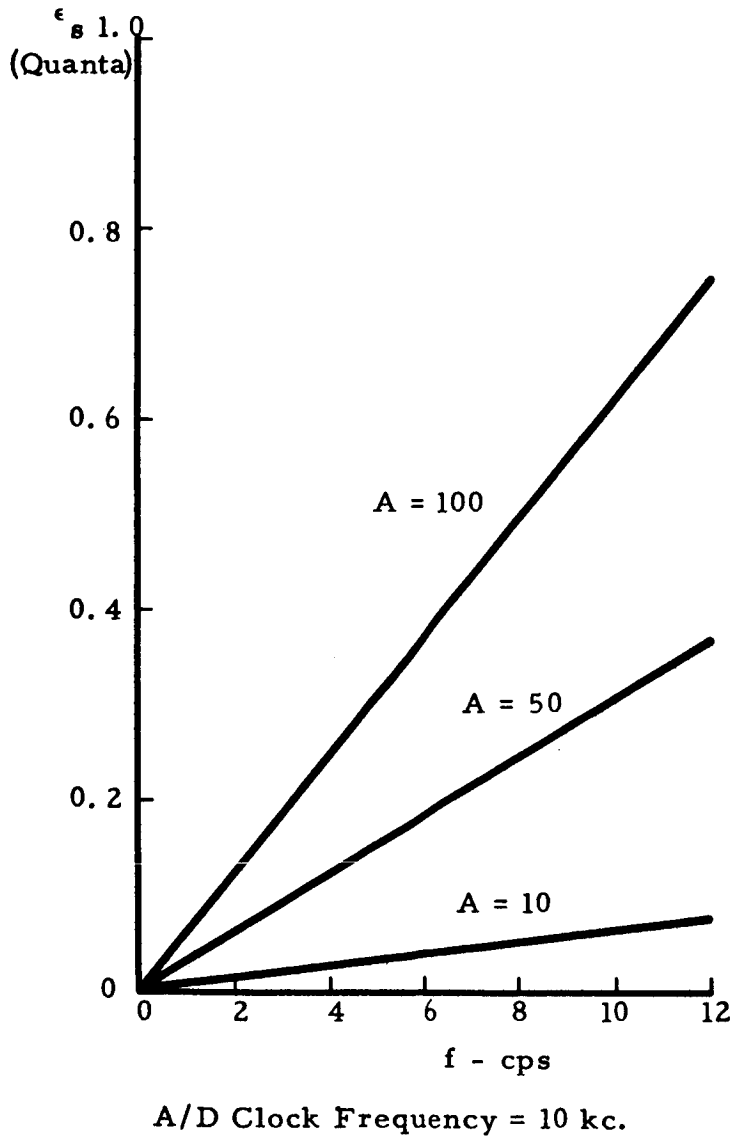
FIG. 35 - A/D DYNAMIC ERROR

rized as follows.

D/A Specifications (Based on 100 quanta = 100v.)

1)	Static Error	:	0.6 volt
2)	Monotonicity	:	0.6 volt
3)	Zero Offset	:	10000000 input produces 0 volt output
4)	Drift	:	0.1 volt/month (approx.)

A/D Specifications

1)	Static Error	:	0.5 volt
2)	Monotonicity	:	0.1 volt
3)	Zero Offset	:	0 volt input produces 10000000 output
4)	Quantization Uncertainty (Hysteresis)	:	0.2 volts
5)	Dynamic Accuracy:		See Figure 35

The above data is for a one volt quanta size and a $\pm$ 100 quanta total range. All errors expressed in terms of percent of one quanta are proportionately less for larger quanta sizes. For example, at 16 volts per quanta, A/D static error is $\frac{.5v}{16v} \times 100\% = 3.2$ percent of one quanta.
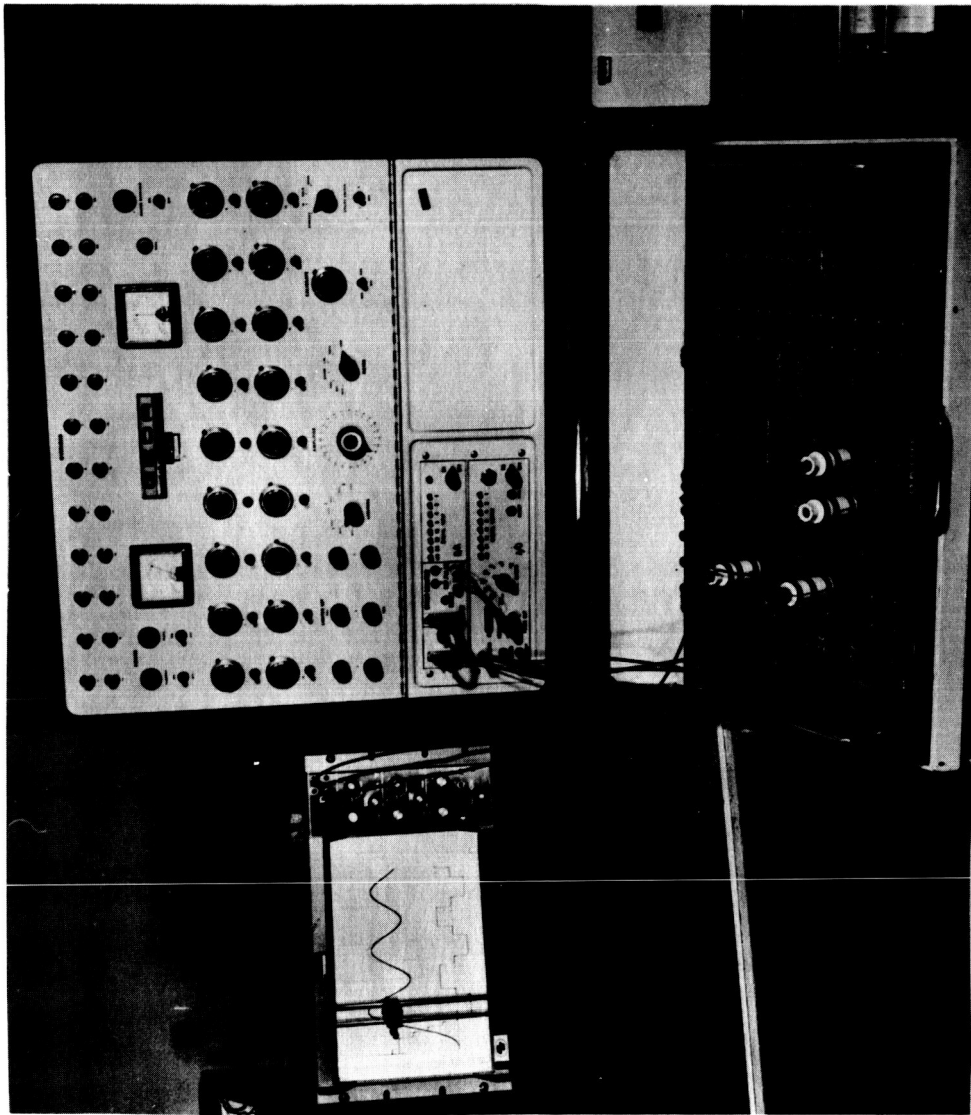
FIG. 36 – ANALOG COMPUTER SIMULATION OF PULSE-DATA SYSTEM USING DESIGNED UNIT

CHAPTER 5

CONTROL SYSTEM SIMULATION

5.1 Introduction

In order to demonstrate the system's flexibility and to show how the designed A/D converter, D/A converter and pulse data logic can be put to use, two typical system simulations will be presented and comments made on the results thereby obtained.

5.2 Pulse Data System

Taft[12] has worked an example problem concerning the stability of a certain class of pulse data systems, which will be presented here to demonstrate the capabilities of the designed analog-digital simulation facility.

Consider a system as shown in Fig. 2, where the process is linear with the transfer function:

$$G(s') = \frac{Kv}{s'(T^2 s'^2 + 2\zeta T s' + 1)} \qquad (29)$$

Time can be normalized by letting $T\tau = t$, or $s' = \frac{1}{T}s$, yielding:

$$G(s) = \frac{KvT}{s(s^2 + 2\zeta s + 1)} \qquad (30)$$

The GEDA analog computer circuit for the pulse data system of Fig. 2 with $G(s)$ as given by Equation (30) is shown in Fig.

37, including the A/D and D/A converter connections. Quanta size was selected as 16 volts, and the problem was run in real time.

Taft's problem was to determine the critical gain KvT at which the system, starting at rest at a quanta line, will go into a limit cycle if given a single pulse input. Fig. 38 shows that this critical value lies between 0.5 and 0.6 for a system where ζ = 0.3, confirming Taft's results. Fig. 39, the critical KvT has been more closely determined, and the system is seen to be stable for single pulse inputs if KvT < 0.571. Fig. 40 is a phase-space projection on the θ -$\dot\theta$ plane of the same system showing both limit cycle and non-limit cycle response. In each case, θ was zero initially, the error counter was at 1000, and the auxiliary switch open. A single pulse was put into the counter, the GEDA function switch turned to OPERATE, and then the recorder sweep started and auxiliary switch closed simultaneously. Taft indicates that the system will go into a limit cycle for larger inputs even though it is stable for a single pulse input. This is demonstrated in Fig. 41, where an initial step of four quanta was applied. Finally, it can be seen in Fig. 42 that the same system which went into a limit cycle with KvT=0.571 and ζ = 0.3, becomes stable if ζ is increased to 0.325. The results just presented demonstrate the type of problem for which the designed

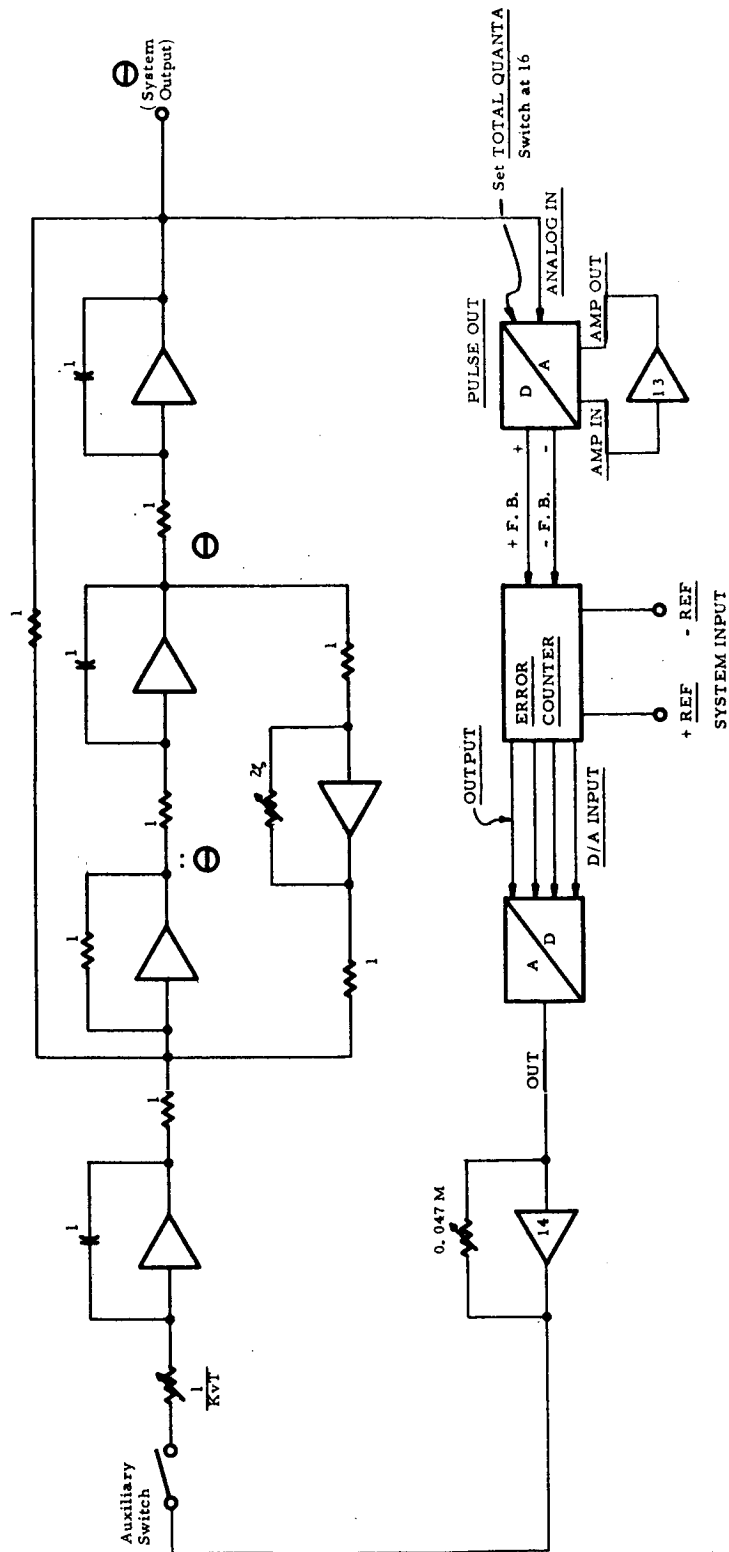FIG. 37 PULSE DATA SYSTEM SIMULATION

FIG. 3B - SINGLE PULSE TEST - VARIABLE KvT

FIG. 39 - SINGLE PULSE TEST - VARIABLE KₜT

$$G(s) = \frac{K_T T}{s(s^2 + 2\zeta s + 1)}$$

$\zeta = 0.3$

Limit Cycle Amplitude

KₜT = 0.555

KₜT = 0.571

1 Sec.

θ (Quanta)

θ (Volts)

-108-
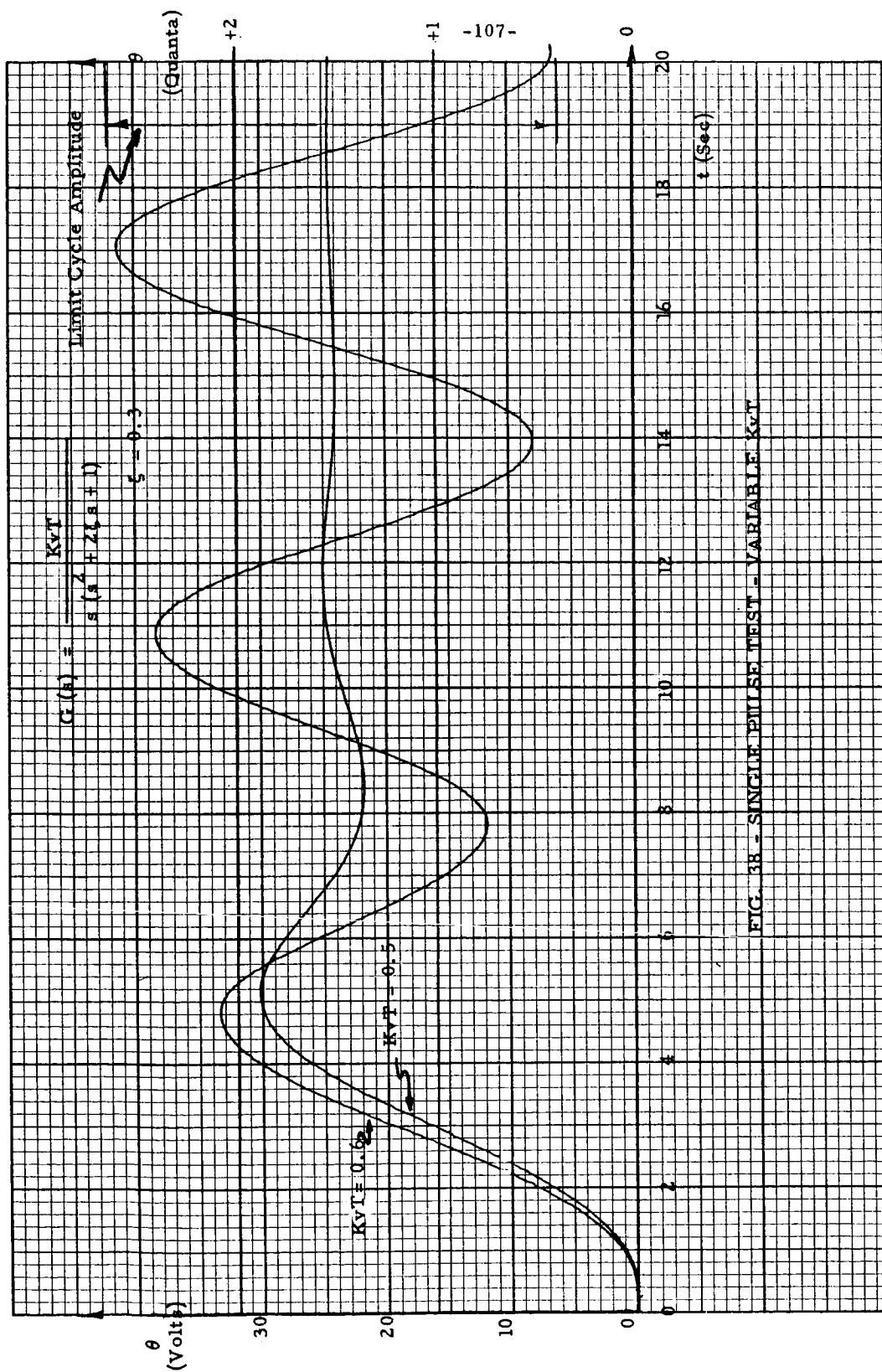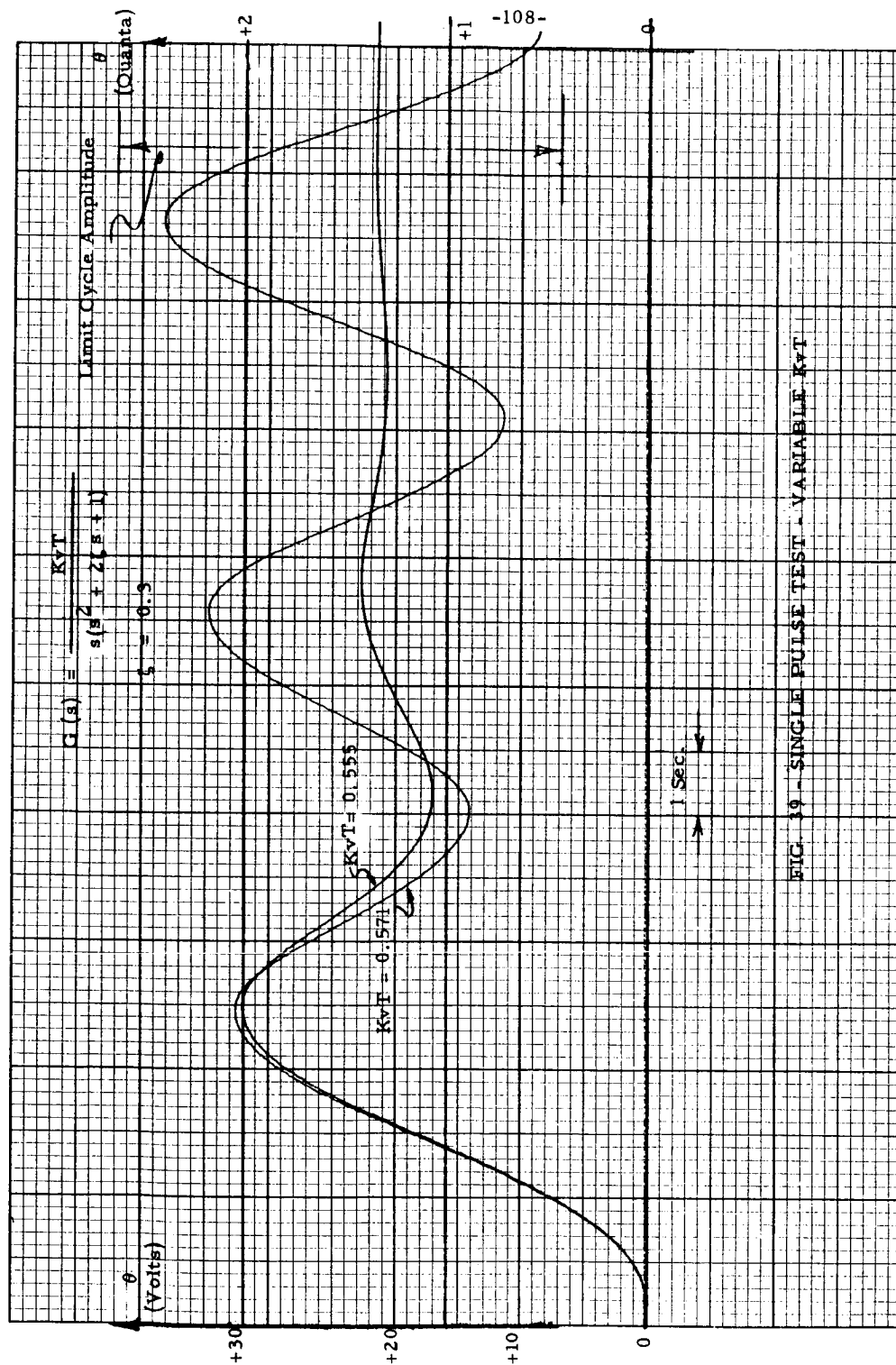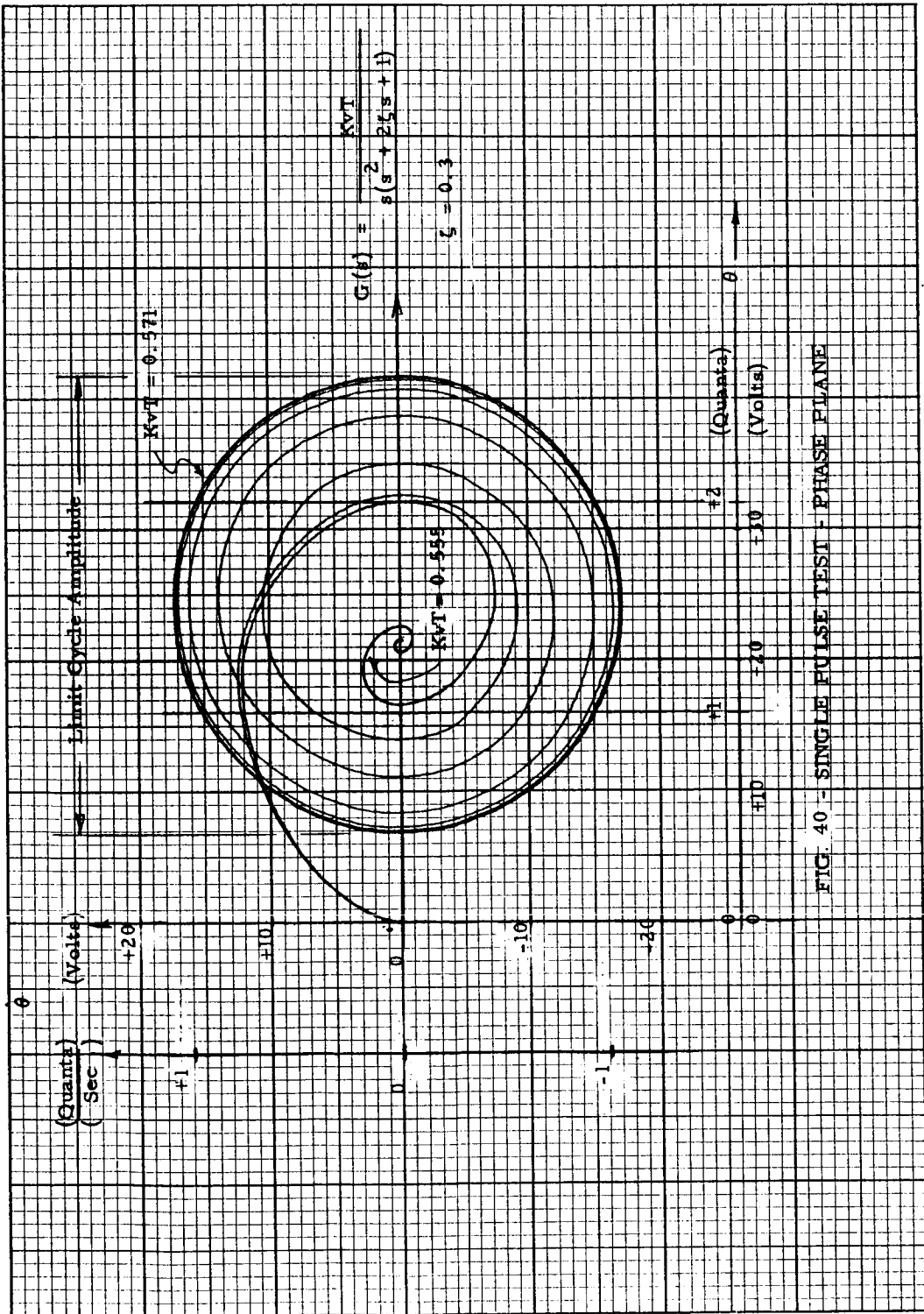
FIG. 40 - SINGLE PULSE TEST - PHASE PLANE

FIG. 41 FOUR QUANTA STEP RESPONSE TEST
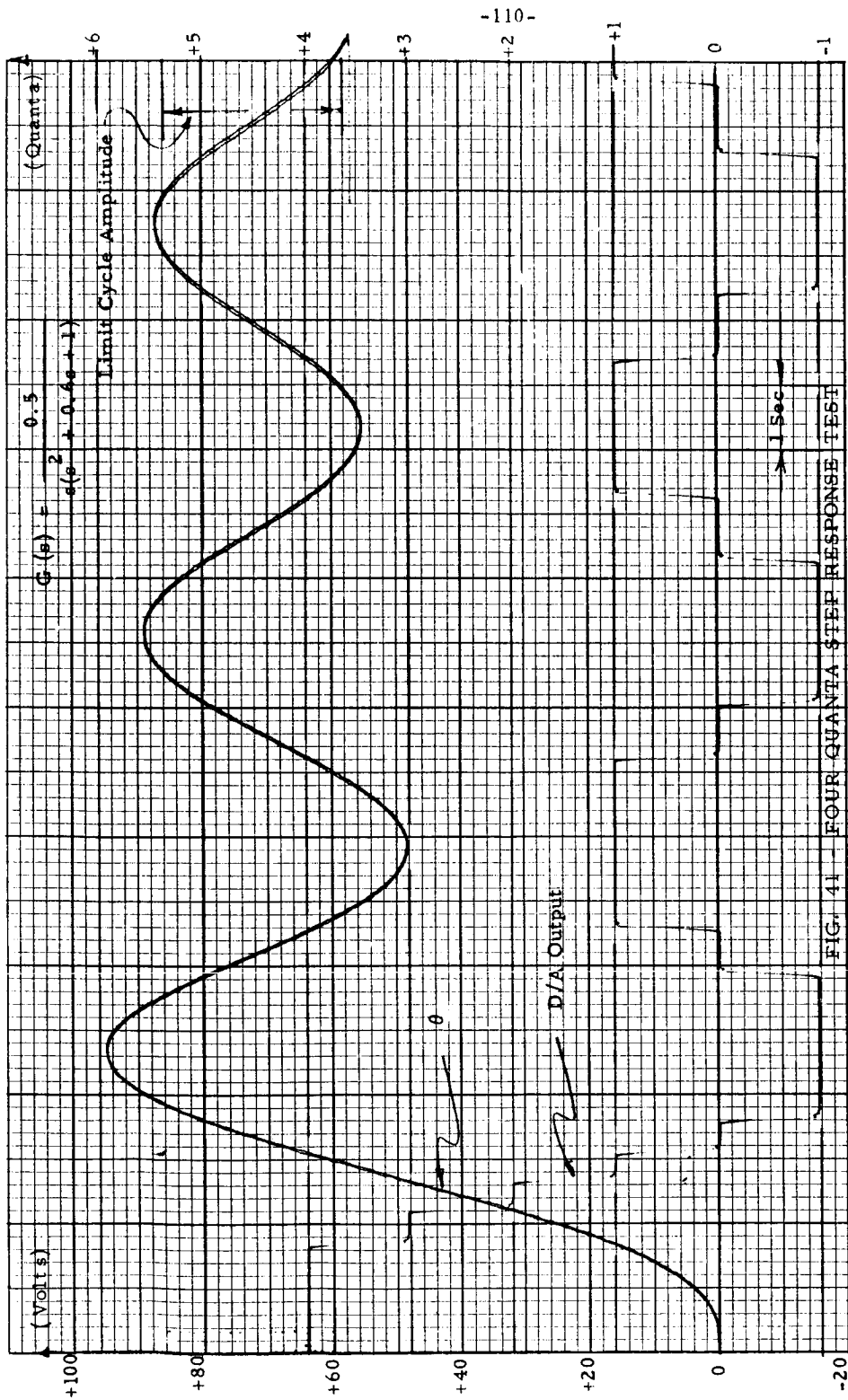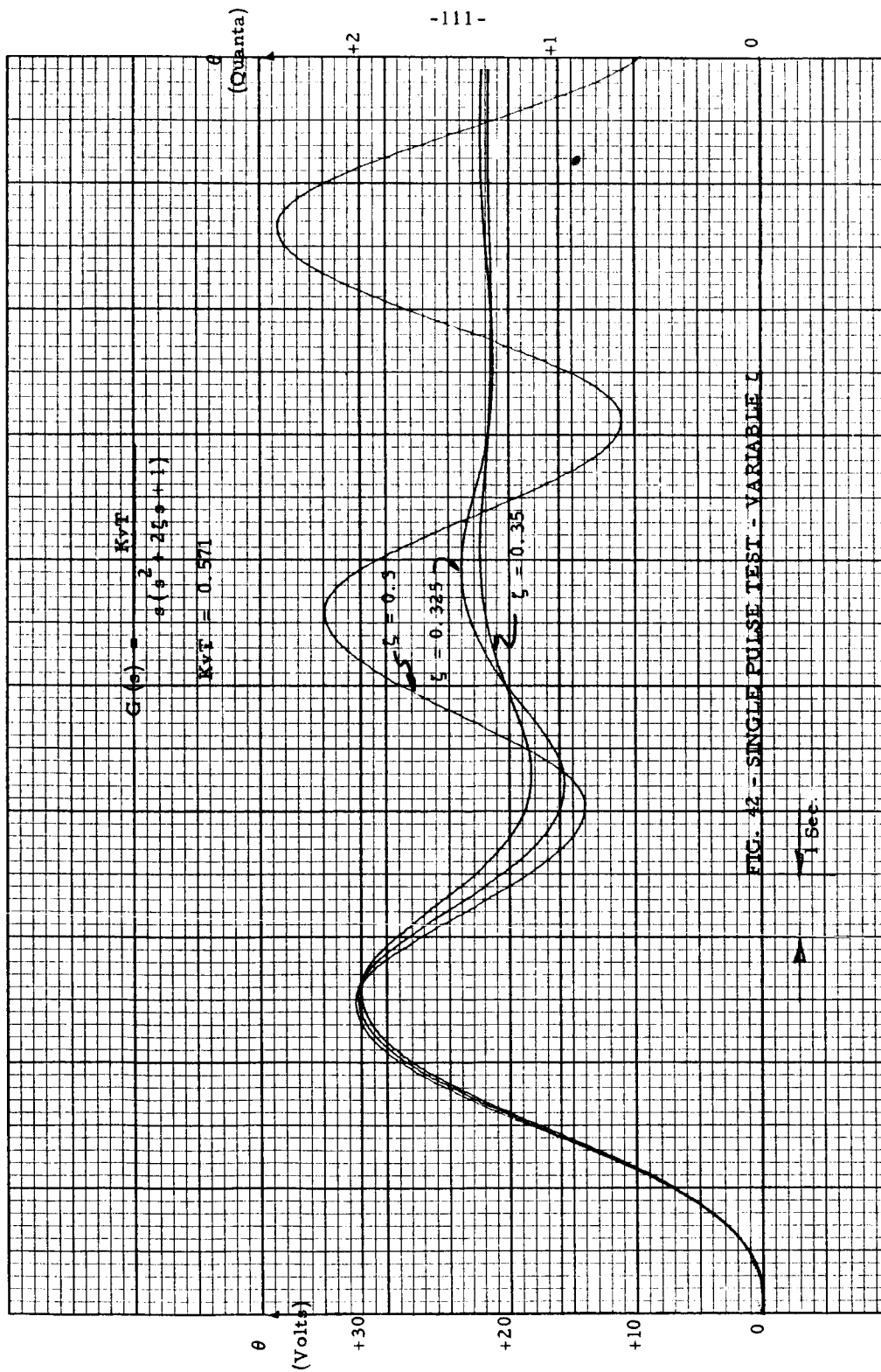
FIG. 42 - SINGLE PULSE TEST - VARIABLE ζ

system was intended, however, by no means must the simulated system be pulse data type.

5.3   Sampled Data Systems

Digital systems in which information appears in absolute form, as in Fig. 1, can also be simulated provided care is taken to synchronize the data extracted from the D/A. In addition, a "Hold" register must be supplied to hold the past value of the digital error (input to the D/A). Other than the synchronization problem, a sampled (and quantized) digital system simulation is patched-up much like a pulse data system. Fig.43 shows how an absolute digital control system with sampling might be simulated. This typical system has a sample clock pulse which gates reference and feedback information in parallel into a comparator which computes a digital error signal. In order to use the designed A/D converter in the feedback loop, the sample clock should be at least 1000 times slower than the A/D clock (less than 10 cps.) so that the A/D sampling effects can be neglected. In order not to gate the A/D output to the comparator when the A/D counter is going through a transistion, readout synchronization logic must be used as shown. The idea behind this synchronization method is to interrogate the A/D (and reference input) only while A/D counter carry enable lines are being
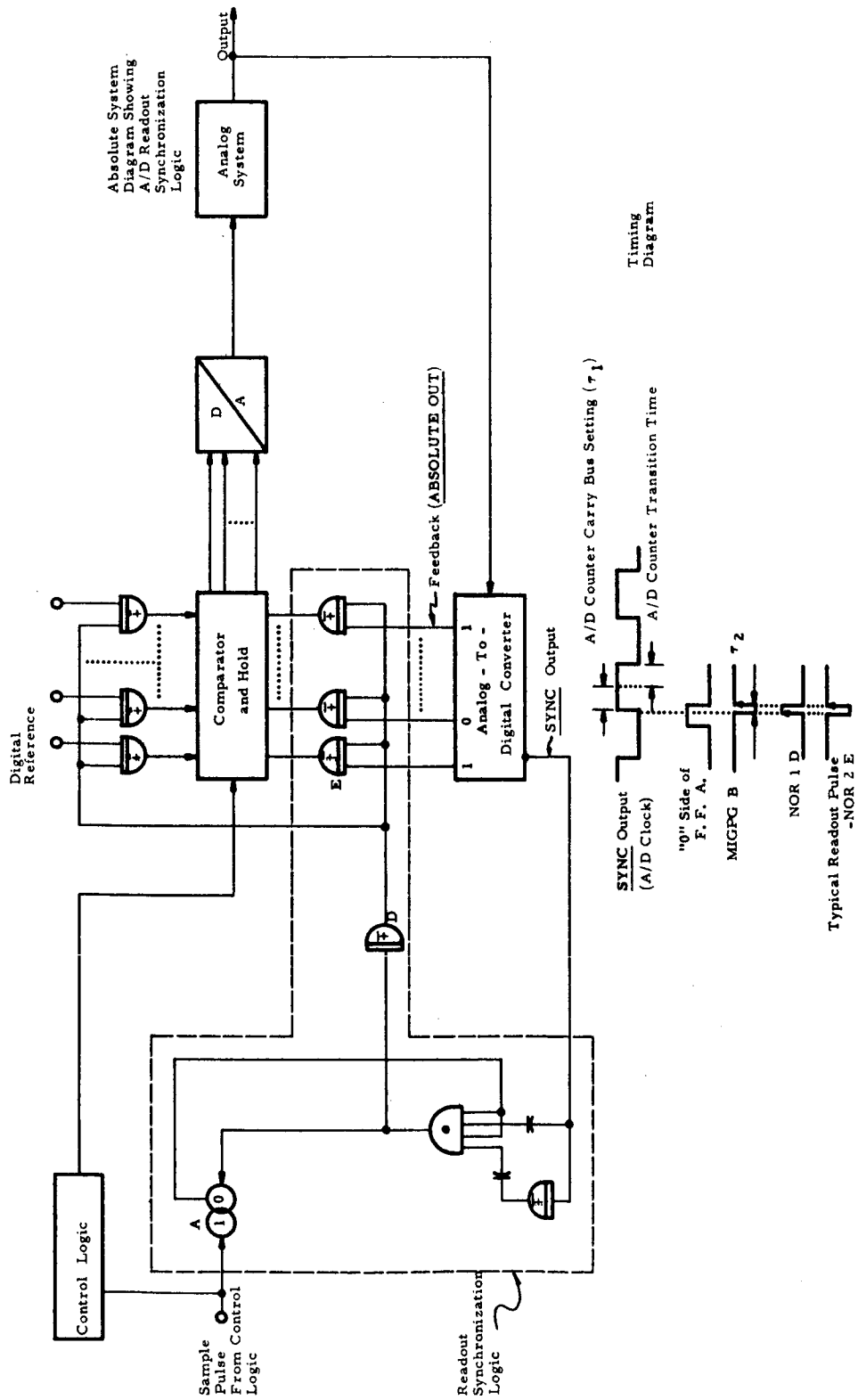
FIG. 43 ABSOLUTE SAMPLED DATA SYSTEM SIMULATION

set (τ_1). MIGPG B delay (τ_2) is made less than τ_1. Since τ_1 is 8 μsec., a τ_2 of 3 μsec. will allow the A/D to be read out before any counter transitions occur.

It is also possible to use the designed A/D converter in an absolute digital control loop where sampling is not used. One such system uses an absolute sign-only comparator for the feedback-reference summing junction, and the comparison operation can be done asynchronously. The A/D transition may cause unwanted spikes in the comparator (and hence the D/A) output, but these can be removed with a suitable low pass filter.

APPENDIX

OPERATION MANUAL

A.1 General System Description

A unit containing an A/D converter, a D/A converter, and a bidirectional counter and anti-coincidence circuit has been designed for use in digital control system simulation on the GEDA analog computer. In the following sections, complete instructions as to the use of the unit are given, and adjustment and calibration procedures are explained.

A.11 Functions

Figures A-1 and A-2 are photographs of the units showing switches, indicating lights, inputs, outputs, and adjustment locations. The following list serves to explain the function of all switches, lights, etc.

NAME	FUNCTION AND LOCATION
FRONT PANEL	
ON-OFF switch and pilot light	Lower right corner. Controls +6v., -12v., $\pm$ 200v. for the A/D converter and all digital logic.
ON-OFF switch and pilot light	Upper right hand side. Con-
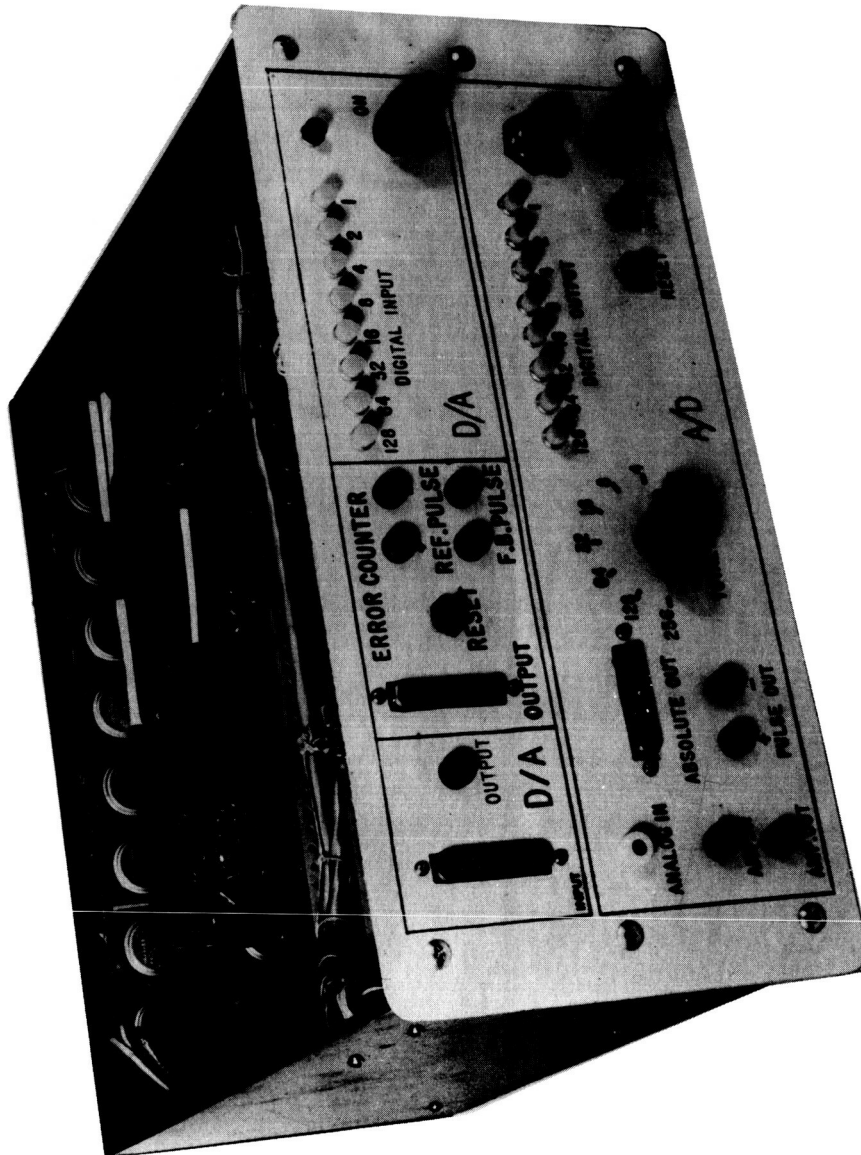
FIG. A-1 - FRONT PANEL
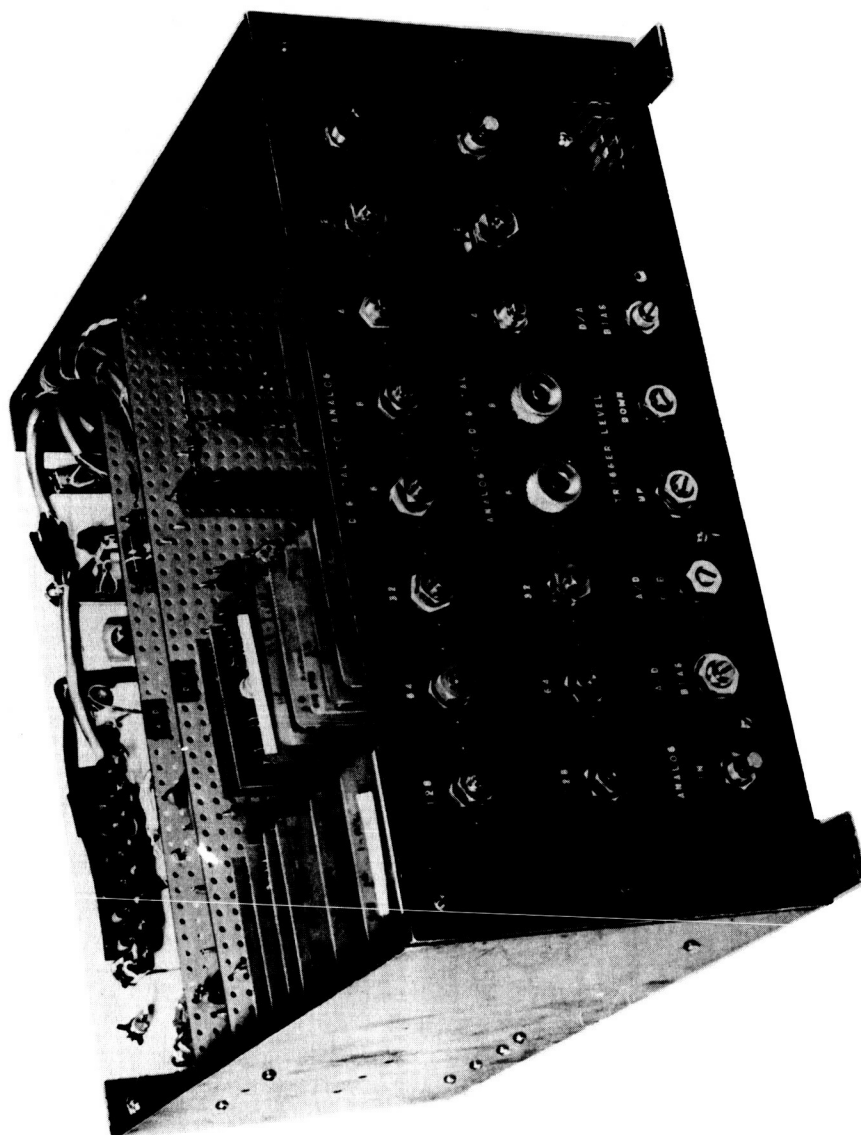
FIG. A-2 - REAR PANEL

trols +6v., -12v., $\pm$200v.
for the D/A converter.

ANALOG IN jack

Banana jack on left hand side.
The analog signal to be con-
verted is inserted here.

AMP. IN and AMP. OUT
jacks

Banana jacks on left hand
side. These are to be con-
nected with corresponding in-
put and output of a GEDA op-
erational amplifier for use as
part of the A/D converter.

PULSE OUT (+ and -)
jacks

Incremental A/D output jacks
(lower left). A -12v. pulse
on "+" indicates the analog
input passed a quanta line go-
ing positively.

TOTAL QUANTA switch

8 position switch. "256" po-
sition corresponds to quanti-
zation of 1 volt per quanta.
"2" position corresponds to
coarsest quantization, or 128
volts per quanta.

ABSOLUTE OUT connector
(A/D)

25 pin connector. Contacts
contain natural binary repre-
sentation of the analog input
signal. Pins 1 through 8 are
for -12v. true representation
(most significant bit is No. 8).
Pins 14 through 21 contain the
one's complement of the num-
ber in pins 1-8 respectively.

SYNC jack

Lower right hand corner.
Provides an output from the

	A/D clock for purposes of readout synchronization.
DIGITAL OUTPUT (128 through 1) (A/D)	Indicates state of A/D counter (natural binary representation of A/D output). Light drivers connect lights 128, 64, ..., 1 with ABSOLUTE OUT pins 8, 7, ..., 1 respectively.
DIGITAL INPUT (128 through 1) (D/A)	Can be used to display the input to the D/A converter. Light drivers connect lights 128, 64, ..., 1, with D/A IN-PUT connector pins 8, 7, ..., 1 respectively.
D/A INPUT Connector	25 pin connector. Pins 21 through 14 connect with most significant through least significant D/A stages respectively.
D/A OUTPUT jack	This is to be connected to a GEDA amplifier input to make up the D/A converter.
RESET button	Lower right corner. This allows the A/D counter to be reset to mid-scale (100000000 display on the DIGITAL OUT-PUT lights).
ERROR COUNTER OUTPUT	25 pin connector. Pins 21, 20, 19, and 18 are normally connected with D/A INPUT pins 21, 20, 19, and 18 respectively. Pins 8, 7, 6, and 5 are normally connected with D/A IN-PUT pins 8, 7, 6, and 5 for

light display.

ERROR COUNTER INPUTS

Connections for anticoincidence circuit inputs.

    + REF. PULSE jack

A pulse applied here will count error counter up.

    - REF. PULSE jack

A pulse applied here will count error counter down.

    + F. B. PULSE jack

A pulse applied here will count error counter down.

    - F. B. PULSE jack

A pulse applied here will count error counter up.

REAR PANEL

DIGITAL TO ANALOG
adjusting pots (single turn)

For adjusting each bit contribution to the D/A converter output. Clockwise rotation increases the "on" bit voltage contribution.

ANALOG TO DIGITAL
adjusting pots (single turn)

For adjusting bit contribution to the A/D converter internal error signal. Clockwise rotation increases the "on" bit voltage contribution.

A/D BIAS pot (single turn)

Counterclockwise rotation increases (positively) A/D zero level. (Normally 0v. =10000000 out).

A/D F. B. pot (single turn)

Used to adjust the amount of hysteresis in A/D con-

verter. Clockwise rotation
decreases hysteresis.

TRIGGER LEVELS (pots)
(single turn)

        UP

Adjusts the level at which
a negatively going **ANALOG
IN** voltage will cause the
"up" trigger to fire. Clock-
wise increases the trigger
level.

        DOWN

Adjusts the level at which
a positively going **ANALOG
IN** voltage will cause the
"down" trigger to fire.
Clockwise increases the
trigger level.

D/A BIAS pot (single turn)

Counterclockwise rotation
increases (positively) the
D/A "zero" output. (Nor-
mally, 10000000 in = 0 volts
out).

POWER INPUT connector

Pin 1, -12v.; connect to
-12v. supply.

Pin 2, +6v.; connect to +6v.
supply.

Pin 3, D/A gnd.; connect
to GEDA junction box term-
inal 15 and 16.

Pin 4, +200v.; connect to
GEDA junction box termi-
nal 13 and 14.

Pin 5, -200v.; connect to
GEDA junction box termi-
nal 17.

Pin 6, digital and chassis
ground; connect to GEDA
junction box terminal 15 and
16.

A.12 Supply Voltage Wiring Diagram

The preceding list serves as an overall checklist when

operating the simulator. In addition, Figure A.3, the supply voltage

wiring diagram, shows how the various sub-units (A/D counter, error

counter, etc.) are connected to the main supplies.

This takes care of general comments on the entire unit.

Next, the operation of each sub-unit will be discussed.

A.2 A/D Converter

The theory behind the operation of the A/D converter was

discussed in Chapter 3. The following is an explanation of the actual

A/D operating and adjusting procedures for both absolute and incre-

mental use.

A.21 Absolute Operation

The A/D converter can be set up to operate in an abso-

lute manner with a digital output in the form of an natural binary num-
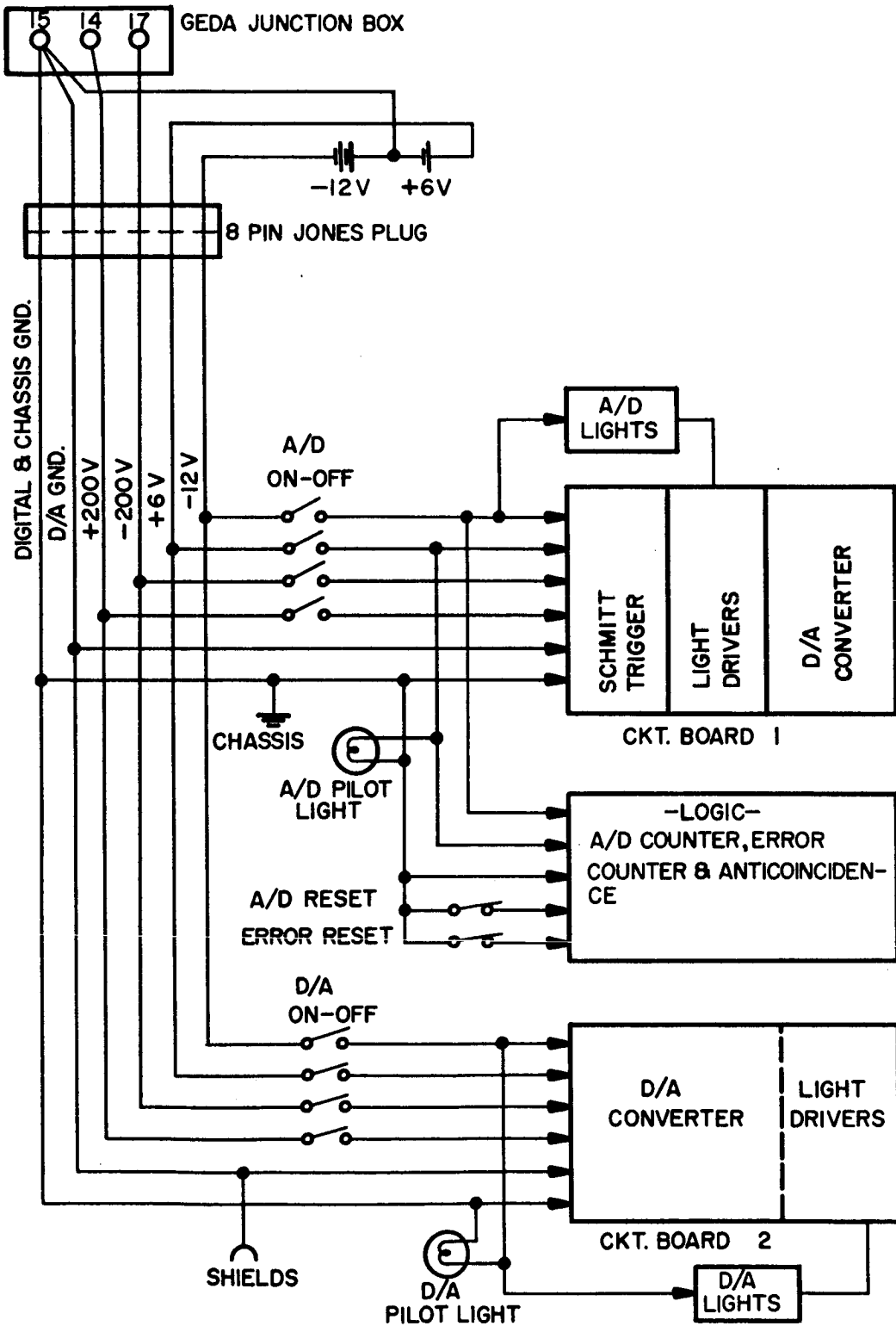
FIGURE A-3 SUPPLY VOLTAGE SCHEMATIC

ber. This mode of operation must be utilized when a digital (quantized) sampled data control system is to be simulated. Often, non-analytic codes are used to code digital information in an absolute system; however, in any systems to be simulated using this A/D, a natural binary code must be used, or provision must be made in the user's logic for suitable code-to-code conversion. Also, the user must supply a digital hold register for holding the past value of computed error.

Assuming the A/D has been properly adjusted and the power cord connected, the procedure for putting the converter into operation is as follows:

1) Select a desired scale factor. This can be 1, 2, 4, 8, 16, 32, or 64 volts per quanta.

2) Connect digital output wires (ABSOLUTE OUT connector). Assuming that bit values are true when the indicator lights are lit, make the connections based on the following:

   a) Pins 1 through 8 exhibit -12v. levels when bit values are true. Pin 8 is the most significant bit, and pin 1 is the least.

   b) Pins 14 through 21 exhibit 0v. levels when bit values are true. Pin 21 is the most significant bit, and pin 14 is the least.

       c)   Obtain the desired scale factor by con-
necting wires for the desired number ·⸴
of bits (2 through 8) starting by con-
necting the most significant bit line to
pin 8 or pin 21 (depending upon the
"truth" level desired, and connect the
remaining wires in order to the "less
significant" connector pins.

3)   Connect the analog voltage to be converted to the
ANALOG IN jack.

4)   Connect AMP. IN and AMP. OUT to the input and
output respectively of one GEDA operational am-
plifier.

5)   Warm up GEDA. Turn GEDA function switch to
I. C.

6)   Connect ANALOG IN to ground.

7)   Turn on A/D. Indicator lights should read
10000000. If not, push A/D RESET button to reset
converter to mid-scale (zero).

8)   Connect a line from the user's logic to the con-
verter's SYNC output as shown in Figure 42.
This connection must be made to insure that an
A/D interrogating pulse does not occur at the in-
stant the A/D may be in transition (at an A/D
clock time). Figure 42 shows one interrogating
circuit that can be built into the user's logic which
will prevent interrogation during transition times
as well as prevent ambiguity if the SYNC pulse oc-
curs simultaneously with the interrogate pulse.

The preceding instructions cover all cases where the

A/D output is taken as a binary number which is sampled periodical-

ly by an external command logic supplied by the user. Such Sampling should be done at a rate less than 10KC to minimize the effects of the A/D sampling. The other case of A/D operation, that in which the output information is taken as a pair of pulse trains, is the type for which the converter was specifically designed. Due to the fact that the logic required to manipulate these trains is quite simple compared to that required in an absolute system, a bidirectional counter and anticoincidence circuit was incorporated into the overall design. Next, the procedure for setting up a "pulse data" (incremental) control loop will be covered.

A.22 Incremental Operation

Again assuming the A/D has been adjusted, the steps in setting up the converter for incremental operation are as follows:

1) Repeat steps 1, 3, and 4 as under "Absolute Operation."

2) Instead of making connections as under step 2 of Sect. A2.1, connect PULSE OUT + to F. B. PULSE+ and PULSE OUT- to F. B. PULSE-. This assumes that the built-in bidirectional counter and anticoincidence circuit are to be used.

3) Set A/D QUANTA switch according to the desired scale factor. That is:

   for 1 volt/quanta, set the switch at 256
   for 2 volt/quanta, set the switch at 128

for 4 volt/quanta, set the switch at 64
for 8 volt/quanta, set the switch at 32
for 16 volt/quanta, set the switch at 16
for 32 volt/quanta, set the switch at 8
for 64 volt/quanta, set the switch at 4
for 128 volt/quanta, set the switch at 2

4) Warm up GEDA. Turn GEDA function switch to
    I. C.

5) Connect ANALOG IN to ground.

6) Turn on A/D. Indicator lights should read
    10000000. If not, push A/D RESET button to reset
    A/D to mid-scale (zero).

A.23 Adjustment and Calibration--A/D Converter

A quick check of A/D accuracy can be made by tracing out

out a curve on a X-Y plotter such as is shown in Figure 30. Set up

one of the GEDA integrators so that it integrated a step input to pro-

duce a slowly rising ramp voltage (one volt per second). Using a

piece of accurately ruled graph paper in the plotter, adjust the X-ax-

is gain so that a full-scale sweep occurs for 0 to 100 volts input. Ob-

tain the 100 volt calibrating signal from a GEDA potentiometer. Con-

nect the A/D ABSOLUTE OUT to the D/A INPUT. Feed the D/A out-

put to the plotter Y-axis and adjust the plotter and /or. D/A gain to

obtain a full-scale reading with the D/A output at 100 (11100100 = +100,

00011010 = -100). Connect the integrator output to the ANALOG IN

and plotter X-axis, and plot out the A/D's response to this slow ramp input. Y-axis step changes (D/A output) should occur at equal increments of A/D input. Repeat the test for ramps of both polarities. If the results of this check indicate too much A/D "roughness" and misalignment, the following adjustment procedure must be carried out.

The potentiometers which must be adjusted are: comparator levels (Up and Down Trigger Levels), A/D bias level, A/D feedback resistance, analog input resistance, and D/A bit resistances (8). Since there are so many adjustments to make, it is imperative that a systematic procedure be followed each time readjustment is required. The following is one suggested adjustment procedure.

1) Turn GEDA on. Put GEDA function switch on STANDBY.

2) With converter on bench, connect up power using power cord extension

3) Connect AMP. IN and AMP. OUT to input and output of a GEDA amplifier.

4) Connect ANALOG IN jack to the wiper of a GEDA pot, set up for a "minus" output voltage.

The UP and DOWN TRIGGER LEVELS are now ready to

be adjusted.

5)   Monitor AMP. OUT with the GEDA voltmeter or a sensitive voltmeter such as a 0.01 percent digital voltmeter.

6)   Turn on A/D and turn GEDA function switch to I. C.

7)   Manually increase (negatively) the voltage applied to ANALOG IN and observe the value of AMP. OUT voltage after which an abrupt change occurs. Decrease the input voltage to zero and repeat, adjusting the DOWN TRIGGER LEVEL potentiometer until the trigger fires at exactly -20.0v.

8)   Repeat step 6, but use a positive input voltage and keep readjusting the UP TRIGGER LEVEL pot until the UP trigger fires at exactly +20.0v.

The next sub-system to be adjusted is the A/D's D/A converter.

9)   Turn off A/D and put GEDA in STANDBY.

10)   Disconnect plug marked "LIMITER", located on circuit board marked "D/A". This removes limiters and built-in feedback resistor from circuit.

11)   Remove jumper from GEDA amplifier output to AMP. OUT jack.

12)   Patch a variable resistor across the GEDA amplifier. This resistor should be set at about 30K initially.

13)   Disconnect the A/D clock by removing the FRMV card from card location 5. Replace this clock with a slow speed mutivibrator (2-10 cps) such as

a Wang variable frequency pulse generator. Connect one pulse generator to pin M, card location 15, and the complementary pulse signal to pin P, card location 15.

14) Connect a variable d. c. supply (up to $\pm$ 25 v.) to the __AMP. OUT__ jack. The A/D counter can now be counted up or down at a slow rate by increasing the d. c. supply voltage enough to trigger the __UP__ or the __DOWN__ trigger. This will facilitate the job of checking out the D/A output for all possible input numbers (states of the A/D counter).

15) Turn the GEDA to I. C. and the A/D __ON__.

16) Push __RESET__ to reset the A/D counter to mid-scale.

17) Monitor the GEDA amplifier output on a voltmeter (D.V.M. or GEDA standard potentiometer) and adjust the __A/D BIAS__ pot until the amplifier output is zero.

Now begins the D/A bit adjusting procedure. The main idea is to have each bit voltage contribution in the amplifier output differ from its neighbor by a factor of 2. Two main restrictions will cause trouble in making the adjustments. First, each bit voltage contribution must be such that it is possible to adjust the other bits, increasing or decreasing by powers of 2, without coming to the end of a pot. Also, no pot must be turned to within less than 10 percent of the end where it exhibits zero resistance. This insures against excessive noise amplification when a bit is in the "off" state.

18) Count the A/D counter down until all indicator lights are off.

19) Adjust the patched-in feedback resistor on the GEDA amplifier until the amplifier output is 64.0v. Use the following table of desired voltage values for various primary counter readings.

Counter Reading	Desired Amplifier Output Voltage	Counter Reading	Desired Amplifier Output Voltage
00000000	-64.0v.	10000001	+0.5
00000001	-63.5	10000010	1.0
------10	-63.0	-----100	2.0
-----100	-62.0	----1000	4.0
----1000	-60.0	---10000	8.0
---10000	-56.0	--100000	16.0
--100000	-48.0	11000000	32.0
01000000	-32.0	11111111	63.5
10000000	00.0		

20) Count the counter up and successively adjust each bit voltage to the value indicated on the above chart. It is a good idea to check to see that the mid-scale reading still produces 0v. output after each adjustment has been made. If necessary, bring it back to zero with the A/D BIAS pot.

21) If the D/A is completely out of adjustment at the outset, steps 17 through 20 may have to be repeated a number of times so as to be able to bring all bits into line without running any one adjusting potentiometer to either end of its travel.

22) After each of the eight bits has been adjusted singly, or in combination with the most significant bit, other combinations may be checked and further corrections made to distribute any errors present more evenly over a range of output values.

23) Reconnect the A/D for normal operation. Apply a +100v. signal to ANALOG IN. Adjust ANALOG IN pot so that just as the applied analog voltage reaches +100v. (increasing slowly positive) the DIGITAL OUTPUT reads 11100100 (+100). Repeat using a slowly increasing (negatively) signal and readjust ANALOG IN pot so that the A/D counter reads 000111000 (-100) just as the ANALOG IN signal reaches -100v.

24) A/D F. B. pot must now be adjusted. It controls the amount of hysteresis present in the A/D. Apply a low frequency (< 5 cps) sine wave of a few volts amplitude to the converter. Look at AMP. OUT on an oscilloscope. Slowly turn A/D F. B. pot clockwise. Stop when multiple oscillations can be observed at a trigger transition in the AMP. OUT signal. Turn back the A/D F. B. pot slightly to insure that no multiple oscillations, caused by too little hysteresis occur.

Now that the A/D converter has been adjusted, a check to verify its operation can be made.

A.24 A/D Checkout

A check for A/D linearity and absolute accuracy can be made by recording the AMP. OUT wave form in response to a slow (quasi-static) ramp input.

1) Set up a GEDA integrator such that RC for the integrator is about 10 seconds. Apply a step input of 10 volts and adjust the integrator resistor so that the output ramp is exactly 1.00v./sec. This can be done using a stopwatch and checking the integrator output after a 100 second run.

2)   Having set up an integrator which puts out a 1v./ sec. ramp, attach a strip chart recorder, with a one second time marker built in, to AMP. OUT.

3)   Apply the 1v./sec. ramp to ANALOG IN and record AMP. OUT on the strip chart. The result should be a sawtooth wave with a 1.00 second period.

4)   The strip chart record can be examined for any irregularities in sawtooth period, and thus any repetitive errors caused by bit misadjustment can be quickly located.

A.3 D/A Converter

The D/A converter has been covered in chapter 3 as well as in the preceding section A.2, since the D/A converter used is essentially identical to the D/A converter found as part of the A/D converter.

A.31 D/A Operation

The procedure for operating the D/A is as follows:

1)   Select the number of input bits required.

2)   Connect the most significant bit line ('0v. "true") to D/A INPUT connector, pin 21. Lesser significant bit lines should be connected to pins 20, 19, --- down to 14, respectively. Any bit locations not being used must be tied to ground.

3)   If the digital signal to be converted is to be displayed on the DIGITAL INPUT lights, connect the most significant bit line (-12v. "true") to pin 8.

Lesser significant bit lines should be connected
to pins 7, 6, --- down to 1 respectively.

4) Connect the <u>D/A OUTPUT</u> jack to the input of a
GEDA amplifier.

5) Patch a one megohm variable decade resistor
across the GEDA amplifier. The actual value at
which the variable resistor should be set depends
upon the desired quanta size. The setting proce-
dure is to first set in the maximum number as in-
put to the D/A. Knowing what analog output volt-
age this input should produce, adjust the decade
resistor until the amplifier output is at the de-
sired level. This output voltage can be checked
with the GEDA calibrating potentiometer.

6) Turn the D/A on with the switch located in the
upper right hand corner of the front panel.

A.32 <u>D/A Adjustment Procedure</u>

Adjustment of the D/A converter is essentially the same
as adjustment of the A/D's D/A converter. The adjusting procedure
is as follows:

1) Set up the D/A for operation as in steps 1 through
5 in section A.31. Use as inputs to the D/A the
<u>ABSOLUTE OUT</u> output of the A/D converter.

2) Set the digital input to 10000000 and adjust the
<u>D/A BIAS</u> pot until the D/A output is zero volts.

3) Adjust each D/A bit by successively applying var-
ious input numbers by varying the analog input to
the A/D, following the procedure in steps 17
through 22 of section A.23 for the A/D's D/A.

A.4 Error Counter and Anticoincidence Circuit Operation

A single pulse data control loop can be simulated by using the A/D converter, D/A converter, and the error counter and anticoincidence circuit included in the unit. Connections for the error counter are provided at the top center of the front panel.

The counter has four bits, and may be reset to 1000 with the ERROR COUNTER RESET button. Counter output lines are terminated in the ERROR COUNTER OUTPUT connector. Pins 1, 2, 3, and 4 are permanently grounded, and pins 5, 6, 7, and 8 are "-12v. true" outputs, 5 being the least significant bit. The complementary outputs ("0v. true") are pins 18, 19, 20, and 21, 18 being the least significant. Pins 14, 15, 16, and 17 are permanently tied to -12v.

+REF. PULSE and +F. B. PULSE inputs are wired to the anticoincidence circuit such that a pulse on the +REF. PULSE line will count the counter up, and a pulse on the +F. B. PULSE line will count the counter down; similarly for -F. B. PULSE and -REF. PULSE inputs.

A.5 Parts Costs

The following is a breakdown of the approximate cost of reproducing one D/A converter, one A/D converter, and one error counter plus anticoincidence circuit, complete with chassis.

1) D/A Converter

   a) D/A

      Resistors - - - - - - - - 14.00
      Potentiometers - - - - - - 20.00
      Transistors - - - - - - - - 9.00
                                  43.00

   b) Miscellaneous Hardware and Indicator Lights - - - - - - - - - - - - - 24.00

                            TOTAL $67.00

2) A/D Converter

   a) D/A

      Same as (1a)- - - - - - - - 43.00

   b) Miscellaneous Resistors, Pots, and Diodes - - - - - - - - - - - - - 12.00

   c) Parts for Logic Cards

      4 - Type 302 B.D.C. Cards
      1/2- NOR 2 Card
      1 - FRMV Card
      2/3- NOR 1 Card
      1/2- Type 308 MIGPG Card

                       - - - - - - - 28.00

d)   <u>Comparator</u> (Schmitt Triggers)- - - - 10.00

e)   <u>Miscellaneous Hardware and Indicator Lights</u>   - - - - 40.00

TOTAL $133.00

3)   <u>Error Counter and Anticoincidence Circuit</u>

a)   <u>Parts for Logic Cards</u>

7 - Type 311 RSTT Flip-flop Cards
2 - Type 302 B.D.C. Cards
1 - FRMV Card
1 - NOR 2 Card
1 - Type 214 G.P.G. Card
1/3 - NOR 1 Card
1/2 - Type 308 MIGPG Card

- - - - 37.00

b)   <u>Miscellaneous Hardware and Indicator Lights</u>   - - - - 18.00

TOTAL $55.00

4)   <u>Chassis (Labor and Material)</u>

Estimated - - - - - - - - - $75.00

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