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A TRANSITION MAP METHOD OF COUNTER SYNTHESIS

Report No. EDC 1-65-35

by

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1965

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ABSTRACT

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Conventional procedures for the synthesis of counters apply only to synchronous designs. A synthesis method is presented which provides a complete description of the logical operation of both synchronous and asynchronous counters.

The logical operation of a flip-flop is characterized in terms of state transitions.

A convention is defined for representing the logical action of a flip-flop on a map.

A standard form of problem statement is given, and rules for translating the synthesis problem into transition map form are presented.

Input equation derivation rules and input equation requirements are defined.

The asynchronous synthesis procedure is formally defined, and a detailed example of its application is given.

Author

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I INTRODUCTION TO TRANSITION MAPS

Historical Background

The concept of using a modified form of Venn diagram as a means of simplifying Boolean expressions was first proposed by E. W. Veitch [1] in 1952. The following year M. Karnaugh [2] introduced the change in the organization of Veitch charts which resulted in the present form of maps.

The map method of simplification presented by Karnaugh has proved to be extremely valuable for the synthesis of combinational logic because it provides insight into the structure of a Boolean expression. The introduction of additional notation in 1961 by H. W. Mergler [3] and independently by M. P. Marcus [4] in 1962 resulted in the ability of maps to provide insight into the structure of sequential circuits. In the transition map scheme presented by Mergler, not only the relationships between the entries on the map for each individual flip-flop, but also the relationships between entries on the maps for different

flip-flops are utilized. This added dimension provides the information necessary for the synthesis of asynchronous counters in which each flip-flop makes at most one transition between stable states of the counter. In the transition map method described here, a dimension corresponding to time is added in order to enable the synthesis of asynchronous counters in which the flip-flops may make more than one transition between stable states of the counter.

Flip-Flop Logical Operations

The type of flip-flop to be considered, commonly referred to as an R-S-T flip-flop, is shown symbolically in Figure 1.

The flip-flop has four outputs -- two pulse outputs and two level outputs. The two level outputs, q and $\bar{q}$, define the state of flip-flop Q at all times except transient periods. When q = 1, the flip-flop is said to be in the ONE state. When q = 0, it is said that the flip-flop is in the ZERO state. The two level outputs always assume complementary values -- whenever q = 0, then $\bar{q}$ = 1; and whenever q = 1, then $\bar{q}$ = 0.

The two pulse outputs, α_Q and β_Q, define the state-of-transition of flip-flop Q at all times. An α transition is defined to be the change in state of a flip-flop that occurs as the flip-flop goes from the ZERO state to the ONE state. When α_Q = 1, the level output $\bar{q}$ changes from $\bar{q}$ = 1 to $\bar{q}$ = 0, and flip-flop Q is said to make an α transition. A β transition is defined to be the change in state of a flip-flop that occurs as the flip-flop changes from the ONE state to the ZERO state. When β_Q = 1, the

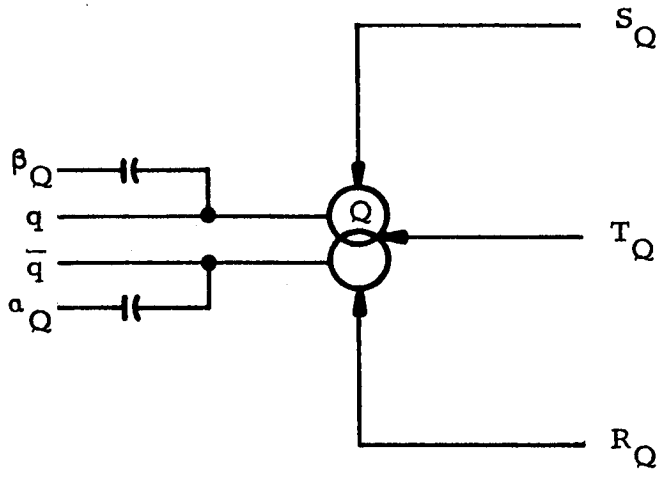


Figure 1. R-S-T Flip-Flop.

level output q changes from q = 1 to q = 0, and flip-flop Q is said to make a β transition. The two pulse outputs have the following characteristics: Two pulses are never present simultaneously -- whenever $\alpha_Q = 1$, then $\beta_Q = 0$; and whenever $\beta_Q = 1$, then $\alpha_Q = 0$. Two pulses never appear successively at the same output without an intervenient pulse at the opposite output. If neither pulse is present -- $\alpha_Q = 0$ and $\beta_Q = 0$ -- the state of the flip-flop is defined by the two level outputs, q and $\bar{q}$.

The R-S-T flip-flop has three inputs -- a RESET, a SET, and a TRIGGER input; denoted by "R," "S," and "T," respectively. The inputs control the logical operation of the flip-flop in the following manner:

If flip-flop Q is in the ZERO state, a pulse at the SET input will cause Q to make an α transition -- $\alpha_Q = 1$. If the flip-flop is in the ONE state and a pulse appears at the SET input, the state of the flip-flop will not change.

When the flip-flop is in the ZERO state, a pulse at the RESET input has no effect on its state. When flip-flop Q is in the ONE state, a pulse at the RESET input

forces the flip-flop to make a β transition -- $\beta_Q = 1$.

If flip-flop Q is in the ZERO state and the TRIGGER input is pulsed, the flip-flop will make an α transition -- $\alpha_Q = 1$. If Q is in the ONE state and the TRIGGER input is pulsed, Q will make a β transition -- $\beta_Q = 1$.

If the SET and TRIGGER inputs are pulsed simultaneously when the flip-flop is in the ZERO state, the effect will be the same as that of pulsing either input alone, and the flip-flop will make an α transition. If the flip-flop is in the ONE state and both the SET and TRIGGER inputs receive signals at the same time, the action of the flip-flop will be indeterminate.

When the TRIGGER and RESET inputs are pulsed simultaneously, and the flip-flop is in the ONE state; the result is the same as the result of pulsing either input alone, that is, the flip-flop makes a β transition. If the flip-flop is in the ZERO state when both the TRIGGER and RESET receive pulses, the action of the flip-flop will be indeterminate.

If the SET and RESET inputs or all three inputs are pulsed simultaneously, the action of the flip-flop will be

indeterminate.

The R-S-T flip-flop as a physical device has certain inherent delays and restrictions. There is a finite time lapse between the arrival of an input pulse and the reflection of its effect at the output. Consecutive input signals must be sufficiently spaced in time in order for the flip-flop to properly respond. Both of these points will be taken into consideration in arriving at a practical design.

Transition Maps

A transition map is a precise description of the logical action of a given flip-flop under a particular set of circunstances. Transition maps are presented in the format of Karnaugh maps. Each square of a transition map represents an initial set of flip-flop states, and each map is uniquely associated with a particular flip-flop.

Entries on the maps describe the action of the associated flip-flop for each initial combination of flip-flop states according to the following convention:

If, for an initial combination of flip-flop states, the associated flip-flop does not receive an

input pulse, the square is left blank.

If an input causes the flip-flop to make an α transition, the entry is an "α." From the definition of an α transition, an "α" can only be entered on the half of the map for which the initial state of the associated flip-flop is ZERO.

If the flip-flop associated with the map is initially in the ZERO state, and if an input pulse causes the flip-flop to remain in the ZERO state; the map entry is a "0."

If the result of an input pulse is a β transition, the map entry is a "β." By definition, a "β" can only be entered on the half of the map for which the associated flip-flop is initially in the ONE state.

If the associated flip-flop is initially in the ONE state, and if an input pulse results in the flip-flop remaining in the ONE state; the entry is a "1."

If a particular initial set of flip-flop states does not occur, or if the action of the associated flip-flop is indeterminate for a particular initial

combination of states, the entry is a "-."

Transition maps can be used in two ways. The first is in the determination of the logical action of a flip-flop when its input equation set is given. Using the convention defined above and the definition of RESET, SET, and TRIGGER inputs; a single-variable transition map can be derived for each of the following input equation sets:

$$\begin{Bmatrix} R_Q = p \\ S_Q = 0 \\ T_Q = 0 \end{Bmatrix} \quad \begin{Bmatrix} R_Q = 0 \\ S_Q = p \\ T_Q = 0 \end{Bmatrix} \quad \begin{Bmatrix} R_Q = 0 \\ S_Q = 0 \\ T_Q = p \end{Bmatrix}$$

In these equations and throughout the following, a lower-case "p" is used to denote a pulse source. The transition maps corresponding to these equations sets are shown in Figure 2. The convention is adopted that if an input is equal to "0" -- that is, if an input does not receive a pulse -- the equation is simply omitted from the equation set.

In each of the three sets of input equations above, only one input receives a signal. Single variable transition maps can also be derived for each of the three combinations of two simultaneous input pulses and for the

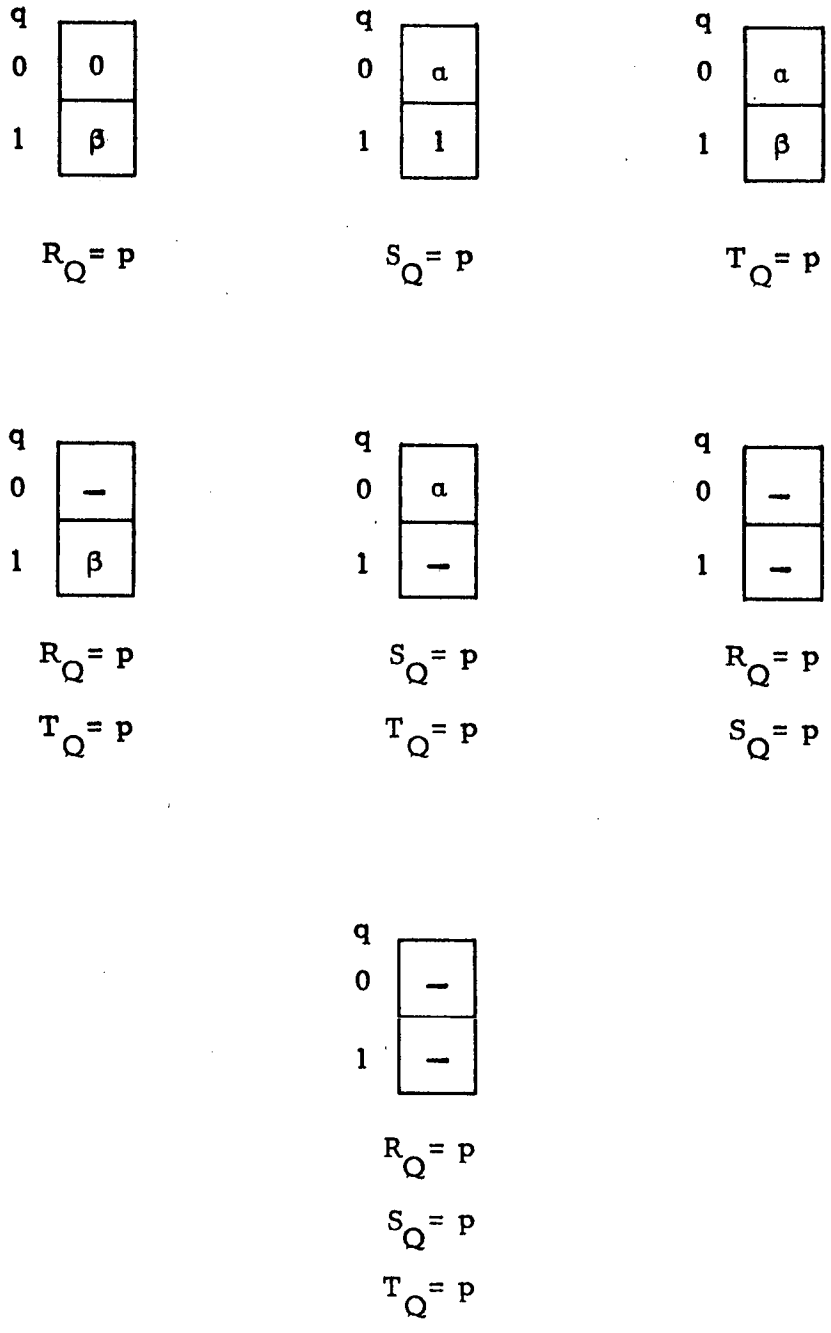


Figure 2. Single-variable transition maps derived from input equations for flip-flop Q.

case of three simultaneous signals:

$$\left\{\begin{matrix} R_Q = p \\ S_Q = p \end{matrix}\right\} \quad \left\{\begin{matrix} R_Q = p \\ T_Q = p \end{matrix}\right\} \quad \left\{\begin{matrix} S_Q = p \\ T_Q = p \end{matrix}\right\} \quad \left\{\begin{matrix} R_Q = p \\ S_Q = p \\ T_Q = p \end{matrix}\right\}$$

The transition maps corresponding to these equation sets follow directly from the descriptions given previously. Figure 2 displays these maps.

The second manner in which transition maps are used is in the derivation of input equations when the logical action of a flip-flop is specified. In contrast to the previous problem, the determination of the logical action of a flip-flop from its input equation set, the problem of deriving a set of input equations from a given transition map does not necessarily have a unique solution.

Consider the following transition map:

Flip-Flop Q:

q	
0	α
1	

By the previously defined convention for map entries, this map indicates that when flip-flop Q is initially in

the ZERO state, it receives an input pulse which causes it to make an α transition. When flip-flop Q is initially in the ONE state, it does not receive <u>any</u> input signal. An examination of Figure 2 shows that an "α" may be entered on a map as a result of either a SET input or a TRIGGER input or both -- the input equation is not uniquely determined. Because the q = 1 square of the above map is blank, the input signal which produces the α transition when flip-flop Q is in the ZERO state must be inhibited when Q is in the ONE state. Thus, the input equation corresponding to the above transition map is $S_Q = \bar{q} \cdot p$ or $T_Q = \bar{q} \cdot p$ or both. These three are equivalent to each other in that each will produce the logical action defined by the transition map.

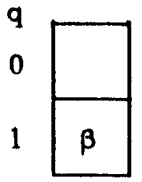
The following transition map indicates that when the associated flip-flop is initially in the ZERO state, it does not receive an input signal. When the flip-flop is initially in the ONE state, it receives an input pulse and remains in the ONE state.

Flip-Flop Q:

q	
0	
1	1

Reference to Figure 2 shows that a "1" may be entered on a map only when the input is a SET pulse. In order that the flip-flop associated with this map not receive an input pulse when it is in the ZERO state, the input pulse is inhibited when q = 0 -- $S_Q = q \cdot p$.

The input equations corresponding to the map entries "α" and "1" have been derived. These correspondences and those for "β" and "0" are illustrated in Figure 3.



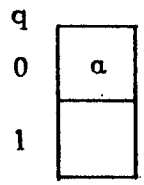
$R_Q = q \cdot p$

or

$T_Q = q \cdot p$

or

$$\left\{ \begin{array}{l} R_Q = q \cdot p \\ T_Q = q \cdot p \end{array} \right\}$$



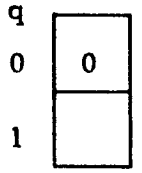
$S_Q = \bar{q} \cdot p$

or

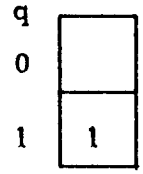
$T_Q = \bar{q} \cdot p$

or

$$\left\{ \begin{array}{l} S_Q = \bar{q} \cdot p \\ T_Q = \bar{q} \cdot p \end{array} \right\}$$



$R_Q = \bar{q} \cdot p$



$S_Q = q \cdot p$

Figure 3. Input equations derived from transition maps for a flip-flop Q.

II. THE SYNTHESIS OF SYNCHRONOUS COUNTERS

Introduction

In the preceding chapter, the description of the logical operation of the R-S-T flip-flop was translated into transition map representation, and the results were shown in Figure 2. Using these results as a basis, input equations corresponding to the map entries "α," "β," "1," and "0," were determined. The correspondences were illustrated in Figure 3. The relationships displayed in Figure 2 and 3 form the basis for the transition map synthesis technique. In this chapter, the concepts of determining transition maps from input equations and vice versa will be generalized to include the case of multivariable maps. This augmented technique will then be applied to some illustrative examples.

Problem Statement and Translation

In the counter synthesis problems which will be considered,

the problem statement will be in the form of a specified sequence of counter states. Table 1 specifies a state sequence for a counter with two flip-flops.

The problem statement is translated from the counter state sequence table into transition map form by use of the following rules:

1. Draw and label one transition map for each flip-flop required for the counter. Each map must display all possible states of the counter.
2. Determine which of the possible counter states, if any, do not occur in the sequence. For each such state, enter a "-" in the corresponding square on every map.
3. For each counter state in the sequence, determine which type of transition, if any, each flip-flop makes when the counter goes into the next state in the sequence. Enter these transitions on the maps. Do not make "0" or "1" entries.

As an example of the application of the rules above, consider the sequence in Table 1. Rule 1 requires that two two-variable maps be drawn and labeled. Rule 2 states

TABLE 1

SEQUENCE OF COUNTER STATES

A	B
0	0
0	1
1	1
0	0

that any redundancies are to be entered on the maps. Since there are four possible states for a two bit counter, and since there are only three different states listed in the sequence, there is one redundant state. Rule 3 requires that each state in the sequence be inspected. When the counter goes from its initial state of 00 to the 01 state, flip-flop B makes an α transition. Thus, an "α" is entered in the 00 square on the map for flip-flop B. Because flip-flop A does not make a transition at this time, the 00 square on the map for flip-flop A is left blank. At the next input pulse, the counter goes from the 01 state into the 11 state. Now A makes an α transition, and B remains in the ONE state. Thus, an "α" is entered in the 01 square on the map for A, and the 01 square on the map for B is left blank. When the counter receives a third input pulse, it returns to the 00 state. Both flip-flops make β transitions; therefore, a "β" is entered in the 11 square on both maps. The completed maps are shown in Figure 4.

Assumed Form of Combinational Circuitry

In the synthesis examples which are to follow, various

Flip-Flop A:

a \ b	0	1
0		α
1	—	β

Flip-Flop B:

a \ b	0	1
0	α	
1	—	β

Figure 4. Result of application of translation rules to sequence in Table 1.

logical elements will be used in addition to the R-S-T flip-flop.

In forming logical functions of the flip-flop output levels, the AND-OR-NOT system will be used. It will be assumed that the propagation times associated with these three elements are negligible compared to the delays inherent in the R-S-T flip-flop. This assumption implies that pulses from a given source will reach their destinations at essentially the same time, regardless of the difference in the number of gates in each path. In this way, the advantages of being able to pulse more than one input to a flip-flop at a time can be fully exploited without requiring that the number of levels of gating be the same for inputs which are to receive simultaneous pulses.

Two pulse logic elements, a PULSE-AND gate and a PULSE-OR gate will be used in the implementation of flip-flop input equations. Symbolically, no differentiation will be made between PULSE-OR and OR gates, although in practice, different circuits might be used. The propagation time of the PULSE-OR will be assumed negligible.

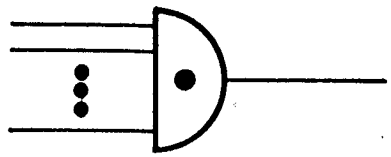
The PULSE-AND gate will have the following characteristics. The element will have one pulse input and at least

one level input. The output will be in pulse form, and there will be negligible delay between input pulse and output signal. A pulse at the input will cause a pulse to appear at the output if and only if all the level inputs have the truth value ONE at the instant the pulse first appears at the input. The output of the PULSE-AND gate will be based upon the truth values of the level inputs at the instant of arrival of the input pulse, and changes in these levels which occur after this instant will not affect the output even though the input pulse may still be present.

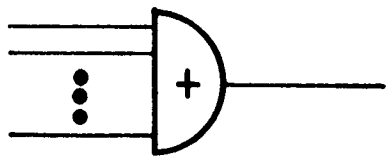
In addition to the various logic gates, use will be made of a pulse delay element. The output will consist of a single pulse emitted after a delay of τ from the time of arrival of the input pulse.

The symbolic representation of the various elements noted above is presented in Figure 5.

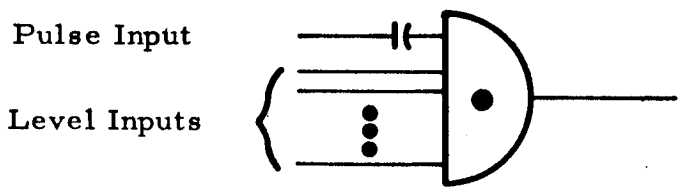
The fact that minimal forms of input gating will be investigated for only one particular set of logical connectives, the AND-OR-NOT system, is not a restriction in the generality of the approach. It has been shown by



AND Gate



OR Gate or PULSE-OR Gate



PULSE-AND Gate

INVERTER DELAY

Figure 5. Symbolic representation of the combinational circuitry.

Earle [5] that "in going from the canonical form of a function using one set of operators, to a minimal form of the function with another set of operators, ... minimizing and then transforming gives the same result as transforming and then minimizing."

Derivation of Input Equations

In the translation of the problem statement into transition map form, "0" and "1" entries are not made on the maps. This convention has been adopted in order that the maps display (in addition to the "-" entries) only those entries which denote a change in state, because it is only the transitions which must be accounted for in the input equations in order that the proper sequence of states result. For minimal forms of input equations, "0" and "1" entries should be made on the maps only when they contribute to the simplification of the input equations.

The relationships illustrated in Figure 3 and the points discussed above form the basis of the rules for the derivation of input equations:

A "0" may be entered in any blank square on the

ZERO half of a map.[1]

A "1" may be entered in any blank square on the ONE half of a map.[2]

A blank square must correspond to an absence of all input pulses.

Every "α" must be taken into account by either a SET pulse ot a TRIGGER pulse or both simultaneously.

Every "β" must be taken into account by either a RESET pulse or a TRIGGER pulse or both simultaneously.

Every "0" must be taken into account by a RESET pulse.

Every "1" must be taken into account by a SET pulse.

Any "-" may be used to simplify any input expression.

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[1]The "ZERO half of a map" is that portion of a transition map for which the initial state of the associated flip-flop is ZERO.

[2]The "ONE half of a map" is the area including those squares for which the associated flip-flop is initially in the ONE state.

As an example of the application of the rules above, consider the transition maps shown in Figure 4. The counter input pulse will be denoted by "p."

On the transition map for flip-flop A, the "α" implies that A must receive either a SET pulse or a TRIGGER pulse or both when a = 0 and b = 1. The "β" implies that either the RESET input or the TRIGGER input or both must be pulsed when a = 1 and b = 1. The simplest input expression satisfying both these requirements is $T_A = b \cdot p$. For this particular case, the "-" entry does not help simplify the input equation.

The pattern of entries on the transition map for flip-flop B is such that a number of alternative input expressions exist. These alternatives and two possible input sets for flip-flop A are illustrated in Figure 6.

One variation of the completed design is shown schematically in Figure 7. The convention will be adopted that flip-flop inputs and outputs which are not used in a design are omitted from the diagram.

As a second example of the application of the synthesis technique, a three bit counter will be designed.

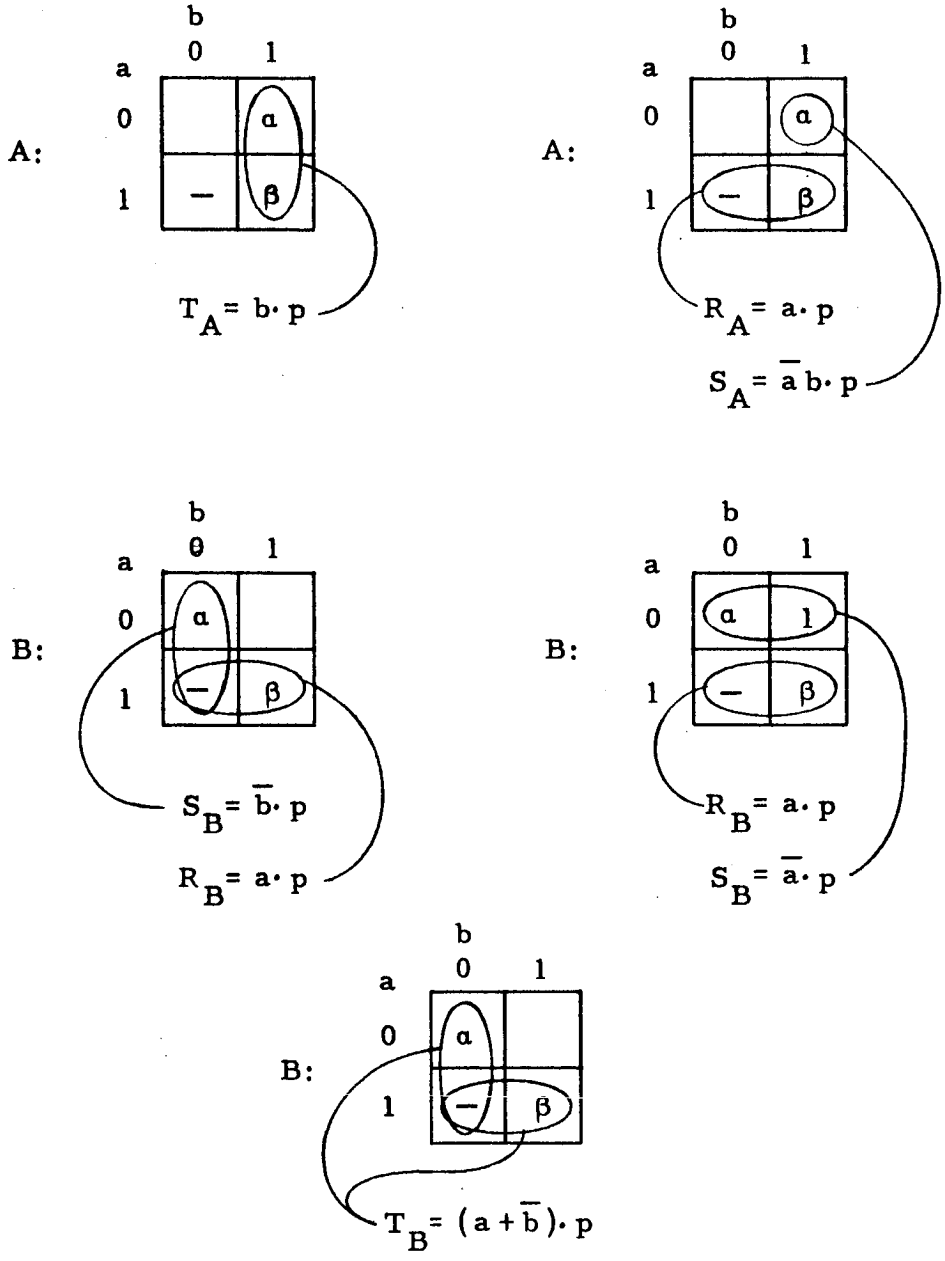

Figure 6. Derivation of some of the possible input expressions for the counter defined in Table 1.

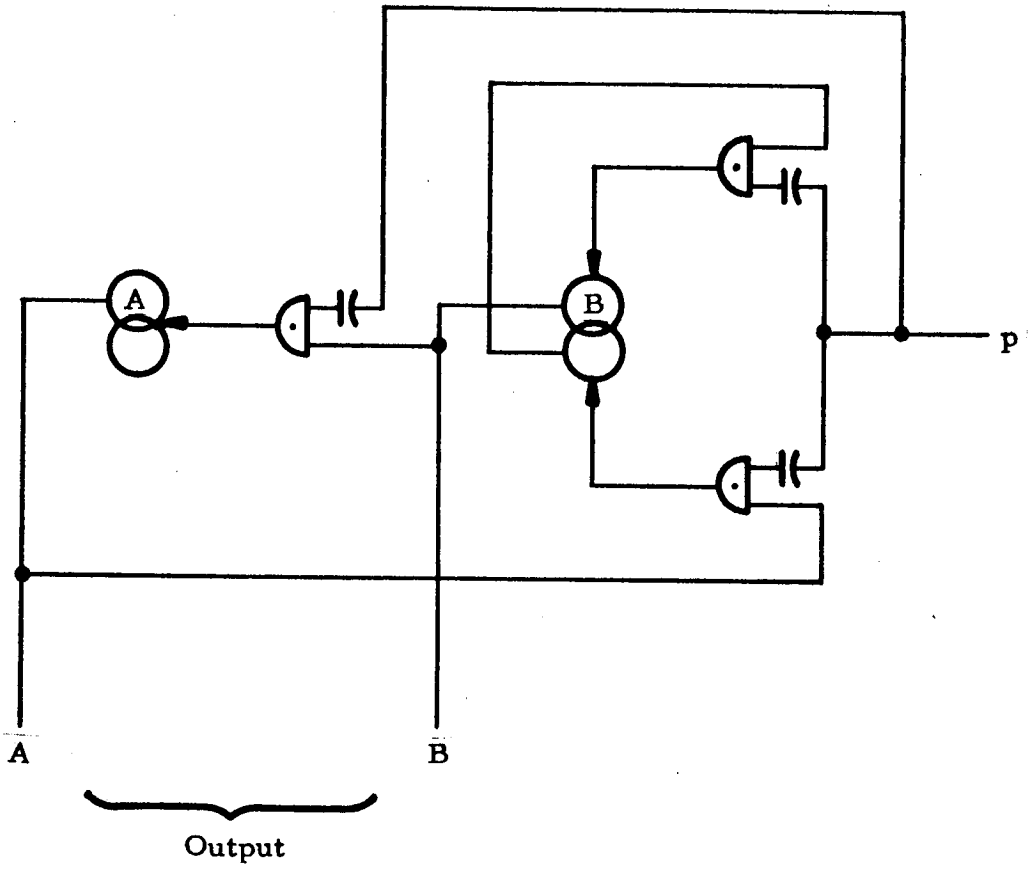

Figure 7. Completed design of the counter defined in Table 1.

$$T_A = b \cdot p \qquad S_B = \overline{b} \cdot p$$

$$R_B = a \cdot p$$

The binary equivalent to the first few terms in the Fibonacci series (see Table 2) will be used as the sequence of counter states.

The desired sequence of states having been specified, the problem statement is translated into transition map form. The result of this translation is shown in Figure 8.

Once the synthesis problem is in transition map form, the input equation derivation rules are applied. The application of these rules is illustrated in Figure 9.

After determining the simplest sets of input equations, the synthesis is complete (see Figure 10).

TABLE 2

BINARY FIBONACCI SERIES
COUNTER

A	B	C
0	0	0
0	0	1
0	1	0
0	1	1
1	0	1
0	0	0

A:

ab \ c	0	1
00		
01		α
11	—	—
10	—	β

B:

ab \ c	0	1
00		α
01		β
11	—	—
10	—	

C:

ab \ c	0	1
00	α	β
01	α	
11	—	—
10	—	β

Figure 8. Result of application of translation rules to sequence of states of the binary Fibonacci series counter.

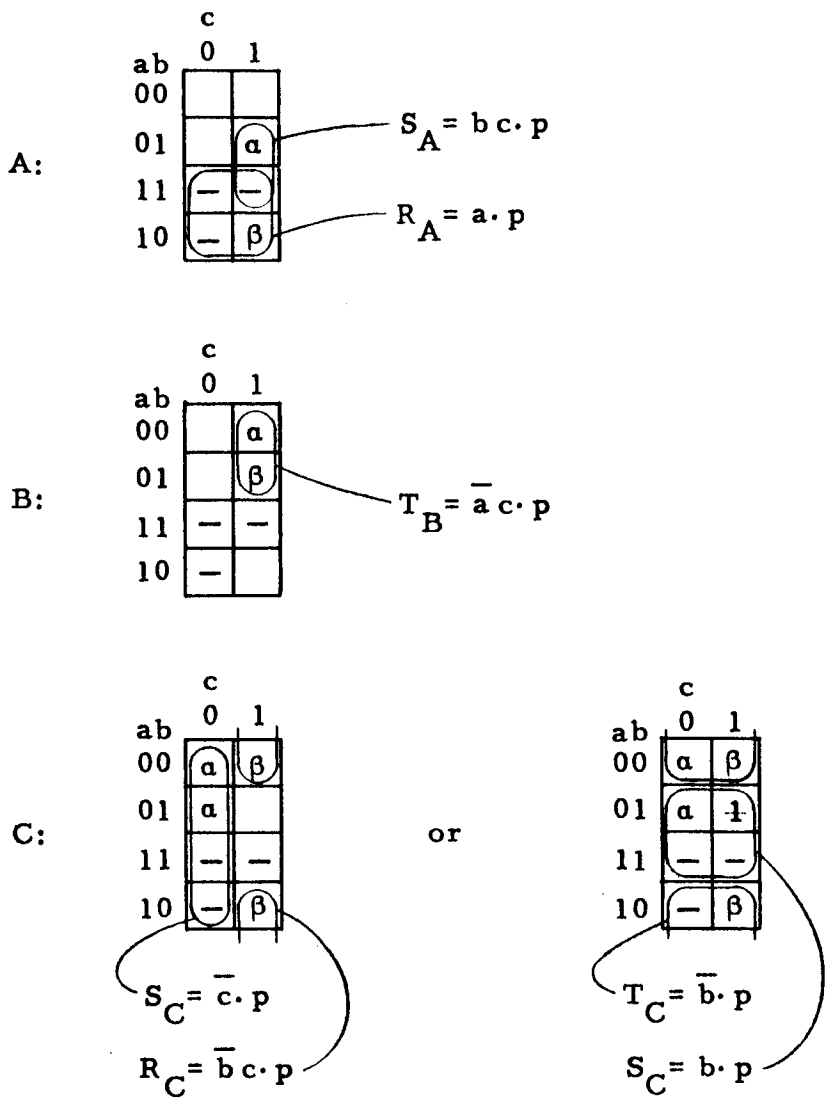

Figure 9. Derivation of input equations for the binary Fibonacci series counter.

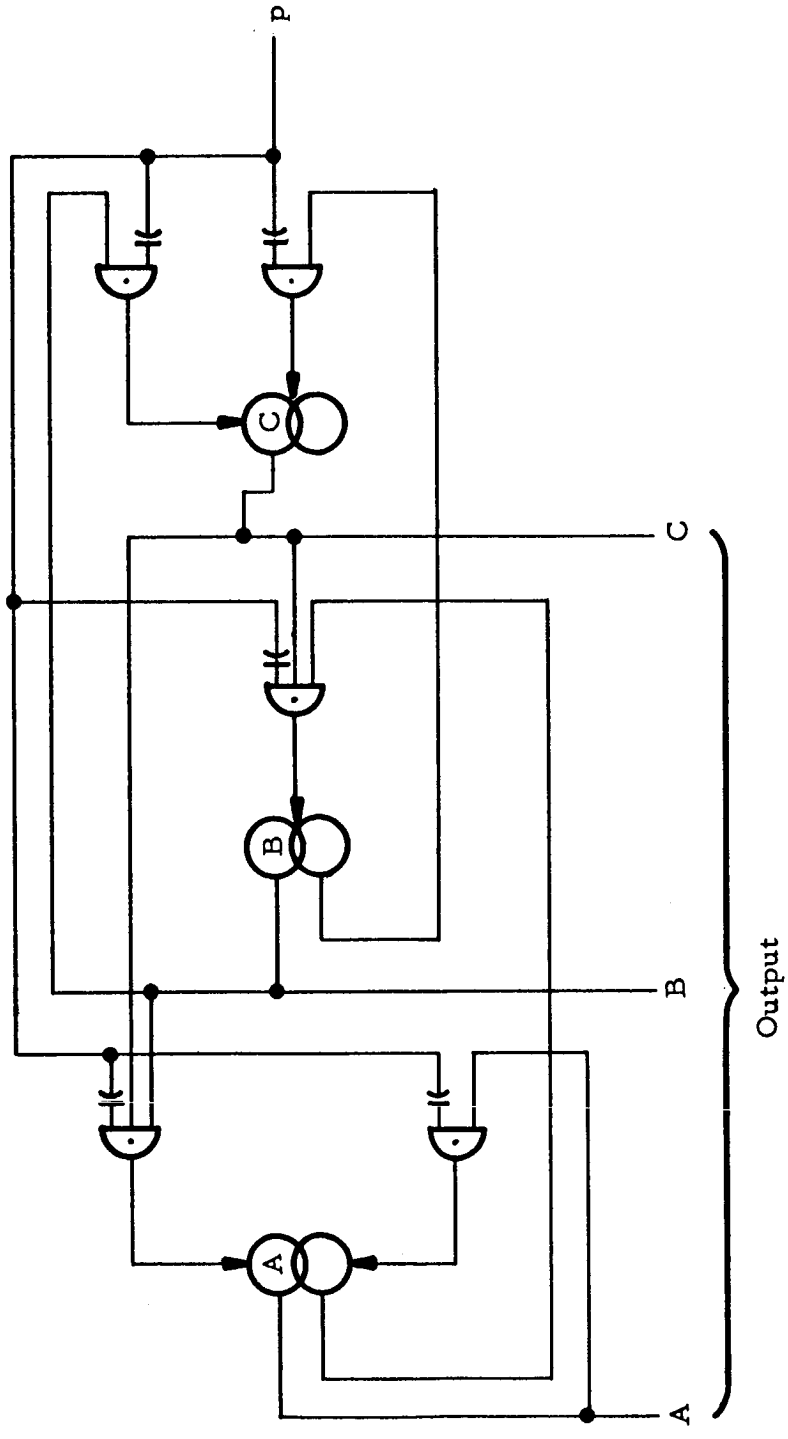

Figure 10. Completed design of the binary Fibonacci series counter.

$R_A = a \cdot p \quad S_A = bc \cdot p \quad T_B = \bar{a}c \cdot p \quad S_C = b \cdot p \quad T_C = \bar{b} \cdot p$

III. THE SYNTHESIS OF ASYNCHRONOUS COUNTERS

Problem Statement and Assumptions

As was done in the previous chapter, it will be assumed that the problem is stated in the form of a sequence of counter states to be implemented. It will also be assumed that the circuitry which is to be connected to the counter output will not be adversely affected by the temporary appearance of unstable states during the transition of the counter from one state in the sequence to the next -- a condition which is a prerequisite for the practicality of an asynchronous counter. A third assumption, which is implied in the following technique, is that the time it takes for a flip-flop to change state is small compared to the length of time between counter input pulses. This condition makes it possible for the counter to go through a number of unstable states between the specified states of the sequence.

In the examples which have been treated up to now and in the problems which are to be presented, the state of the

counter for which all flip-flops are in the ZERO state is arbitrarily taken to be the starting state. This artifice in no way limits the generality of the techniques presented.

Motivation for the Asynchronous Synthesis Procedure

Suppose it is desired to synthesize a three bit counter which will count in the natural binary sequence (see Table 3). The problem is easily solved by using the techniques presented in the preceding chapter: the derivation of the input equations is illustrated in Figure 11, and the synchronous solution is shown schematically in Figure 12.

For the type of counter under consideration -- counters which are intended to execute a specific sequence of states -- the logical action of each flip-flop at the arrival of a counter input depends upon -- and is determined by -- the initial state of the counter. In the counter designed above (and in synchronous counters in general), the internal transmission of information about the state of the counter is achieved by the use of flip-flop output levels. Flip-flop A, for example, must make a transition when the counter is initially in either the 011 or the 111 state. The information

TABLE 3

THREE BIT NATURAL BINARY COUNTER

A	B	C
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1
0	0	0

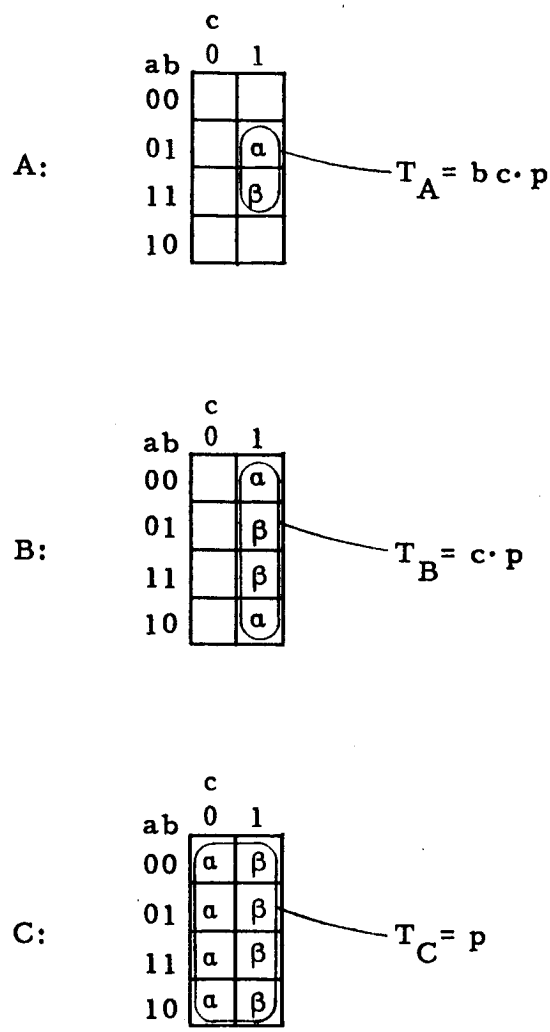

Figure 11. Derivation of input equations for the three bit natural binary counter.

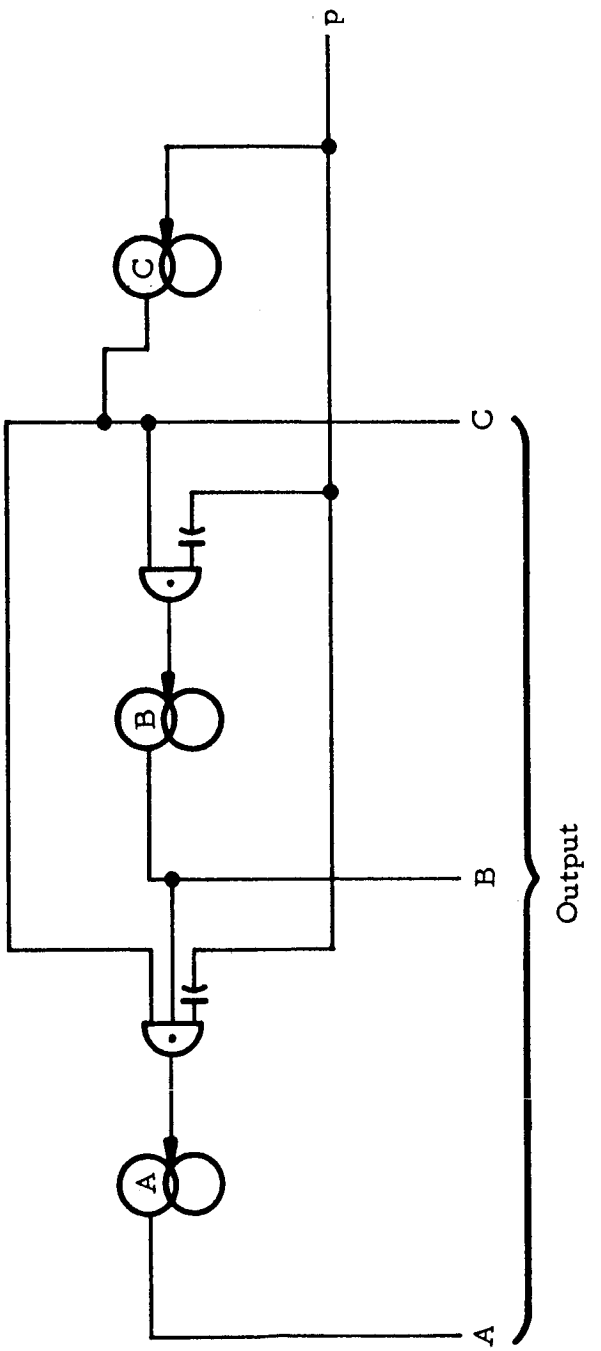

Figure 12. Synchronous three bit natural binary counter.

$T_A = b\,c \cdot p \qquad T_B = c \cdot p \qquad T_C = p$

that the counter is in one of these states is transmitted to the input of flip-flop A by means of the output levels b and c.

In the internal structure of a synchronous counter, the flip-flop output levels serve as sources of information about the state of the counter. An inspection of the transition maps in Figure 11, however, reveals that there is a second source of information available. The transition map for flip-flop C, for example, indicates that C makes a transition for every initial counter state. Thus, $\alpha_C = 1$ indicates that the counter was initially in a state in which $c = 0$; $\beta_C = 1$ conveys the information that the counter was initially in the 001, 011, 101, or 111 state. From the transition map for flip-flop B, it follows that (1) $\alpha_B = 1$ implies that the initial state of the counter was either 001 or 101, (2) $\beta_B = 1$ indicates that the counter was in either the 011 or the 111 state prior to the input pulse. The transition map for flip-flop A shows that the initial counter states 011 and 111 can be uniquely represented by $\alpha_A = 1$ and $\beta_A = 1$, respectively.

There are essential differences between the two sources of information described above. Information pertaining to

the state of the counter is available from the flip-flop output levels prior to the arrival of the counter input pulse. In contrast, the flip-flop transition pulses appear after the arrival of an input signal. In addition to this temporal difference in the information, there is a variance in the total amount of information available from each source. Whereas the set of output levels of all flip-flops is sufficient to distinguish between every state of the counter, the transition pulses are inadequate in this respect. This inadequacy, however, does not always significantly restrict the use of transition pulses, as will be shown in the next paragraph.

The information available at the pulse outputs of the flip-flops is used in the following manner. Consider the transitions enterd on the transition map for flip-flop B in Figure 11. All four of these transitions are entered in squares corresponding to the β transitions of flip-flop C. It follows that if the input equation were $T_B = \beta_C$, flip-flop B would make the desired transitions. Now consider the α and β transitions of flip-flop A. These two transitions are entered in squares corresponding to the two

transitions of flip-flop B. Thus, the β pulses of flip-flop B can be used as the TRIGGER input pulses of flip-flop A. Figure 13 displays the complete design.

In the counter design of Figure 13, flip-flop state transitions are used as information sources and the corresponding transition pulses are employed as the information carriers. This is in contrast to the design of Figure 12, in which flip-flop output levels serve as information sources and gated counter input pulses serve as information carriers. The lack of synchronism in the counter of Figure 13 is the price that is paid for the simplicity of that counter compared to the one in Figure 12. It is this lack of synchronism, caused by the inherent delay at output of each flip-flop, that gives rise to the term "asynchronous."

Consider the scale-of-six counter defined by Table 4. The transition maps for this counter (see Figure 14) closely resemble those for the three bit natural binary counter (see Figure 11). It is therefore natural to investigate the possibility of finding input equations similar to those which resulted in the simple design of Figure 13.

Examine the map for flip-flop Z in Figure 14. According

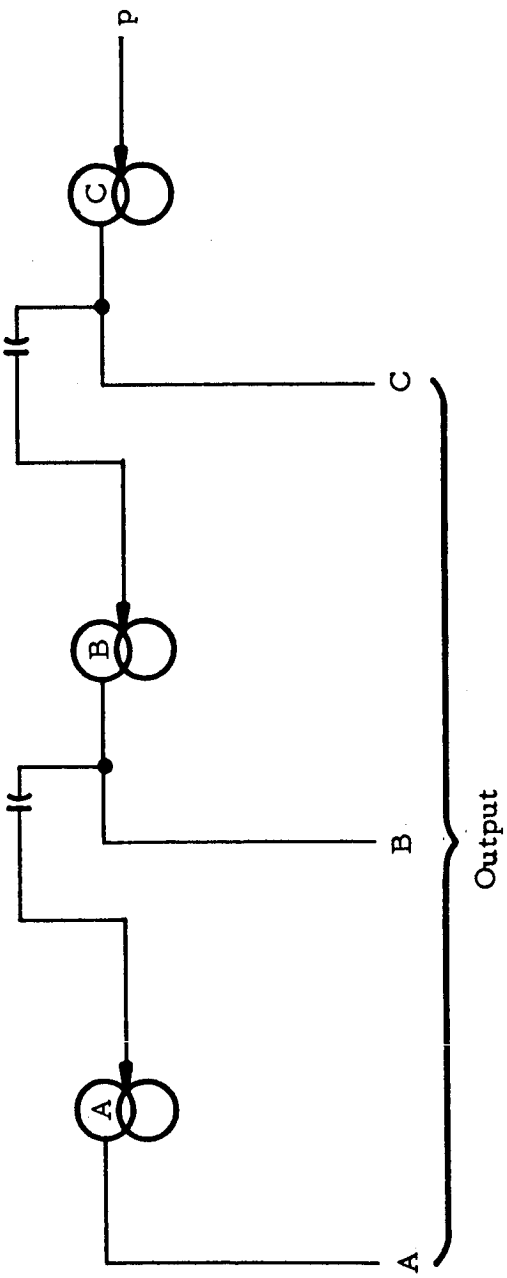

Figure 13. Asynchronous three bit natural binary counter.

$T_A = \beta_B \quad T_B = \beta_C \quad T_C = p$

TABLE 4

SCALE-OF-SIX
COUNTER

X	Y	Z
0	0	0
0	0	1
0	1	0
0	1	1
1	1	0
1	1	1
0	0	0

X:

xy \ z	0	1
00		
01		α
11		β
10	—	—

Y:

xy \ z	0	1
00		α
01		
11		β
10	—	—

Z:

xy \ z	0	1
00	α	β
01	α	β
11	α	β
10	—	—

Figure 14. Transition maps for scale-of-six counter.

to the rules for the derivation of input equations, the "-" entries may be used to simplify the input equation. Thus, the simplest input expression for Z is $T_Z = p$.

Now compare the map for flip-flop Y with the map for flip-flop Z. If there were a "β" in the 011 square of the map for Y, then the β transition pulses of Z could be used as the TRIGGER input signal for Y. Moreover, an examination of the map for X reveals that if this additional β transition were present on the map for Y, then the β pulses from Y could be used as the TRIGGER input pulses for X. The conclusion is that it is very desirable (from the standpoint of achieving a simple counter) for flip-flop Y to make a β transition when the counter is initially in the 011 state. If the counter is to execute the sequence of states defined by Table 4, however, the effect of any such additional β transition must be compensated for by an additional α transition immediately following it. Clearly, any gain in simplicity achieved by the expedient of adding a β transition must therefore be weighed against the loss caused by having to account for the additional α transition.

There are two possible ways in which the additional α

transition may be taken into account. First, the counter input pulses which arrives when the counter is in the 011 state may be delayed and then applied to the SET input of flip-flop Y after the β transition is completed. This scheme would require a PULSE-AND gate with three level inputs and a DELAY element. Second, the transition maps may be examined in an attempt to find a transition pulse to the SET input of Y. This approach would require only a DELAY element, provided such a transition pulse could be found. Carrying out the examination reveals that the required transition pulse does indeed exist; it is α_X.

Having ascertained that the additional α transition of flip-flop Y can be easily taken into account, proceed with the design of the scale-of-six counter by adding a "β" to the 011 square of the map for Y (see Figure 15). A second map, drawn to the right of the first, may be employed to enter the compensating α transition. The derivation of input equations is illustrated in Figure 15, and the counter design is shown schematically in Figure 16.

The completed scale-of-six counter is an example of the degree of simplicity which may sometimes be achieved through

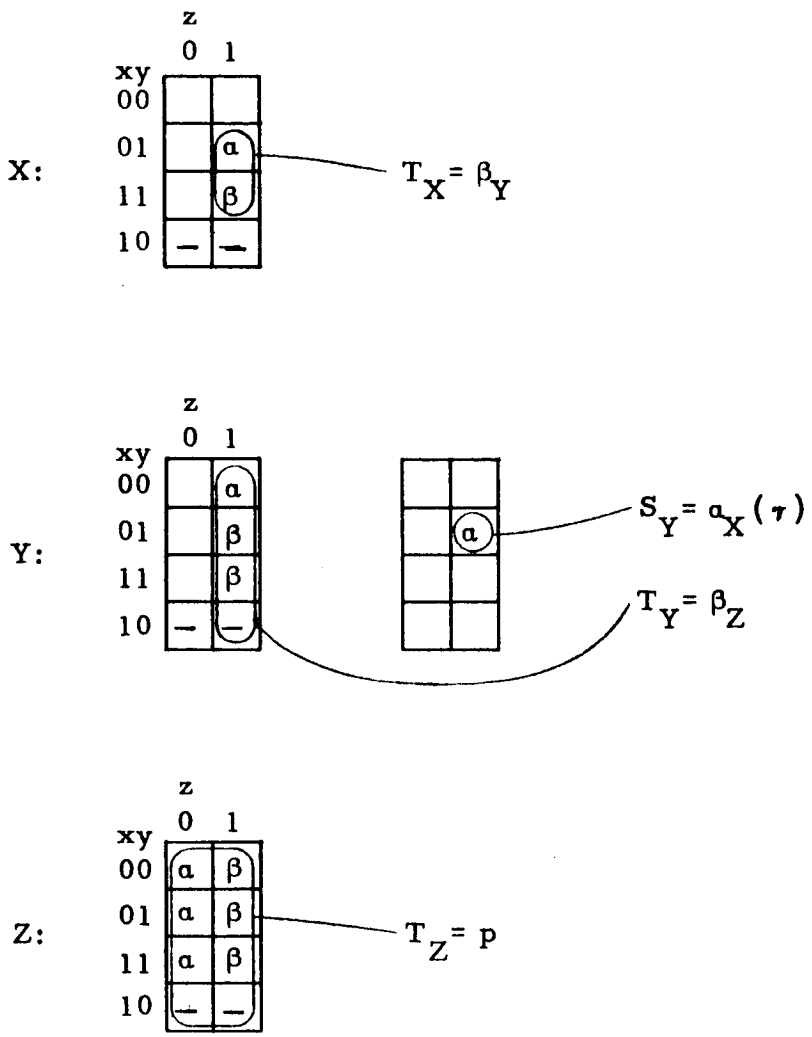

Figure 15. Derivation of input equations for scale-of-six counter with feedback.

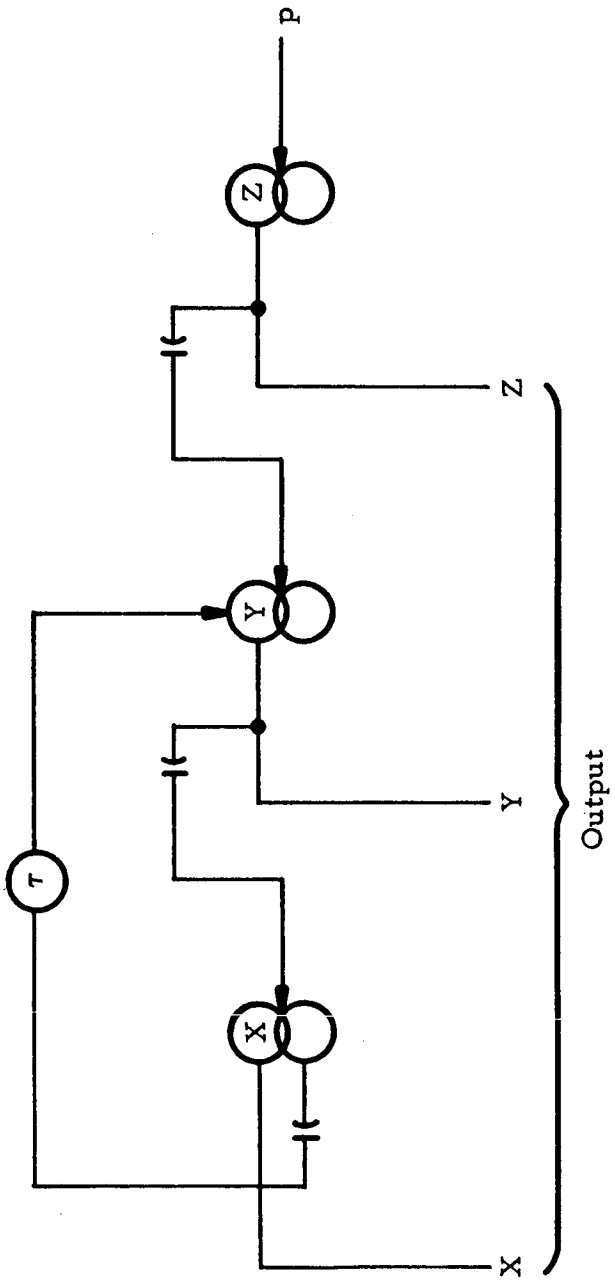

Figure 16. Asynchronous scale-of-six counter employing feedback.

$T_X = \beta_Y \quad S_Y = \alpha_X(\tau) \quad T_Z = p$

$T_Y = \beta_Z$

the use of asynchronous and feedback techniques.

The Asynchronous Synthesis Procedure

In order to be able to precisely describe the operation and design of asynchronous counters in a concise manner, it is necessary to introduce some additional notation and terminology.

A set of transition maps arranged as shown in Figure 17 will be called a "map array." The particular map array shown is for a three bit counter with flip-flops A, B, and C. The column of maps on the extreme left is labelled in the conventional manner and is used for the translation of the counter state sequence table in the previously defined manner.

The circled numeral below each map in Figure 17 will be called the "time index."

Transitions entered on the map array will be classified into four types:

Essential transition: a change of state which is required by the counter state sequence table.

Expedient transition: a change of state which is

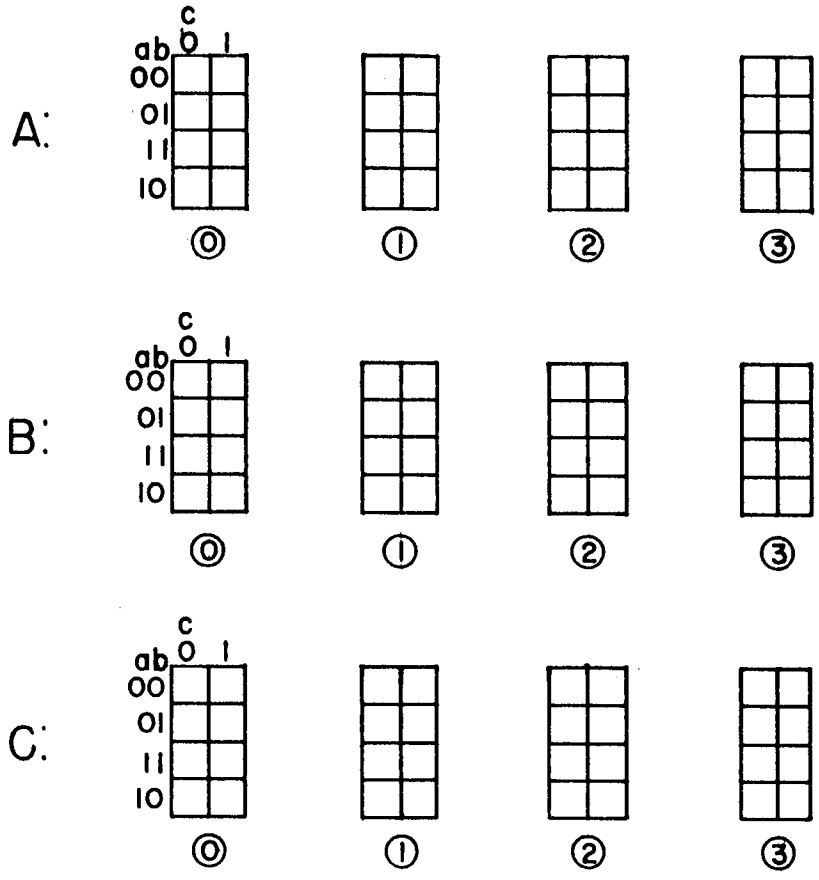

Figure 17. A map array
for a three bit counter with flip-flops A, B, and C.

employed in order to simplify an input equation.

Side-effect transition: an undesired change of state which occurs as a result of the particular expedient and feedback transition scheme used.

Feedback transition: a change of state which is used to cancel the effect of an expedient or side-effect transition.

The procedure for synthesizing an asynchronous counter from a counter state sequence table consists of the following steps:

1. Translate the counter state sequence table onto the maps of time index 0 on a map array.
2. Examine each transition map to determine which transitions to produce by means of the counter input pulse and which to produce by means of the output pulses of other flip-flops.
3. Consider the transitions which are to be produced by the counter input pulse.
   a. Add expedient transitions where profitable.
   b. For each expedient transition added, enter a corresponding feedback transition on the map

of time index 1 in the same row.

c. Derive input equations for the essential and expedient transitions under consideration.

d. Place a dot in the lower left corner of each square containing a transition which has been taken into account.

4. Consider the essential transitions which are to be produced by the output pulses of other flip-flops.

a. Remove each of these transitions from its position at time index 0, and re-enter it in the corresponding square on the map in the same row at time index one greater than the output pulse which is to produce it.

b. Add expedient transitions where profitable.

c. For each expedient transition added, enter a corresponding feedback transition on the map of time index one greater in the same row.

d. Derive input equations for the essential and expedient transitions under consideration.

e. Place a dot in the lower left corner of each sqaure containing a transition which has been

taken into account.

5. Consider the feedback transitions which do not have dots in the lower left corners of their squares.

   a. If any feedback transition does not have a time index at least one greater than the pulse which is to produce it, remove it and re-enter it in the corresponding square on the map in the same row at time index one greater than the pulse which is to produce it.

   b. Add expedient transitions where profitable.

   c. For each expedient transition added, enter a corresponding feedback transition on the map of lowest time index greater than both the expedient transition and the pulse which is to produce the feedback transition.

   d. Derive input equations for all transitions which do not have dots in the lower left corners of their squares.

   e. Place a dot in the lower left corner of each square containing a transition which has been

taken into account.

6. For each transition which has a dot in the lower left corner of its square:
   a. Place a dot in the lower right corner of its square.
   b. Check all input equations to determine if the transition will cause any flip-flop to receive an input pulse which has not been entered.
   c. For each such input pulse:
      i. Make the corresponding entry on the map which is located in the row for the flip-flop which receives the pulse and has a time index one greater than the transition which causes it.
      ii. If the corresponding entry is a transition, place a dot in the lower left corner of its square.
      iii. If the corresponding entry is a transition, enter a feedback transition on the map of time index one greater in the same row.
7. If there are any squares which contain transitions

but do not have dots in both lower corners, then erase all the dots in the lower right corners and repeat steps 5 and 6. The procedure terminates when either (1) all squares containing transitions have dots in both lower corners, in which case the design is complete; or (2) the particular input equation scheme being pursued is found to be unusable, in which case the procedure must be restarted and a different equation scheme employed.

Step 7 of the synthesis procedure requires that the procedure be terminated when the input equation scheme being persued is found to be unusable. An input equation scheme -- that is, the plan of the equations derived in steps 3 and 4 -- is unusable if after a number of iterations of steps 5 and 6, the number of side-effect transitions being generated does not decrease. This condition will result, for example, when an unstable loop has been created.

Asynchronous Input Equation Requirements

When the asynchronous synthesis procedure is employed,

the input equations must satisfy the following requirements:

1. Every input equation must include either the counter input pulse or a flip-flop output pulse.
2. If a flip-flop output pulse is used to account for a map entry in the input equations, the transition which causes the pulse must be located in the corresponding square on a map of time index less than that of the entry.
3. If an input equation implies the use of a PULSE-AND gate, the flip-flops whose output levels are used as the level inputs to the gate must not change state prior to the arrival of the pulse input to the gate.
4. If, for a given initial state of the counter, a flip-flop receives more than one input pulse, each input pulse must have a minimum delay of τ[1] with respect to the preceding pulse.

In the asynchronous synthesis procedure, the counter state sequence table is first translated onto the map array.

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[1] τ is the maximum length of time which must elapse between two successive input pulses in order for reliable operation to result.

The procedure and the input equation requirements then make use of the correspondences between the entries on the map array in order to derive the input equations. It is shown in the Appendix that permutations of the digit positions need not be investigated during the search for a simple counter design.

IV. APPLICATION OF THE SYNTHESIS PROCEDURE

As a demonstration of the synthesis procedure, the duodecimal counter defined in Table 5 will be designed. The R-S-T flip-flop will be used.

In order to obtain a design which requires a minimum amount of logical gating, the synthesis procedure will be applied a number of times. First the procedure will be used to arrive at a design which does not employ expedient and feedback transitions. This design will be used as a basis of evaluation for more sophisticated designs employing feedback.

1. Translate the counter state sequence table onto the maps of time index 0 on a map array.

Step 1 is carried out by applying the translation rules to Table 5. The result is shown in Figure 18.

2. Examine each transition map to determine which transitions to produce by means of the counter input pulse and which to produce by means of the output pulses of other flip-flops.

TABLE 5

DUODECIMAL COUNTER

A	B	C	D
0	0	0	0
0	0	0	1
0	0	1	0
0	1	1	0
0	1	1	1
0	1	0	0
1	0	0	0
1	0	0	1
1	0	1	0
1	1	1	0
1	1	1	1
1	1	0	0
0	0	0	0

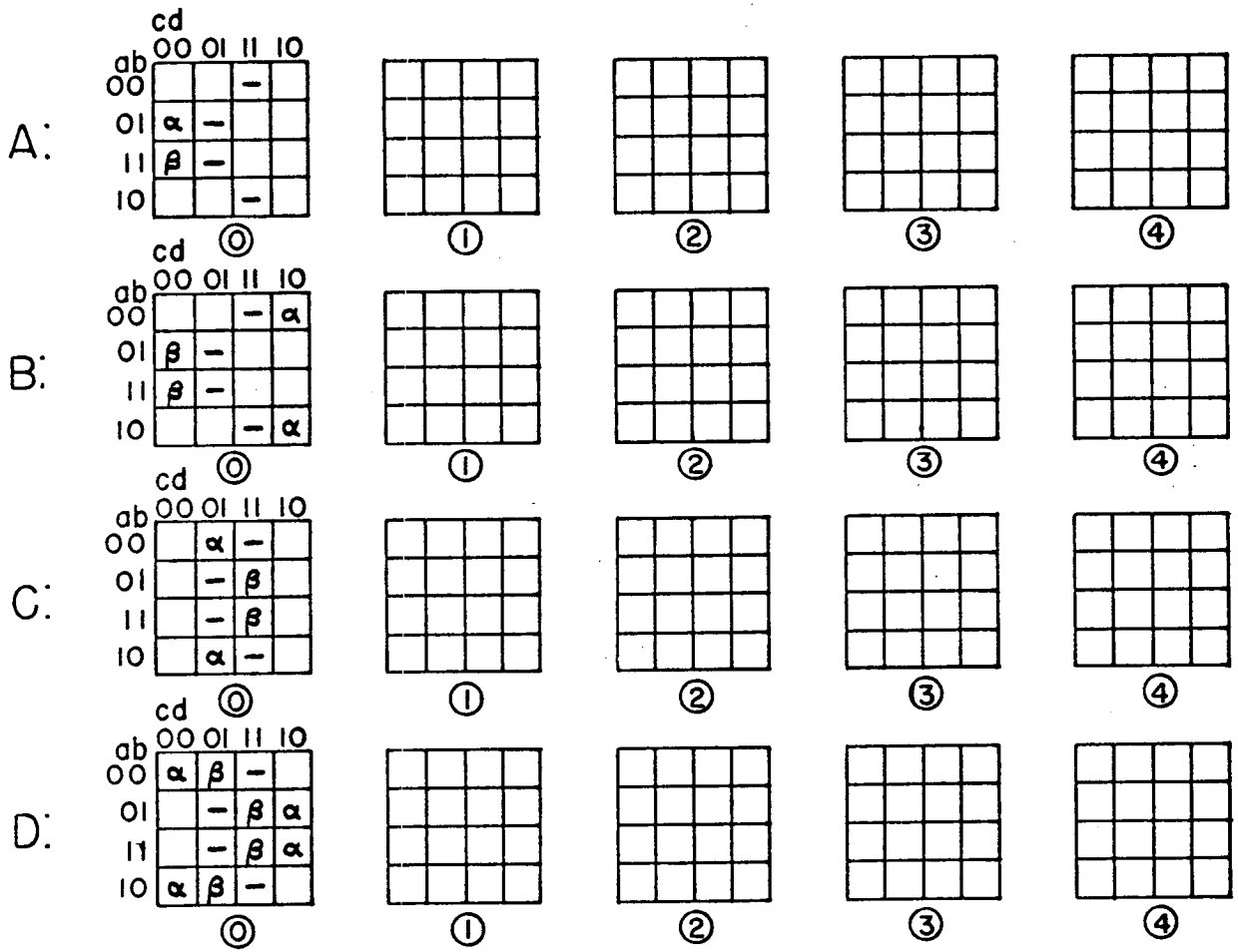

Figure 18. Result of step 1 in the design of the duodecimal counter.

The map for flip-flop A at time index 0 indicates that A makes a transition when the counter is initially in either the 0100 or 1100 state. The map for flip-flop B shows that B makes β transitions for both of these initial counter states. Thus, if the β pulses from B are used as the TRIGGER input signal for flip-flop A, A will make a transition when the counter is initially in the 0100 or 1100 state, as required.

The four transitions on the map for flip-flop B are entered in squares for which neither the map for C nor the map for D contain entries. The counter input pulse will be used to take these transitions into account.

Examination of the map for flip-flop C at time index 0 discloses that C makes a transition when the counter is initially in the 0001, 0111, 1111, or 1001 state. The transition map for D shows that flip-flop D makes a β transition each time the counter is initially in one of these states. The transitions of flip-flop C can be produced, therefore, by using the β pulses from flip-flop D as TRIGGER pulses for C.

The counter input pulse will be used to cause the transitions of flip-flop D.

3. Consider the transitions which are to be produced by the counter input pulse.
   a. Add expedient transitions where profitable.
   b. For each expedient transition added, enter a corresponding feedback transition on the map of time index 1 in the same row.
   c. Derive input equations for the essential and expedient transitions under consideration.
   d. Place a dot in the lower left corner of each square containing a transition which has been taken into account.

The transitions on the maps for flip-flop B and D will be produced by means of the counter input pulse. No expedient transitions will be used. The input equation for flip-flop D is $T_D = (\bar{b}\bar{c} + bc)\cdot p$. The input equation for flip-flop B could be either $T_B = \overline{(\bar{b}\bar{c} + bc)}\cdot p$ or $R_B = \bar{c}\cdot p$, $S_B = c\cdot p$. The latter is chosen arbitrarily. The result of step 3 is shown in Figure 19.

4. Consider the essential transitions which are to be produced by the output pulses of other flip-flops.
   a. Remove each of these transitions from its

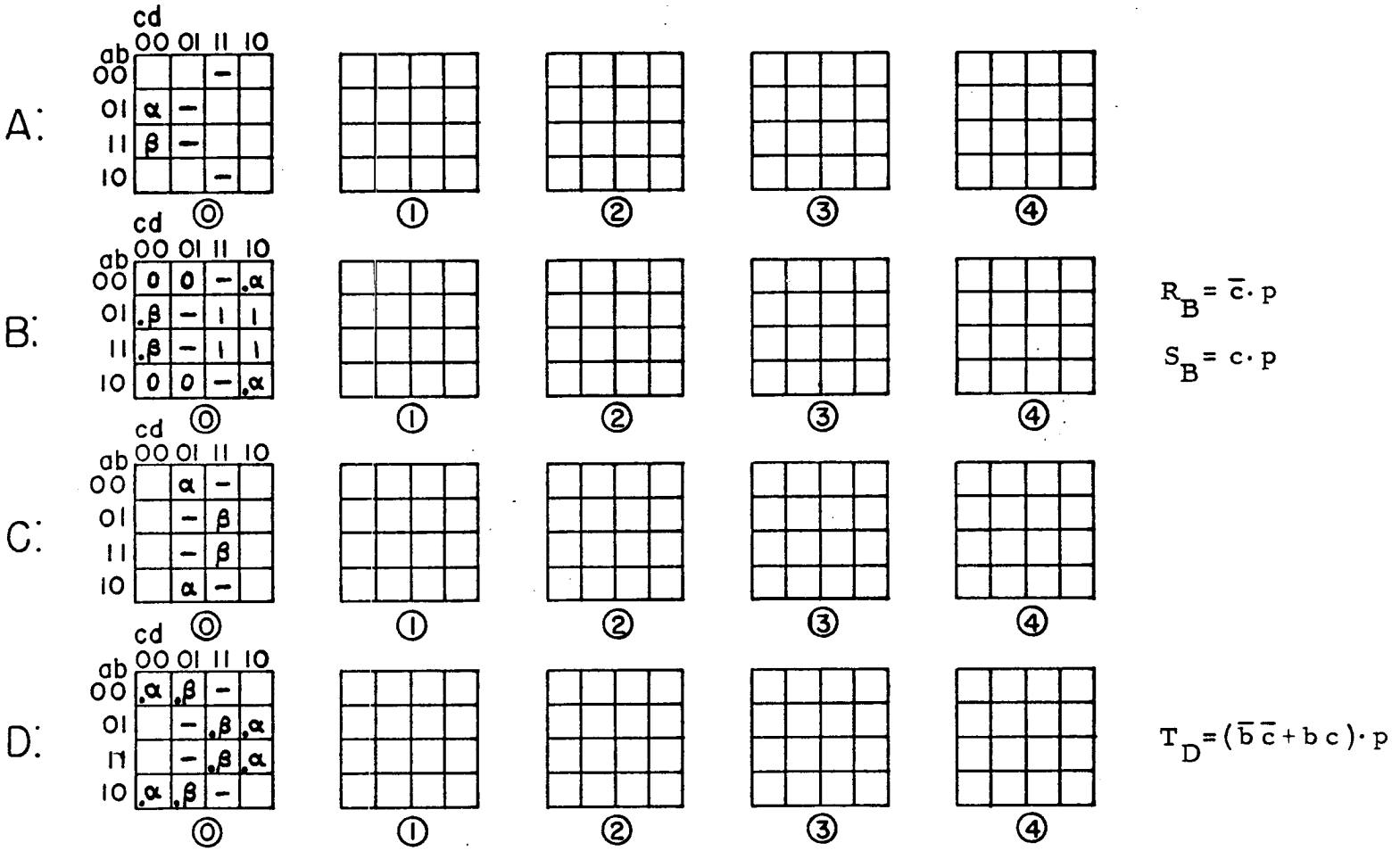

Figure 19. Result of step 3 in the first design of the duodecimal counter.

position at time index 0, and re-enter it in the corresponding square on the map in the same row at time index one greater than the output pulse which is to produce it.

b. Add expedient transitions where profitable.

c. For each expedient transition added, enter a corresponding feedback transition on the map of time index one greater in the same row.

d. Derive input equations for the essential and expedient transitions under consideration.

e. Place a dot in the lower left corner of each square containing a transition which has been taken into account.

The transitions of flip-flop A are to be produced by β pulses from flip-flop B. Since the β transitions of B which cause these pulses are located at time index 0, the transitions of A must be moved to the map for A at time index 1. The transitions for flip-flop C will be produced as a result of the β transitions of D at time index 0 and must therefore be moved to time index 1. Because the transitions of flip-flop A are entered in squares which correspond exactly to the squares

in which the β transitions of B are entered, and because the transitions of C are located in squares which exactly correspond to the squares of the map for flip-flop D which contain β transitions, no expedient transitions are needed to simplify the input equations for A and C. The input equations are $T_A = \beta_B$ and $T_C = \beta_D$. Figure 20 shows the result of step 4.

Step 5 of the synthesis procedure deals with feedback transitions. Since there are none in this design, step 5 is not applicable.

6. For each transition which has a dot in the lower left corner of its square:

   a. Place a dot in the lower right corner of its square.

   b. Check all input equations to determine if the transition will cause any flip-flop to receive an input pulse which has not been entered.

   c. For each such input pulse:

      i. Make the corresponding entry on the map which is located in the row for the flip-flop which receives the pulse and has a time index one greater than the transition

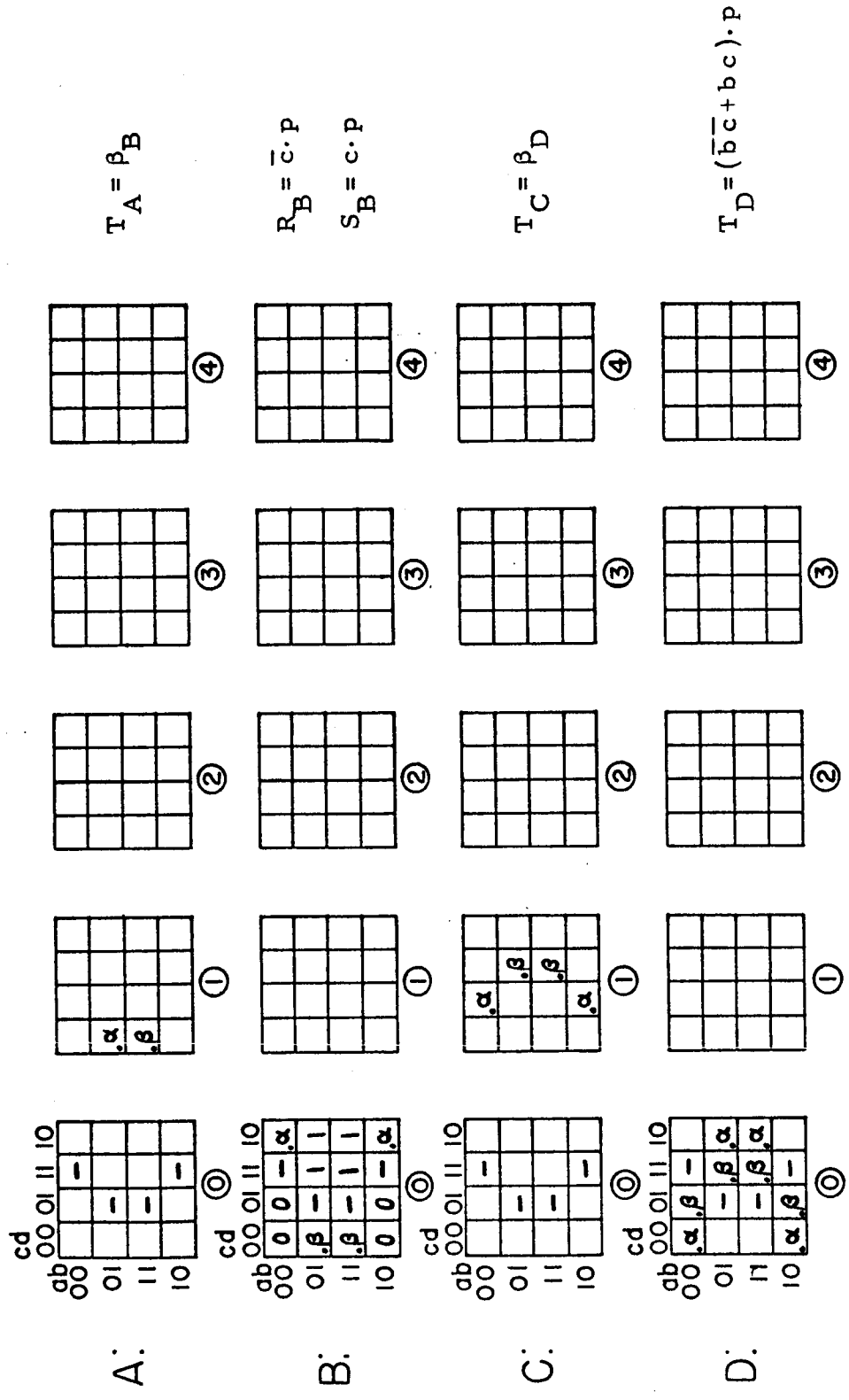

Figure 20. Result of step 4 in the first design of the duodecimal counter.

which causes it.

ii. If the corresponding entry is a transition, place a dot in the lower left corner of its square.

iii. If the corresponding entry is a transition, enter a feedback transition on the map of time index one greater in the same row.

A check of each transition against all of the input equations reveals that there are no input pulses which have not been entered. The result of step 6 is shown in Figure 21.

7. If there are any squares which contain transitions but do not have dots in both lower corners, then erase all the dots in the lower right corners and repeat steps 5 and 6. The procedure terminates when either (1) all squares containing transitions have dots in both lower corners, in which case the design is complete . . .

An examination of the map array in Figure 21 reveals that all squares containing transitions have dots in both lower corners. A dot in the lower left corner of a square containing a transition indicates that the transition has

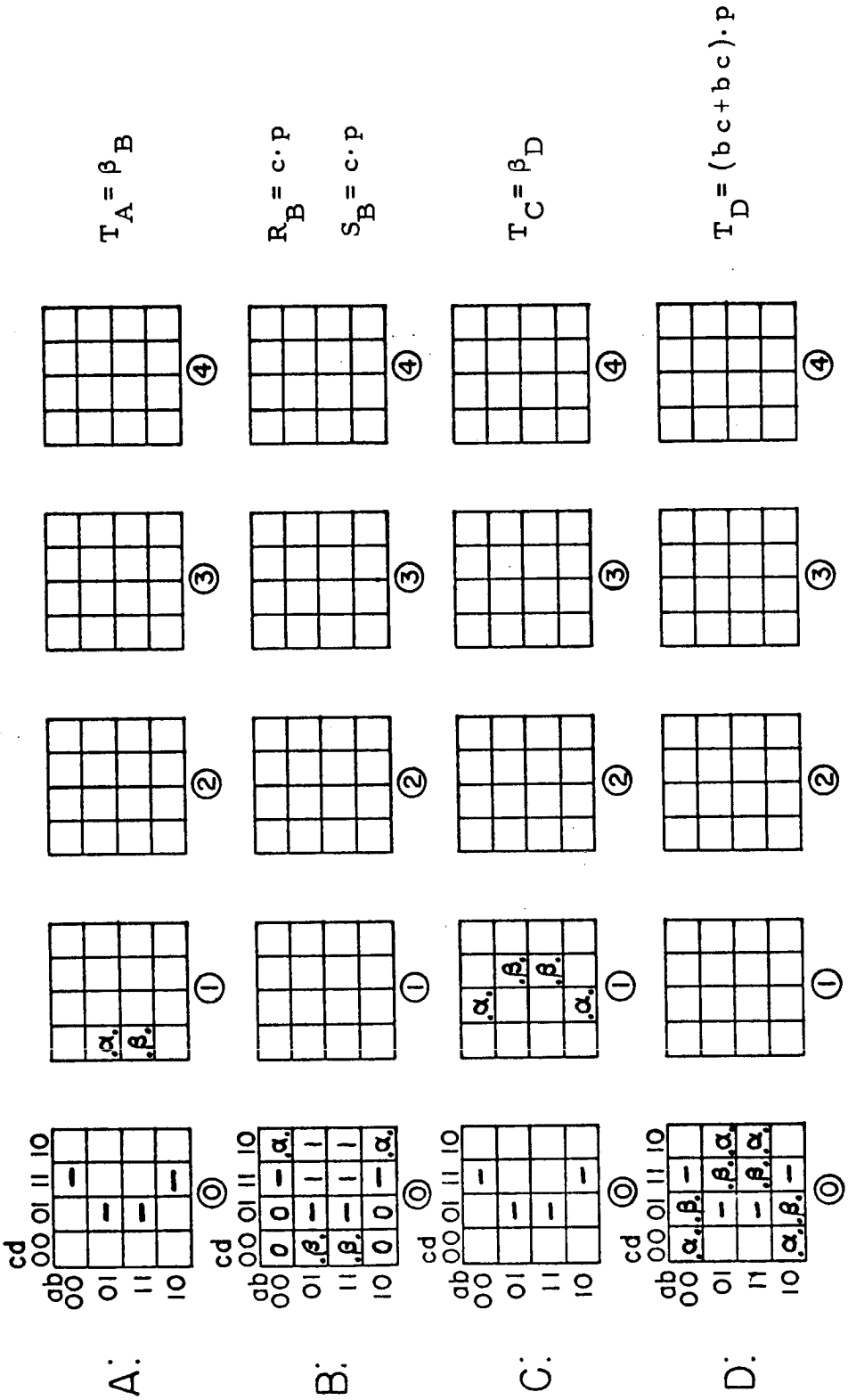

Figure 21. Result of step 6 in the first design of the duodecimal counter.

been taken into account in the input equations. A dot in the lower right corner indicates that the transition has been checked against all input equations and that all input pulses which the transition causes have been entered on the map array. Thus, the fact that all squares containing transitions have dots in both lower corners means that the map array presents an accurate account of the action of all flip-flops. The design is therefore complete; the counter is shown in Figure 22.

The synthesis procedure will now be employed a second time in an effort to minimize the amount of gating needed.

1. Translate the counter state sequence table onto the maps of time index 0 on a map array.

The result of step 1 is the same as for the first design, shown in Figure 18.

2. Examine each transition map to determine which transitions to produce by means of the counter input pulse and which to produce by means of the output pulses of other flip-flops.

It is desirable to produce the transitions of flip-flop A by means of the β transition pulses of flip-flop B, and the

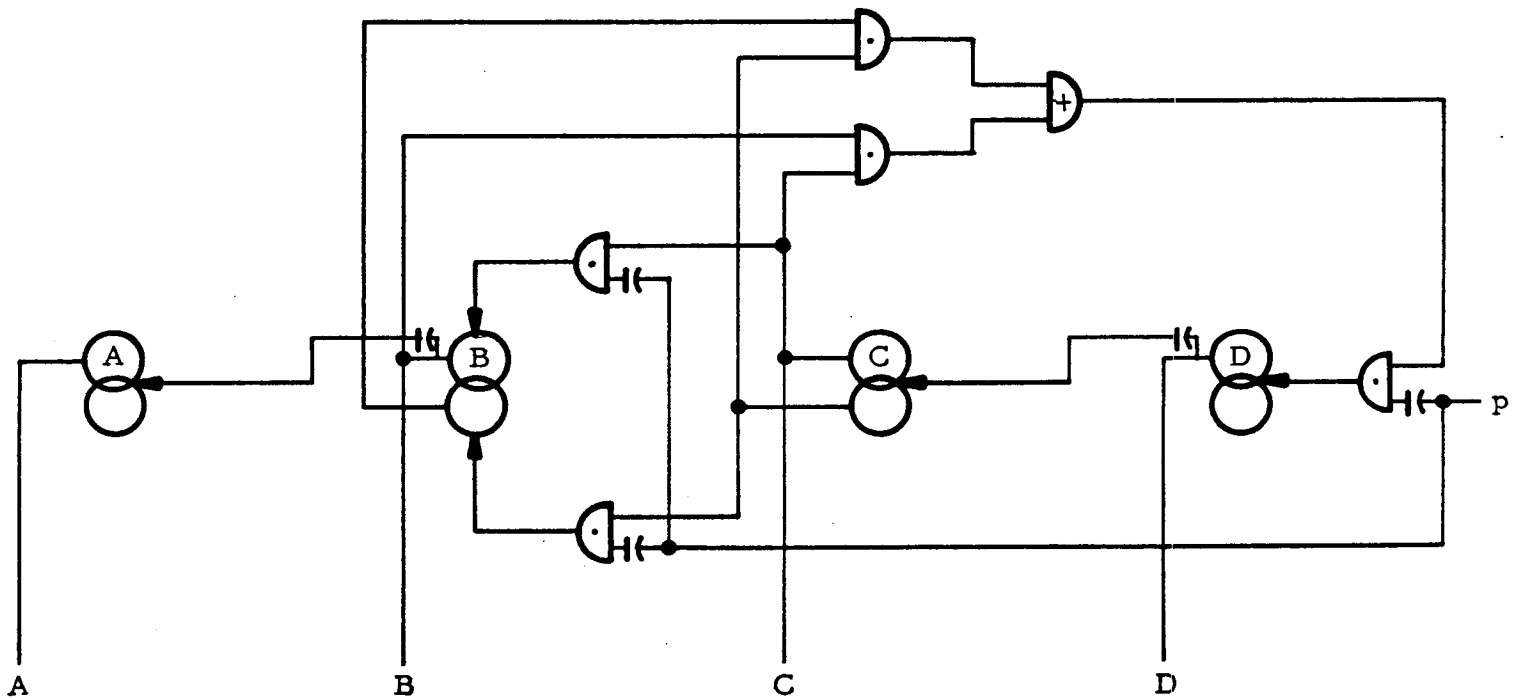

Figure 22. First design of the duodecimal counter.

transitions of C by the β pulses of D, as was done in the first design, since this scheme does not require logical gating.

The four blank squares on the map for flip-flop D at time index 0 represent states of the counter for which D is initially in the ZERO state and remains in the ZERO state. If instead of this action, flip-flop D were to make α transitions for these four initial counter states, the map for D shows that D would make transitions for every state in the counter state sequence table. In this circumstance, the transition of flip-flop D could be produced by using the counter input pulse as the TRIGGER input signal for D. No logical gating would be necessary.

If expedient α transitions were added to the blank squares on the map for D at time index 0, the α transitions of flip-flop B could be produced by using the α pulses of D which occur when c = 1 as the SET input signal to B. The β transitions of flip-flop B could be taken into account by using the α pulses of D which occur when c = 0 as the RESET input pulses to B.

3. Consider the transitions which are to be produced

by the counter input pulse.

a. Add expedient transitions where profitable.

b. For each expedient transition added, enter a corresponding feedback transition on the map of time index 1 in the same row.

c. Derive input equations for the essential and expedient transitions under consideration.

d. Place a dot in the lower left corner of each square containing a transition which has been taken into account.

The essential transitions of flip-flop D are to be produced by means of the counter input pulse. Four expedient α transitions will be entered in the blank squares on the map for D at time index 0. In order to cancel the effect of these α transitions, four feedback β transitions must be entered in the corresponding squares on the map for D at time index 1. The essential and expedient transitions of flip-flop D will be taken into account by means of the counter input pulse -- $T_D = p$. Figure 23 shows the result of step 3.

4. Consider the essential transitions which are to be

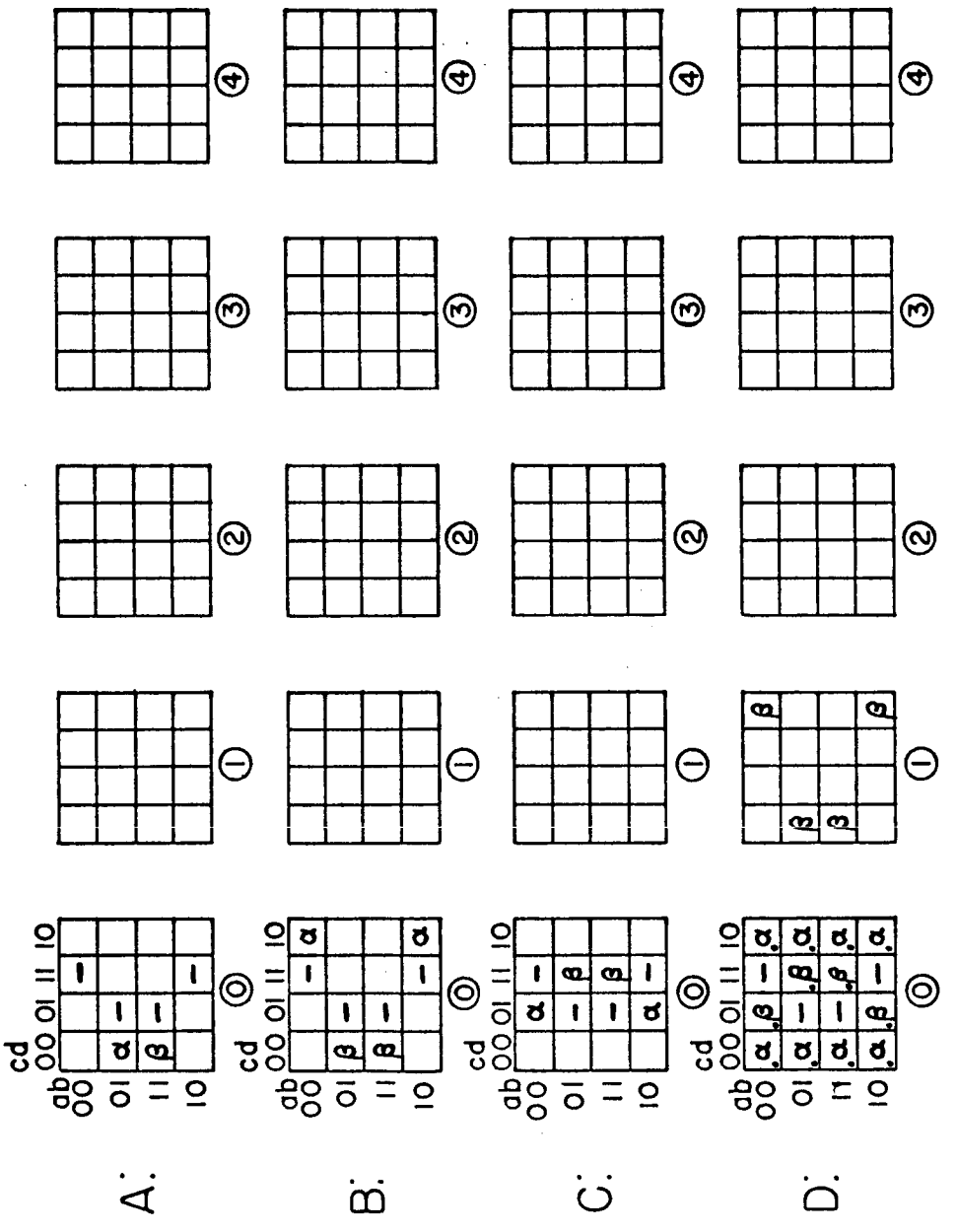

Figure 23. Result of step 3 in the second design of the duodecimal counter.

produced by the output pulses of other flip-flops.

a. Remove each of these transitions from its position at time index 0, and re-enter it in the corresponding square on the map in the same row at time index one greater than the output pulse which is to produce it.

b. Add expedient transitions where profitable.

c. For each expedient transition added, enter a corresponding feedback transition on the map of time index one greater in the same row.

d. Derive input equations for the essential and expedient transitions under consideration.

e. Place a dot in the lower left corner of each square containing a transition which has been taken into account.

The essential transitions of flip-flops A, B, and C will be produced by the output pulses of flip-flops. The four transitions of flip-flop C will be produced by the β pulses from D at time index 0 and must therefore be moved to time index 1. The α pulses of flip-flop D at time index 0 will be used to cause the four transitions of B; thus, the

latter have to be moved to time index 1. The two transitions of flip-flop A will be produced by means of the β pulses of B, which have been moved to time index 1; accordingly, they must be placed at time index 2. No expedient transitions will be used. The input equations for flip-flops A, B, and C are $T_A = \beta_B$; $S_B = c \cdot \alpha_D$, $R_B = \bar{c} \cdot \alpha_D$; and $T_C = \beta_C$. Figure 24 shows the result of step 4.

Because flip-flop C does not change state for those initial states of the counter for which flip-flop D makes α transitions, asynchronous input equation requirement 3 is satisfied in the case of $S_B = c \cdot \alpha_D$ and $R_B = \bar{c} \cdot \alpha_D$.

5. Consider the feedback transitions which do not have dots in the lower left corners of their squares.
   a. If any feedback transition does not have a time index at least one greater than the pulse which is to produce it, remove it and re-enter it in the corresponding square on the map in the same row at time index one greater than the pulse which is to produce it.
   b. Add expedient transitions where profitable.
   c. For each expedient transition added, enter a

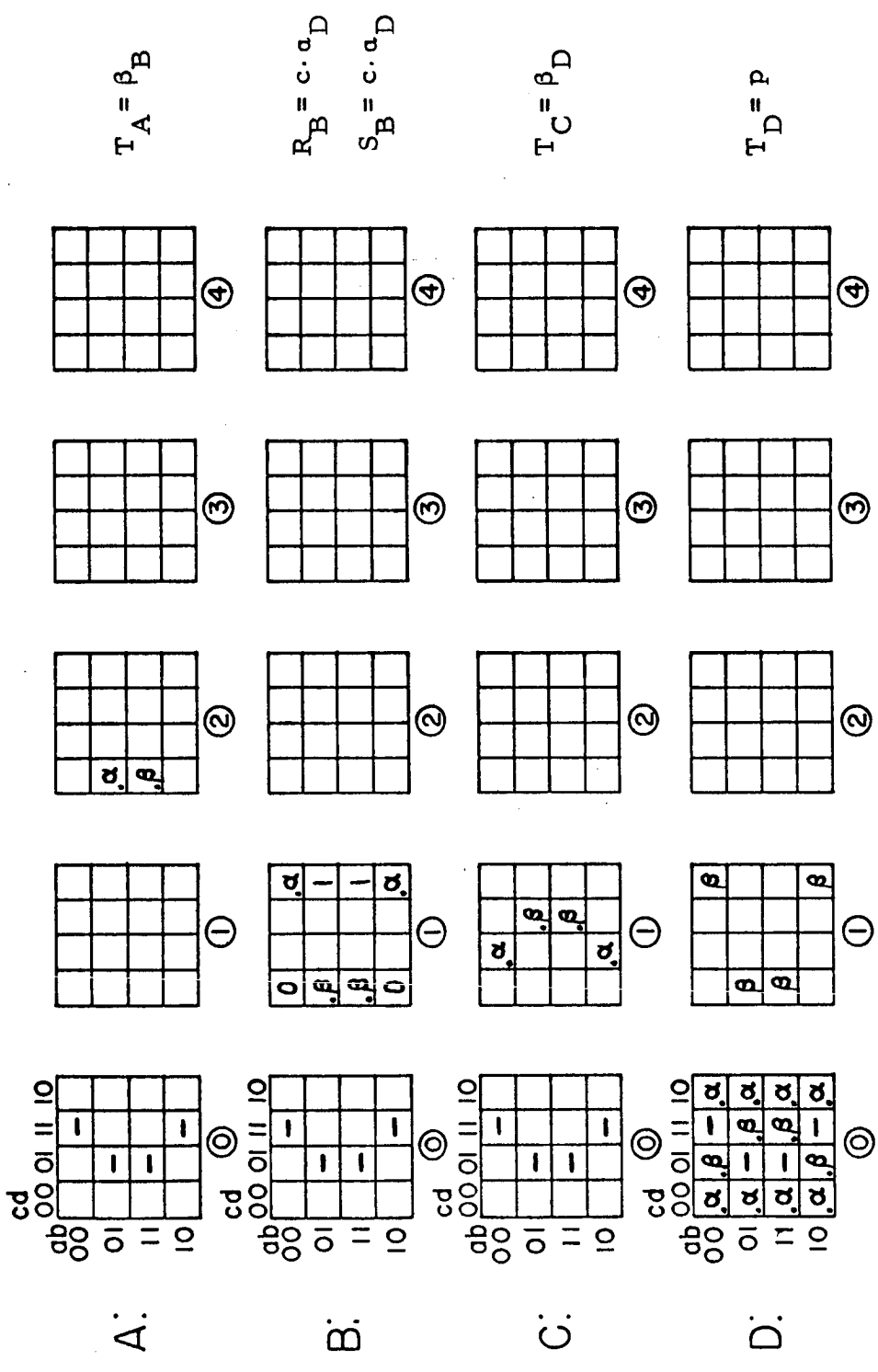

Figure 24. Result of step 4 in the second design of the duodecimal counter.

corresponding feedback transition on the map of lowest time index greater than both the expedient transition and the pulse which is to produce the feedback transition.

d. Derive input equations for all transitions which do not have dots in the lower left corners of their squares.

e. Place a dot in the lower left corner of each square containing a transition which has been taken into account.

The four β transitions on the map for D at time index 1 are the only feedback transitions. These four feedback transitions are located in squares corresponding to the squares in which the transitions of flip-flop B are entered; hence, they could be produced by using the transition pulses of B as RESET pulses for D. Since, the transitions of B are located at time index 1, the four feedback transitions of D must be moved to time index 2. No expedient transitions are needed.

In order to satisfy asynchronous input equation requirement 4, the input pulses which produce the feedback transitions of D have to be delayed. The input equation is

$R_D = (\alpha_B + \beta_B)(\tau)$. The fact that α_B and β_B are delayed by the inherent delay of flip-flop B is not sufficient to guarantee that requirement 4 will be satisfied, since the internal delay of B may be less than τ. Figure 25 shows the result of step 5.

6. For each transition which has a dot in the lower left corner of its square:
    a. Place a dot in the lower right corner of its square.
    b. Check all input equations to determine if the transition will cause any flip-flop to receive an input pulse which has not been entered.
    c. For each such input pulse:
        i. Make the corresponding entry on the map which is located in the row for the flip-flop which receives the pulse and has a time index one greater than the transition which causes it.
        ii. If the corresponding entry is a transition, place a dot in the lower left corner of its square.

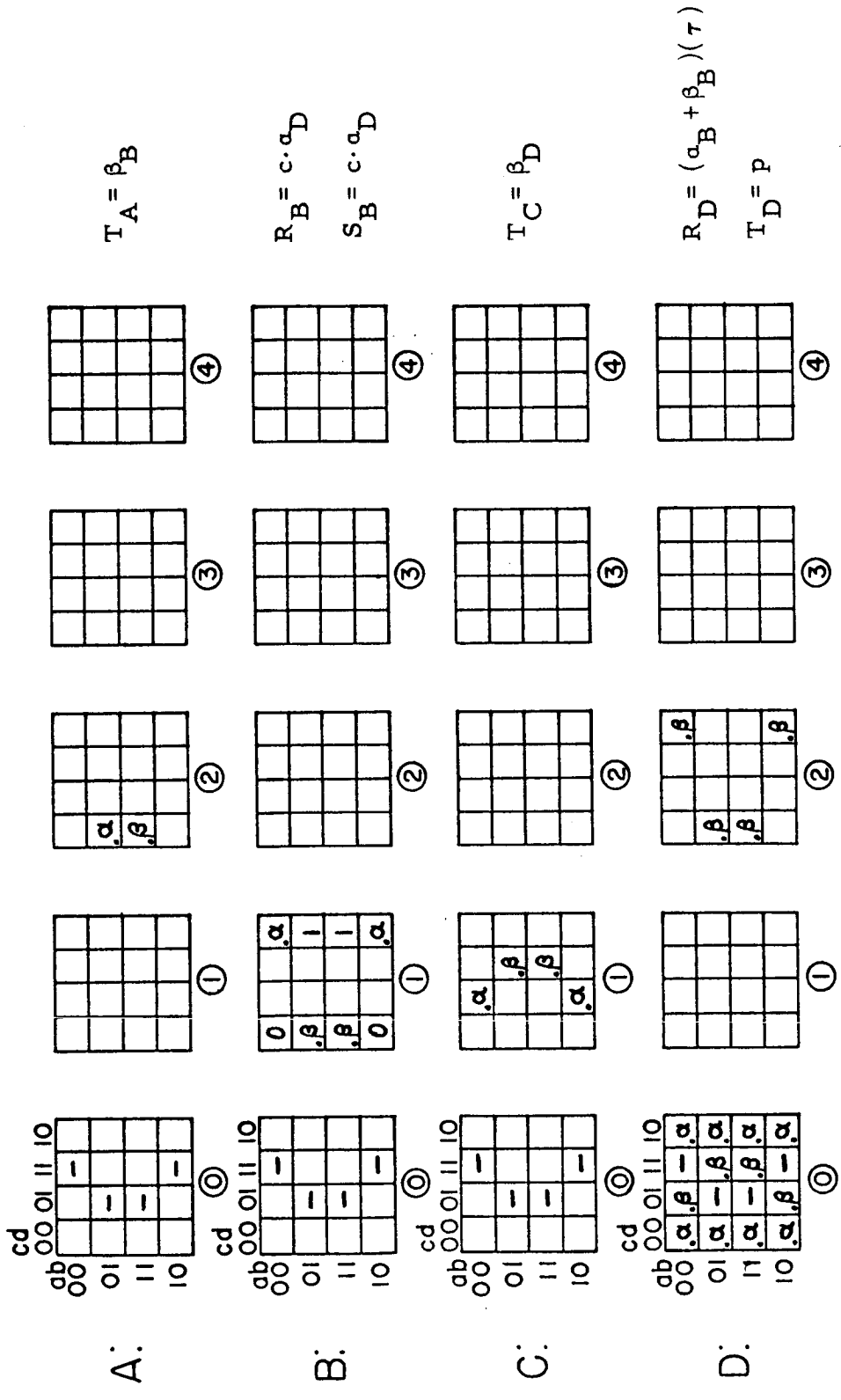

Figure 25. Result of step 5 in the second design of the duodecimal counter.

iii. If the corresponding entry is a transition, enter a feedback transition on the map of time index one greater in the same row.

All of the transitions shown in Figure 25 have dots in their lower left corners, indicating that they have been taken into account in the input equations. A check of all transitions against the input equations reveals that only the four β transitions of flip-flop D at time index 2 cause input pulses which have not been entered. These four cause flip-flop C to receive four TRIGGER input pulses. The two feedback transitions which occur when flip-flop C is initially in the ZERO state cause C to make α transitions; the two which occur when C is initially in the ONE state cause β transitions. The four of flip-flop C are entered on the map for C at time index 3 (see Figure 26). Dots are placed in the lower left corner of the squares in which these four entries are made, indicating that these entires are taken into account in the input equations. Four corresponding feedback transitions are entered on the map for flip-flop C at time index 4 in order to cancel the effect of these side-effect transitions.

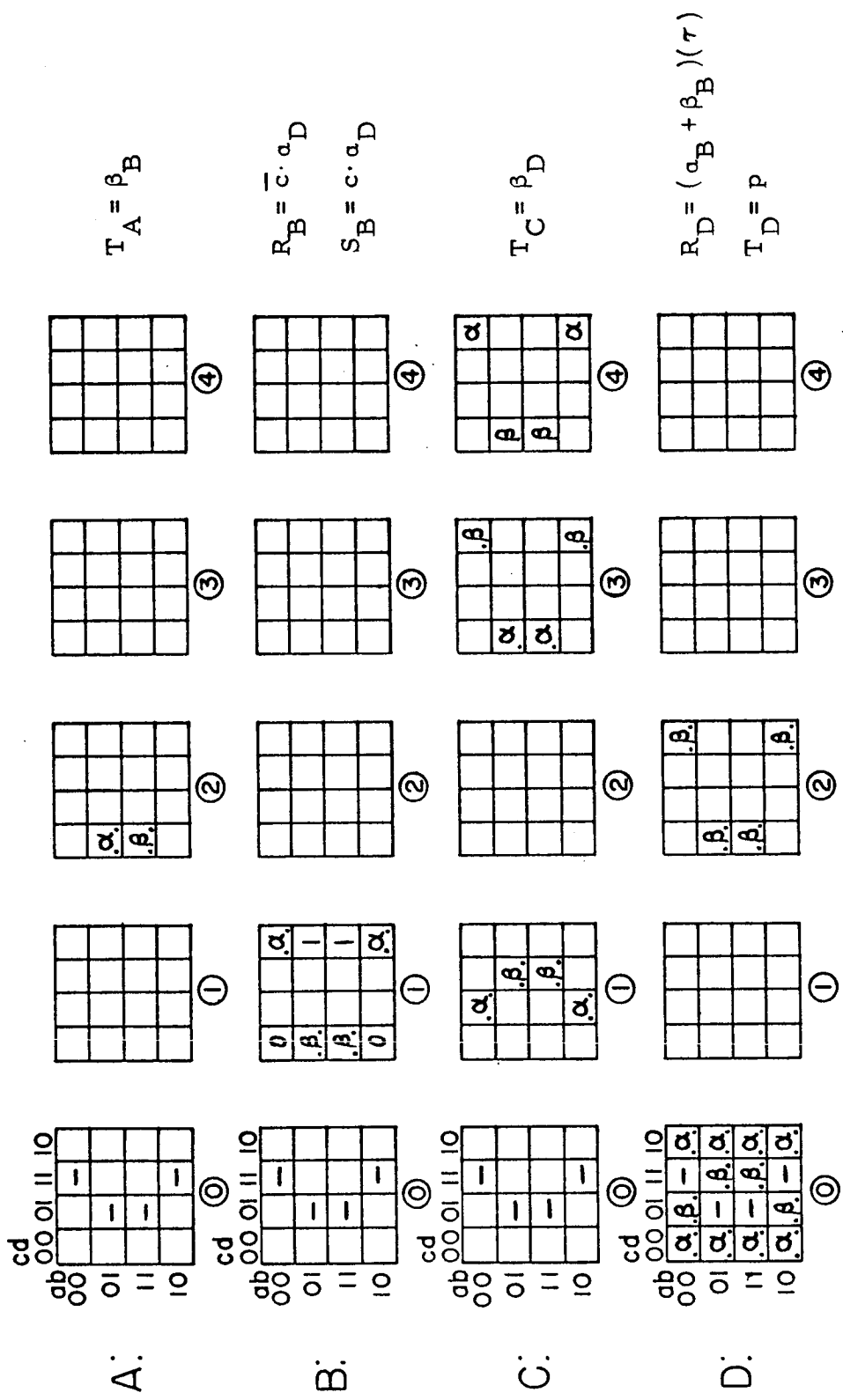

Figure 26. Result of step 6 in the second design of the duodecimal counter.

7. If there are any squares which contain transitions but do not have dots in both lower corners, then erase all the dots in the lower right corners and repeat steps 5 and 6. The procedure terminates when either (1) all squares containing transitions have dots in both lower corners, in which case the design is complete; or (2) the particular input equation scheme being pursued is found to be unusable, in which case the procedure must be restarted and a different equation scheme employed.

A check of the map array in Figure 26 reveals that there are some squares which contain transitions but do not have dots in both lower corners. The four side-effect transitions on the map for C at time index 3 do not have dots in the lower right corners of their squares, indicating that these transitions have not been checked against the input equations. The four feedback transitions on the map for C at time index 4 do not have any dots in their squares; this implies that these transitions have neither been taken into account in the input equations nor been checked against the

input equations. All the dots in the lower right corners of squares must therefore be erased, and step 5 has to be repeated.

Step 5 of the procedure requires that all feedback transitions be accounted for in the input equations. The feedback transitions on the map for flip-flop C at time index 4 are the only feedback transitions which do not have dots in the lower left corners of their squares and are thus the only ones which have not been taken into account. The two feedback β transitions of C at time index 4 will be produced by using the two β transitions of flip-flop B at time index 1 as RESET signals. The two feedback α transitions of flip-flop C at time index 4 will be produced by using the two α transitions of B at time index 1 as SET signals.

In order to satisfy asynchronous input equation requirement 4, the input pulses which are used to produce the feedback transitions on the map for C at time index 4 have to be delayed a minimum of τ with respect to the pulses which cause the side-effect transitions at time index 3. The side-effect transitions of C at time index 3 are caused by the feedback transitions on the map for D at time index 2, which are in turn caused, after a delay of τ, by the transitions

of B at time index 1. The total elapsed time from the occurance of an output pulse at flip-flop B to the arrival of an input pulse at flip-flop C is thus equal to the delay τ between the output of B and the input of D, plus the propagation time τ' [1] between the input and output of D. The output pulses of B which are to produce the feedback transitions of C at time index 4 have to be delayed by this length of time, $\tau + \tau'$, plus the delay specified by requirement 4, τ. The input equations are $S_C = \alpha_B(2\tau + \tau')$ and $R_C = \beta_B(2\tau + \tau')$. Figure 27 shows the result of this step.

The reasoning of the preceding paragraph is an example of the analysis which is used to ensure satisfaction of asynchronous input equation requirement 4. The general approach is the following. When one input signal must be delayed with respect to another, the two signals are first traced back to a common source. This can be done, since the counter input pulse is the source which initiates all action. The total time along each path is then calculated,

[1] τ' is the maximum length of time which elapses between the arrival of a pulse at the input of a flip-flop and the appearance of a transition pulse at the output.

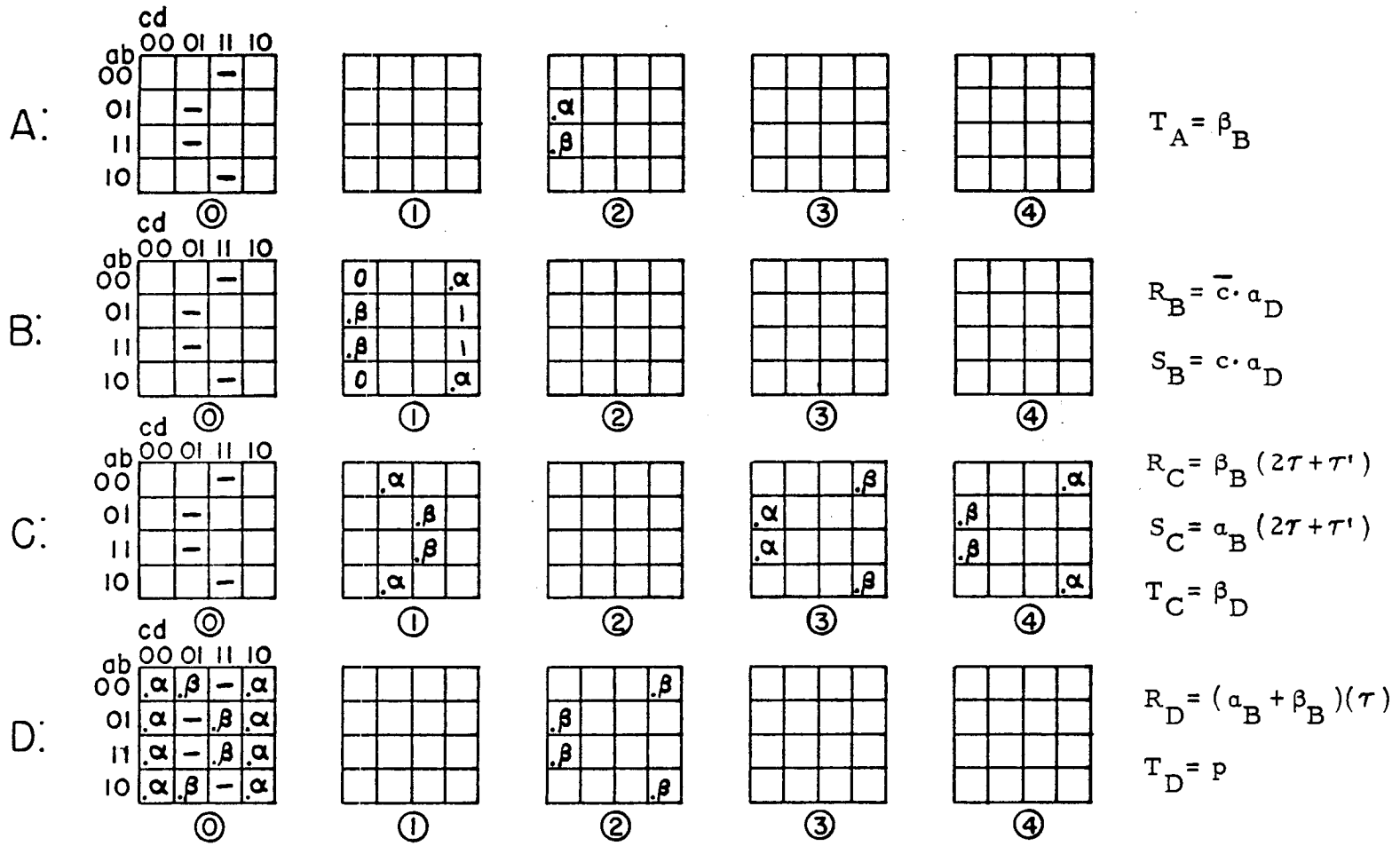

Figure 27. Result of the second application of step 5 in the second design.

and an additional delay is added to the path of the signal which is to be delayed, if necessary.

Step 6 of the procedure requires that each transition with a dot in the lower left corner of its cell be checked against all input equations. This must be done in order to insure that the map array present an accurate account of all input pulses and transitions.

Figure 27 shows that every transition has a dot in the lower left corner of its square; each must be checked against the input equations. Checking all transitions reveals that all necessary map entries have been made. (A dot in the lower right corner of a square containing a transition marks that transition as having been checked). The result of this step is shown in Figure 28.

Because all of the squares containing transitions have dots in both lower corners (see Figure 28), the design is complete by virtue of step 7.

A comparison of the first design of the duodecimal counter, shown in Figure 22, and the second design, Figure 29, discloses that three gates have been eliminated at a cost of adding three delay elements. This change in the design was

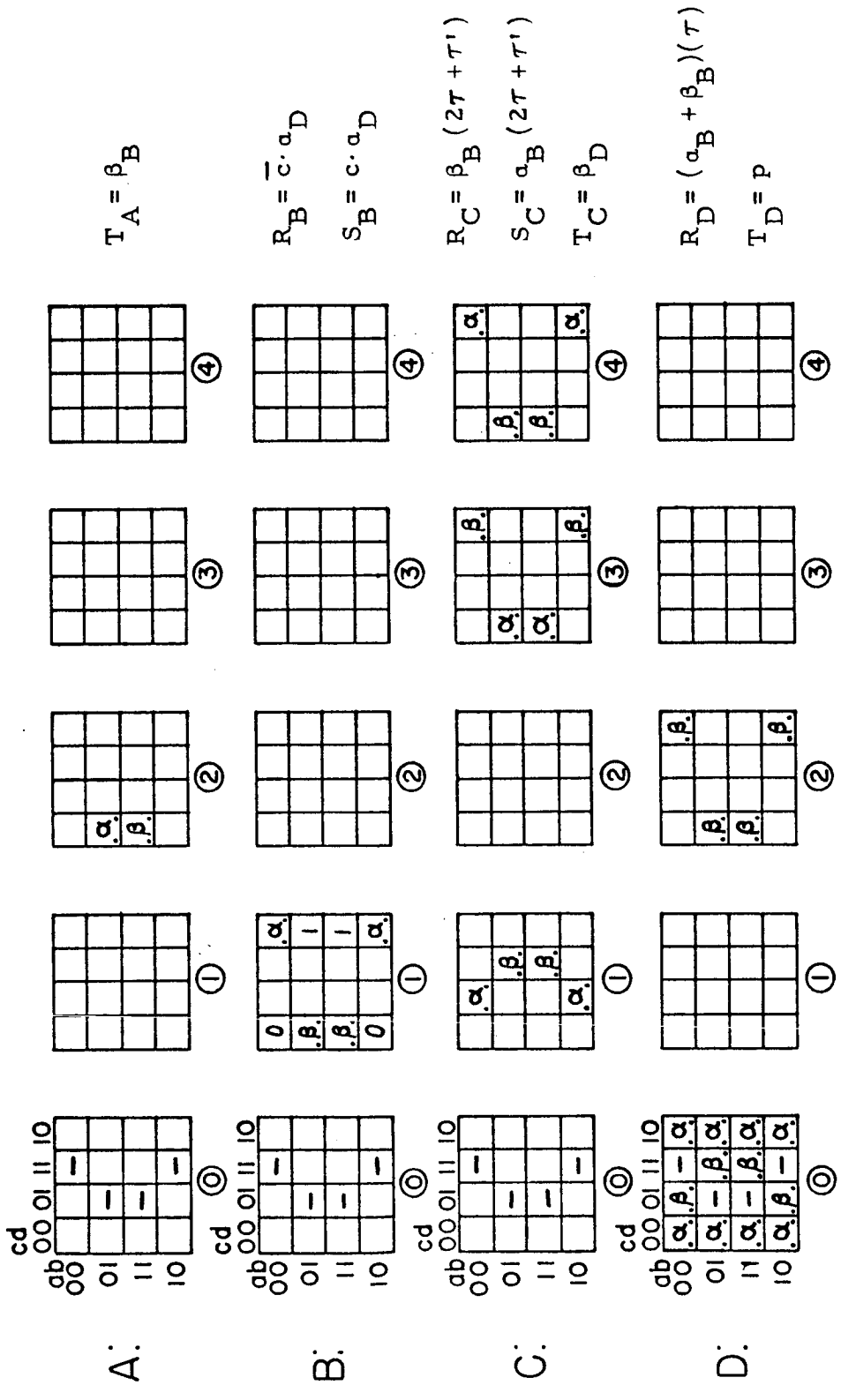

Figure 28. Final result of the second design of the duodecimal counter.

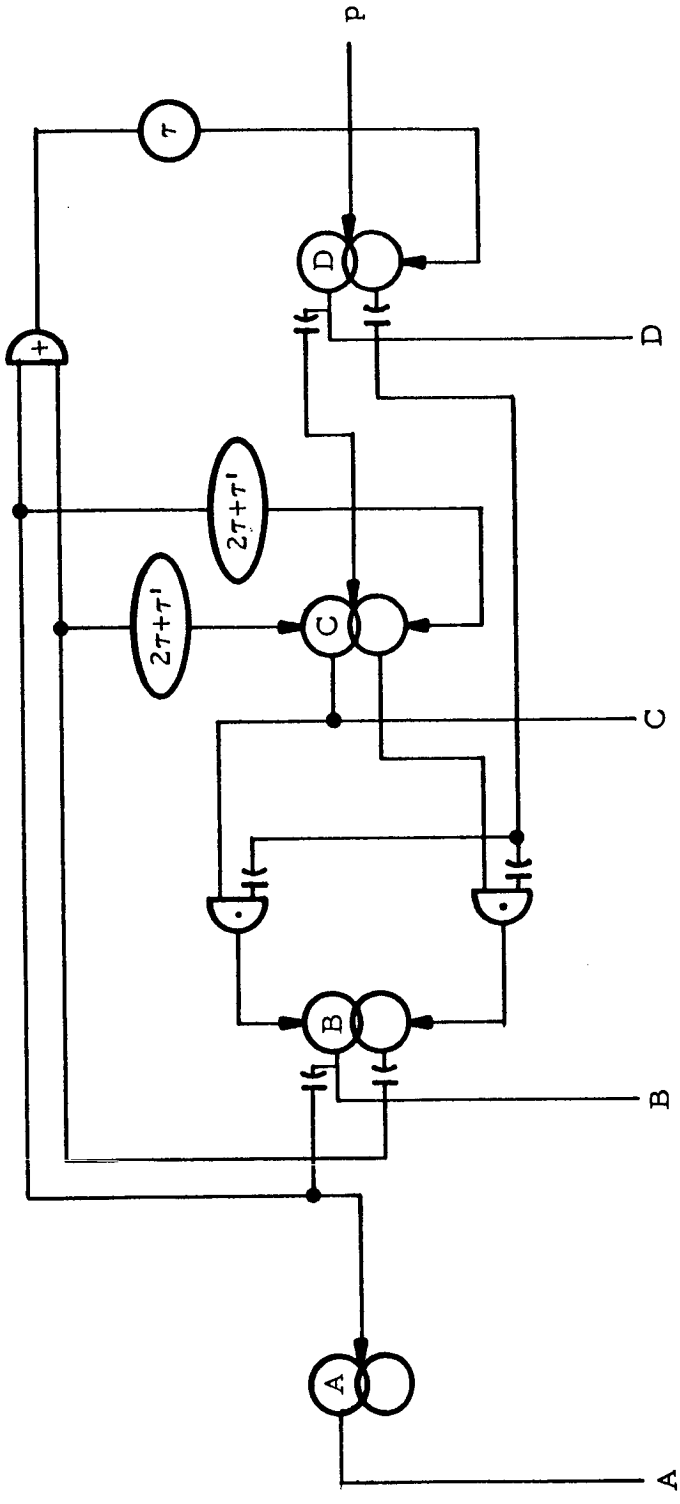

Figure 29. Second design of the duodecimal counter.

made possible by having flip-flop D undergo expedient transitions. It is therefore logical to investigate the possibility of using expedient transitions to reduce or eliminate the input gating to flip-flop B. Toward this end, the synthesis procedure will be employed a third time.

For the third design of the duodecimal counter, the first three steps will be executed exactly as they were in the second design; the result is shown in Figure 23.

4. Consider the essential transitions which are to be produced by the output pulses of other flip-flops.
   a. Remove each of these transitions from its position at time index 0, and re-enter it in the corresponding square on the map in the same row at time index one greater than the output pulse which is to produce it.
   b. Add expedient transitions where profitable.
   c. For each expedient transition added, enter a corresponding feedback transition on the map of time index one greater in the same row.
   d. Derive input equations for the essential and expedient transitions under consideration.

e. Place a dot in the lower left corner of each square containing a transition which has been taken into account.

In Figure 23, the transitions of flip-flop C are located in squares corresponding to those in which the β transitions of flip-flop D at time index 0 are entered. The transitions of C can therefore be produced by using the β pulses of D as the TRIGGER input signal -- $T_C = \beta_D$. The transitions of C have to be moved to time index 1.

The transitions of flip-flop B are entered in squares associated with initial states for which flip-flop D makes α transitions. If expedient transitions are added to the 0000, 0110, 1110, and 1000 squares on the map for B, the essential and expedient transitions of flip-flop B can be produced by using the α pulses of flip-flop D as TRIGGER pulses -- $T_B = \alpha_D$. These essential and expedient transitions have to be located at time index 1. Because flip-flop B is initially in the ZERO state for the 0000 and 1000 squares, the expedient transitions entered there are α transitions. Flip-flop B is initially in the ONE state for the 0110 and 1110 squares; the entries are therefore β

transitions (see Figure 30). In order to cancel the effect of the expedient transitions, feedback transitions must be entered on the map for B at time index 2. Figure 30 shows that two β feedback transitions have been placed in the squares corresponding to the squares which contain the α expedient transitions at time index 1. Two α feedback transitions have been entered at positions corresponding to the β expedient transitions.

Figure 23 shows that the two transitions of flip-flop A correspond to the two β transitions of flip-flop B. In the first and second designs, this fact was used to write $T_A = \beta_B$ as the input equation for flip-flop A. In this third design, however, flip-flop B undergoes two expedient β transitions and two feedback β transitions (see Figure 30) in addition to the two essential β transitions shown on the map array of Figure 23. Thus, in order to employ the input equation $T_A = \beta_B$ in this third design, and thereby avoid the use of logical gating to produce the transitions of A, expedient transitions are added to the maps for A. In Figure 30, the transitions in the 0100 and 1100 squares of the map for A at time index 2 are the essential transitions of flip-flop A;

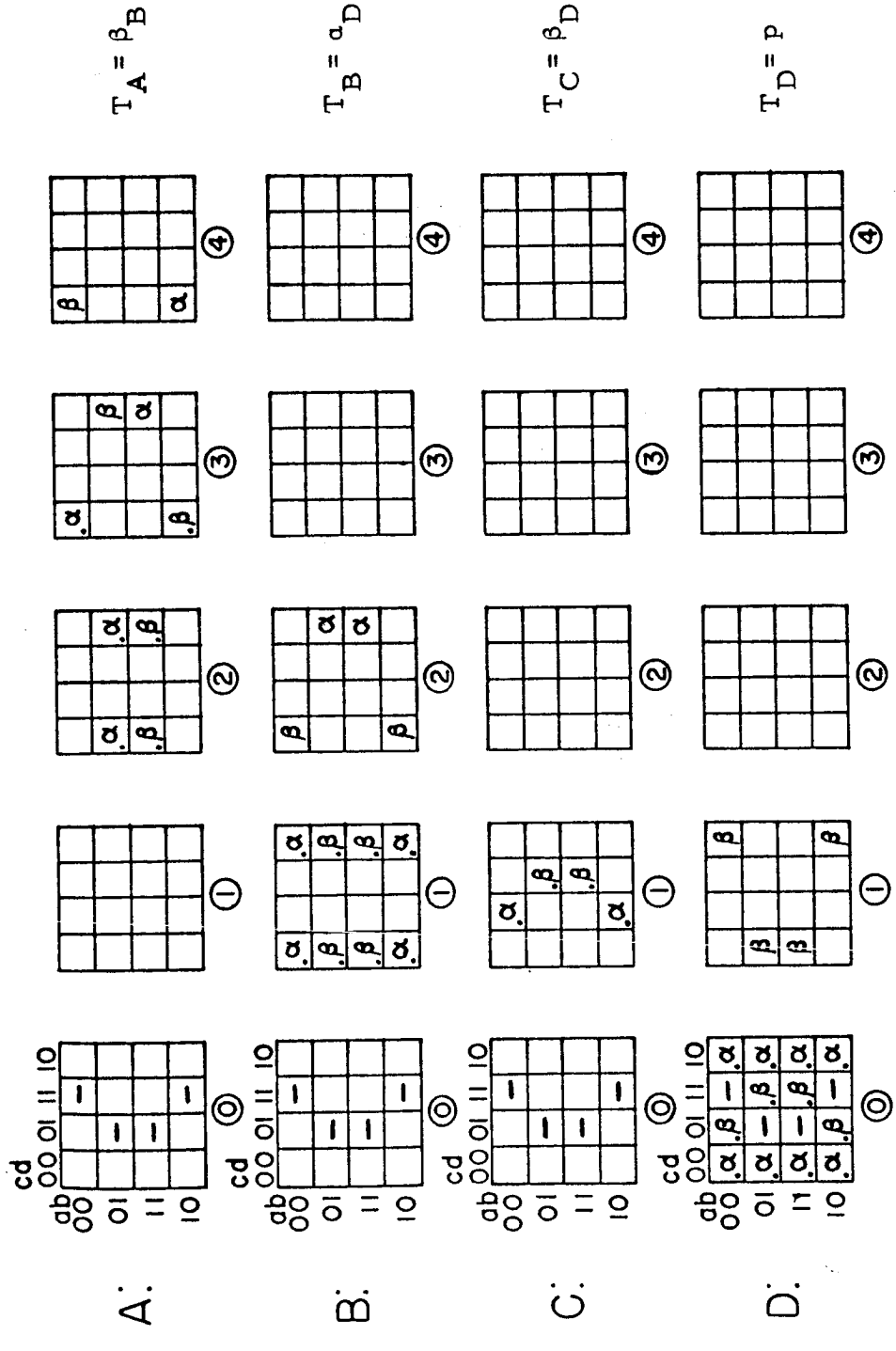

Figure 30. Result of step 4 in the third design of the duodecimal counter.

those in the 0110 and 1110 squares at time index 2 and the 0000 and 1000 squares at time index 3 are expedient transitions. (If the input equation $T_A = \beta_B$ were used, and these four expedient transitions were not entered at this point in the procedure, step 6 would require that they be entered at that time). Four feedback transitions must be employed to cancel the effect of the expedient transitions; these are entered in the 0110 and 1110 squares at time index 3 and the 0000 and 1000 squares at time index 4.

5. Consider the feedback transitions which do not have dots in the lower left corners of their squares.
   a. If any feedback transition does not have a time index at least one greater than the pulse which is to produce it, remove it and re-enter it in the corresponding square on the map in the same row at time index one greater than the pulse which is to produce it.
   b. Add expedient transitions where profitable.
   c. For each expedient transition added, enter a corresponding feedback transition on the map of lowest time index greater than both the

expedient transition and the pulse which is to produce the feedback transition.

d. Derive input equations for all transitions which do not have dots in the lower left corners of their squares.

e. Place a dot in the lower left corner of each square containing a transition which has been taken into account.

The four β feedback transitions on the map for flip-flop D at time index 1 will be produced by using the counter input pulse -- $R_D = ((\,b\bar{c} + \bar{b}c\,)\cdot p)(\tau)$. The dash entries in the 0011, 0101, 1101, and 1011 squares (see Figure 31) have been used to simplify the input expression. Note that in order to satisfy asynchronous input equation requirement 3, the RESET signal must be delayed <u>after</u> the PULSE-AND gate; the counter input pulse must <u>not</u> be delayed <u>before</u> it is applied to the gate.

The two feedback β transitions of flip-flop B, located on the map at time index 2, will be accounted for by $R_B = (\bar{b}\,\bar{c}\,\bar{d}\cdot p)(\tau + \tau')$. The delay of $\tau + \tau'$ is necessary because the input pulses which cause the expedient transitions of B

at time index 1, that is, the α pulses from flip-flop D, are delayed by τ' with respect to the counter input pulse; the pulses which produce the feedback transitions at time index 2 must be delayed by an additional length of time τ. The two feedback α transitions on the map for flip-flop B at time index 2 will be produced by the SET signal $S_B = (b\,c\,\bar{d}\cdot p)(\tau + \tau')$.

The two feedback transitions of flip-flop A entered in the 0110 and 1110 squares at time index 3 can be produced by means of the TRIGGER signal $T_A = (b\,c\,\bar{d}\cdot p)(\tau + 2\tau')$. The delay of $\tau + 2\tau'$ is determined by the following reasoning. The pulses which produce the feedback transitions at time index 3 must be delayed by at least τ from the pulses which cause the expedient transitions at time index 2. The expedient transitions at time index 2 are produced by the β output pulses from flip-flop B at time index 1. The pulses of flip-flop B are delayed by at most τ' with respect to the input signals which cause them -- the α pulses from flip-flop D. The α pulses of D are delayed by at most τ' with respect to the counter input pulses. Thus, the pulses which produce the feedback transitions at time index 3 must

be delayed a minimum of $\tau + 2\tau'$ with respect to the counter input pulse.

The two feedback transitions of flip-flop A at time index 4 will be produced by means of the TRIGGER input signal $T_A = (\bar{b}\,\bar{c}\,\bar{d}\cdot p)(2\tau + 2\tau')$. The delay is derived as follows. The pulses which produce the feedback transitions at time index 4 must be delayed by at least τ from the pulses which cause the expedient transitions at time index 3. These expedient transitions are caused by the β pulses from flip-flop B at time index 2, which have a delay of at most τ' with respect to the input pulses which cause them. The transitions of B at time index 2 are produced by the RESET signal $R_B = (\bar{b}\,\bar{c}\,\bar{d}\cdot p)(\tau + \tau')$. Thus, the total delay is $\tau + \tau' + (\tau + \tau') = 2\tau + 2\tau'$.

Because the term $\bar{b}\,\bar{c}\,\bar{d}\cdot p$ appears in both the RESET equation for flip-flop B and the TRIGGER equation for flip-flop A, the same gate can be used to implement both equations. Also, only one gate is needed for the term $b\,c\,\bar{d}\cdot p$, which appears in the SET equation for flip-flop B and the TRIGGER equation for flip-flop A.

6. For each transition which has a dot in the lower

left corner of its square:

a. Place a dot in the lower right corner of its square.

b. Check all input equations to determine if the transitions will cause any flip-flop to receive an input pulse which has not been entered.

c. For each such input pulse:

   i. Make the corresponding entry on the map which is located in the row for the flip-flop which receives the pulse and has a time index one greater than the transition which causes it.

   ii. If the corresponding entry is a transition, place a dot in the lower left corner of its square.

   iii. If the corresponding entry is a transition, enter a feedback transition on the map of time index one greater in the same row.

All of the transitions entered on the map array in Figure 31 have dots in the lower left corners of their squares. A check of each transition against the input

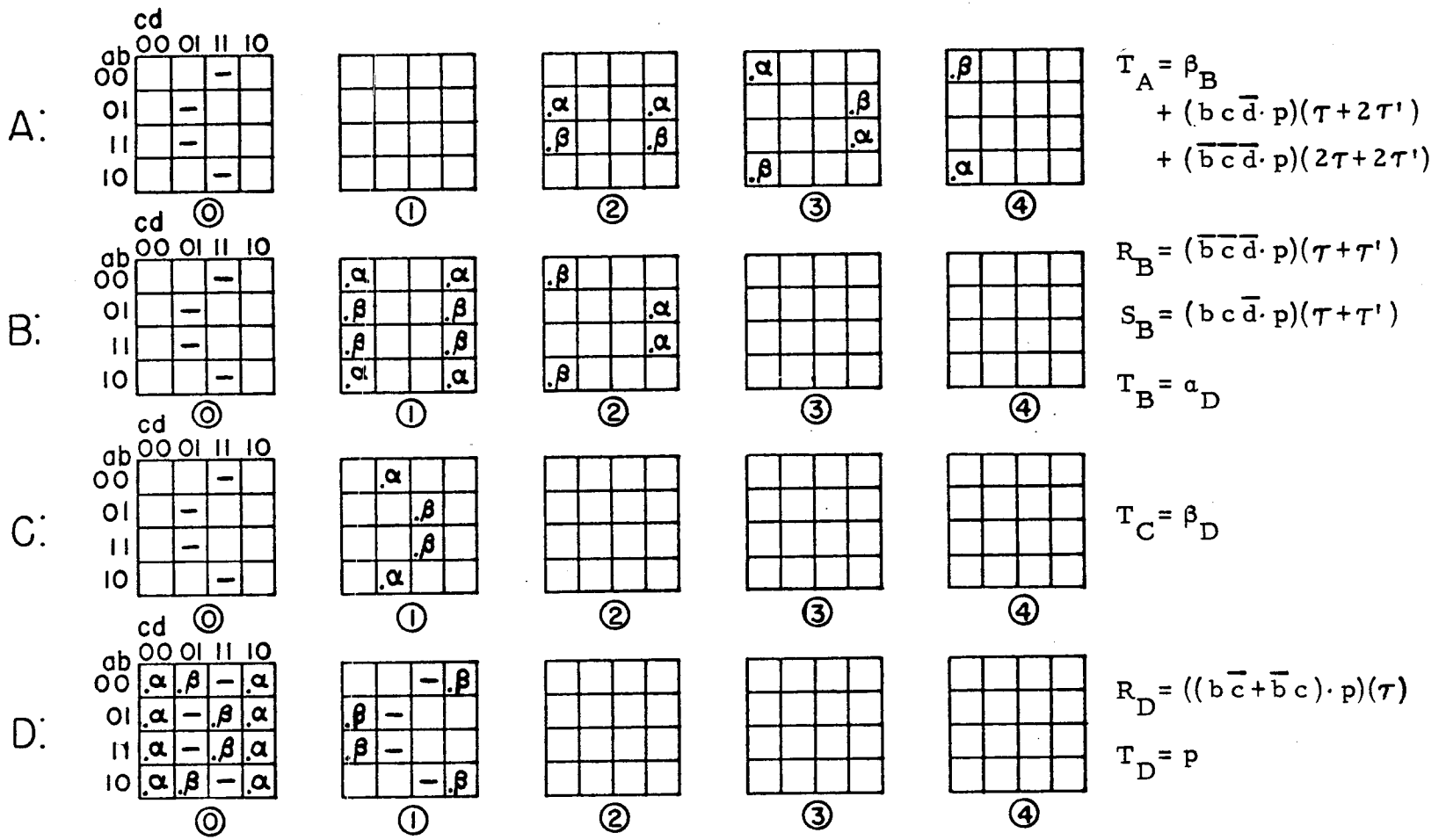

Figure 31. Result of step 5 in the third design of the duodecimal counter.

equations discloses that only the four β transitions of flip-flop D at time index 1 cause the input pulses which have not been entered. These four β transitions cause flip-flop C to receive four TRIGGER input pulses (see Figure 32) at time index 2. The two feedback transitions of flip-flop D which occur when flip-flop C is in the ZERO state cause C to make α transitions; the two which occur when C is in the ONE state cause β transitions. Dots are placed in the lower left corners of the squares of these side-effect transitions, indicating that they are accounted for in the input equations. Four corresponding feedback transitions are entered on the map for flip-flop C at time index 3 in order to cancel the effect of the side-effect transitions.

7. If there are any squares which contain transitions but do not have dots in both lower corners, then erase all the dots in the lower right corners and repeat steps 5 and 6....

An examination of the map array in Figure 32 reveals that the squares containing the side-effect and feedback transitions of flip-flop C do not have dots in both lower corners. Thus, step 5 must be repeated.

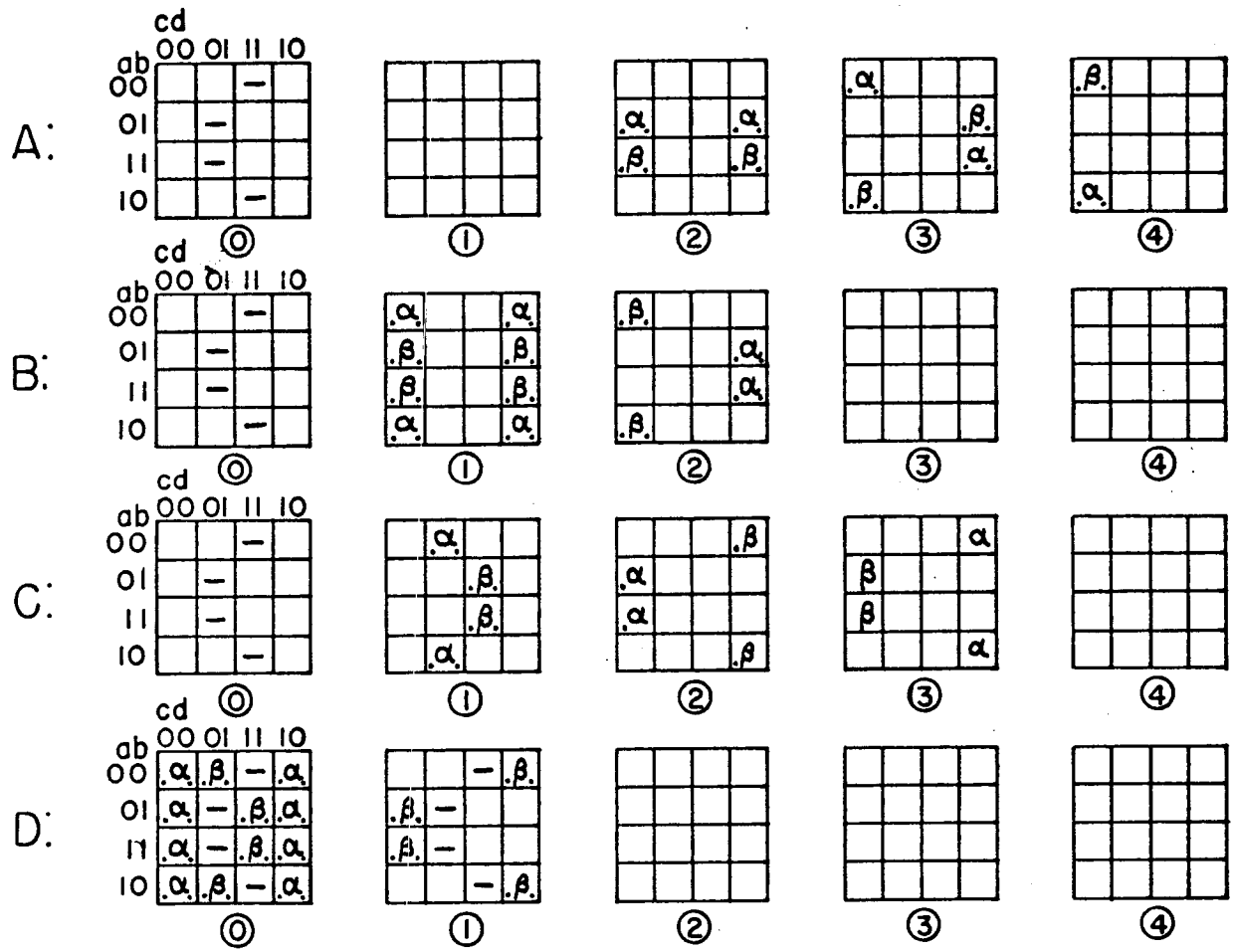

Figure 32. Result of step 6 in the third design of the duodecimal counter.

Step 5 of the procedure requires that input equations be derived for all feedback transitions. The four feedback transitions on the map for flip-flop C at time index 3 (Figure 32) are the only transitions which do not have dots in the lower left corners of their squares; these are the only transitions which are not accounted for in the input equations.

The two β transitions of flip-flop C at time index 3 will be produced by using the β pulses of flip-flop B at time index 1 as RESET pulses. Expedient β transitions are entered in the 0110 and 1110 squares on the map for C at time index 3 (see Figure 33). These entries are made in order to eliminate the need for logical gating to select only the β pulses entered in the 0100 and 1100 squares as RESET pulses. Adding the two expedient β transitions makes it necessary to add two feedback α transitions in the 0110 and 1110 squares at time index 4.

The input equation for the β transitions at time index 3 is $R_C = \beta_B(2\tau + \tau')$. The delay of $2\tau + \tau'$ is determined as follows. The side-effect transitions of C at time index 2 are caused by the β pulses from D at time

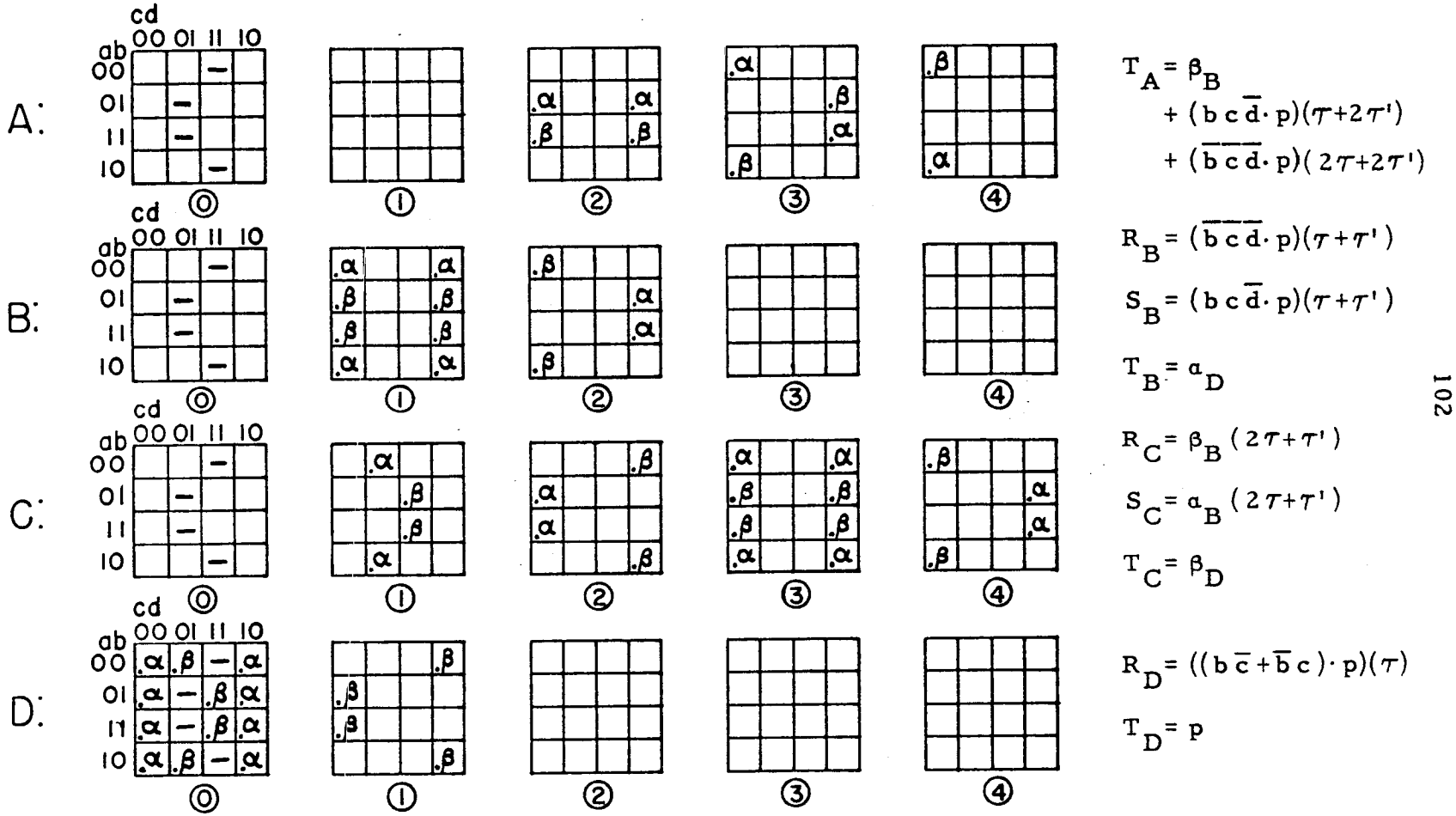

Figure 33. Result of second application of step 5 in the third design.

index 1. These β pulses are delayed at most τ' with respect to the input signal which causes them -- $R_D = ((b\bar{c} + \bar{b}c)\,p)\,(\tau)$ -- which is delayed by τ with respect to the counter input pulse. Thus, the pulses which cause the side-effect transitions of C at time index 2 are delayed by a total length of time $\tau + \tau'$ with respect to the counter input pulse. The signal which produces the β transitions at time index 3 must be delayed by an additional length of time τ in order to satisfy asynchronous input equation requirement 4.

The two α transitions of flip-flop C at time index 3 will be produced by using the α pulses of flip-flop B at time index 1 as SET pulses. Expedient α transitions will be entered in the 0000 and 1000 squares of the map for C at time index 3 in order to avoid the use of logical gating at the SET input of flip-flop C. Two feedback β transitions must be entered in the 0000 and 1000 squares at time index 4.

The input equation for the α transitions of flip-flop C at time index 3 is $S_C = \alpha_B(2\tau + \tau')$. The amount of delay required is the same as that for the RESET input of flip-flop C.

Part d of step 5 requires that input equations be derived for the transitions located on the map for C at time index 4.

Note that the four transitions of C at time index 4 are located in squares corresponding to those which contain the four transitions of B at time index 2. The two β transitions of flip-flop B at time index 2 will cause the two β transitions of flip-flop C at time index 4 by means of the RESET input $R_C = \beta_B(2\tau + \tau')$. The two α transitions of B at time index 2 will produce the α transitions of C at time index 4 by means of the SET input $S_C = \alpha_B(2\tau + \tau')$. Thus, all transitions on the map array of Figure 33 are accounted for in the equations.

Step 6 of the procedure requires that all transitions with dots in the lower left corners of their squares be checked against the input equations. A check of the transitions on the map array in Figure 33 shows that all the input pulses implied by the input equations have been taken into account. The result of step 6 is shown in Figure 34.

All of the squares containing transitions (Figure 34) have dots in both lower corners; step 7 states that the design is therefore complete. The third design of the duodecimal counter is shown in Figure 35.

The repeated application of the asynchronous synthesis

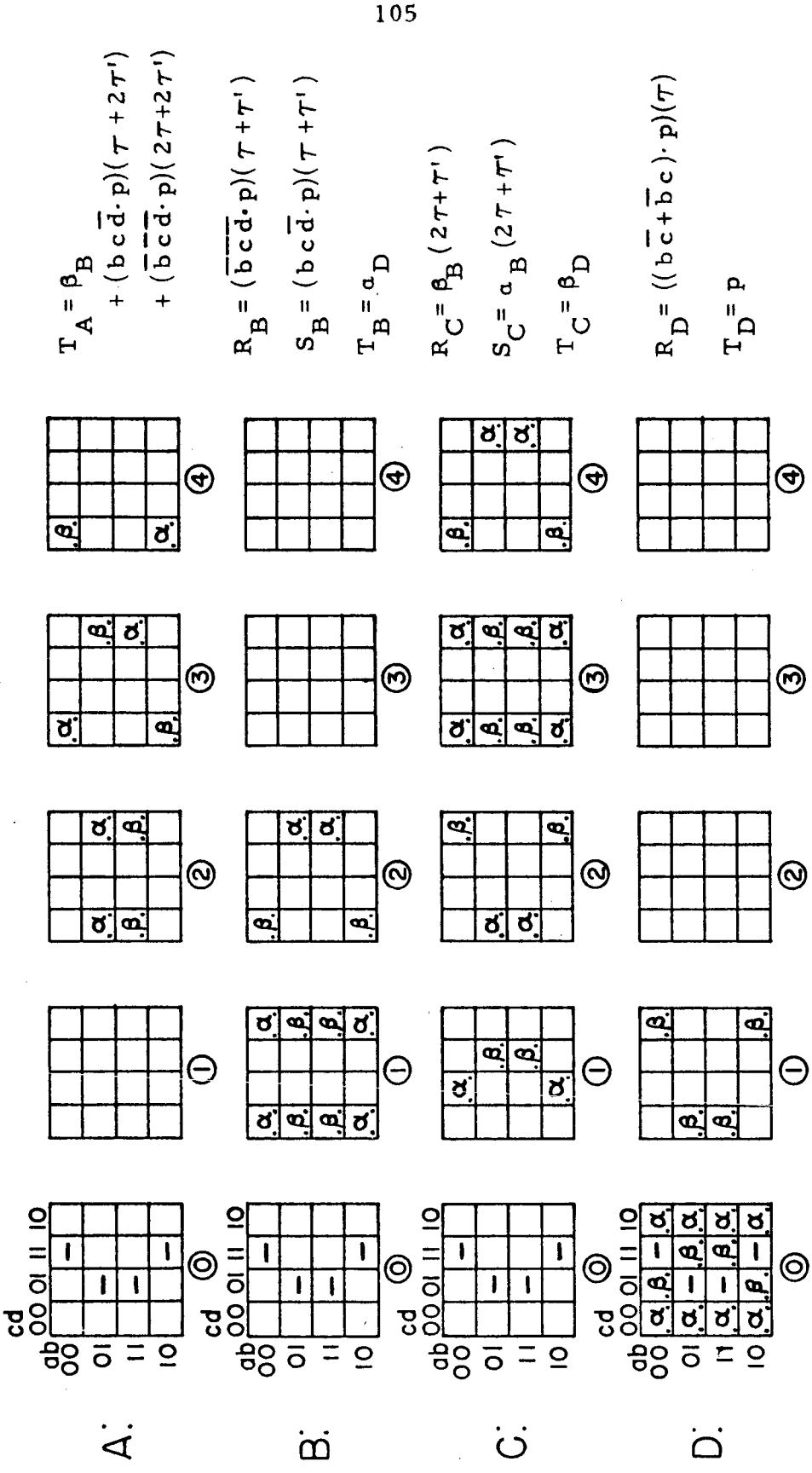

Figure 34. Final result of the third design of the duodecimal counter

procedure to the design of the duodecimal counter exemplifies an approach to the problem of synthesizing counters with a minimum amount of logical gating. First, the procedure was used to arrive at a design which did not employ expedient and feedback transitions. Such a design was needed as a basis of evaluation for the more sophisticated designs to be attempted. The synthesis procedure was then applied a second time, and a conservative number of expedient transitions were introduced in an attempt to minimize logical gating. Having found that the expedient transitions used in the second design resulted in the simplification of the input equation set, the procedure was employed a third time. In the third design, a number of expedient transitions were intorduced in addition to those used in the second design. The result was an increase in complexity compared to the initial design.

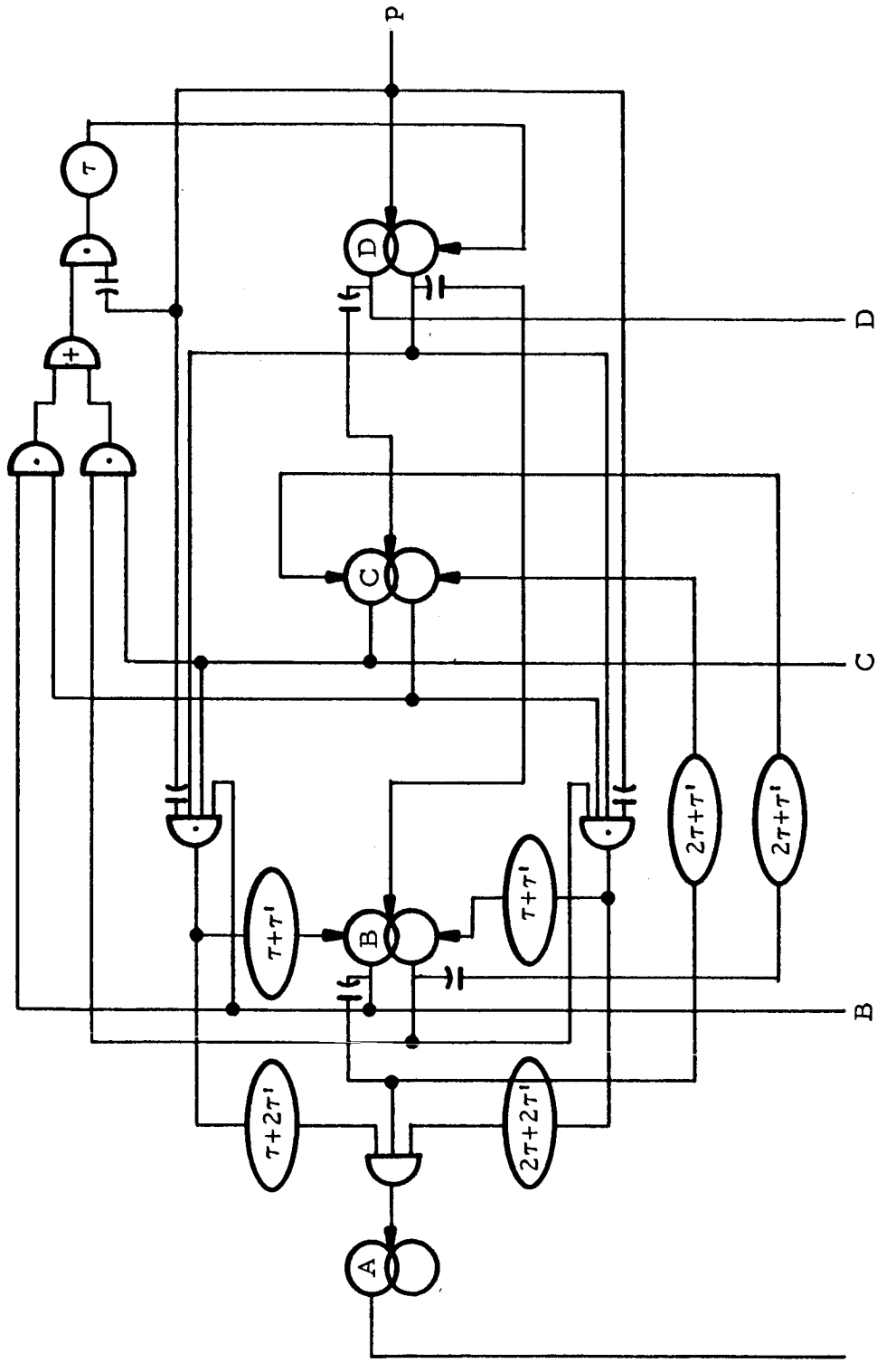

Figure 35. Third design of the duodecimal counter.

V. CONCLUSIONS

The logical design of single input sequential circuits, or counters, is commonly carried out by first applying the well developed synchronous design procedures and then reducing the amount of hardware by heuristic means. The latter step often leads to the utilization of asynchronous techniques.

A systematic method has been presented which, starting with a specified counting sequence, leads to an asynchronous implementation of the counter.

In the method that has been presented, the logical operation of a flip-flop is characterized in terms of the change of state which occurs when the flip-flop is in a given initial state and is subjected to a given input signal. This is in contrast to the conventional approach of describing the logical operation of a flip-flop in terms of the next state assumed by the flip-flop as a function of initial state and input signal.

Although the difference between characterizing a flip-flop

in terms of state transitions and describing it in terms of its next state may appear slight, the former has distinct advantages. The reason is that using the present state and next state of a flip-flop to describe its logical operation naturally leads to the use of clock pulse gated output levels for the transmission of information within a counter. The characterization in terms of state transitions, however, enables the use of a second source of information and a second information carrier. In addition to flip-flop output levels, use is made of the level changes as a source of information. In addition to gated output levels, pulses dervied from the output level changes serve as information carriers.

The characterization of the logical action of a flip-flop in terms of state transition is one of the two basic concepts in the transitions map method presented. The second fundamental concept is the display of all logical information in transition map form. A single transition map provides sufficient information for the derivation of synchronous input equations for a single flip-flop. A single set of transition maps -- one for each flip-flop -- displays sufficient

information for the derivation of asynchronous input equations for a counter without logical feedback. A map array, with its additional dimension corresponding to time, displays sufficient information for the synthesis of asynchronous counters employing logical feedback.

APPENDIX

The fact that permutations of the digit positions in the counter state sequence table need not be investigated during the search for a simple counter design can be demonstrated by proving that

(1) if, for a given arrangement of digit positions, a single entry on one transition map and a single entry on a second transition map are located in squares corresponding to the same initial state, then the same entries will be located in corresponding squares for any permutation of the digit positions;

(2) if, for any given arrangement of digit positions, a group of adjacent entries on one transition map and an equal number of adjacent entries on a second transition map are located in squares corresponding to the same initial states, then the same groups will be located in corresponding adjacent squares for any permutation of the digit positions; and

(3) if the digit positions are rearranged, the number of occurrences of each type of entry on each transition map

remains constant.

The proof of these three statements will demonstrate that every map entry correspondence--that is, the correspondence that exists between map entries which are located in squares corresponding to the same initial state of the counter--is unchanged by permutation of the digit positions. The proof will also indicate that no new map entries are created by rearranging the digit positions. It follows that permuting the digit positions creates no new map entry correspondences which might aid in the simplification of the counter.

In the following proofs, let $X_1X_2 \ldots X_n$ denote a particular digit position arrangement for a counter state sequence table which defines the operation of an n bit counter. For each X_m, the m^{th} column of the sequence table, there is an associated flip-flop and an associated transition map. Let $x_1x_2 \ldots x_n$ and $x_1'x_2' \ldots x_n'$ range over all 2^n possible values of $X_1X_2 \ldots X_n$--x_m, $x_m' \in \{0, 1\}$ for $m = 1, 2, \ldots, n$. For every value $x_1x_2 \ldots x_n$ and $x_1'x_2' \ldots x_n'$ there is an associated square on each transition map.

Let the operation of replacing one arrangement of the digits $X_1X_2 \ldots X_n$ by a second arrangement $X_{i_1} X_{i_2} \ldots X_{i_n}$ be

denoted by $P(X_1X_2\ldots X_n) = X_{i_1}X_{i_2}\ldots X_{i_n}$. The permutation P replaces every value $x_1x_2\ldots x_n$ by $P(x_1x_2\ldots x_n) = x_{i_1}x_{i_2}\ldots x_{i_n}$. Let the permutation be such that the j^{th} digit in the original arrangement is moved to the k^{th} position in the permuted order--$X_j = X_{i_k}$. Then the value of the j^{th} digit of a particular $x_1x_2\ldots x_n$ is equal to the value of the k^{th} digit in $P(x_1x_2\ldots x_n) = x_{i_1}x_{i_2}\ldots x_{i_n}$, that is, $x_j = x_{i_k}$. Further assume that under P, the p^{th} digit X_p is moved to the q^{th} position--$X_p = X_{i_q}$. Thus, the value x_{i_q} in $x_{i_1}x_{i_2}\ldots x_{i_n}$ is equal to the value x_p in $x_1x_2\ldots x_n$.

Let $e_1, e_1', e_2, e_2', \ldots$ be particular map entries, including the possibility of a blank--$e_ie_i' \in \{$ (blank), 0, 1, α, β, —$\}$ for $i = 1, 2, \ldots$.

Proof Statement (1)

Assume that the $x_1x_2\ldots x_n$ square of the transition map for a particular flip-flop X_j contains the entry e_1, and that the $x_1x_2\ldots x_n$ square of the transition map for flip-flop X_p contains the entry e_2.

Two cases must be examined:

(a) If the state $x_1x_2\ldots x_n$ does not appear in the original sequence table, then e_1 = "-" and e_2 = "-." Since the state

$x_1x_2\ldots x_n$ does not appear in the original sequence table, and since the permutation P is a one-to-one function, the state $P(x_1x_2\ldots x_n) = x_{i_1}x_{i_2}\ldots x_{i_n}$ does not appear in the rearranged sequence table. It follows that the $x_{i_1}x_{i_2}\ldots x_{i_n}$ squares on the maps for X_{i_k} and X_{i_q} will each contain the entry "-." Now since "-" = e_1 and "-" = e_2, the correspondence between the entry e_1 on the map for $X_j = X_{i_k}$ and the entry e_2 on the map for $X_p = X_{i_q}$ has been preserved under the permutation P.

(b) If the state $x_1x_2\ldots x_n$ is listed in the original sequence table, then the entries e_1 and e_2 are determined by the next state in the sequence. Let $x_1'x_2'\ldots x_n'$ be the next state. Entry e_1 in the $x_1x_2\ldots x_n$ square on the map for X_j is determined by x_j and x_j'. Entry e_2 in the $x_1x_2\ldots x_n$ square on the map for X_p is determined by x_p and x_p'. Under the permutation p, $p(x_1x_2\ldots x_n) = x_{i_1}x_{i_2}\ldots x_{i_n}$ and $P(x_1'x_2'\ldots x_n') = x_{i_1}'x_{i_2}'\ldots x_{i_n}'$. The entry e_3 in the $x_{i_1}x_{i_2}\ldots x_{i_n}$ square on the map for X_{i_k} is determined by x_{i_k} and x_{i_k}', and the entry e_4 in the $x_{i_1}x_{i_2}\ldots x_{i_n}$ square on the map for X_{i_q} is determined by x_{i_q} and x_{i_q}'. Because $x_{i_k} = x_j$ and $x_{i_k}' = x_j'$, however, $e_3 = e_1$. Because $x_{i_q} = x_p$ and $x_{i_q}' = x_p'$, $e_4 = e_2$. Thus the correspondence between the entry e_1 on the map for

$X_j = X_{i_k}$ and the entry e_2 on the map for $X_p = X_{i_q}$ has been preserved under the permutation P.

Proof of Statement (2)

Assume that on the maps for the original counter state sequence table, the $x_1x_2\ldots x_n$ square and the $x_1'x_2'\ldots x_n'$ square are adjacent in the Karnaugh map sense, that is, $x_1x_2\ldots x_n$ and $x_1'x_2'\ldots x_n'$ differ in the value of exactly one digit. Assume that the difference is in the value of the j^{th} digit--$x_m = x_m'$ for all m except j. Since the permutation merely rearranges the digit order and does not change the individual digit values, it follows that $x_{i_m} = x_{i_m}'$ for all m except k. Then because $x_{i_1}x_{i_2}\ldots x_{i_n}$ and $x_{i_1}'x_{i_2}'\ldots x_{i_n}'$ differ in exactly one digit value, the associated squares must be adjacent (in the Karnaugh map sense) on the maps for the rearranged counter table.

Now assume that on one transition map, the $x_1x_2\ldots x_n$ square contains the entry e_1, and the adjacent $x_1'x_2'\ldots x_n'$ square contains the entry e_1'. Assume that on a second transition map, e_2 is entered in the $x_1x_2\ldots x_n$ square, and e_2' is entered in the $x_1'x_2'\ldots x_n'$ square. The proof of statement (1) ensures that the individual correspondences between

e_1 and e_2 and between e_1' and e_2' will be preserved under the permutation P. The preceding paragraph indicates that the adjacency of the two squares will be maintained by P. It follows that if a pair of adjacent entries on one transition map and a pair of adjacent entries on a second map are located in squares corresponding to the same initial states, this correspondence is preserved by the permutation. Since this conclusion can be applied to <u>any</u> adjacent pair of entries on a map, it can be applied successively to each adjacent pair of a group of entries. Thus, if, for a given arrangement of digit positions, a group of adjacent entries on one transition map and an equal number of adjacent entries on a second map are located in squares corresponding to the same initial states, this correspondence between the two groups will be preserved by the permutation.

<u>Proof Statement (3)</u>

The proof of statement (3) follows from the proof of statement (1). There it was demonstrated that if e_1 is entered in the $x_1x_2\ldots x_n$ square of the map for X_j, then e_1 will be entered in the $P(x_1x_2\ldots x_n) = x_{i_1}x_{i_2}\ldots x_{i_n}$ square on the map for $X_{i_k} = X_j$. Since this fact is true for every

type of entry and every square, it follows that the number of occurrences of each entry on each map remains constant under the permutation.

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