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A COMPUTER PROGRAM TO EVALUATE THE EFFECTIVENESS OF PCM FRAME SYNCHRONIZATION STRATEGIES

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ABSTRACT

This paper describes a computer program which simulates the PCM (Pulse Code Modulation) conversion equipment, and through the Monte Carlo technique measures the effectiveness of a given strategy for the equipment control settings for a given satellite. Rather than testing all possible 24,576 strategies, a manual elimination method is described for reducing the number of strategies to be tested to a feasible number. In addition to evaluating strategies for the conversion process, the program can be used to evaluate proposed modifications to the conversion equipment presently in use, and can also aid in determining the size of the frame identifier for the telemetry systems of future PCM satellites.

Author

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INTRODUCTION

General

Satellite telemetry data are recorded on magnetic tapes at a world-wide network of stations. These magnetic tapes are sent to GSFC, or more specifically, to the Data Processing Branch within GSFC, for processing. These data can be termed raw analog data. The processed product, in the form of a digital magnetic tape, is sent to the satellite experimenters for final processing and analysis. A vital step between the receipt of the raw analog data tapes and the shipment of processed digital tapes is the analog-to-digital conversion process. Special equipment known as STARS (Satellite Telemetry Automatic Reduction Systems) lines are used for this operation. The analog-to-digital conversion process dictates both the amount and the fidelity of the data that are provided to the experimenter, from the total amount of data captured from the satellite by the world-wide acquisition network. Of course, if the quality of the raw data tapes is poor because of atmospheric noise conditions or otherwise, the conversion process cannot improve the usefulness of the data. On the other hand, a continuous effort is made to insure that as many usable data are extracted from the raw data tapes as is permitted by the present state of the art.

Two major types of telemetry systems are employed for GSFC satellites - Pulse Code Modulation (PCM) and Pulsed Frequency Modulation (PFM). Different conversion processes are used in each case. Only the PCM data conversion is covered herein. Simply stated, PCM data conversion consists of three steps: bit synchronization, signal conditioning, and frame synchronization. These functions are described next, but it is the last step; namely, frame synchronization, and more pointedly, the strategy used for frame synchronization, to which this paper is primarily directed.

PCM Conversion Process

The raw analog tape contains a continuous stream of bits. This bit stream in turn is comprised of multiplexed sets of experimenter data channels (typically 8 or 9 bits per channel). Each

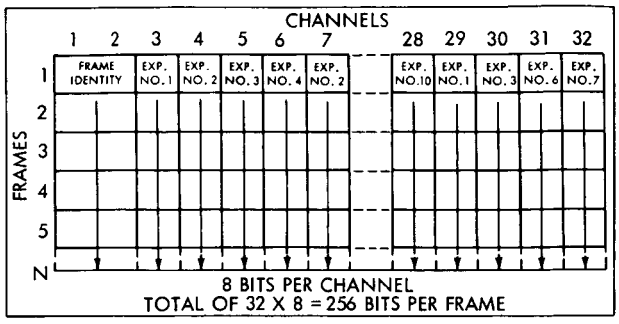

Figure 1—Example of a 32 channel telemetry format (exp. no. refers to data from a given experiment).

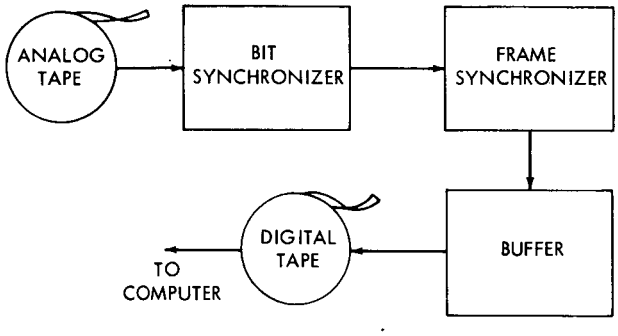

Figure 2—Simplified PCM data conversion process.

set of channels is designated a frame. Present satellite telemetry formats vary from 32 channels per frame up to 128. An example of a 32 channel format is given in Figure 1.

One analog tape contains thousands of frames. Present in each frame, in a fixed position, is a combination of bits known as a frame identifier. Its purpose is twofold: first, it is the reference point by which the various experimenter data channels within each frame can be differentiated; second, because it is a known code, it serves as an indicator of the error rate of the data recorded on a given tape.

A simplified diagram of a typical PCM conversion process is given in Figure 2. Data from the analog tape, in the form of a continuous bit stream corrupted by noise, are fed into the bit synchronizer. After bit synchronization is established a determination is made whether each bit is a one or a zero. After this determination, the reconstructed bit is fed into a frame synchronizer. The function of the frame synchronizer is to recognize the presence of the frame identifier within each frame of data.

The hardware in the STARS I line presently utilized to perform the frame synchronization (i.e. recognize the frame identifier), operates in three modes: search, verify, and lock. The search and verify modes are used to establish frame synchronization. The data examined by the system when these two modes are in operation, are lost to the experimenters. Once frame synchronization has been established the lock mode is entered. All the data processed when the lock mode is in operation are recorded on a digital tape for computer processing and subsequent shipment to the experimenters. A brief description of the frame synchronization logic system within each of the three modes of operation is given in Appendix C.

Frame Synchronization Strategy

The frame synchronizer has a number of controls with settings that can be varied by means of a patchboard. These controls are as follows:

1. Allowable number of errors - search mode
2. Allowable number of errors - verify mode
3. Allowable number of errors - lock mode

4. Correct verify counter (predetermined maximum)
5. Incorrect verify counter (predetermined maximum)
6. Correct lock counter (predetermined maximum)
7. Incorrect lock counter (predetermined maximum)

In general, a strategy consists of a set of values for the seven above mentioned controls. In the case of STARS I line, however, there is a number of equipment design restrictions to the strategy. These restrictions are as follows:

1. The value for the allowable number of errors in each of the three modes must be equal.
2. The allowable number of errors must be a discrete value of from 0 to 5.
3. The predetermined maximum value for the correct verify counter must be equal to that of the correct lock counter.
4. The predetermined maximum for all counters must be a discrete value of from 1 to 16.

As a result of the above restrictions, a strategy as it pertains to the STARS I line consists of a set of four values shown in Table 1.

Table 1

Strategy of STARS I Line.

Controls	Value Limits	
	Minimum	Maximum
Allowable number of errors (search, verify, lock)	0	5
Correct verify counter, correct lock counter - predetermined maximum	1	16
Incorrect verify counter - predetermined maximum	1	16
Incorrect lock counter - predetermined maximum	1	16

Two types of errors can occur in seeking to establish and maintain frame synchronization. One is where the actual combination of bits recorded on tape for frame identification purposes is not recognized as such when fed into the STARS line. The second type of error refers to wrongfully designating a combination of bits as the frame identifier. Errors of the first type are dependent upon the bit error rate present in the data, the length of the frame identifier, and the number of allowable errors. Errors of the second type are independent of the bit error rate but do depend on the length of the frame identifier, the number of bits per frame, and the bit pattern chosen for the frame identifier.

It might appear that our objective should be to minimize both types of errors and at the same time recover the maximum amount of correct data. Unfortunately this is not possible since the one objective works against the other.

Due to the many interacting factors involved, the problem of formulating the equations and performing the calculations necessary to arrive at the optimum strategy is a formidable one. Another approach, however, is to develop a computer program which would simulate the logic of the STARS line regarding frame synchronization. Then, on a trial by trial basis, each strategy can be tested by the computer program, using Monte Carlo techniques for simulating random data and for simulating the occurrence of pertinent factors such as bit slippage and bit errors. This approach was taken, and the computer program developed for this purpose is the subject of this paper.

Strategy Effectiveness

In the case of the STARS I line, there are 24,576 possible strategies. The question arises as to which is the best strategy. To resolve this question it is desirable to compare different strategies in terms of a meaningful measure. One such measure is the Frame Recovery Rate (FRR), defined below:

$$FRR = \frac{F_{L,S}}{F_{L,S} + F_{L,\bar{S}} + F_S + F_V} \times 100 = \frac{F_{L,S}}{F_T} \times 100,$$

where

F_T = Total number of frames processed.

$F_{L,S}$ = The number of frames processed in the lock mode while correctly synchronized.

$F_{L,\bar{S}}$ = The number of frames processed in the lock mode while incorrectly synchronized.

F_S = The number of frames processed in the search mode.

F_V = The number of frames processed in the verify mode.

Using the measure of effectiveness, FRR, that strategy which provides the highest value of FRR would be the optimum frame synchronization strategy for the given satellite. It would then be expected that this strategy would recover a greater amount of correctly synchronized data than any other strategy.

DESCRIPTION OF THE COMPUTER PROGRAM (SIMPCM)

SIMPCM is a general purpose computer program designed for simulating and evaluating PCM frame synchronization strategies. The operation of SIMPCM can be thought of as being divided into four steps as follows:

1. Input of specified values for variable parameters

For each test it is necessary to input to the program by means of punch cards, desired values for 15 different parameters. The titles of these parameters along with the range of values acceptable to the program are shown in Table 2.

2. Generation of simulated PCM data

Frames of binary data are generated by the computer. The values of B_f and B_i are specified on input cards prior to the start of a run. Data bits ($B_f - B_i$ bits per frame) are generated by a pseudo random number generator with each bit having an equal probability of being a zero or one. The frame identifier bits are generated in two phases. First, the computer generates a sequence

Table 2

Parameters and Value Ranges for SIMPCM.

Parameter Titles	Value Limits	
	Lower	Upper
B_f (number of bits per frame)	1	10^5
B_i (number of bits in frame identifier)	1	10^8
Bit configuration of nominal frame identifier	0	2^{B_i}
Bit error rate	0	1.0
Slippage rate*	0	1.0
Allowable errors in search	0	B_i
Allowable errors in verify	0	B_i
Allowable errors in lock	0	B_i
Correct verify counter - predetermined maximum	1	10^5
Incorrect verify counter - predetermined maximum	1	10^5
Correct lock counter - predetermined maximum	1	10^5
Incorrect lock counter - predetermined maximum	1	10^5
Maximum slippage	0	$B_f/2$
Maximum number of frames to be scanned (when this value is attained, the run automatically ends).	1	10^7
Maximum combined search and verify frames (when this value is attained, the run automatically ends).	1	10^7

*Normally the beginning of the frame identifier of a given frame is found B_f bits after the beginning of the frame identifier of the previous frame. When the true frame identifier is located in a position other than B_f bits following the frame identifier of the previous frame, slippage is said to have occurred. The slippage rate is equal to the number of frames in a file in which slippage occurred, multiplied by 100 and divided by the total number of frames in the file.

of bits identical to the configuration of the nominal frame identifier as specified on the input card. A change or no change decision is then made on each bit in the frame identifier on the basis of a random number between 0 and 1 (generated by a pseudo random number generator) and the bit error rate specified on the input card. If, for example, the bit error rate specified on the input card was 0.01, a given bit would be changed if the random number relating to that bit was between 0 and 0.010000. The bit would not be changed if the random number was between 0.010001 and 1.0. After a frame of data is generated, it is subjected to a slippage or no slippage decision. This decision is made on the basis of a random number between 0 and 1 (generated by a pseudo random number generator) and the slippage rate specified on the input card and is performed in a manner similar to that just described for the frame identifier bit change or no change decision. If the decision for a given frame is slippage, then a sub-routine (which utilizes the pseudo random number generator and the maximum slippage specified on the input card) determines the amount of slippage, the direction of slippage and the location within the frame of the slippage.

3. Simulation of synchronizer logic

SIMPCM utilizes the synchronizer logic system and the strategy specified by the input parameters to analyze the simulated data previously generated by SIMPCM. Decisions are made as to the appropriate mode of operation (search, verify or lock). Once having determined the appropriate mode of operation, SIMPCM simulates the performance of that mode of operation until the decision is made to change to a different mode of operation. A detailed flowchart of the manner in which the synchronizer logic is simulated by SIMPCM is contained in Appendix D.

4. Tabulation and summary of results

As the simulated data are analyzed by the simulated synchronizer logic, a tabulation is produced of: the total number of frames processed in the search mode (F_S); the number of frames processed in the verify mode (F_V); the number of frames processed in the lock mode while correctly synchronized ($F_{L,S}$); and the number of frames processed in the lock mode while incorrectly synchronized ($F_{L,\overline{S}}$).* These tabulated values are utilized to compute the frame recovery rate. In addition, there are other tabulations produced which provide supplementary information. These tabulations count the occurrences of the various types of mode change, and are described in Appendix B.

COMPUTER TIME REQUIREMENT

The amount of UNIVAC 1107 computer time required for a given run can be estimated by:

$$T = 1 + (F_S + F_V)\,\frac{(B_f)}{1,200} + \frac{F_L}{4,000},$$

where

T = time in seconds.

F_S = number of frames processed in search.

F_V = number of frames processed in verify.

B_f = number of bits per frame.

F_L = number of frames processed in lock.

Two variable input parameters are provided to limit the computer time requirement for any given run. One of the parameters is the maximum value for total number of frames processed (F_T). The second parameter is the maximum value for the number of frames processed in the search and verify modes ($F_S + F_V$). When either of these two maxima is reached, the run ends and the output is printed.

*Includes those frames which were processed in part while correctly synchronized and in part while incorrectly synchronized.

APPLICATIONS OF SIMPCM

Determination of Optimum Strategy

SIMPCM was used to determine the optimum strategy for processing OGO-A and OSO-B2 data. The 1107 computer time requirement to do this would have been prohibitive if all possible strategies (24,576) were to be evaluated for the seven data quality conditions that were of interest. It was therefore necessary to follow a plan which would result in the identification of the optimum or near optimum strategy, but which would require only a small percentage of the total ($24,576 \times 7 = 172,032$) possible runs. This was accomplished by means of a hill-climbing technique which was used as the basis for selecting strategies for evaluation. The strategies so selected were all evaluated under worst-case data quality conditions where worst-case was considered to be bit error rate = 0.10, slippage rate = 0.02. The selection procedure terminated when it could be determined that the optimum and near optimum strategies were all identified. This required an evaluation of only 112 of the 24,576 possible strategies. Since it was conceivable that the strategy determined to be optimum under worst-case data quality conditions might turn out to be a poor strategy under good or excellent data quality conditions, it was necessary to perform further evaluations. The strategy determined to be optimum for the worst-case data quality condition and a few of the strategies determined to be close to optimum under these same data quality conditions were evaluated under seven sets of conditions covering a wide range of data quality. The results of these evaluations for both OGO-A and OSO-B2 showed that the strategy that was optimum under the worst-case data quality conditions was also optimum (or very close to optimum) for the entire range of data quality conditions. Appendix A presents some of the highlights of the OSO-B2 strategy evaluations.

Determination of Optimum Strategy for Future Satellites

SIMPCM will be used to determine the optimum strategy for future PCM satellites. Besides OGO-A and OSO-B2, it has provided strategies for AE-B, DME-A, B satellites, and the follow-on OGO and OSO satellites.

Evaluation of Modification to STARS Line

SIMPCM can be utilized to estimate the increase or decrease in the frame recovery rate that would result from contemplated modifications to the logic system of the STARS I line frame synchronizer. An application of this type is described as follows:

A modification to the present frame synchronization logic system was suggested. The modified system would involve only two variable parameters, whereas the present system involves four variable parameters. The proposed system calls for going from the search mode to the lock mode immediately after the first hit* in the search mode, and for going from the lock mode to the search mode immediately after the first miss† in the lock mode. The variables of the proposed

*A hit is said to have occurred when a comparison of the bit configuration in the shift register with the preset frame identifier configuration yields a number of differences equal to or less than the predetermined allowable number of errors.

†A miss is said to have occurred when a comparison of the bit configuration in the shift register with the frame identifier bit configuration yields a number of differences greater than the predetermined allowable number of errors.

system are: allowable number of errors in search, and allowable number of errors in lock. The differences between the proposed system and the present system are as follows:

1. In the present system the allowable number of errors in search must be equal to the allowable number of errors in lock and must be a discrete value of from 0 to 5. In the proposed system, there is no requirement for these values to be equal and the values can be any discrete value of from 0 to B_1 (where B_1 = the number of bits in the frame identifier).
2. Three of the four variable parameters of the present system are counter maxima. The three counters to which these counter maxima relate are:
   a. Correct verify, correct lock counter
   b. Incorrect verify counter
   c. Incorrect lock counter

Since the proposed system changes from search to lock on the basis of the first hit encountered, and changes from lock to search on the basis of the first miss encountered, there is no requirement for counters and therefore no requirement for counter maxima.

The specific problem was to determine if in processing OSO-B data, the proposed system could be expected to improve on the frame recovery rate that was being produced by the present

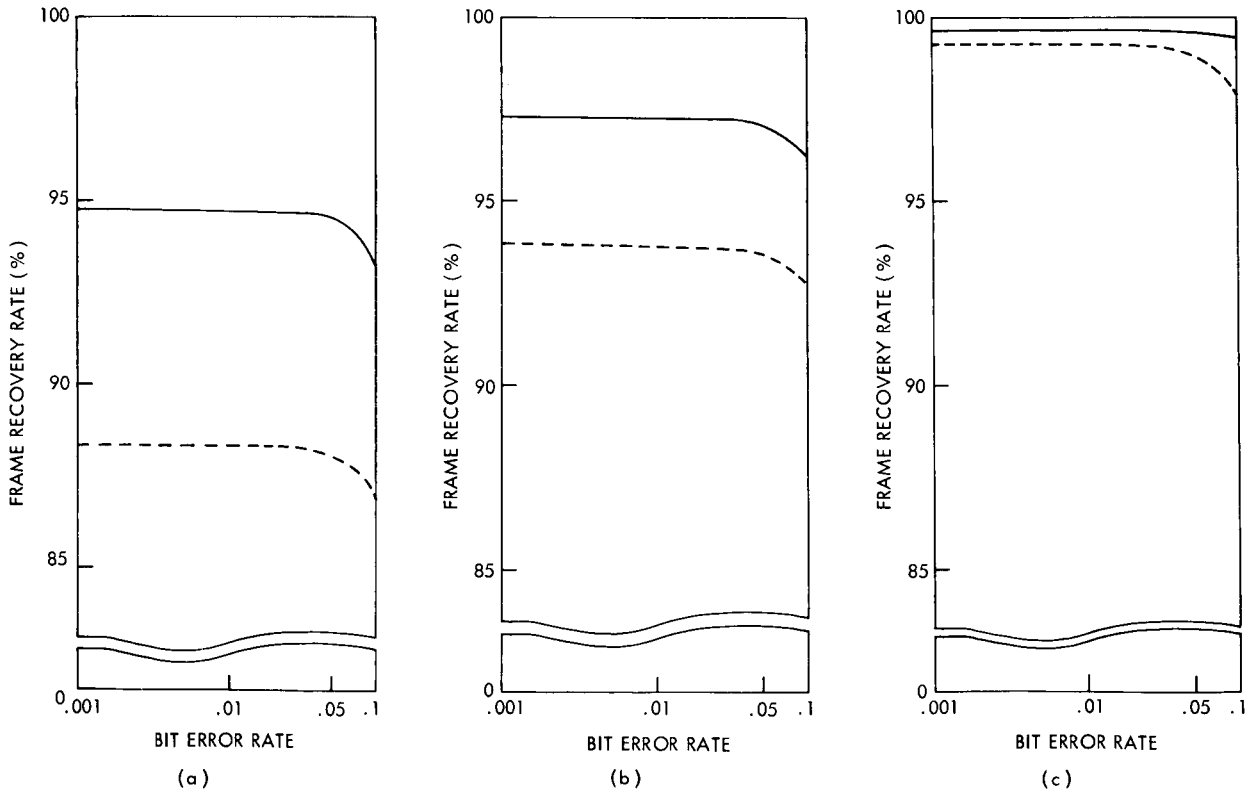

Figure 3—Frame recovery rate of a 2-variable system (——) versus a 4-variable system (----); (a) slippage rate = 0.02, (b) slippage rate = 0.01, and (c) slippage rate = 0.001.

system. The first step in providing a solution to this problem was to utilize SIMPCM to find the optimum strategy for processing OSO-B data by means of the proposed system. The next step was to compare that strategy with the optimum strategy for processing OSO-B data by means of the present system. (The optimum strategy for processing OSO-B data by means of the present system was already known as a result of a previous application of SIMPCM.) Highlights of these comparisons are contained in Figure 3.

Figure 3a shows frame recovery rates for a 0.02 slippage rate. Figure 3b shows frame recovery rates for a 0.01 slippage rate and Figure 3c for a 0.001 slippage rate. All three charts show frame recovery rates for varying bit error rates for the optimum system strategy for both the present and proposed systems.

The following can be concluded from Figure 3:

1. For all values of the bit error rate $\leq$ 0.05, the frame recovery rate is very nearly a constant. This is true for each of the three slippage rates tested (0.001, 0.01 and 0.02) and is true for both the proposed system and the present system.
2. For the entire range of slippage rates and bit error rates tested (slippage rate from 0.001 through 0.02, bit error rate from 0.001 through 0.1), the percentage of frames lost (frame loss percent = 100 percent - frame recovery rate) for the proposed system is approximately one half of the percentage of frames lost under the present system.

Determination of Values for B_i and B_f for Future Satellites

The applications of SIMPCM mentioned above, all pertained to estimating frame recovery rates for satellites with values of B_i and B_f which were already established. SIMPCM can also be used as an aid in establishing values of B_i and B_f for future satellites. A hypothetical example of this type of application is as follows:

The desired frame length B_f for some future satellite is 2304 bits (two times the value of B_f for the OGO-A satellite). The question arises as to what the length of the frame identifier (B_i) should be. Should B_i be equal to 27, 36, 45, 54, or some other number? SIMPCM can provide estimates of the frame recovery rates which would result from each of the B_i values under consideration.

Appendix A

Highlights of Results of Strategy Effectiveness Evaluation - OSO

Using parameters related to the OSO satellite, a series of computer runs was made to determine the best strategy for the present four variable system for performing the signal processing operation (i.e., the analog-to-digital conversion).

Tabulations are shown in Table A-1 for nine strategies, four of which were found to be the best or close to best for the OSO telemetry format. The remaining five strategies are presented to indicate the degradation in recovery rate that may occur from the selection of a poor strategy. Results of the four best strategies are given under six combinations of varying data quality conditions as well as the worst case condition. The five poorer strategies are only shown for the worst-case condition.

Table A-1

Tabulation of Data for OSO.

Strategy Description					Frame Recovery Rate: Estimated Percent of Frames Recovered While in Frame Sync						
Strategy Designation**	Allowable Errors - Search Verify and Lock	Correct Verify Counter, Correct Lock Counter	Incorrect Verify Counter	Incorrect Lock Counter	Data Quality Condition: Slippage Rate (SR) Bit Error Rate (BER)						
					SR = 0.0001 BER = 0.01	0.0001 0.05	0.0001 0.10	0.01 0.01	0.01 0.05	0.01 0.10	0.02* 0.10
A	1	1	1	6	99.9	99.9	98.9	92.9	92.7	90.0	83.9
B	2	1	1	4	99.9	99.9	99.2	93.8	93.6	92.3	86.7
C	2	2	2	5	99.9	99.9	99.6	92.6	92.3	91.6	85.6
D	3	2	5	3	99.9	99.9	99.6	92.5	92.4	91.5	84.7
E	0	1	1	6	-	-	-	-	-	-	62.2
F	1	1	3	6	-	-	-	-	-	-	77.8
G	2	3	1	7	-	-	-	-	-	-	74.0
H	3	2	1	4	-	-	-	-	-	-	57.1
I	4	1	1	3	-	-	-	-	-	-	62.6

*Worst-case condition of all combinations tested.

**Strategies A, B, C, and D were determined to be the best strategies under the worst-case data quality conditions (slippage rate = 0.02, bit error rate = 0.10). Strategies E, F, G, H, and I represent a sample of all other strategies tested only under worst-case data quality conditions.

Appendix B

Description of SIMPCM Output

The basic output of the SIMPCM program is illustrated in Table B-1. The right performance factors that appear in Table B-1c are defined below. The notation used in these definitions is as follows.

$F_T = F_S + F_V + F_L$ = Total number of frames processed

F_S = Number of frames processed in the search mode

F_V = Number of frames processed in the verify mode

$F_L = F_{L,S} + F_{L,\bar{S}}$ = Number of frames processed in the lock mode

$F_{L,S}$ = Number of frames processed in the lock mode while correctly synchronized

$F_{L,\bar{S}}$ = Number of frames processed in the lock mode while out of synchronization (including partially correct* frames)

$F_{L,\bar{S}*}$ = Number of frames processed in the lock mode while out of synchronization (excluding partially correct frames)

$E_S = S_A - S_T$ = Actual minus theoretical number of slips occurring during the lock mode (correctly synchronized)

S_A = Actual number of slips that occurred in the lock mode while the system was correctly synchronized

S_T = Slippage rate × ($F_{L,S}$ + the number of partially correct frames)

M = Predetermined maximum for the incorrect lock counter

$N_{L,\bar{S}}$ = Number of entries to the lock mode while out of synchronization

$N_{L,S}$ = Number of entries to the lock mode, while correctly synchronized

Each of the eight performance factors is defined below. The order in which they are presented corresponds to the number appearing in Table B-1c.

1. Frames recovered correctly as a percent of total frames (unadjusted),

$$\frac{F_{L,S}}{F_T} \times 100 .$$

*A partially correct frame is one which was processed in part while correctly synchronized and in part while incorrectly synchronized. (This will occur for a given frame when that frame is being processed in the lock mode while correctly synchronized and slippage occurs while the frame is being processed.)

Table B-1

Main Output of SIMPCM.

B-1a

Total Frames Processed.

Mode of Operation	No. of Frames
Search	523.0
Verify	0.0
Lock	9,677.0
TOTAL	10,200.0

B-1b

Frame Error Distribution for Frames in Lock.

No. Of Errors In Frame Identifier	Total No. of Frames In Lock	No. of Frames in Lock, Where:		
		Complete Frame Was In Sync	Part of Frame Was In Sync	Complete Frame Was Out Of Sync
0	1,728	1,692	36	0
1	3,024	2,961	63	0
2	2,484	2,438	46	0
3	1,280	1,244	36	0
4	472	454	14	4
5 or more	689	136	4	549
TOTAL	9,677	8,925	199	553

B-1c

Summary Performance.

Performance Factor	Percentage
1	87.500
2	92.922
3	5.127
4	7.771
5	88.396
6	93.626
7	87.512
8	88.408

2. Frames recovered correctly as a percent of total frames (adjusted for slippage correction),

$$\frac{F_{L,S} + F_{L,\bar{S}*}}{F_T} \times 100 .$$

3. Frames in search and verify as a percent of total frames (unadjusted),

$$\frac{F_S + F_v}{F_T} \times 100 .$$

4. Frames recovered incorrectly as a percent of frames recovered (unadjusted),

$$\frac{F_{L,\bar{S}}}{F_L} \times 100 .$$

5. Frames recovered correctly as a percent of total frames (adjusted for slippage sampling variation),

$$\frac{F_{L,S} + E_S \left(\frac{F_S + F_V + MN_{L,\bar{S}}}{N_{L,S} + \frac{1}{2}} + M + 1 \right)}{F_T} \times 100$$

6. Frames recovered correctly as a percent of total frames (adjusted for slippage correction and adjusted for slippage sampling variation)

$$\frac{F_{L,S} + F_{L,\bar{S}*} + E_S\left(\frac{F_S + F_V + MN_{L,\bar{S}}}{N_{L,S} + \frac{1}{2}} + 1\right)}{F_T} \times 100 .$$

7. Frames recovered correctly as a percent of total frames (adjusted for bias due to termination of run in the search and verify mode)

$$\frac{F_{L,S}}{F_T - .5\left(\frac{F_S + F_V + MN_{L,\bar{S}}}{N_{L,S} + \frac{1}{2}}\right)} \times 100 .$$

8. Frames recovered correctly as a percent of total frames (adjusted for slippage sampling variation and adjusted for bias due to termination of run in the search or verify mode),

$$\frac{F_{L,S} + E_S\left(\frac{F_S + F_V + MN_{L,\bar{S}}}{N_{L,S} + \frac{1}{2}} + M + 1\right)}{F_T - .5\left(\frac{F_S + F_V + MN_{L,\bar{S}}}{N_{L,S} + \frac{1}{2}}\right)} \times 100 .$$

Factors 2, 5, 6, 7, and 8 reflect one or more of three adjustments, each of which is described below.

1. *Slippage correction adjustment* - In processing actual satellite telemetry data, it is possible to have the computer program detect and correct for frame slippage which occurred during the analog-to-digital conversion. The slippage correction adjustment factor modifies the unadjusted frame recovery rate to reflect the assumption that all totally incorrect frames that are recovered will be corrected by the computer program and therefore should be counted as frames recovered correctly.

2. *Slippage sampling variation adjustment* - The actual slippage rate for a given run will deviate from the input slippage rate due to sampling error. The slippage sampling variation adjustment normalizes the frame recovery rate so as to remove most of the effect of the sampling error.

3. *Adjustment for bias due to termination of run in the search or verify mode* - Under SIMPCM a run is programmed to terminate when either the total frames reaches a given maximum or

when the frames in search and verify reaches a given maximum. Because of this feature of SIMPCM, the frame recovery rate is subjected to a bias. When the run terminates in the lock mode, the frame recovery rate is biased upward. However, this bias is negligible and no bias correction procedure is provided. When the run terminates in the search or verify mode, the frame recovery rate is biased downward. This bias can be of some significance and an adjustment procedure is therefore provided.

In addition to the information shown in Table B-1, SIMPCM also provides supplementary output information as shown in Tables B-2 through B-6. These tables contain tabulations in terms of the number of instances that specific types of mode changes that occurred and the average number of frames processed in a given mode of operation before shifting to another mode of operation.

The terminologies used in these tables are:

1. Correct verify - Entries to the verify mode following a correct recognition of the frame identifier in the search mode
2. Incorrect verify - Entries to the verify mode following the incorrect identification of the frame identifier in the search mode
3. Correct search - The initial entry to the search mode for a given run or, entries to the search mode which follow
   a. An incorrect entry to the verify mode
   b. A slippage that occurs in the verify mode
   c. An incorrect entry to the lock mode
   d. A slippage that occurs in the lock mode
4. Incorrect search - Entries to the search mode which follow
   a. A correct entry to the verify mode with no slippage occurring while in the verify mode
   b. A correct entry to the lock mode with no slippage occurring while in the lock mode
5. Correct lock - Entries to the lock mode which follow
   a. A correct recognition of the frame identifier in the verify mode
   b. A correct recognition of the frame identifier in the search mode for those strategies that do not call for a verification mode
6. Incorrect lock - Entries to the lock mode which follow
   a. An incorrect recognition of the frame identifier in the verify mode
   b. An incorrect recognition of the frame identifier in the search mode for those strategies that do not call for a verification mode

It should be noted that Tables B-2, B-3 and B-4 will contain all zeros when the correct verify counter - predetermined maximum is 1. For all values other than 1, Table B-6 will contain all zeros. The data presented in Tables B-2 through B-6 are based on a case where the correct verify counter is set to 1.

Table B-2

Search To Verify.

	Correct Search		Incorrect Search		Total	
	No. of Times	Avg. No. of Frames	No. of Times	Avg. No. of Frames	No. of Times	Avg. No. of Frames
Correct Verify	0	0.0	0	0.0	0	0.0
Incorrect Verify	0	0.0	0	0.0	0	0.0
TOTAL	0	0.0	0	0.0	0	0.0

Table B-3

Verify To Search.

	Correct Verify		Incorrect Verify		Total	
	No. of Times	Avg. No. of Frames	No. of Times	Avg. No. of Frames	No. of Times	Avg. No. of Frames
Correct Search	0	0.0	0	0.0	0	0.0
Incorrect Search	0	0.0	0	0.0	0	0.0
TOTAL	0	0.0	0	0.0	0	0.0

Table B-4

Verify To Lock.

	Correct Verify		Incorrect Verify		Total	
	No. of Times	Avg. No. of Frames	No. of Times	Avg. No. of Frames	No. of Times	Avg. No. of Frames
Correct Lock	0	0.0	0	0.0	0	0.0
Incorrect Lock	0	0.0	0	0.0	0	0.0
TOTAL	0	0.0	0	0.0	0	0.0

Table B-5

Lock To Search.

	Correct Lock		Incorrect Lock		Total	
	No. of Times	Avg. No. of Frames	No. of Times	Avg. No. of Frames	No. of Times	Avg. No. of Frames
Correct Search	202	47.6	20	3.1	222	43.6
Incorrect Search	0	0.0	0	0.0	0	0
TOTAL	202	47.6	20	3.1	222	43.6

Table B-6

Search To Lock.

	Correct Search		Incorrect Search		Total	
	No. of Times	Avg. No. of Frames	No. of Times	Avg. No. of Frames	No. of Times	Avg. No. of Frames
Correct Lock	202	1.9	0	0.0	202	1.9
Incorrect Lock	20	1.0	0	0.0	20	1.0
TOTAL	222	1.8	0	0.0	222	1.8

Appendix C

Description of Frame Synchronization Logic System Within Each of the Three Modes of Operation

SEARCH MODE

The output from the bit synchronizer, bit by bit, is fed into a shift register which holds a number of bits equal to B_i (where B_i = the number of bits in the frame identifier). A comparison is made each bit time, of the bit configuration in the shift register with the frame identifier nominal bit configuration. This process continues until a hit* occurs, at which time the verify mode is entered. (The verify mode can be programmed to be bypassed so that the lock mode can be entered directly from the search mode.

VERIFY MODE

The procedure for comparing the contents of the shift register with the frame identifier after each single bit shift continues as in the search mode. In the verify mode, however, two counters, the correct verify counter and the incorrect verify counter, are active. (The correct verify counter is initially set to 1 and the incorrect verify counter is initially set to 0). When a miss† occurs, neither of the two counters is incremented. Each time a hit occurs, a 1 is added to either the correct verify counter or to the incorrect verify counter. The 1 is added to the correct verify counter when the hit occurs exactly B_f bits (where B_f is the number of bits per frame), or a multiple of B_f bits from the bit position at which the search mode hit occurred. When the hit occurs at any other bit position, the 1 is added to the incorrect verify counter. If the incorrect verify counter reaches its predetermined maximum before the correct verify counter, the system reverts to the search mode. If the predetermined maximum for the correct verify counter is reached first, the system switches to the lock mode.

LOCK MODE

Unlike the search and verify modes, comparisons in the lock mode between the contents of the shift register and the frame identifier are made only once per frame rather than B_f times per frame. The comparisons are made at each multiple of B_f bits from the bit position at which the

*A hit is said to have occurred when a comparison of the bit configuration in the shift register with the preset frame identifier configuration yields a number of differences equal to or less than the predetermined allowable number of errors.

†A miss is said to have occurred when a comparison of the bit configuration in the shift register with the frame identifier bit configuration yields a number of differences greater than the predetermined allowable number of errors.

search mode hit occurred. Two counters, the correct lock counter and the incorrect lock counter are active. Each time a hit occurs, the correct lock counter is incremented by 1. Each time a miss occurs, the incorrect lock counter is incremented by 1. If the incorrect lock counter reaches its predetermined maximum first, the system reverts to the search mode. If the correct lock counter reaches its predetermined maximum first, both counters are reset to 0 and the system continues in the lock mode.

Appendix D

SIMPCM Logic Flowchart

This Appendix contains a prose type of flowchart Figure D-1a, b and c which portrays the manner in which the frame synchronizer logic is simulated by SIMPCM. Definitions of terms used in the flowchart are

BP - Expected percentage of bits in error

SP - Expected percentage of frames with slippage

Scan position C - The actual bit position within the current frame

Scan position H - The hardware determined bit position within the current frame. When scan position H agrees with scan position C, the system is in-sync.

Sync Word Compare - A count of discrepancies between the correct sync and the sync-word-length bite lying at scan position C

Generated frame of data - A set of binary bits is formed by

1. Taking the actual sync-word and changing some of the bits. This is done by generating for each bit a random number between 0 and 1. Whenever the random number is less than BP, the bit is changed.
2. Completing the frame with random bits allowing each bit equal probability of being 0 or 1.

Slippage - This is defined as the occurrence of the frame sync identifier in other than B_f bits from the occurrence of the preceding frame sync identifier. B_f is the number of bits in a frame. It is simulated for each frame by generating a random number to determine if slippage occurs in the frame. If the random number is less than SP, slippage is applied to that frame. Both the amount and the direction of slippage are also determined by the random number generator technique.

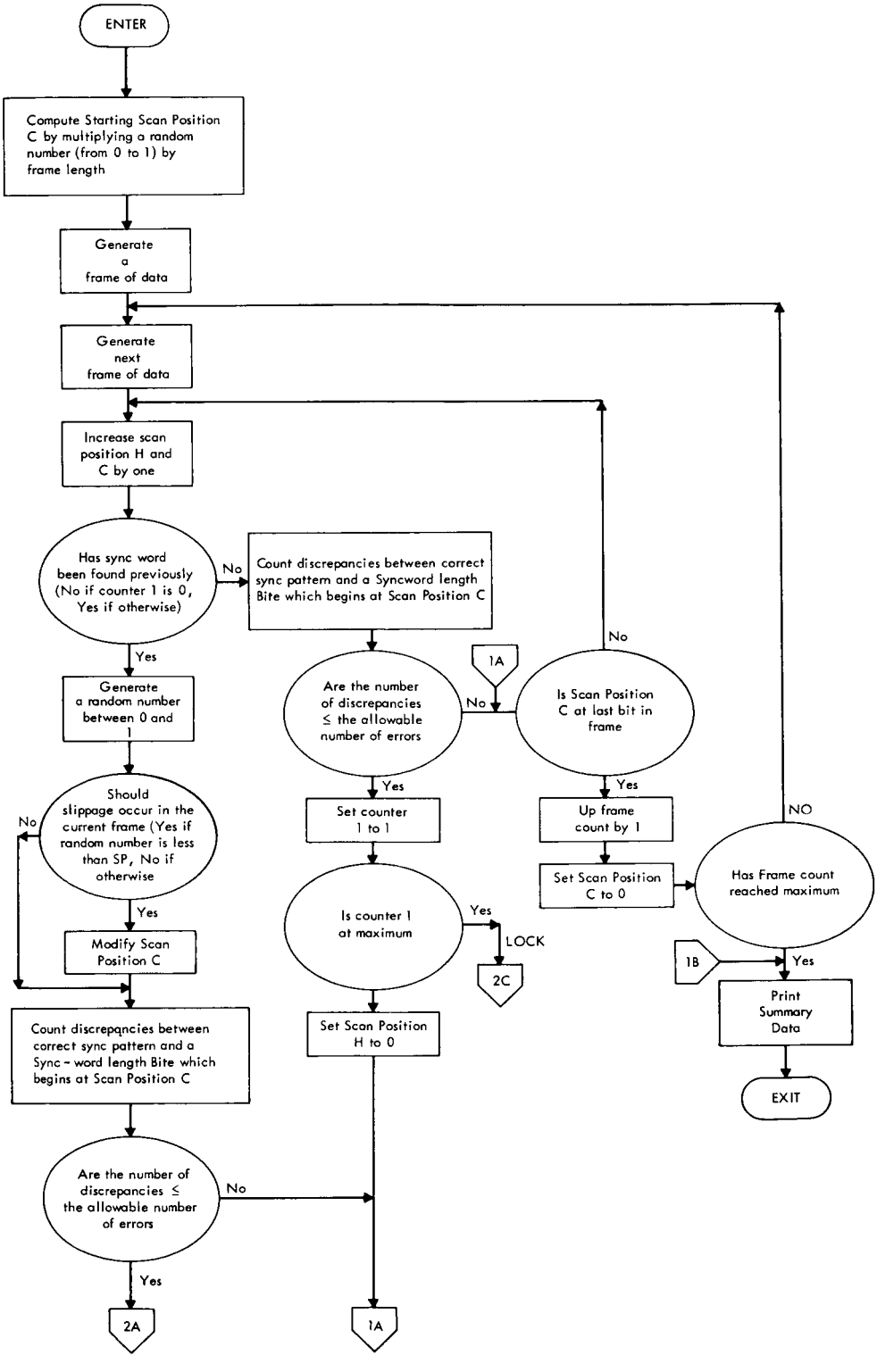

Figure D-1a—SIMPCM logic flowchart.

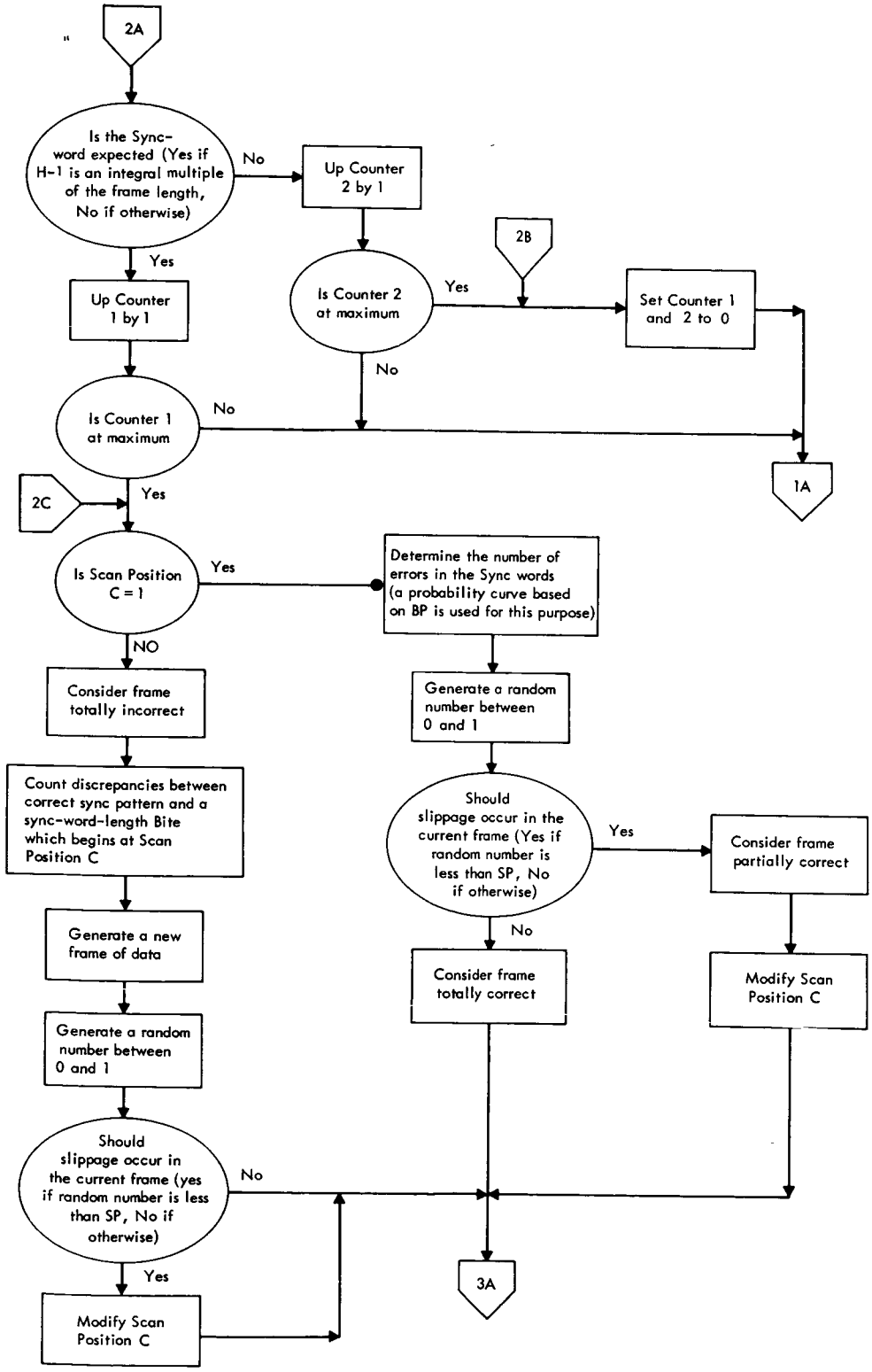

Figure D-1b—SIMPCM logic flowchart.

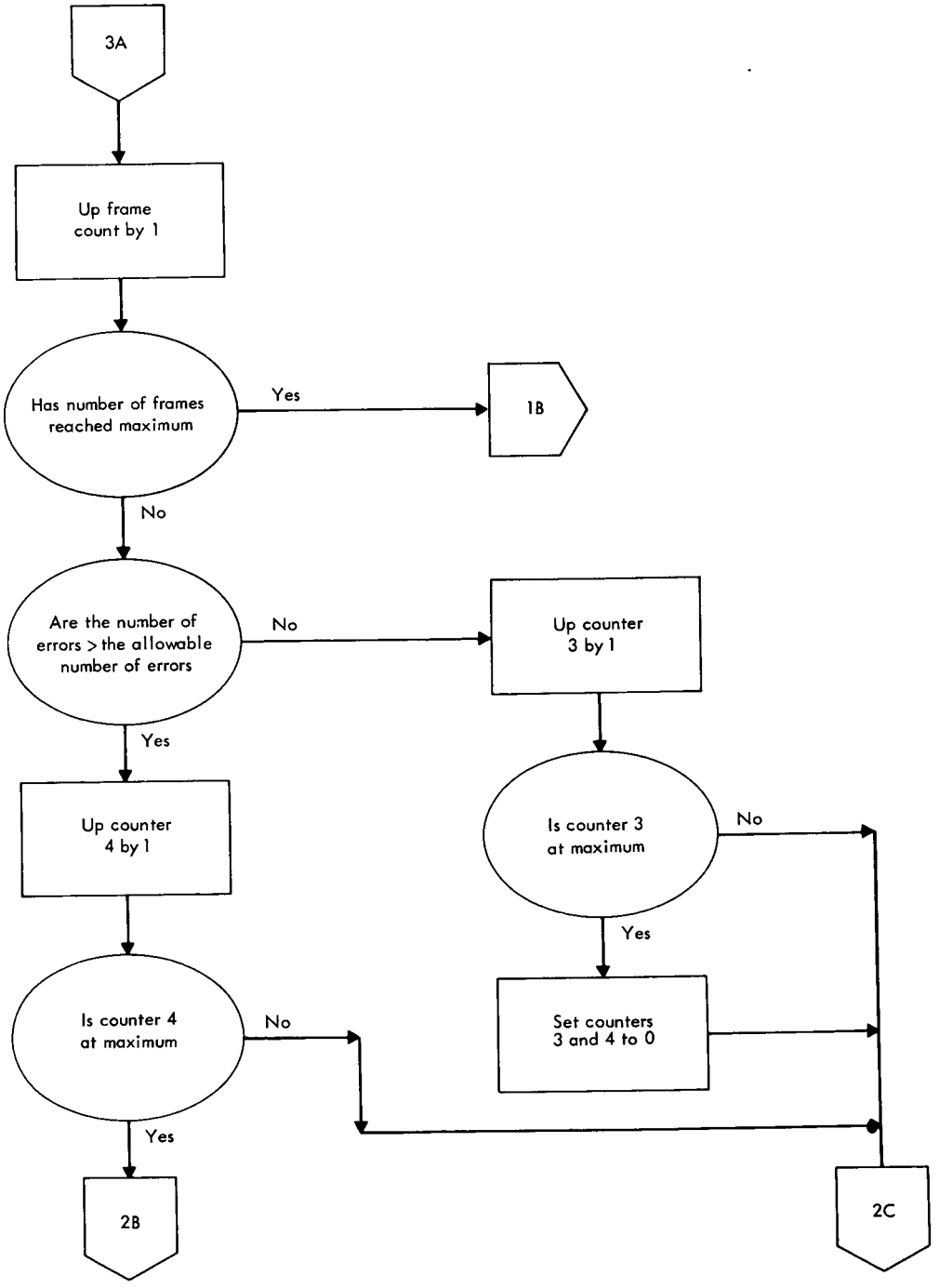

Figure D-1c—SIMPCM logic flowchart.

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