FINAL REPORT

FOR

METAL OXIDE SEMICONDUCTOR (MOS) TRANSISTOR RESEARCH AND DEVELOPMENT PROGRAM

PART II - DEVELOPMENT OF STABLE COMPLEMENTARY MOS FIELD EFFECT TRANSISTORS

March 1965 - November 1965

NAS 5-3758

Prepared By

WESTINGHOUSE ELECTRIC CORPORATION
DEFENSE AND SPACE CENTER
AEROSPACE DIVISION

For

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND

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1.0 INTRODUCTION AND SUMMARY

The objective of the MOS FET Research and Development Program initiated in March 1965 was to provide stable N and P channel units using processing techniques compatible with the fabrication of complementary MOS FET monolithic functional blocks. The work was funded by GSFC-NASA under the following contract and task numbers:

Contract No. NAS 5-3758

Proc. Control No.	W. G.O. No.
670-W46787	A51248BA
670-W46786	A51248AZ
670-W46753	A51248AW
670-W46752	A51248AY

Under these tasks Westinghouse was required to deliver stable N and P channel MOS FETs and the detailed process specifications required to fabricate the units. Also process specifications for monolithic complementary MOS FET using both junction and dielectric isolation were required.

The report entitled "MOS FET Research and Development Program, Part 1" covers the initial phase of work carried out under this program.

A process for the simultaneous fabrication of complementary enhancement mode MOS transistors in epitaxial material has been developed. The turn on voltages at 10 μa drain to source current is typically +1.5 volts for the N channel and 4.8 volts for the P channel MOS FETs. Stable N and P channel units were delivered November 4, 1965. The process specifications and stability data are enclosed in this report.

2.0 TECHNICAL DISCUSSION

2.1 MOS FET Design Considerations

2.1.1 Mask Design

In the early part of the program, frequency response or switching speed was not of primary concern but rather, the goal was ease of fabrication with readily defined dimensions. An annular configuration was chosen so that no surface channel paths would enter into the results other than between the source and drain. The dimensions of importance are shown in Table 1 for the device shown in Figure 2.1.

Channel Width	ω/l	Areas (less contact pads) Gate	Drain Source
0.5 mil	76	58 $mils^2$	75 mil^2 150 $mils^2$
1.0 mil	40	82 $mils^2$	75 mil^2 160 $mils^2$

Table 2.1

Masks for a new unit have been fabricated which have dimensions reduced by a factor of two. These new units have line widths and spacings of 0.25 mil and have areas one fourth that of the original design. The masks were also designed such that complementary units could be fabricated without making additional mask designs.

2.1.2 Review of MOS FET Theory

The basic theory of MOS FETs is reviewed briefly to point out the major factors involved in the design. Given first is the threshold voltage (V_T) which is the gate voltage which corresponds to the onset of inversion at the surface or which corresponds to the onset of current flow through the surface channel.[1,2]

$$V_T = -q \frac{(N_{ss} \pm N_B)}{K_o \epsilon_o} \cdot t_{ox} + \phi_{ms}$$

where q = electronic charge

K_o = dielectric constant of the oxide

ϵ_o = permittivity of free space

t_{ox} = oxide thickness

N_{ss} = surface state charge

N_B = bulk charge contribution (+ for N type substrate thus for p channel MOS FETs)

ϕ_{ms} = metal-semiconductor work function

The channel conductance with no bias on the source and drain is

$$g_{ds} = \left.\frac{I_{ds}}{V_{ds}}\right|_{V_{gs}} = \frac{\bar{\mu} k_o \epsilon_o w_c}{t_{ox} l_c} (V_{gs} - V_T)$$

The transconductance in the region beyond current pinch off is

$$g_m = \left.\frac{I_{ds}}{V_g}\right|_{V_d} = \frac{\bar{\mu} k_o \epsilon_o w_c}{t_{ox} l_c} (V_{gs} - V_T)$$

It is seen that for the conditions specified above

$$g_m = g_{ds}$$

Both of these expressions have been used to calculate the channel effective mobility $\bar{\mu}$ from the measured values of g_m and g_{ds}. Clearly, those factors that increase the transconductance decrease the drain to source resistance for the conditions given.

The threshold voltage (V_T) may be determined from the expression for the channel conductance (g_{sd}) for $V_d < (V_{gs} - V_T)$ or it may be determined from the expression for the drain current in the pinch off region as shown below.

$$I_{ds} = \frac{\bar{\mu} k_o \epsilon_o w_c}{2 l_c t_{ox}} (V_{gs} - V_T)^2$$

Of course from the definition $V_{gs} = V_T$ when I_{DS} or g_{DS} is equal to zero. In practice, the gate voltage to achieve 10 μa drain to source current with the device biased in the pinch off region is normally used to characterize the turn on. This gate voltage is called the turn on voltage (V_{gst}). Further, it is general practice to let $V_{ds} = V_{gs}$ for this measurement. One obtains the transfer characteristic shown in Figure 2.2. On the C-V curve, the turn on voltage (V_{gst}) will lie closer to the capacitance minimum than the threshold voltage (V_T) as shown in Figure 2.3. See also the discussion in Part I of this report.

In the mask design, provision was made to fabricate MOS capacitors on the same wafer with the devices to eliminate difficulties in interpretation of the C-V measurements made on the transistors which is caused by the source and drain junction capacitance. The C-V curves were made to provide a direct measurement of the surface states (N_{ss}). Once one has the surface state density one may calculate the threshold voltage (V_T). It has been shown that the voltage difference between C-V curves with ideally no surface states and the case with surface states is

$$\Delta V = \phi_{ms} \frac{-q N_{ss} t_{ox}}{k_o \epsilon_o}$$

A theoretically best obtainable and a typical experimental C-V curve is shown in Figure 2.4. This voltage shift caused by the surface states corresponds to the voltage shift between the theoretically best obtainable threshold voltage V_T and those obtained experimentally as shown in the same figure.

One of the important parameters involved in the design of complementary MOS FETs is the bulk doping level ($|N_A - N_D|$). By proper choice of background doping level, one may hope to obtain matching threshold voltages for N and P channel MOS FETs. Figure 2.5 shows the threshold voltage vs. the doping lvel for $\phi_{ms} = 0$ for p channel, $\phi_{ms} = -0.7v$ for n channel, $t_{ox} = 1200\text{Å}$ and for $N_{ss} = 5 \times 10^{11}$ cm^{-2}. In the calculation, it is assumed that the surface is completely inverted so that N_B is the product of the net dopant elements per cubic centimeter and the thickness of the depletion region.

The value of N_B may be determined experimentally by observing the minimum capacitance for the high frequency C-V measurements. From this value of N_B and sheet resistivity measurements then, the mobility of the majority carriers of the bulk material may be determined. Thus, the C-V measurements combined with MOS FET measurements may be used to correlate bulk and surface mobilities of opposite carrier types in the same crystal.

2.2 Processing Considerations and Experimental Results

The fundamental approach taken in the design and fabrication of these N and P channel MOS FETs was that all of the processing steps would be compatible with the fabrication of monolithic complementary FEB's. For this reason and to eliminate starting material variations all of the studies were conducted on epitaxial material.

2.2.1 Processing Prior to Formation of Gate Oxide

In the fabrication of separate N or P channel units and complementary units, the following procedures are used.

2.2.1.1 Mechanical Polish Substrate

(10 Ω-cm N or P type)

2.2.1.2 Chemical Clean

2.2.1.3 HCl etch at 1200°C for 30 minutes.

2.2.1.4 Epitaxial deposition at 1200°C using $SiCl_4$ in hydrogen with PH_3 and B_2H_6 dopants.

Typical resistivities and thickness

P	0.2 - 0.4 Ω-cm	16 to 18 microns
N	3.5 Ω-cm	16 to 18 microns

(See reference 3,4,5 and 6 Epitaxial Procedures)

2.2.1.5 Oxidation (6000Å)

O_2 bubbled through H_2O at 90°C, oxidation temperature was 1050°C.

(See reference 7 for Oxidation Procedure)

2.2.1.6 Photoengraving of ohmic contact and/or source and drain

(See reference 8)

2.2.1.7 Clean in H_2SO_4 to remove photoresist. Then clean using hot HNO_3 and hot H_2SO_4 followed by cold and hot water rinses.

2.2.1.8 Diffusion from B_2H_6 source for source and drain of P channel and/or substrate ohmic contact of N channel.

$\rho_s < 20\ \Omega/sq.$ $X_j = 6 - 8$ fringes $t_{ox} = 4K\mathring{A}$

Deposition Temperature 1150°C	Drive In Temperature 1000°C
Deposition Time 15 minutes	Drive In Time 50 minutes
Std Atmosphere	O_2 through H_2O at 100°C

See reference 7,9

2.2.1.9 Photoengraving of ohmic contact and/or source and drain.

2.2.1.10 (Same as 2.2 1.7)

2.2.1.11 Diffusion from PH_3 source for source and/or drain of N channel and substrate ohmic contact of P channel

$\rho_s < 20\ \Omega/sq.$ $X_j = 6 - 8$ fringes $t_{ox} = 4K\mathring{A}$

Deposition Temperature 1100°C	Drive In Temperature 1000°C
Deposition Time 10 minutes	Drive In Time 50 minutes
Std Atmosphere	O_2 through H_2O at 100°C

See reference 7,9

2.2.1.12 Photoengraving of Gate Region

NOTE: Three variations were used at this point. One is to use the original oxide and etch back to the desired thickness. The second is to not use photoengraving but to strip all of the oxide from the wafer prior to the gate oxide formation. The third is to use the photoengraving technique to remove the oxide in the gate region. The latter technique was preferred since this gives thick oxides under the aluminum bonding pads. The thick

oxide (5 - 6KÅ) guarantees the full breakdown voltage of the gate oxide. The etch back technique was found to not offer any advantages over the etch thru technique.

The sheet resistivities and junction depths of the source and drain diffusions are critical especially when the distance between the source and drain is less than 0.5 mil. First, the junction depths should be kept to about 1 micron initially. Secondly, when the gate oxide is formed the final junction depth sould be kept to less than three microns. Note that if the mask spacing between source and drain is 12 microns and the final junction depth 3 microns then the resultant source to drain distance is just 6 microns or about 0.25 mil. As the source to drain distance is made smaller on the mask, the junction depth becomes more critical. For example, the transconductance will exhibit a greater spread across the wafer and the depletion layer spreading of the drain junction begins to affect both the transconductance and the source to drain breakdown voltage of the device.

2.2.2 Formation of the Gate Oxide

To determine the important factors in the formation of the gate oxide, a series of experiments was devised using MOS-capacitors. The experiments take into account the initial surface condition, oxygen vacancy distibution, segregation of the silicon dopant, thermal stress of the oxide and contamination through the presence of hydroxyl or alkali ions. The results of these experiments are contained in Part One dated 1 October 1965 of this two volume report. The results of those experiments formed the basis for the processing used on the MOS field effect transistors. Because of difficulty in obtaining correlation between the original capacitor C-V measurements and devices made using similar processing techniques several variations were made in the gate-oxide and gate-electrode processing. The most significant changes made were variations in the use of P_2O_5 glass and variations in the aluminum sintering process. It is important to note that even though capacitor C-V curves are a good indicator of the surface statess (N_{ss}) they do not adequately predict the threshold voltage one expects for an MOS transistor because of additional factors in the fabrication which affect the knee of the C-V curve (thus the threshold voltage) and which are not readily discernable on the C-V curves. The position of the threshold voltage on the knee of the C-V curve was found to vary significantly with the manner in which the SiO_2 - P_2O_5 - Al interface was treated. The processing of MOS FETs wafers and the measurement of the capacitors and transistors on those wafers is described in the following paragraphs.

The following experiments are treated in chronological order. The results of each of these experiments is shown in figures 2.6 and 2.7.

2.2.2.1 Run 334A - 314B (N and P Channel Units)

This gate oxide was formed using standard procedure developed for the C-V measurements reported in Part I and is described below.

a. Cleaning Procedure: The wafer is dipped in HF for about 15 seconds or until the silicon surface in the gate region is hydrophobic. The wafers are then boiled in double distilled water for about 20 minutes.

b. Initial Oxide: An oxide is grown in a neutral tube at 1000°C for 10 minutes in dry O_2. The purpose of this oxide is two-fold. One reason is to mask against autodoping from the source and drain diffusions and the second is to mask against phosphorus from the tube used for the higher temperature oxidation.

c. Oxidation in Phosphorus Doped Tube: The purpose of oxidation in a phosphorus doped tube was to use the P_2O_5 on the tube to mask the movement of sodium from the tube to the wafers. (Note: It was shown later that oxidations in neutral tubes were not different.) Secondly, the deposition of a P_2O_5 glass could be carried out without removal of the wafers. The time, temperature and gas ambient cycle is shown below:

	Temp.	Time	Gas
Pre-heat:	350-450°C	15 min	N_2
Oxidation:	1100°C	42 min	O_2
Anneal:	1100°C	60 min	N_2
P_2O_5 Deposition:	1100°C	5 min	PH_3 in 1% O_2
Flush:	1100°C	5 min	N_2
Cool:	350-450°C	5 min	N_2

The purpose of the preheat cycle is to drive off water accumulated during wafer transfer. The anneal cycle is used to redistribute oxygen vacancies and reduce the boron depletion from the surface.

d. Aluminum Evaporation: Aluminum is evaporated onto the entire surface of the wafers immediately after the oxidation to minimize contamination. The aluminum evaporation is done from a source in a filament on a heated substrate in a system with a liquid nitrogen cold trap. The wafers were heated to 250°C and the evaporation was carried out at 55°C. The aluminum film is approximately 5KÅ.

e. Photoengraving: The wafers are covered with photoresist and the contact window pattern is printed. The aluminum film is then removed with KOH and rinsed in water. The wafers are then etched in an oxide etch to remove the SiO_2 from the areas of contact. The wafers are cleaned in TCE.

f. Aluminum Evaporation: Prior to the contact evaporation, the wafers are vapor degreased with isopropyl alcohol. An evaporation like the first is repeated.

g. Photoengraving: The aluminum contact pattern is etched and the wafers cleaned in TCE.

h. Measurements on FETS and capacitors were made prior to the alloying step.

i. Alloying: These wafers were alloyed in O_2 for two minutes at a temperature close to 580°C. This is the laboratory standard alloying procedure.

2.2.2.2 Run 333 - 334B (N and P Channel Units)

This run was originally meant to show the difference between 1200°C oxides and 1100°C oxides with the 1100°C P_2O_5 deposition. The initial 10 min. oxide at 1000°C was left out accidently and as a result autodoping at 1200°C occurred on the P-channel device. Data on the N-channel devices showed that they were quite similar to 334A.

2.2.2.3 Run 357 - 334C (N and P Channel Units)

The main purpose of this run was to determine the effects of oxidation at 1200°C and the effects of P_2O_5 deposition at 900°C for various lengths of time. All of the steps for this run were the same as 2.2.2.1 (run 314B-334A) except for the oxidation step. The differences in the time, temperature and ambient gas cycle are shown below.

	Temp.	Time	Gas
Pre-heat:	350-450°C	30 min	N_2
Oxidation:	1200°C	20 min	O_2
Anneal:	1200°C	30 min	N_2
Cool:	1000°C	5 min	N_2
	350-450°C	5 min	N_2
	Removed from Furnace		
Pre-heat:	900°C	15 min	N_2
P_2O_5 Deposition:	(a) 900°C	15 min	PH_3 in 30% O_2
	(b) 900°C	30 min	PH_3 in 30% O_2
	(c) 900°C	45 min	PH_3 in 30% O_2
Flush:	900°C	5 min	N_2

The purpose of the cooling cycle above was to reduce the stress on the oxide. The purpose of the different deposition times of the P_2O_5 was to get a range of thicknesses.

After the final photoresist step, the wafers were sintered at 490°C for various lengths of time.

2.2.2.4 Run 334d (N Channel Units)

The purpose of this next run was to show the differences between oxides grown at 1100 and 1200°C with a 900°C P_2O_5 glass deposition. Also one additional aluminum sentering step prior to the opening of the contact windows was added. This run is essentially a repeat of 2.2.23 except for the added sintering step. The times, temperatures and gas ambient cycles are shown below:

	Temp.	Time	Gas	Temp.	Time	Gas
Preheat:	350-450°C	15 min	N_2	350-450°C	15 min	N_2
Oxidation:	1100°C	42 min	O_2	1200°C	20 min	O_2
Anneal:	1100°C	50 min	N_2	1200°C	50 min	N_2
Cool:	350-450°C	5 min		1000°C	5 min	N_2
				350-450°C	5 min	N_2

	Temp.	Time	Gas
Preheat	900°C	5	N_2
P_2O_5 Deposition	900°C	30	PH_3 in 30% O_2
Flush	900°C	5	N_2

After the final aluminum etching process capacitor and device measurements were made then the wafers were sintered again at 490°C for about 30 minutes.

2.2.2.5 Run 334e (N and P Channel Units)

Run 2.2.2.4 was repeated for both N and P channels using the 1200°C oxidation process and the extra aluminum sintering step prior to photoresist.

2.2.3 Discussion of Results

The capacitance-voltage curves taken at 100KC and the MOS transistor turn on characteristics at various current levels are shown in Figures 2.5 and 2.6. The measurement techniques are described in Part I of this two volume report.

The experiment described in 2.2.2.1 (Run 334A-314B) showed that even though the basic procedures such as surface cleaning, oxide growth, and aluminum evaporation remained the same, significant differences between the C-V curves obtained on the capacitors made early in the program and these capacitors existed. Also, the device threshold voltages did not agree with the C-V measurements made on the same wafer initially. After the devices were alloyed at about 580°C the C-V curve was found to have shifted to the left indicating an increase in N_{ss}. Correlation between C-V curves and threshold voltages still was not obtained. The voltage shift between the theoretical curve with $N_{ss} = 0$ and this experimental curve was about 7 volts indicating an N_{ss} of about 1.2×10^{12} which was much higher than that typically obtained with the earlier capacitor runs. The conclusion was drawn that the process variations that existed between capacitor and device fabrication were most significant and that they would have to be eliminated to obtain good devices. The main areas of processing differences between capacitors and devices are first the steps required to obtain the source and drain diffusions and second, the etching of the aluminum and oxide to obtain windows for ohmic contacts.

The experiment described in 2.2.2.2 (333-334B) is the same as that in 2.2.2.1 except that the gate oxidation was done at 1200°C. The autodoping that occurred on the P-channel wafers showed that the 10 minute oxidation at 1000°C was necessary. In this case, the wafers were sintered at 490°C after the aluminum contact pattern was etched to determine if the high alloying temperature was causing any problems. The curves show that before heat treatment the 1200°C oxides were not as good as 1100°C oxides and after heat treatment both moved to the left indicating an undesirable process. The low temperature sintering did not move the curves as much as the alloying step so that the final result for both runs is about the same. The high temperature (580°C) alloying step was deleted from the processing and all further runs were sintered at about 500°C. In 2.2.2.3 (Run 357-334C) an experiment is described which was designed to show the effect of oxidation at 1200°C with a P_2O_5 glass deposition at 900°C for various lengths of time. The reason for the change in temperature for the P_2O_5 deposition was that it had been reported that not only did P_2O_5 prevent sodium ions from moving into the glass but also that the P_2O_5 was a very good getter of sodium ions already present in the glass.[10] The curves in Figure 2.6 show that the initial surface states were large; however, upon sintering at 500°C for long periods of time the surface states were reduced. From this run it appeared that the 30 minutes deposition was better than the 15 minutes and 45 minutes depositions since lower surface states were obtained. This was the first run where correlation between C-V curves and threshold voltages of capacitors and transistors on the same wafer were obtained. It was observed that over sintering was possible, i.e. as the sintering time was increased the curves first moved in showing a decrease in surface states and

then moved out showing an increase in surface states. These capacitors did not behave in a manner similar to the capacitors made early in the program indicating further process adjustment was necessary.

In the experiment described in 2.2.2.4 (Run 334d) it was shown that there was little difference between oxides grown at 1100°C and 1200°C with the time, temperature cycles used. The most significant part of this experiment was that the one additional sintering step prior to etching the windows through the SiO_2 for ohmic contact appeared to reduce the surface states significantly. The first measurements were made after the first sintering step but after the photoresist step. These measurements indicated that the N_{ss} was about 6×10^{11} which is comparable to that obtained with the C-V measurements reported in Volume I. The turn on voltage at 10 μa for the N-channel units was about +1.5v.

Note that excellent correlation between the turn on voltage measured and as indicated by the C-V curve was obtained.

In 2.2.2.5 (Run 334e) the experiment discussed in 2.2.4 (Run 334d) was repeated using only the 1200°C oxidation process for both N and P channel units. Again, the added sintering step after the first aluminum evaporation but prior to the photoresist step was used. The results obtained in this experiment were the same as obtained in 334d with only tenths of volts differences in turn on voltages between the two runs.

Also note that after 30 minutes anneal at 490°C that no shift in the C-V curve was observed except for a change in the shape of the knee of the curve. This change could be caused by increased frequency response of the surface states. A slight increase in the turn on voltage was observed for the P-channel units.

In summary, both the phosphorus glass and the two aluminum processing steps with sintering immediately after the first aluminum evaporation were required to obtain N and P channel enhancement mode devices. Note that the N and P channel units were fabricated simultaneously showing that the processing steps are suitable for the fabrication of complementary monolithic functional blocks in epitaxial material. The flow diagram of the final process is shown in Figure 2.7.

One final point should be brought out. That is that the doping level (Na) indicated by the C-V curves is much higher than that indicated by the four-point-probe resistivity measurements on the epitaxial material. This points to the fact that the majority carrier mobility in the epitaxial layer is much lower than mobility in bulk material that has not been through temperature cycles.

It was estimated that the majority carrier mobility in the epitaxial material is smaller by a factor of two than the mobility in untreated bulk silicon. Also from measurements of the transconductance the majority carrier mobility in the inversion layer is smaller by more than a factor of three than the mobility in untreated bulk material.

A summary of the typical electrical characteristics of the N and P channel units is shown in Table 2.2.

2.2.4 Stability Tests

Both N and P channel MOS transistors fabricated as shown by the flow diagram in Figure 2.7 were packaged and subjected to temperature-bias stress to determine the stability of the turn on voltage (Vgst). The results of the tests are shown in Table 2.3. The turn on voltage was measured at 10 μa in every case. It is important to note that the bias was removed while the units were at 150°C. The units were then removed from the oven and allowed to cool to room temperature. Upon further discussion of stability it was realized that if polarization occurred at the elevated temperature which was caused by the bias that removal of the bias at the elevated temperature might allow the polarization to relax such that the original oxide state was obtained. The stability test was repeated but in this case the units were allowed to cool to room temperature with the bias applied. The results are shown in Table 2.4 Column A. The units were then stored with no bias at room temperature for six hours. Measurements were then repeated and the results shown in Column B. Finally the units were stored at 150°C for two minutes with no bias. The results are shown in Column C. Note that first, the polarization was slowly relaxing at room temperature and second that the polarization rapidly relaxed at 150°C. Note that the final turn on voltage is almost the same as the initial voltage. This point is important since the tests indicate that the turn on voltage changes are caused by a polarization effect and not ionic drift. The polarization effect is not permanent while changes caused by ionic drift are permanent shifts and would be observed no matter how the units were cooled.

TABLE 2.2 TYPICAL MOSFET CHARACTERISTICS

	N-Channel	P-Channel
Turn-on Voltage (V_{gST}) I_{ds} = 10 ua V_{DS} = V_{gS}	+ 1.5 v	- 4.8 v
Source-to-Drain Breakdown Voltage (BV_{DS}) V_{gS} = 0	+ 28 v	- 80 v
Gate-to-Source Breakdown Voltage (BV_{gS})	110 v	110 v
Transconductance (gm) V_{ds} = 10 v, I_{DS} = 5 ma	1300 umhos	1400 umhos
I_{DS} = 1 ma	560	670
I_{DS} = 0.2 ma	250	335
Drain to Source Conductance (g_{dS})	1400 umhos (V_{gS} = + 4 v)	1400 umhos (V_{gS} = - 11 v)
Drain to Source Leakage Current (I_{DSO}) V_{gS} = 0, V_{dS} = 10 V	10 namps	10 namps
Average Channel Mobility	280 cm^2/v-sec	150 cm^2/v - sec
Channel Length (see Table 2.1)	1 mil	1 mil

TABLE 2.3

STABILITY TESTS

Vgst @ 10 μa

Unit No.	Bias	160 hrs. - 150°C B	A	V Shift
ae 46 - 1(N)	+22.5v	1.97v	1.82v	-.05v
ae 46 - 4(N)	-22.5	0.84	0.94	+0.10
af 6 - 11(N)	+22.5	2.66	2.62	-.04
af 6 - 12(N)	-22.5	2.53	2.43	-.01
		17 hrs. - 150°C		
ad 87 - 5 (P)	+22.5	-4.49	-4.73	-.24
ad 87 - 6(P)	-22.5	-4.54	-4.91	-.37
ad 87 - 1(P)	+6.8	-4.57	-4.60	-.03
ad 87 - 2(P)	-6.8	-4.42	-4.47	-.05

TABLE 2.4

	Initial	A After Temp-Bias Stress		B After Room Temp Recovery	C After High Temp Recovery
Bias		+12v	-12v	0	0
Time		16 hrs	16 hrs	6 hrs	2 min
Temp	25°C	150°C	150°C	25°C	+150°C
af-7 (N-channel)					
V_{gst}	+1.91	+1.44		+1.73	+1.90
ΔV		-0.47		-0.29	-0.01
V_{gst}			+2.15	+1.98	+1.90
ΔV			+0.24	+.07	-0.01
M 841-A (P-channel)					
V_{gst}	-4.43	-5.04		-4.84	-4.43
ΔV		-0.71		-0.41	0
V_{gst}			-4.09		-4.44
ΔV			+.34		-.01

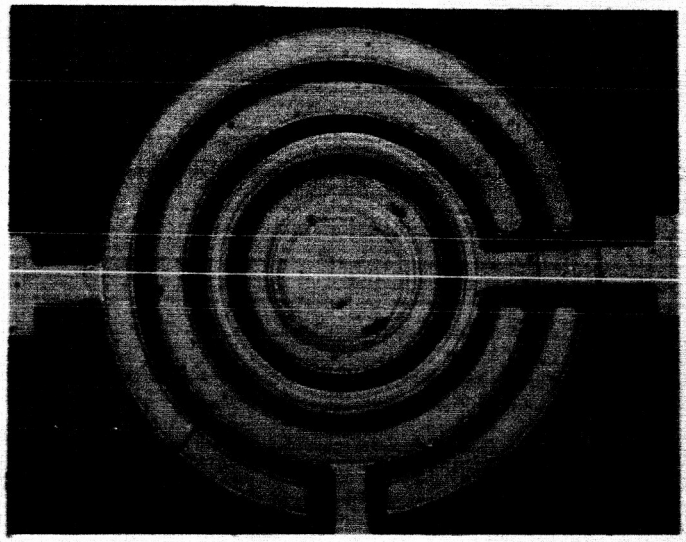


Figure 2.1 Annular MOS FET Geometry

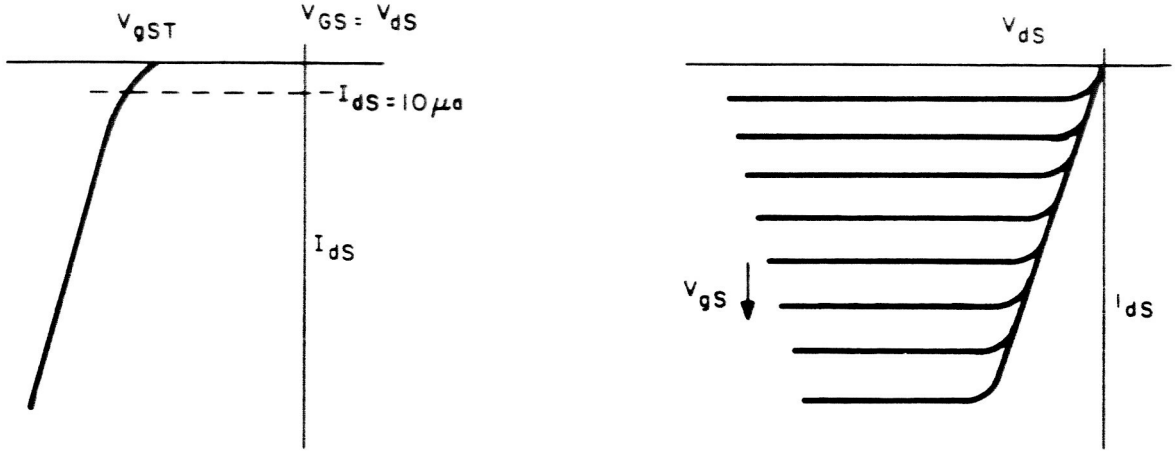


Figure 2.2 Transfer Characteristics

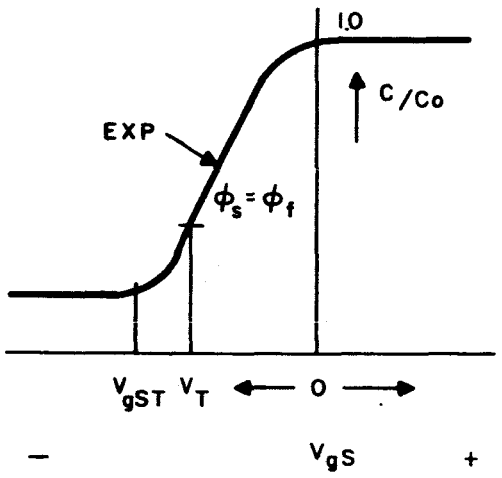
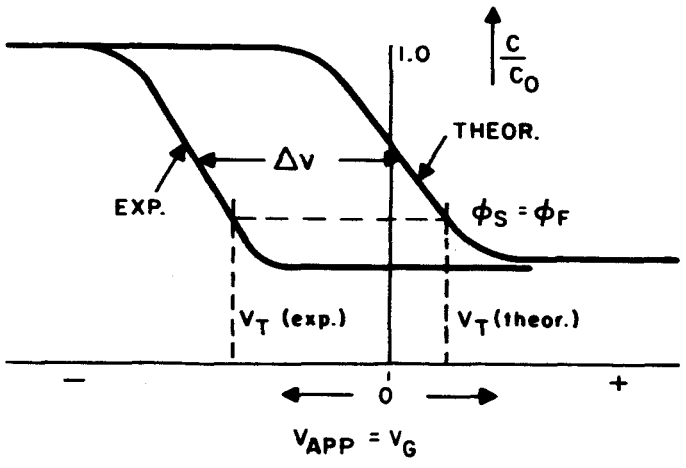


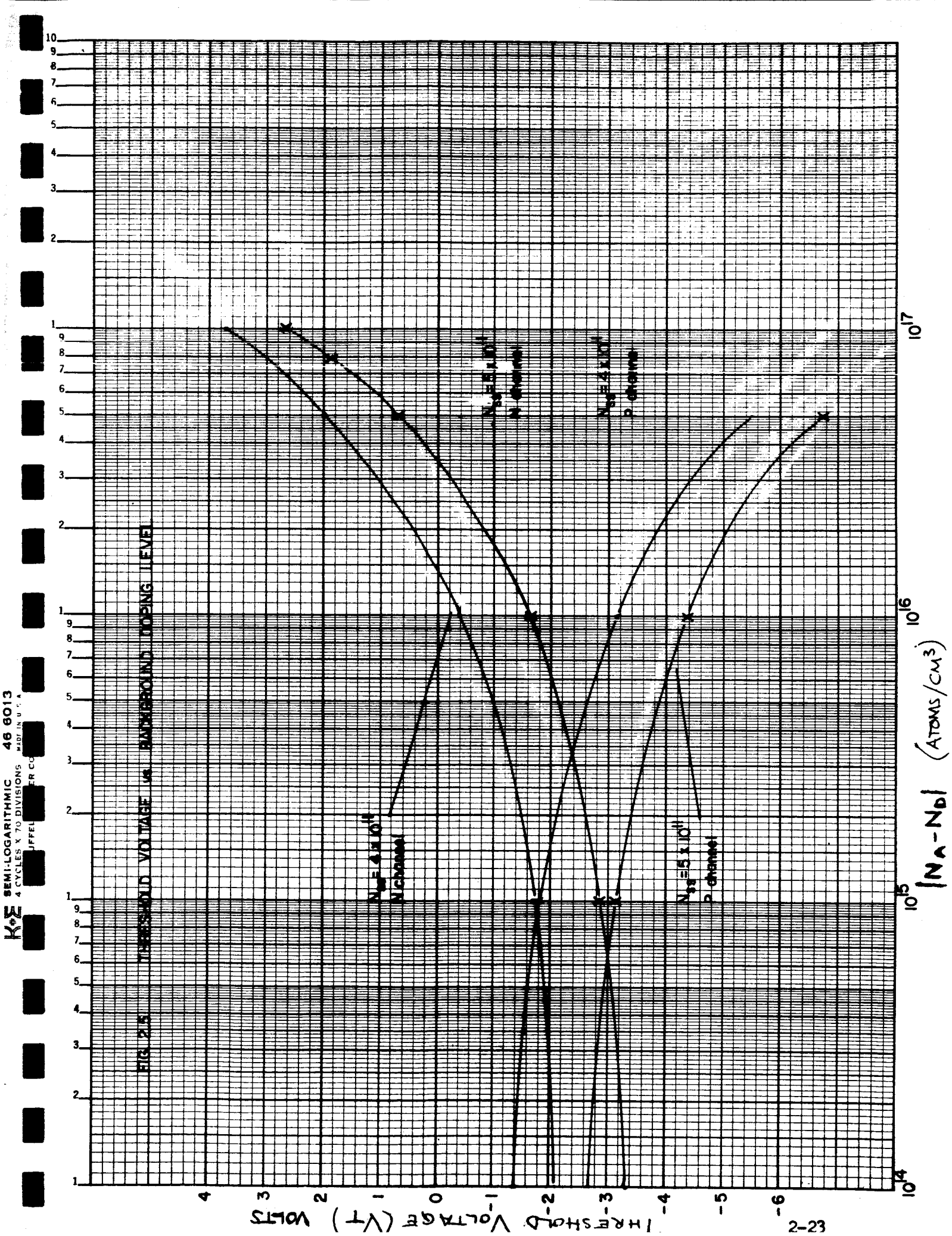
Figure 2.3 Comparison of V_T and V_{gst} on C-V Curves



$$V_T(\text{theor.}) = \frac{+q N_B t_{OX}}{K_O \epsilon_O}$$

$$V_T(\text{exp.}) = \phi_{MS} - \frac{q(N_{SS} - N_B) t_{OX}}{K_O \epsilon_O}$$

Figure 2.4 Determination of N_{ss} By Shift in C-V Curves


THRESHOLD VOLTAGE vs BACKGROUND DOPING LEVEL
Threshold Voltage (VT) Volts
|NA-ND| (Atoms/cm³)
N channel
P channel
N channel
P channel
K&E SEMI-LOGARITHMIC 46 6013
4 CYCLES X 70 DIVISIONS

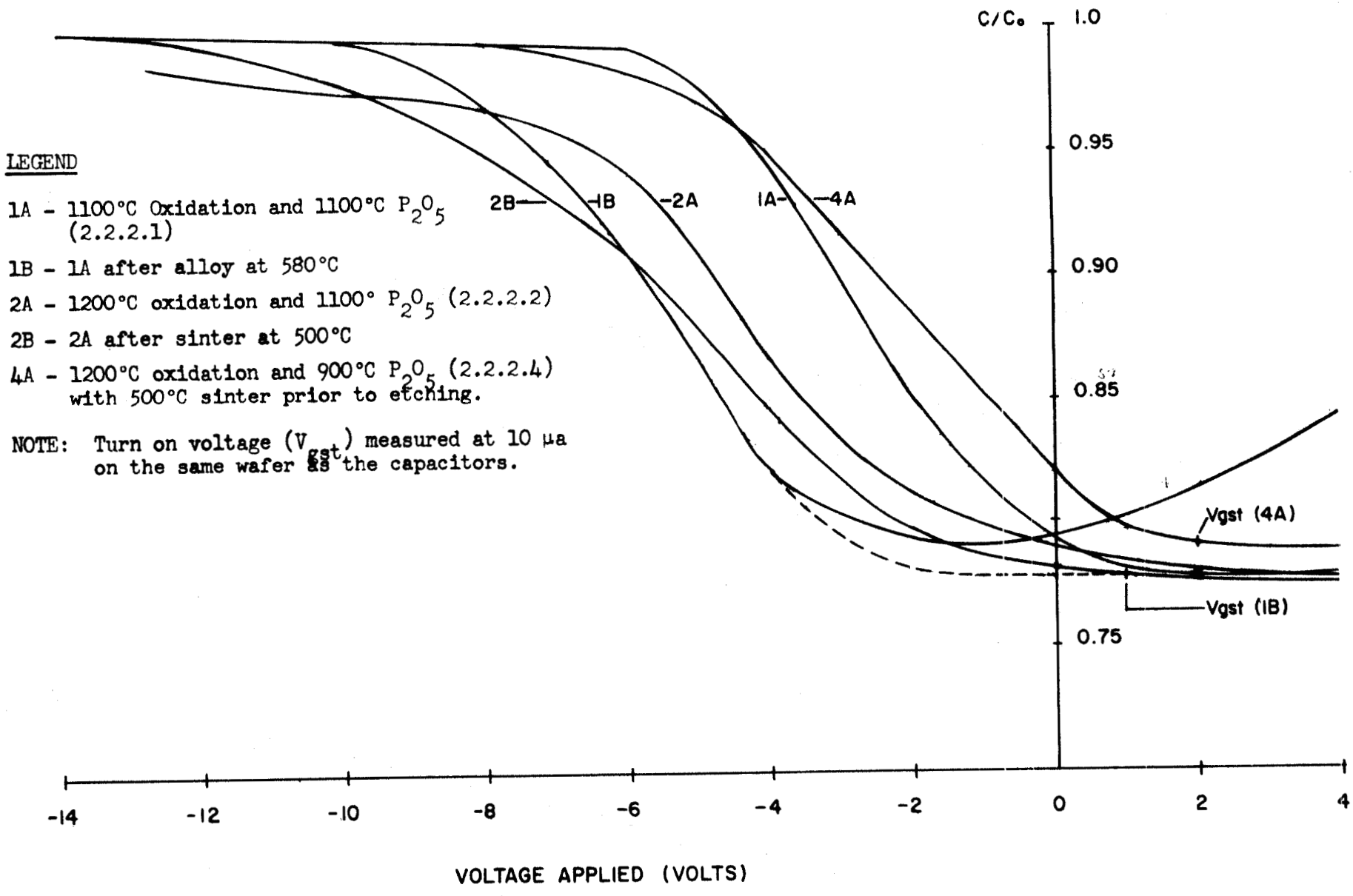


Figure 2.6 C-V Curves and Turn On Voltages (N Channel)

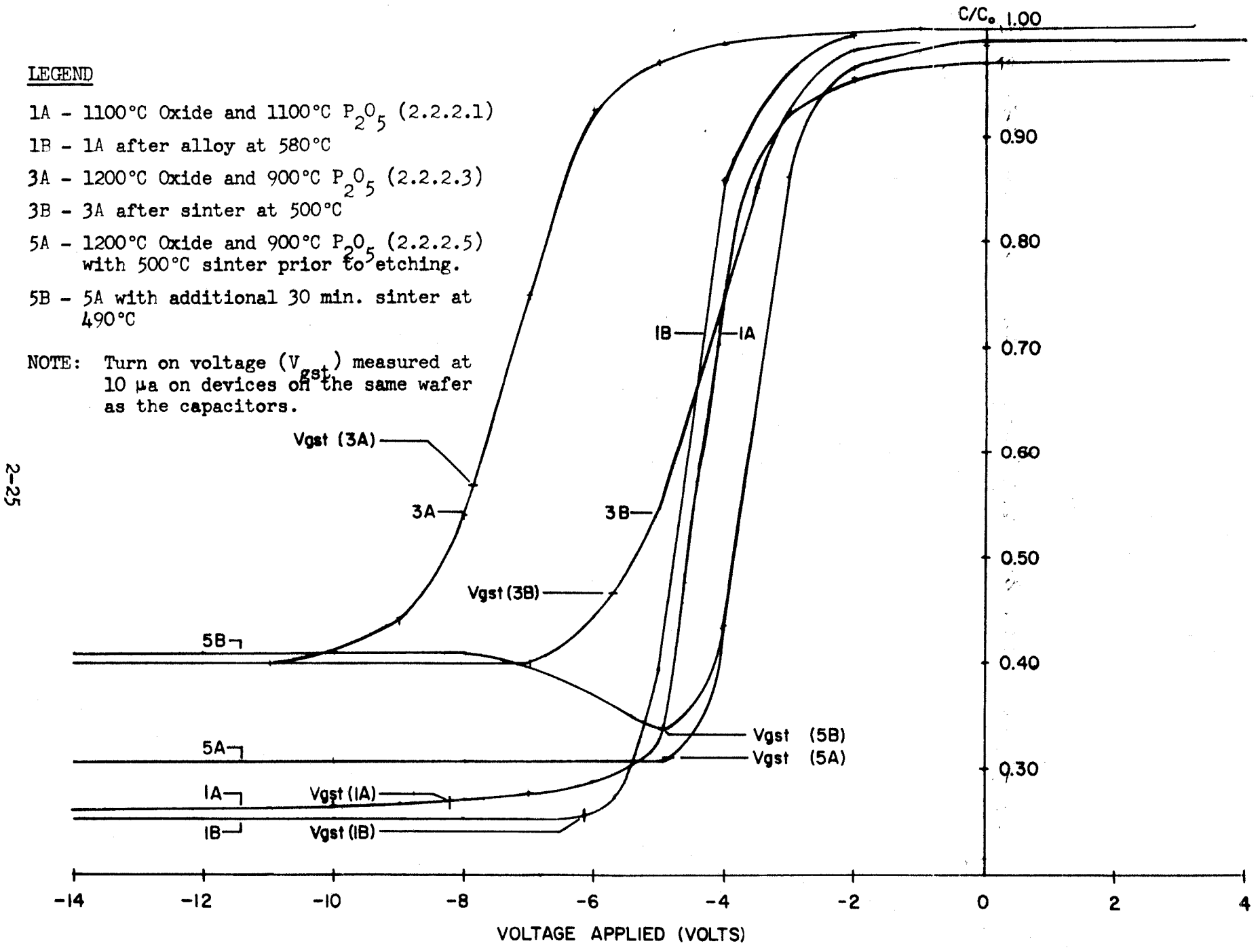


Figure 2.7 C-V Curves and Turn On Voltages (P-Channel)

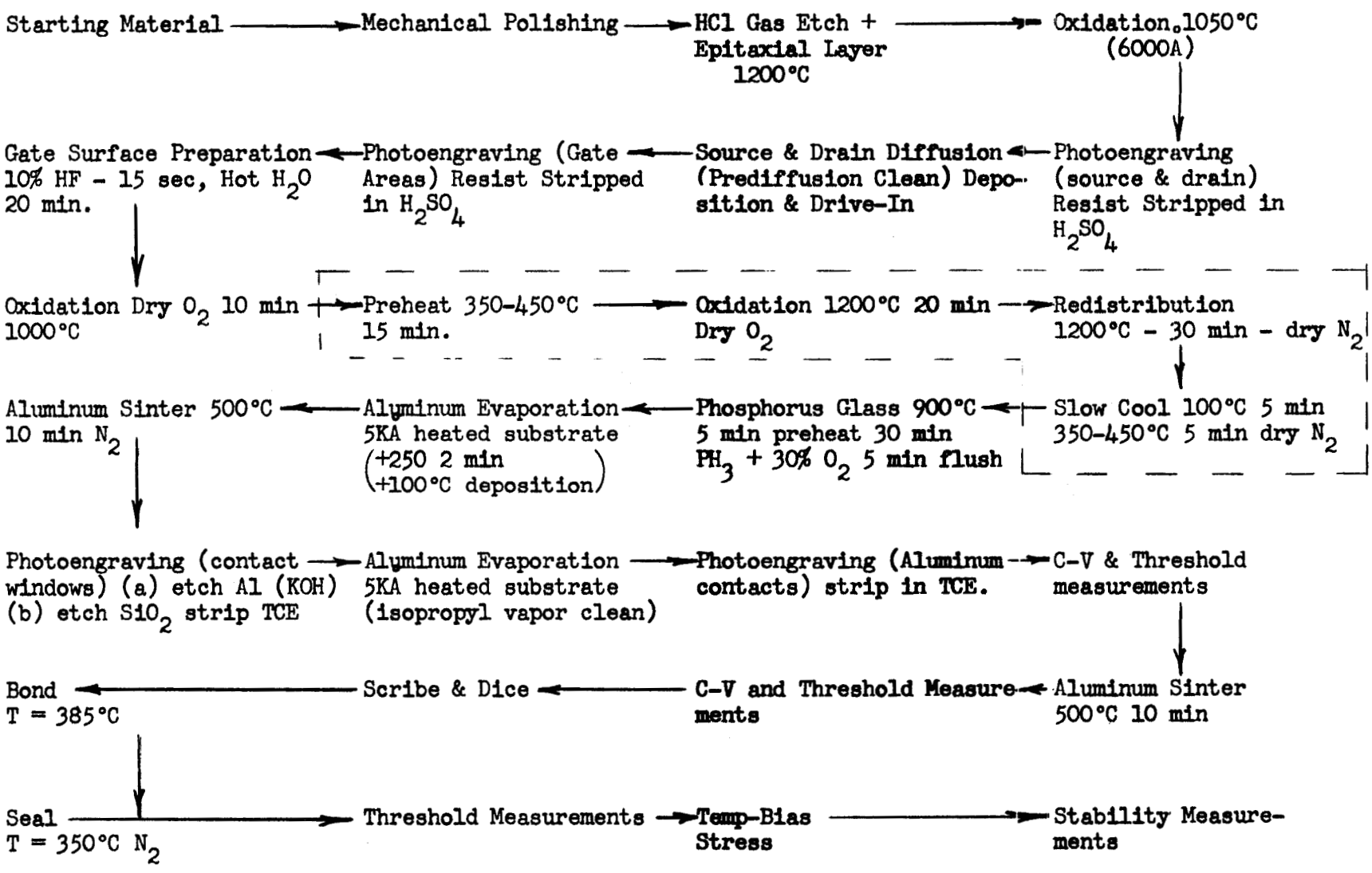


Figure 2.8 Process Flow Diagram

3.0 CONCLUSIONS AND RECOMMENDATIONS

A process for the fabrication of complementary enhancement mode MOS transistors has been developed. The techniques used for the fabrication show that the process is compatible with the simultaneous fabrication of N and P channel units on epitaxial material. The turn on voltage at 10 μa drain to source current for the P channel units is about -5v and the turn on voltage for the N channel units is about +1.5v. The stability tests indicate that while there is no permanent shift of the turn on voltage upon temperature-bias stress there is a temporary shift caused by polarization of the phosphorus glass. Processing improvements such as optimizing the phosphorus glass time-temperature cycle and aluminum sintering process are required.

It is recommended that less P_2O_5 glass be utilized, that greater emphasis be placed on the time and temperature of the sintering step immediately after first aluminum evaporation and further experiments be conducted using different types of aluminum vapor deposition systems. Further, since many of the variables have been eliminated, it would be informative to repeat the experiments using other metals for the gate electrode such as nickel or chrome-gold. An experiment to compare devices made in untreated bulk silicon would also be of interest. Finally, experiments in which the N or P channel device is made in a diffused pocket would significantly aid the fabrication of integrated complementary logic circuits.

It is the authors' opinion that these processing variations can best be determined while engaged in the fabrication of a complementary monolithic circuit with specific operational goals.

4.0 LIST OF REFERENCES

1. C. T. Sah, "Characteristics of the Metal-Oxide-Semiconductor Transistors," IEEE Transactions of the Electron Device Group, July 1964.

2. V_T as originally presented by Sah did not include the metal-semiconductor work function ϕ_{MS} as indicated in equation 2-3, however, this term is important in determining the n-channel MOST electrical characteristics.

3. Interim Progress Report for Phase I Groove Etching Study, 15 Oct 64 - 15 Jan 65, Contr. No. NAS 5-3758, W.O. 670-190-5

4. Interim Progress Report for Phase II of Groove Etching Studies Chemical Deposition in Grooves, 1 Jan - 1 Apr 1965, Contr. No. NAS 5-3758, Procurement No. 670-W46374, Westinghouse G.O. 51248AQ1A.

5. Final Report - Phase III Groove Etching Studies Oxide Barrier Isolation, 1 Feb - 1 Jun 1965, Contr. No. NAS 5-3758, Procurement No. 670-W46712, W.GO. 51248AN1A

6. Final Report - Epitaxial Process for Development for Monolithic Complementary MOS FET Structure with Oxide Barrier Isolation, 15 Mar - 15 Sep. 1965, W.O. 670-W46784, Contr. No. NAS 5-3758, Westinghouse G.O. No. 51248BD.

7. Westinghouse Oxidation Process Specification #400.

8. Final Report - Semiconductor Wafer Improvement Through Photoengraving, 1 Mar - 1 July 65, Contr. No. NAS 5-3758, Procurement No. 670-W46756, W.G.O 51248AS1A

9. Final Report for Investigation and Development in the Diffusion of Gaseous Impurities into Silicon, 1 Jun 64 - 1 Mar 65, Contr. No. NAS 5-2755.

10. E. Yan, W. H. Ko, A. B. Kuper, "Sodium Distribution In Oxide by Radiochemical Analysis and its Effect on Surface Potential", International Electron Devices Meeting, #19.2, Oct. 1965.