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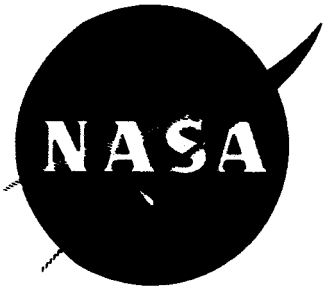

5KW PULSE WIDTH MODULATED STATIC INVERTER

By

W. V. Peterson and R. J. Resch

Prepared For

National Aeronautics and Space Administration

CONTRACT NAS 3-6475

TRW EQUIPMENT LABORATORIES
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MID-CONTRACT REPORT

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SUMMARY

This document is the Mid-Contract Report covering the work performed under Contract NAS 3-6475. The purpose of this work was to design, breadboard and test a 5 KW, Three Phase, 400CPS Static Inverter utilizing pulse width modulation techniques. This report covers the period from March 15, 1965 to November 15, 1965, during which design verification tests were performed on most of the individual circuits and also on a preliminary single phase breadboard operating at an output power level of 650 watts. These tests proved the feasibility of meeting the design objectives. Work during the second half of this program will include generation of final schematics and parts lists and the fabrication and testing of a deliverable breadboard.

I. INTRODUCTION

The development work being carried out under Contract NAS 3-6475 is a continuation of the work that was done on the Optimization Study of High Power Static Inverters and Converters under Contract NAS 3-2785. During the study program various step-wave power conversion techniques were considered. Although use of a many-step approach can result in an unfiltered output having a total harmonic distortion of less than ten percent, the power transformers must operate at the power frequency, which, in this case, is 400 cycles.

Thus, it is seen that the step-wave approach requires only little filtering compared to that required to convert a pure square wave to a sine wave, but it still has a high concentration of weight in the transformers. The approach that was selected for further evaluation in breadboard form utilizes a naturally sampled pulse width modulation technique that eliminates the need for transformers in the power stage. Here the filtering requirements are kept to a minimum by sampling at a high frequency and a weight reduction is achieved because all 400 cycle power transformers are eliminated.

If space power systems provided a primary power source of approximately 200 volts, there would be no need for any power transformers in the pulse width modulated inverter. However, the design specifications for the present program require that the inverter operate from a source of 56 volts. Therefore, it is necessary to include a DC-DC converter to step up the voltage sufficiently so that the transformerless output power stage can provide 120 volts RMS. This DC-DC conversion can be performed at a frequency higher than 400 cycles which helps keep the weight of the associated transformers low.

Following is a summary of the design objectives for the pulse width modulated (PWM) static inverter.

Input Voltage	56 volts DC, + 10%, - 20%
Output Voltage	120/208 volts RMS, 3 phase, 400 cps
Regulation	± 2%
Output Power	5 KW, 0.7 p.f. continuous 10 KW, 0.7 p.f. for 5 seconds.
Overload	Short Circuit Protection Required

Harmonic Distortion	5% Total, 2% Single
Efficiency	80%

II. DESCRIPTION OF OPERATION

The block diagram of the complete inverter is shown in Figure 1. The three phase square wave reference generator produces the low frequency (400 cps) modulating signal. These three signals are displaced 120 degrees with respect to each other to establish the three phase relationship of the output voltage. The reference waves are then passed through a controllable attenuator which has a normal attenuation of zero, but when an overload current is detected at an output line, the proper attenuator is activated to attenuate the size of the modulating signal which in turn reduces the voltage of the overloaded line. After passing through the attenuator, the fundamental frequency of the of the output square wave is extracted by a narrow band filter. The purity of this resulting sine wave is as high as practical because it determines the waveshapes of the output voltage. The modulating sine waves are then mixed with the sweep wave in the three summing networks. The resulting waveform is a sinusoidally undulating sawtooth wave which is then sent to the slicer circuit. The slicer circuit is an absolute level detecting system that produces pulses having a width proportional to the modulating signal level during the sampling interval. The sampling interval is determined by the sweep wave generator which produces a sawtooth sweep wave at the carrier frequency. Waveforms showing generation of the PWM signal are shown in Figure 2.

The variable pulse width signal is then amplified and sent to the driver stage which transforms this signal into a form suitable for driving the power stages. The power stages convert the low level drive signals into the required high power level output. The power source for the power stage is the regulated DC-DC input converter. The input converter raises the input voltage to the required voltage level for use by the power stages. The high power output voltage of the inverter is then filtered to eliminate the carrier and its sidebands from the output voltage leaving only the power frequency voltage. The voltage regulator and reference develops an error signal which is fed back to the input regulator to maintain a constant output voltage. Also present at the output lines are three current transformers which detect any overload currents and act on the modulating signal via the current limit and reference circuit to reduce the power frequency output voltage, thereby limiting the overload current. The individual blocks will be discussed in more detail in the following sections.

PULSE WIDTH MODULATION INVERTER BLOCK DIAGRAM

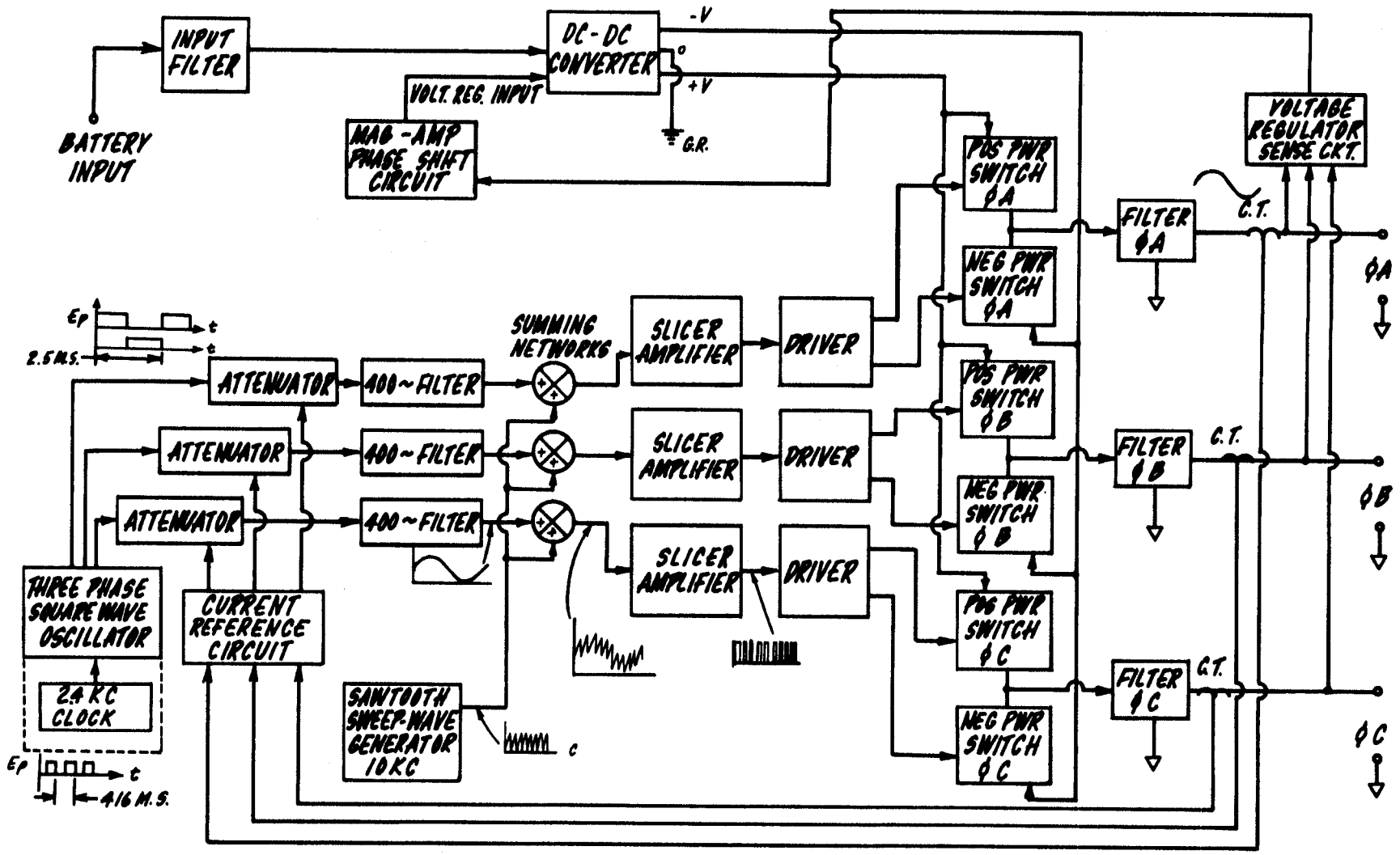


FIGURE 1

NATURAL SAMPLING

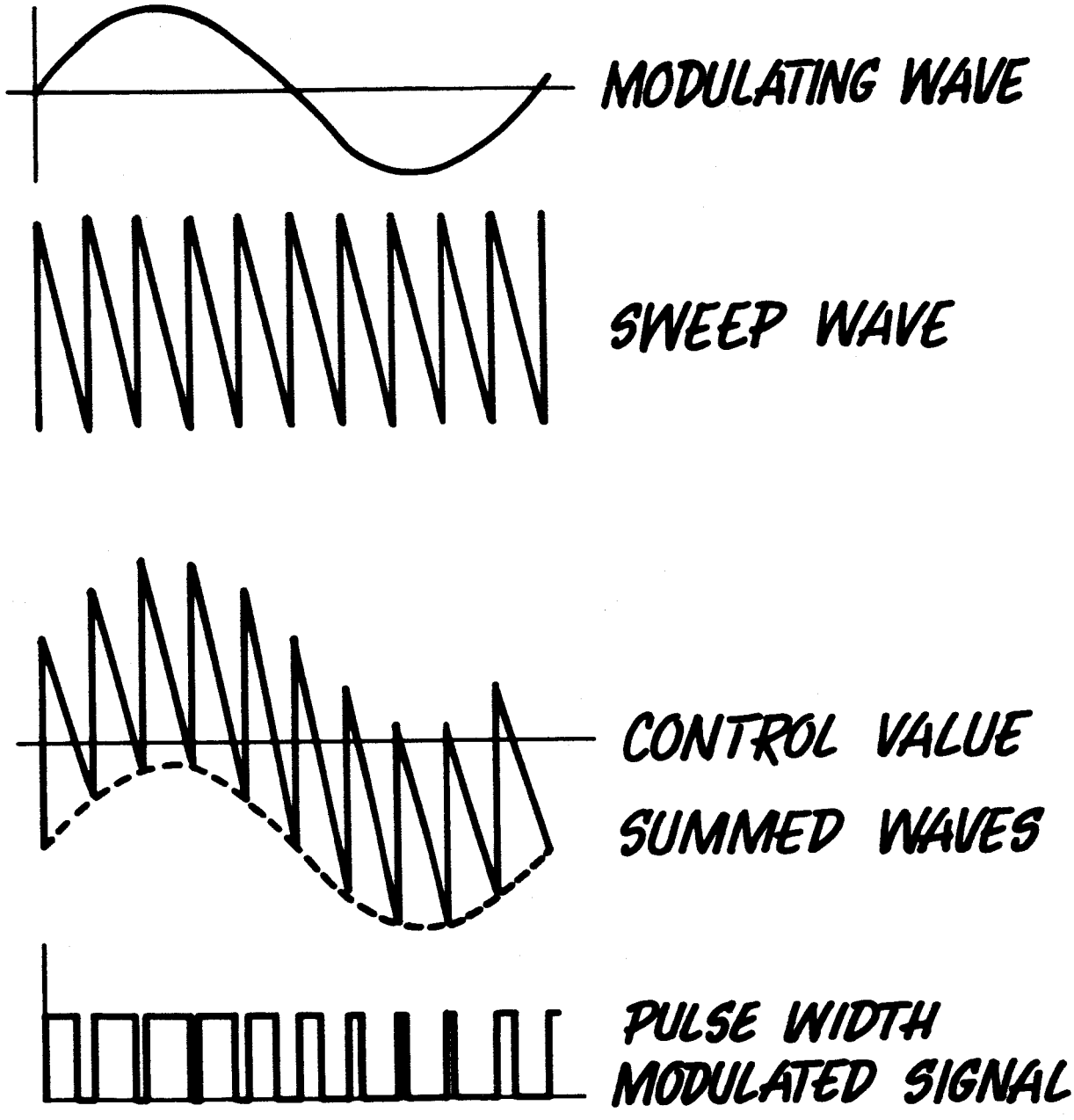


FIGURE 2

III. LOGIC AND LOW LEVEL CIRCUITS

The circuits discussed in this section were constructed in breadboard form and given preliminary tests to determine their performance characteristics. Evaluation of the power stage circuit configuration and components was accomplished by interconnecting these logic circuits to provide the necessary drive signals and hence form a complete single phase inverter (except for the DC-DC Converter) operating at a reduced power output. Operation of this rather complete design verification breadboard allowed any circuit interface problems to be solved prior to fabrication of the deliverable unit.

A. THREE PHASE 400CPS REFERENCE

This circuit provides the three phase reference or modulation signal for the inverter. It consists of a stable two-transistor astable multivibrator operating at a frequency of 2.4 KC. The output of this multivibrator is applied to a ring counter consisting of three flip-flops the outputs of which are 400 cps square waves with appropriate time displacements to form the three phase output.

A start-preference circuit is included to insure that the ring counter starts properly and also to force it back to its correct sequence in case an abnormal noise signal causes it to get out of step.

B. CURRENT REFERENCE AND ATTENUATOR

A means for limiting the inverter output current is provided by reducing the amplitude of the modulating signal which in turn causes the output voltage to be reduced. The implementation of this current limit function is done in the current reference and attenuator circuit which is between the 400 cps square wave reference oscillator and the 400 cps filter.

Output current sensing is accomplished with a current transformer, the output of which is rectified, filtered and applied to the current reference circuit consisting of a zener reference element. As the current starts to exceed the preset limit, a signal from the current reference circuit is applied to the attenuator which, by means of a shunting transistor at the base circuit of an emitter follower effects a reduction in the amplitude of the 400 cps square wave. This signal is reduced such that the output current is limited to a value only slightly greater than the set point.

The attenuation for current limit is done at a point where the reference or modulating signal is still a square wave. This prevents distortion problems that could result if the attenuator were to operate directly on the sine wave reference.

C. 400 CPS FILTER

After considering the complexity and sensitive nature of a twin-T feedback amplifier a 400 cps narrow band LC filter was chosen for use in converting the reference square wave to a sine wave. The selected filter is a small encapsulated module of military grade. This unit performed very well in the design verification breadboard.

D. SWEEP WAVE GENERATOR

This circuit generates a sawtooth wave which is used to sample the modulation or reference signal and ultimately produces the PWM signal. The circuit consists of a capacitor that is charged in a constant current manner by means of a transistor. Because the charging current is constant, the voltage developed is a linear ramp. As the voltage across the charging transistor drops below a preset level a one-shot multivibrator is triggered and causes the capacitor to discharge in three or four microseconds. The output from the sweep wave generator is taken through an emitter follower so that non-linearities due to loading are kept to a minimum.

A bootstrapped unijunction circuit was tried for this ramp generation application. It provided a very linear ramp over most of the cycle but the response limitations of the unijunction caused rounding at the ends of the waveform which resulted in marginal operation of the inverter at a modulation index of greater than 0.8.

E. SUMMING NETWORK

The summing network mixes the output of the 400 cps filter and the sawtooth voltage of the seeep wave generator. The network consists of two transistors with separate drives but having a common collector load. One transistor is driven with the 400 cps sine wave signal and the other with the 7 KC sawtooth. The output at the common collector load is a linear summation of the two input signals.

F. SLICER AMPLIFIER

This circuit performs the final operation in preparing the signal to be applied to the drive stage which controls the operation of the inverter power stage. It consists of a two-transistor differential amplifier that switches on when the input voltage exceeds the reference voltage established by the bias. To provide additional gain and to obtain an output signal which is referenced to ground a third transistor is used which takes its input from the collectors of the differential pair and has its collector load connected to ground.

The output of this slicer amplifier is a pulse width modulated waveform. The frequency is equal to that of the sweep wave generator; however, the pulse width is a function of the instantaneous amplitude of the 400 cps modulating signal.

G. DRIVER

Each driver stage must provide the necessary isolated signals to operate the power stage transistors for one phase. The circuit consists of two Darlington transistors operated in a push-pull configuration driving a transformer with a center-tapped primary winding. Darlington transistors are used so that little additional pre-drive circuitry would be required between the slicer and the driver. The output of the main drive transformer has two windings. One is used for operating the positive half phase and the other for the negative half phase of the power stage.

It will be shown later in this report that a saturating transformer is also required for proper operation of the power stage. Therefore, this transformer also obtains its drive signal from this driver stage.

IV. POWER STAGE

The major emphasis during the design verification phase of the inverter program was placed on evaluating the performance of the PWM power stage. There are no inherent limitations associated with the circuits discussed thus far. In the PWM power stage, however, there are various restrictions which are imposed because of the limitations of available switching devices. It is the purpose of this section to clearly point out the requirements for correct power stage operation, indicate what limitations are present, show the various circuits and approaches that were considered and tested and describe the solutions which are most effective in overcoming the component limitations.

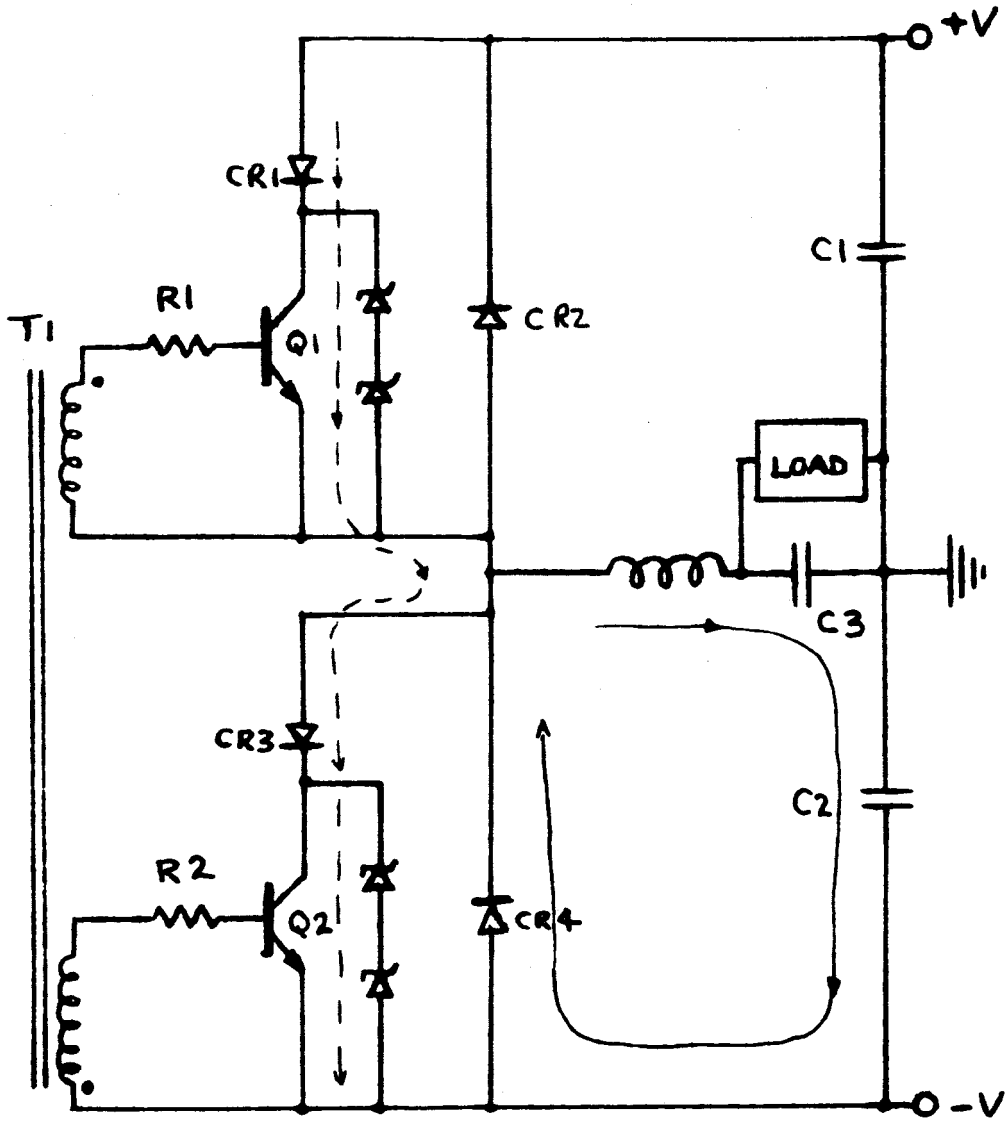
A. BASIC OPERATION

A simplified diagram of one phase of the PWM power stage is shown in Figure 3. For a three phase inverter, three such stages are required which have the correct phase relationships between the 400 cycle component of their drive signals.

The drive signals to the power stage transistors appear across the two transformer output windings. The input to the transformer comes from the driver stage which was discussed previously. These are PWM signals and the signal applied to the positive half phase is 180 degrees out of phase with that applied to drive the negative half phase.

To follow the operation of this power stage assume that Q1 is on. This causes current to be drawn from +V through blocking diode CR1 and transistor Q1 and on through the filter and load to ground. At the time the drive signal to Q1 reverses, the drive to Q2 also reverses to turn this negative phase switch on. However, because of the lagging current that is drawn by the filter and load, no current will flow in Q2 at the instant it is turned on. Instead, the current that has built up in the filter and load must find a path to allow it to continue flowing in the same direction it had been. This path is down through C2, up through CR4 and through the load and filter. During the time current flows through this path, the voltage across the inductor is reversed because it becomes the source of energy to keep current flowing in the same direction. When this current reduces to zero, transistor Q2 takes over and current is drawn from ground through the load and filter, through the blocking diode CR3 and the transistor Q2 and to the negative supply voltage. This same action then repeats for each cycle of the carrier frequency of the PWM signal. The L-C filter removes the carrier frequency and its harmonics and sidebands and the 400 cps voltage waveform appears across the load.

BASIC POWER STAGE CIRCUIT



REACTIVE CURRENT PATH AT END OF Q1 CONDUCTION TIME

"SHOOT-THRU" PATH DURING STORAGE TIME

FIGURE 3

If it were't for the reactive currents that are present because of the nature of the filter and load, the reactive diodes, CR2 and CR4, and the reactive capacitors, C1 and C2, would not be required. Without these components to form a path for these reactive currents, high voltage transients and excessive waveform distortion would result.

Capacitors C1 and C2 would not be required if the source of +V and -V were a storage battery which can handle reverse currents. However, we are to assume that the source of power may be of a type that cannot pass current in the reverse direction. Solar cells fall into this class of sources.

B. TRANSISTOR CONSIDERATIONS

It will be seen that the power transistors are the limiting devices in the PWM power stage. For a single pair of transistors to efficiently provide the specified undistorted power output for each phase of the PWM inverter, the general characteristics for each transistor without safety factors would be as follows:

Voltage Rating	400 volts
Current Rating	70 amps
Switching Characteristics	
Delay & Rise Time	1 microsecond
Storage & Fall Time	1 microsecond
Saturation Resistance	.01 ohms

Since no transistors having these characteristics are presently available, certain compromises must be made. Before considering the extent of these compromises a comparison of three power transistors that either were or are now available will be made. Refer to Table 1.

The RCA developmental-type TA 2110 was withdrawn from the market prior to the present contract work but is included here for additional comparison. Considerable testing and evaluation of the 2N2583 transistor in the PWM power stage has been done on this program, details of which will be presented in the following sections of this report. It should be noted that production of the 2N2583 was discontinued during October, 1965. About this time evaluation of the selected DTS-0710 transistor was started. This is the device that is presently working in the power stage of the low power design verification breadboard.

TABLE 1. Comparison of High-Power High-Voltage Switching Transistors

	TA2110 (RCA)	2N2583 (Delco)	Selected DTS-0710 (Delco)
Collector Voltage	400	500	500
Collector Current (amps)	10	10	5
Power Rating (watts)	150	150	100
Turn-on Time (μsec.)	1	2.1	1
Turn-off Time (μsec.)	1.5	3.2	1.5
Saturation Resistance (ohms)	0.1	0.1	0.12

Notice from the above charts that all of the transistors that were considered fall short of providing a safety factor of two on their voltage ratings. Either a compromise had to be made on this safety factor or considerable circuit complexity had to be incorporated to operate two transistors in series. The reduction in safety factor was selected as the most appropriate approach for the present program.

The second obvious discrepancy between the required rating and the rating of an available device is in the current handling capability. Here it was necessary that seven 2N2583 transistors be operated in parallel for each half phase, and for the DTS-0710, fourteen must be placed in parallel for each half phase of the inverter to provide the specified power output.

The third rating of concern is the switching characteristic of each transistor. During the testing with the 2N2583 and the DTS-0710, it was found that a very considerable discrepancy existed between the turn-off times measured in the power stage circuit as compared with those times listed in the manufacturers data sheets. Because of the longer storage times, extensive circuit development and testing was done to find the best way to overcome this limitation. Even so, it was necessary to reduce the carrier frequency from 10KC to 7KC so that a reasonably high index of modulation could be used. As the modulation index goes higher, the pulse widths that must be handled by the power stage transistors get narrower. As the modulation index goes down the filter size increases and the peak voltage that appears across the transistors goes up.

C. POWER STAGE EVALUATION

The power stage of the single phase design verification breadboard contains four power transistors. Two of these transistors were connected in parallel for the positive half phase while the other two were connected in parallel for the negative half phase. (See Figure 3 for the general single phase power stage configuration). The power stage was fabricated on two heat sinks with each heat sink containing one positive and negative power transistor. The required blocking diodes, reactive diodes, and zener diodes were also mounted to these heat sinks. One balancing reactor was used for each half phase. The output filter inductor and capacitor values for this low power breadboard were determined from a previous computer study. These values are 470 microhenries and 29 microfarads for a ten ohm load impedance. An air core inductor design was used.

The output drive transformer design was given special attention since it must be capable of passing this pulse width modulated waveform with a minimum amount of distortion. Therefore, the transformer must have a frequency response from 400 cycles to at least 200KC. Two drive transformers were fabricated and operated in the driver stage. The first transformer design had its primary and secondary windings separated with its secondary wound over the primary. The rise time of this transformer into a 2.5 ohm non-inductive load was approximately 4.5 microseconds. The second transformer design utilized interleaving of the primary and secondary windings in order to minimize the transformer leakage inductance. Its rise time into a 2.5 ohm non-inductive load was found to be 3 microseconds. Both transformer designs used EI-375-6H laminations to form a square stack.

An alternate driver stage approach utilizing current feedback was investigated and compared with the proposed voltage drive approach. The results of this investigation revealed that a slight increase in the driver stage efficiency would be obtained with this current feedback approach. However, the increase in circuit complexity required to implement this approach more than nullifies the slight advantage in efficiency. Therefore, the voltage drive approach was used.

A reactive current capacitor was placed across each of the two high voltage DC power supplies. The value for these capacitors was calculated to be 255 microfarads each. Their sizing is discussed in detail in Appendix A of Section VII. In order to simulate the DC-DC converter more closely, blocking diodes were placed in the outputs of each of these DC supplies so that their internal filters were isolated from the reactive currents of the power stage.

The low level logic circuitry was connected to this power stage to complete

the low power breadboard. This breadboard was then operated at low DC input voltages in order to determine its operating characteristics. Although the inverter appeared to operate properly, large short circuit currents were observed in the collectors of the four power transistors. The duration of these short circuit currents ranged from three to ten microseconds. In order to simplify the investigation of this problem, the power stage was reduced to two transistor switches and their associated circuitry. The load resistance was changed to 20 ohms while the AC filter inductor and capacitor were changed to 0.84 millihenries and eight microfarads respectively. It was found that these short circuit currents were caused by the finite switching times of the 2N2583 power transistors. The storage and fall times of these power transistors are usually longer than their delay and rise times. Therefore, the transistors in both half phases for this power stage can be conducting simultaneously for the time differential between these turn-on and turn-off times, placing a short circuit across the two DC supplies. The magnitude of this short circuit current is limited by the external circuit, the DC supply impedance and the base drive current to these power transistors. In this circuit the base drive current is limited to a value sufficient to switch ten amperes peak collector current and still maintain a small collector to emitter voltage drop. As the collector current exceeds ten amperes, as is the case for these short circuit currents, the power transistors go out of saturation and larger voltages appear across their collector to emitter junctions, limiting the short circuit currents. Large peak powers are generated in the junctions of these power transistors which will cause them to fail if their peak power ratings are exceeded. Most of the power transistor failures that occurred during the testing of this breadboard have been caused by these short circuit currents.

A large discrepancy in the switching times occurred for these power transistors when they were tested in the Delco test circuit and when they were used in the pulse width modulated power stage. The switching times and especially the transistor storage times were found to be two to four times longer when the transistors were operating in the power stages. These increases in the switching times further aggravated this short circuit current problem and reduced the maximum modulation index, M, that could be used. A detailed investigation of this problem revealed that these switching times are essentially independent of the type of load that is used in the collector circuit as long as the collector current has the same magnitude. However, the switching times are reduced as the collector current magnitude is increased for a fixed base drive current. This is to be expected since the power transistor comes progressively out of saturation as this collector current is increased. These results still did not account for the large switching time discrepancies. It was found that the leakage inductance and the available sweepout voltage in the constant voltage base drive circuits were major factors in causing these long

switching times. Therefore, modifications of the base drive circuitry were investigated in an attempt to eliminate these problems and maintain high power stage efficiencies with a minimum amount of waveform distortion. The following circuit configurations and techniques were tried with varying degrees of success.

1. Delayed Turn-on Using Timing Core

A time delay circuit was placed in the base drive circuitry of each power transistor as shown in Figure 4. This time delay is made longer than the maximum switching time differential that occurs between the power transistors in order to eliminate the short circuit problem. Therefore, each base drive turn-on signal is delayed to each of the power transistors so that the previously conducting transistor will turn off before the base drive turn-on signal is applied to the transistor in the opposite half phase. Examining this circuit for the unmodulated case reveals that the output voltage of the drive transformer, T1, is a 10KC square wave. When this voltage becomes positive, current to the power transistor base is delayed by saturable reactor T2. In order to prevent power transistor Q1 from being turned on by the reactor, T2, exciting current, the base end of its set winding, N1, is returned through the parallel combination of R2 and C2 to a point that is more negative than the emitter of Q1. After an eight to ten microsecond time delay, the reactor saturates and positive turn-on current is provided to the power transistor base through the parallel combination of R1 and C1. When the transformer voltage reverses, the power transistor base circuit is reversed biased, sweeping the charge out of the base-emitter junction through fast-recovery diode CR1 and reset winding N2. The resulting reverse current that occurs during this sweepout time aids in resetting T2. The saturable reactor is also reset by the reverse current flowing through the parallel combination of R2 and C2 and windings N1 and N2 during this negative half cycle.

The short circuit currents were eliminated with this circuit for both the unmodulated and modulated cases. The long switching times of the transistors, however, required that the time delay be set for at least eight microseconds. This long time delay limited the maximum modulation index to 0.7. A modulation index greater than this caused the loss of the minimum-width pulses and introduced additional harmonic distortion to the 400 cycle power frequency which would require additional filtering to reduce. Reduction of the time delay below eight microseconds allowed higher modulation indexes to be obtained, but short circuit currents began to appear. For this reason it seemed necessary to find a method that would cause the power transistors to turn off faster.

DELAYED TURN-ON USING TIMING CORE

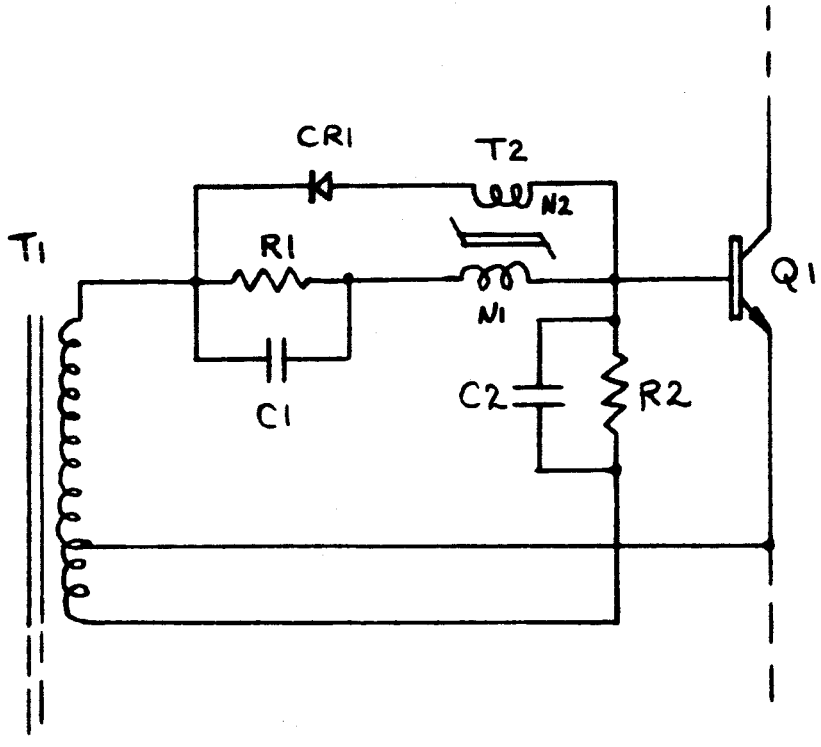


FIGURE 4

2. Drive Circuit Using Timing Core and Base-Collector Diode

A modification of the base drive circuit described above is shown in Figure 5. This circuit uses a high speed diode clamp to keep the power transistors out of saturation by diverting some of their base drive current to the collector. The series base drive resistor was divided into two resistors, R1 and R2. After the time delay during the positive half cycle, full base drive current is available to the power transistor. At this time, fast recovery diode CR2 is reversed biased. However, as the collector potential drops below the potential at the junction between R1 and R2, diode CR2 becomes forward biased, diverting some of the base current into the collector circuit. The amount of base current that will be diverted depends on the R2/R1 ratio selected and will become larger as the R2/R1 ratio is increased.

The transistor switching times and especially its storage time were effectively reduced by operating these power transistors out of saturation. The minimum time delay of the saturable reactor could be reduced to five microseconds before short circuit currents began to appear. A maximum modulation index of 0.8 was obtained before the minimum-duration pulses began to disappear. An overall efficiency of 80% was obtained for the power stage which consisted of one power transistor in each half phase. Although improvements in efficiency and modulation index were obtained, they were still below the required levels of 90% efficiency and a modulation index of 0.9. Therefore, further improvements in the base drive circuitry were required in order to obtain transistor switching times that approach their test condition values.

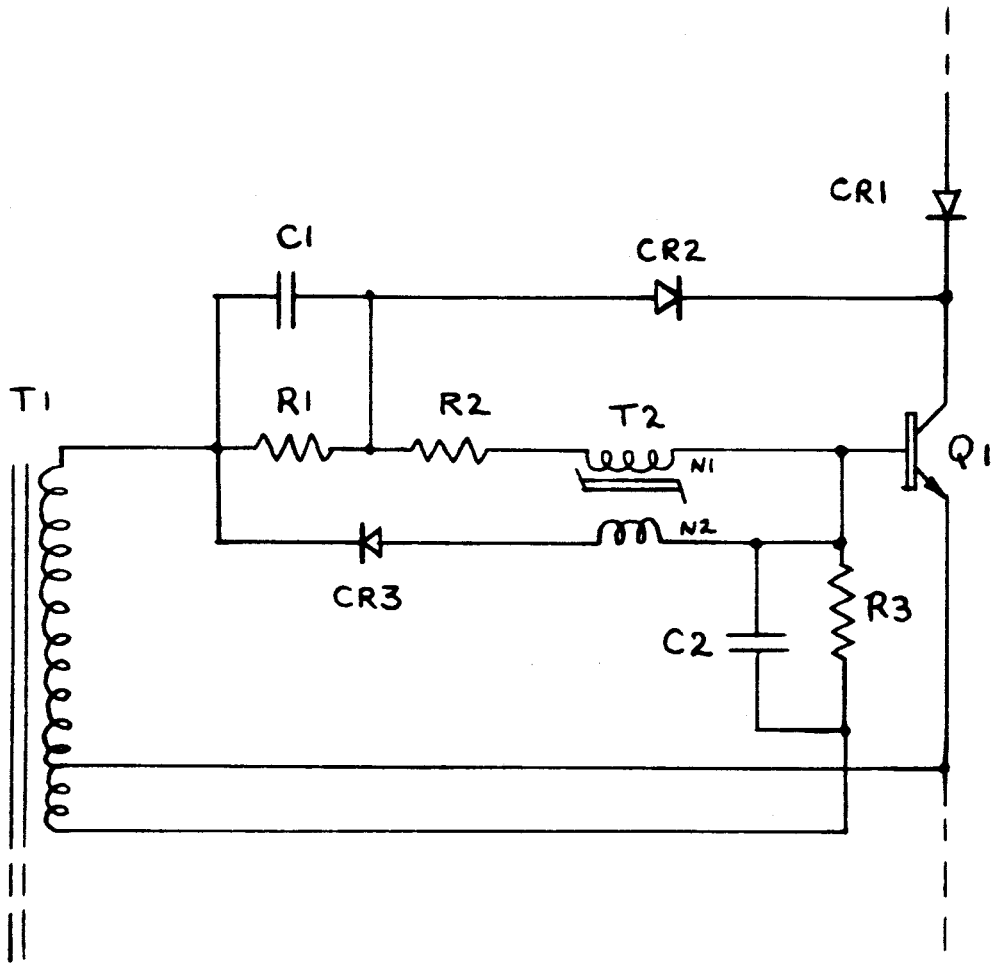
3. Split Output Filter Inductor Approach

The AC filter inductor was split up and placed in each half phase in an attempt to limit the rate of rise of this short circuit current as shown in Figure 6. The original voltage drive circuit was used to supply the base drive current. The reactive current diodes CR2 and CR6 were connected in a cross-coupled configuration to provide a reactive current path for these split inductors. Examining this circuit reveals that the individual filter inductors will be required to carry unidirectional load current as well as the current that develops during the short circuit conditions. The circuit operates as follows:

a) Assume transistor Q1 is just turning on while transistor Q2 is just turning off.

b) At this time a short circuit occurs between Q1 and Q2 placing inductors L1 and L2 across the two DC power supplies (+V, -V). During this short circuit time interval the inductors limit the rate

BASE DRIVE USING TIMING CORE & SATURATION PREVENTING DIODE



R1	0.6 Ω	CR1	IN3913
R2	0.6 Ω	CR2	IN 3886
R3	5 Ω	CR3	IN4001
C1	1 μf	T1	DRIVE TRANSFORMER
C2	0.5 μf	T2	TIMING CORE, MAGNETICS 80615-½D N1 = 4 TURNS N2 = 2 TURNS
Q1	2N2583		

FIGURE 5

POWER STAGE WITH SPLIT FILTER INDUCTOR

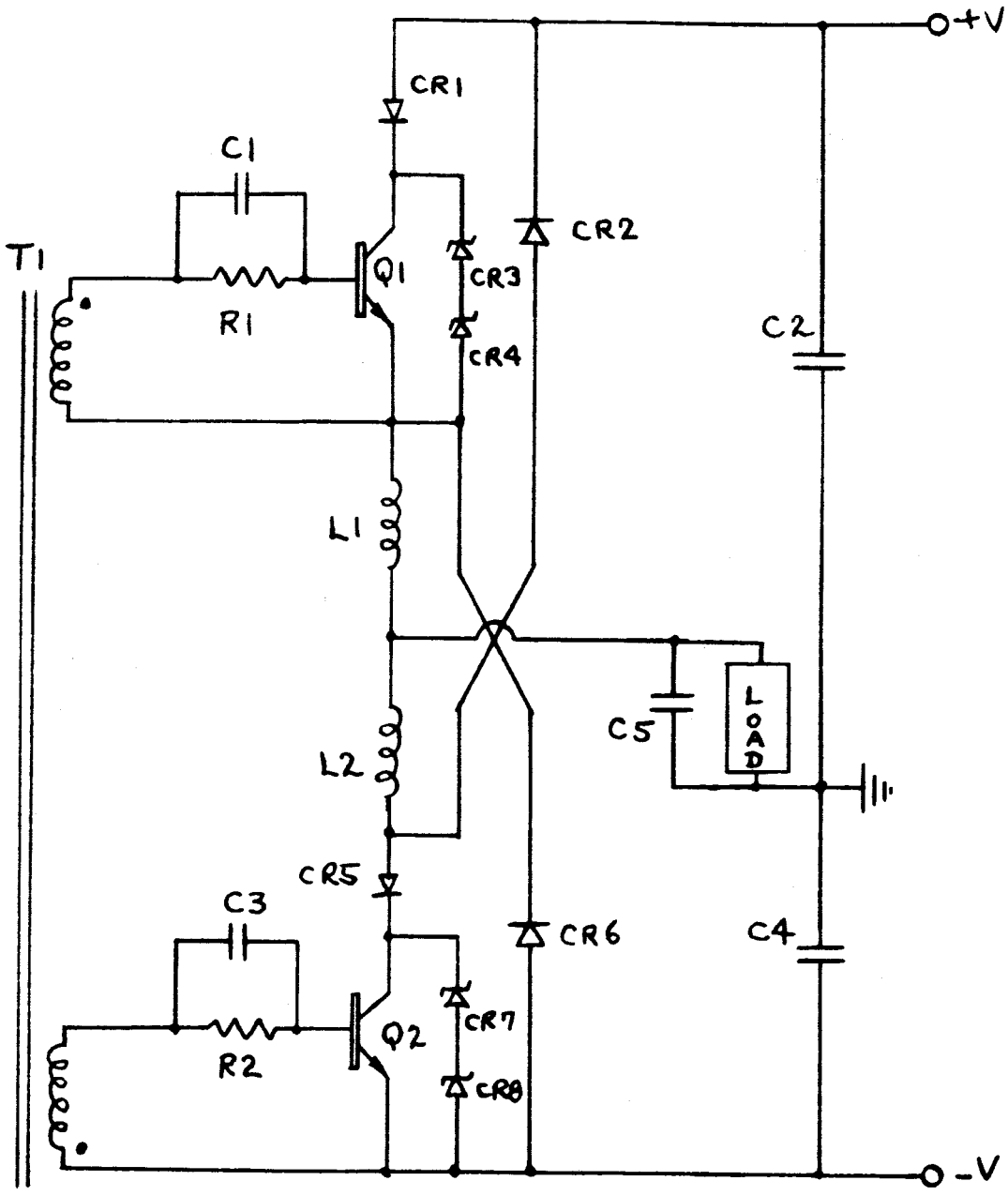


FIGURE 6

of current rise to a low value, determined by the L/R time constant of the circuit.

c) During the same time interval, the load current starts to flow through Q1, L1, load, and C5 for a unity power factor load.

d) After the storage and fall times of Q2 have elapsed, it turns off, and the short circuit path is removed.

e) However, inductor L2 tries to maintain this short circuit current level by reversing its polarity and diverting its current through the parallel current paths composed of CR2, CR1, Q1 and L1, and CR2, C2, load and C5.

f) The reverse procedure occurs when Q1 turn off and Q2 is just turning on.

An equilibrium point is obtained for the magnitude of the short circuit current that is determined by the L/R ratio of the parallel discharge path. The resultant energy storage of these inductors caused by the short circuit currents reduced the efficiency of the power stage and distorted the load voltage waveform, although the short circuit current was minimized.

This basic circuit approach was modified in a number of ways in order to improve the power stage efficiency. However, an efficient usage of the energy stored in the inductors due to the short circuit currents was not obtained with these approaches.

4. Current Sense and Drive Inhibit Approach

Various current feedback sensing circuit approaches were tried in an attempt to eliminate the short circuit problem and to simplify the drive circuitry. The most promising of these approaches utilized a current transformer to sense the individual current pulses that occurred when the power transistors in each half phase were turned on. Therefore, the current transformer was placed in the common line between the power transistor and the AC filter - reactive diode combination. The corresponding voltage pulses developed on the secondary windings of this current transformer were used to inhibit the drive signals to the transistor in the half phase that was trying to turn on until the transistor in the opposite half phase had completely turned off. The short circuit currents were effectively eliminated over the major portion of each power frequency cycle. However, short circuit currents appeared at the low current levels as the 400 cycle current waveform crossed through zero. Therefore a very sensitive and stable circuit would be required on the secondaries of this current transformer in order to amplify and clip these very low level

current pulses. The additional amplifier and level sensing circuitry would increase the complexity of thiscircuit approach. Improvements in the constant voltage base drive circuit used in this approach will be required in order to reduce the power transistor switching times so that a higher modulation index and improved power stage efficiency can be obtained. Further investigation of these current feedback approaches was terminated because of the circuit complications that were encountered.

5. Delayed Turn-on Using Shunt Transistor

The basic delayed turn-on base drive circuits, discussed in Sections 1 and 2 were modified to improve the base current rise time that is applied to the power transistors in order to reduce their turn-on switching losses. Figure 7 is a schematic of this circuit approach. The rise time of the base current is limited by the L/R ratio established by the transformer leakage inductance and winding resistance, lead inductance and resistance, and the equivalent load resistance. Examining this circuit reveals that the time delay at turn-on is facilitated by the shunting transistor, Q1, rather than the series saturating reactor used in Sections 1 and 2. The time delay is generated by saturating transformer T2 which is driven from the same drive circuit as the normal drive transformer, T1. As the voltage at the secondary of T1 goes positive, a voltage is applied to the base of shunt transistor Q1 from transformer T2. The emitter of Q1 is returned to a voltage which is more negative than the emitter of power transistor Q2 so that its base-emitter junction remains reversed biased while Q1 is conducting. Therefore, during the delay time while Q1 is conducting, the base current is diverted from the power transistor, Q2, keeping it turned off. At the end of the delay time, Q1 stops conducting and the current is switched into the base of Q2. Since the delay time is longer than the voltage rise time at the secondary of T1, almost full base current is switched into the base of Q2 with a significant reduction in the base current rise time. A clamping diode, CR6, (discussed in Section2) is used to decrease the storage and fall times of power transistor Q2 by keeping it slightly out of saturation.

The base current rise times were reduced to between 0.2 and 0.4 microseconds for this drive circuit approach compared with current rise times of between 1.5 and two microseconds that were obtained for the delayed base drive circuits in Sections 1 and 2. With this circuit in Figure 7, it was possible to use a single drive transformer, T1, for one complete phase. Only the parts included in the dotted section must be repeated for each parallel power transistor stage. A new drive transformer designed to handle a complete phase was constructed with the additional bias voltage windings. The transformer output rise time was measured to be between one and 1.5 microseconds with a 7 ampere non-inductive load.

DELAYED TURN-ON USING SHUNT TRANSISTOR

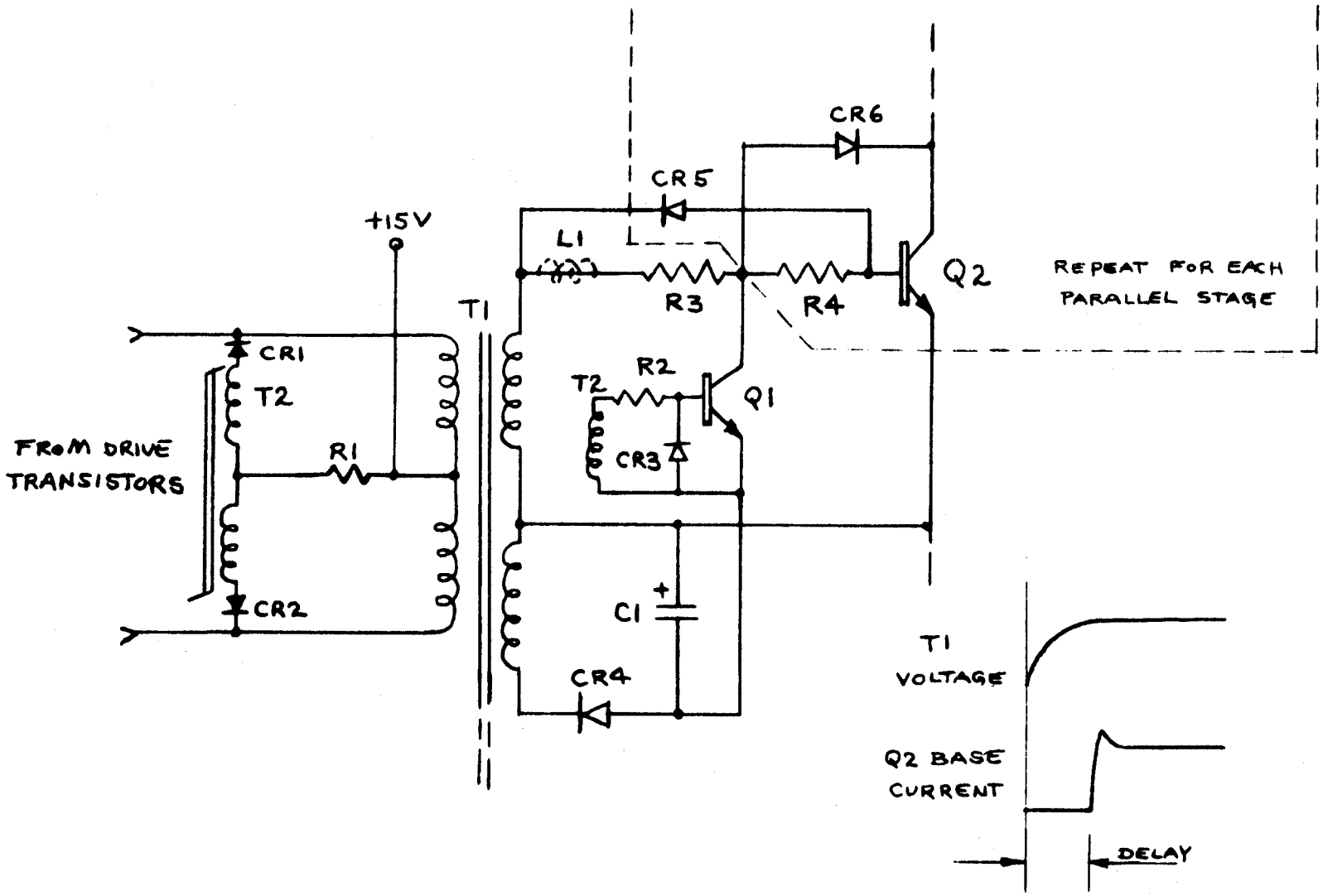


FIGURE 7

Electrical data at unity and 0.7 power factor load conditions were obtained for the power stage using this base drive approach and is tabulated in Table 2. The data was taken for one pair of 2N2583 power transistors with no parallel stages and no balancing reactors. The power stage efficiencies that were obtained are higher than those obtained by using the drive circuits previously discussed. This was mostly due to the improvement in the base current rise time which reduced the turn-on losses.

6. Parallel Operation Using Shunt Delayed Turn-on Drive

The circuit described in Section 5 was selected to be used to provide the base drive current for operation of two power transistors in parallel in each half phase of the power stage. Here a set of balancing reactors were used to force proper current sharing in the parallel set of transistors. Although these balancing reactors were very effective in equalizing the load current among the paralleled transistors during their conduction times, current unbalance problems occurred during the power transistor switching times. The unbalance in load current during these switching times was caused by inherent differences in the delay and rise times and storages and fall times of these power transistors. The majority of this current unbalance occurred during the storage and fall times where the peak load currents occur for lagging power factors. Also, the turn-off time for these power transistors is usually considerably longer than their turn-on time and the forward base drive rise time in this circuit is very fast so that the paralleled transistors turn on together.

The unbalanced turn-off time problem can be quite severe when considering several transistors operating in parallel, because the transistor having the longest storage and fall time must assume the collector currents of the other transistors which turned off first. Therefore, in the case of N paralleled transistors, the current that tries to flow through the slowest device can be as high as N times its normal peak value. Thus very large peak currents and hence peak powers can be created in the slowest transistor for this difference in turn-off time because it will be base drive limited for a collector current of slightly greater than ten amperes. Degradation of the transistor junction and evantual failure will occur for the slowest transistor unless this current unbalance problem can be eliminated. Various circuit modifications were tried in order to eliminate this current unbalance problem and still maintain high power stage efficiency with a minimum amount of waveform distortion.

The first attempt to eliminate this current unbalance problem was to replace the original balancing reactors with larger ones which were designed to support 200volts for ten microseconds. These new reactors did not limit the peak current in the slowest transistor, but only limited the rate

TABLE 2. Data and Conditions for Two (2) 2N2583 Transistors Operating in Power Stage with Delayed Turn-On Using Shunt Transistor

	Case I	Case II	Case III
DC Input Volts	140	140	140
Carrier Frequency	10 KC	10 KC	7KC
Modulation Index	0.77	0.77	0.83
Power Factor	1.0	0.7	1.0
Power Out (watts)	300	220	350
Filter Inductor	0.84 mh	0.84 mh	1.06 mh
Filter Capacitor	8μf	8μf	8μf
Power Stage Efficiency	86%	85%	88%

of rise for this unbalanced current. In addition, large induced voltages were impressed across the faster power transistors during these switching intervals. Zener diodes are placed across the power transistors to protect them from these large induced voltages; however, additional losses will occur if larger balancing reactors are used. Therefore, the use of larger volt-second balancing reactors was not the solution to this current unbalance problem.

7. Parallel Operation Using Separate Filter Inductors and Reactive Diodes

An approach which worked quite well in eliminating the turn-off current unbalance was to split the filter inductor into as many parts as there are parallel stages in each phase. This circuit approach is shown in Figure 8. The value of each of these filter inductors will be N times the value that would be required for one common filter inductor, where N is the number of paralleled filter inductors required. Separate reactive diodes were needed for each of these inductors in order to provide a continuous path for the reactive currents. A basic disadvantage of this approach was that it required separate base drive circuits for the positive half phases in order to maintain the required isolation between the paralleled power transistors. This eliminated the common base drive approach and increased the number of circuit components required. A common base drive circuit could be used if a PNP complimentary power transistor could be found that would replace the present NPN power transistors in the positive half phases. However, an extensive investigation revealed that no PNP power transistor was available that could match the power transistor specifications required.

The split inductor approach was tried on the two parallel stages in the laboratory and was successful in eliminating the current unbalance. As the fastest transistor, say Q1, turned off, the voltage across its inductor reversed and current passed through the associated reactive diode. Current through the slowest transistor, Q2, did not increase during this time interval because of the isolation provided by the separate filter inductors. Separate blocking diodes were found to be required for each of the power transistors if clamping diodes were used in the base drive circuitry to keep the power transistors partially out of saturation. The separate blocking diodes prevent the base drive currents for each power transistor from flowing in the other power transistor circuits. These additional fast recovery blocking diodes will further increase the number of power stage components required. Although this circuit approach worked quite well in eliminating the current unbalance, it resulted in a very complex circuit that has a large parts count when more than three power transistors are paralleled for each half phase. For example, the original parts count for the proposed 5 KW, three-phase power stage and filter was 255. Using this approach, the parts count increased to approximately 550.

PARALLEL OPERATION USING SEPARATE

INDUCTORS AND REACTIVE DIODES

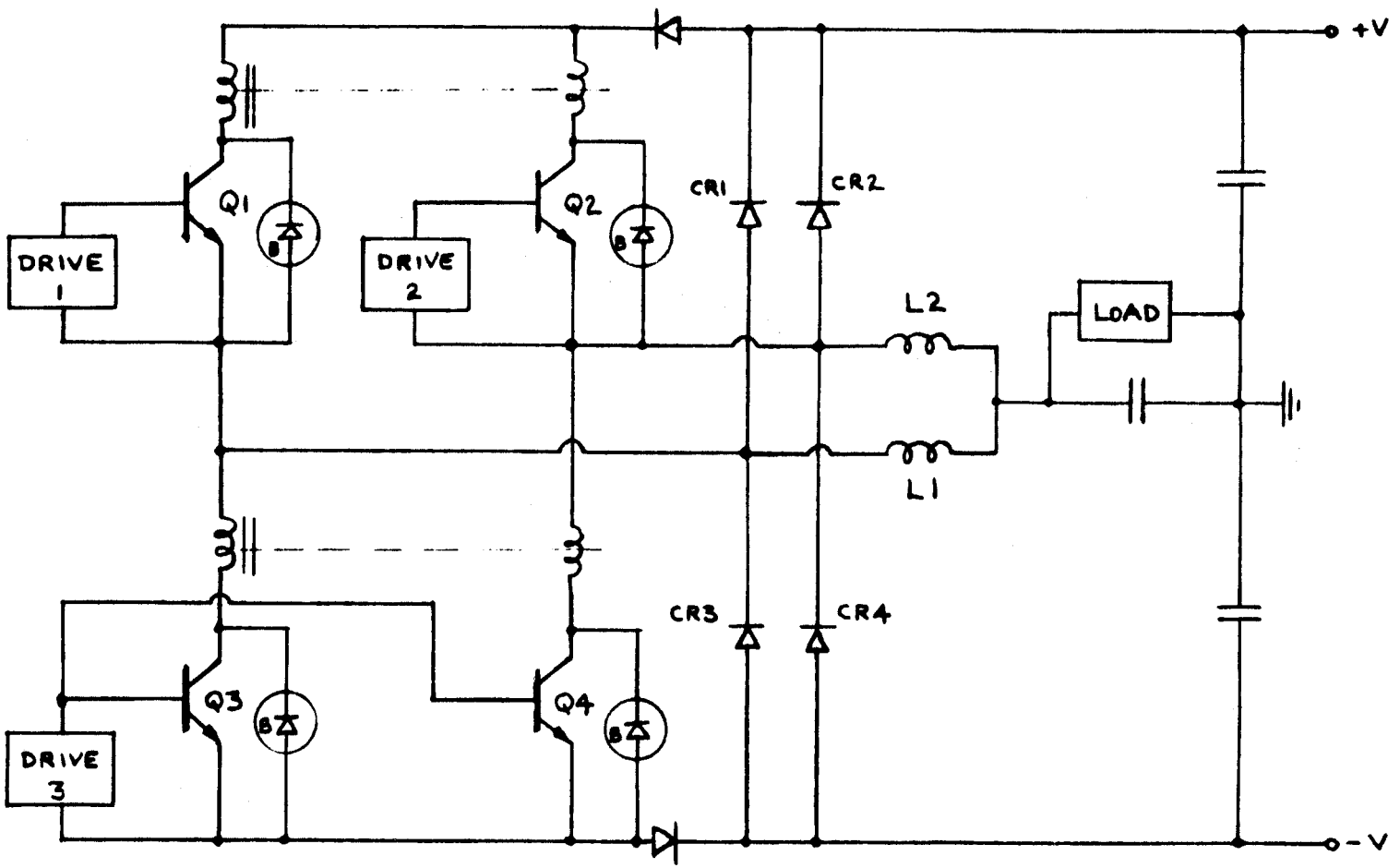


FIGURE 8

Therefore, a better solution was sought for this current unbalance problem.

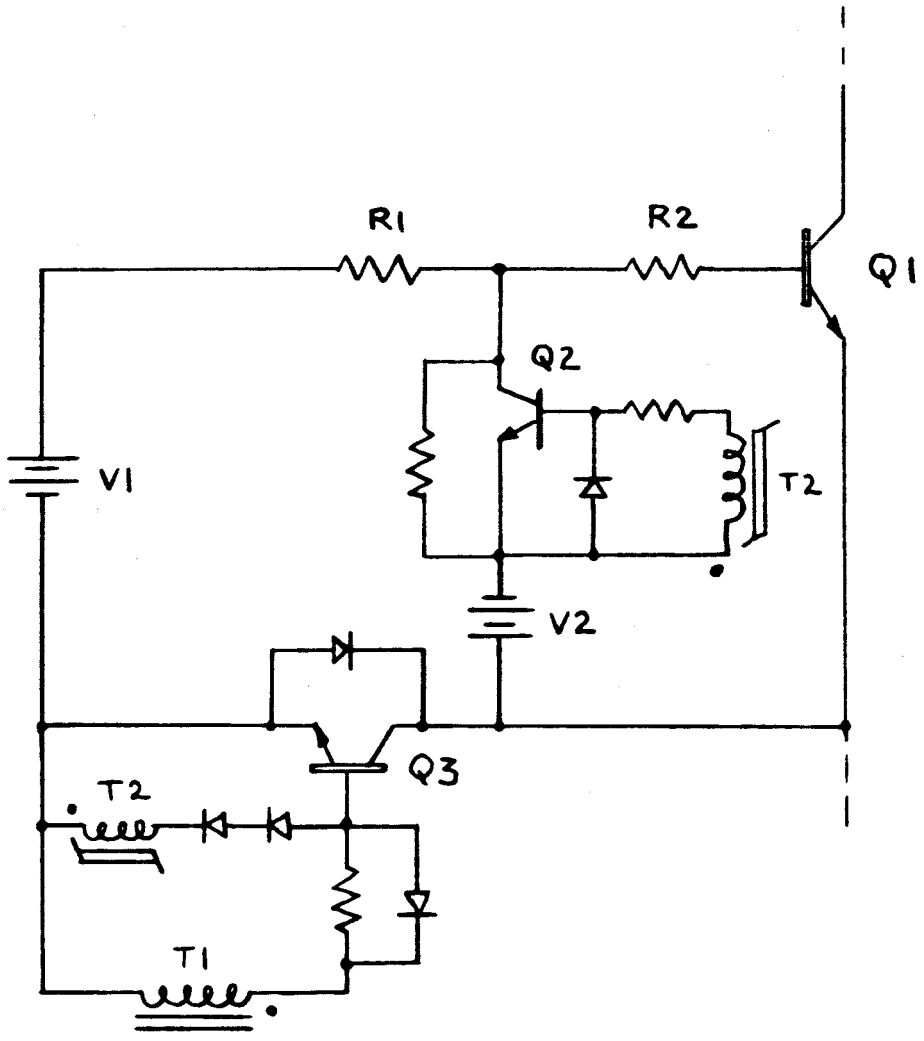
8. Series Delay Turn-on and Forced Turn-off

Discussions with Delco, the manufacturer of the 2N2583 power transistor that was selected for the power stage, revealed that higher reverse bias voltages and sweepout currents can be used to reduce their storage and fall times. Therefore, the maximum reverse base-emitter voltage of five volts specified in their data sheets can be exceeded providing that the average power dissipation in this junction is kept below 12 watts. They indicated that they were not able to predict transistor performance by testing them in a simple switching time circuit with a resistive load. They found that the storage time varied significantly as a function of the circuit configuration used. Their only suggestion was that they test their transistors in our circuit in order to select transistors for a narrow range of storage times and matched gains. These selected transistors would minimize this current unbalance problem without resorting to any circuit modifications. However, they indicated that the yield for these matched transistors would be very low, thus effecting delivery time and cost. A new part number would be assigned to this selected transistor, so that subsequent transistors could be ordered from this specification.

It was decided for the present that matched transistors would limit the usefulness of this inverter because of the low yield that would be obtained. Therefore, a further modification of the power transistor base drive circuit was made in order to reduce the storage time by increasing the sweepout currents and provide some control in matching their switching times. A simplified base drive circuit for one half phase is shown in Figure 9. A series switching transistor, Q3, was used to delay the turn-on current to the power transistor, Q1, while the shunt transistor, Q2, provided a path for the power transistor sweepout current when it was turning off. Forward drive current to the power transistor was obtained from the isolated power supply, V1, while the sweepout current was obtained from the isolated power supply, V2. The drive transformer, T1, modulated the series switching transistor with the pulse width modulated waveform. Very fast rise times were obtained from this drive transformer because of the gain of transistor Q3 which resulted in a very low L/R ratio. Both the isolated DC power supplies, V1 and V2, and their lead wires must have very low self-inductances in order to keep the current rise times to one microsecond or less. The series and shunt transistors, Q3 and Q2, have switching times that are at least five times faster than the power transistors.

Using this base drive circuit, power transistor switching speeds and efficiency data were taken on the power stage that had only a single pair

SERIES DELAY TURN-ON & FORCED TURN-OFF



DRIVE TRANSFORMER

FIGURE 9

of power transistors. The power transistor storage time was reduced to an average of three microseconds at full load current of ten amperes when the reverse bias power supply, $V2_1$ was increased to minus eight volts. Further increase in the magnitude of this negative bias only resulted in increased dissipation in the base-emitter junction and did not cause any further decrease in the transistor storage time. A significant reduction in the power transistor storage time at full load was obtained with this circuit. Blocking diodes placed in series with the overvoltage protection zener diode circuits around each power transistor were helpful in obtaining these storage times by eliminating this path for the collector to base current that occurred during sweepout. These fast recovery blocking diodes also improved the switching speeds of the zener diodes by minimizing their shunt capacity effects.

The efficiency data was taken with a unity power factor load and is tabulated in Table 3. The resultant efficiency of 90.2% was 2.2% higher than was obtained in Table 2 for the base drive circuit described in Section 5. This improvement in efficiency can be attributed mainly to the decrease in the turn-off losses which resulted from the reduction of the storage time. The losses associated with the AC output filter were included in these efficiency measurements.

Unlike the base drive compensation offered by the base-collector diodes in the drive circuit described in Sections 2 and 5, the storage time will not be compensated in this base drive circuit approach since the base drive current will remain constant independent of the collector current. Therefore, the power transistor storage time will increase as the collector current decreases with load. The longest storage time will occur when the collector current is zero. Thus, the time delay must be adjusted for this case when the power stage is modulated in order to prevent short circuit currents from occurring between the transistors in each half phase.

Two power transistors were connected in parallel for each half phase, as shown in Figure 10. One common base drive circuit was used for each half phase. Even though the storage and fall times of the power transistors have been reduced by using this base drive circuit, the turn-off time current unbalance problem still existed to a small degree. The maximum turn-off time differential can be as high as two to three microseconds during which time the slowest transistor will be required to carry the full load current. The storage and fall times of these power transistors can be adjusted to a certain extent by adjusting the magnitude of the sweepout current in each transistor. This can be accomplished by adjusting the values of the shunt resistors, R2, R4, R6, and R8. To reduce the transistor's storage and fall times, the value of its associated resistor must be decreased. Increasing this resistance will increase the transistor storage and fall times. The matching is usually attempted to the fastest

TABLE 3. Data and Conditions for Two (2) 2N2583 Transistors Operating in Power Stage Using Series Delay Turn-On and Forced Turn-Off

DC Input Volts	150
Carrier Frequency	7KC
Modulation Index	0.838
Power Factor	1.0
Power Out (Watts)	398
Filter Inductor	1.06 mh
Filter Capacitor	8μf
Load Resistor	20 ohms
Power Stage Efficiency	90.2%

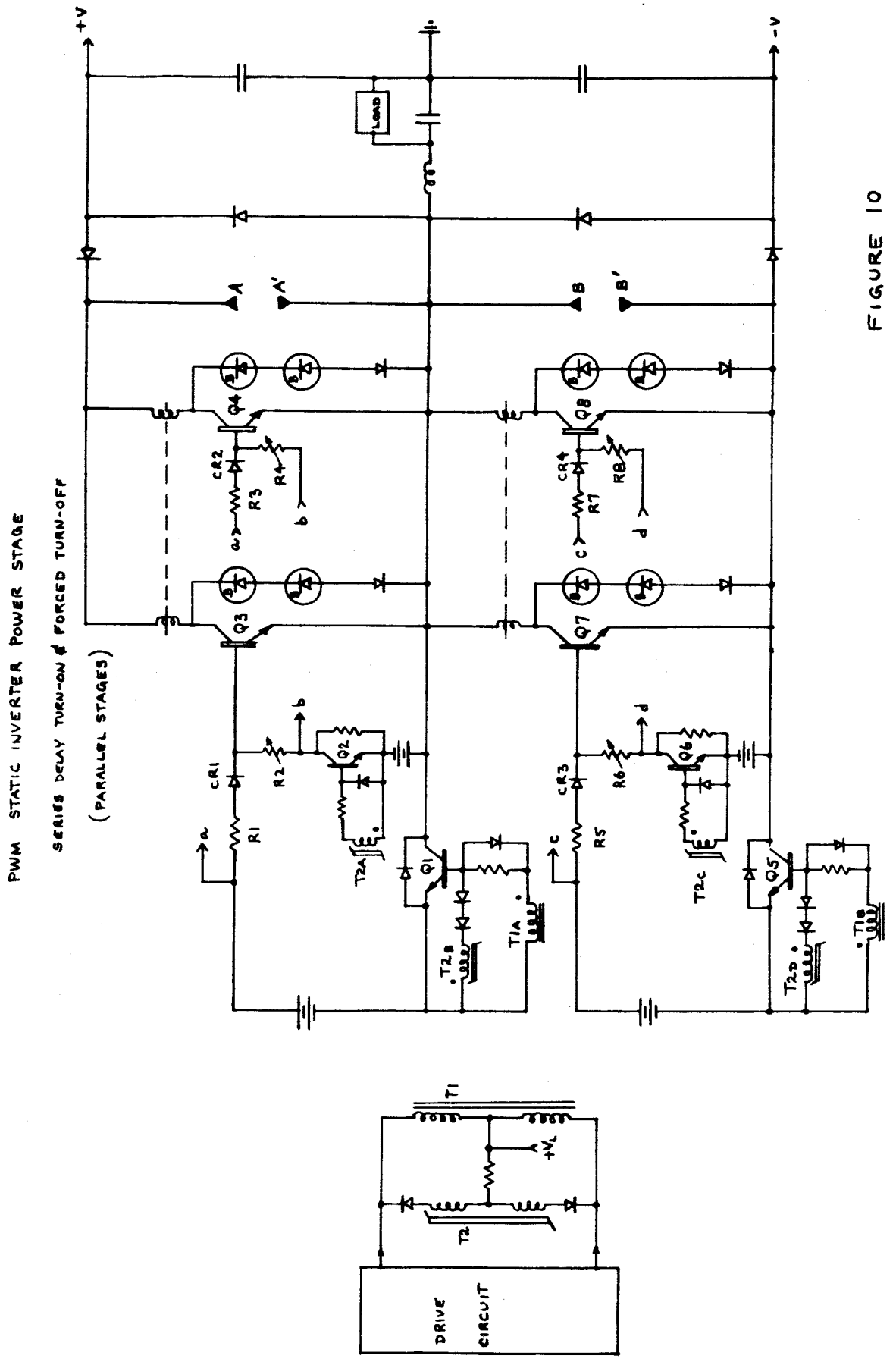

PWM STATIC INVERTER POWER STAGE
SERIES DELAY TURN-ON & FORCED TURN-OFF
(PARALLEL STAGES)
+V
-V
LOAD
A
A'
B
B'
Q4
Q8
Q3
Q7
Q2
Q6
Q1
Q5
CR1
CR2
CR3
CR4
R1
R2
R3
R4
R5
R6
R7
R8
a
b
c
d
T2A
T2B
T2C
T2D
T1A
T1B
T1
T2
+V
DRIVE
CIRCUIT

FIGURE 10

transistor in each half phase. However, limitations in the average power dissipation of the base-emitter junction and their avalanche breakdown voltages will create a compromise in this matching. Fast recovery diodes, CR1 through CR4, were added to block the shunting effects of R1, R3, R5, and R7 during the turn-off time interval.

Trimming these shunt resistors, R2, R4, R6, R8, was effective in eliminating this current unbalance problem. However, this approach has the disadvantages that when one transistor fails and must be replaced, the new transistor must have its sweepout resistor adjusted to match the switching times of the other transistors.

The peak sweepout current for each power transistor varied from three to four amps. Therefore, for the 5KW, three phase power stage, shunting transistors Q2 and Q6 must be capable of switching currents as high as 25 amperes for seven power transistors in parallel. The series turn-on transistors, Q1 and Q5, must be able to switch peak currents between eight and nine amperes. Twelve isolated low impedance DC voltages will be required for the base drive circuitry for this full power inverter.

9. Clamping Circuits

Clamping circuits were evaluated as an alternate means of eliminating this current unbalance in place of trimming the power transistor sweepout currents. The connection for these clamping circuits which essentially shunt the power transistors, are shown at points A-A' and B-B' of Figure 10. The clamps form a low impedance path across the power transistors and assume the load current as the transistors turn off. The following clamping circuits were investigated to determine their effectiveness. Figure 10 should be used as a guide when examining these circuits.

a) The first clamping circuit that was tried is shown in Figure 11. It consisted of a capacitor which was used to divert the unbalanced current at turn-off. This circuit was connected at points A-A' and B-B' of Figure 10. Capacitor C is clamped to essentially zero voltage by the conduction of transistors Q3 and Q4. At the end of the positive conduction period transistor Q3 starts to turn off before Q4. Transistor Q4 will then assume the full load current and its collector-to-emitter voltage begins to increase. However, capacitor C diverts this load current when series diode CR conducts. Therefore, as the voltage across transistors Q3 and Q4 finally turns off, transistor Q4 turns off into a low voltage determined by the magnitude of the clamping capacitor, C. At this point, capacitor C charges up to twice the supply voltage as the load current is picked up by the reactive diode. Capacitor C remains charged until the beginning of the next positive conduction period when it discharges through transistors Q3 and Q4

CAPACITOR - DIODE CLAMP

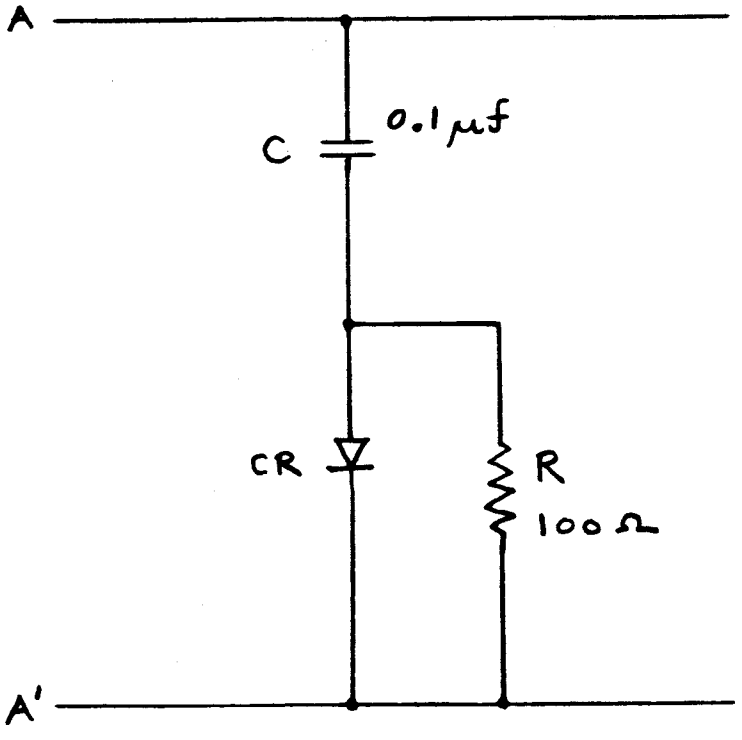


FIGURE 11

and resistor R. This circuit was effective in clamping the unbalanced current with the values specified in Figure 11. However, additional transistor losses were obtained because of the discharge currents of the capacitors. In addition, short circuit currents occurred between the two half phases because the time constant of the capacitor and the AC filter - load combination exceeded the turn-on time delay of transistors Q7 and Q8 in the negative half phase. Reducing the size of capacitor C to less than 0.05 microfarads eliminated the short circuit problem but the circuit was only partially effective in eliminating the unbalanced current at turn-off. A larger value of capacity will assume more of the load current and allow the slowest transistor to turn off into a lower voltage thus reducing its turn-off losses. But this would require that the turn-on time delay be increased to a value that would eliminate the short circuit problem. The extension of this delay would require a reduction of the carrier frequency in order to obtain a modulation index of 0.9. This would, in turn, increase the AC filter weight and size.

b) A modification of the clamping circuit described above is shown in Figure 12. This circuit uses two SCR's to replace the diode and resistor of the previous clamping circuit. The advantage gained with this circuit is that an external discharge path is provided for capacitor C by SCR-2, thus eliminating the additional losses in the power transistors. Capacitor C and SCR-1 are clamped to essentially zero voltage by the conduction of transistors Q3 and Q4. At the end of the positive conduction period, transistor Q3 starts to turn off before Q4. However, SCR-1 has been gated on with the reversal of the power transistor base drive voltage and will provide a shunting path for the load current through capacitor C. Therefore, the voltage across transistors Q3 and Q4 is clamped down until Q4 finally turns off. Again transistor Q4 will turn off into a low voltage determined by the size of the clamping capacitor, C. At this point, capacitor C charges up to twice the supply voltage and SCR-1 turns off as the charging current falls below its holding current. Capacitor C remains charged until the beginning of the next positive conduction period when SCR-2 is gated on, discharging capacitor C which in turn returns SCR-2 to its blocking state.

Identical results were obtained for this clamping circuit as were obtained for the previous circuit. Short circuit currents were eliminated when the capacitor value was made less than 0.05 microfarads. The time constant of the capacitor, C, and the AC filter - load combination must be shorter than the turn-on time delay in order to allow SCR-1 to be in its blocking state before SCR-2 is gated on. Otherwise, a short circuit path will develop between SCR-1 and SCR-2 which will damage the power transistors in the opposite half phase at

CAPACITOR - SCR CLAMP

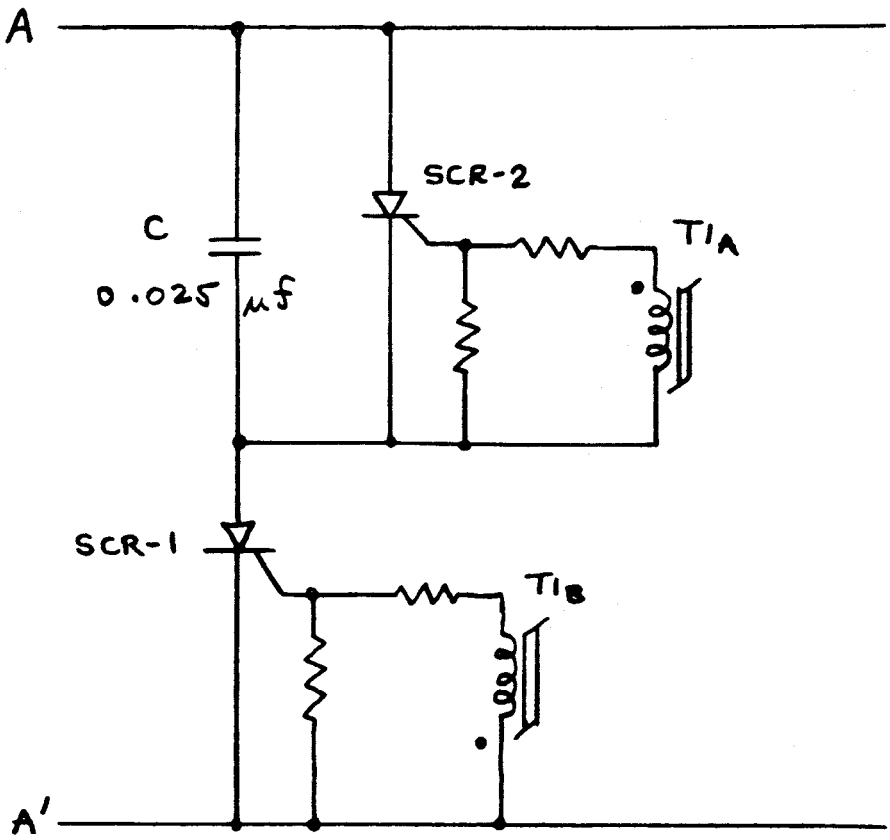


FIGURE 12

the beginning of the next half cycle. The SCR's misfired during modulation when the DC source voltages were made greater than 90 volts each. These misfires were apparently caused by dv/dt turn-on. Some improvement was obtained by placing R-C stubs across the SCR's but they reduced the clamping effect of the circuit.

The power stage efficiency was found to be lower when this clamping circuit was used. This reduction in efficiency was apparently caused by the energy absorbed in the capacitor during turn-off which must be dissipated as a loss in SCR-2 when the capacitor is discharged. Although this clamping circuit was effective in minimizing the unbalanced current during turn-off, the reduction in power stage efficiency and the time constant problem more than nullifies its usefulness. Therefore, the ideal clamping circuit should have a large current capacity with very fast switching times which are independent of the AC filter and load parameters.

c) A slow recovery diode was tried as a clamping circuit and is depicted in Figure 13. This diode was primed in the forward direction by the power transistor collector-to-base sweepout current which occurs at the end of the positive conduction period for transistors Q3 and Q4. This sweepout current flows up through the slow diode in the forward direction and then down through the collector-base junctions of the power transistors and back to the base circuit sweepout power supply. At the end of this sweepout time, as the fastest transistor, Q3, begins to turn off, the slow recovery diode becomes reversed biased due to the increase in the collector-to-emitter voltage drop of Q4 when it begins to assume the entire load current. The slow recovery diode will then conduct the load current in the reverse direction until it recovers its blocking characteristics. During this recovery time, transistor Q4 is clamped down and will turn off into a low voltage, thus reducing its turn-off switching losses and limiting the unbalanced current. The diode reverse recovery time was found to be a function of the load current for a fixed forward priming current. Therefore, as the load current was increased the recovery time became shorter for the unmodulated case. Different types of slow recovery diodes, such as the IN2157, IN1203, IN1401, and IN3267 were tried in this clamping circuit with varying degrees of success. The average reverse to forward current gains for these diodes ranged from five to ten.

The diode clamping circuit was very effective in eliminating the unbalanced current problem at low load current levels for the unmodulated case. However, as the source voltages were increased, which increased the load currents, the collector-to-base sweepout current became smaller thus lowering the priming current in the slow recovery

SLOW DIODE CLAMP

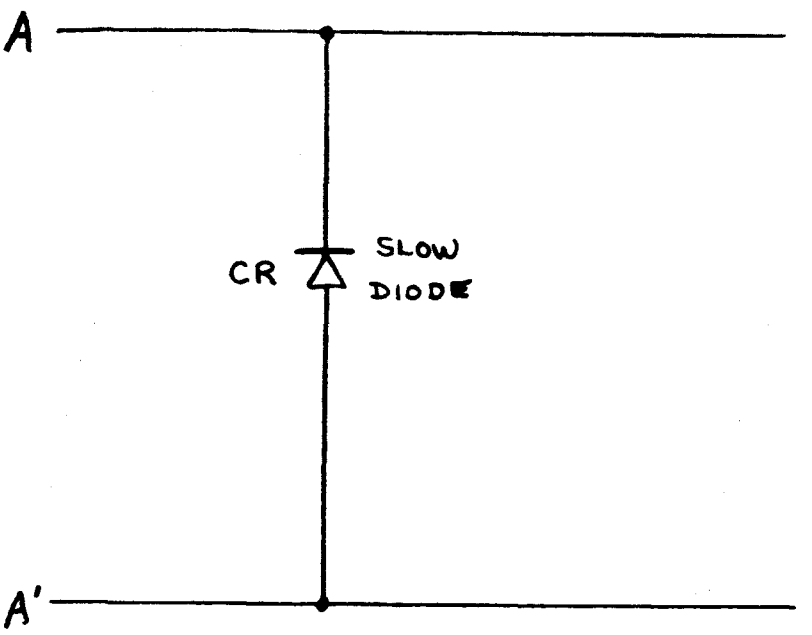


FIGURE 13

diodes. The reduction of this priming current decreased the effectiveness of this diode clamping circuit which in turn increased the amount of current unbalance handled by the slowest transistor. Therefore, an external priming circuit should be used to eliminate this problem.

d) A number of priming circuits were designed and tried for this slow diode clamping circuit. The results obtained from these circuits revealed that a constant priming current cannot be used under modulated conditions because the diode recovery time varies at a 400 cycle rate with the load current. Therefore, as the load current amplitude goes to zero the diode recovery time becomes longer than the fixed time delay of the base drive circuit. This results in short circuit currents between this slow recovery diode and the power transistors in the opposite half phase. Therefore, the magnitude of the priming current must be proportional to the load current and should be in phase with it for loads of any power factor. This will result in a fixed recovery time for the slow diodes throughout the modulated cycle which will eliminate these short circuit conditions. Such a circuit is depicted in Figure 14. In this circuit, a current transformer senses the load current that is switched by the power transistors. A priming current whose magnitude is determined by the turns ratio of this current transformer flows in the forward direction through the slow recovery diode, the power transistors (Q1 and Q2), and then back to the current transformer secondary. At the end of this positive conduction period transistor Q3 starts to turn off before Q4. However, SCR-1 has been gated on with the reversal of the power transistor base drive voltage and will provide a shunting path for the load current which passes in the reverse direction through the slow diode. The priming current in the secondary of the current transformer is diverted through SCR-1 at this time. The slow recovery diode will continue to conduct the load current in the reverse direction until it recovers its blocking characteristics at which time the load current drops to zero in the current transformer, allowing SCR-1 to return to its blocking state. During this recovery time, transistor Q4 is clamped down by the slow diode-SCR combination and will turn off into a low voltage, thus reducing its turn-off switching losses and eliminating the unbalanced current. Fast recovery diodes are shunted around the current transformer secondary windings to insure a continuous current path.

This diode clamping circuit was very effective in eliminating the unbalanced currents in the slowest transistor for any source voltage and modulation index level. A IN1203 slow recovery diode was used. The current transformer turns ratio was nominally set for 4:1, thus making the priming current one-fourth of the load current. The resultant

SLOW DIODE - CURRENT TRANSFORMER CLAMP

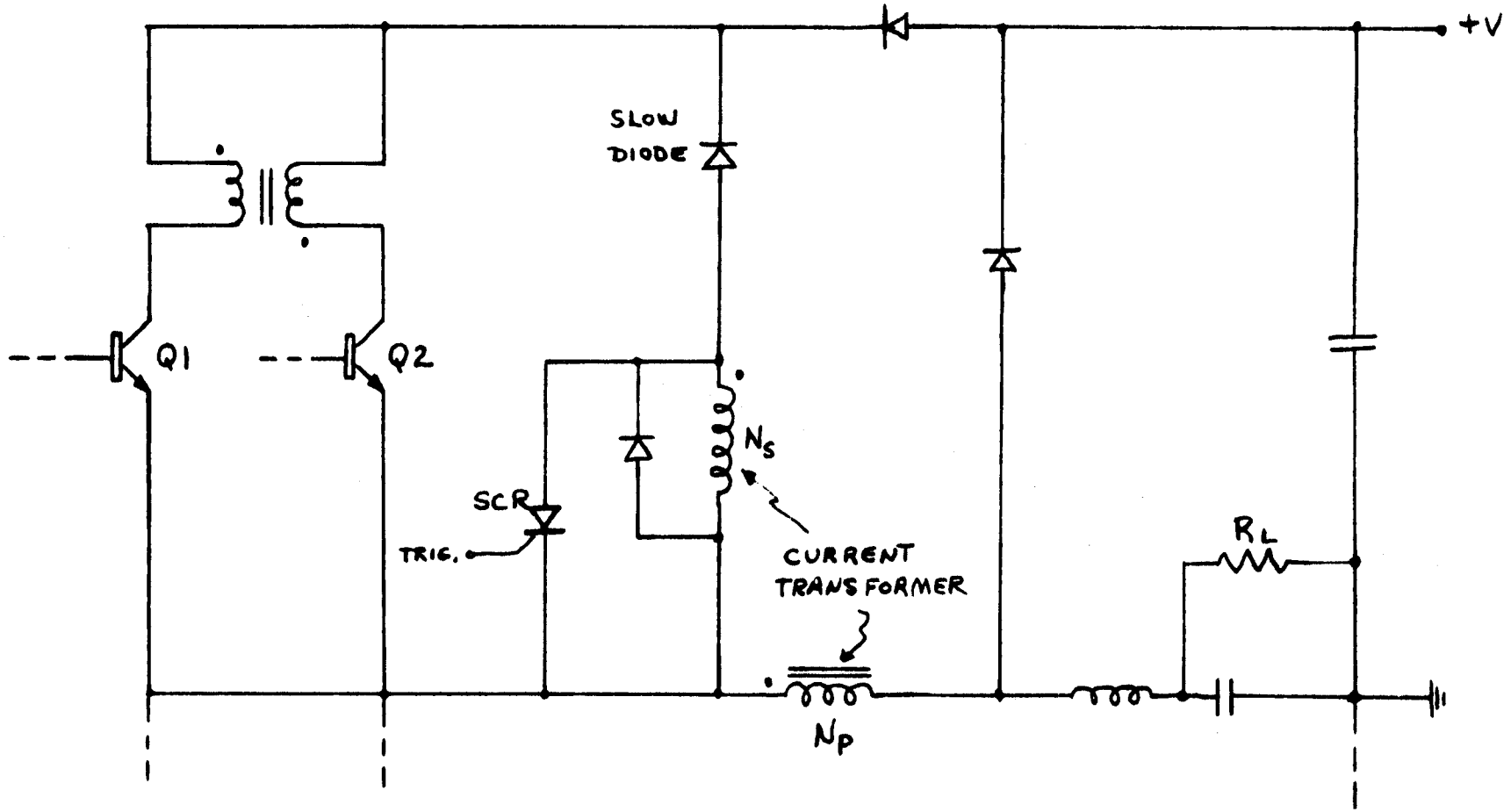


FIGURE 14

diode recovery time was about four microseconds for all parts of the pulse width modulated waveform. The recovery time can be reduced by increasing the turns ratio of the current transformer thus reducing the priming current. However, the slowest power transistor will turn off into a larger voltage, increasing its switching losses. The overall useful load capacity for each half phase will be reduced by the amount of priming current required for the slow diodes. Therefore, diodes with large reverse to forward current gains should be selected. This clamping circuit will be given further consideration in the final breadboard design as a possible means of eliminating the turn-off current unbalance in the power transistors.

D. SELECTED CONFIGURATION

1. Power Transistors

As indicated previously, production of the Delco 2N2583 transistor has been discontinued. Just prior to this, several meetings were held with representatives from Delco to discuss the use of these transistors in the PWM power stage. After presenting our circuit application in detail and discussing the problems that were encountered, they concluded that the 2N2583 transistors would be operating in excess of their power ratings at full collector voltages of 400 volts during their turn-off switching times. They indicated that the maximum power dissipation curve of 150 watts shown in the output characterstics graph illustrated in the engineering data sheet for the 2N2583 transistor was in error and that the power dissipation capacity was much lower at these voltage levels. The maximum power dissipation for the collector voltage level of 400 volts should not exceed 30 watts. The reduction in the maximum power dissipation capacity at the higher operating voltage is caused by the increase in the thermal resistance of the transistor junction which results from an apparent reduction in the usable wafer thickness. This apparent reduction in the wafer thickness is caused by the large electric fields established by these collector voltages.

The sustaining voltage of 325 volts for this 2N2583 power transistor presented another application problem in the PWM power stage. This is the maximum voltage that can appear across the power transistor when it is switching off collector current and still remain in the positive resistance region. For voltages less than the sustaining voltage, the power transistor will turn off any type of load current when a reverse base current is applied. However, for supply voltages that are greater than the sustaining voltage, this load current will decrease and pass through a negative resistance region where it will remain at a given level determined by the power transistor characteristics. A high dissipation will occur in the

transistor junction at this current level. The transistor will remain at this point of high dissipation as the reverse base current is increased. However, the emitter current will be further concentrated by the increase in the reverse base current, causing the heating to become more localized in this junction. If the collector current fails to "break away" from this level before a critical emitter current density is reached, a localized burnout of the transistor junction will occur. At the sustaining voltage of 325 volts, the collector current will "break away" and go to zero at a reverse base current which is less than that required to cause the transistor junction to fail. However, at the collector voltage of 400 volts that will be present in our power stage circuit, the probability of transistor failure caused by this local burnout will be increased considerably.

Previous indications were that the 2N2583 transistor could be selected for higher voltages and also for matched gains and switching times. However, due to manufacturing difficulties at Delco, this was not possible. The technical representatives from Delco strongly recommended that serious considerations be given to their DTS-0710 transistor, which is similar to the 2N2583 except that its collector current rating is five amperes and it is packaged in a TO-3 case rather than a TO-36 case. The DTS-0710 transistor offers the following advantages:

a) It is produced in sufficiently large quantities to allow selection for higher sustaining voltage, higher collector breakdown voltage and matched gain and switching times.

b) It is presently being used and qualified on at least two military projects.

c) Its switching speed is slightly faster than the 2N2583.

Several engineering samples of the DTS-0710 power transistors selected for a sustaining voltage of greater than 400 volts were obtained and evaluated in the PWM power stage. Successful operation was achieved under conditions of full input voltage using two transistors in parallel in each half phase. Immediately after it was determined that these selected DTS-0710 transistors would be suitable for use in the PWM power stage, Delco announced that the 2N2583 was being discontinued, thus leaving the DTS-0710 as the only usable device for the power stage.

2. Circuit Description

The power stage circuit configuration that has been selected for the deliverable breadboard unit is basically the same as was presented in Figure 10. It uses a fixed delay operating in conjunction with a transistor in series with the power transistor base to provide a delayed turn-on which

eliminates the short circuit current problem A forced turn-off function is provided by a separate DC voltage and transistor switch and is effective in reducing the power transistor turn-off time to an acceptable level. Of course, for the complete 5KW inverter, 14 of the five ampere DTS-0710 power transistors must be paralleled for each half phase. However, only one drive circuit, such as Q1, Q2 and associated components as shown in Figure 10, is required for each half phase. Clamping circuits connected across points A-A' and B-B' will be used only if it is found that they are absolutely necessary to limit the peak powers occurring during the turn-off portion of each cycle.

3. Performance

A total of four Delco DTS-0710 power transistors were used in the power stage of the design verification breadboard. A slight adjustment of one of the sweepout resistors was made to balance up the turn-off times of the parallel units, thus preventing damage to the slowest transistor.

Preliminary load tests and efficiency measurements were made on this power stage for an effective modulation index of 0.8 and a carrier frequency of 7 KC. Table 4 shows the various load conditions and source voltages that were used. A maximum power level of 650 watts was obtained from this power stage for both source voltages set for 190 volts and a load resistance of 17.5 ohms. The power stage was operated at this load level for 40 minutes without any adverse effects being observed. The power transistor heat sinks were only slightly warm to the touch during this operating time. The source voltages were not increased above 190 volts each because the zener diode clipping circuits began to conduct current during too much of each cycle. At present the zener diode voltages were selected for 400 volts ±5% so at the low end this voltage is 380 volts or just about the limit of twice the source voltage setting of 190 volts. These zener diode voltages will be selected for higher voltage levels in the final breadboard design. Figures 22, 23 and 24 illustrate typical waveforms taken in this power stage breadboard circuit.

The preliminary efficiency measurements for this power stage at various source voltage levels are illustrated below.

TABLE 4. Efficiency Data For Power Stage Using Four (4) DTS-0710 Transistors

$V_{in}(+)$ Volts	$I_{in}(+)$ Amps	$V_{in}(-)$ Volts	$I_{in}(-)$ Amps	P_{in} (Total) Watts	P_{out} (Total) Watts	Eff. η
150	1.43	150	1.375	420	378	90.0%
180	1.68	180	1.63	595	534	89.9%
190	1.79	190	1.75	672	594	88.5%

These efficiency measurements were recorded for an effective modulation index of 0.8, a carrier frequency of 7 KC, and a load resistance of 20 ohms. The slight reduction in the power stage efficiency when the source voltages were increased to 190 volts is caused by the losses in the zener diodes which were conducting two ampere spikes that had a time duration between 1 to 1.5 microseconds. Two 400 cycle fan motors were used as a load both with the 20 ohm resistive load and then alone. Both motors started and ran at their normal speeds for both conditions. The combined motor load current for both motors was 1.5 amps while their starting current was about 3.0 amps. Larger single phase 400 cycle motors were not available at the time these tests were made.

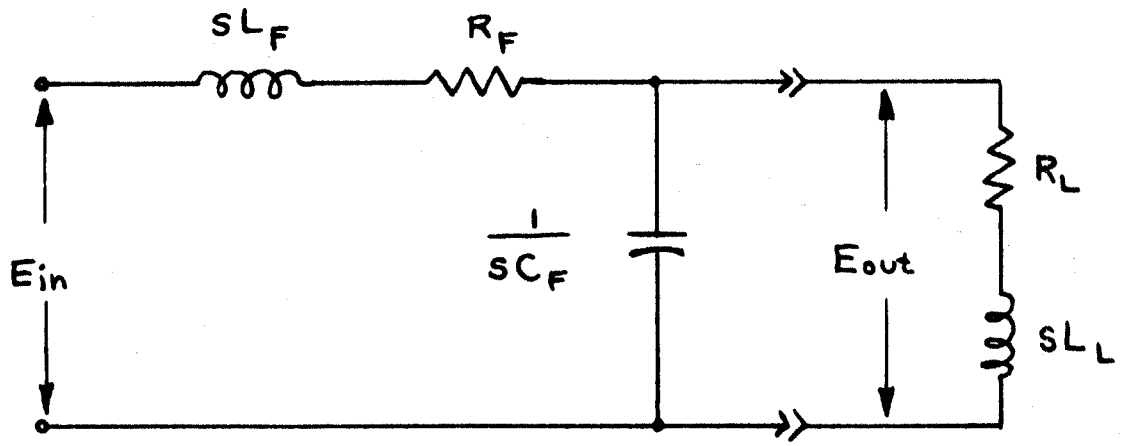
E. OUTPUT FILTER DESIGN

A low pass L-C filter is required at the output of each phase of the PWM inverter to suppress the carrier frequency component and its associated harmonics and sidebands while passing the 400 cycle power frequency component to the load. A typical low pass filter and its load impedance are illustrated in Figure 15. The filterparameters, inductor L_F and capacitor C_F, must be sized to reduce the total harmonic distortion to 5% maximum and the individual harmonics to 2% maximum for all load conditions.

The generalized input impedance and voltage transfer function for the steady state conditions were derived for this filter.

$$Z_{in} = \frac{S^3 L_F L_L + S^2\left[L_F R_L + R_F L_L\right] + S\left[\frac{L_F}{C_F} + R_F R_L + \frac{L_L}{C_F}\right] + \left[\frac{R_F}{C_F} + \frac{R_L}{C_F}\right]}{S^2 L_L + SR_L + \frac{1}{C_F}} \quad \text{Eq. 1}$$

AC LOW PASS POWER FILTER



L_F = Series Filter Inductance

R_F = Equivalent Inductor Resistance

C_F = Shunt Filter Capacitor

R_L = Equivalent Load Resistance

L_L = Equivalent Load Inductance

FIGURE 15

$$\frac{E_{out}}{E_{in}} = \frac{S + \frac{R_L}{L_L}}{S^3 C_F L_F + S^2\left[R_F C_F + \frac{R_L L_F C_F}{L_L}\right] + S\left[\frac{R_F R_L C_F}{L_L} + \frac{L_F}{L_L} + 1\right] + \left[\frac{R_F}{L_L} + \frac{R_L}{L_L}\right]} \quad \text{Eq. 2}$$

The filter resonance frequency and equivalent impedance for various load conditions were also determined so that the filter currents could be minimized.

$$\omega_R^4 + \omega_R^2\left[\frac{R_L^2}{L_L^2} - \frac{1}{L_F C_F} - \frac{2}{L_L C_F}\right] + \left[\frac{1}{L_L L_F C_F^2} + \frac{1}{L_L^2 C_F^2} - \frac{R_L^2}{L_L^2 L_F C_F}\right] = 0 \quad \text{Eq. 3}$$

$$Z_{in\,R} = \omega_R^4 R_F L_L^2 + \omega_R^2\left[R_F R_L^2 - \frac{2R_F L_L}{C_F}\right] + \frac{\left[\frac{R_F}{C_F^2} + \frac{R_L}{C_F^2}\right]}{\omega_R^4 L_L^2 + \omega_R^2\left[R_L^2 - \frac{2L_L}{C_F}\right] + \frac{1}{C_F^2}} \quad \text{Eq. 4}$$

Transient conditions were not investigated for this filter design since the PWM inverter will be "soft started" through its DC-DC converter power section.

The values for the filter inductor, L_F, and capacitor, C_F, were calculated for a single phase full load capacity of 1667 watts at a line to neutral load voltage of 115 V_{RMS} and a minimum power factor of 0.7, using the Equations 1 through 4. The PWM frequency spectrum for a 0.9 modulation index was used to determine the amount of attenuation that will be required by the filter and is shown in Figure 16. Examining this spectrum reveals that the carrier frequency is the predominate frequency that must be suppressed. Its output voltage is 56.7% of the 400 cycle voltage. Therefore, the filter design was based on suppressing this carrier frequency to 2% of the 400 cycle fundamental and to minimize the low pass filter current under all load conditions.

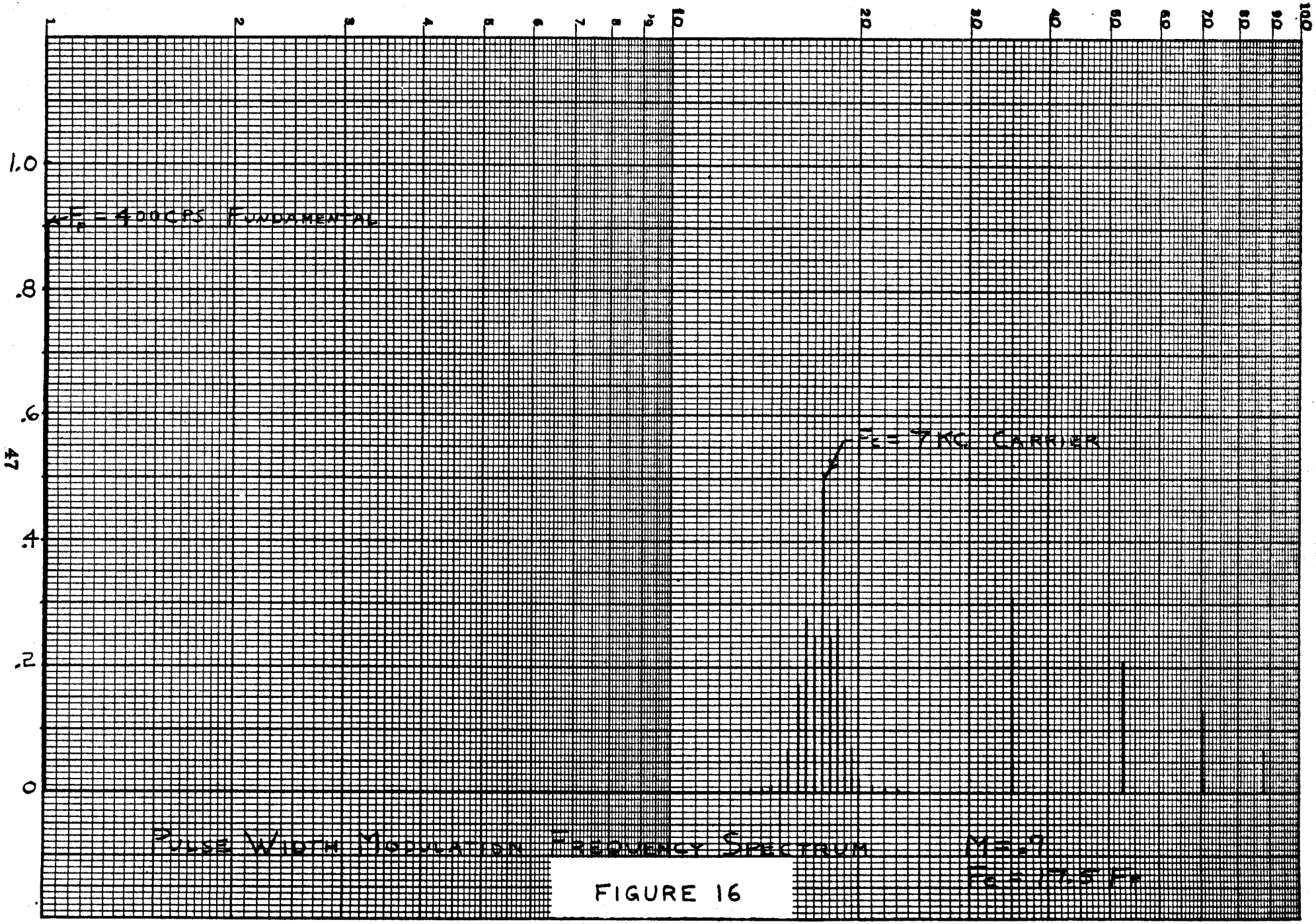

1
2
3
4
5
6
7
8
9
10
20
30
40
50
60
70
80
90
100
1.0
.8
.6
.4
.2
0
47
F_c = 400 CPS FUNDAMENTAL
F_c = 7 KC. CARRIER
PULSE WIDTH MODULATION FREQUENCY SPECTRUM
M = .9
F_c = 17.5 F_f

FIGURE 16

A filter inductor resistance, R_F, of 0.1 ohms maximum was assumed for these calculations. The resultant filter parameters were found to be L_F = 0.5 mh and C_F = 24 μfd. A flat spiral air core design was used for this filter inductor. Aluminum conductor strip 1/2" wide by 0.5" thick was used to minimize the filter inductor weight. Its finished weight was estimated to be three pounds and its finished diameter to be ten inches. The calculated winding resistance was found to be R_{DC}= 0.053 ohms. This resistance was about half the estimated value used in the calculations. However, some eddy current loss will occur in this winding at these high frequencies and will be reflected as an equivalent, R_{AC}, resistive component that will add to the winding resistance, R_{DC}, to increase the filter inductor resistance. The calculated inductor power loss was 23 watts for a full load current of 20.7 amps RMS at 0.7 power factor.

Metalized polycarbonate dielectric material was selected for the AC filter capacitor because of its low dissipation factor at high frequencies. The Sprague 260P series capacitors were selected. Six of the 4 μfd - 300V capacitors (260 P40593T7) were placed in parallel to obtain the required 24 μfd capacity. The estimated weight for these six capacitors was found to be 0.9 pounds.

The present filter parameters (L_F = 0.5 mh, C_F = 24 μfd) are only calculated values for a given maximum load condition and have yet to be tried in the final breadboard system. These parameters will change if the power capacity of the inverter is altered significantly.

V. DC - DC CONVERTER

Because the AC output voltage for this inverter is greater than the DC input voltage and because there are no power transformers in the power stage, it is necessary that a step-up DC-DC converter be incorporated in the unit. This converter was not breadboarded during the period covered by this report. However, the general circuit configuration and many of the design details were selected.

A. BASIC DESCRIPTION

The basic converter as presently designed consists of two push-pull or parallel inverter stages operating at a frequency of 1 KC. Each inverter stage provides half of the required output power. A magnetic-coupled oscillator generates the basic signal to drive the power inverter stages. One stage is driven directly from an amplified signal derived from the master oscillator, while the other inverter stage incorporates a magnetic amplifier in its pre-drive circuit. Signals applied to the control windings of the magnetic amplifier allow the output of the second power inverter stage to be phase shifted relative to the first inverter stage.

The transistors which must be used to handle the large currents in these power stages are relatively slow devices. Therefore transistor storage time will probably result in both transistors of a given inverter stage being on simultaneously for a short time during each cycle. In order to eliminate the high peak currents that would result, special feedback windings will be provided on the power transformers and connected in such a way that one transistor cannot turn on until its mate has turned off.

The output windings of the two power transformers are connected in series to obtain voltage addition. When both stages are operating in phase the output is a square wave. If one is phased back relative to the other, a quasi-square wave results. These voltage added outputs are applied to diode rectifier circuits and filters to provide a plus 200 volt DC output and a minus 200 volt DC output with respect to ground reference.

B. REGULATION

Voltage regulation of the inverter is accomplished by sensing the AC output voltage and adjusting the DC-DC converter output to maintain the AC voltage constant. Three small single phase transformers are used to sense the output voltage. The outputs of these transformers are rectified, filtered and fed to a control winding on the magnetic amplifier in the DC-DC converter. As the AC voltage starts to change from either

line or load conditions, the magnetic amplifier causes a change in the phase relationship between the two DC-DC converter power stages which results in the DC voltage being changed the proper amount to keep the overall inverter AC output essentially constant.

C. SOFT START

As discussed in the power stage section, large capacitors are required across the output of the DC-DC converter to handle reactive currents. The value of these capacitors is considerably larger than what would be needed to just filter the quasi-square waves from the converter. Such large capacities cause a start-up problem when power is first applied to the unit because of the excessively high currents that would be drawn in charging them. To overcome this difficulty a soft-start circuit was included in the design of the converter. When power is first applied, a signal to a control winding of the magnetic amplifier starts the two converter power stages almost 180 degrees out of phase and then allows them to shift slowly to their normal operating region. This results in a slow voltage build up and therefore limits the capacitor charging currents.

VI. SWITCHING REGULATOR AND LOW POWER DC-DC CONVERTER

A. SWITCHING REGULATOR

The DC supply voltage to the PWM Static Inverter can vary from 44.8 to 61.6 volts. Because of this it is necessary to provide some regulation for the circuits that provide the base drive signals to the main DC-DC converter power stages and those circuits that provide drive signals to the PWM power stages. If regulation were not included for these circuits, conditions would exist where power transistors would either be grossly underdriven or overdriven, both of which are undesirable.

A regulator has been designed for this application which consists of a single Darlington power transistor connected as a series switching element operating at a frequency of 7 KC. It was necessary to make this a switching regulator to keep the efficiency as high as possible. The series switching element is driven from a saturating core transformer that is operated in a push-pull circuit supplied by the unregulated DC voltage. As the DC input voltage increases, the output pulse width from the saturating transformer decreases and reduces the average voltage at the output of the switching regulator. The operating frequency of the transformer remains constant since it is derived from the stable 7 KC sweep wave generator.

The output of the switching regulator is filtered by means of a simple L-C filter. A flyback diode is included to provide a current path during the time the switching element is off.

B. LOW POWER DC-DC CONVERTER

The selected PWM power stage configuration showed that two isolated DC voltages are required in the base drive circuit for each half phase. This means a total of 12 isolated DC supplies are needed to operate the power stages for the three phase inverter. The design for generating these isolated voltages incorporates two Darlington transistors operating in push-pull and driving the primaries of three step-down transformers. The voltage for operation of this converter is supplied from the output of the switching regulator and is approximately 36 volts DC. The drive signal is derived from a flip-flop which is triggered by the 7 KC sweep wave generator.

Each of the three transformers has four center-tapped output windings which are applied to full-wave rectifier circuits.

Two outputs from each transformer are approximately five volts and are used to provide turn-on drive power to the positive and negative halves of one phase of the PWM power stage. The other two windings from each transformer provide approximately seven volts for use in turning off one phase of the power stage.

VII. APPENDIX

A. SIZING OF REACTIVE CURRENT CAPACITORS

Reactive current capacitors will be required on the output side of the DC-DC converter to provide a current path for the reactive current developed by by the PWM power stage. Reactive current diodes will also be required to complete the electrical path. The sizing of the capacitors depends on the magnitude of the reactive current and the allowable voltage regulation, ΔV, that can be tolerated on the DC-DC converter output voltages. The following simplified analysis was made in an effort to determine these reactive current capacitor sizes.

The single phase full load case was considered as the worst case condition since all of the reactive current must be absorbed by these capacitors compared with the three phase case which will allow some of the reactive current to be passed through the power transistors of the various phases. The simplified PWM power stage is depicted in Figure 17. The following assumptions were made throughout this analysis.

a) Single phase load at 0.7 power factor.

b) All reactive current goes through D2 - C2 circuit path when Q1 turns off for the positive half of the current cycle.

c) All reactive current goes through D1 - C1 circuit path when Q2 turns off for the negative half of the current cycle.

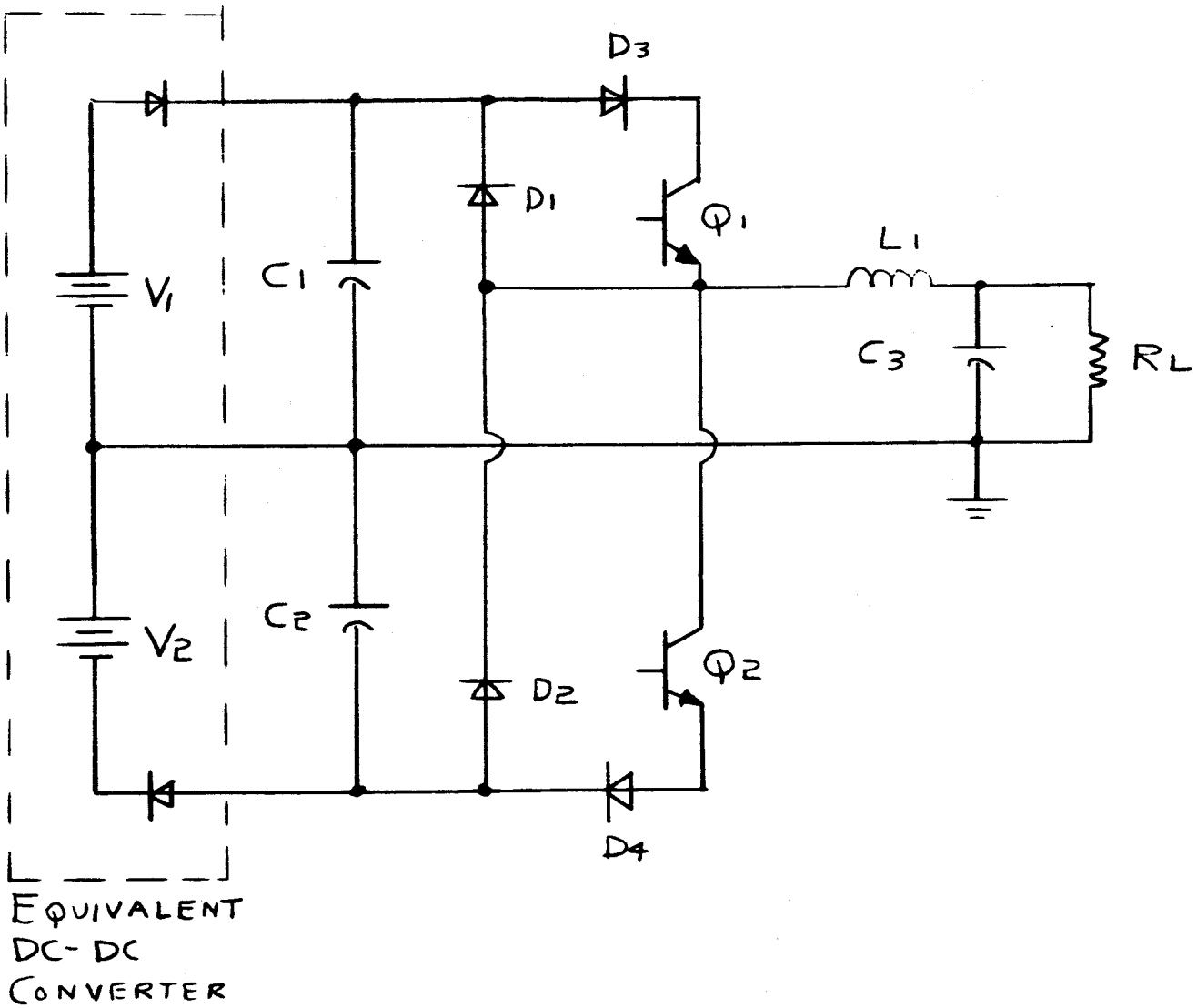
d) Capacitor C2 does not discharge until the positive current goes negative and Q2 starts to conduct.

e) Capacitor C1 does not discharge until the negative current goes positive and Q1 starts to conduct.

f) The resistance in series with reactive current capacitors C1 and C2 is assumed to be negligible.

g) The current pulses are assumed to comprise a sinusoidal pattern at the power frequency.

h) The ripple current from the DC - DC converter will be assumed negligible.



SIMPLIFIED PWM POWER STAGE

FIGURE 17

Using the above assumptions, the following analysis was made:

$$dv = \frac{dq}{c} \qquad \text{Eq. 1}$$

Where:

$$i = \frac{dq}{dt} \qquad \text{Eq. 2}$$

Therefore,

$$dv = \frac{idt}{c} \qquad \text{Eq. 3}$$

Equation 3 can be integrated in order to obtain a relationship between the current and voltage with respect to the capacitor size.

$$\int_{V_o}^{V_f} dv = \frac{1}{C} \int_{t_s}^{t_f} idt \qquad \text{Eq. 4}$$

Where:

V_f = final voltage on capacitor

V_o = initial voltage on capacitor

t_f = finish time of each pulse

t_s = start time of each pulse

Since the current, i, is a function of time, its pulse form expression must be obtained. Therefore, the current expression will be designated in the following form:

$$C = \frac{\sum_{m=1}^{m=k} \int_{t_s}^{t_f} idt}{\Delta V} \qquad \text{Eq. 5}$$

Where:

ΔV = the change in capacitor voltage

$= \left[V_f - V_o\right]$

$m = 1 \longrightarrow k$ are the number of current pulses

Since the current pulses are assumed to form a sinusoidal pattern, then the current, i, can be expressed as:

$$i = I_{max} \sin\omega t \qquad \text{Eq. 6}$$

Therefore:

$$\int_{t_s}^{t_f} i\,dt = \frac{I_{max}}{\omega} \times \left[\cos\omega t_s - \cos\omega t_f\right] \qquad \text{Eq. 7}$$

Where:

$$\omega = 2\pi\ Fp = \frac{2\pi}{Tp}$$

Tp = period of power frequency

Substituting Equation 7 into Equation 5 results in the final expression for the reactive current capacitor, C.

$$C = \frac{\frac{I_{max}}{\omega} \sum_{m=1}^{m=k} \left[\cos\omega t_s - \cos\omega t_f\right]}{\Delta V} \qquad \text{Eq. 8}$$

The pulse times were then summed up for the 400 cps power frequency and a 10 KC carrier assuming a 0.7 power factor load as the worst case. The following relationship was obtained:

$$C = \frac{0.183 \times 10^{-3} \times I_{max}}{\Delta V} \qquad \text{Eq. 9}$$

For Fp = 400cps

Fc = 10 KC

Power Factor = 0.7

$\Delta V = \left[V_f - V_o\right]$ for 1/2 cycle

I max = peak load current.

M = 0.9 modulation index

The following examples will be used to illustrate the use of Equation 9.

Example 1. The maximum single phase load that will be seen by this PWM inverter is:

$$\text{VA/single phase} = \frac{5\text{KW}}{.7(3)} = 2.38 \text{ KVA}$$

Its output voltage is Vrms = 115V; therefore Irms = 20.7 amps and I max = 29.3 amps peak.

A table of capacitor size, C, verses allowable ΔV may now be constructed for this peak current as follows:

ΔV	C μf	I max Amps	V_o Volts	V_f Volts
1	5360	29.3	200	201
2	2680	29.3	200	202
5	1072	29.3	200	205
10	536	29.3	200	210
20	268	29.3	200	220

The above results are theoretical in nature and assume ideal components with AC filter input currents being 100% of the full load currents. The next example will be used to compare actual measured results with the results obtained using Equation 9.

Example 2. In this example a model of the circuit depicted in Figure 17 was constructed and tested. A unity power factor load of 20 ohms was used which is a departure from the criteria of using a 0.7 pf load. Reactive current capacitors C1 and C2 were made 255μf each. Both the reactive current and voltage regulation were measured across each capacitor with the following results:

I max = 6.2 Amps peak

ΔV = 3.6 volts

Both these values were substituted into Equation 9 in order to obtain the theoretical value of C. It was found to be:

$$C_{\text{theoretical}} = 320 \ \mu f$$

This value of capacity was 65 μf larger than the actual value of capacity used, which was 255 μf, producing an error of about 20%. This error can be attributed to the following:

a) A unity power factor load instead of a 0.7 power factor load was used.

b) A modulation index of 0.72 was used instead of 0.90.

c) The rise and fall times on the current pulses were assumed to have infinite slope in the theoretical case. However, in the actual case the current pulses resembled a sawtooth waveform thus containing less ampere - seconds compared with their theoretical counterparts.

Despite these errors, Equation 9 may be used to obtain an approximate size for the reactive current capacitors for a given ΔV and I max. The actual values of these reactive current capacitors can then be obtained byexperiment for the same voltage regulation, ΔV.

B. OSCILLOSCOPE WAVEFORMS

Waveforms taken on the preliminary Design Verification Breadboard are presented in Figures 18 through 27. Figures 18 through 21 show waveforms of some of the key logic and low level signals. Figures 22, 23 and 24 show current waveforms taken while the inverter was providing 650 watts to a resistive load.

Figure 25 shows a short duration current pulse ahead of the normal filter current ramp. This added pulse appears when the turn-on delay is too short. Figure 26 shows a slight increase in the collector current just prior to turn-off. This is the unbalanced current which occurs when the other parallel transistor turns off first. The unbalance is very slight in the waveform of Figure 26.

Figure 27 shows the typical turn-off voltage and current waveforms for the unmodulated case.

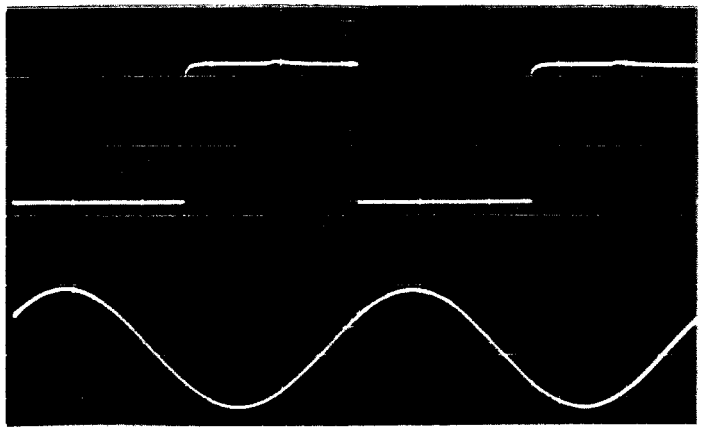


Figure 18. 400 cps Reference Square Wave and Sine Wave

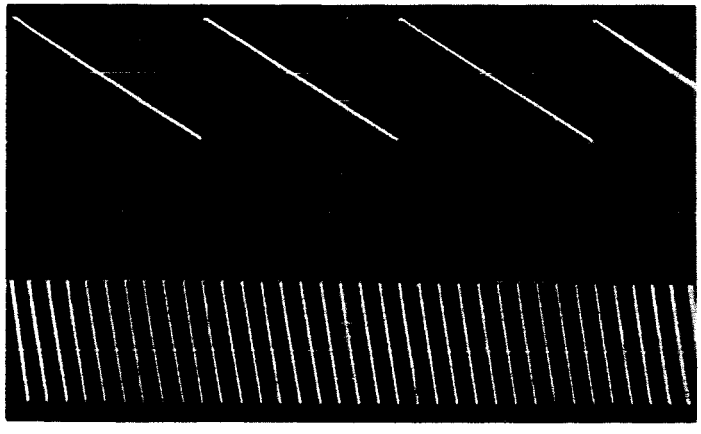


Figure 19. 7KC Sweep Wave Generator Output. Top Trace Expanded

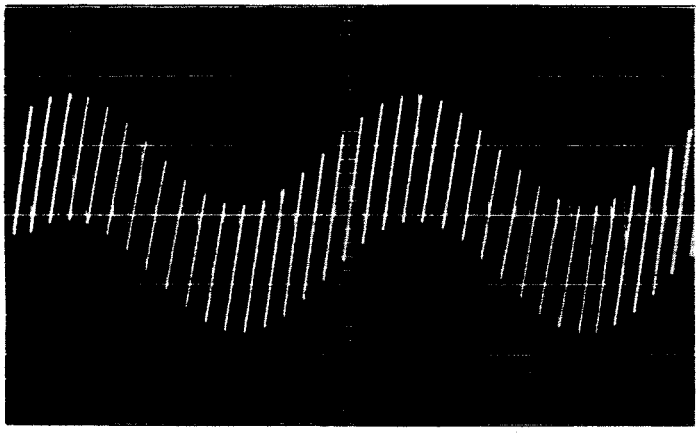


Figure 20. Summing Network Output

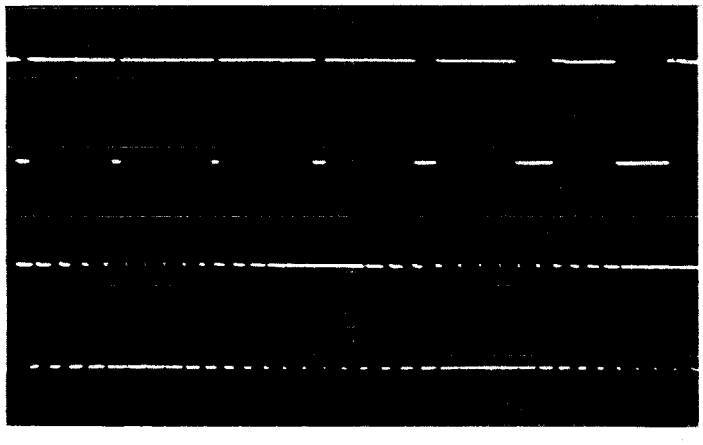


Figure 21. Slicer Amplifier Output. Top Trace Expanded

Figure 22. DTS-0710 Modulated Collector Current.
Vert. = 2 amp/cm
Hor. (Top) = 1 ms/cm
Hor. (Bot.) = 0.2 ms/cm

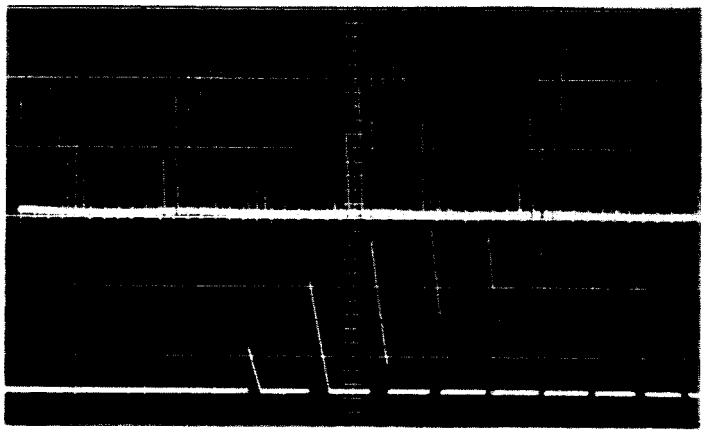


Figure 23. Reactive Diode Current
Vert. = 4 amp/cm
Hor. (Top) = 1 ms/cm
Hor. (Bot.) = 0.2 ms/cm

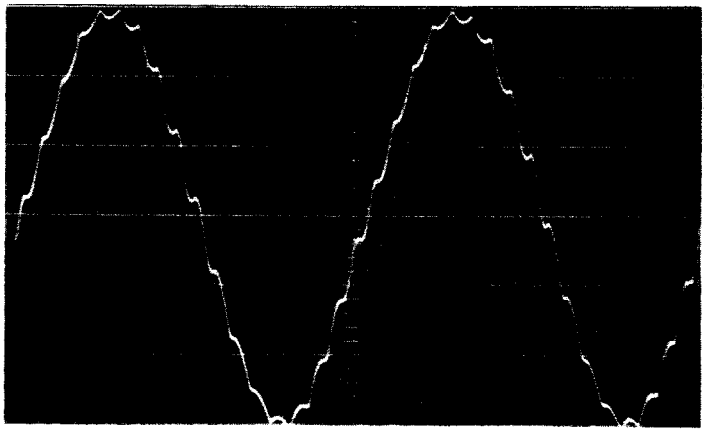


Figure 24. Filtered 400 cps Output Current for Resistive Load. 16 Amps peak-to-peak.

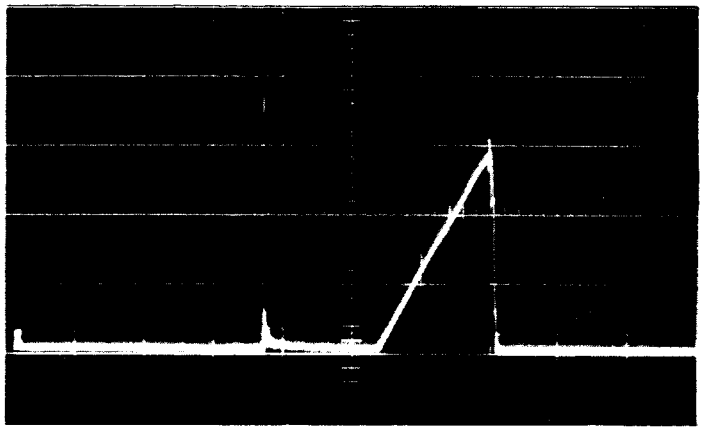


Figure 25. Short Circuit Current Spike Due to Improper Turn-on Delay

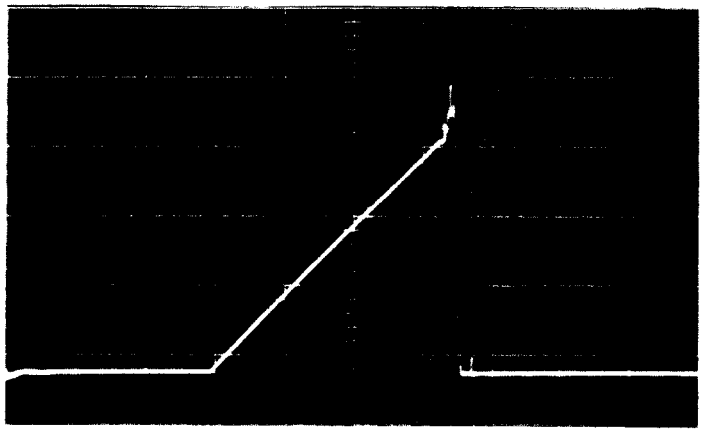


Figure 26. Unmodulated Collector Current Showing Small Additional Peak Due to Unbalanced Turn-off Times

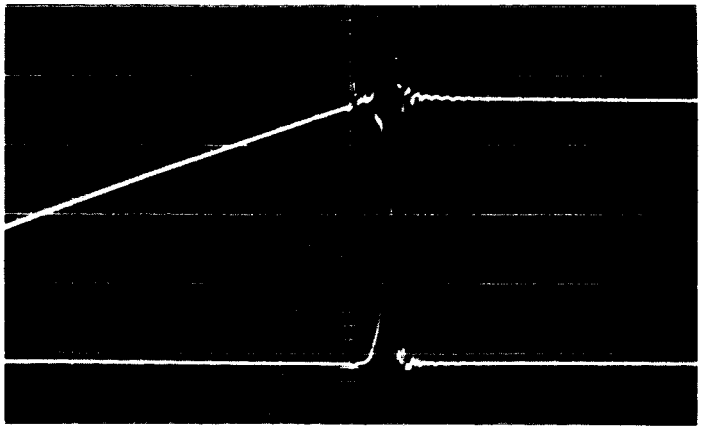


Figure 27. Power Transistor Turn-off Switching Pattern. Ramp is Collector Current. Other Waveform is Collector Voltage. (Unmodulated)