X-614-66-37

NASA TM X- 55454

PULSE TRAIN GENERATOR FOR ROCKET CAMERA

BY

ROBERT S. LEE

JANUARY 1966

NASA — GODDARD SPACE FLIGHT CENTER

GREENBELT, MARYLAND

PULSE TRAIN GENERATOR FOR ROCKET CAMERA

By

Robert S. Lee
Goddard Space Flight Center
Greenbelt, Maryland

INTRODUCTION

This paper describes a solid-state pulse-train generator to control shutter and film-advance timing of camera experiments on sounding rockets. Circuit simplicity, flexibility, accuracy and low power-consumption were the major design objectives. The final circuit configuration produces a time-sequential train of four shutter timing pulses of different widths, with a fixed interval following each shutter timing pulse to allow time for advancing the film. The timing cycle commences when power is applied to the circuit, and recycles continuously until power is commanded "OFF".

The output of the pulse-train generator was used to activate a solenoid, which in turn operated the camera shutter. The shutter timing was 1/20, 1/10, 1/3 and 1 second, with a fixed 0.6-second spacing following each shutter timing pulse for film advance.

The circuit described was successfully flown on NASA Aerobee 4.53 on October 26, 1965, and Aerobee 4.145 on December 2, 1965, both from White Sands Missile Range, New Mexico. The circuit flown is shown mounted on the electronic compartment of the rocket in its unpotted form (Fig. 4).

BLOCK DIAGRAM DESCRIPTION

As shown in the block diagram (Fig. 1), the circuit consists of a unijunction clock driving a 7-stage flip-flop counter. NAND gates are connected to this counter to obtain voltage transition at the desired time to "set" and "Reset" an output flip-flop. This flip-flop circuit generates the time-sequential pulse train to control the shutter solenoid.

Since the smallest timing interval is 1/20 second, a clock rate of 20 cps was selected to minimize the number of flip-flop stages necessary in the counter. Once the basic clock rate is chosen, the widths of the output pulses that may be derived must be in multiples of the clock period.

The NPN transistor of the first NAND gate (Fig. 3, schematic diagram) is turned "ON" by the first clock pulse after counter reset (Fig. 2) and is turned "OFF" by the second clock pulse. This NAND gate output is differentiated and amplified, using the leading edge and trailing edge to "Set" and "Reset" the output flip-flop respectively. This results in a 50 millisecond output pulse. The output flip-flop remains in the "Reset" state until the second NAND gate is turned "ON" by the 14th clock pulse, allowing a 0.6-second spacing between the first and second output pulse. The leading edge of the second NAND gate is used to "Set" the output flip-flop, and the leading edge of the third NAND gate - 16th clock pulse, is used to "Reset" the output flip-flop, resulting in a 100 millisecond output pulse.

NAND gates 4 through 7 are connected as shown in Figure 2 to obtain output pulses of 300 and 1,000 milliseconds, with 600 millisecond spacing between each pulse. The four "Set" pulses are OR'ed together, as are the four "Reset" pulses, to gate the output flip-flop.

Since the 7-stage slip-flop counter will not run out until the 128th clock pulse, NAND gate number 8 was used to reset the counter on clock pulse No. 77, and the pulse train generator will recycle at this time. The recycling will continue until power is removed from the timer.

Complementary flip-flops were used to conserve power (Fig. 3). Should space and weight have a higher priority than power consumption, then micro-logic chips could be used for not only the flip-flops, but the NAND gates as well.

The complete circuit diagram is shown in Figure 3. No detailed circuit description will be made since all circuits used are standard logic circuits.

MECHANICAL SPECIFICATIONS

The circuit was packaged on three single sided printed circuit boards 4.25 inches long and 2.65 inches wide. The three boards stacked and potted has a height of 2.25 inches. It must be stated that due to time limitation no attempt was made to miniaturize the final package. It is conservatively estimated that thirty percent space saving could have been obtained had time allowed.

The fourteen outputs from the 7-stage flip-flop counters

are located on one edge of the top board, and the wiring to the diodes input of each NAND gate are color-coded to facilitate timing changes should it be necessary.

"Eccofoam" potting was used because the unit is mounted in a pressurized compartment in the rocket where outgassing is not a problem. The unit in potted form survivded 10G sine and random shake on all three axes.

ELECTRICAL SPECIFICATIONS

The timer has two internal power supplies to convert +28 V rocket battery to +15 V and +5 V. These power supplies are pulse-rate-modulated for good efficiency and regulation. The total power required is +28 V @6ma. The flight unit will tolerate an input voltage change of from +25 to +35 V and a temperature change of -20°C to +60°C. The timing accuracy of the output wave form is ±1% with the above temperature and battery voltage change. The internal power supplies give this circuit a high degree of noise immunization, transients of up to 10 V on the battery line will not affect the operation of the circuit.

CONCLUSIONS

The two rocket flights have demonstrated the reliability and adaptability of this circuit to rocket work. All of the major design objectives were achieved. The flexibility of this circuit makes it possible to obtain any reasonable pulse width and the simplicity of the circuit makes duplication easy. With the addition of two more flip-flops in the counter string, six output

pulses of 1/20, 1/10, 1/3, 1, 3 and 10 seconds with one-second spacing between each pulse may be obtained.

For experiments where continuous recycling is not necessary, the "Reset" NAND gate could be used to activate a clamp to clamp the clock, or binary logic may be added to obtain any number of cycles desired.

ACKNOWLEDGEMENT

I would like to thank Mr. Gary Harris of the Solar Physics Branch who did most of the breadboard and development work, packaging and trouble shooting. Also, Mr. Albert Eschinger of Aero Geo Astro Corporation for the design of printed circuit boards in a very limited time.

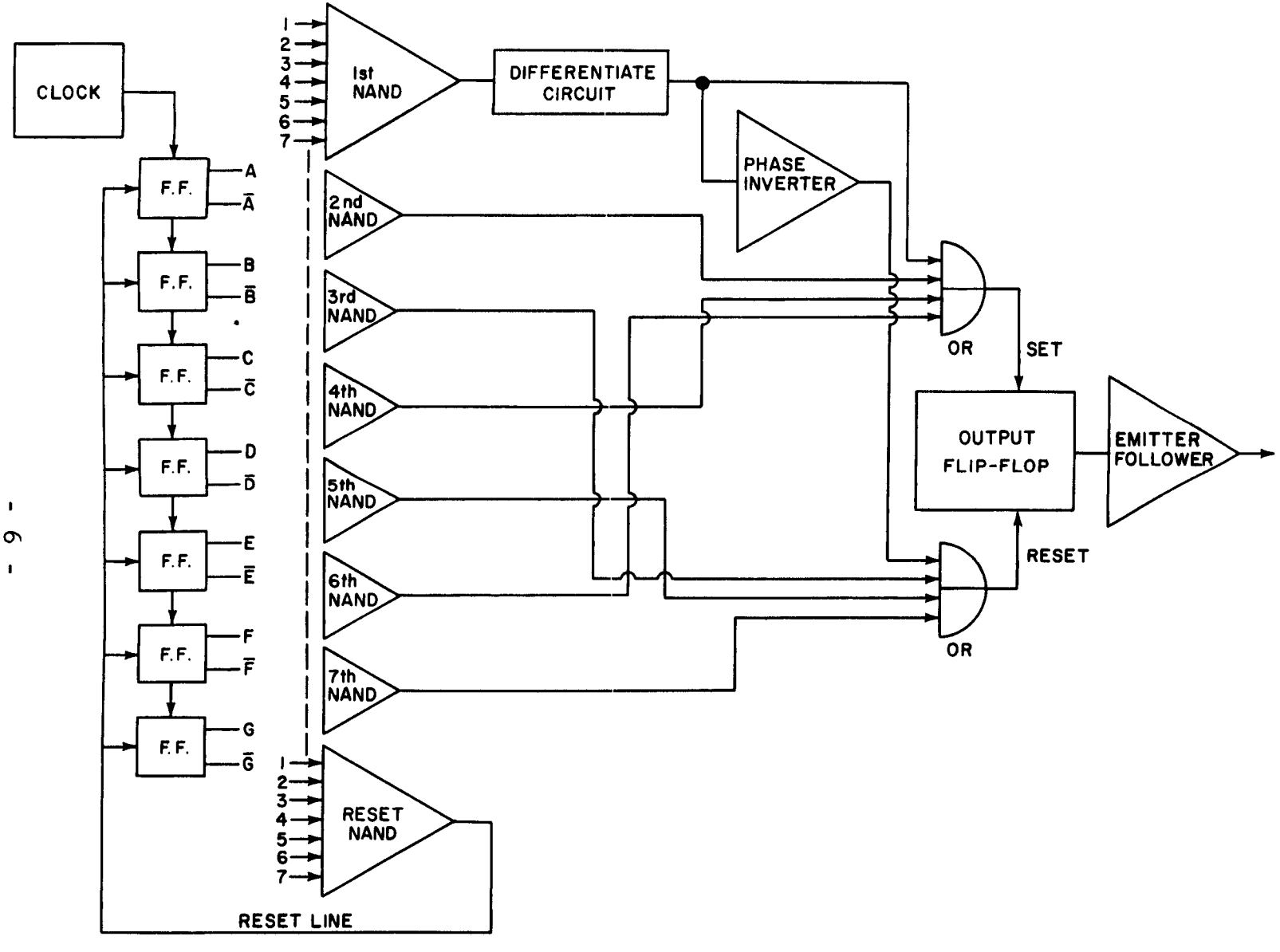

Figure 1. Block Diagram

	1st NAND	2nd NAND	3rd NAND	4th NAND	5th NAND	6th NAND	7th NAND	RESET NAND
F.F. 1	1	0	0	0	0	0	1	1
F.F. 2	0	1	0	0	1	1	0	0
F.F. 3	0	1	0	1	0	1	0	1
F.F. 4	0	1	0	1	0	1	0	1
F.F. 5	0	0	1	1	0	0	0	0
F.F. 6	0	0	0	0	1	1	0	0
F.F. 7	0	0	0	0	0	0	1	1
CLOCK PULSE	#1	#14	#16	#28	#34	#46	#65	#77

Figure 2. NAND Logic Truth Table

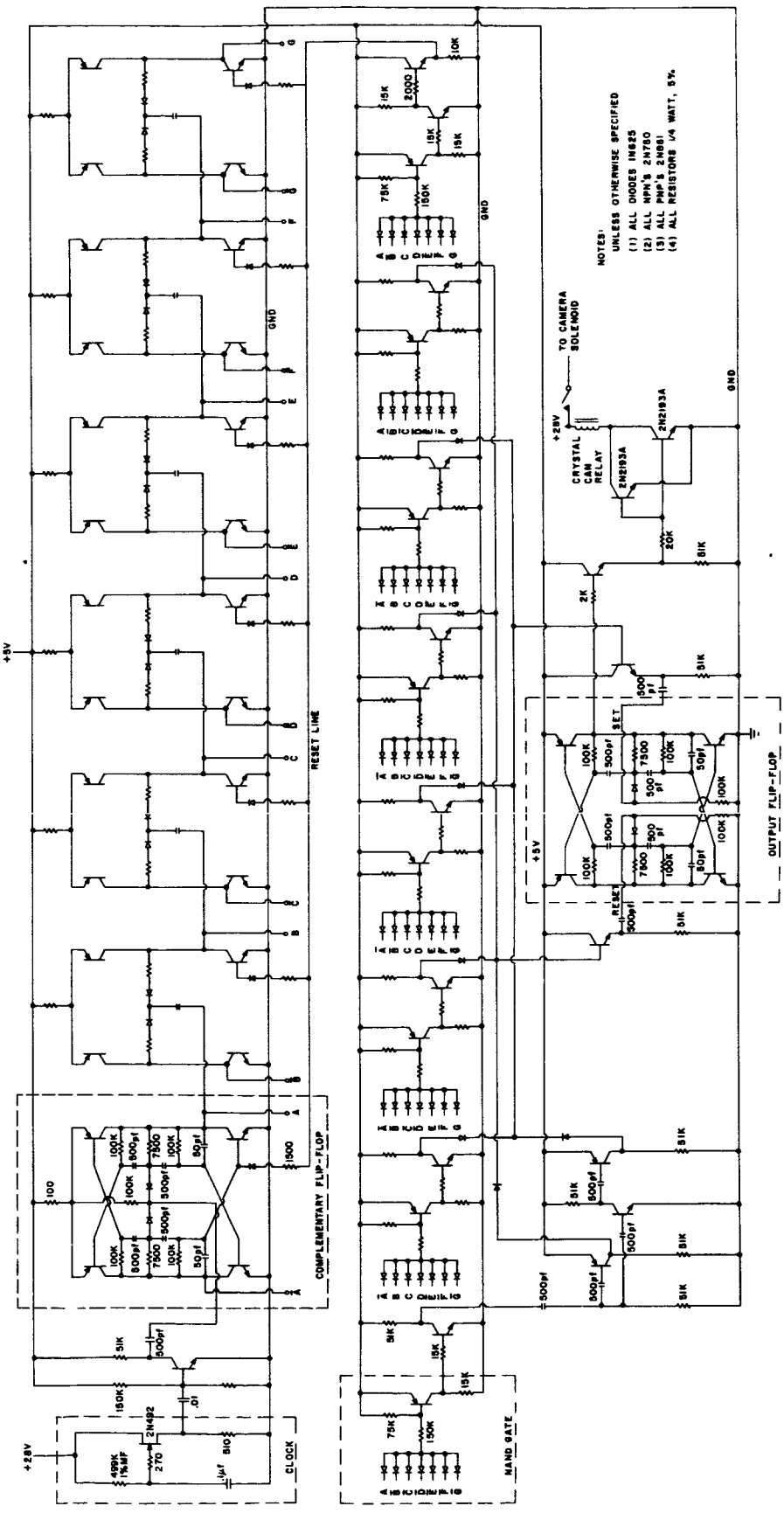

Figure 3. Schematic Diagram

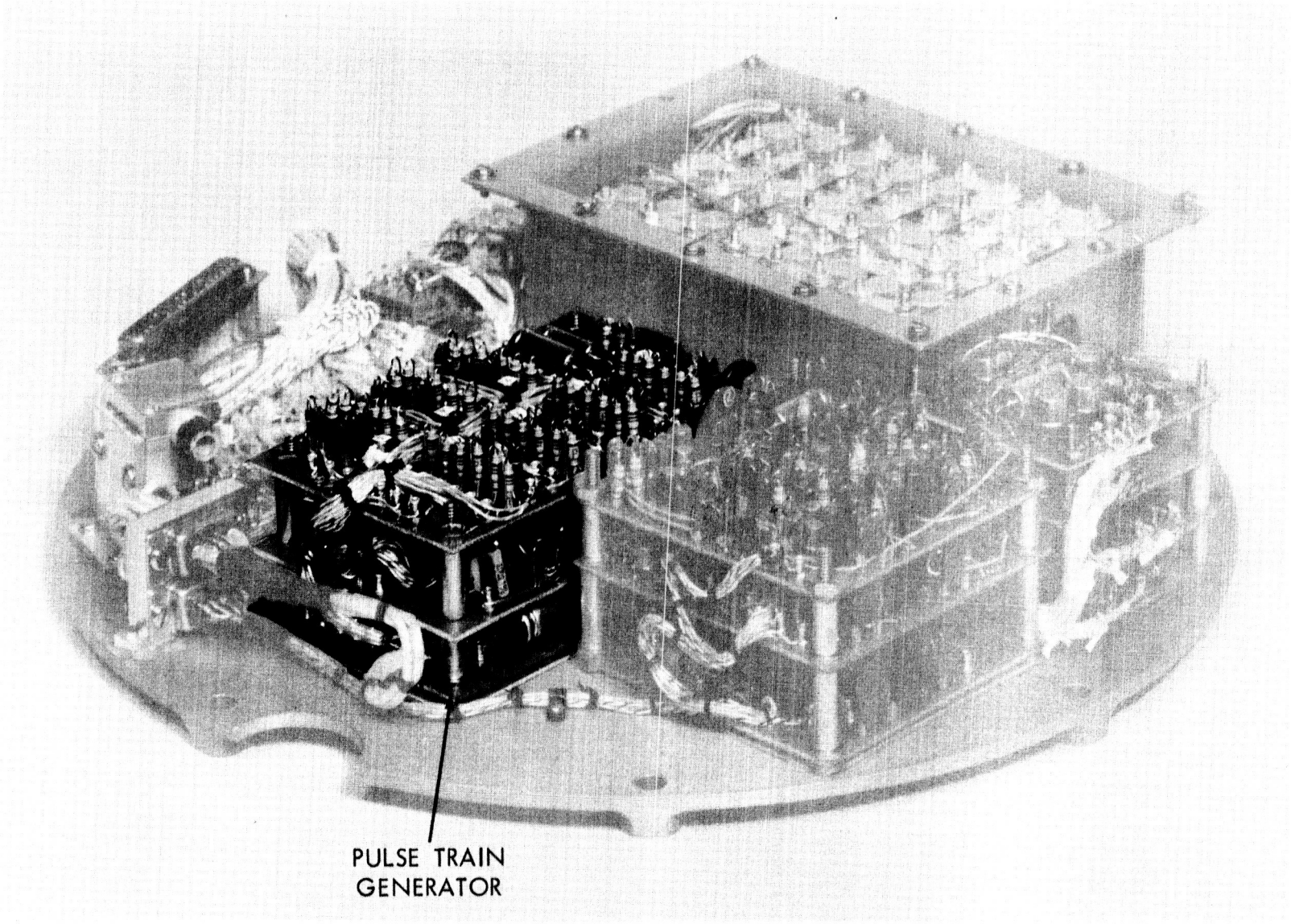

Figure 4. Unpotted Unit Mounted On Electronics Compartment Base Plate