

FINAL PROJECT REPORT PHASE 1

NONDISSIPATIVE DC to DC REGULATOR-CONVERTER STUDY

15 JUNE 1964 TO 31 DECEMBER 1965

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GODDARD SPACE FLIGHT CENTER
Greenbelt, Maryland

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GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND

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1.0 ABSTRACT

This report covers the work effort from 15 June 1964 through 31 December 1965. Effort during this phase included:

1. Initial search and analysis
2. Development of a chopper-regulator
3. Development of a booster-regulator
4. Breadboard testing and evaluation

The principle results of this period are:

1. The selection of a self-stabilizing chopper power supply was made for the low voltage (V_{OUT} less than $V_{IN MIN}$) output series of power supplies. The control technique adopted was a variable frequency, variable on time switching schemes where the "on" time was a function of input voltage.
2. The selection of a line compensated flyback booster was made for the high voltage output (V_{OUT} greater than $V_{IN MAX}$) series of power supplies. The control technique adopted was a variable "on" time, fixed frequency switching scheme where the "on" time was a function of both input voltage and load.
3. The nominal switching selected for both the chopper and booster series of power supplies was 30KC. This frequency appeared to be consistent with the minimum size and weight and maximum efficiency requirements.
4. Breadboard testing and evaluation was done with 8 breadboards. The breadboard power levels were 10, 25, 50 and 100 watts. Breadboard testing included voltage regulation, efficiency, ripple voltage output, and ripple current feedback.

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2.0 PURPOSE

The purpose of this program is to provide concepts, techniques, and developed modular circuitry for non-dissipative DC to DC converters in the power range of up to 100 watts.

Major program goals are the maximization of efficiency, simplicity, and reliability, along with the minimization of size, weight, and response times of the converters.

The circuits are to be modular in concept, so that a minimum of development is required to tailor a circuit to a specific application requirement. The concept should also allow, inasmuch as practical, for the use of state-of-the-art manufacturing techniques.

The program is multi-phased, including a study, analysis, and design phase, and a breadboard phase during which the concepts are to be verified by construction and test of eight breadboards.

3.0 INTRODUCTION

This report covers the work effort done on this program from 15 June 1964, through 31 December 1965. This effort was principally concerned with the power stage circuitry for chopper and booster regulator-converter. The electrical characteristics of the 8 pre-regulator converters is shown in Table I.

An initial search and analysis phase was conducted. Included in this effort was a literature search, an analysis of voltage control techniques, a study of efficiency versus switching frequency and a component materials review.

Development effort was first initiated on the chopper series of regulator converters. The self-stabilizing chopper was selected as the basic power stage. Several problem areas with the self-stabilizing scheme were uncovered early in the breadboard development phase which required extensive investigations. The problems were associated with circuit starting, circuit recovery time, and balanced operation. Solutions to each of these problems were determined. A nominal switching frequency was selected based on frequency-efficiency testing and a preliminary size and weight analysis of the 10 watt chopper.

Initial development effort on the chopper circuit was done at the 10 watt level. Scaling designs for the 25, 50 and 100 watt power levels were based on the results of the 10 watt development program.

Development effort on the booster series of regulator-converter was initiated near the completion of development effort on the chopper power supplies. The results of the frequency-efficiency testing were utilized in the selection of the nominal switching frequency for the booster. A "flyback booster" using a line compensated pulse width modulator was selected for the basic power stage. Minor development problems occurred, such as selection of choke inductance for proper no load and full load operation, limiting the flyback transistor peak current and control circuit compensation. Solutions to these problems were determined.

Initial development effort on the booster circuit was done at the 10 watt level. Scaling designs for the 25, 50 and 100 watt power levels were based on the results of the 10 watt program.

Selected electrical performance tests were run on the four chopper breadboards and four booster breadboards. These breadboards were open-loop configurations and were manually controlled. Data analysis was performed on each of the 10 watt power supplies.

TABLE IELECTRICAL CHARACTERISTICS OF PRE-REGULATOR CONVERTERS

Reg-Conv. Configuration	Voltage		Power Watts	Vout Ripple		Iin Ripple, MA PK	Size Cu. In.	Weight Oz.
	Input, V	Output, V		MV	P-P			
A	10-20	22	10	20		15	15	10
B	10-20	9	10	20		25	15	10
C	10-20	22	25	40		30	20	12
D	10-20	9	25	40		50	20	12
E	12-20	22	50	60		60	25	14
F	12-20	11	50	60		100	25	14
G	22-33	35	100	75		120	30	16
H	22-33	21	100	80		200	30	16

ALL: Regulation: $\pm 1\%$ for Line and 75-100% or 100-75% Load

Recovery Time: 50 m sec. maximum (10 milliseconds objective)

Transient Excursion: $\pm 2\%$ maximum

Efficiency: 90% minimum with output powers above 25%

Temperature: -20 to +70°C

4.0 TECHNICAL DISCUSSION

4.1 INITIAL SEARCH AND ANALYSIS

4.1.1 Literature Search

The literature search has revealed only five basic, non-dissipative switching-type regulator-converters. They are:

- a) Chopper Regulator
- b) Capacitive Divider
- c) Bedford Step-up
- d) Capacitive Doubler
- e) Inverter-Rectifier

The first two are "buck" systems, the second two are "boost" systems, and the last may be either.

Of these five basic types, a number of variations exist. The most obvious variation is the push-pull connection. In general, the other variations differ only in drive circuitry and the means of controlling the output duty cycle. The only known exception to this statement is the use of the "positive clamp" which changes the inverter-rectifier to the booster and hence modifies the circuits function.

There are also many other variations which use a combination of basic circuits. An example is the use of a chopper regulator to supply an unregulated inverter-rectifier and in this manner maintain a regulated output voltage. In general, these variations are more complex and inherently less efficient than the basic types and so are not considered here.

All of the applicable transistorized, regulated, power state circuits discussed in the literature search may be classified according to the five basic types as follows:

TABLE II

CLASSIFICATION OF POWER STAGES INTO BASIC TYPES

<u>BASIC TYPE</u>	<u>SINGLE-ENDED</u>	<u>PUSH-PULL</u>
Chopper Regulator	Two-State Modulator Telstar Blocking Oscillator Low Frequency Pulse Generator Monostable Regulator Chopper Regulator	Self-Stabilizing Chopper
Capacitive Divider	Capacitive Divider	None
Capacitive Doubler	Capacitive Doubler	None
Bedford Step-Up	Bedford Step-Up	None
Inverter-Rectifier	Unsymmetrical Low Voltage Converter	Pulse-width Modulated Power Supply Improved Booster-Converter Sliding Square-Wave Converter One-Step Converter

Circuitry Selection Criteria

A group of factors to be used as criteria for selection of circuitry were jointly agreed upon by NASA and HSED engineering. The factors selected for evaluation were:

- 1) Degree of commonality of circuitry for "buck" or "boost"
 - 2) Number of magnetic components
 - 3) Number of components
 - 4) Efficiency
 - 5) Input ripple current
 - 6) Output ripple voltage
 - 7) Overload/short circuit protection
 - 8) Minimum size and weight
 - 9) Isolation of input/output grounds
1. Degree of commonality of circuitry for "buck" or "boost" application. This is a rather subjective item to evaluate, however, the following definitions will be used:

Commonality exists only if the same circuit arrangement can be used for either operation. The inverter-rectifier, for example, can be made to buck or boost merely by changing a transformer ratio. The chopper and the Bedford Step-Up have no commonality even though the components used in each may be identical, because they require a change of arrangement to go from one function to the other.

The weighting factor for this item is 5, and the rating may vary from zero to 5, where 5 is the minimum degree of commonality.

2. Number of magnetic components. The weighting factor is 3, and each magnetic component is rated as 2.5.
3. Number of components. Each component is rated at 0.5, and the weighting factor is 5.
4. Efficiency. This rating is based upon the maximum efficiencies which have been reported for the various approaches. Efficiency ratings are:
 - a) near 95%, 1
 - b) near 90%, 2
 - c) near 85%, 3
 - d) near 80%, 4
 - e) near 75%, 5

The weighting factor is 4.

5. Input ripple current. This is rated on the relative degree of filtering required to smooth the input. The maximum is 5, minimum 0. The weighting factor is 2.
6. Output ripple voltage. Circuits with LC filters are rated 2.5, and capacitive filters at 5. The weighting factor is 5.
7. Overload/short circuit protection. Ratings are:
 - a) circuits which do not have a series element capable of being "opened" so as to isolate the source from the load fault are rated at 5.
 - b) circuits which have elements capable of being "opened", but where current must be sensed on a DC basis (resistor sensing) are rated at 2.5.
 - c) circuits of category b) where sensing can be done on an AC basis (current transformer) are rated at 0.

The weighting factor is 5.

8. Minimum size and weight. Each magnetic component is rated at 1, and each resistor, capacitor, or semiconductor at 0.5. The weighting factor is 3.
9. Isolation of input-output grounds. Transformer-coupled circuits are rated at 0, and those without isolation at 5. The weighting factor is 2.

Two additional criteria, that of output voltage regulation and dynamic regulation recovery time, initially appeared in the above listed but have been deleted on the basis that these items are determined by the control circuitry rather than the basic power stage.

The selection criteria and weighting factors thus serve to penalize those circuits which have the highest valued summation of rating and weighting factor products.

Comparison of Power Stages

Figure 1 shows eight power stages, which represent the simplest configuration capable of performing the necessary functions.

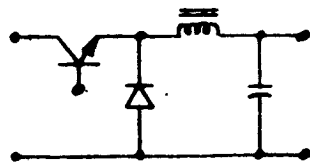
In comparing these circuits, the assumptions were made that the power stages were independent of drive and control circuitry, and that all circuits are operated at the same repetition rate. This means that the ripple components of the push-pull stages will be at twice the frequency of those of the single ended stages and consequently easier to filter.

Single-ended Chopper

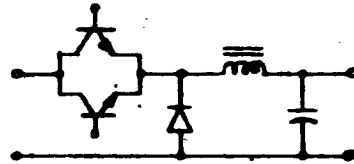
1. Commonality - none. Rating = 5
2. Magnetic components - one. Rating = 2.5
3. Components - four. Rating = 2
4. Efficiency - near 92%, but DC current sensing will reduce this to about 90%. Rating = 2
5. Input ripple current - high. Rating = 5
6. Output ripple voltage - LC filter. Rating = 2.5
7. Protection - series element with DC sensing. Rating = 2.5
8. Size and weight - one magnetic and three other components. Rating = 2.5
9. Isolation - none. Rating = 5

Push-pull Chopper

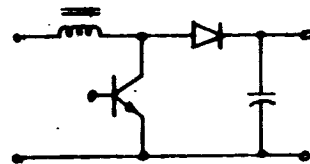
1. Commonality - none. Rating = 5
2. Magnetic components - one. Rating = 2.5
3. Components - five. Rating = 2.5
4. Efficiency - near 92%. Rating = 2
5. Input ripple current - twice the frequency of the single-ended unit. Rating = 2.5
6. Output ripple voltage - LC filter. Rating = 2.5
7. Protection - series element with AC sensing. Rating = 0
8. Size and weight - one magnetic and four other components. Rating = 3
9. Isolation - none. Rating = 5



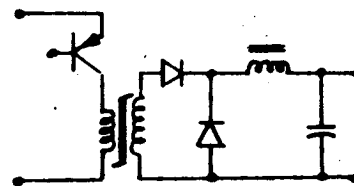
Single-Ended Chopper



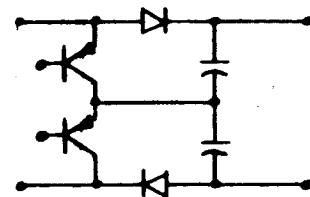
Push-Pull Chopper



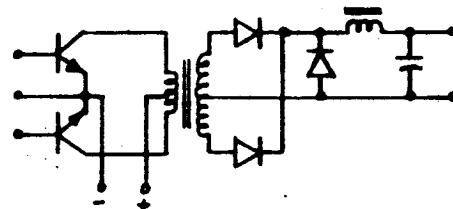
Bedford Step-Up



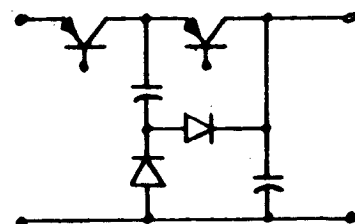
Single - Ended
Inverter - Rectifier



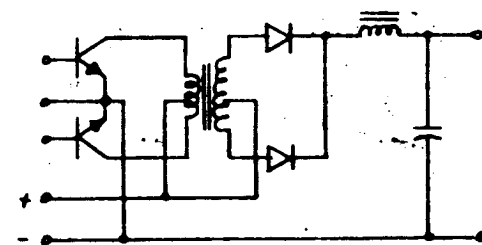
Capacitive Doubler



Push-Pull Inverter Rectifier.



Capacitive Divider



Push-Pull Booster

FIGURE 1

REPRESENTATIVE BASIC POWER STAGES

Bedford Step-up

1. Commonality - none. Rating = 5
2. Magnetic components - one. Rating = 2.5
3. Components - four. Rating = 2
4. Efficiency - 95%. Rating = 1
5. Input ripple current - high. Rating = 5
6. Output ripple voltage - capacitive filter. Rating = 5
7. Protection - circuit cannot be protected without additional series element. Rating = 5
8. Size and weight - one magnetic and three other components. Rating = 5
9. Isolation - none. Rating = 5

Single-ended Inverter-rectifier

1. Commonality - yes. Rating = 0
2. Magnetic components - two. Rating = 5
3. Components - two magnetic and four other components. Rating = 3
4. Efficiency - 90 to 85%, but DC current sensing will limit it to about 80%. Rating = 4
5. Input ripple current - high. Rating = 5
6. Output ripple voltage - LC filter. Rating = 2.5
7. Protection - series element with DC sensing. Rating = 2.5
8. Size and weight - two magnetics and four other components. Rating = 4
9. Isolation - yes. Rating = 0

Push-pull Inverter-rectifier

1. Commonality - yes. Rating = 0
2. Magnetic components - two. Rating = 5
3. Components - eight. Rating = 4
4. Efficiency - 85%. Rating = 3
5. Input ripple current - twice the frequency of that of single-ended unit. Rating = 2.5
6. Output ripple voltage - LC filter. Rating = 2.5
7. Protection - series element and AC sensing. - Rating = 0
8. Size and weight - two magnetic and six other components. Rating = 5
9. Isolation - yes. Rating = 0

Push-pull Booster

1. Commonality - deletion of the output potential clamp and change of transformer ratio will allow this unit to "buck". Rating = 2.5
2. Magnetic components - two. Rating = 5
3. Components - seven. Rating = 3.5
4. Efficiency - varies according to the degree of boost. Average about 90%. Rating = 2

5. Input ripple current - varies depending on the degree of boost, but is better than conventional push-pull because of continuous DC content. Rating = 1
6. Output ripple voltage - LC filter. Rating = 2.5
7. Protection - circuit cannot be protected without additional series element. Rating = 5
8. Size and weight - two magnetics and five other components. Rating = 4.5
9. Isolation - none. Rating = 5

Capacitive Doubler

1. Commonality - none. Rating = 5
2. Magnetic components - none. Rating = 0
3. Components - six. Rating = 3
4. Efficiency - near 90% unregulated, probably will decrease to 80-85% with regulation. Rating = 3
5. Input ripple current - high - Rating = 5
6. Output ripple voltage - capacitive filter. Rating = 5
7. Protection - series element with DC sensing. Rating = 2.5
8. Size and weight - six non-magnetic components, however, the capacitors are quite large and will be rated as if they were magnetic components. Rating = 4
9. Isolation - none. Rating = 5

Capacitive Divider

1. Commonality - none. Rating = 5
2. Magnetic components - none. Rating = 0
3. Components - six. Rating = 3
4. Efficiency - no experimental data available, however, it would appear to be about equal to that of the Capacitive Doubler. Rating = 5
5. Input ripple current - high. Rating = 5
6. Output ripple voltage - capacitive filter. Rating = 5
7. Protection - series element with DC sensing. Rating = 2.5
8. Size and weight - six non-magnetic components. However, excessive capacitance is required, so the capacitors will be rated as magnetics. Rating = 4
9. Isolation - none. Rating = 5

Figure 2 is a comparison chart which shows the selector criteria, the ratings, weighting factors, and sub-totals for each power stage. The bottom line is the summation for each circuit, which indicates that the relative capability of each circuit to meet the overall specification requirements and goals. On this basis, the circuits which were selected for further consideration are the push-pull chopper, and the single-ended and push-pull inverter-rectifiers.

CRITERION	SINGLE-ENDED CHOPPER		PUSH-PULL CHOPPER		BEDFORD STEP-UP		SINGLE-ENDED INVERTER-RECTIF.		PUSH-PULL INVERTER-RECTIF.		PUSH-PULL BOOSTER		CAPACITIVE DOUBLER		CAPACITIVE DIVIDER	
	RAT. 1	SUB- WE = TOTAL	RAT. 1	SUB- WE = TOTAL	RAT. 1	SUB- WE = TOTAL	RAT. 1	SUB- WE = TOTAL	RAT. 1	SUB- WE = TOTAL	RAT. 1	SUB- WE = TOTAL	RAT. 1	SUB- WE = TOTAL	RAT. 1	SUB- WE = TOTAL
COMMONALITY OF CIRCUITRY	5	5	5	5	5	5	0	5	0	5	0	5	5	5	5	5
NO. OF MAGNETICS	2.5	3	2.5	3	2.5	3	5	3	5	3	5	3	0	3	0	0
NO. OF COMPONENTS	2	5	2.5	5	2	5	3	5	4	5	3.5	5	3	5	3	5
EFFICIENCY	2	4	2	4	1	4	4	4	3	4	2	4	3	4	3	4
INPUT RIPPLE CURRENT	5	2	2.5	2	5	2	5	2	2.5	2	1	2	5	2	5	2
OUTPUT RIPPLE VOLTAGE	1.5	5	2.5	5	5	5	2.5	5	2.5	5	2.5	5	5	5	5	5
OVERLOAD/S.CRT. PROTECTION	2.5	5	0	5	5	5	2.5	5	0	5	5	5	2.5	5	2.5	5
SIZE & WEIGHT	2.5	3	3	3	2.5	3	4	3	5	3	4.5	3	3	3	4	3
ISOLATION	5	2	5	2	5	2	0	2	0	2	5	2	5	2	5	2
	103.0		97.5		144.0		99.0		78.5		116.0		121.5		121.5	

FIGURE 2. POWER STAGE COMPARISON CHART

4.1.2 Voltage Control Techniques

Sorensen 1) presents a very descriptive discussion of the various means of modulation, using switching techniques, in which he discusses the characteristics of pulse-width, pulse-ratio, and two types of pulse-frequency modulation.

Several important points can be taken from his discussion:

- a) Some controllers inherently have minimum ON or OFF times.
- b) In modulation systems in which the frequency varies, the output low-pass filter must be designed for the lowest frequency.
- c) If either the ON or OFF time approaches zero, the bandwidth of the controller must approach infinity.

The first point may be seen in, for example, the monostable multivibrator, which has a minimum recovery, or OFF, time. The second point, obviously, implies that the filter for a given regulator will be smallest for a pulse-width modulated system, since its frequency is fixed. The third point has several implications. First, the design of the controller is more severe. Second, since the gain bandwidth product of any physically realizable controller is limited, this means that the regulation of the device suffers because of decreasing gain, and the controller may tend to be unstable.

Assuming no transformer scaling, regulator B must produce 9 volts from a 10-20 volt source. Allowing for a 1 volt series drop, the duty ratio must vary from 100% down to about 45%. Likewise, regulator G must produce 35 volts from a 22-23 volt source, with a duty ratio varying from about 40% to 5%. If transformer scaling is used, the turns ratio may be adjusted for, say, a step-up of 1.15, which shifts the duty ratio of regulator B to a range of 87% to 39%, thus decreasing the severity of the bandwidth requirement.

Another means of bypassing points a) and c) above is through the use of two modulating functions simultaneously, as in either the Pulse Width Modulated Power Supply or the Self-Stabilizing Chopper. Here a constant volt-second transformer establishes the ON time and varies the duty ratio as a function of input voltage, while a separate bistable multivibrator, operating over a relatively narrow range of frequencies, furnishes the necessary OFF time to compensate for load changes. In the limiting case of near 100% duty cycle, the transformer is operating close to its normal 180° saturated switching mode, and the multivibrator is operating close to its design frequency.

- 1) "Linear Control using ON-OFF Controllers,"
A. Sorensen, Electro-Technology, V71, n4, April 1963.

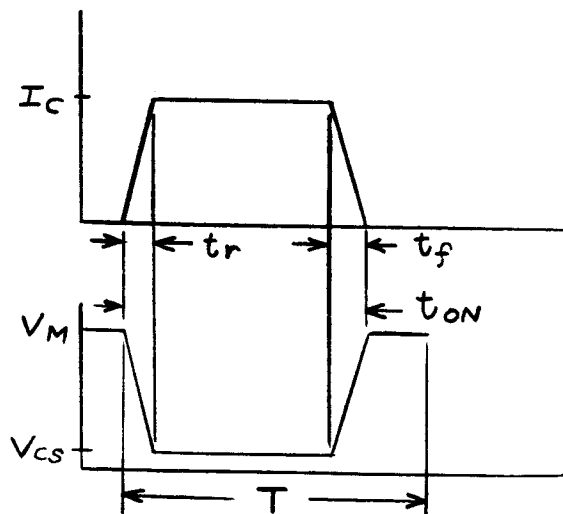
It should be noted, that since the low-pass output filters are LC with free-wheeling diodes, it is advantageous, from an efficiency viewpoint, to limit the OFF time as much as possible and hence decrease the amount of conduction time of the diode.

4.1.3 Efficiency versus Switching Frequency

Investigations were conducted into the loss of characteristics of semiconductors and transformers in an effort to determine the maximum switching frequency consistent with high efficiency and minimum size and weight.

Frequency Range Characteristics of Semiconductors

In order to determine the usable frequency range as a function of the semiconductor characteristics, a model was established, consisting of a single transistor switching through an ideal choke input filter into a resistive load with voltages, currents, and duty cycle equivalent to those of the 10 watt regulator, as follows:



V_M	V_{OUT}	P_{OUT}
20V	9V	10.1W
10V	9V	10.1W

Figure 3 Switching Model

In these calculations, delay and storage times were not considered. Transistor OFF losses were also ignored as being only a small percentage of total losses. Calculations were made at frequencies of 1, 10, 100, 250, and 500 KC with the following transistors:

TABLE III
2N2880 PARAMETERS

Cond. Time	$t_r + t_f$	I_B	I_C	V_{CS}	V_{BS}	Freq.
45.2%	.35 μs	.112	1.12	.12V	.9V	1KC
45.4%		.112	1.13			10KC
47.0%		.114	1.14			100KC
49.6%		.116	1.16			250KC
54.1%		.120	1.20			500KC
91.1%		.112	1.12			1KC
91.2%		.112	1.12			10KC
92.9%		.113	1.13			100KC
95.5%		.114	1.14			250KC
99.9%		.116	1.16			500KC

Detailed curves for the 2N2880 were available, so typical values were selected for the above parameters. Variation of β with frequency was not available, so it was held constant, somewhat arbitrarily, at all frequencies.

Table IV. 2N1908X (assumed) PARAMETERS

Cond. Time	tr+tf	I _B	I _C	V _{CS}	V _{BS}	Freq.
45.2%	1.8us	.112	1.12	.08V	.9V	1KC
46.0		.113	1.13			10KC
54.1		.120	1.20			100KC
67.6		.135	1.35			250KC
90.5		.112	1.12			1KC
91.4		.113	1.13			10KC
99.5		.116	1.16			100KC

Detailed curves were not available for the 2N1908, so (tr+tf), I_B, V_{CS}, and V_{BS} were established so as to illustrate the effect of low saturation voltage and medium switching speed as a contrast to the medium saturation voltage and high speed of the 2N2880.

Tables were prepared, using the formulas below:

$$\text{COND. TIME} = \frac{V_{OUT}}{V_M - V_{CS}} + \frac{tr + tf}{2T} \quad 1.)$$

$$I_C = P_{OUT} / (V_M - V_{CS}) \left(\frac{2t_{on} - 2t_r - 2t_f}{3T} \right) \quad 2.)$$

$$P_{SWITCHING} = \frac{I_C}{6T} (tr + tf) (V_M + 2V_{CS}) \quad 3.)$$

$$P_{ON} = \frac{I_C V_{CS}}{T} (t_{on} - t_r - t_f) \quad 4.)$$

$$P_{BASE} = \frac{I_B V_{BS}}{T} (t_{on} - t_r - t_f) \quad 5.)$$

$$P_D = P_{SWITCHING} + P_{ON} + P_{BASE} \quad 6.)$$

$$\eta = P_{OUT} / P_{OUT} + P_D \quad 7.)$$

Table V. 2N2880 DISSIPATION vs. ENERGY

Cond. Time	P _{sw}	P _{on}	P _B	P _D	η	Freq.	V _m
45.2%	.00132	.0609	.0457	.108	98.92	1KC	20
45.4%	.0133	.0612	.0459	.120	98.83	10KC	20
47.0%	.135	.0595	.0446	.239	97.68	100KC	20
49.6%	.342	.0571	.0428	.442	95.83	250KC	20
54.1%	.708	.0526	.0394	.800	92.66	500KC	20
91.1%	.000669	.122	.0918	.214	97.96	1KC	10
91.2%	.00669	.122	.0916	.220	97.87	10KC	10
92.9%	.0675	.121	.0909	.279	97.30	100KC	10
95.5%	.170	.119	.0890	.378	96.37	250KC	10
99.9%	.346	.114	.0856	.546	94.84	500KC	10

Table VI 2N1908X DISSIPATION vs. FREQUENCY

Cond. Time	P _{sw}	P _{on}	P _B	P _D	η	Freq.	V _m
45.2%	.00675	.0252	.0454	.0774	99.21	1 KC	20
46.0%	.0681	.0249	.0449	.138	98.63	10 KC	20
54.1%	.724	.0217	.0389	.785	92.75	100 KC	20
67.6%	2.04	.0153	.0275	2.08	82.92	250 KC	20
90.5%	.00339	.0506	.0911	.145	98.54	1 K	10
91.4%	.0342	.0506	.0911	.176	98.25	10 KC	10
99.5%	.351	.0473	.0851	.483	95.46	100 KC	10

Transistor efficiency versus frequency is plotted in Figure 4 for each transistor at each condition of input voltage and conduction time.

In the very low frequencies, switching time ($t_r + t_f$) is insignificant, and the 2N1908X is superior because of its lower saturation (VCS) voltage. The condition of 45% duty cycle is more efficient than the 90% condition merely because the ON losses ($P_{in} + P_{Base}$) occur for a smaller portion of the period.

In the higher frequencies, where switching time is a significant portion of the period, the 2N2880 is clearly superior by virtue of its switching speed. The 2N1908X cannot be operated much above 100KC, because of the assumed switching speed, since above this frequency the switching time soon becomes greater than the ON time. In the higher frequency region, the 90% duty cycle condition is the most efficient because the ratio of switching time/ON is less than that for the 45% condition.

Frequency Range Characteristics of Transformers

Several sample designs were done for the 10-watt output transformer shown in Figure 5. The designs were based on the use of Indiana General type O-5 material, a low loss ferrite, and the results are shown in Table VII.

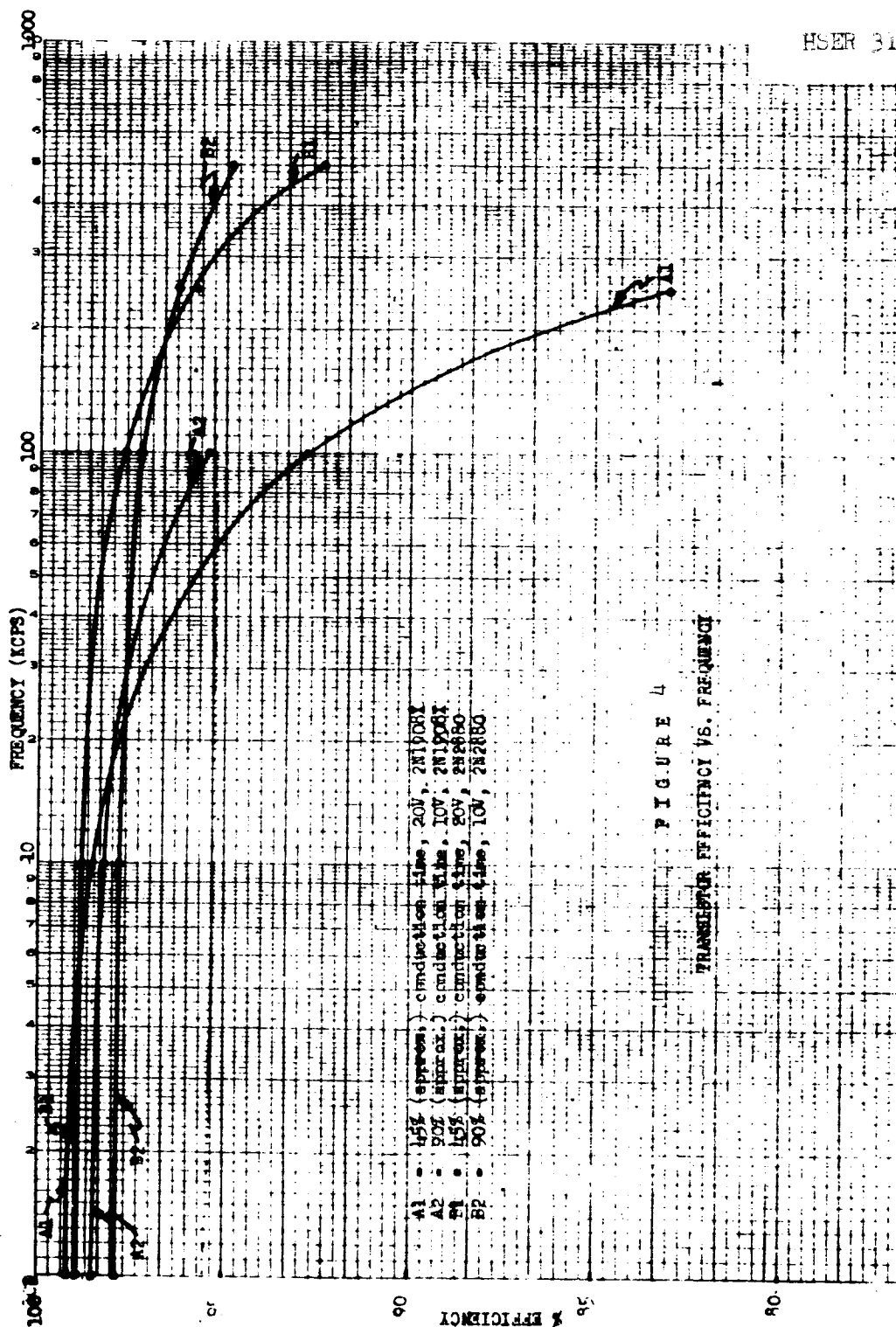


FIGURE 4
TRANSISTOR EFFICIENCY VS. FREQUENCY

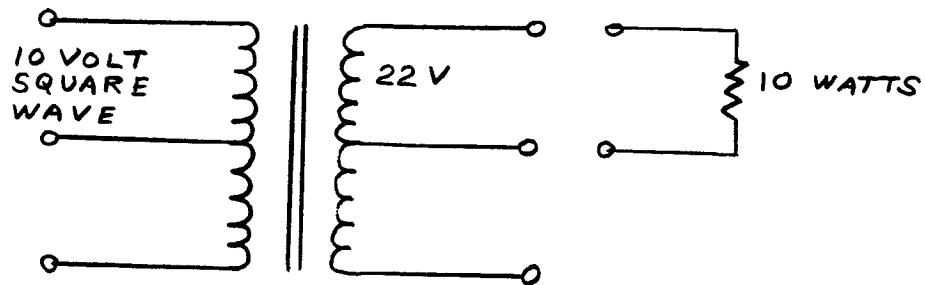


Figure 5 - 10 Watt Output Transformer

The table illustrates that relatively efficient transformers with reasonable sizes and weights can be designed for operation to at least 50 KC. What is not apparent from the table is a definitive relationship among efficiency, weight, and frequency of operation. General Electric confronted with the same problem developed an analysis to determine a definitive relationship of efficiency, weight and size versus frequency of operation. 2)

The analysis showed that core and winding losses vary as the cube of transformer dimensions while power rating varies as the fourth power of transformer dimensions. Therefore, an increase in the size of a transformer, with all other quantities held constant, will increase the efficiency of operation.

Efficiency will also be effected by the current density. Winding losses will increase as the square of current density while output power is directly proportional to this same parameter. Therefore, efficiency will ultimately be adversely affected. However, up to the point at which core and winding losses are equal, increasing current density will improve efficiency. In practice, even further increases may be desirable to improve light load operation and to attain a greater power output for a given design weight.

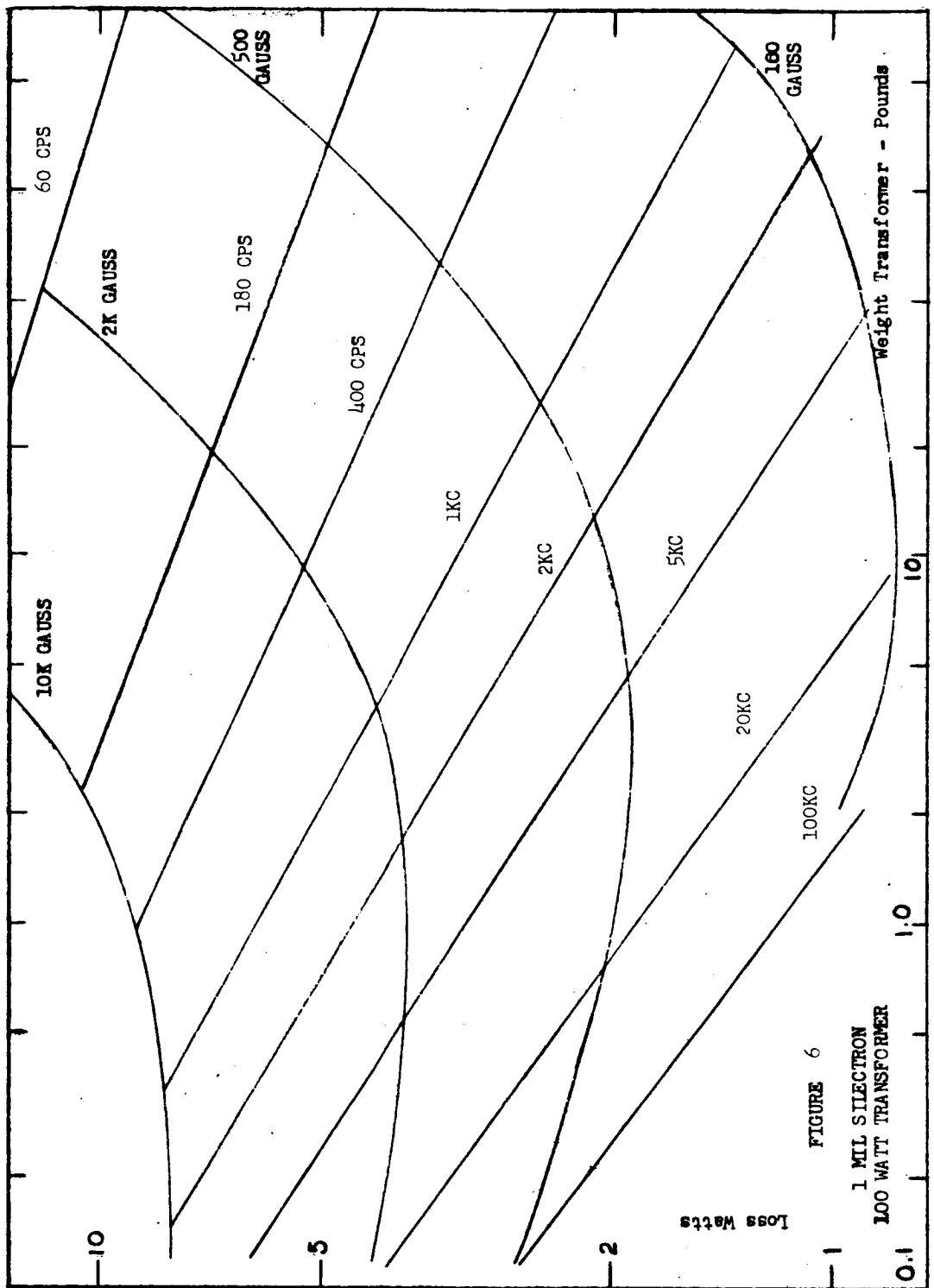
Figures 6 and 7 show power loss versus transformer weight for two different core materials. These curves are for a model 100 watt design. These curves can be used for power levels other than 100 watts with appropriate axis scaling. The shift factor K can be obtained utilizing the three-quarter power relationship.

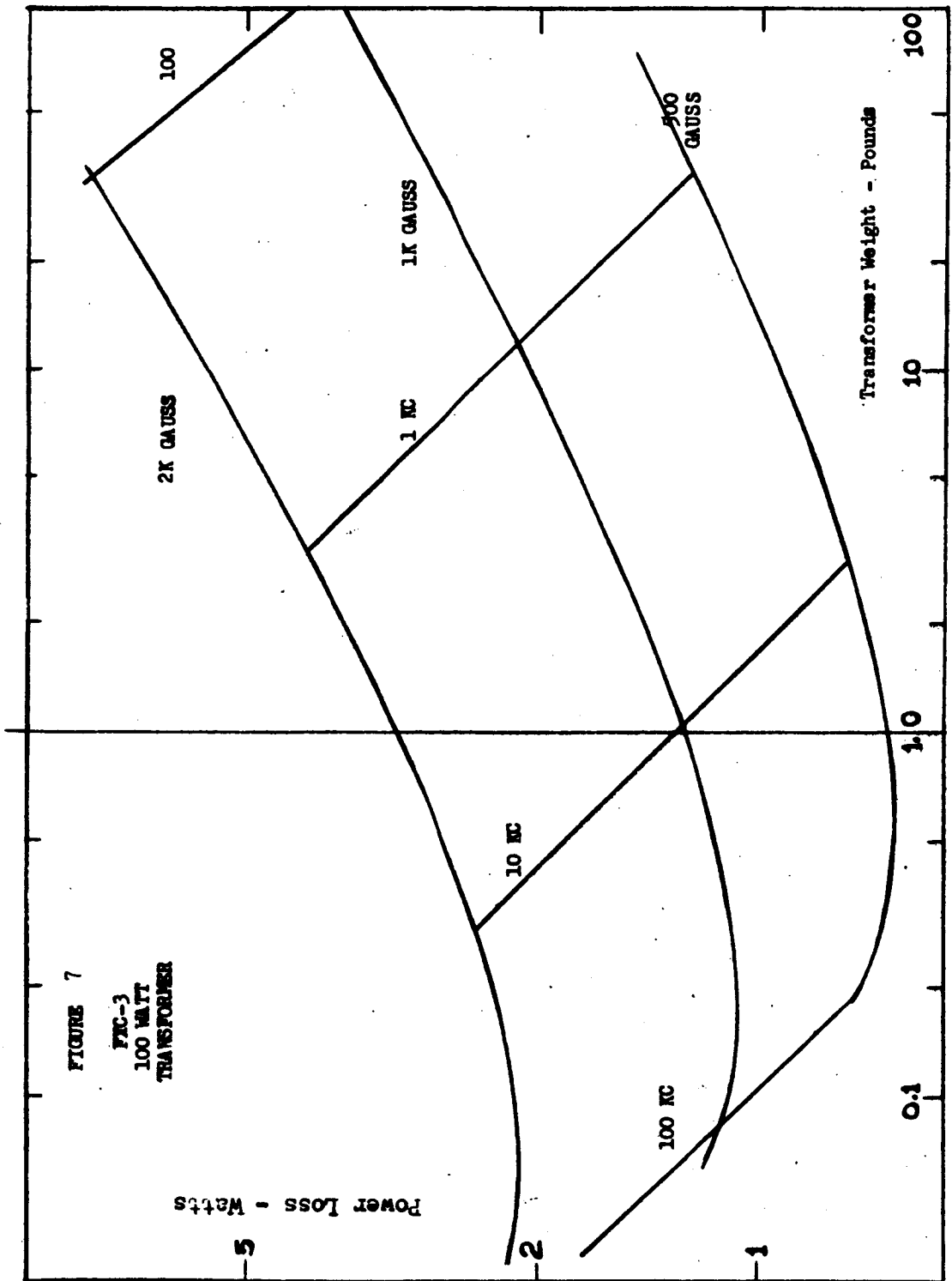
2) Voltage Regulation and Conversion in Unconventional Electrical Generator Systems, Final Report, Volume 2, August 31, 1963, Bureau of Naval Weapons Contract NCW 62-0984-d.

TABLE VII

10 WATT OUTPUT TRANSFORMER

Freq.	Flux Density	Copper Loss	Core Loss	Efficiency	O.D.	Size Ht.	Volume Cu. In.	Wt. Lbs.	Number
10KC	2 Kg	.162W	.109W	97.3%	1.43"	.62"	.99	.07	F2070
10KC	1.5 Kg	.089W	.063W	98.6%	1.8"	.80"	2.05	.164	F--626-2
25KC	750 g	.143W	.04 W	98.2%	1.5"	.62"	1.0	.072	F2070
25KC	750 g	.05 W	.045W	99.1%	1.87"	.87"	2.4	.165	CF-113
50KC	2 Kg	.07 W	.208W	97.3%	.75"	.5 "	.22	.013	F-846-3
50KC	500 g	.193W	.03W	97.7%	1.37"	.62"	.915	.048	F-624-3
50KC	500 g	.065W	.072W	98.5%	1.37"	.62"	.915	.062	F2070
50KC	500 g	.034W	.08W	98.9%	1.62"	.62"	1.28	.108	CF-113





$$\left(\frac{P_{01}}{P_{02}}\right)^{3/4} = K$$

where: P_{01} = Power rating desired
 P_{02} = 100 watt power rating
 K = shift factor

e.g. For a 10 watt transformer;

P_{01} = 10 watts

P_{02} = 100 watts

$$\left(\frac{P_{01}}{P_{02}}\right)^{3/4} = K = \left(\frac{10}{100}\right)^{3/4} = 0.18$$

Thus, values of power loss and weight, determined by the use of Figures 6 and 7, must be multiplied by 0.18 to be used for a ten watt design.

In a similar manner, changes in other design parameters can be accommodated, thus lending a universal character to these curves.

One other significant point should be mentioned: examination of these graphs clearly indicates the possibility of efficient transformer designs at reasonable weights throughout the 10 KCPS to 100 KCPS frequency range.

4.1.4 Materials Review

A review of electrical components was made to determine component availability and component limitations for high frequency switching.

Semiconductors

Vendor literature was searched for transistors with fast switching times and low saturation voltages. Table VIII shows representative, presently-available transistors within the applicable power, voltage, and current range. It is interesting to note, that, of the four germanium devices with frequency capabilities from 600 KC to 15 MC, the switching speeds are not nearly as high as most of the devices.

Table IX shows the available high-speed power rectifiers in the range of 1 to 20 amps.

VENDOR	NUMBER	TYPE	DEVICE RATING		β	REMY	LEAKAGE CURRENT	SWITCHING TIMES, TYPICAL				FORM
			POWER	BK _{CE} BV _{CE}				t _d	t _r	t _s	t _f	
MOT.	2N3297	SIL.	25W	40V	1.5	.5	.5mA					200MC
TI	2N2151	SIL.	30W	80V	2	.5	.125mA					10MC
BEN.	2N3016	SIL.	5W	50V	40	.5	.1mA					300MC
TI	2N2567	GE.	20W	60V	20	.3	.35mA	200ns	480ns	290ns	2150ns	3
TI	2N2986	SIL.	15W	120V	30	.3	.63mA					10MC
TI	2N3036	SIL.	10W	80V	30	.3	.35mA	100ns	237ns	567ns	237ns	20MC
MOT.	2N3026	SIL.	25W	60V	40	.3	.33mA					100MC
FAIR.	2N2873	SIL.	30W	80V	50	.3	.38mA	—300ns	—	—1500ns	—	20MC
TI	2N1725	SIL.	50W	80V	50	.3	.5mA					10MC
DELCO	2N3212	GE.	80V	80V	12	.5	.24mA	—3	45	3.545	145	3
SSPI	2N2849	SIL.	5W	4V	100	.5	.4mA	20ns	40ns	350ns	50ns	600KC
BEN.	2N3017	SIL.	10W	50V	30	.5	.1mA					80MC
M-H	2N2880	SIL.	30W	80V	40	.5	.28mA	20ns	25ns	700ns	440ns	300MC
M-H	MNT 6016	SIL.	40W	80V	100	.5	.5mA	20ns	25ns	700ns	440ns	50MC
M-H	MNT 2001	SIL.	5W	80V	100	.5	.15mA	—350ns	—	—	—	50MC
RCA	2N3231	SIL.	25W	80V	70	.7	.7mA					40MC
PSI	PT1941	SIL.	90W	80V	15	.7	.14mA	—	45	—	—	10MC
TI	2N1722A	SIL.	50W	80V	20	.3	.3mA	—16	45	—	—	1MC
WEST.	130-08	SIL.	120W	80V	18	.5	.5mA	—600ns	—	—	—	10
PSI	2N1902	SIL.	125W	50V	25	.5	.1mA	40ns	200ns	700ns	220ns	50MC
PSI	2N1900	SIL.			10	.5	.15mA	—	45	—	—	10MC
RCA	TA 2110	SIL.			12	.5	.15mA	—	45	—	—	15MC
TI	2N1046B	GE.	30W	50V	10	.5	.1mA					300MC
BEN.	2N3018	SIL.	25W	50V	40	.5	.1mA	12ns	200ns	1200ns	550ns	30MC
M-H	2N2814	SIL.	40W	80V	40	.5	.1mA	250ns	800ns	350ns	250ns	50MC
TI	2N211	SIL.	40W	80V	20	.5	.1mA	100ns	800ns	2500ns	1000ns	10MC
TI	2N1908	GE.	60W	50V	30	.5	.075mA	70ns	40ns	5000ns	400ns	10
TI	2N1937	SIL.	150W	80V	10	.5	.1mA	20ns	180ns	1700ns	800ns	40MC
M-H	MNT 8003	SIL.	100W	80V	40	.5	.1mA	—300ns	—	—	—	15
RCA	2N3263	SIL.	80W	90V	25	.5	.05mA					20MC
M-H	MNT 8302	SIL.	100W	80V	10	.5	.06mA					25MC

TABLE VIII PRESENTLY-AVAILABLE HIGH-FREQUENCY POWER TRANSISTORS

VENDOR	NUMBER	RATINGS		V_F	I_F	I_r	V_r	I_{rr}	t_{rr}	I_F	CASE STYLE
		PRV	I_F								
UNITRODE	UTR 01 - 61	50-600V	1a	1V	.5a	10ma PRV			100ns	1a	GLASS BEAD
UNITRODE	UTR 02 - 62	50-600V	2a	1V	.75a	10ma PRV			100ns	1a	GLASS BEAD
G.E.	IN 3958-3963	100-600V	3.5a	1.4V	2a	.4ma			3µs	10a	STUD
HUGH.	IN 3879-3883	50-400V	6a	1.4V	6a	1ma PRV		2a	200ns	-	STUD
TI	TIX 440-442	50-200V	6a	1.3V	6a	1ma PRV		1.5a	100ns	1a	STUD
HUGH.	IN 3884-3898	50-400V	12a	1.4V	12a	3ma PRV		2a	200ns	-	STUD
WEST.	379A - 379H	50-400V	12a	1.15V	12a	10ma PRV		1a	100ns	1a	DISC
HUGH.	IN 3879-3903	50-400V	20a	1.4V	20a	6ma PRV		3a	200ns	-	STUD
HUGH.	HF SERIES	EQUIVALENT TO	TO	6, 12, 20a		IN 3879-	3903 BUT		t_{rr}	(TYPICAL)	80ns

TABLE IX PRESENTLY - AVAILABLE
HIGH - SPEED RECTIFIERS

In the lower power range there are numerous transistors and diodes available with high frequency capabilities.

Magnetic Materials

One of the considerations of this program is to minimize the contribution of the magnetic components to stray magnetic fields. Several factors which contribute to stray fields are air-gaps, non-uniform winding distributions, and loose coupling between windings and core.

In surveying the available magnetic materials, both stamped laminations and c-cores were eliminated immediately because they have built-in air-gaps and because their windings cannot be uniformly distributed or tightly-coupled to the core. The hermetically-sealed, oil-filled, tape wound variety of toroids was considered, but these cores are available with a minimum tape thickness of 1 mil, which allows for operation up to about 10KCPS, beyond which the core losses become prohibitive.

The configurations which offer the most promise are the toroidal and the tape-wound bobbin cores. The toroids offer high permeability, uniform winding distribution, tight coupling, and inductive tolerances of about $\pm 20\%$ maximum. Their prime use is non-critical inductors and transformers where small size is a requirement. Their frequency range is a function of the core material, and materials available include molybdenum-permalloy, iron powder, and ferrites.

The tape-wound bobbin cores cover the frequency range of 2 KCPS to 500 KCPS. Use of stainless steel rather than ceramic bobbins is recommended, because their smaller wall thickness gives smaller winding periphery, hence lower overall winding resistance, and better ratio of core cross-sectional area to overall bobbin cross-sectional area, thus reducing flux leakage somewhat. These cores are available in either Orthonol or Permalloy 80 materials, and in tape thicknesses of 1/8, 1/4, 1/2 and 1 mil. At the present time no published core loss curves and almost no laboratory-type curves are available for these materials so that in general the vendors can only recommend what to use for a particular application.

In the power-frequency range, say up to 500 CPS, the prime requisite for core material is high permeability, and core losses and switching time are secondary considerations. In the audio range, from 500 CPS to 15 KCPS, both hysteresis and eddy current losses become important, and only moderate permeability is required. In the high frequency range, from 15 KCPS upward, eddy current losses predominate, switching time becomes important and permeability can be quite low.

Generally speaking, materials, such as Orthonol, which have very square hysteresis loops have slower switching times than those materials which have more rounded loops, such as 4-79 Molybdenum-Permalloy, at a given drive level in Oersteds.

At this time, little specific information regarding the magnitude of losses vs. frequency has been assembled. However, the following table shows, for each frequency range, the relative characteristics of the applicable core materials:

TABLE X RELATIVE CHARACTERISTICS OF CORE MATERIALS FOR SPECIFIC FREQUENCY RANGES

Freq. CPS	Core Material	Hysteresis Loss	Eddy Cur Loss.	Permeability
0.5-15KC	Moly-Perm.Powder	Low	Low	High, Decreasing
	Iron Powder	Moderate	Low	High, Decreasing
	Ferrite	High	Low	Low, Constant
15-40KC	Moly-Perm.Powder	Low	High	Moderate, Decreasing
	Iron Powder	Low	Moderate	Moderate, Decreasing
	Ferrite	Moderate	Low	Moderate, Constant
40-200KC	Moly-Perm.Powder	Low	Excessive	Low
	Iron Powder	Low	High	Low
	Ferrite	Low	Low	High

(Tape-wound bobbin cores not included because logs curves are not available)

4.2 DEVELOPMENT OF CHOPPER-REGULATOR

4.2.1 Concept Evaluation and Selection

The basic self-stabilizing chopper power stage shown in Figure 8, consists of two power transistors Q1 and Q2, two driver transistors Q3 and Q4 and a base drive transformer T1. Resistors R2 and R4 control the base current supplied to Q1 and Q2.

A description of circuit operation follows; assume transistor Q3 is biased in the forward direction. If the leakage current through resistor R3 is sufficient to turn on transistor Q2 slightly, part of the input voltage E will be applied across transformer T1. Current will flow through transistor Q3 thus driving transistor Q2 into saturation and delivering power to the load. Drive voltage for transistor Q2 is maintained for $E t$ volt-seconds until transformer T1 saturates. Drive voltage for transistor Q2 collapses after saturation of the drive transformer, thus turning transistor Q2 off. The chopper circuit is forced into a cut-off state until transistor Q4 becomes energized. When transistor Q4 becomes energized, the cycle repeats itself with transistor Q1 delivering power to the load. Note that starting of the self-stabilizing chopper is required to initiate each half cycle.

Self-stabilization of the chopper is obtained through the constant volt-second product of the saturating core drive transformer T1. The volt-second product of this transformer is capable of sustaining a voltage of E volts for a time of t seconds. Thus, at a fixed load and frequency, the on time of the core will decrease in proportion to the increase in voltage to maintain the constant volt-second product. This results in inherent regulation of the output voltage with variations of input line voltage.

The self-stabilizing chopper does not have inherent regulation for variations in load. Variations in load cause variations in output voltage. These variations in output voltage can be compensated by a variable drive frequency to the chopper stage. The variable drive frequency produces a variable off time of the chopper thus resulting in a constant output voltage.

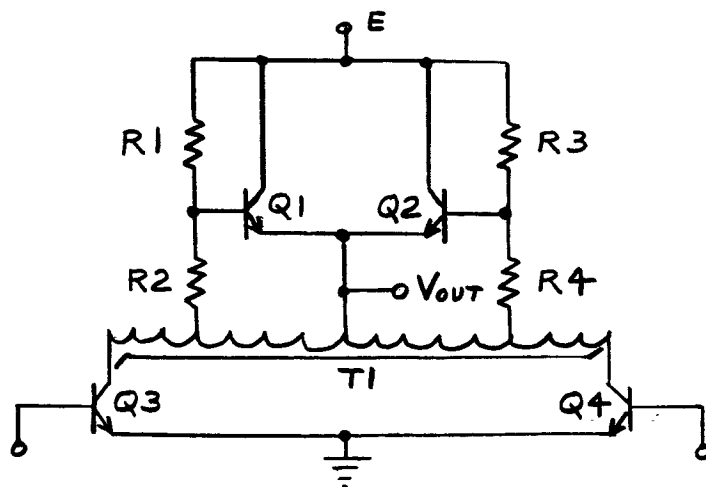


Figure 8 Basic Self-Stabilizing Chopper Power Stage

4.2.2 Initial Development Effort

Several problem areas were uncovered with the basic self-stabilizing chopper scheme early in the breadboard development stage. One problem was concerned with circuit starting. A second problem was associated with insuring rapid turn-off of the self-stabilizing chopper after the drive transformer T1 saturated. A third problem was associated with obtaining a balanced output of the push-pull stage consisting of transistors Q1 and Q2.

Circuit Starting Problem

An external means of starting the self-stabilizing chopper is required to initiate each half-cycle of operation. This is necessary since the saturation of the drive transformer T1 during the previous half cycle shuts off the main chopper transistors.

A modification was investigated and decided upon as a solution to the starting problem. This circuit utilizes a gate pulse input rather than the fixed leakage coupling previously discussed. The gate pulse is synchronized to the variable frequency square wave source so that it is applied to the bases of transistors Q1 and Q2 alternately, at the same instant that either transistor Q4 or Q3 is forward biased. The gate pulse momentarily forward biases the bases of transistors Q1 and Q2 alternately, at the same instant that either transistor Q4 or Q3 is forward biased. The gate pulse momentarily forward biases the bases of transistors Q1 and Q2 alternately, thus allowing the input voltage E to be impressed across drive transformer T1. The regeneration process is initiated, and the circuit operates as previously described.

Satisfactory starting characteristics were obtained with this starting method. All further breadboard testing was done using the gate pulse starting technique.

Circuit Recovery Time Lag Problem

The finite recovery time of the main chopper transistors, after driver transformer T1 has saturated, results in a transient low impedance condition existing across the input voltage. This causes a large current spike to be drawn through the driver transformer. This current spike introduces an additional time delay in circuit recovery time, thus resulting in significant power losses for the system. Preliminary breadboard testing indicated that if this current pulse could be limited, the recovery time of the chopper circuit could be increased, and the power losses associated with this recovery lag could be minimized.

Investigations were conducted to determine circuit methods for achieving some form of current limiting. The investigation covered three methods, designated as resistive current limiting, degenerative feedback current limiting, and transistor current limiting.

The degenerative feedback current limiting shown in Figure 10, was determined to be the best solution to the current spike problem. Assume transistor Q1 and Q3 are driven into saturation; a current spike is drawn through transformer T1 and transistor Q3 when T1 saturates. As the current increases, the voltage drop across resistor R6 also increases reducing the base-emitter bias of transistor Q3. This causes transistor Q3 to come out of saturation, thus introducing a large resistance into the line. The result is a current spike whose amplitude is significantly less than that with no current limiting.

Effects of Degenerative Feedback Current Limiting

Experimental testing has shown that the chopper system using degenerative feedback current limiting requires a larger frequency range, compared to a system with no current limiting, to maintain a constant output voltage for line and load variations. Figure 9, shows a typical collector to ground waveform in the driver stage.

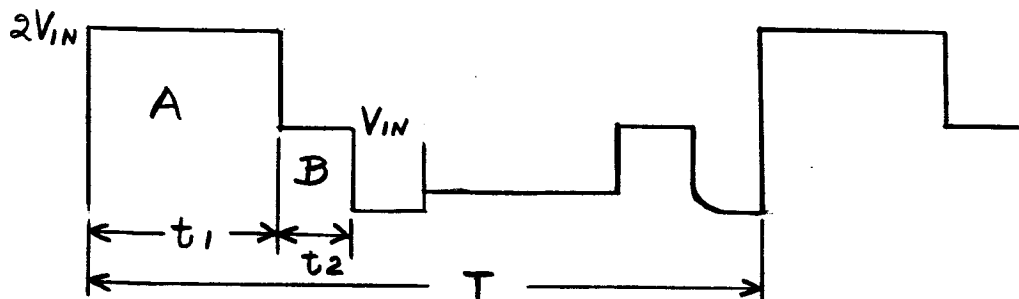


Figure 9 Collector To Ground Waveform - Driver Stage

It was found that the area of section A during transistor saturation remained relatively constant as input voltage was varied. However, both the voltage magnitude and the pulse width of section B during current limiting increased as input voltage increased. The amplitude of section B is approximately the input voltage applied from the collector to ground. The pulse width of section B appears to be dependent on the storage time of the chopper transistor. The effect of current limiting is to leave the base of the chopper transistor floating, since the magnitude of the induced reverse voltage upon saturation is made very small by this current limiting method. The magnitude of this reverse voltage is not large enough to reverse bias the chopper transistor, thus tending to increase its storage time.

As input voltage increases, the effective gain of the chopper transistor decreases. This is because the base drive for the transistor is derived from the variable input impressed across the driver transformer. The net effect is to require a larger frequency range for controlling the output voltage against line and load variations with this degenerative feedback method of current limiting.

Balanced Output Problem

A problem occurred early in the experimental testing in connection with obtaining a balanced output waveform from the push-pull chopper power stage. The asymmetrical output of the push-pull chopper occurred over the entire input voltage range and for all load conditions. The degree of asymmetry was greater at light loads than at full load. This asymmetrical operation of the chopper made operation erratic at low input voltage and heavy load. Conditions were such that only one side of the push-pull chopper could be pulse-width controlled.

Preliminary tests indicated that the problem was caused by the input impedance characteristics of the chopper transistors. It appeared that an input impedance mismatch of the chopper transistors reflected an unbalanced load of sufficient magnitude to affect operation of the saturating driver transformer. A possible solution to this problem would be to cancel out the impedance variation characteristics of the chopper transistors. To effectively do this would require the series resistors R_2 and R_4 of Figure 8 to have values significantly larger than the maximum reflected input impedance characteristics of the chopper transistors. This condition would not be compatible with the high efficiency requirement since significant power losses would now be associated with these resistors. An alternate solution to this problem would be to require matched input impedances for the chopper transistors; this would require both matching of transistor gain and base-emitter voltage. In addition, the input characteristics of the transistors would have to be closely matched for all possible voltage and load conditions.

The resultant disadvantages of the solutions above required an investigation for an alternate self-stabilizing chopper scheme. A circuit concept investigated was a single-ended version of the basic push-pull chopper. The single-ended self-stabilizing chopper power stage is shown in figure 10. Circuit operation is similar to the push-pull chopper except for the output of the driver. The output of the driver is half wave rectified through diodes D_3 and D_4 and connected in a frequency doubling configuration at the base of transistor Q_1 . Thus, transistor Q_1 operates at twice the fundamental frequency of the system. This circuit concept utilizes the full power capability of the driver stage.

The single-ended version of the chopper was tested and gave satisfactory performance. All development testing and performance testing discussed in this report was accomplished using the single-ended circuit scheme.

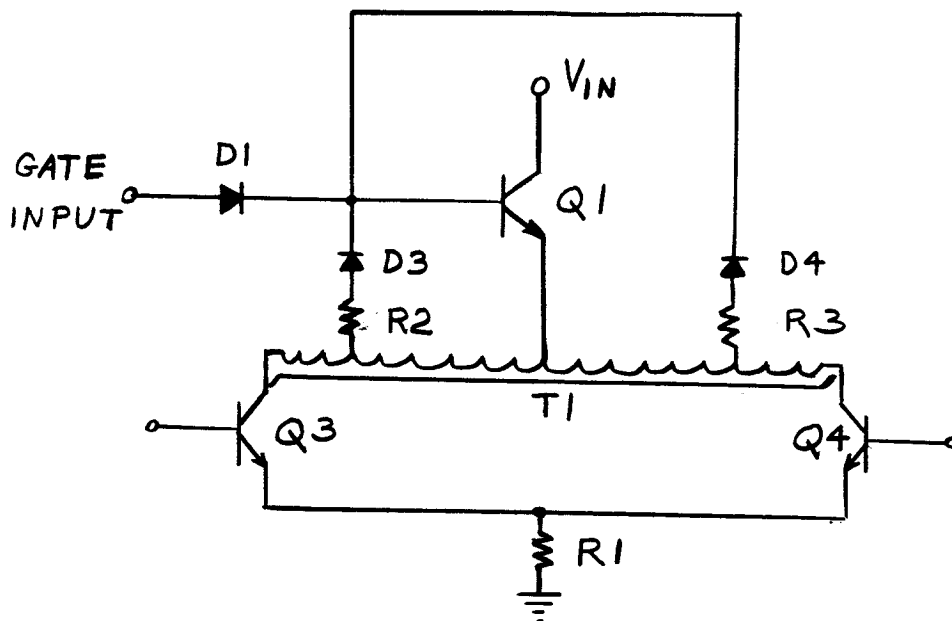


Figure 10 Single Ended Self-Stabilizing Chopper

4.2.3 Final Circuit Configuration

The final circuit configuration of the chopper power supply is shown in Figure 11. Since the chopper is working in the open loop configuration a separate voltage source is required for the variable frequency oscillator and drive circuitry.

Oscillator

The oscillator is a conventional saturating core square wave oscillator consisting of a push-pull amplifier, transistors Q1 and Q2, a saturating transformer T1, which supplies base drive to the transistors and an output coupling transformer T2. A starting circuit of diode D1 and resistor R6 insures starting of the oscillator.

The frequency of oscillation is defined by the equation $f = \frac{E \times 10^8}{4 NBA}$ where N is the number of turns on the primary of transformer T1, B is the flux density in lines/sq. inch. and A is the cross sectional area of core in sq. inches. The voltage E, impressed across the primary is a square

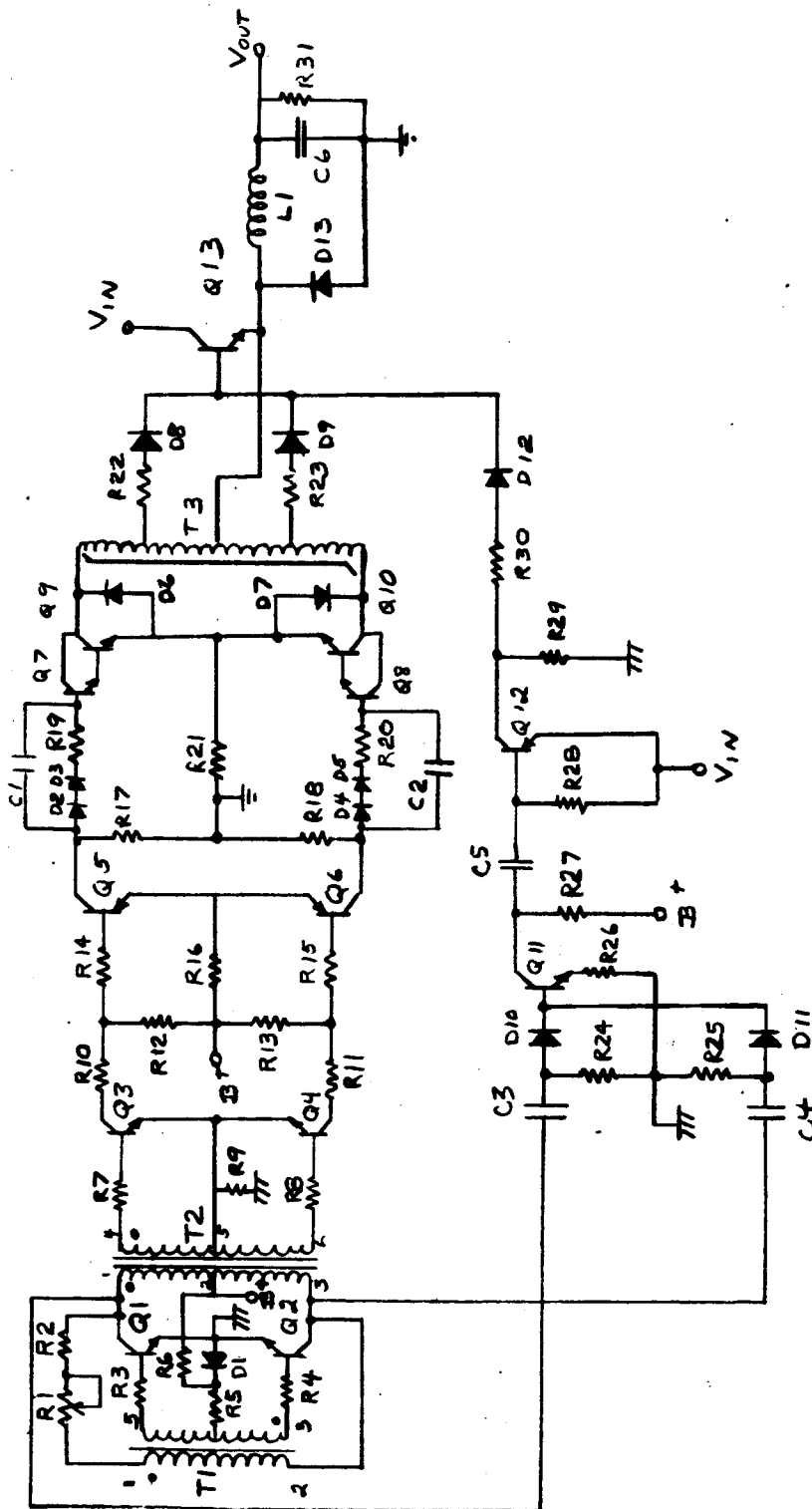


FIGURE 11
FINAL CIRCUIT CONFIGURATION
CHOPPER REGULATOR

wave with a peak amplitude equal to twice the supply voltage minus the drop across the feedback resistor R1. Thus, when the resistance of R1 is a minimum, the maximum frequency of oscillation is obtained. If resistance R1 is increased, the voltage developed across transformer T1 will decrease. Since the volt second product is constant, the frequency of oscillation will, therefore, decrease. The minimum limit of operating frequency is determined by the minimum base-to-emitter voltage required to drive the switching transistors, Q1 and Q2. The result is a range of frequencies found experimentally to be about 2.5 to 1.

The Gate Circuit

The operation of the gate circuit is as follows: The square wave across transformer T2 is differentiated by R24-C1 and R25-C2, half-wave rectified and applied to the base of transistor Q11 as a train of positive pulses at twice the frequency of the oscillator. This frequency doubling is required since the output pulses of transistor Q12 are used to gate on the chopper transistor Q13 every half cycle.

Two transistor stages are required to provide adequate amplification of the pulses to the base of transistor Q13. This is accomplished mainly by the second stage, transistor Q12, whose B+ is made to follow the input to chopper transistor Q13.

The Driver Stage

The driver stage consists of two push-pull stages (Q3-Q6) and a push-pull Darlington pair (Q7-Q10) for driving the main chopper transistor. The use of Darlington amplifiers in the third stage is necessary to achieve the high gain requirements.

The three stages in the driver are necessary in order to maintain a carefully controlled drive into the Darlington amplifier. Controlled drive is required to insure effective current limiting.

Output Filter

The output filter consists of a free-wheeling diode D13 and a low pass filter consisting of choke L1 and capacitor C6. The low pass filter averages the output of the chopper stage to provide a constant DC output.

System Operation

Assume a positive voltage is applied to the base of drive transistor Q7. At the same instant, a positive pulse from the gate circuit is

applied to the base of chopper transistor Q13. This turns transistor Q13 on for a very short instant of time. Through transformer action, base drive for transistor Q13 begins to flow. When the volt-second ratio of transformer T3 is exceeded, T3 saturates and current limiting results. The base drive to transistor Q13 collapses and Q13 turns off.

The other half-cycle is initiated when the base of transistor Q8 is forward biased at the same instant transistor Q13 is pulsed on. Regeneration occurs and the process repeats itself.

The output voltage from the chopper is applied across the free-wheeling diode D13.

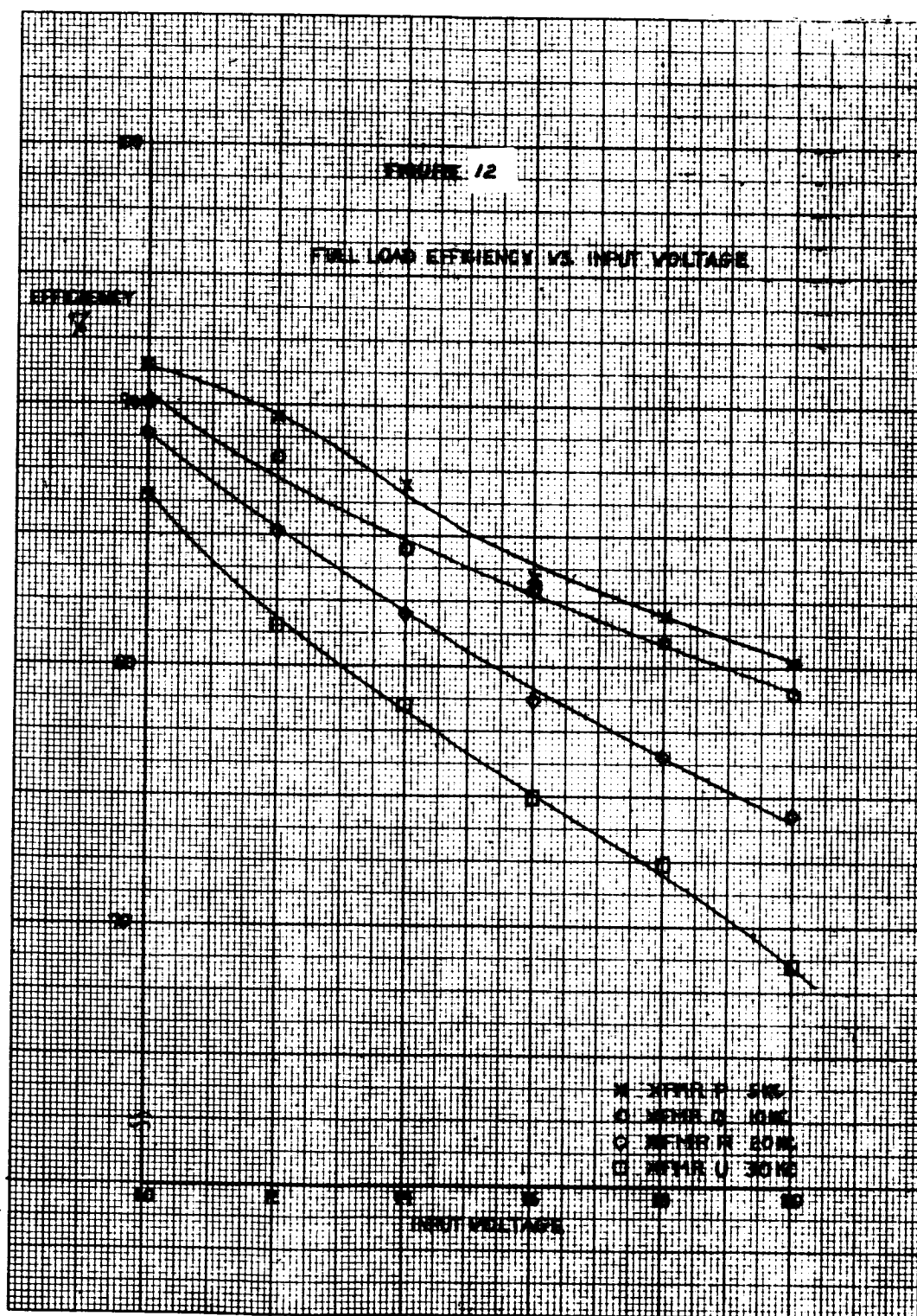
The low pass filter averages chopped voltage to provide a DC output voltage.

4.2.4 Preliminary Data

Preliminary tests were performed to determine the efficiency-frequency characteristics of the chopper circuit. Efficiency tests were run on a 10 watt self-stabilizing chopper power stage and output filter at several switching frequencies. These tests were performed to determine the frequency-efficiency characteristics of this circuit. The power stage was operated in a single-ended configuration, and a constant 470 load (approximately 2% load) was maintained across the output terminals to simulate normal control circuit loading. The efficiency measurements were based on power measurements at the input of the chopper power stage and at the output of the filter. The input power measurements included gate drive power but did not include frequency control stage power or buffer driver stage power. Efficiency measurements were made for nominal switching frequency designs of 5, 10, 20, and 30KC. The degenerative feedback current limiting technique was used in these tests.

Figure 12 shows the full load efficiency versus input voltage for each of the frequencies tested. The curves show that the drop off of efficiency is more rapid for the higher switching frequencies. The peak efficiency for the 5KC test was 91.5% whereas the peak efficiency for the 30KC test was 86.3%; both of these points occurred at 10 volts input. At 20 volts input the efficiency for the 5KC test dropped to 79.0% whereas the efficiency for the 30KC test was only 68.6%.

Investigations were conducted to determine the distribution of losses in the circuit. It was found that the bulk of the power losses were in the filter circuit with the losses increasing significantly with the input voltage. Preliminary tests showed that a significant portion of



the power losses at high voltage occurred across the free-wheeling diode. The diode used was a fast switching type, but had a typical forward drop of 0.8 volts at 1 amp. The conduction time of this diode increased to nearly 50% at 20 volts input because of the duty cycle requirement. The remainder of the losses in the filter occurred primarily across the choke as combined AC and DC losses with the DC losses alone being approximately one-half watt.

The power stage and driver stage showed relatively high efficiency of operation; the average efficiency of these stages over the input voltage range was 94%. Measurements were made of the drive losses at the input of the main chopper transistor. The drive power was mainly a function of the input voltage and was relatively independent of load. For example, the drive power at 10 volts input varied from 105 milliwatts at no load to 110 milliwatts at full load; the drive power at 20 volts input varied from 405 milliwatts at no load to 470 milliwatts at full load.

4.2.5 Chopper Scaling Design

The criterion on which the scaling was based is given below for the different stages within the system.

Saturating Core Square Wave Oscillator

The primary turns of transformer T1 were calculated for a maximum frequency of 30KC for the various B+ supply voltages according to the equation $f = \frac{E \times 10^8}{4 NBA}$

where: N = number of primary turns of transformer T1

B = Flux density in lines/square inch

A = cross sectional area of core in square inches

E = peak amplitude of the square wave across the primary

A +10% tap was added to the primary to compensate for variations in the flux density of transformer T1 and the frequency of operation of driver transformer T3.

Driver Stage

The scaling of component values within the three-stage driver was based on the power requirements of chopper transistor Q13. The value for

the degenerative feedback resistor R21 was determined experimentally based on the amount of current limiting required and the frequency range required for control of line and load variations.

Gate Circuit

The gate control stage was relatively unaffected by loading and required no major changes for the 10, 25 and 100 watt choppers.

Chopper Stage

The turns ratio of driver transformer T3, the value of the base resistors R22 and R23, and the types of transistors to be used for Q9, Q10 and Q13 were determined by the power requirements of chopper transistor Q13. The primary turns of the driver transformer were set for a maximum frequency of approximately 30KC.

Choke Input Filter

The component values for the 10 watt output filter were determined experimentally for the 10 watt unit and scaled for the 25, 50, and 100 watt converters with the following relationships:

$$L = \frac{k_1}{I_{DC}} \text{ Min.}$$

Where k_1 is a function output voltage, input frequency and percent duty cycle.

$$C = \frac{k_2}{L}$$

Where k_2 is a function of allowable peak to peak ripple voltage, input frequency and per cent duty cycle.

A high speed rectifier was selected for diode D13 to minimize power losses during switching.

4.3 DEVELOPMENT OF BOOSTER REGULATOR

4.3.1 Booster Concept and Evaluation

The push-pull inverter-rectifier was initially selected for the booster series of power supplies, as a result of the initial search and analysis phase. The preliminary tests conducted on the chopper series of power supplies indicated that the weight and efficiency goals would probably be impossible to meet with the inverter-rectifier (I/R) circuit as the basic booster configuration. Estimates of the component weight increase indicated a 40% increase in weight of the I/R booster compared to the chopper. Estimates of the efficiency loss indicated by an approximate 9% loss of efficiency of the I/R booster compared to the chopper.

These serious disadvantages required a re-evaluation of the selection of the I/R circuit as the basic booster configuration. The basic flyback converter, described in detail in the following section, has been reconsidered as the basic booster configuration. This concept has the inherent ability to overcome the weight and efficiency disadvantages of the I/R circuit discussed above.

One of the series limitations, presented in the initial analysis of the flyback converter is its inability to provide inherent protection against short circuits. Means of providing short circuit protection for this circuit are presently being actively investigated.

4.3.2 Initial Development Effort

The basic flyback circuit makes use of an induced voltage in series with the source voltage to boost the output voltage. The basic circuit is shown in Figure 13

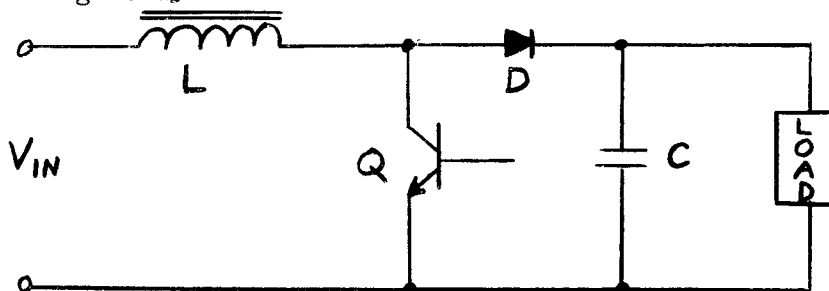


Figure 13 BASIC FLYBACK BOOSTER CIRCUIT

With transistor Q on and diode D off the voltage across the inductor L is equal to V_{IN} , and there is a linear current build-up in L. $\frac{di}{dt} = \frac{V_{IN}}{L}$

After a given time transistor Q is turned off and diode D is forward biased. The current through the inductor L is then directed through diode D, capacitor C, and the load. (L is made large enough to supply current for the load and C during the period that Q is off and D is on). During this period the voltage across L is equal to $V_{OUT} - V_{IN}$. When transistor Q turns on again, diode D is back biased, and capacitor C supplies power for the load while the input source is causing a current build-up in the inductor L.

The result is a rectangular voltage across L with a positive value of $V_{OUT} - V_{IN}$ and a negative value equal in magnitude to V_{IN} . The current through L is a dc value with a triangular wave of ripple superimposed due to the current build-up and decay through the inductor.

The output voltage is a function of the on and off time of the flyback transistor and is given by: $V_{OUT} = \frac{V_{IN}}{f t_{off}}$ where f is the frequency

of operation, and t_{off} is the off time of the flyback transistor. Thus, the output can be theoretically boosted to any voltage greater than V_{IN} . The maximum boost voltage is limited by the switching characteristics of the flyback transistor, diode, and energy storage capabilities of the inductor and capacitor.

The basic flyback power stage is not inherently line compensated. This compensation must be supplied by a pulse width modulated drive. The amount of boost is dependent on the ratio of t_{ON} to t_{OFF} , and the amount of boost required is dependent on the ratio of V_{OUT} to V_{IN} . The on-time of the flyback transistor must be made to change as V_{IN} varies to obtain inherent line regulation. This could be accomplished by a voltage level sensitive device such as the Schmitt trigger shown in Figure 14. The voltage developed across resistor R_2 is proportional to the input voltage. This voltage is compared to a linearly changing

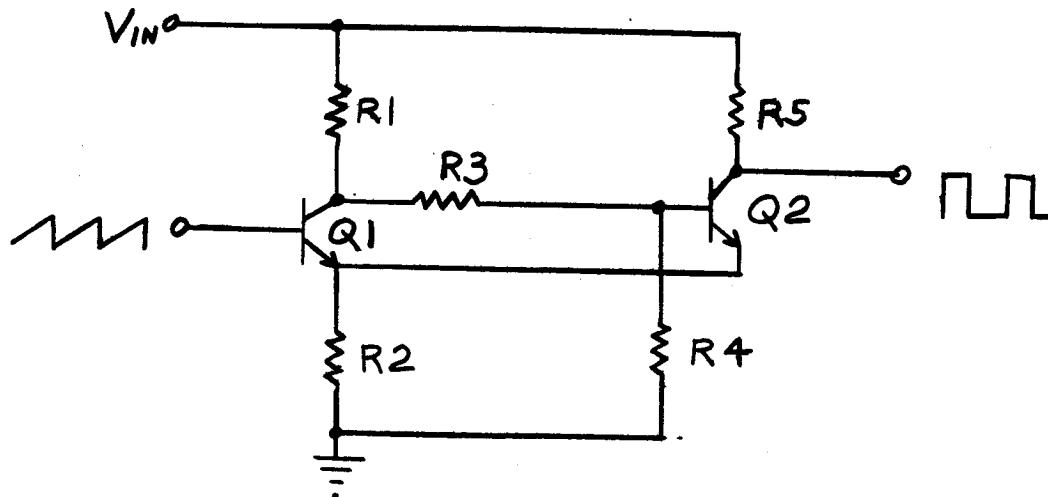


Figure 14 BASIC SCHMITT TRIGGER

voltage at the input to transistor Q_1 , thus setting the firing point of the transistor. The pulse width at the output of transistor Q_2 , is, therefore, made a function of the comparison between the ramp input to transistor Q_1 and the voltage across resistor R_2 .

4.3.2 Initial Development Problems

Several minor development problems occurred during the initial development phase. One problem was concerned with selection of choke

inductance value for proper no load and full load operation. A second problem was concerned with limiting the flyback transistor peak current. A third problem was concerned with control circuit compensation.

Choke Inductance

The current through choke L1 increases linearly during the on-time of the flyback transistor. During on-time the transistor current is equal to the choke current, thus the peak transistor current is the DC input current plus one half of the total change in current through the choke. The net change in choke current is a triangular wave that has equal positive and negative peaks about the dc level.

The magnitude of this triangular wave is inversely proportional to the choke inductance; therefore, L1 must be large enough to keep this peak current at an acceptable level.

The inductance L1 must supply current for the load, the output capacitor and the control circuits while the booster transistor is off, and the current through the inductor decreases linearly during this part of the cycle. At extremely light loads the DC current through the inductance can approach zero before the end of the off time period of the booster transistor. The voltage across the inductor decreases when this occurs. This makes the normal voltage compensation ineffective which results in an increase in the output voltage. To prevent this, a critical inductance is required and a bleeder resistor, R20, is necessary to maintain a minimum current for critical inductance.

Flyback Transistor Peak Current

The output voltage of the converter is momentarily placed across the flyback transistor at the instant of transistor turn-on. This is caused by the finite recovery time of diode D in the flyback circuit. As a result of this, the transistor draws a spike of current much greater than the normal peak switching current. A fast switching rectifier must be used for diode D to minimize this spike current.

Control Circuit Compensation

For proper operation of the line compensating section of the pulse width modulator circuit there must be a change in the trigger reference voltage proportional to each change in source voltage. The base-emitter drop of transistor Q1 must be added to the voltage across resistor R2 to get the effective reference voltage for triggering. This base-emitter drop introduces a non-linearity which must be compensated for. It can be seen from the circuit diagram of the ~~final~~ pulse width modulator

circuit (Figure 15) that the emitter-base drop of transistor Q3 compensates for only half of the drop, and the addition of diode D1 is necessary to completely compensate for the base-emitter drop in Q1.

4.3.3 Final Circuit Configuration

In the final circuit, shown in Figure 16, the basic booster circuit is driven from transformer T1 and is switched by two supplementary windings on the transformer, the trigger and reset windings. A current feedback approach is used, because it supplies efficient drive at all levels.

The trigger winding is necessary only to initiate the turn-on of the flyback transistor Q9; after turn-on the current feedback winding supplies sufficient drive to maintain saturation.

The reset winding is necessary to reset the core during the off time of the flyback transistor and to supply a large negative current spike to insure fast transistor turn-off. Capacitor C5 is charged through resistor R19 to supply the current spike necessary for reset. Resistor R18 prevents capacitor C5 from discharging excessively during turn-off, so that it can supply the voltage necessary to reset the core of the drive transformer.

The reset transistor Q8 is turned on and off by the pulse width modulated rectangular wave form transistor Q6. Transistor Q6 is used to amplify the output of the pulse width modulator circuit. The trigger transistor Q7 is turned on through capacitor C4 when transistor Q8 turns off.

The pulse width modulator, which supplies the control for switching the reset, is triggered by a sawtooth voltage formed across capacitor C1. Capacitor C1 is charged through resistor R4 and transistor Q1; the voltage across capacitor C1 is reset to zero, to initiate each half cycle. Transistor Q2 is pulsed from a conventional unijunction relaxation oscillator which operates at a frequency of about 30KC. Open loop control of the output voltage is accomplished by varying the state of conduction of transistor Q1. This is accomplished by varying its base bias with the voltage divider consisting of resistors R1, R2, and R3.

4.3.4 Booster Preliminary Data

Preliminary tests were performed to determine the efficiency-frequency characteristics of the booster circuit. Efficiency tests were run on a 10-watt booster for nominal switching frequencies of 10KC, 20KC and 40KC. Power was measured at the source terminals and the output terminals, and did not include losses in the unijunction oscillator or the ramp generator. Figure 17 shows the full load efficiency versus

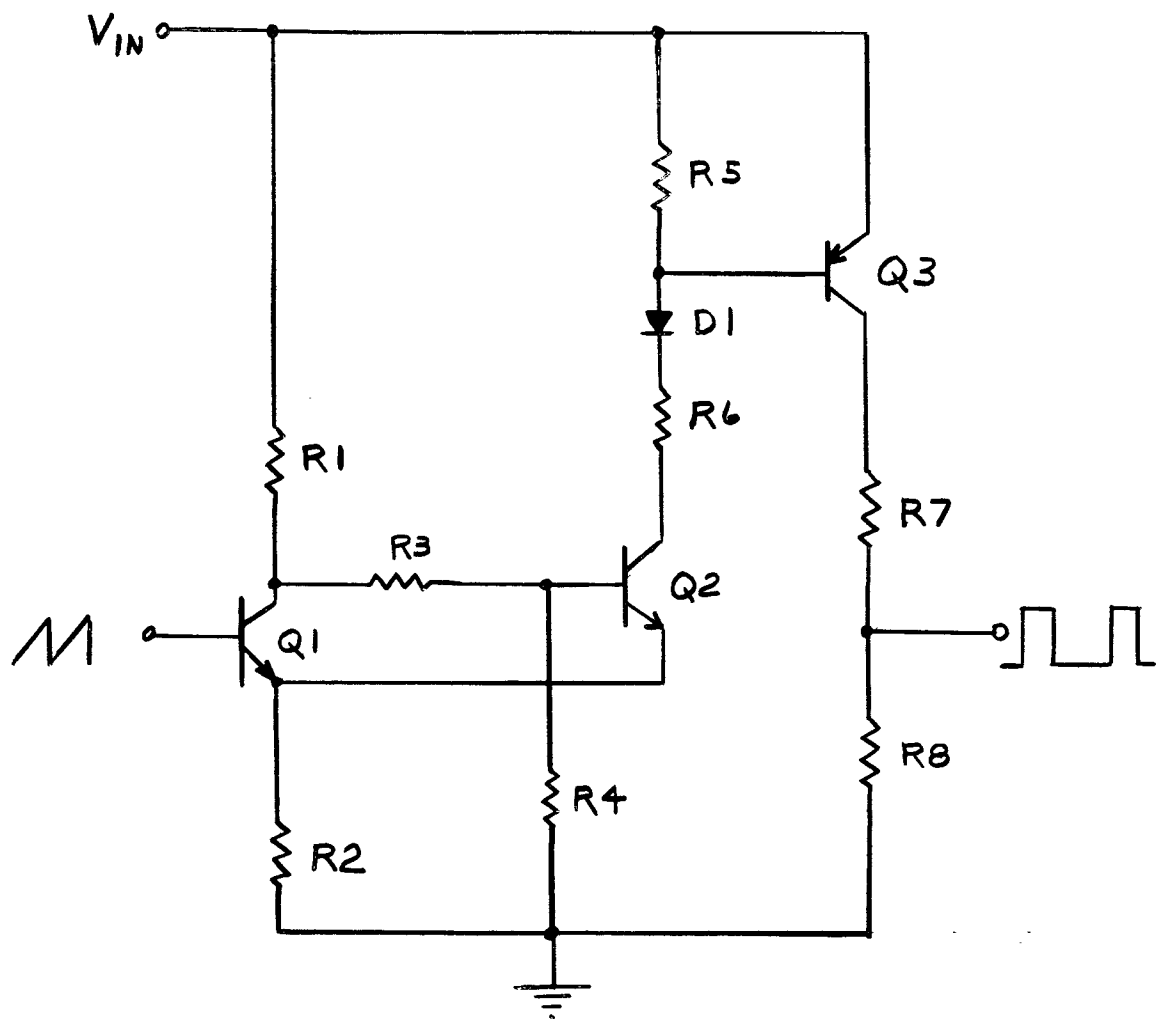


Figure 15 PULSE WIDTH MODULATOR

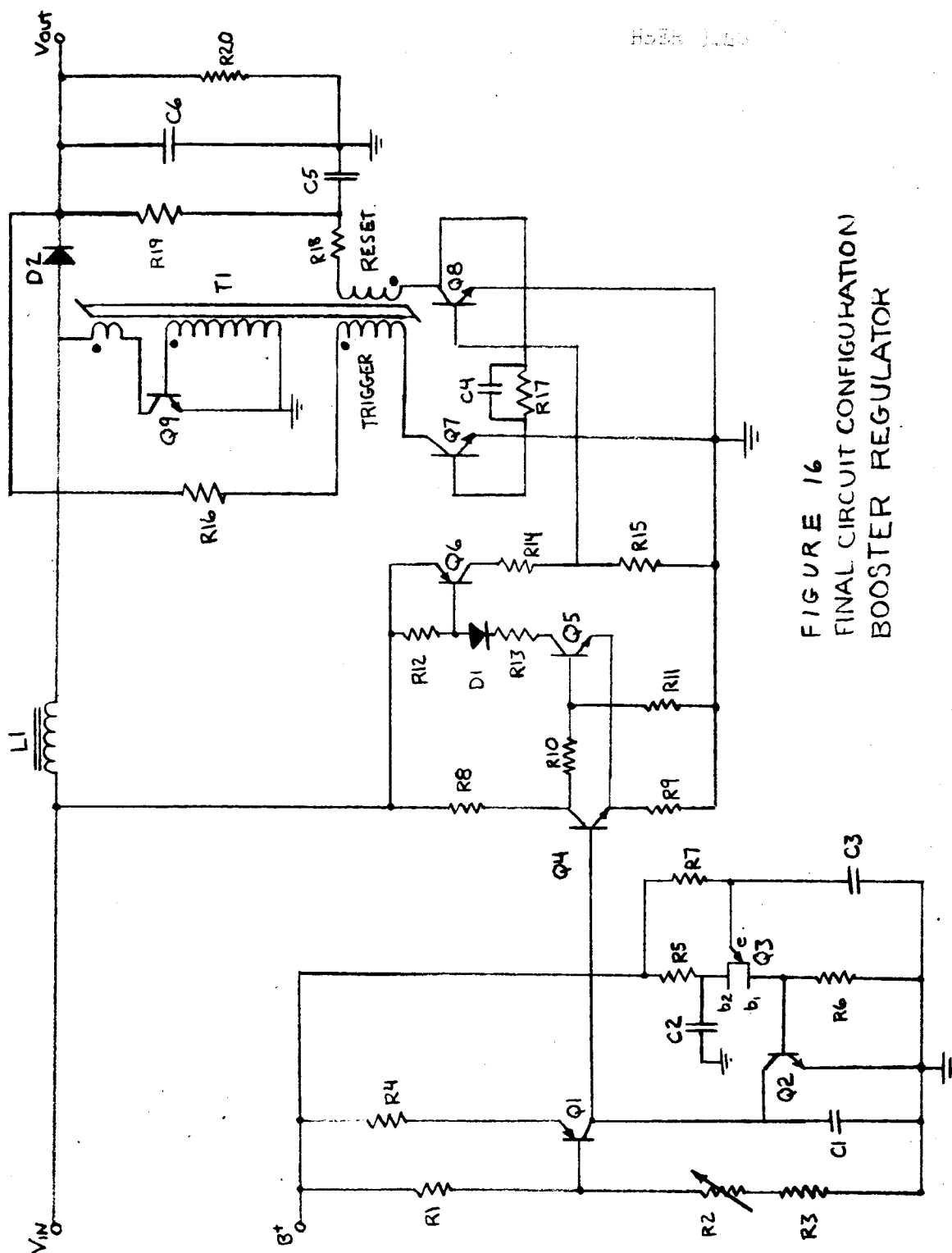
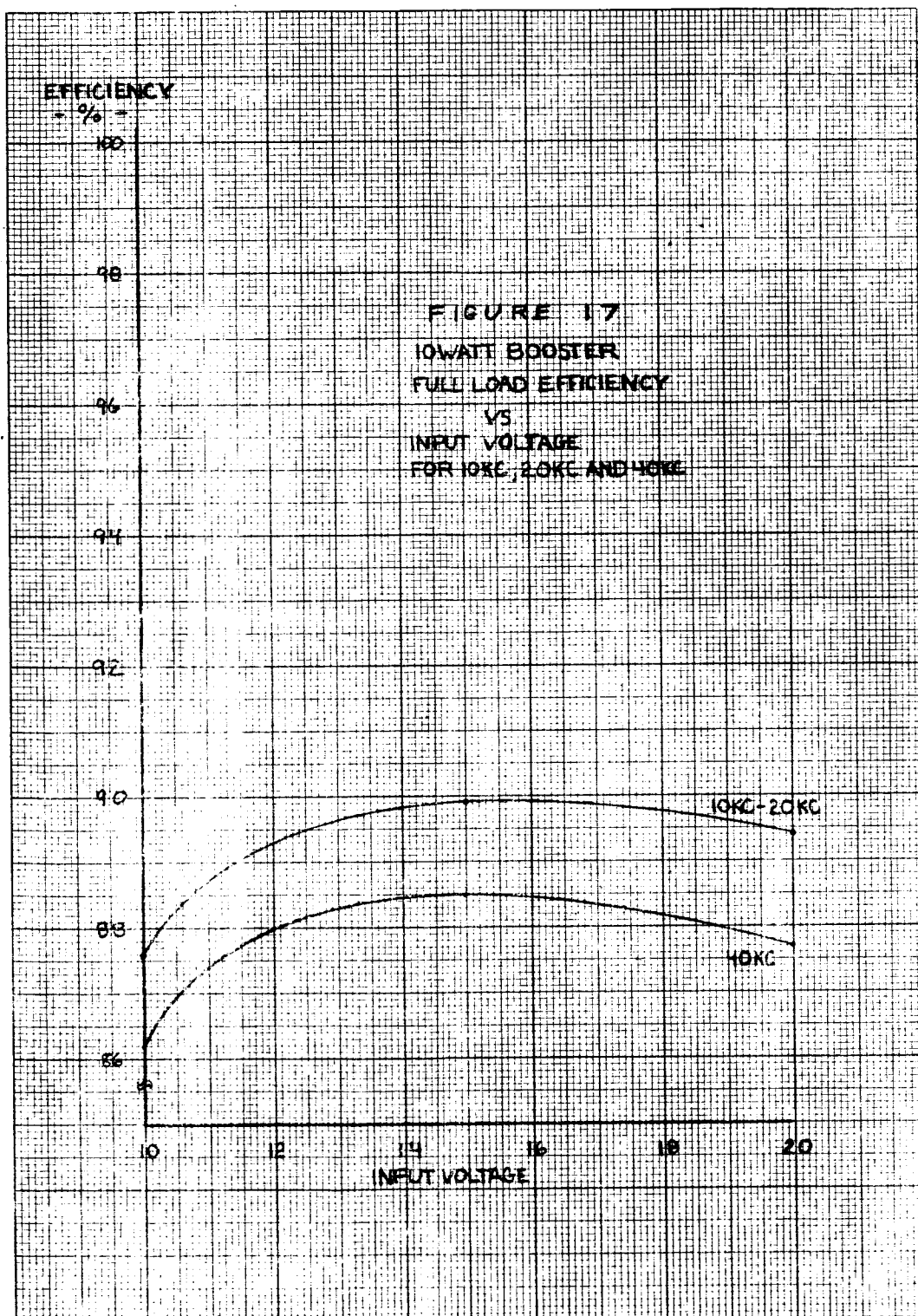


FIGURE 16
FINAL CIRCUIT CONFIGURATION
BOOSTER REGULATOR



input voltage for each of the frequencies tested. At 10 KC and 20KC the peak efficiency was 98.9% and at 40KC the maximum was 88.5%, and the minimum efficiencies were 87.6% at 10KC and 20KC and 86.2% at 40KC.

For all frequencies the maximum efficiency occurred at the 15 volt input and the minimum efficiencies were at low-line.

Investigations were conducted to determine the distribution of losses in the 10-watt booster. At low-line it was found that the bulk of the losses were fairly evenly distributed with about 0.4 watt each in the reset circuit, the flyback diode and the choke, and about 0.3 watt in the flyback transistor. At high-line the losses in the choke and flyback transistor became very small (about 0.1 watt each), and the losses in the diode were about 0.4 watt, but the reset losses increased to about 0.55 watt.

4.3.5 Booster Scaling Design

The booster was divided into two main sections; The power stage and the control stage. The control stage consisted of a unijunction relaxation oscillator, a linear ramp generator, a pulse width modulator, and the trigger-reset circuit.

The control stage was relatively unaffected by loading and required no major changes for the 10, 25 and 50 watt boosters, because the base drive for the power stage was supplied by a current feedback transformer. The 100 watt booster operated at higher voltage levels, therefore, all resistors were increased in proportion to the voltage increase to keep the current levels approximately constant.

The power stage, which consisted of the basic flyback circuit and driver transformer, had to be scaled for the different current levels of the 10, 25, and 50 watt units and the higher voltage levels of the 100 watt unit.

The critical value for L is defined by the minimum DC input current with no external load on the booster. This was assumed to be approximately 5% of full load input current. At the critical value $I_{DC} = \frac{\Delta i}{2}$

Δi = peak to peak ripple current in amperes and L was defined by:

$$L = \frac{E_{IN} (E_{OUT} - E_{IN})}{f E_{OUT} \Delta i} \quad \text{henrys}$$

f = frequency of operation

L was calculated for the condition where E_{IN} was equal to one half E_{OUT} ; it can be shown that this is the maximum value for L .

The flyback transistor Q9 was sized according to peak collector current which was approximately equal to the DC input current. Diode D2 was sized by the average current through it which was calculated as the product of the DC input current and the duty cycle of the diode.

The transformer was unchanged for the 10, 25, and 50 watt units except for wire size. The 100 watt booster operated at a higher voltage, thus, the number of turns in the reset wind was increased.

Capacitor C6 was sized by voltage rating and permissible ripple voltage. The ripple voltage requirements were satisfied by:

$$C = \frac{E_{OUT} - E_{IN}}{f R_L \Delta V} \quad \Delta V = \begin{array}{l} \text{peak to peak output ripple} \\ \text{voltage} \end{array}$$

$$R_L = \text{load resistance}$$

The lowest values for E_{IN} and R_L were used to calculate the minimum capacitance necessary to satisfy the ripple requirements.

4.4 BREADBOARD TESTING AND EVALUATION

Selected performance tests were run on the four chopper and four booster breadboards. The following tests were performed on each class of breadboards:

1. Efficiency
2. No load losses
3. Open loop regulation for line variations
4. Open loop regulation for load variations
5. Open loop regulation for line and load variations
6. Open loop regulation versus temperature
7. Output voltage stability
8. Overload and short circuit characteristic
9. Output voltage ripple
10. Input current ripple
11. Frequency control versus input voltage for the chopper breadboards and per cent duty cycle characteristic versus input voltage for the booster breadboards.

Performance curves from the test data are included in appendices I and II. Included with the performance data is a detailed data analysis for the 10 watt chopper and 10 watt booster.

1.5 MODULARIZATION

The overall objective of this program was to satisfy anticipated satellite power conversion system requirements by utilization of modularization concepts for the power conversion circuits. The anticipated modular breakdown consisted of: a regulator-converter module for obtaining voltage regulation and control for DC source variations; DC to DC conversion modules for obtaining isolation, voltage transformation, and multiple output voltages; output regulator modules for providing the required matching characteristics to the load. The present program was limited in scope to modularization of the non-dissipative regulator-converter portion of this system.

The original goals set forth in this program were modularization with respect to output voltage level, and to output power level. Modularization with respect to output voltage level was divided into two groups, one group being those converters having output voltages less than the minimum input voltage, and the second group being those converters having output voltages greater than the maximum input voltage. The converters in these groups were categorized as either choppers or boosters respectively. Modularization with respect to output power level was made at the output power levels of 10, 25, 50, and 100 watts.

The direct result of this modularization approach was to pursue separate programs of development for the chopper regulator converter and for the booster regulator converter. Each of the regulator-converter concepts were to be capable of being scaled to the desired output power levels. Modularization within each converter concept was established as a goal wherein specific signal and control circuits could be made independent of power level. Achievement of this goal would enable these circuits to be utilized at any power level.

The modularization goals achieved during the Phase I program for the chopper regulator were:

1. Scaling with respect to power level was possible.
2. Selection of components for the power stage, driver stage, and filter stage was power dependent.
3. Circuits common to all power levels was restricted to the variable frequency source and the chopper transistor gate circuit.

The modularization goals achieved during the Phase I program for the booster regulator were:

1. Scaling with respect to power level was possible.
2. Selection of components for the power/filter stage and trigger/reset driver stage was power dependent.
3. Circuits common to all power levels was restricted to the fixed frequency source and pulse width modulator circuits.

5.0 CONCLUSIONS AND RECOMMENDATIONS

5.1 CHOPPER - REGULATOR

The final configuration selected for the power stage for the chopper-regulator series is the single - ended self-stabilizing chopper. External gate triggering has been selected as the most suitable means of circuit starting. The degenerative feedback method of current limiting was shown to be the most effective method of improving circuit recovery time. This method of current limiting required a significantly larger range of operating frequency to maintain output voltage control.

The frequency-efficiency tests on the chopper regulator have shown that the peak efficiency occurs at minimum input line, and that a nominal switching frequency of 30 KC was a reasonable frequency consistent with minimum size and maximum efficiency. Analysis of these tests showed that bulk of the power losses were associated with the output filter. Optimization of the output filter should improve this efficiency characteristic. The efficiency tests at full load ranged from 83.5% at 10 watts to 89.9% at 100 watts. This was mainly caused by the power losses within the circuit becoming a smaller percentage of the total output power as the power level increased. At a constant power level, the efficiency decreased as the input voltage increased because the power losses within the circuit were higher at maximum input voltage.

The no load losses increased as the power level increased. This was caused by the higher current being drawn by the 5% bleeder resistor at the higher power levels.

The open loop voltage regulation tests for line and for load showed that the chopper power supply with degenerative feedback current limiting had poor inherent regulation. This problem was caused by the storage time of chopper transistor Q13.

The frequency range vs. input voltage tests showed that approximately a 2.5 to 1 frequency range was required to maintain a constant output voltage. This range could be decreased if the storage time of chopper transistor Q13 were reduced.

The open loop voltage regulation vs. temperature tests have shown that the chopper power supply exhibits a positive temperature coefficient characteristic. This condition can be brought within specification when the system is operated in the closed loop configuration.

The output voltage stability test showed that the output voltage exhibited an increasing upward trend during the forty-four hours. To be considered conclusive, this test would have to be run over a longer period of time with many more points recorded.

The overload and short circuit characteristic tests showed that the chopper switches into a constant current mode of operation as the load is increased above 100%. The amplitude of the constant current was higher at maximum input voltage than at minimum input.

The output voltage ripple tests have shown that the low frequency components were higher at no load than at full load and that they increased as the input voltage increased. The tests also showed that an RFI type filter would be required to reduce the high frequency ripple components to be within acceptable limits.

The input ripple tests showed that the chopper had no inherent means of filtering the ripple current feedback, since the ripple current feedback was the peak switching current. The tests showed that the low frequency components were higher at full load than at no load. At no load, the ripple was fairly constant. At full load, the ripple was a minimum at low-line, increased and leveled off at high-line.

5.2 BOOSTER - REGULATOR

The final circuit configuration selected for the booster-regulator series is the single-ended flyback booster controlled by a line compensated variable pulse width modulator.

The results of the preliminary frequency-efficiency data indicated that 30KC was a reasonable operating frequency consistent with minimum size and maximum efficiency.

The full-load efficiency of the booster power supplies showed an increase with power level; at 10 watts the peak efficiency was 87.7% and at 100 watts the efficiency reached 95.0%. For all power levels the efficiency was greatest at the higher input voltage.

The no-load losses increased at the higher power levels, because the lower inductances used required larger minimum dc currents. The open loop regulation for all variations of line and load was within $\pm 5\%$ of 22.00 VDC for the 10 watt booster and $\pm 2\%$ of 35.00 VDC for the 100 watt booster. Limiting the minimum load to 25% the variations in output voltage were reduced to $\pm 3.4\%$ for the 10 watt booster and $\pm 1.6\%$ for the 100 watt unit. The regulation could be improved considerably by optimizing the choke and reset circuitry.

In the output voltage vs temperature regulation tests, the 10 watt and 100 watt boosters exhibited negative temperature coefficients, while the 25 and 50 showed positive temperature coefficients. These variations of output voltage with temperature were due to the temperature coefficients of the semiconductor junctions, and they can be brought within specifications with closed loop operation.

The overload test indicated that there was no short circuit protection. The output voltage dropped off due to IR drops as the load was increased, but the drop-off was not sufficient to protect the unit or its source.

The percent duty cycle data showed that a control range from about 5% to 55% on-time was capable of regulating the output of all the booster power supplies.

Both input ripple current and output ripple voltage were considerably higher than allowable. This indicated that either a larger choke and output capacitor were necessary, or supplementary L-C filters would have to be added to the input and output of the booster power supplies.

The stability data indicated a general trend toward increasing output voltage over a period of 44 hours. To be conclusive, however, this test would have to be run over a longer period of time with many more data points taken.

5.3 OVERALL RECOMMENDATIONS

It is recommended that the present booster concept be further developed in the Phase II program. The further development work would include optimizing the filters required to satisfy the input/output ripple requirements, and optimizing the control circuits. Final effort would then be directed to obtaining satisfactory closed loop performance with this series of power supplies.

It is recommended that the present chopper concept, which utilizes the variable pulse width variable frequency scheme, be discontinued. The problems associated with circuit starting and current limiting have required that complex auxiliary circuits be used to obtain proper performance of the basic power stage concept. In addition, major effort is still required to obtain good inherent line regulation because of the turn-off problem of the main chopper transistor.

It is recommended that the basic control concept developed for the booster power supplies to the chopper power supplies, since the booster control concept has been shown to provide tighter inherent line compensation and higher overall efficiency. With this concept, further development work for the chopper would include optimization of filters and control circuits and obtaining satisfactory closed loop performance.

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7.0 CONFERENCES

On July 5, 1964, a conference was held with Messrs. Yagerhofer and Pasciutti of NASA Goddard. Discussion concerned program progress, philosophy of the study, and a review of the literature search. The criteria for selection of circuitry was reviewed, and weighting factors established.

On September 25, 1964, a second conference was held with Mr. Pasciutti. Program progress was discussed, and a rough draft of the first quarterly report was reviewed. It was decided that the original program plan should be modified somewhat, with the aim of performing most of the analytical and feasibility investigations before any formal breadboard work was initiated.

A conference was held at NASA, Goddard on July 1, 1965. In attendance were Messrs. F. Yagerhofer and E. Pasciutti representing NASA, and Messrs. E. Trifari and F. Raposa representing HSED. Technical status and contract status of the program were reviewed. Program extension for the phase I program and initiation of the phase II program were discussed and agreed upon.

A conference was held at NASA, Goddard on November 29, 1965. In attendance were Messrs. F. Yagerhofer, E. Pasciutti and G. Burgholder representing NASA, and Messrs. E. Trigari and F. Raposa representing HSED. The outline for the final project report for the Phase I program was reviewed and approved by the NASA technical representatives.

Technical status of the booster concept effort then in process was discussed in detail. A request for contract modification was submitted for retention of the breadboards from the Phase I program for the remainder of the Phase II program.

8.0 NEW TECHNOLOGY

Not applicable during this reporting period.

APPENDIX I

BREADBOARD TEST DATA

CHOPPER REGULATOR POWER SUPPLIES

NOTE

Selected electrical performance tests were run on the four chopper breadboards. The data for the 10-watt breadboard is shown in Figures I-1 through I-11 and typical waveforms of output voltage ripple and input current ripple are shown in Figures I-12 through I-13. Data for the 25, 50 and 100 watt breadboards is shown in Figures I-14 through I-19.

An analysis of the 10 watt chopper breadboard data is presented in this section.

I-1 Efficiency

At full load, the efficiency decreased from 83.5% to 69.5% as the input voltage increased from 10 VDC to 20 VDC. A large part of the power losses in the circuit were in the power stage and the output filter. As the input voltage increased to maximum, the power losses also increased to a maximum, the bulk of the losses being across the free-wheeling diode and the filter choke.

At a constant input voltage, (i.e. 20 VDC), efficiency decreased from 69.5% to 47.5% as the load was decreased from full load to 25% load. This decrease in efficiency was primarily due to the constant base drive associated with constant input voltage. Thus, the drive losses at full load were smaller percentage of the total power drawn from the input than at no load.

I-2 No-Load Losses

The no-load losses increased slightly as the input voltage increased from a minimum to a maximum. This is because the power losses within the driver stage, power stage and output filter increased as the input voltage increased.

As the power level increased from 10 watts to 100 watts, the no load losses also increased. This is caused by the increased power losses within the driver stage, power stage, output filter and load at the higher power levels. However, the bulk of the increased loss is in the filter and load because a bleeder resistor of approximately 5% load is required at the no load condition. Thus, as the power level increased from 10 watts to 100 watts, the bleeder current increased. This caused additional loss in the filter and the load.

I-3 Open Loop Regulation For Line

The frequency was set for an output voltage of 9.0 VDC at 10 VDC input. Keeping the frequency constant, the output voltage had increased to 12.57 VDC at full load as the input voltage was increased to 20 VDC.

This increase in output voltage at constant load was caused by the increase in storage time of chopper transistor Q13. The increased storage time was due to the decrease in the effective gain of chopper transistor Q13 as a result of overdrive.

The output voltage was also set for 9.0 VDC at 10 VDC input for a no load condition. Keeping the frequency constant, the output voltage had increased to 14.23 volts at 20 VDC input. Again, this increase in

output voltage was due to the storage time of transistor Q13. At no load, the overdrive condition was greater than at full load. This was because the base current was relatively independent of load whereas the peak collector current is lower at no load than at full load. This caused the storage time of Q13 to further increase as compared to full load.

I-4 Open Loop Regulation For Load

The frequency was set for an output voltage of 9.0 VDC at full load and 10 VDC input. Keeping the frequency and input voltage constant, the output voltage increased to 9.947 VDC as the load was decreased to no load. This increase in output voltage was caused by; a decrease in the voltage drops in the chopper transistor Q13, and an increase in its storage time.

An output voltage of 9.0 VDC was set at full load and 20 VDC input. Keeping the frequency and input voltage constant, the output voltage increased to 13.92 VDC as the load decreased to no load. This increase in output voltage at 20 VDC input is caused mainly by the storage time of transistor Q13. This is because its base current is highest at 20 VDC input. Thus, as the load current decreased, the collector current of Q13 also decreased causing a greater overdrive condition at 20 VDC input than at 10 VDC input. This resulted in a higher output voltage at no-load at 20 VDC than at 10 VDC input.

I-5 Open Loop Regulation for Line and Load

The frequency was set for an output voltage of 9.0 VDC at 15 VDC input, full load. Keeping the frequency and load constant, the input was decreased to 10 VDC. The output decreased to 7.405 VDC. The input was then increased to 20 VDC and the output voltage increased to 10.31 VDC. This change in output voltage was caused primarily by the change in storage time of chopper transistor Q13.

At no load, the output voltage varied from 10.04 VDC to 16.11 VDC as the input increased from 10 VDC to 20 VDC, and was about 13.2 VDC output at 15 VDC input. Since the output was initially set at 15 VDC input, full load, this increase in output voltage to 13.2 VDC at 15 VDC input, no load was attributed to the very low collector current at no load. This resulted in an overdrive condition since the base current is relatively independent of load and thus caused an increase in storage time of Q13.

The change in output voltage from 10 VDC to 20 VDC input was greater at no load than at full load, which was primarily due to increased storage time.

I-6 Frequency vs. Input Voltage

At no load, 9 VDC output, the frequency varied from 18,160 cps to 11,335 cps as the input increased from 10-20 VDC. At full load, 9 VDC output, the frequency varied from 25,970 cps to 17,280 cps as the input voltage increased from 10-20 VDC. This decrease in frequency at a constant load was caused mainly by the increase in storage time of chopper transistor Q13 as the input voltage increased.

The frequency range at full load was greater than at no load because the losses in the power stage and filter stage are higher at full load.

At 10 VDC input, 9 VDC output, the frequency increased from 25,970 cps to 18,160 cps as the load decreased from full load to no load. At 20 VDC input, 9 VDC output, the frequency decreased from 17,280 cps to 11,335 cps as the load decreased from full load to no load. This decrease in frequency from full load to no load was a result of the increased storage time of chopper transistor Q13. This was because the storage time of Q13 varied inversely with changes in load current.

I-7 Open Loop Regulation vs Temperature

The output voltage of the 10 watt chopper was set at 9.0 VDC at full load, 15 VDC input in an ambient temperature of +21° C. Without resetting the frequency, the temperature was increased to + 70° C and maintained there for one hour. The output voltage at the end of one hour increased to 9.812 VDC. The temperature was then decreased to -20° C and maintained there for one hour, at which time the output was recorded to be 8.466 VDC. The temperature was then increased to +21° C ambient, and the output voltage returned to 9.0 VDC.

I-8 Output Voltage Stability

The frequency of the ten watt chopper was set for an output voltage of 9.0 VDC at 15 VDC input, full load. The unit was then allowed to operate continuously for 48 hours.

From the data, it can be seen that output voltage exhibits an increasing upward trend during the 44 hours. To be considered conclusive, this test would have to be run over a longer period of time with many more points recorded.

I-9 Overload and Short Circuit Characteristics

At 10 VDC input, the output voltage remained constant from no load to 117% load. The chopper breadboard then switched into a constant

current mode of operation, and the output power dropped off rapidly. At about 1.4 VDC output, the system switched out of the constant current modes, and the current increased to a maximum of 2.7 ADC at zero ohms short circuit.

At 20 VDC input, the output voltage remained constant from no load to approximately 360% load. The open loop output then switched into a constant current mode of operation, and the output power dropped off rapidly. The current remained constant at 4.7 ADC into the zero ohm short circuit.

I-10 Output Voltage Ripple

The ripple voltage was divided into two components, The low frequency component was interpreted as the ripple below one megacycle and the high frequency component as all ripple over one megacycle.

The low frequency output ripple voltage at both no load and full load increased, peaked and then dropped off as the input voltage increased from 10 VDC to 20 VDC. This indicated that the AC components of the voltage across the input to the filter peaked and then dropped off as the input increased to 20 VDC input.

The output ripple voltage was higher at no load than at full load. This was because of the lower frequency of operation at no load which resulted in the decreased attenuation of the AC components by the filter.

I-11 Input Ripple Current

The input ripple current was defined as the zero to peak input current which was switched by the chopper power stage. It was divided into two components; the low frequency component was interpreted as the ripple below one megacycle, and the high frequency components as all ripple over one megacycle.

The low frequency input ripple current at full load was a minimum at 10 VDC input voltage. The peak current is a function of the duty cycle of the chopper power stage and of the current drawn during current limiting.

Since the duty cycle at 10 VDC was very high, the current limiting was negligible. This resulted in a minimum value of peak current drawn from the input and thus a lower value of ripple current. As the input voltage increased, the input current increased and then leveled off at a peak current determined by the current drawn during current limiting.

The low frequency input current ripple at no load remained relatively constant as the input increased from 10-20 VDC. This was because the peak current was a function of the current drawn during current limiting which remained constant for changes in line voltage.

FIGURE I-1
EFFICIENCY VS. INPUT VOLTAGE
10 WATT CHOPPER

EFFICIENCY
%

100

90

80

70

60

50

40

FULL

LOAD

3/4

LOAD

1/2

LOAD

1/4

LOAD

10

12

14

16

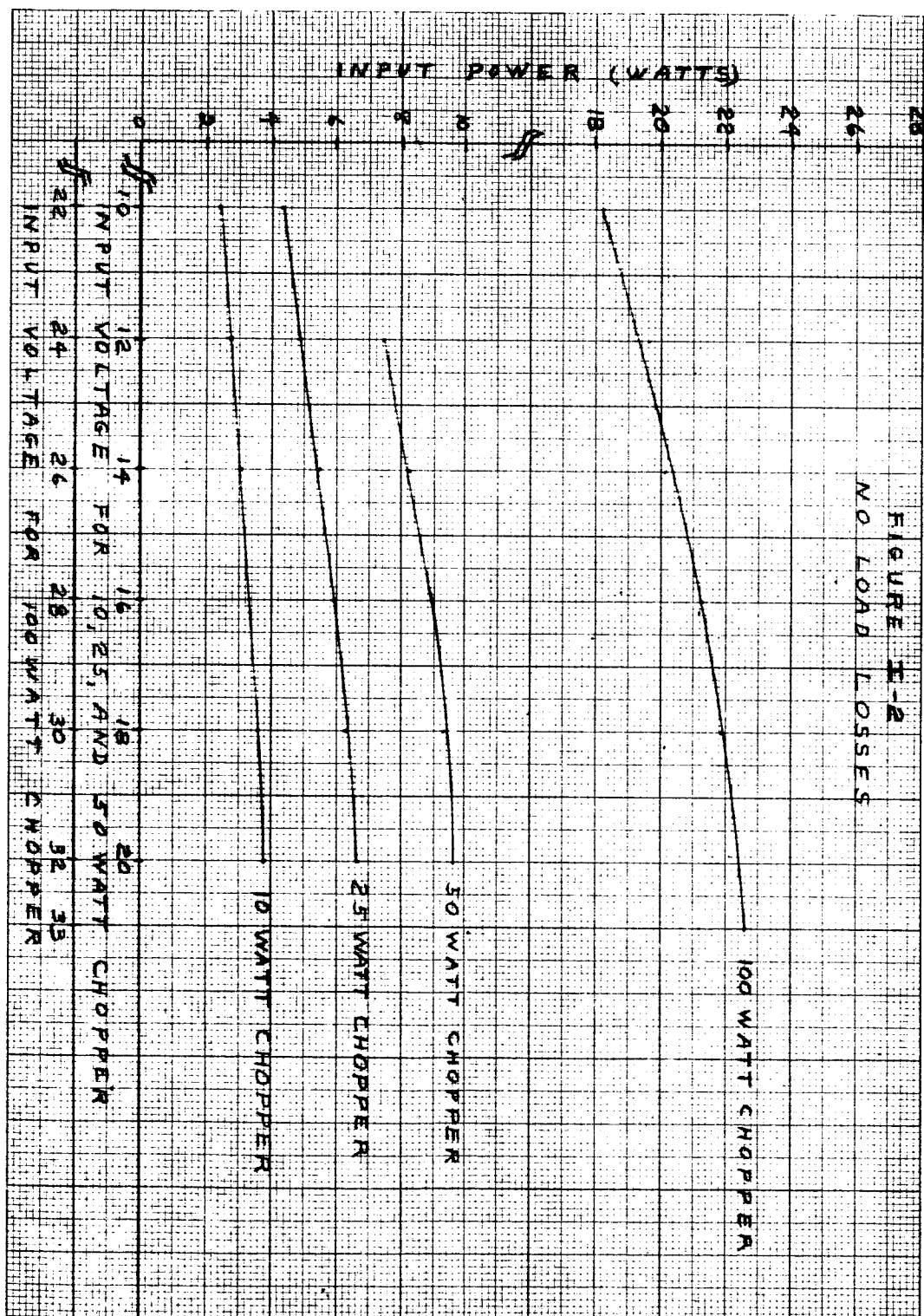
18

20

INPUT VOLTAGE (VOLTS-DC)

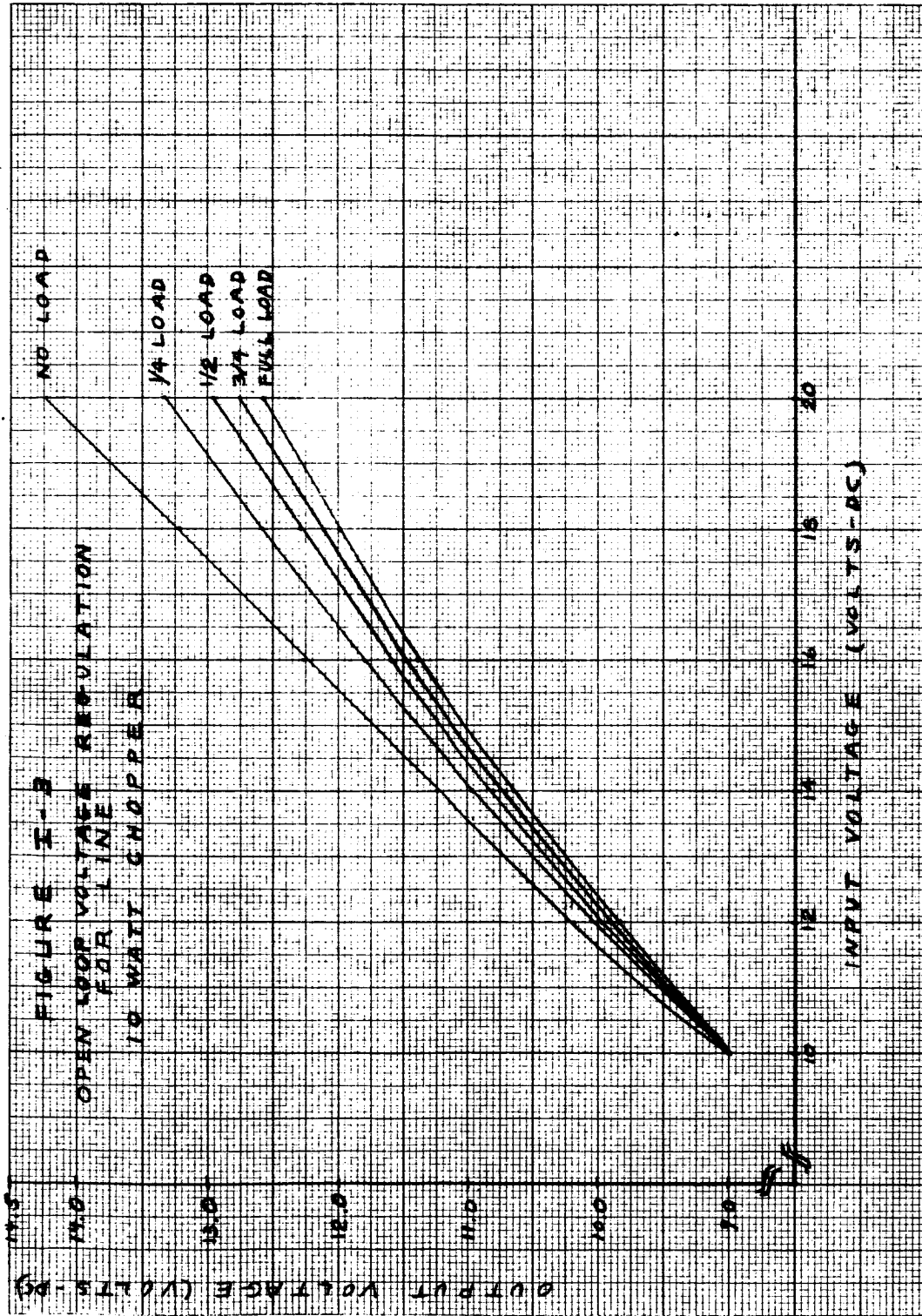
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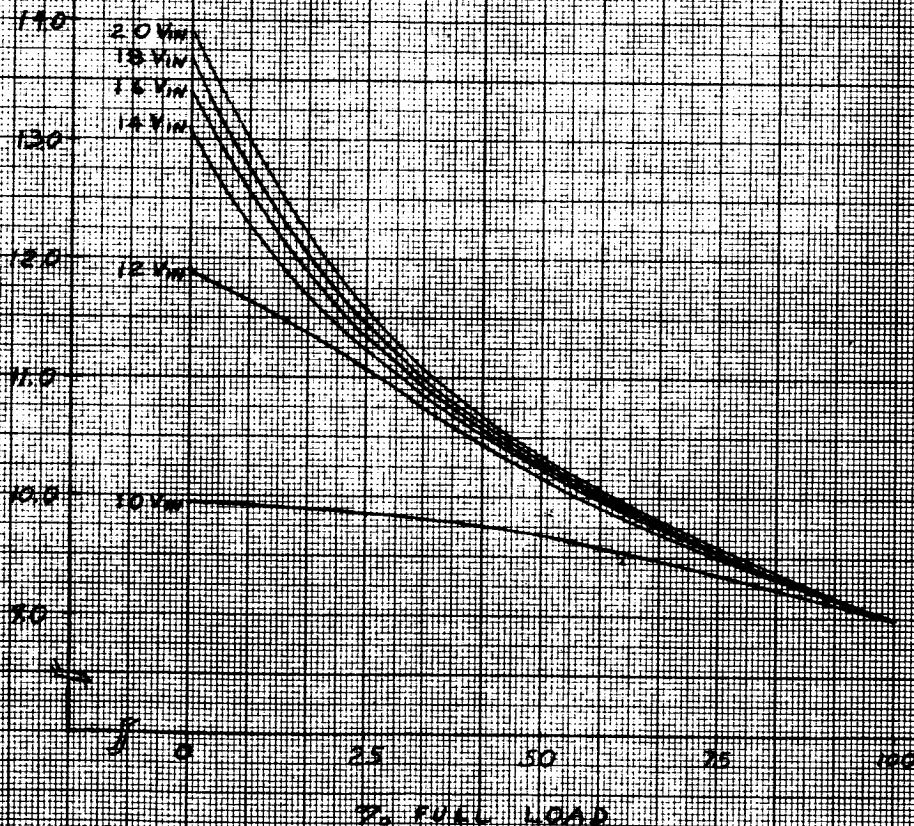


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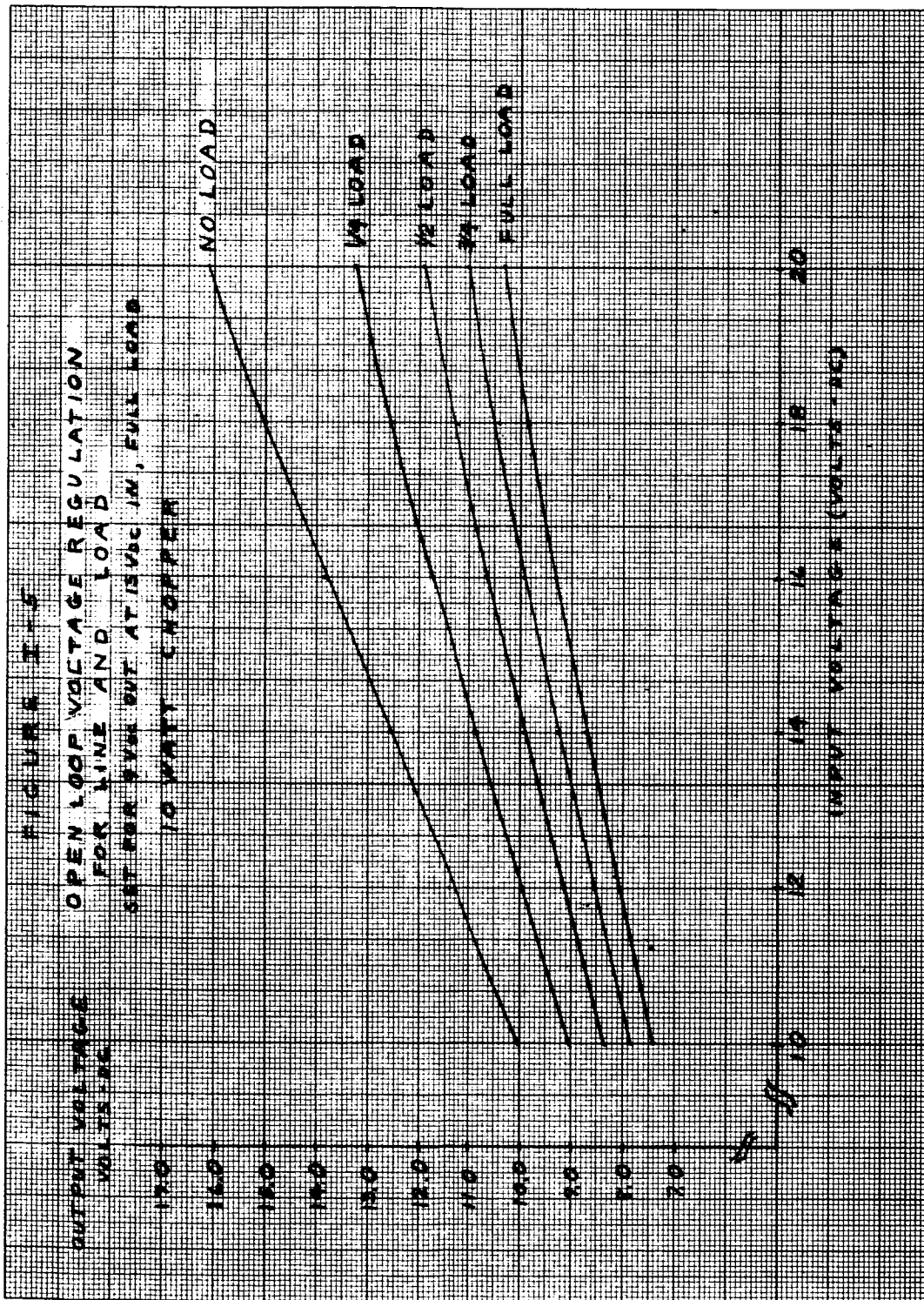
FIGURE I-4

OPEN LOOP VOLTAGE REGULATION
FOR LOAD
SET FOR 9V_{DC} OUTPUT AT FULL LOAD
FOR EACH INPUT VOLTAGE CONDITION
10 WATT CHOPPER

OUTPUT
VOLTAGE
VOLTS-DC



% FULL LOAD



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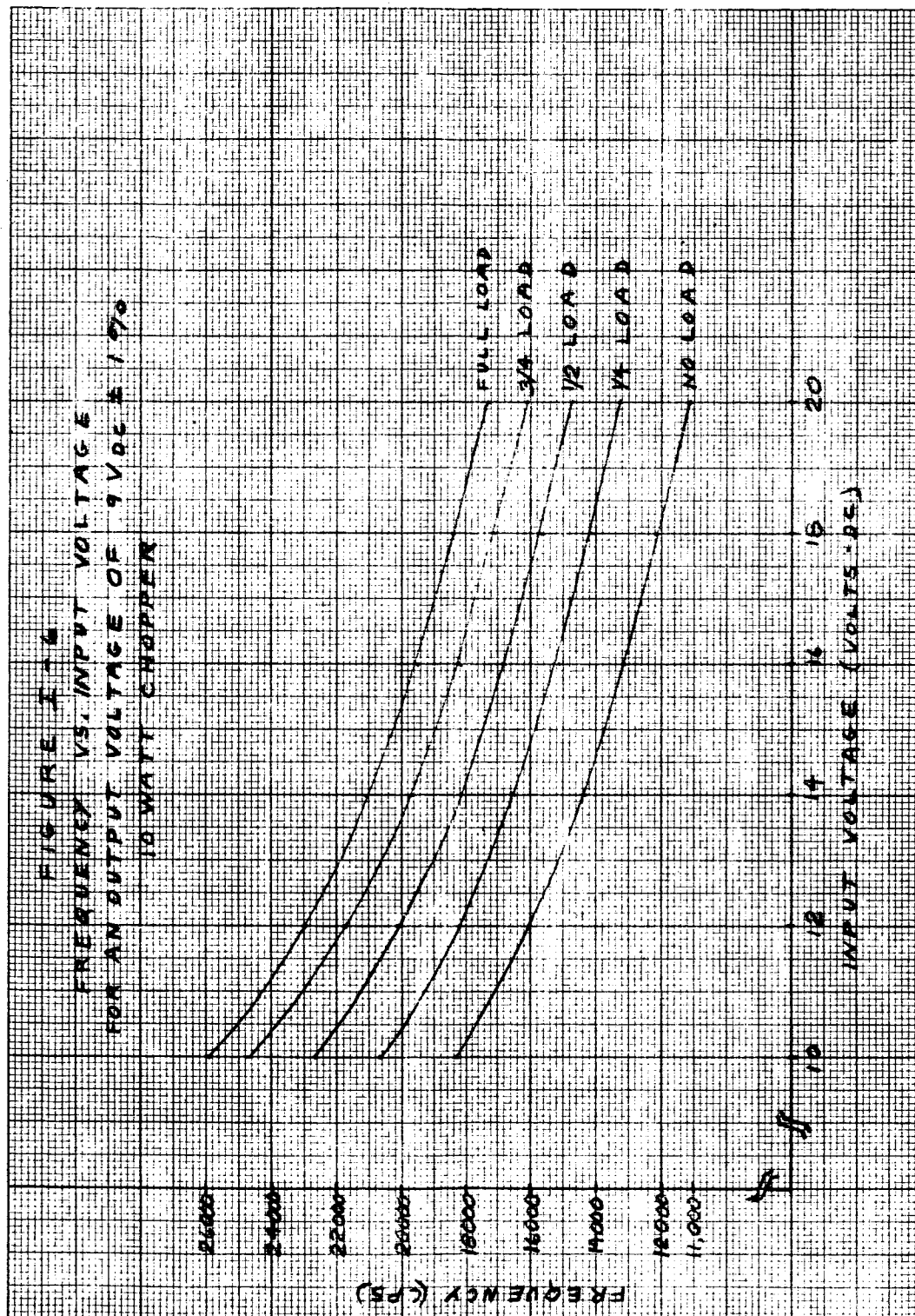
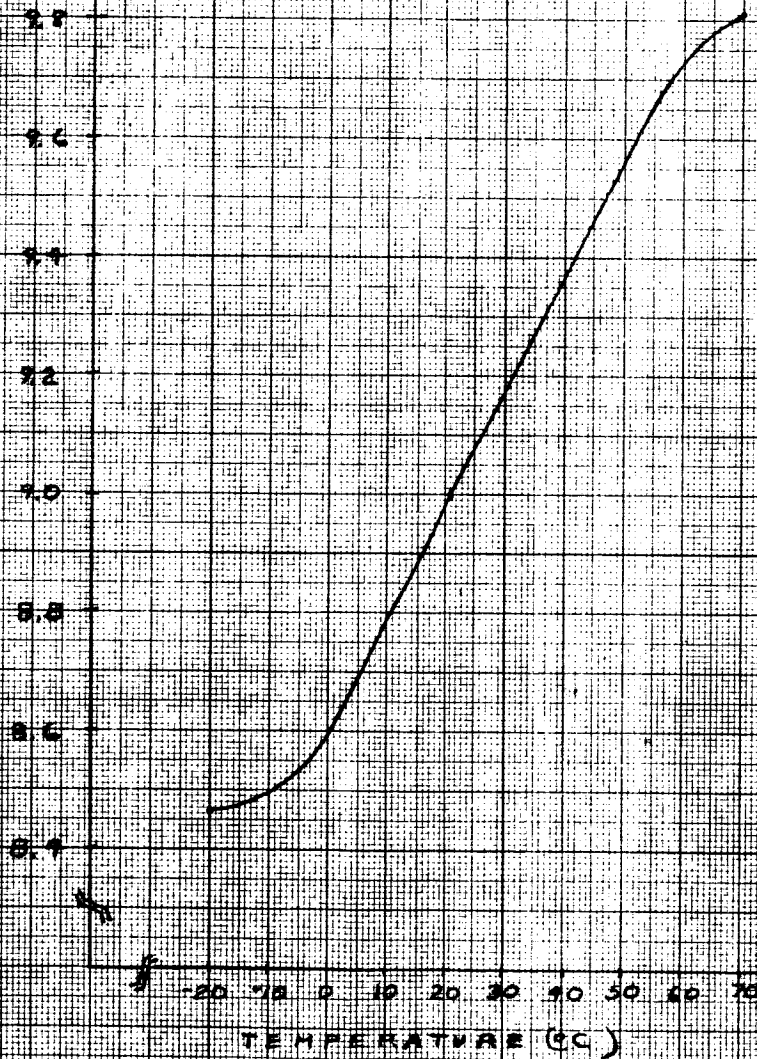


FIGURE I-7
 OPEN LOOP VOLTAGE REGULATION
 VS. TEMPERATURE
 10 WATT CHOPPER
 OUTPUT
 VOLTAGE
 (VOLTS-DC)
 10.0



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FIGURE I-8
OUTPUT VOLTAGE STABILITY
10 WATT CHOPPER

OUTPUT
VOLTAGE
(VOLTS-DC)

7.028

7.026

7.024

7.022

7.020

7.018

7.016

7.014

7.012

7.010

7.008

7.006

7.004

7.002

7.000

0 5 10 15 20 25 30 35 40 45

TIME (HOURS)

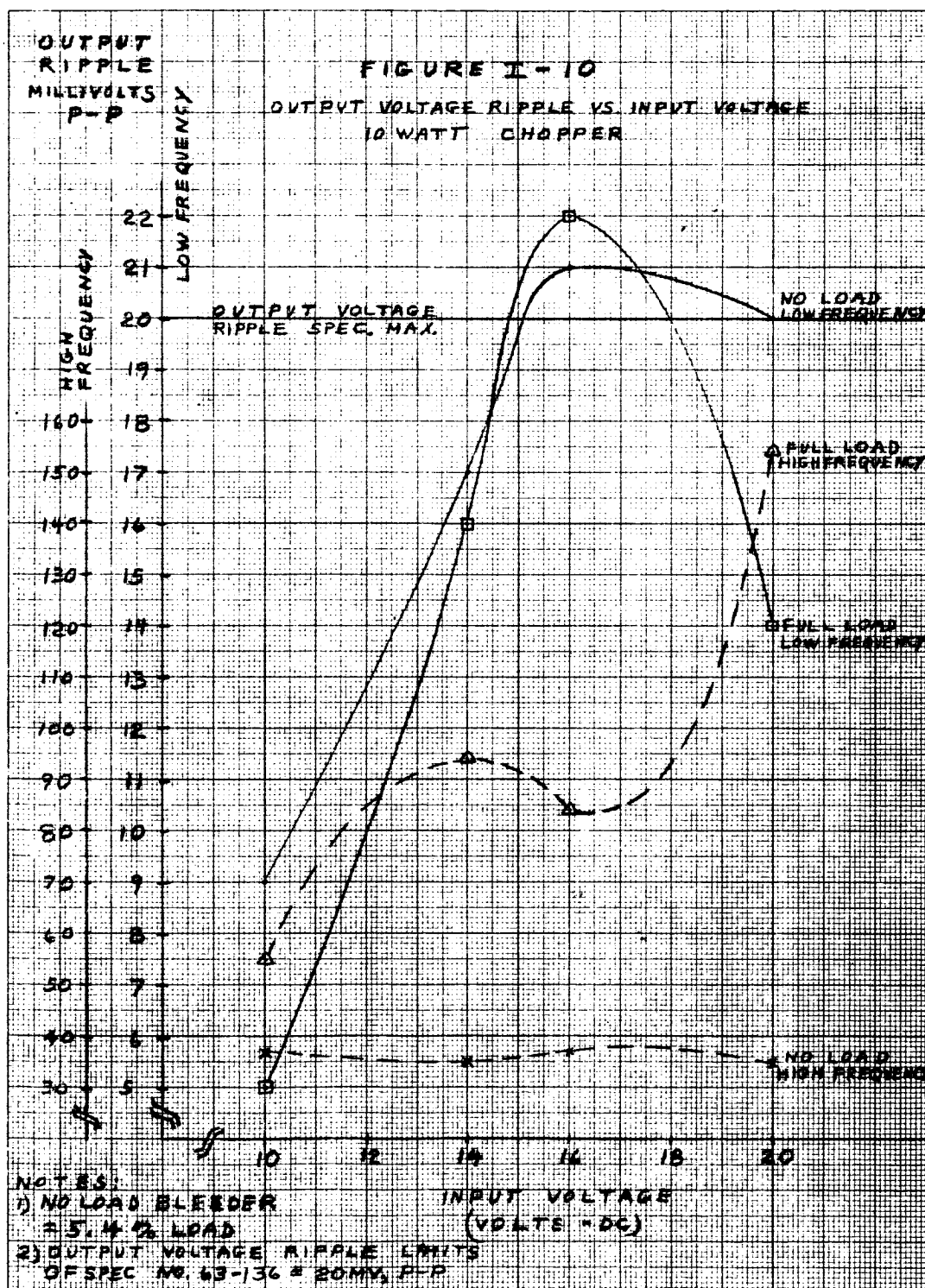
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FIGURE I - 9
OVERLOAD AND SHORT CIRCUIT
CHARACTERISTIC
10 WATT CHOPPER

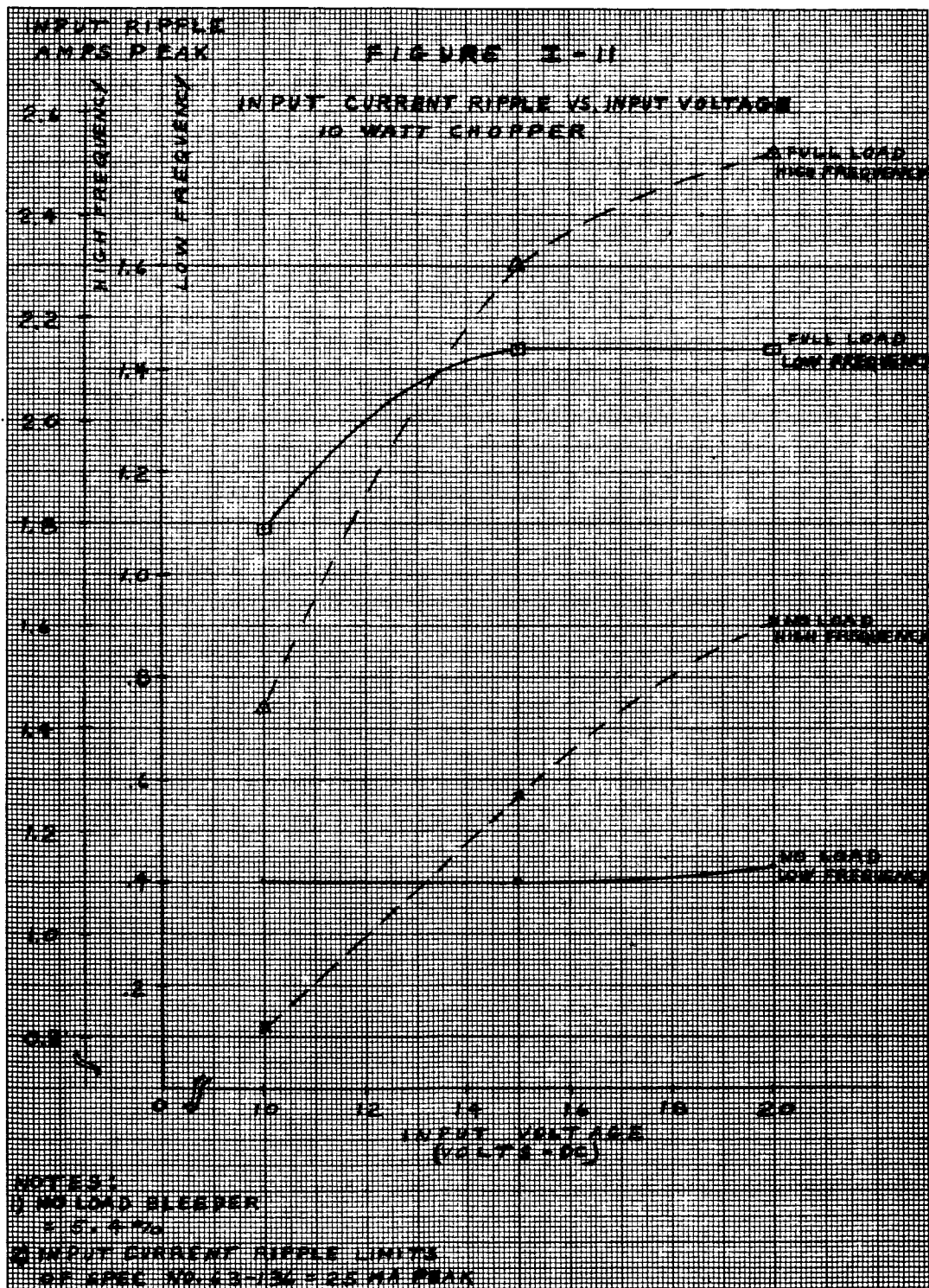


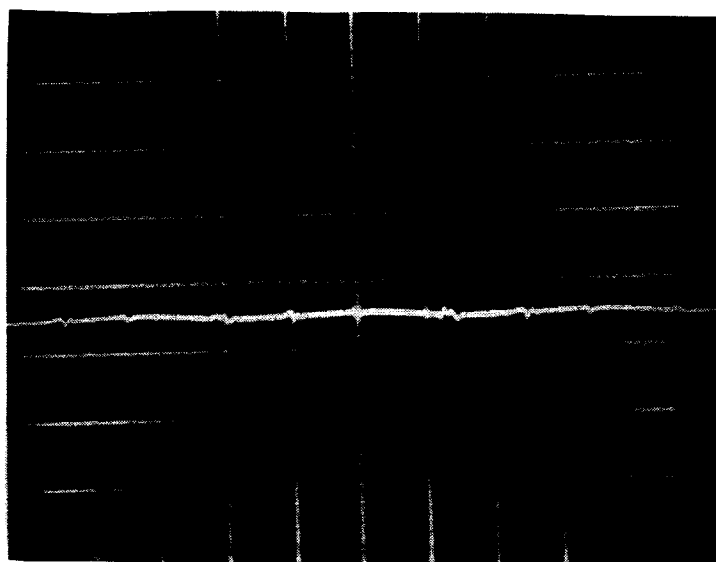
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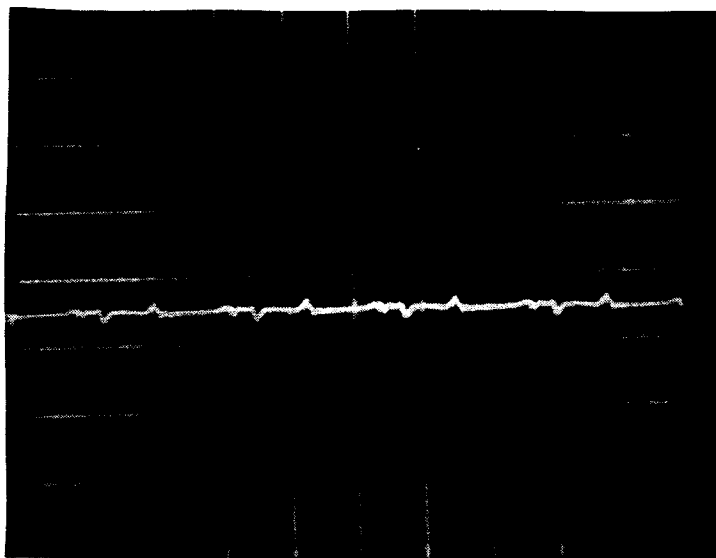
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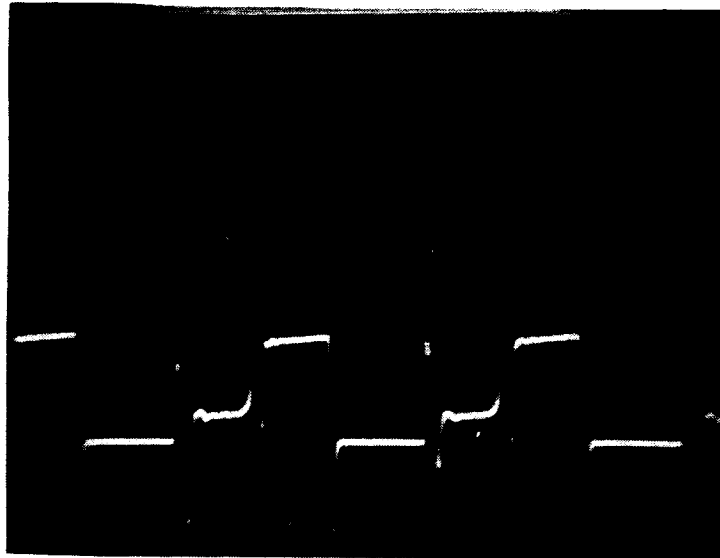


Output Ripple Voltage at No Load - 15 Volt Input
Vertical Scale - 0.1 Volt/CM
Horizontal Scale - 10 μ sec/CM

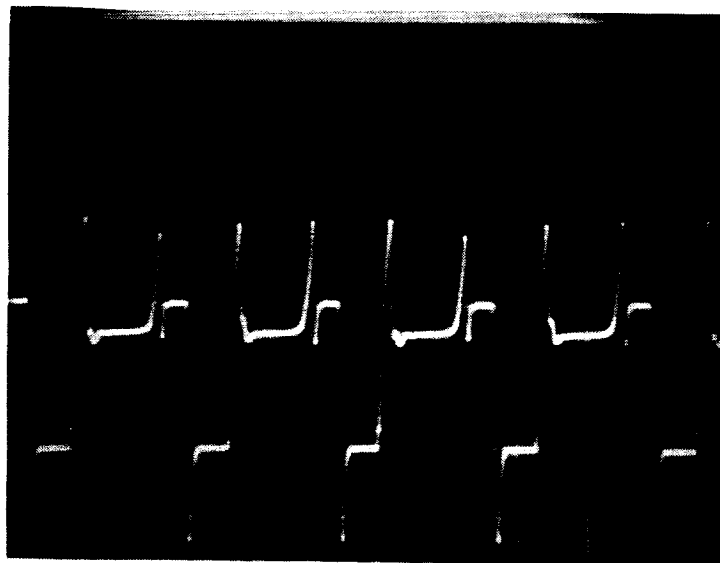


Output Ripple Voltage At Full Load - 15 Volt Input
Vertical Scale - 0.1 Volt/cm
Horizontal Scale - 10 μ sec/cm

Figure I-12 Output Ripple Voltage 10 Watt Chopper



Input Ripple Current At No Load - 15 Volt Input
 Vertical Scale - 0.288 Amps/cm
 Horizontal Scale - 10 μ sec/cm



Input Ripple Current At Full Load - 15 Volt Input
 Vertical Scale - 0.720 Amps/cm
 Horizontal Scale - 10 μ sec/cm

Figure I-13 Input Ripple Current 10 Watt Chopper

FIGURE I-14
EFFICIENCY VS. INPUT VOLTAGE
2.5 WATT CHOPPER

EFFICIENCY
%

100

90

80

70

60

50

50

10

12

14

16

18

20

INPUT VOLTAGE (VOLTS-DC)

FULL
LOAD

3/4
LOAD

1/2
LOAD

1/4
LOAD

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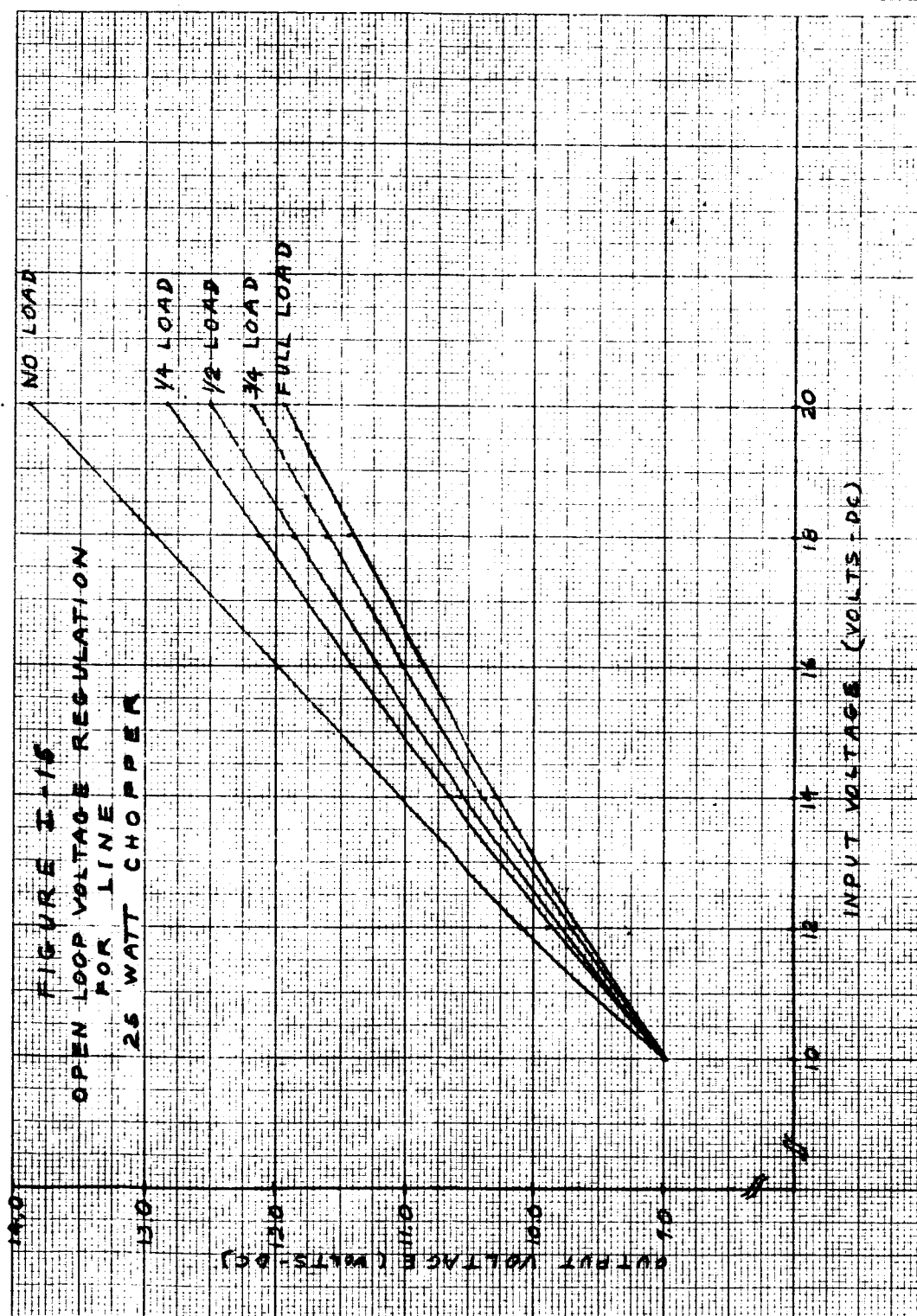
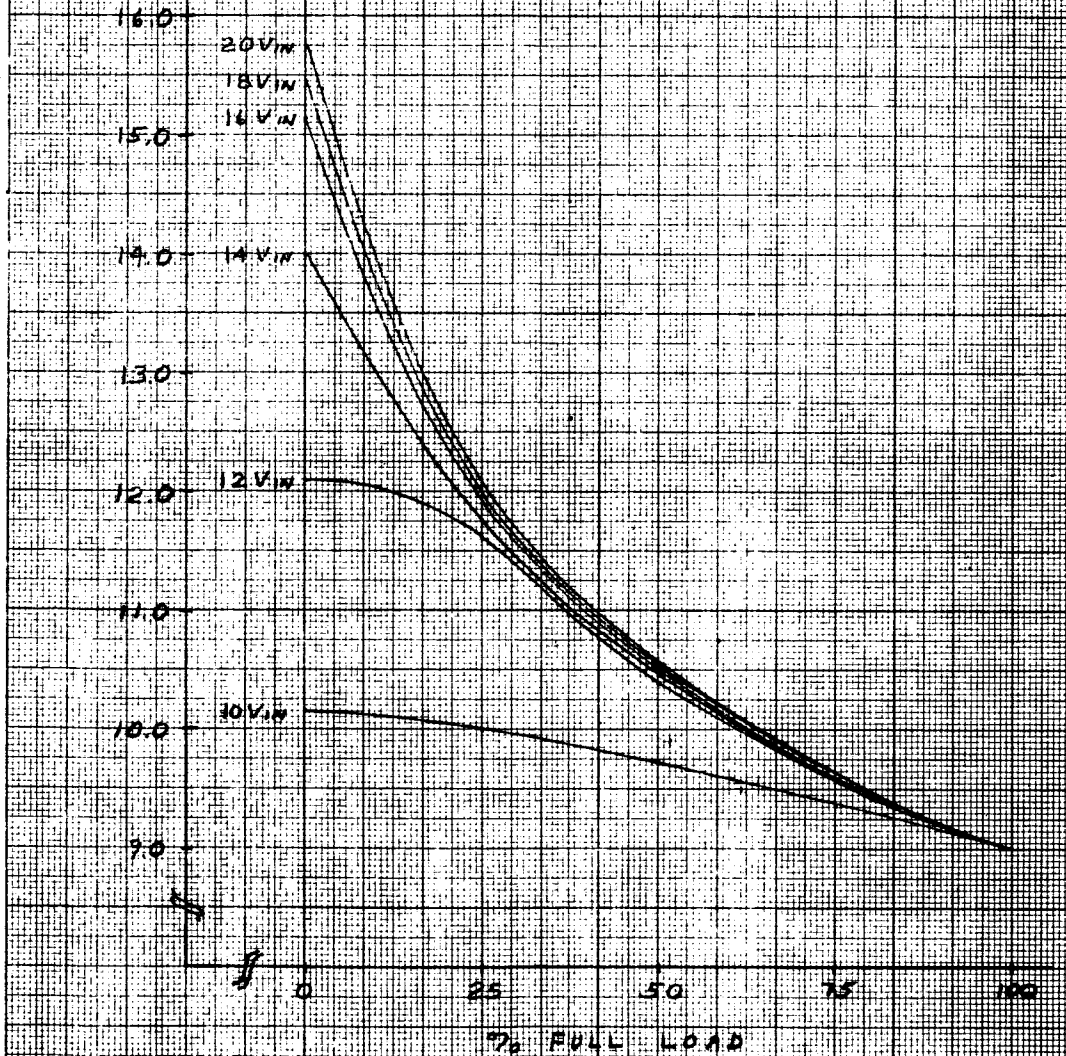


FIGURE I-16

OPEN LOOP VOLTAGE REGULATION
FOR LOAD
SET FOR 9V_{DC} OUTPUT AT FULL LOAD
FOR EACH INPUT VOLTAGE CONDITION
25 WATT CHOPPER



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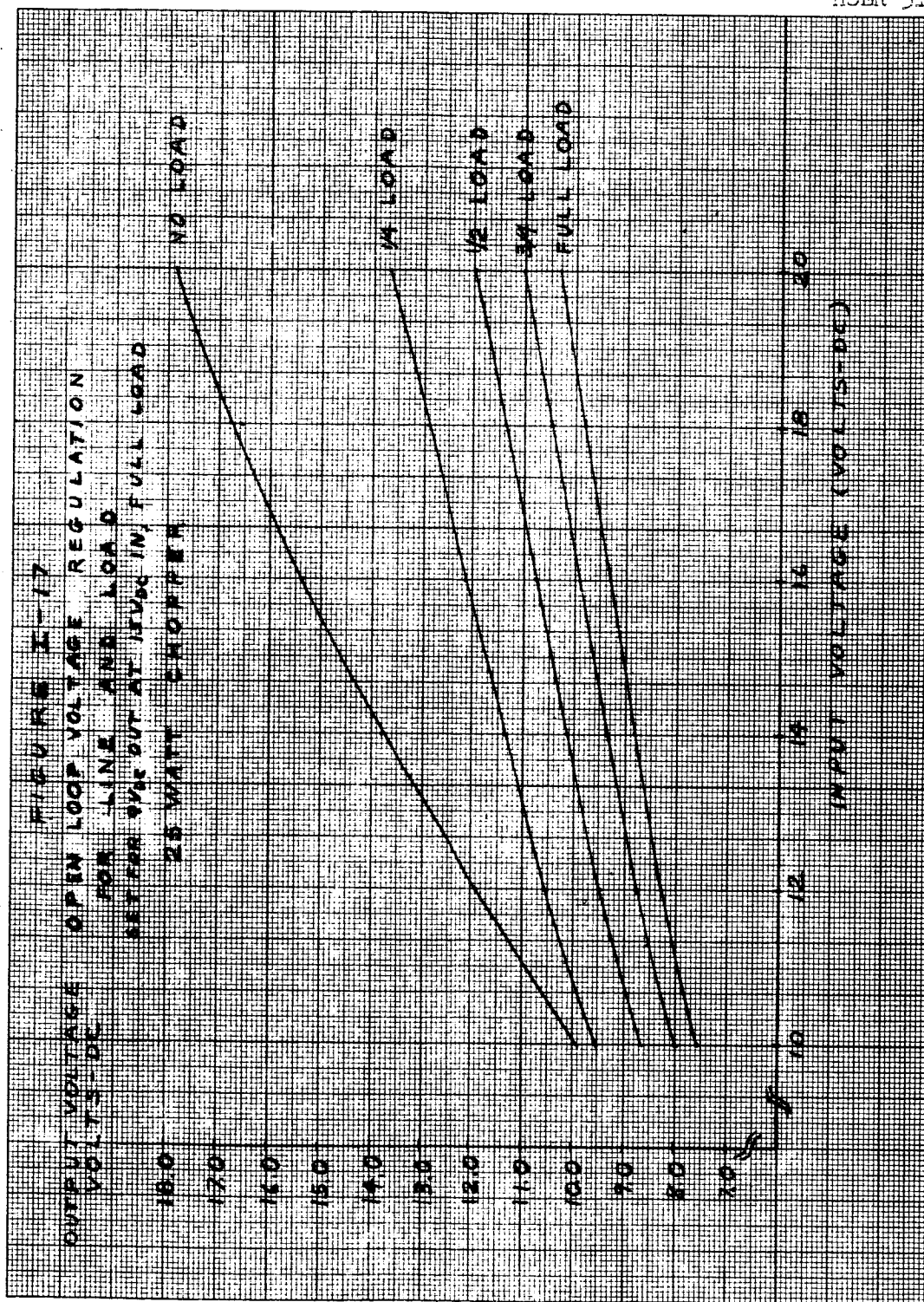
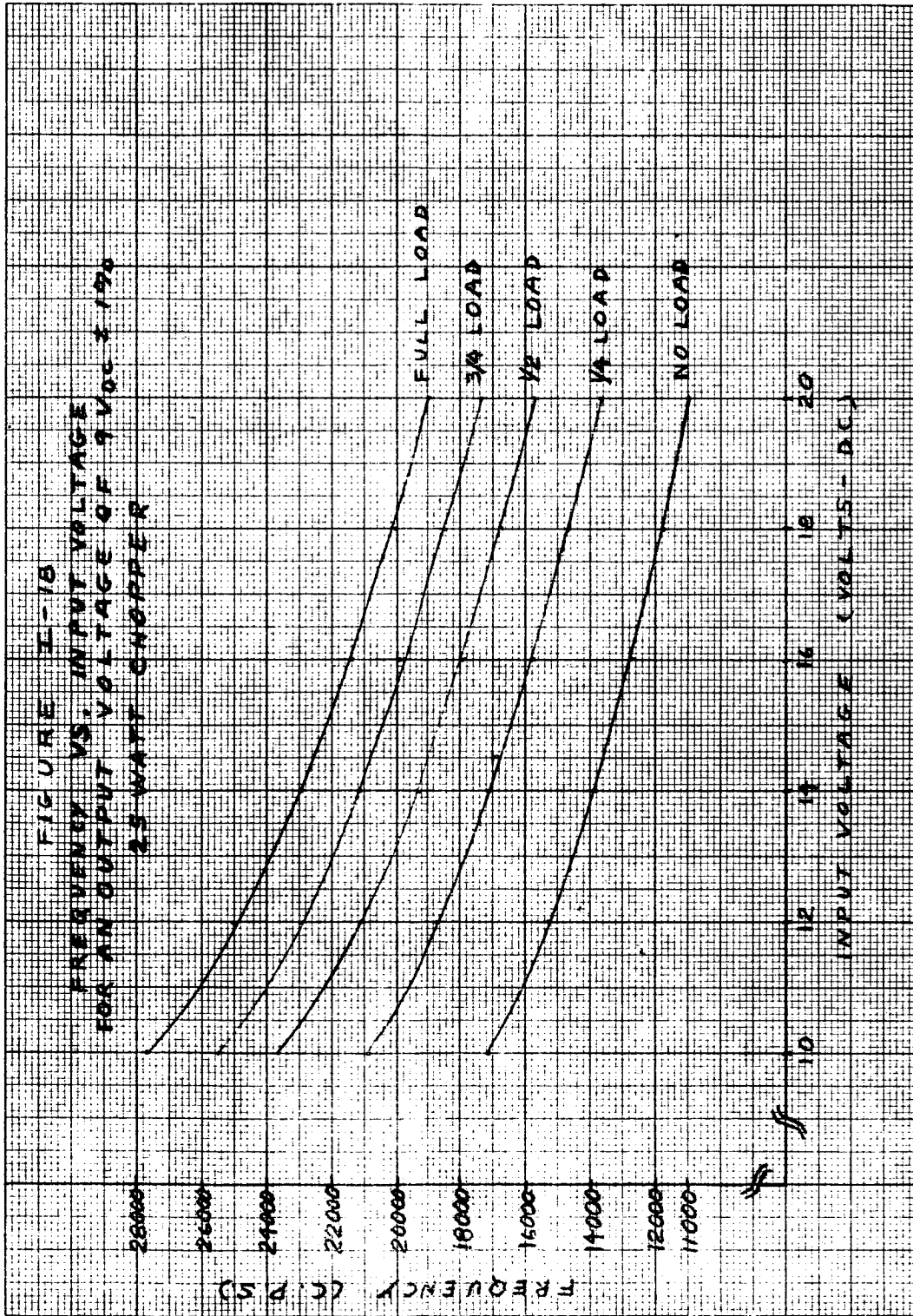


FIGURE 1-18
FREQUENCY VS. INPUT VOLTAGE
FOR AN OUTPUT VOLTAGE OF 9V_{DC} ± 1%
25 WATT CHOPPER



OUTPUT
VOLTAGE
(VOLTS -DC)

FIGURE I-19

OPEN LOOP VOLTAGE REGULATION
VS. TEMPERATURE

2.5 WATT CHOPPER

9.35

9.3

9.2

9.1

9.0

8.9

8.8

8.7

8.6

8.5

-20 -10 0 10 20 30 40 50 60 70

TEMPERATURE (°C)

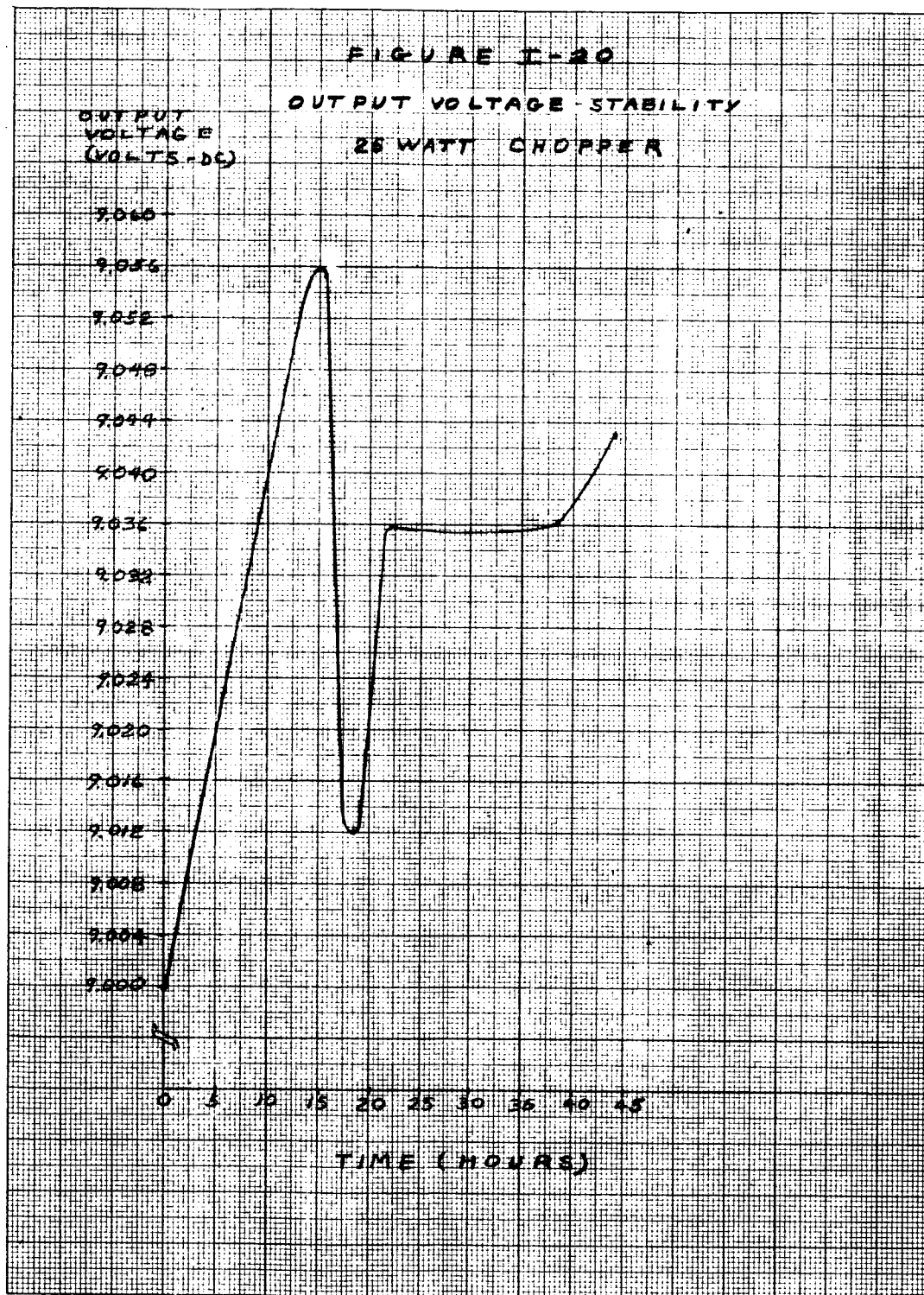
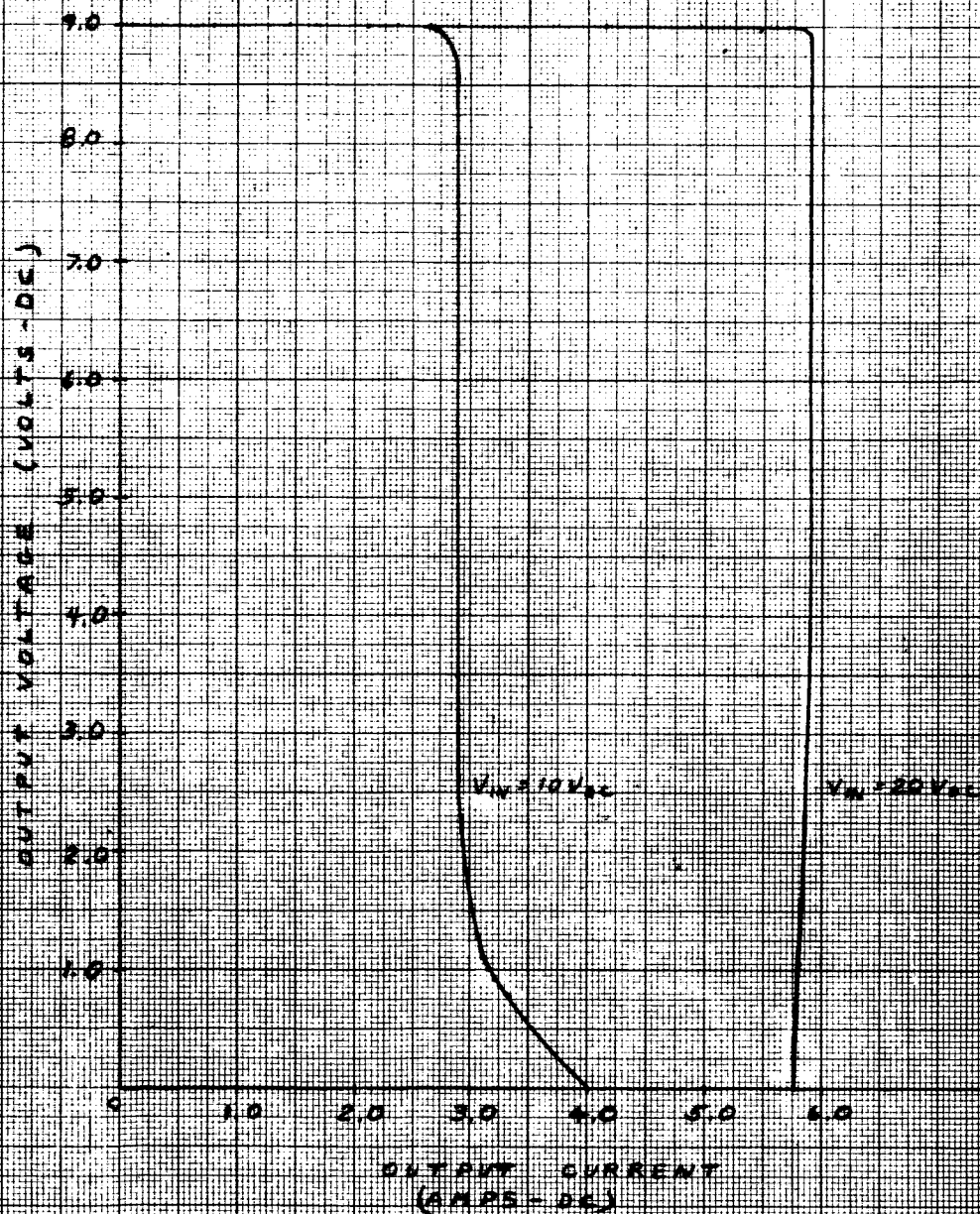
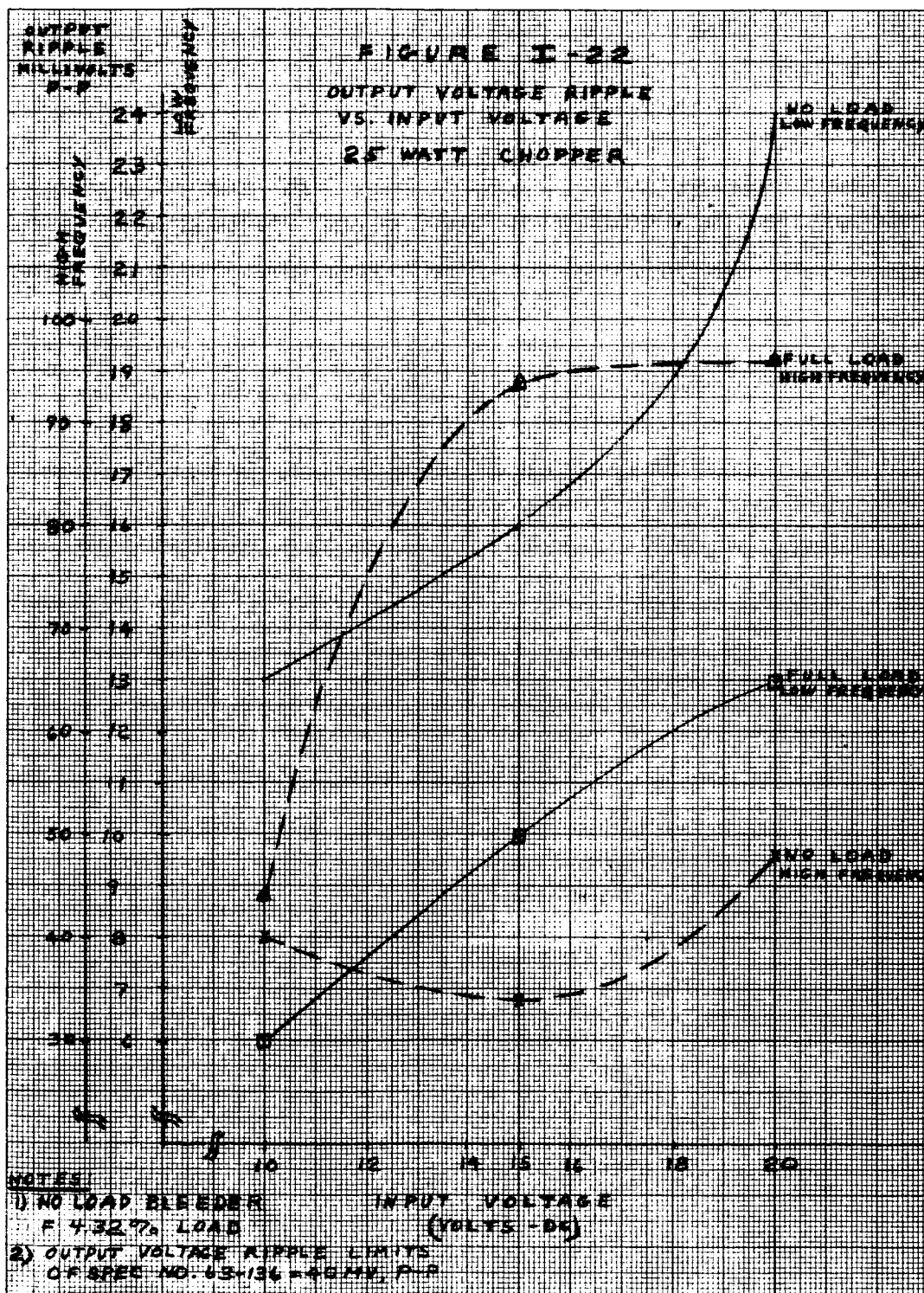
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FIGURE I-21
OVERLOAD AND SHORT CIRCUIT
CHARACTERISTIC
25 WATT CHOPPER



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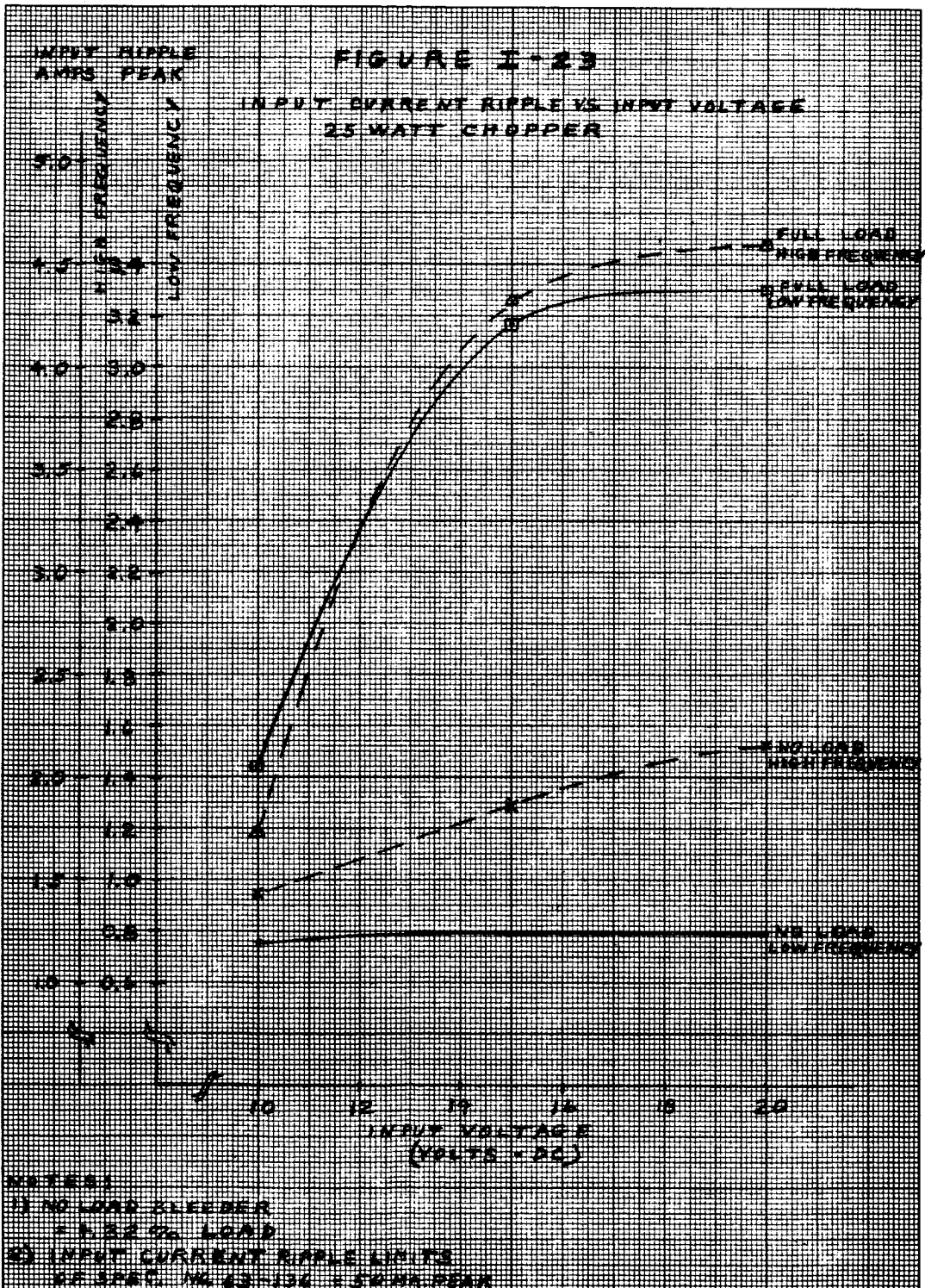
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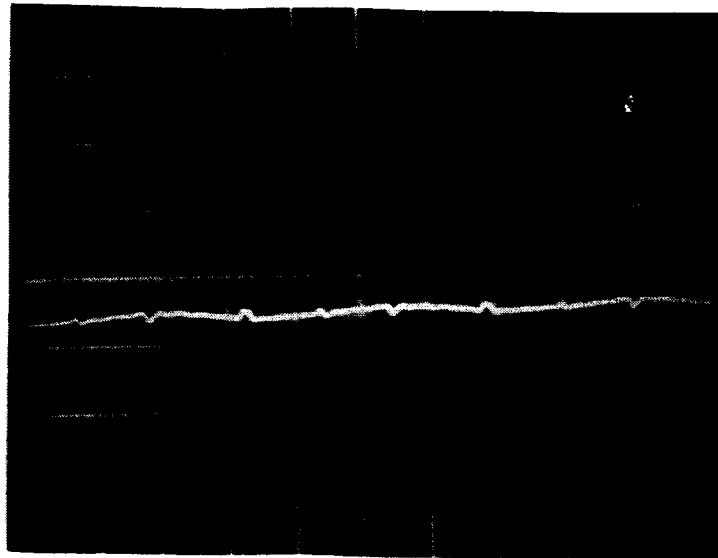
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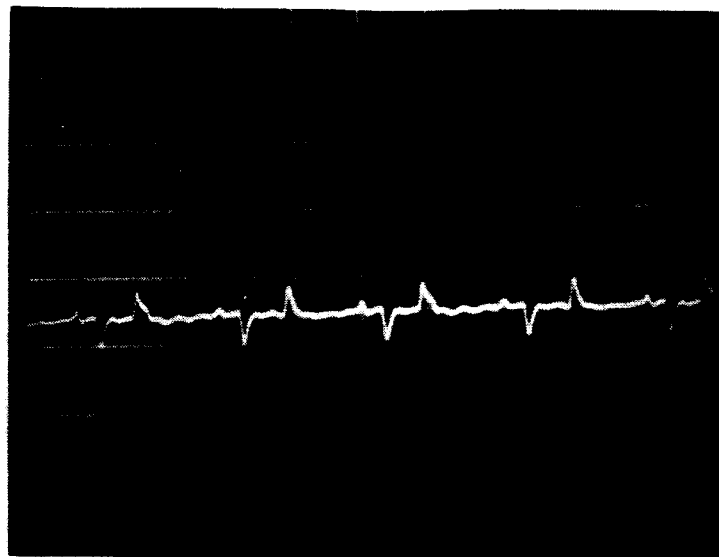
FIGURE I-23

INPUT CURRENT RIPPLE VS INPUT VOLTAGE
25 WATT CHOPPER



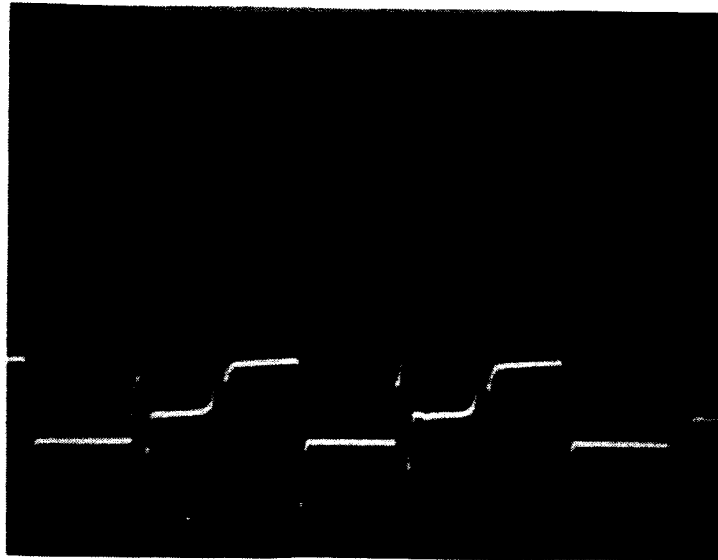


Output Ripple Voltage At No Load - 15 Volt Input
 Vertical Scale - 0.1 Volt/cm
 Horizontal Scale - 10 μ sec/cm

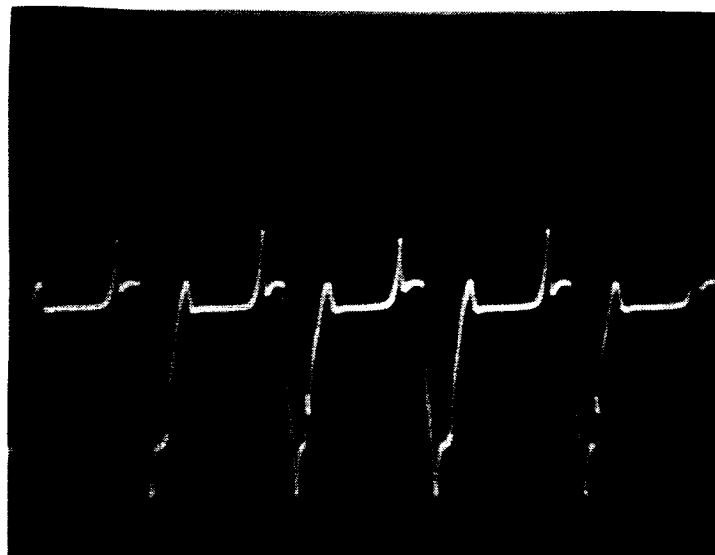


Output Ripple Voltage At Full Load - 15 Volt Input
 Vertical Scale - 0.1 Volt/cm
 Horizontal Scale - 10 μ sec/cm

Figure I-24 Output Ripple Voltage 25 Watt Chopper



Input Ripple Current At No Load - 15 Volt Input
 Vertical Scale - 0.720 Amps/cm
 Horizontal Scale - 10 μ sec/cm



Input Ripple Current At Full Load - 15 Volt Input
 Vertical Scale - 1.44 Amps/cm
 Horizontal Scale - 10 μ sec/cm

Figure I-25 Input Current Ripple 25 Watt Chopper

FIGURE I-26
EFFICIENCY VS INPUT VOLTAGE
50 WATT CHOPPER

EFFICIENCY
%

100

90

80

70

60

50

FULL LOAD

3/4 LOAD

1/2 LOAD

1/4 LOAD

INPUT VOLTAGE (VOLTS-DC)

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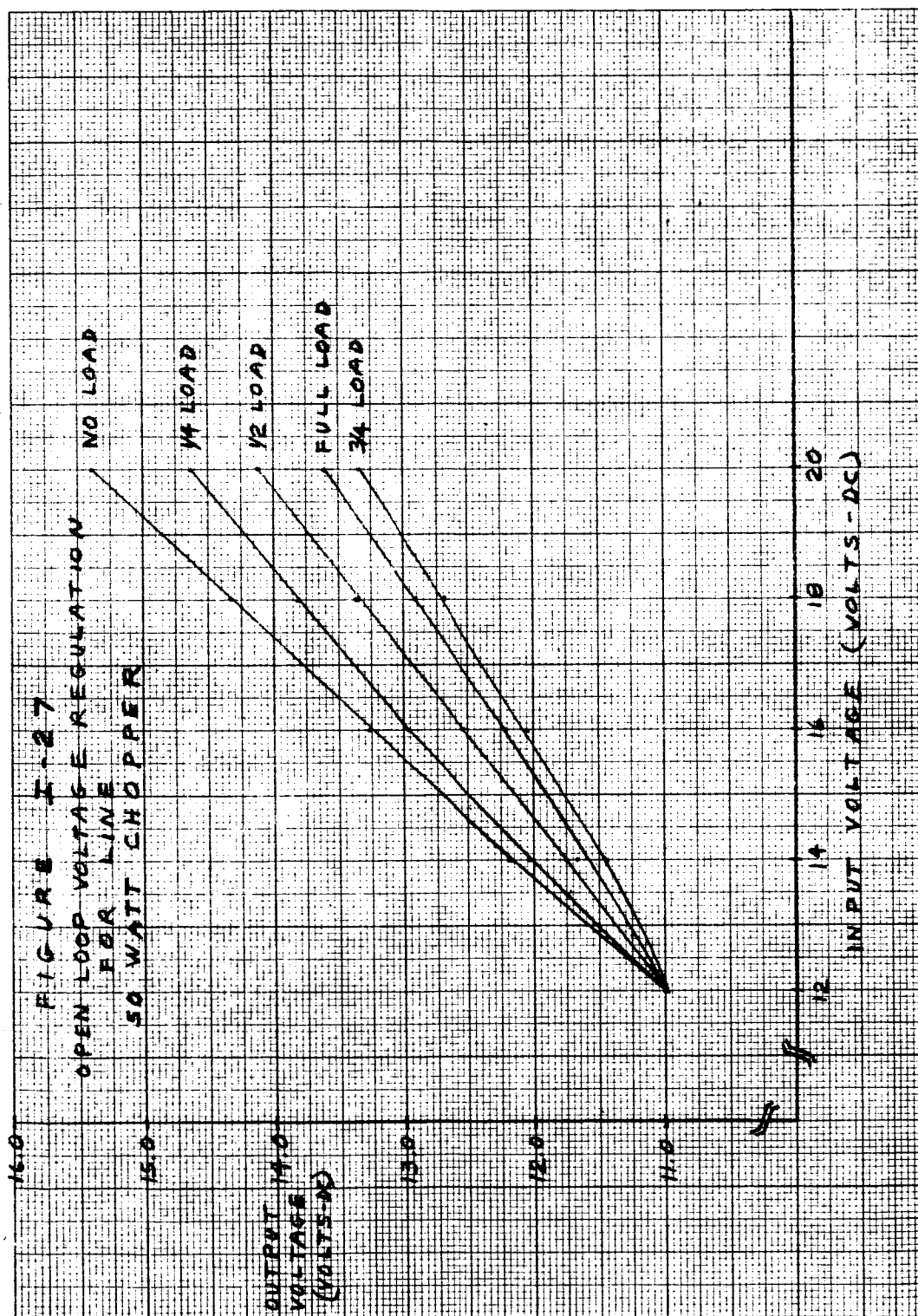


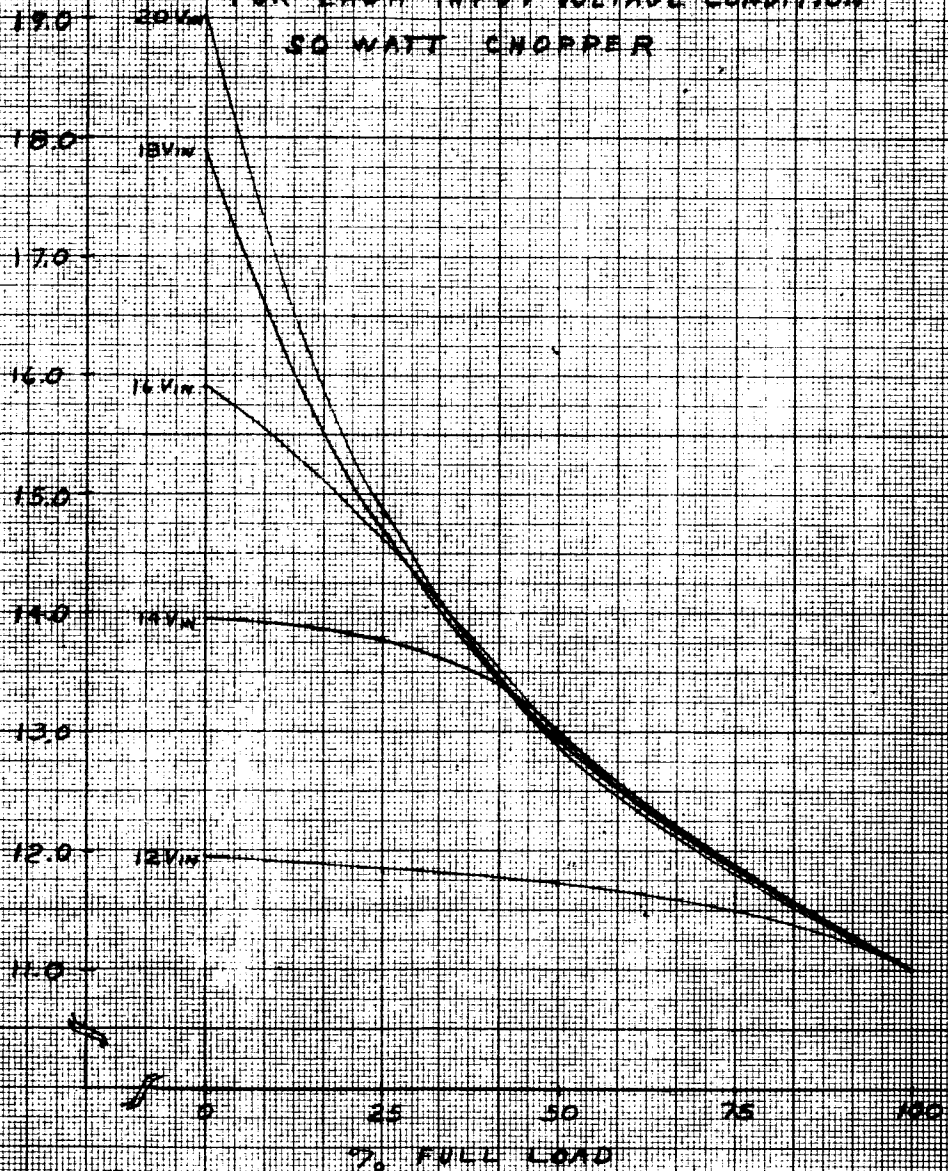
FIGURE I-25

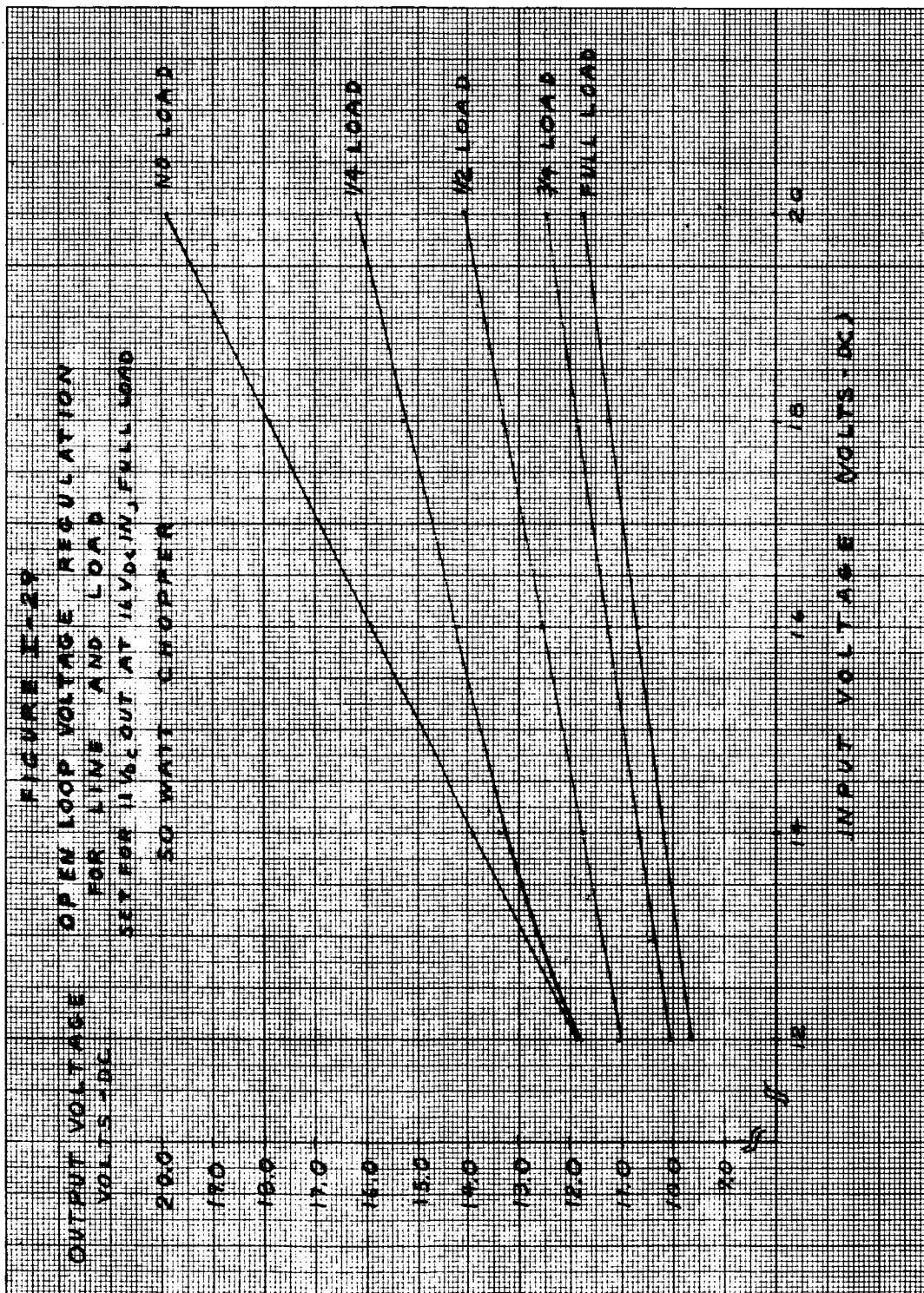
OUTPUT
VOLTAGE
(VOLTS-DC)

OPEN LOOP VOLTAGE REGULATION
FOR LOAD

SET FOR 11V_{DC} OUTPUT AT FULL LOAD
FOR EACH INPUT VOLTAGE CONDITION

50 WATT CHOPPER





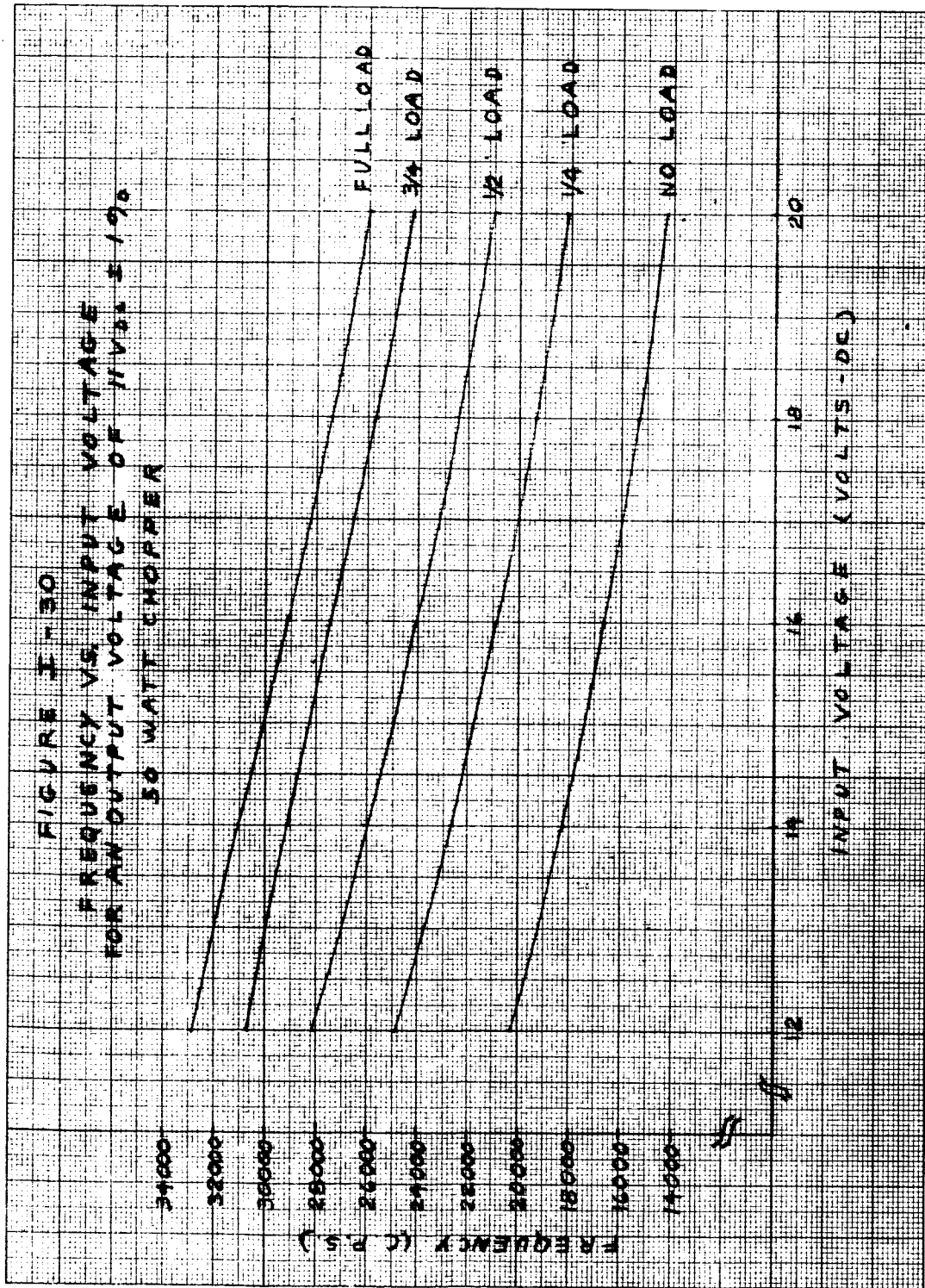
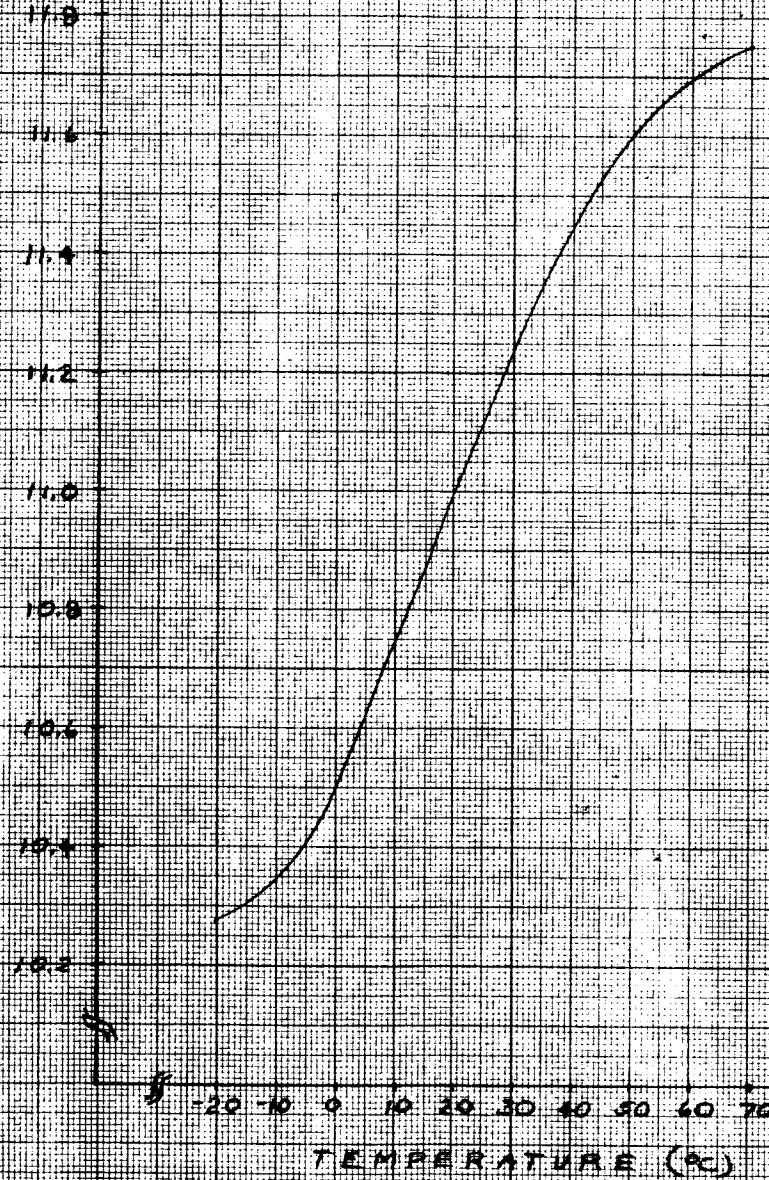


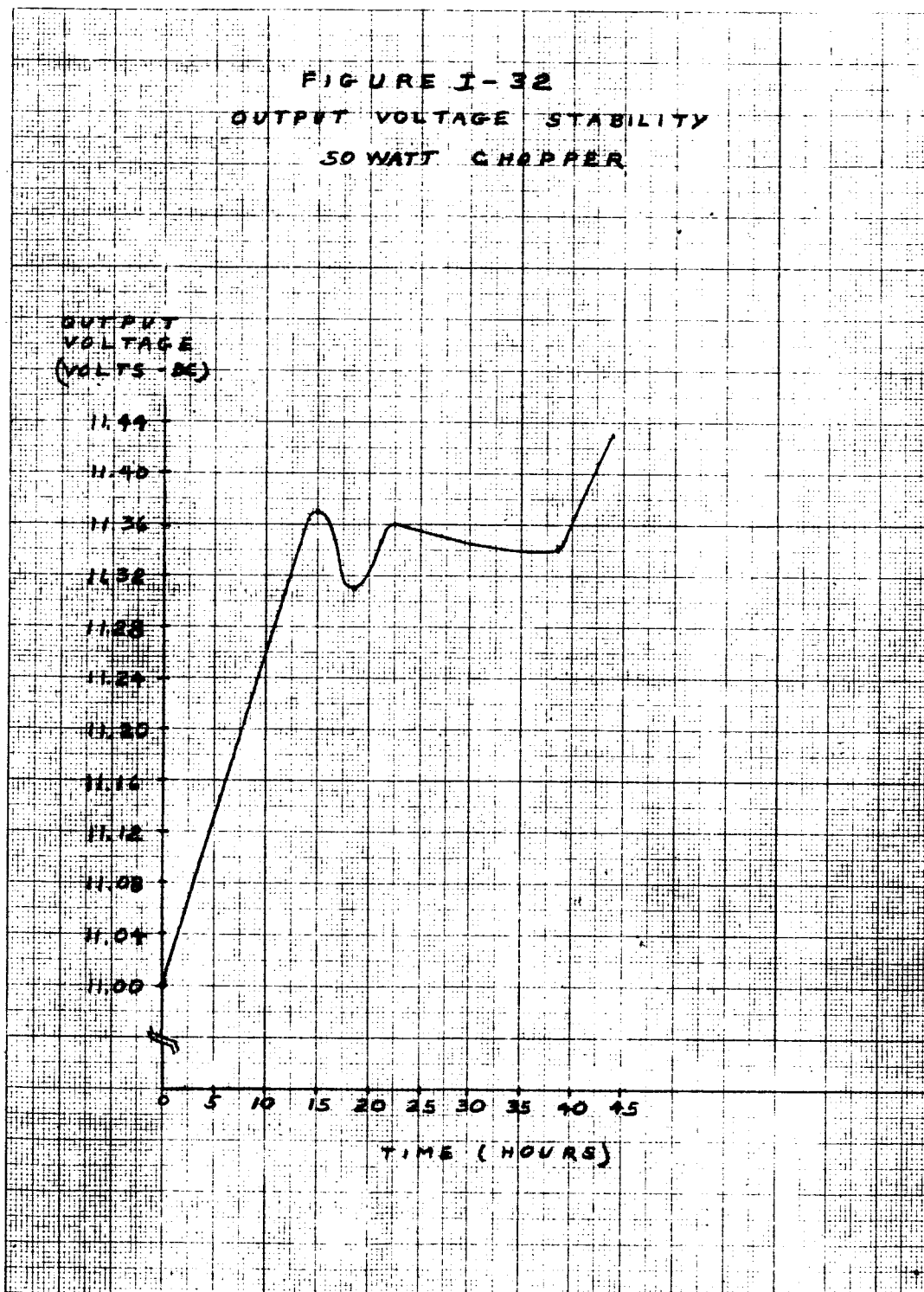
FIGURE I-31
OPEN LOOP VOLTAGE REGULATION
VS. TEMPERATURE
50 WATT CHOPPER
OUTPUT
VOLTAGE
(VOLTS -DC)



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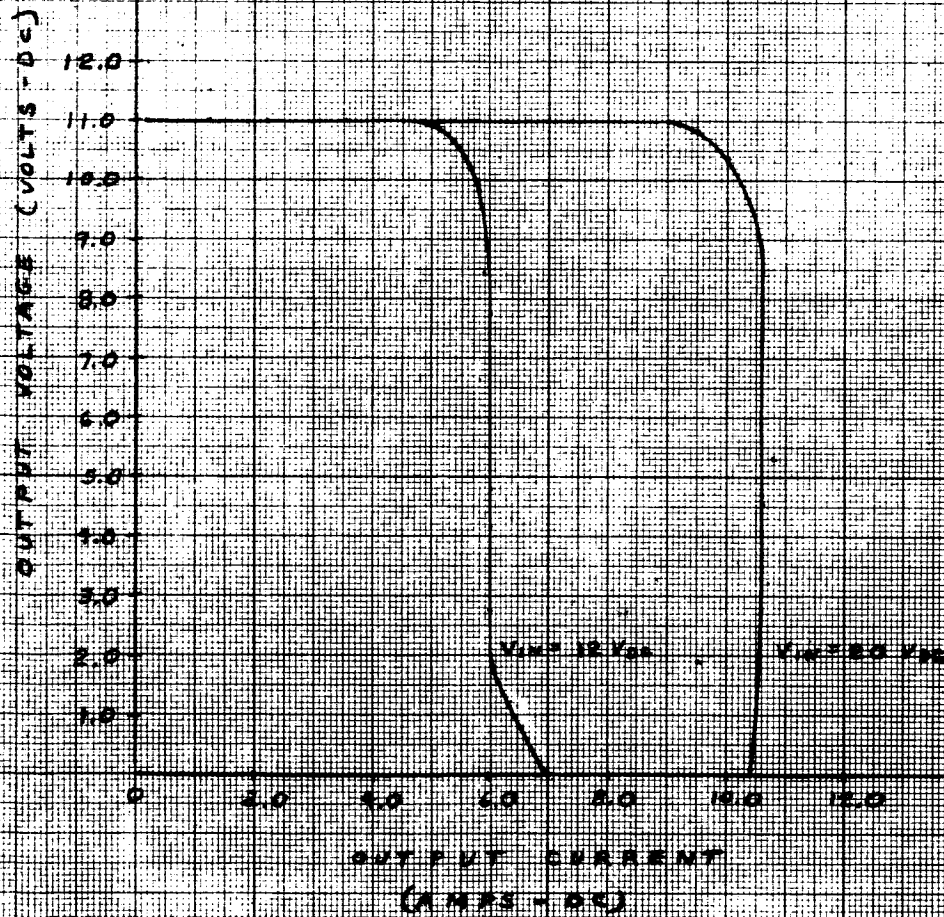
FIGURE I-32
OUTPUT VOLTAGE STABILITY
50 WATT CHOPPER



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FIGURE I-35
OVERLOAD AND SHORT CIRCUIT
CHARACTERISTIC
50 WATT CHOPPER



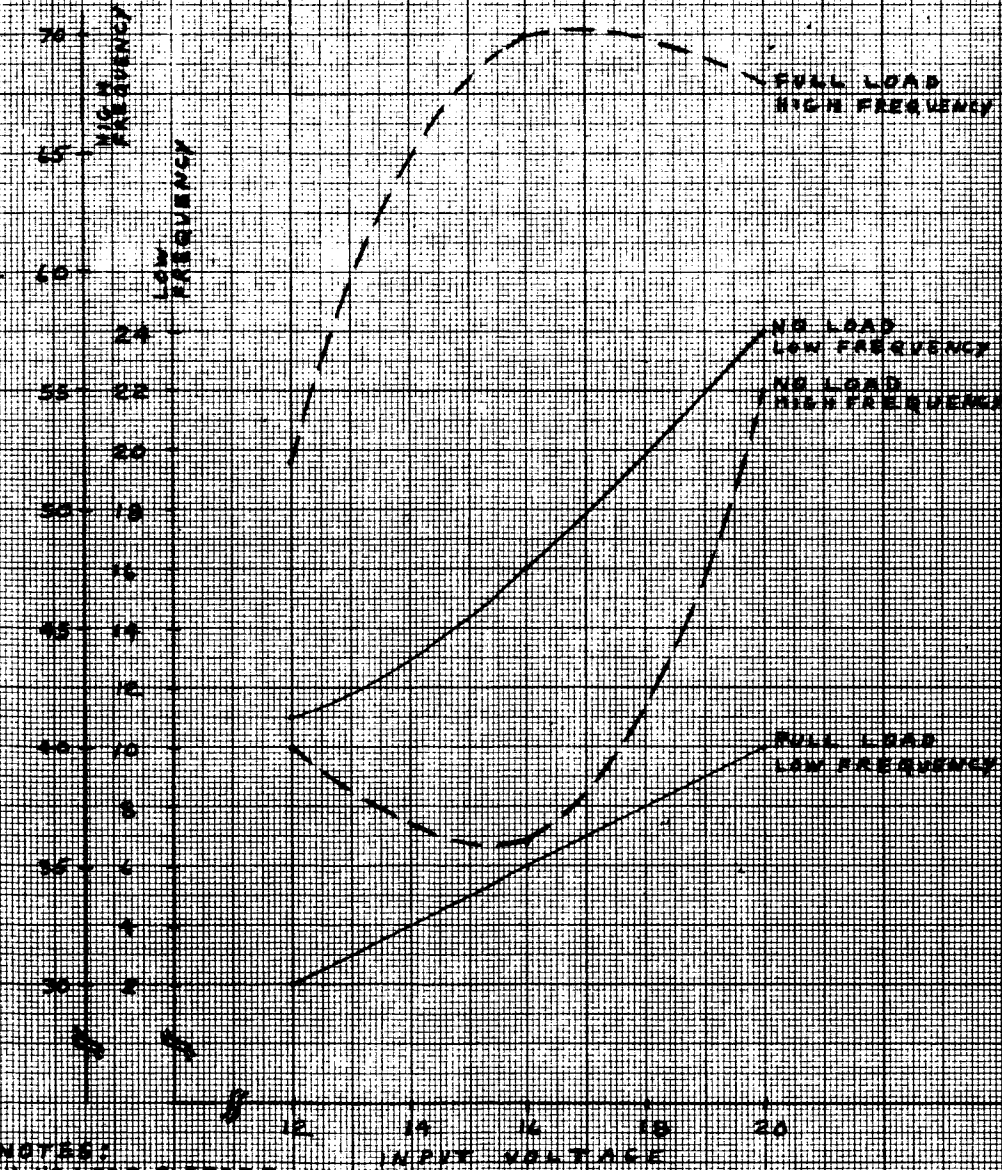
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FIGURE I-34

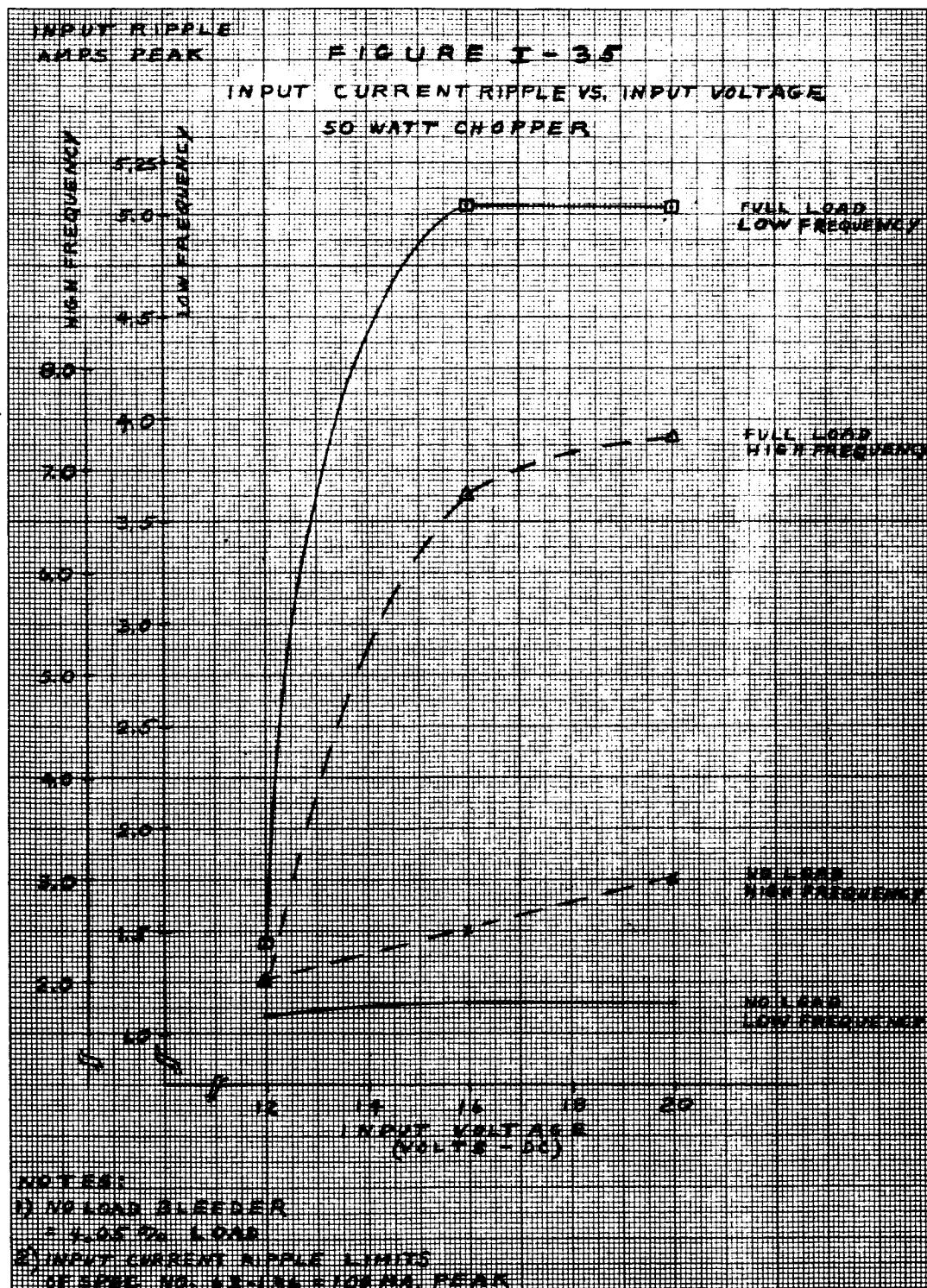
OUTPUT VOLTAGE RIPPLE
VS. INPUT VOLTAGE
50 WATT CHOPPER

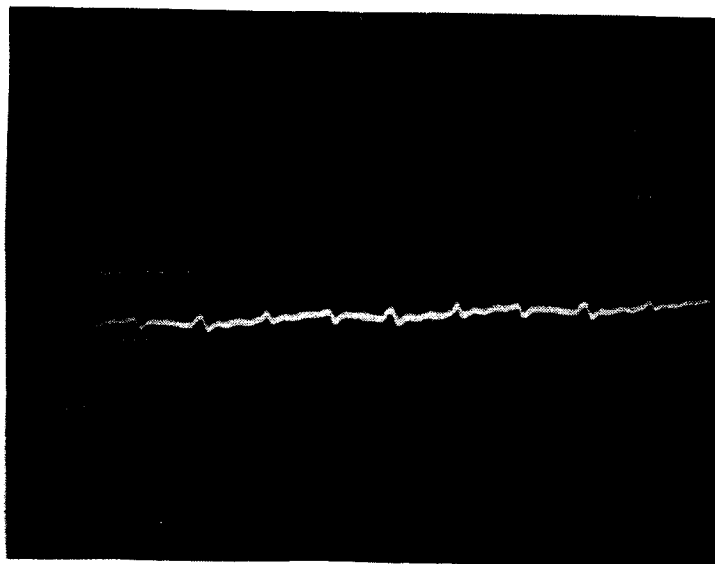
OUTPUT
RIPPLE
MILLIVOLTS
P-P



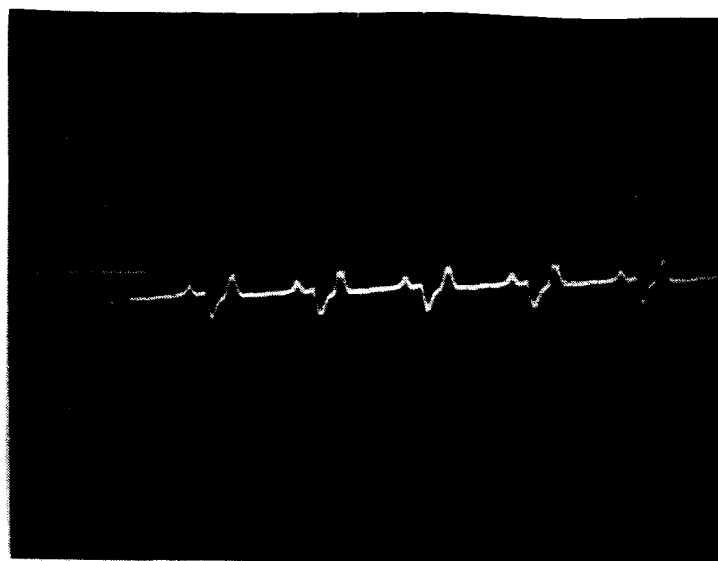
NOTES:

- 1) NO LOAD BLEEDER
= 0.05% LOAD
- 2) OUTPUT VOLTAGE RIPPLE LIMITS
OF SPEC NO. 63-136 = 60 MV P-P

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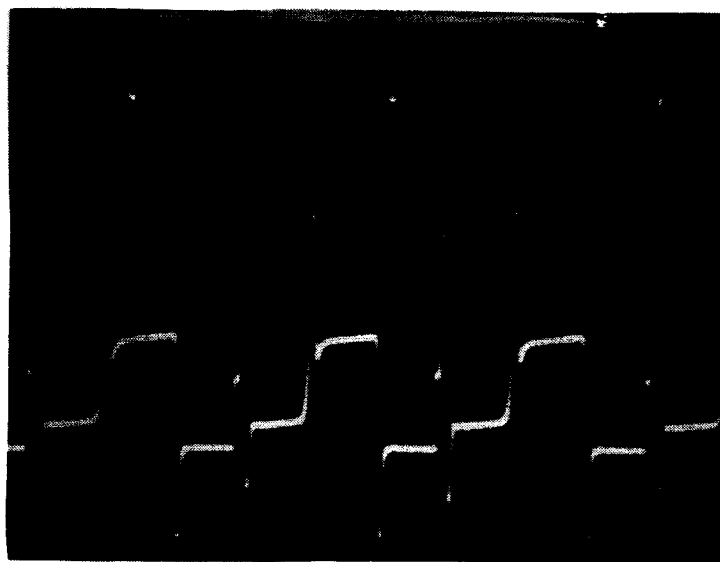


Output Ripple Voltage At No Load - 16 Volt Input
Vertical Scale - .1 Volt/cm
Horizontal Scale - 10 μ sec/cm

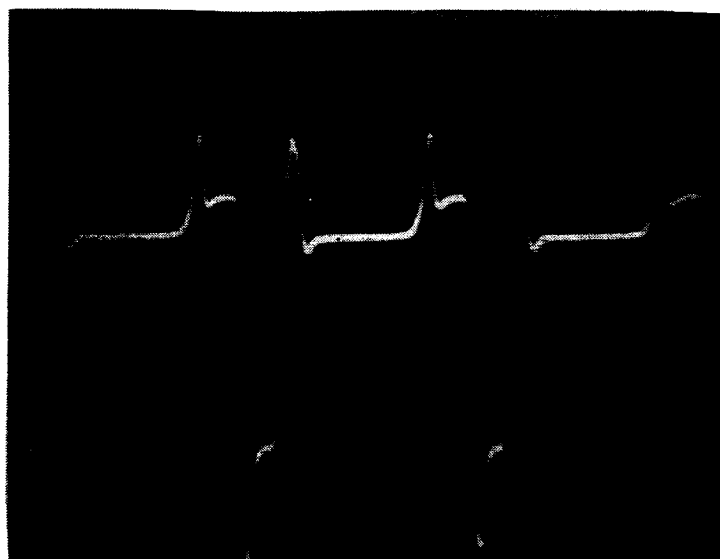


Output Ripple Voltage At Full Load - 16 Volt Input
Vertical Scale - .1 Volt/cm
Horizontal Scale - 10 μ sec/cm

Figure I-36 Output Ripple Voltage 50 Watt Chopper



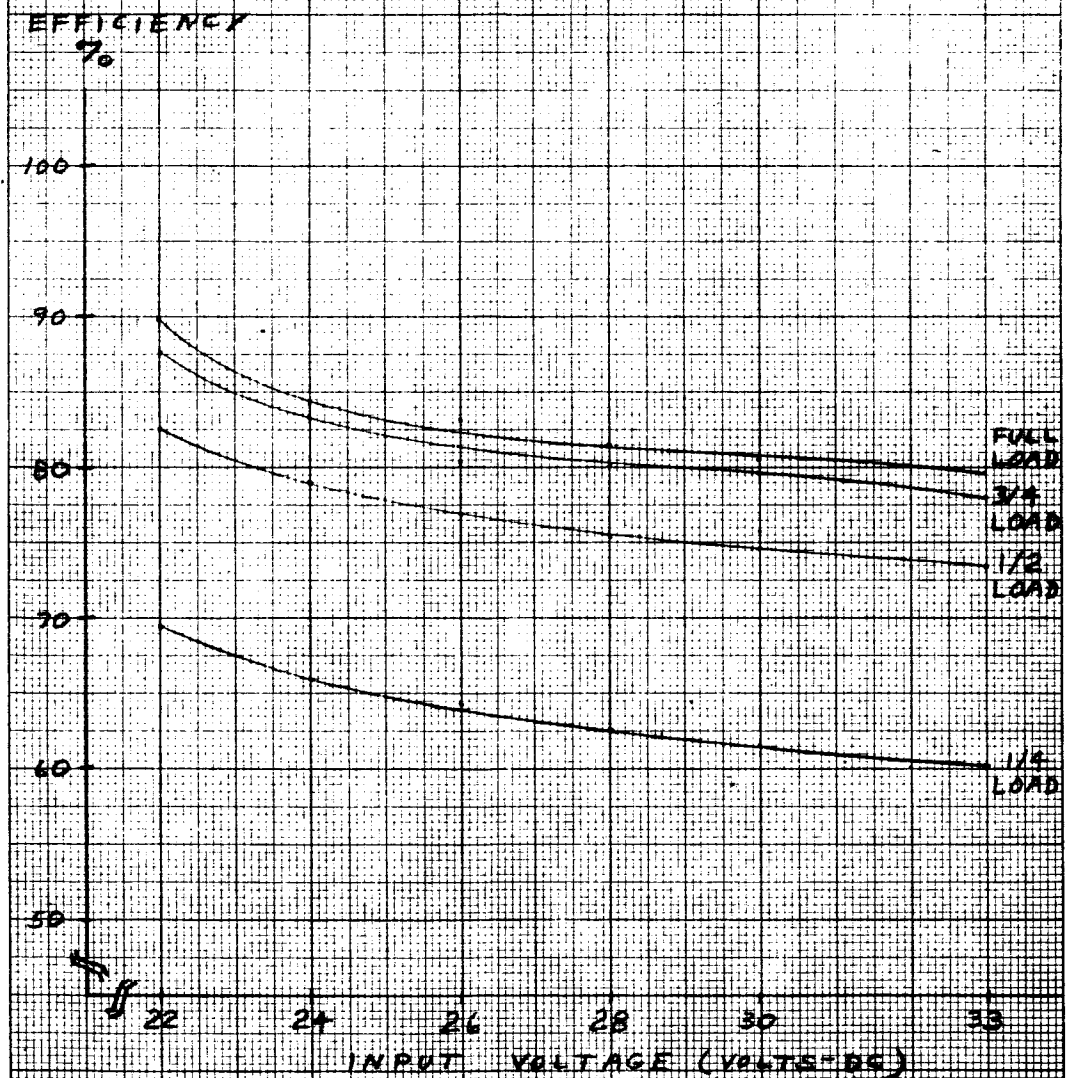
Input Ripple Current At No Load - 16 Volt Input
Vertical Scale - 0.720 Amps/cm
Horizontal Scale - 10 μ sec/cm



Input Ripple Current At Full Load - 16 Volt Input
Vertical Scale - 1.44 Amps/cm
Horizontal Scale - 10 μ sec/cm

Figure I-37 Input Ripple Current 50 Watt Chopper

FIGURE I-38
EFFICIENCY VS. INPUT VOLTAGE
100 WATT CHOPPER

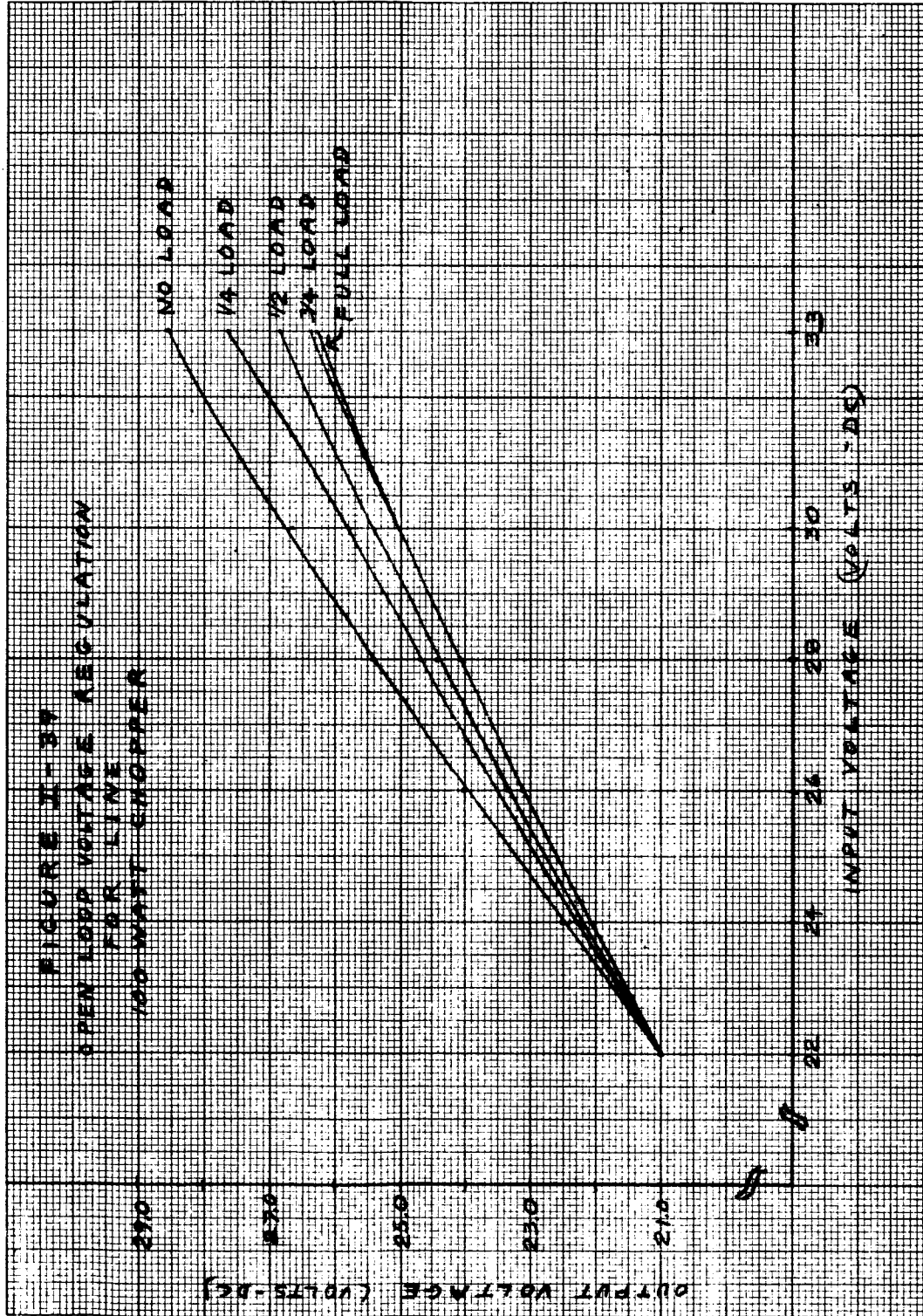


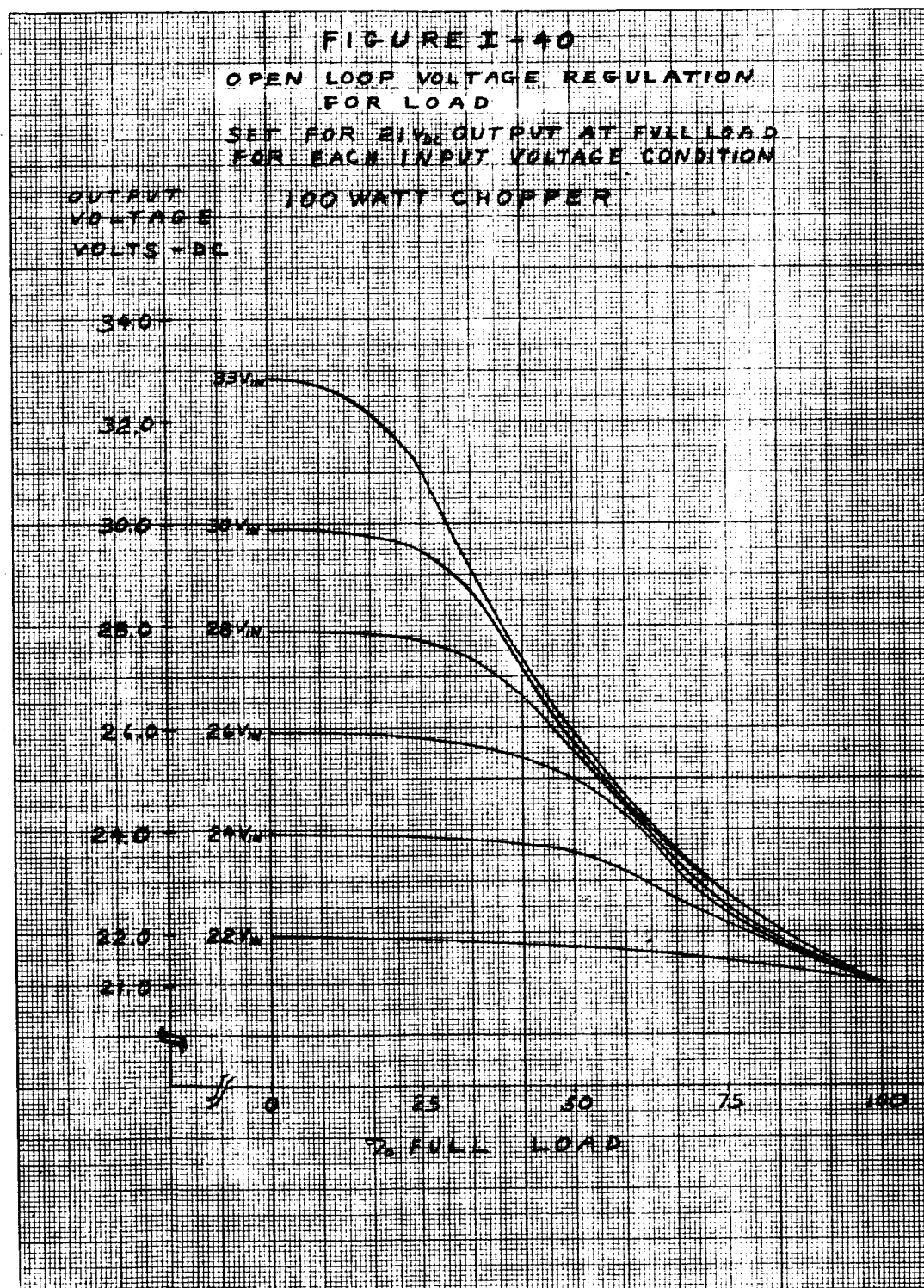
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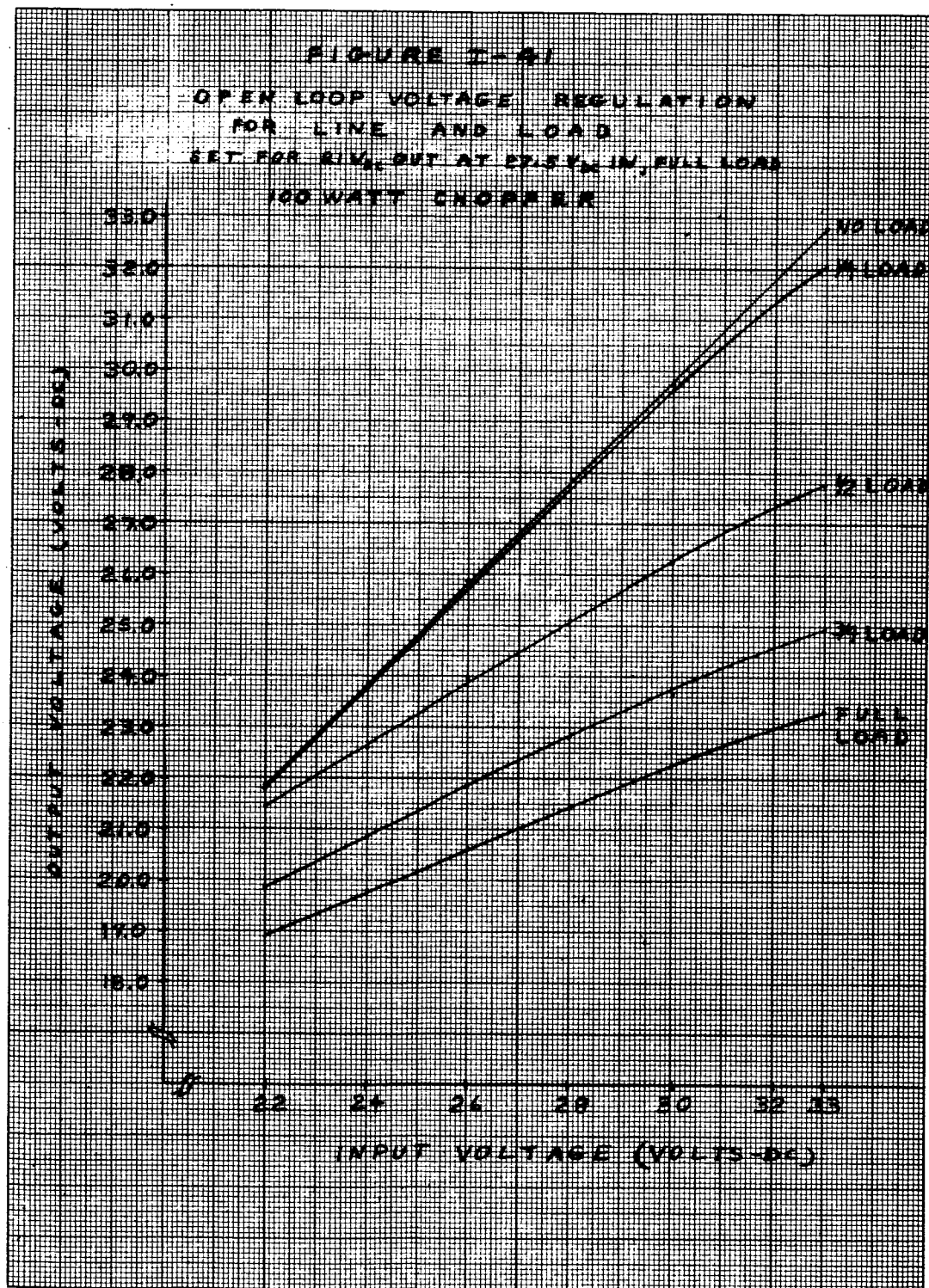


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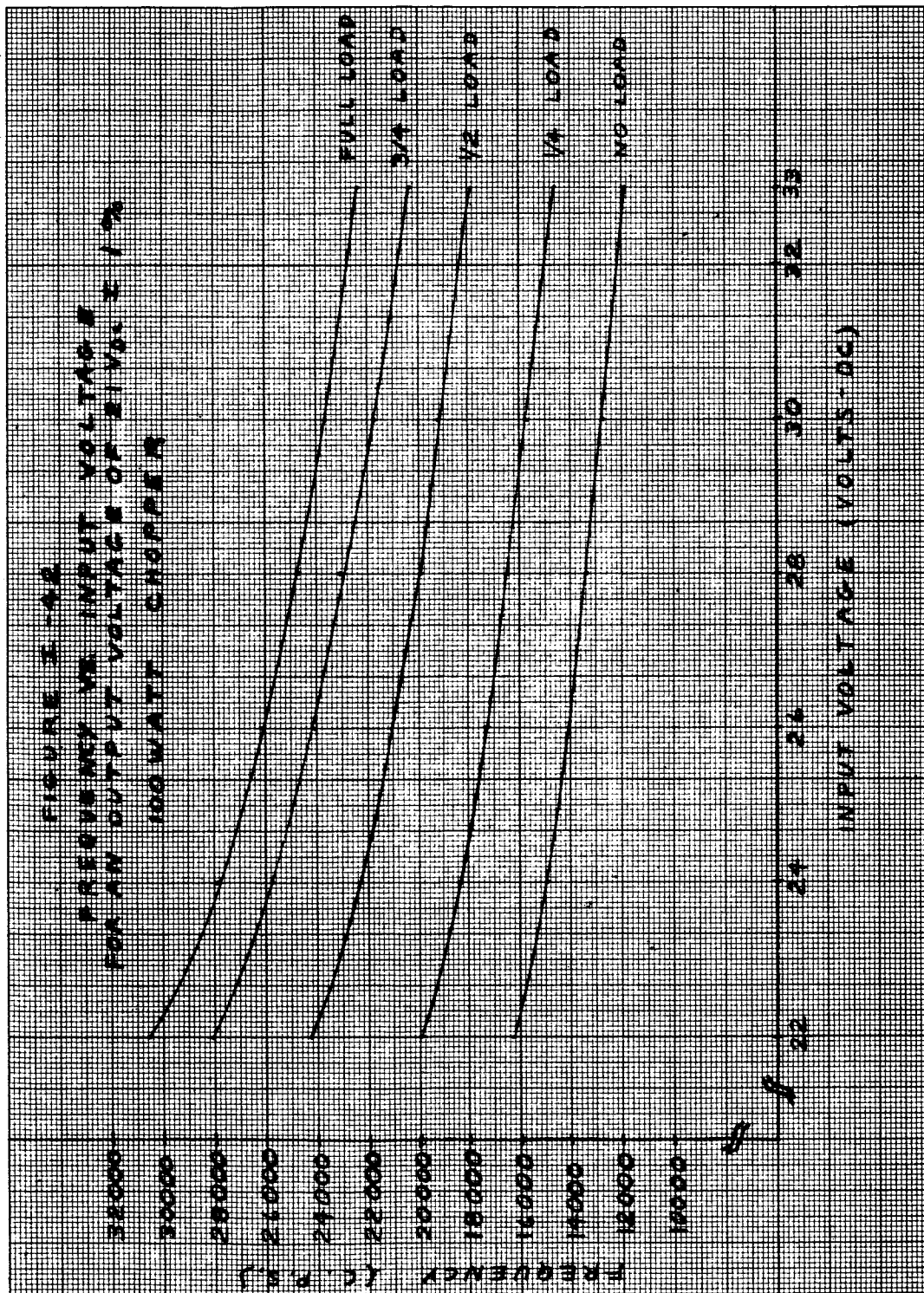


FIGURE I-43
OPEN LOOP VOLTAGE REGULATION
VS. TEMPERATURE
100 WATT CHOPPER

OUTPUT
VOLTAGE
(VOLTS-DC)

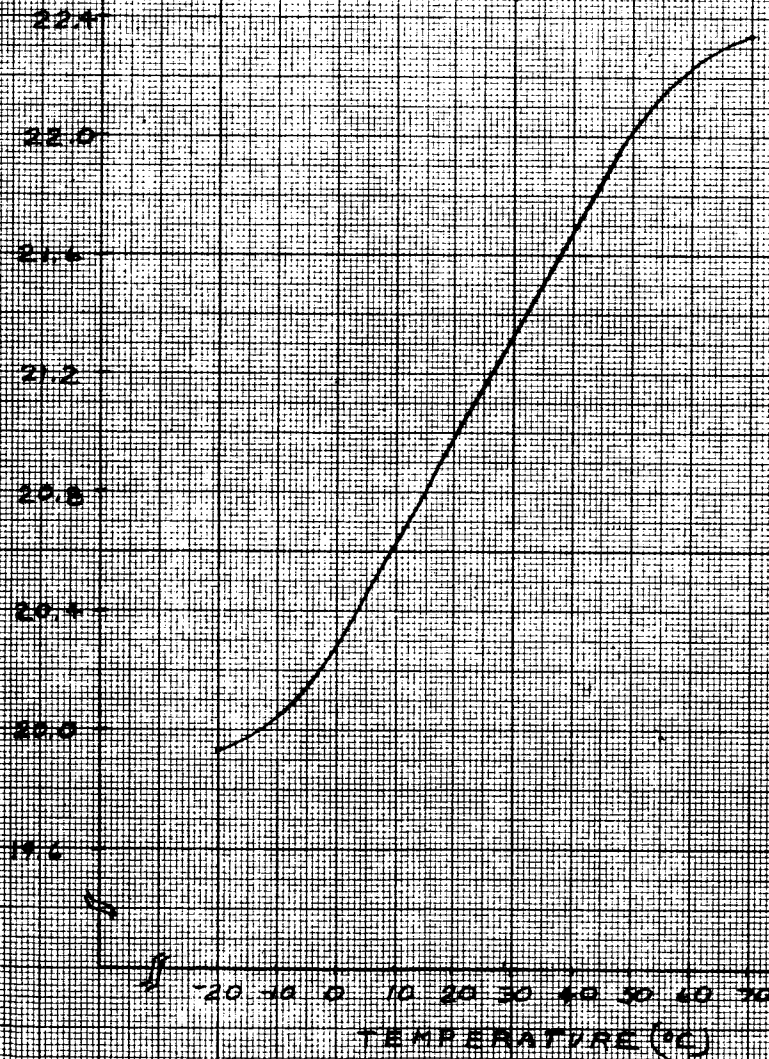


FIGURE I-44
OUTPUT VOLTAGE STABILITY
100 WATT CHOPPER

OUTPUT
VOLTAGE
(VOLTS-DC)

21.60

21.50

21.40

21.30

21.20

21.10

21.00

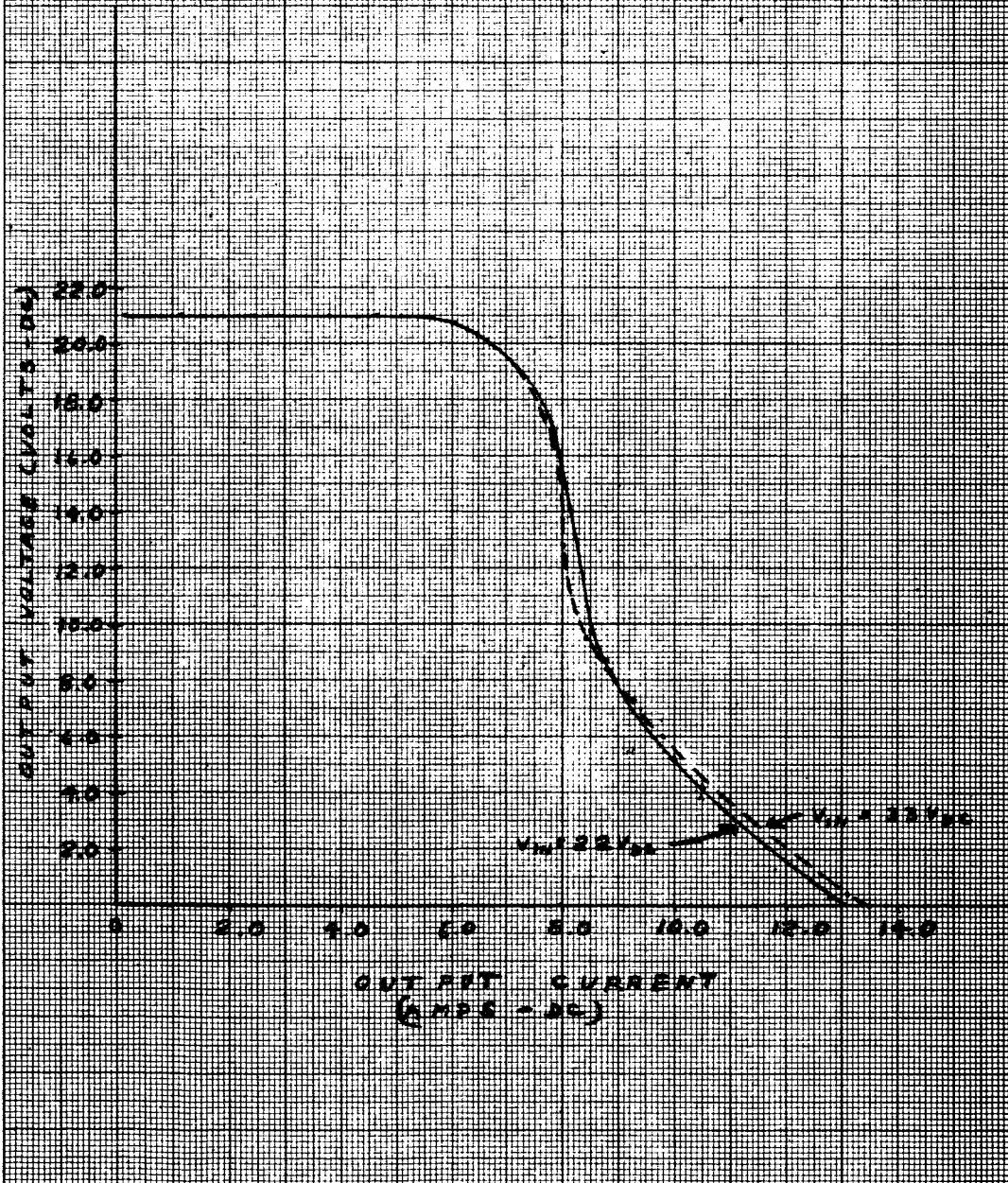
0 5 10 15 20 25 30 35 40 45

TIME (HOURS)

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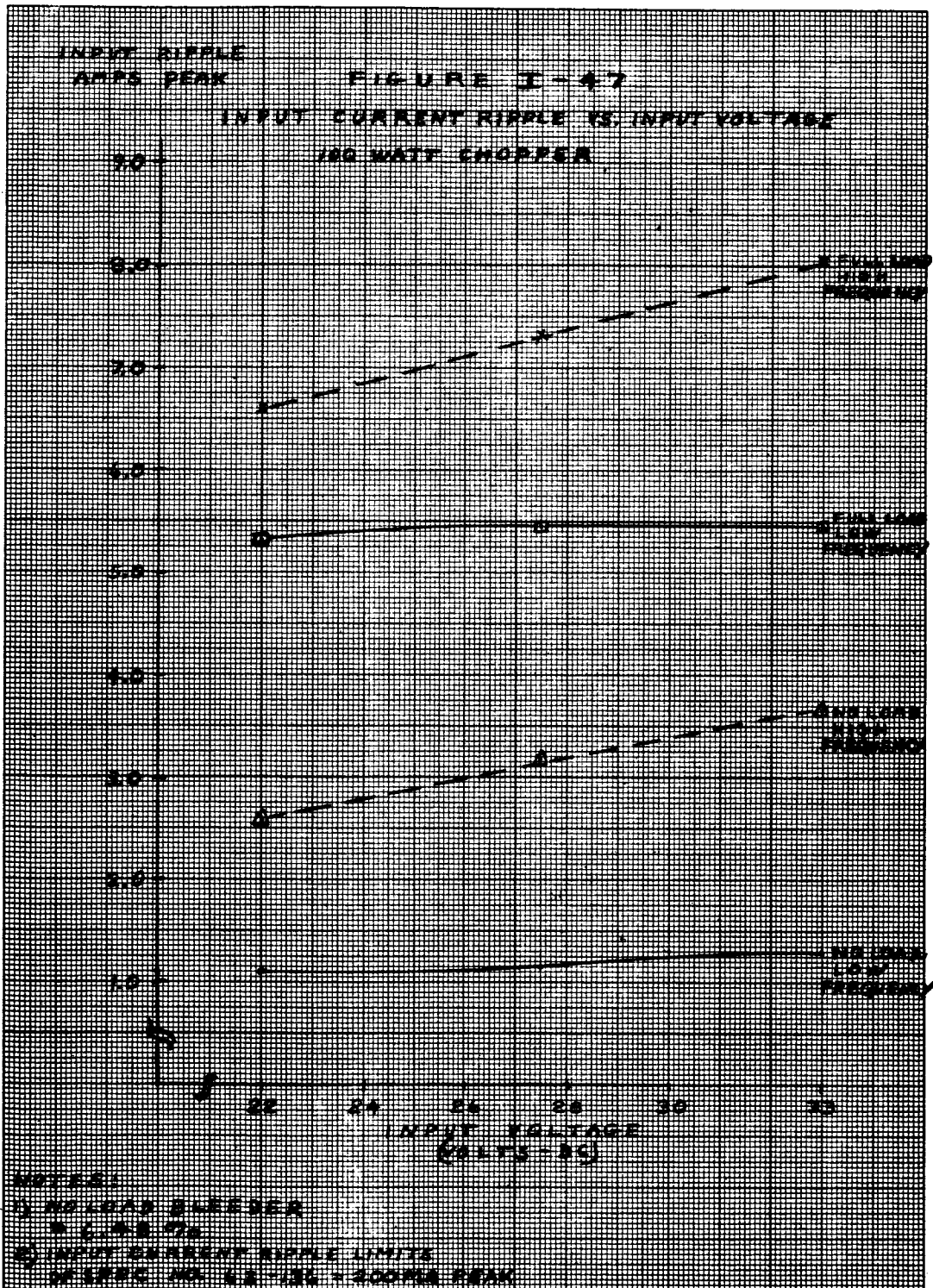
FIGURE I-45
OVERLOAD AND SHORT CIRCUIT
CHARACTERISTIC
100 WATT CHOPPER

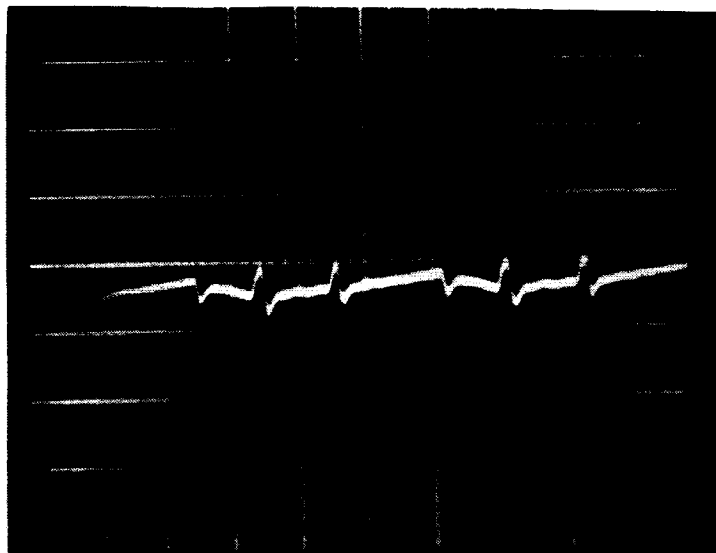


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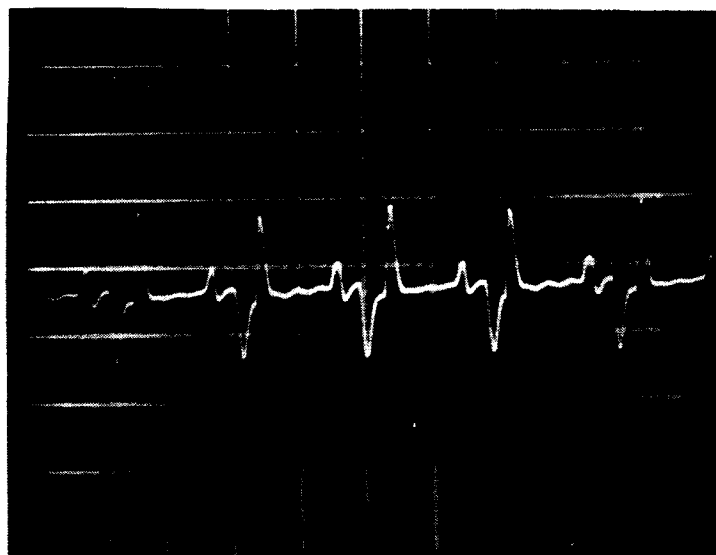
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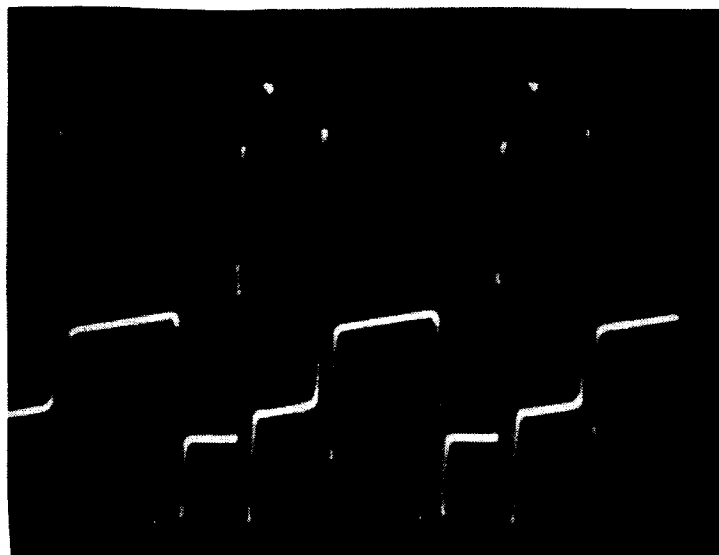


Output Ripple Voltage At No Load - 27.5 Volt Input
 Vertical Scale - .1 Volt/cm
 Horizontal Scale - 10 μ sec/cm

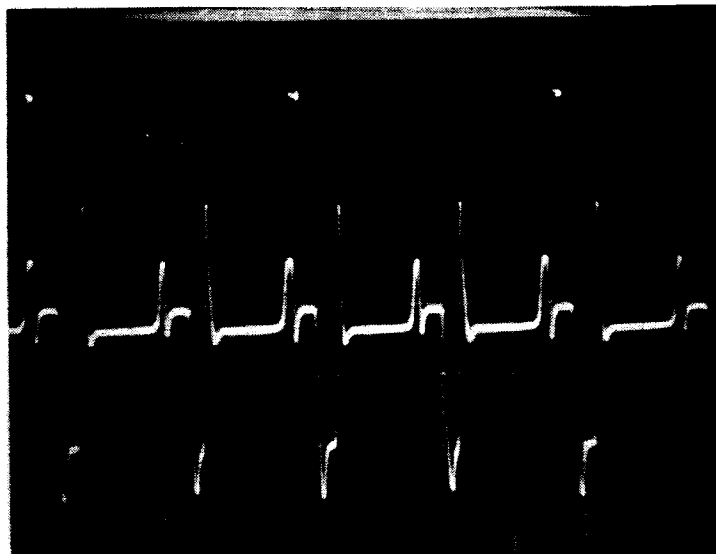


Output Ripple Voltage At Full Load - 27.5 Volt Input
 Vertical Scale - .1 Volt/cm
 Horizontal Scale - 10 μ sec/cm

Figure I-48 Output Ripple Voltage 100 Watt Chopper



Input Ripple Current At No Load - 27.5 Volt Input
 Vertical Scale - 1.44 Amps/cm
 Horizontal Scale - 10 μ sec/cm



Input Ripple Current At Full Load - 27.5 Volt Input
 Vertical Scale - 2.88 Amps/cm
 Horizontal Scale - 10 μ sec/cm

Figure I-49 Input Ripple Current 100 Watt Chopper

APPENDIX II

Breadboard Test Data

Booster Regulator Power Supplies

NOTE

Selected electrical performance tests were run on the four booster breadboards. The data for the 10 watt breadboard is shown in figure II-1 through II-11, and typical waveforms of output voltage ripple and input current ripple are shown in figures II-12 through II-13. Data for the 25, 50 and 100 watt breadboards is shown in figures II-14 through II-49.

An analysis of the 10 watt booster breadboard data is presented in this section.

BOOSTER DATA ANALYSIS

II-1 Efficiency

The efficiency tests were run at full, $3/4$, $1/2$ and $1/4$ load with the output voltage held at 22.0 volts as the input voltage was varied from 10 VDC to 20 VDC. At full load the efficiency increased from 86.4% to 87.7% as the input voltage was increased from 10 VDC to 20 VDC. This was primarily due to a decrease in the DC current through the choke and the peak current through the flyback transistor. At 25% of full load the efficiency decreased from 76.3% at 10 volts in to 67.0% at 20 volts in. This was accounted for by reset losses. At low power levels the losses of the main power components decreased, but the losses in the reset circuit remained relatively constant as the load was decreased and increased with input voltage.

II-2 No Load Losses

The no load losses of the 10 watt booster varied from about .55 watts to .85 watts as the input voltage increased from 10 VDC to 20 VDC, and varied from 4.4 watts to 4.9 watts for the 100 watt booster as the input voltage was varied from 22 volts to 33 volts. The losses were higher for the 100 watt booster, because the inductance was about 25% of the value for the 10 watt booster. This made it necessary to make the no load current in the 100 watt booster about four times that of the 10 watt booster to keep the current in the choke continuous. This demonstrated that at light loads the major losses were in the reset circuit. As explained above, the reset losses were relatively independent of load and increased with input voltage.

II-3 Open Loop Voltage Regulation for Line Variations

The open loop line regulation showed a low point in the output voltage at about 15 volts inputs. The droop became more pronounced at light loads. Experimental data and calculations have shown that at about 15 volts input the ratio of the voltage across the reset capacitor C5 to the on-time of the flyback transistor was a minimum. This indicated that the volt-second product during the on-time of the flyback transistor could become greater than the volt-second product during reset which is supplied by the voltage across capacitor C5. Under this condition the drive transformer saturated during the on cycle and turned off the flyback transistor before its duty cycle was completed. This resulted in a decreased output voltage. This caused a total excursion of about .42 volts at full load and about 1.1 volts at no load.

II-4 Open Loop Voltage Regulation for Load Variations

As the load was decreased from full load to $1/4$ load the output voltage increased from 22.0 to 23.3 volts at low line and 22.0 to 22.18 at high line. The change was linear indicating an effective voltage drop.

At loads less than 25% of full load, the DC input current became smaller than the zero to peak input ripple current, so the choke current dropped to zero during the off-time of the flyback transistor. Because of this the inherent regulation became ineffective and the output voltage increased to 24.1 volts at low line and 22.5 at high line.

II-5 Open Loop Voltage Regulation for Line and Load Variations

The regulation for line and load demonstrated the cumulative effect of the line regulation and the load regulation. For this test the output voltage was set once and not readjusted throughout the test. The changes in output voltage are similar to the line regulation test, except that they are not equal at full load. The equal distances between the curves at different load shows that regulation is linear with respect to load except at no load where the choke current becomes a factor.

The total excursion of output voltage over the entire load and line range was between 24.0 and 21.5 volts.

II-6 Closed Loop Percent Duty Cycle Characteristic

Ideally the percent duty cycle would vary with line voltage and be constant with respect to load variations. The test showed that a slightly longer on-time (i.e. more boost) was required at full load than no load, to compensate for IR drops.

At low line the percent duty cycles for no load and full load were 52.0% and 52.5% respectively, and at high line they were 8.0% and 9.0%. Calculated values for low and high line were 54.5% and 9.1%, respectively. Values are within the accuracy of the test.

II-7 Open Loop Voltage Regulation for Temperature Variations

The 10 watt booster was set at 22 volts out, full load with 15 volts in after the unit had stabilized at room temperature. Without adjusting the output voltage the unit was run at 70°C for one hour. The voltage stabilized at about 20.3 VDC. The temperature was lowered to -20°C for one hour and the voltage stabilized at about 21.7 VDC. The change in output was caused by variations in gain and transistor emitter-base junction changes as a function of temperature.

II-8 Output Voltage Stability

The output voltage stability test was run continuously for 44 hours. The results of the stability test showed a general downward trend in output voltage, but to be conclusive the test would have to be run over a longer period of time with more frequency readings. The maximum excursion was 22.01 to 21.86 volts, however, at the end of the test the voltage had only varied from 22.0 to 22.01 volts.

II-9 Overload Characteristics

The output voltage was set at 22.0 volts at full load for this test; then the load was increased from no load to about 300% of full load. At both high and low line the voltage dropped off almost linearly. No attempt was made to approach a short circuit condition since there were no means of providing short circuit protection.

II-10 Output Ripple Voltage

The ripple voltage was divided into two components. The low frequency was interpreted as the ripple below 1 megacycle and the high frequency as all ripple over 1 megacycle.

The low frequency component was due to the charging and discharging of C6. The ripple should have decreased as V_{IN} increased because it is a function of % on-time. The data showed no increase, but this could have been due to the relative sizes of the high and low frequency components.

II-11 Input Ripple Current

The ripple current was divided into two components. The low frequency was interpreted as the ripple below one megacycle and the high frequency as all ripple over one megacycle.

Theoretically, the ripple at high line should have equalled 1/3 the ripple at low line. Neglecting changes in I_L , the ripple should have been the same at full load and no load. The data showed a relatively constant ripple for both load and line. This was probably because the values measured were very small compared to the high frequency spikes, causing distortion of the wave shape on the oscilloscope. The measured values were about 107 ma peak to peak.

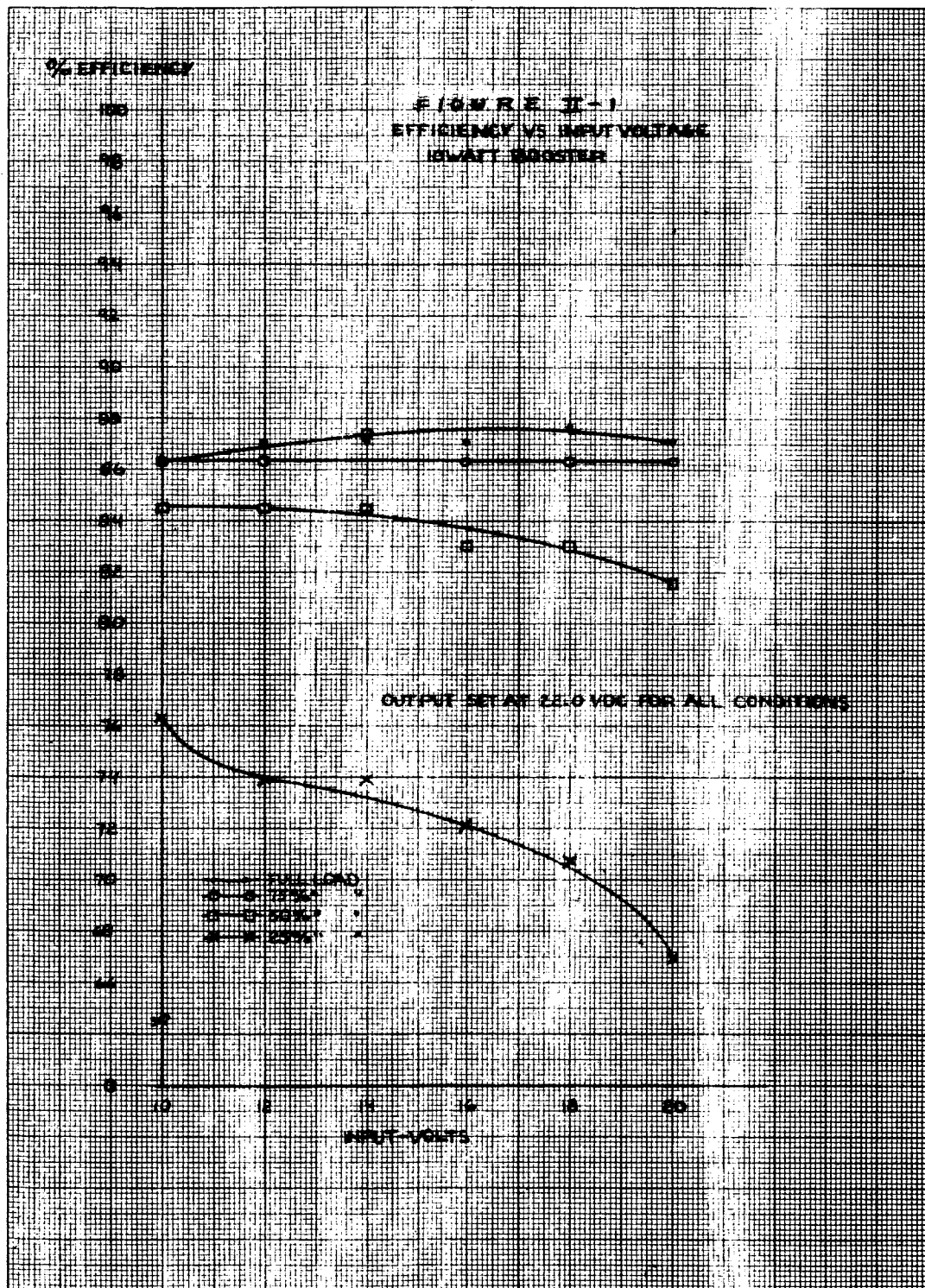


FIGURE II-2
NO LOAD LOSSES VS INPUT VOLTAGE

NO LOAD BLEEDERS USED:

- 10 WATT - NONE REQUIRED
- 25 WATT - 1.1% OF FULL LOAD
- 50 WATT - 1.4% OF FULL LOAD
- 100 WATT - 2.8% OF FULL LOAD

NO LOAD LOSSES
- WATTS -

5.0

4.0

3.0

2.0

1.0

0

10

12

14

16

18

20

22

24

26

28

30

32

34

INPUT VOLTAGE FOR 100 WATT BOOSTER

INPUT VOLTAGE FOR 10 WATT BOOSTER

100 WATT BOOSTER

50 WATT BOOSTER

25 WATT BOOSTER

10 WATT BOOSTER

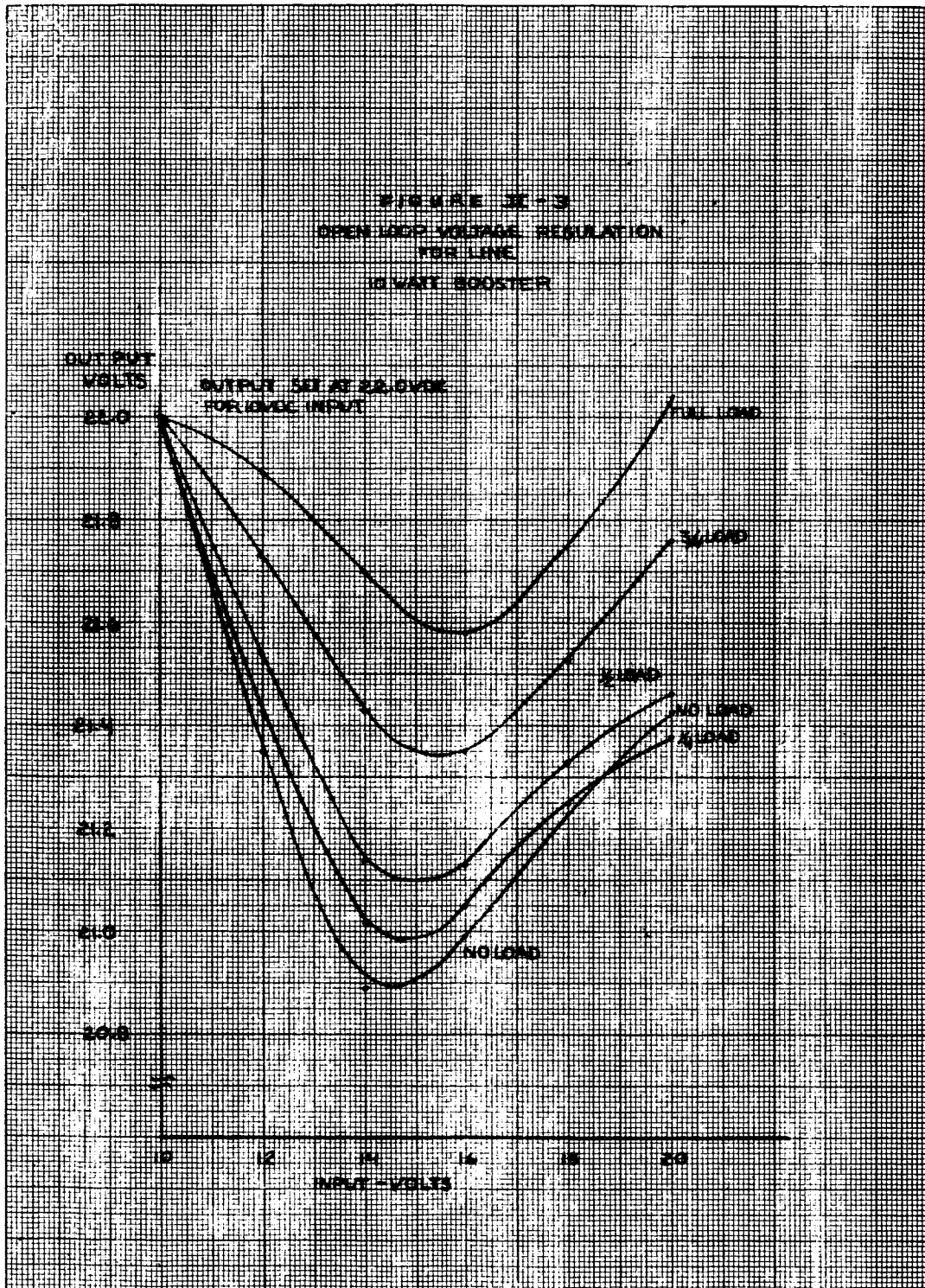
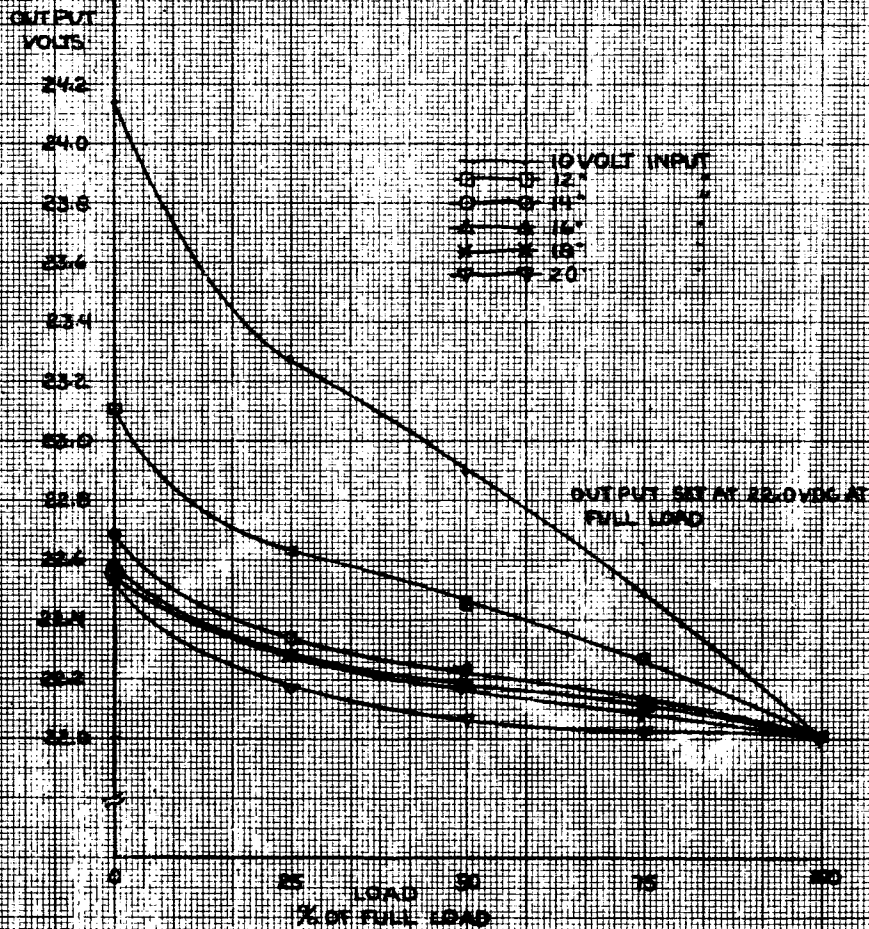


FIGURE II-4
OPEN LOOP VOLTAGE REGULATION
FOR LOAD
10WATT BROOKER



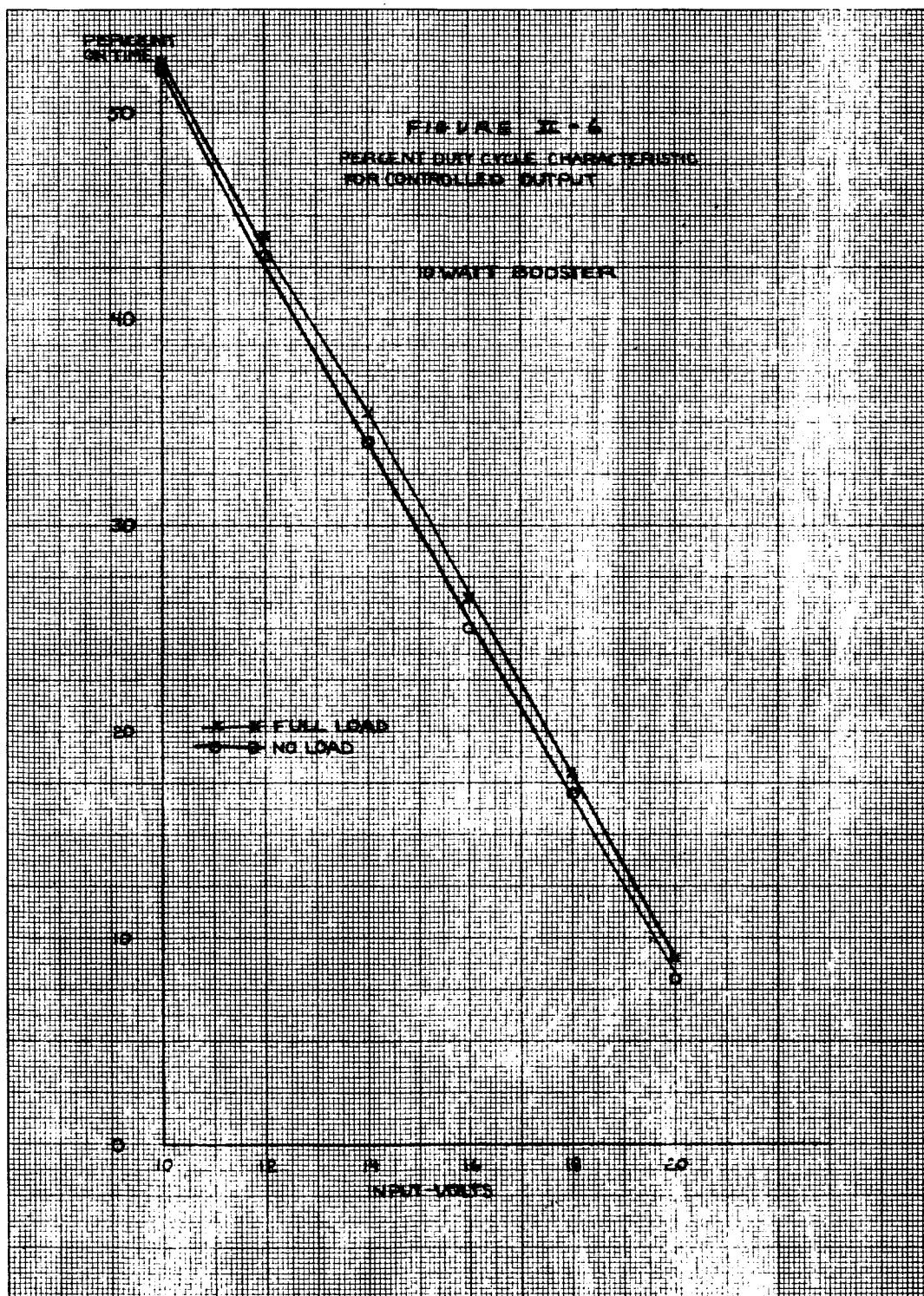


FIGURE 11-5
OPEN LOOP VOLTAGE REGULATION
FOR LINE AND LOAD
10 WATT BOOSTER

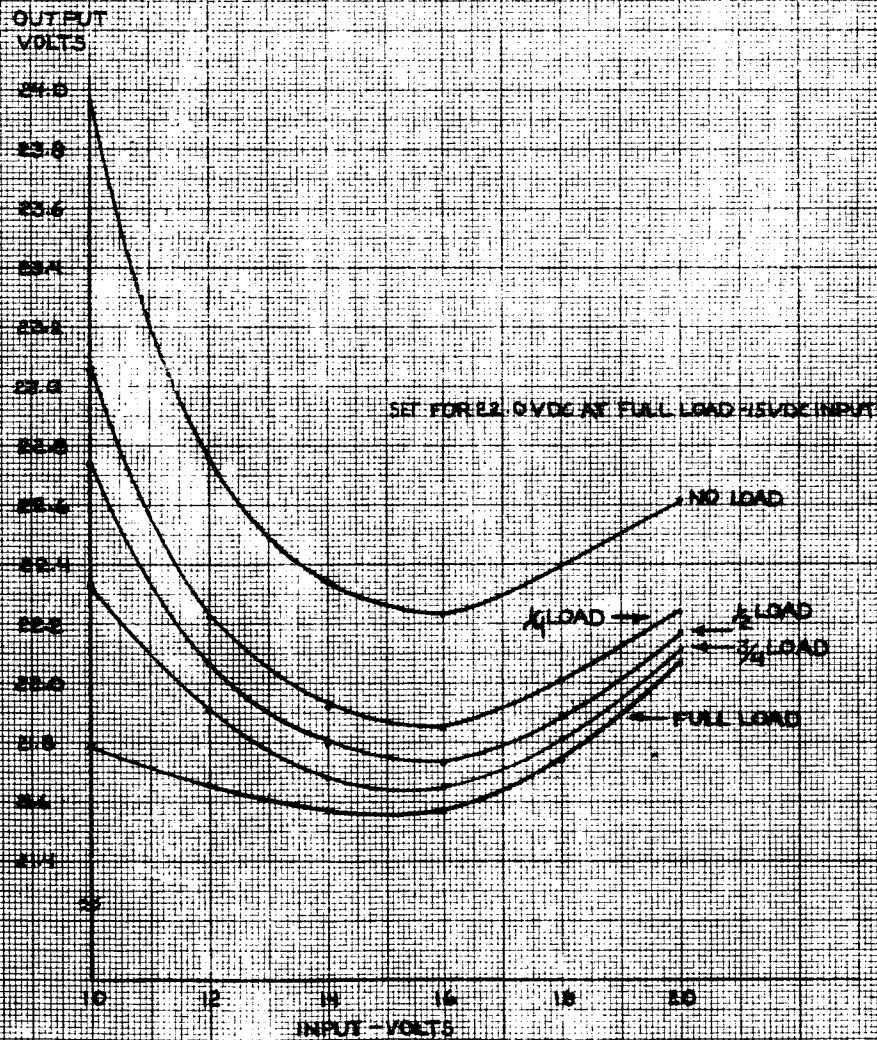
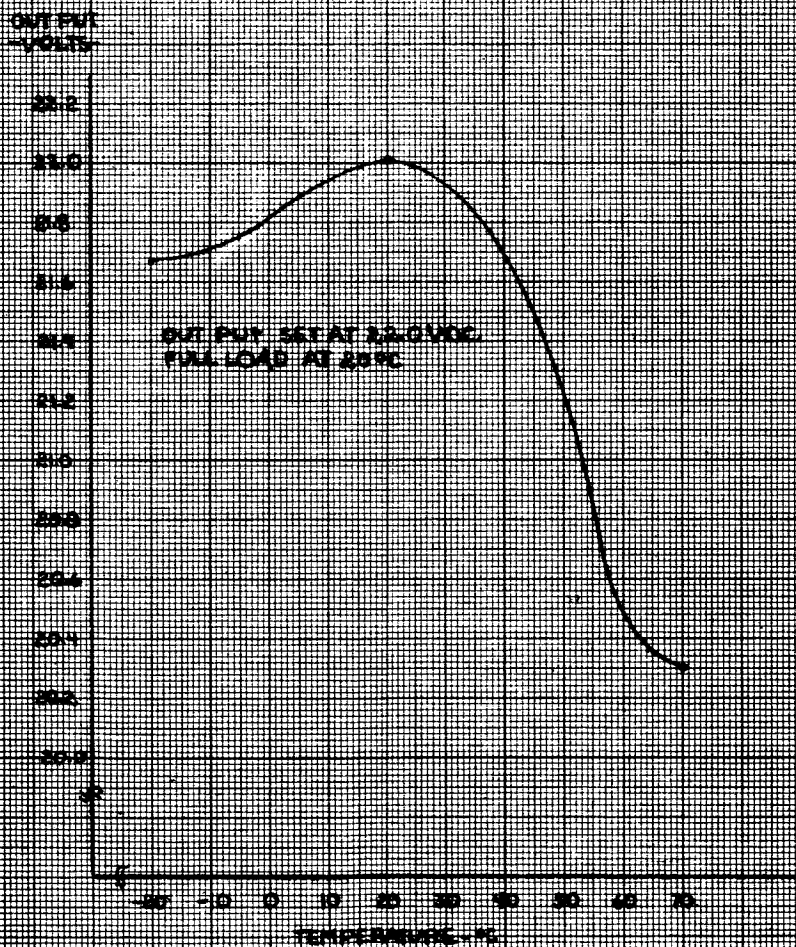


FIGURE II-7
OPEN LOOP VOLTAGE REGULATION
VS TEMPERATURE

LOWANT BOOSTER



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FIGURE 12-8
OUTPUT VOLTAGE STABILITY
10 WATT BOOSTER

OUTPUT
VOLTS

32.0

31.5

31.0

30.5

30.0

100% LOAD

TIME - SECS

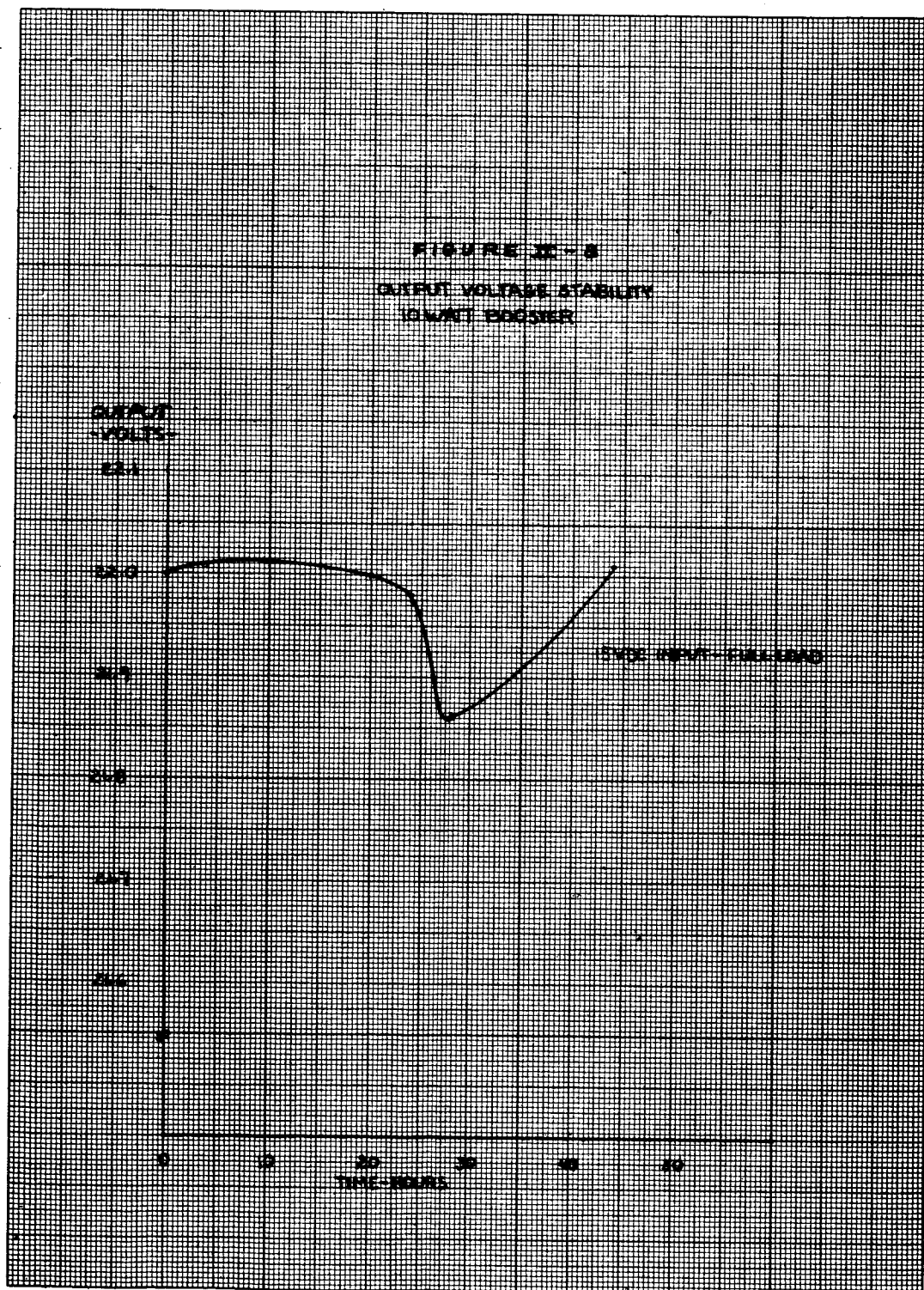
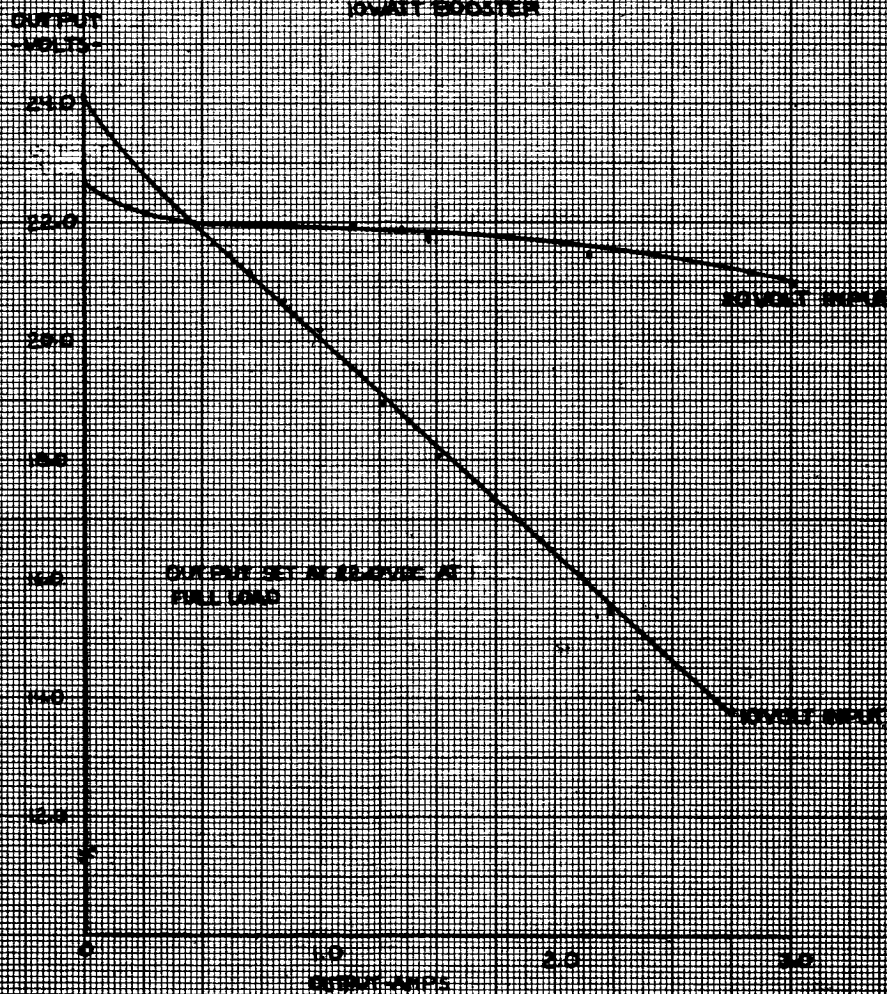


FIGURE II-9
OPEN LOOP OVERLOAD
VOLTAGE VS. CURRENT
JOVATT BOOSTER



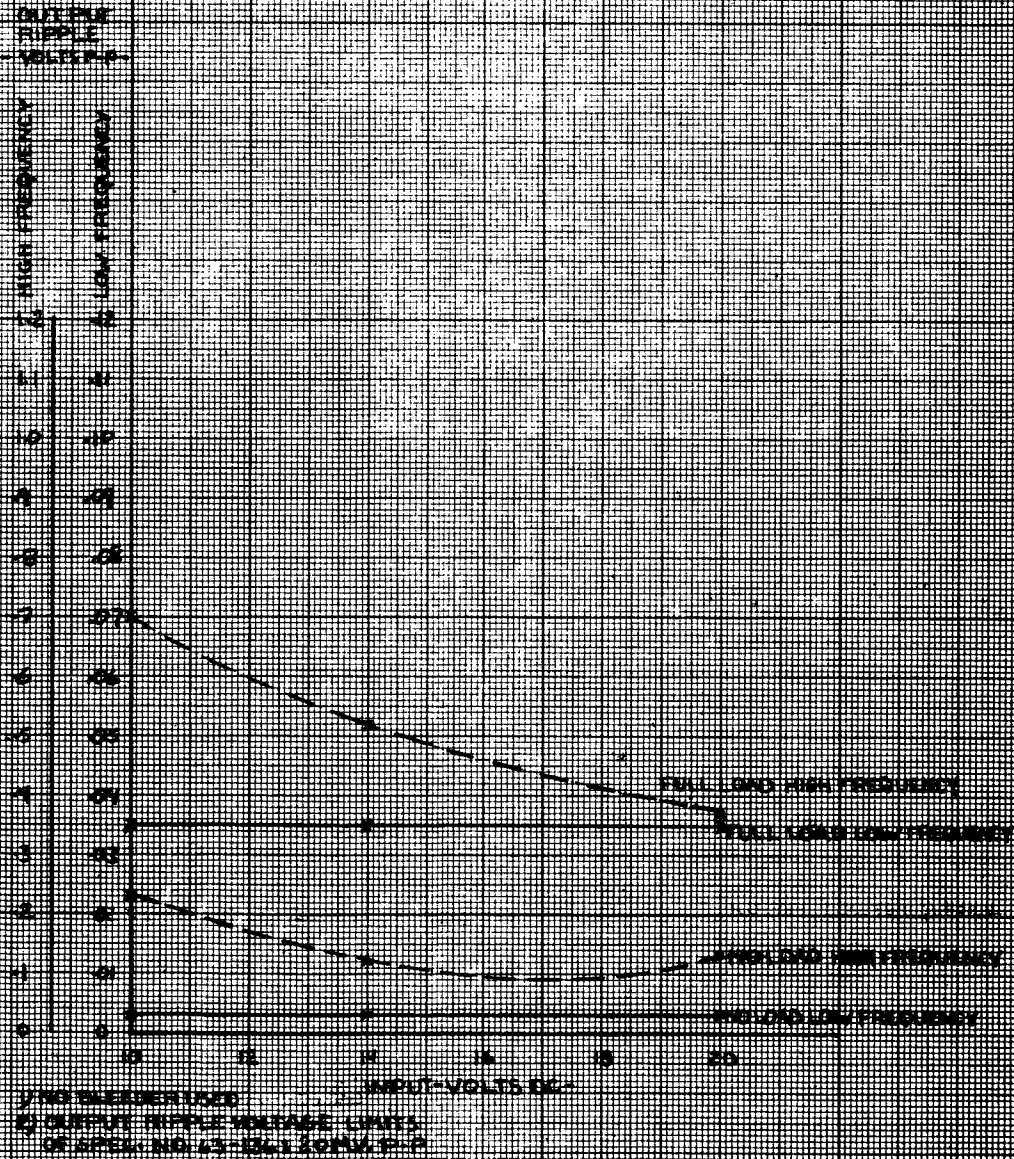
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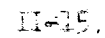
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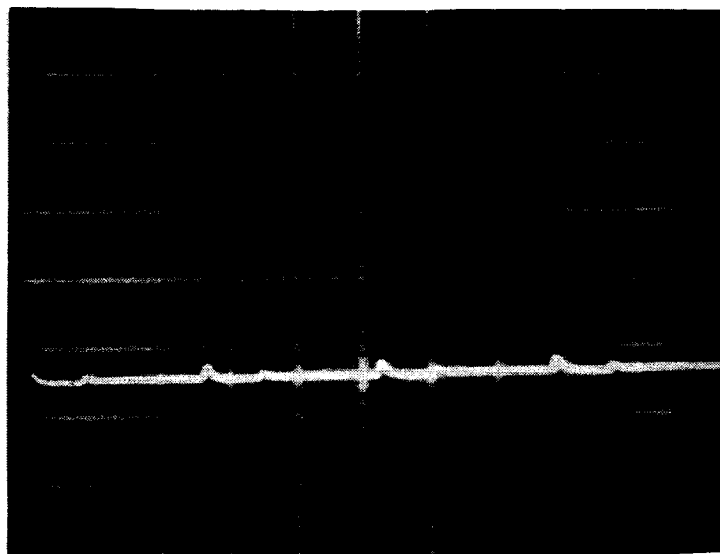
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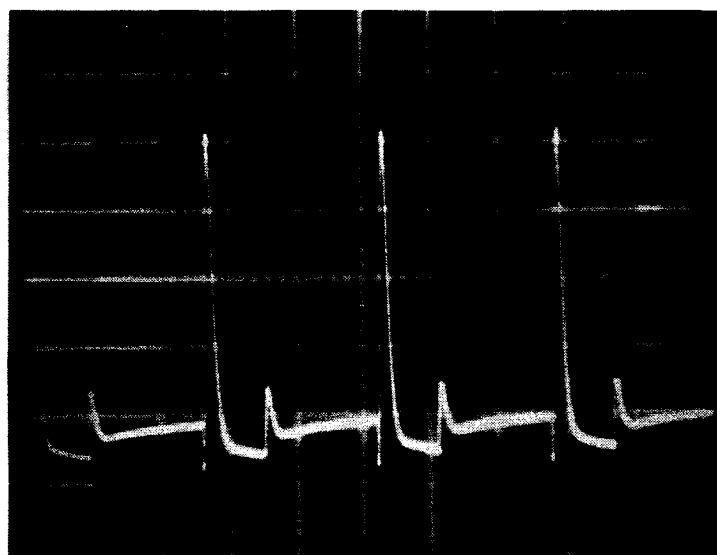
FIGURE 11-10
OUT PUT VOLTAGE RIPPLE VS. INPUT VOLTAGE
10WATT BOOSTER





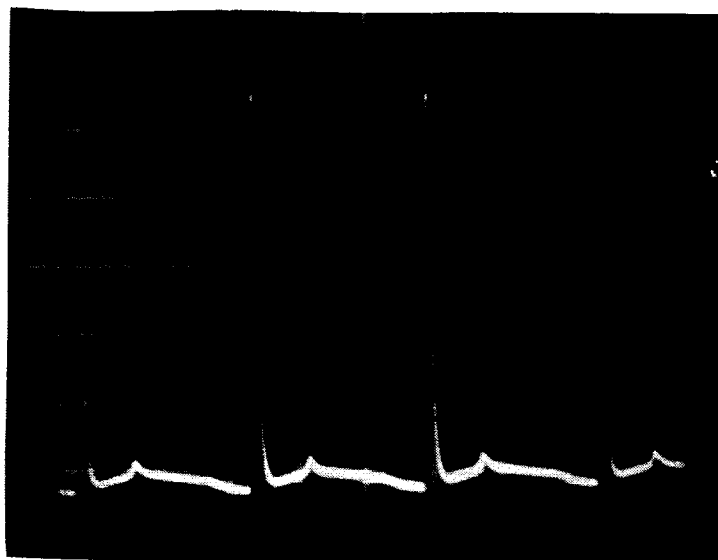


Output Ripple Voltage At No Load - 15 Volt Input
Vertical Scale - .1 Volt/cm
Horizontal Scale - 10 μ sec/cm

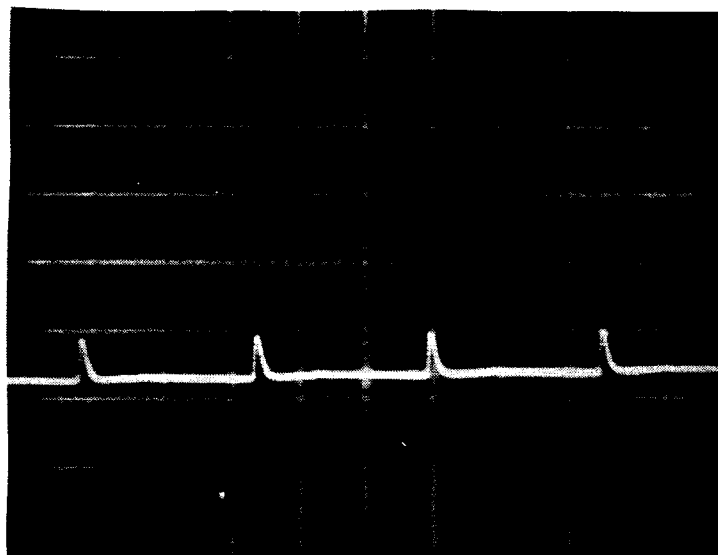


Output Ripple Voltage At Full Load - 15 Volt Input
Vertical Scale - .1 Volt/cm
Horizontal Scale - 10 μ sec/cm

Figure II-12 Output Ripple Voltage 10 Watt Booster



Input Ripple Current At No Load - 15 Volt Input
Vertical Scale - .27 Amp/cm
Horizontal Scale - 10 μ sec/cm

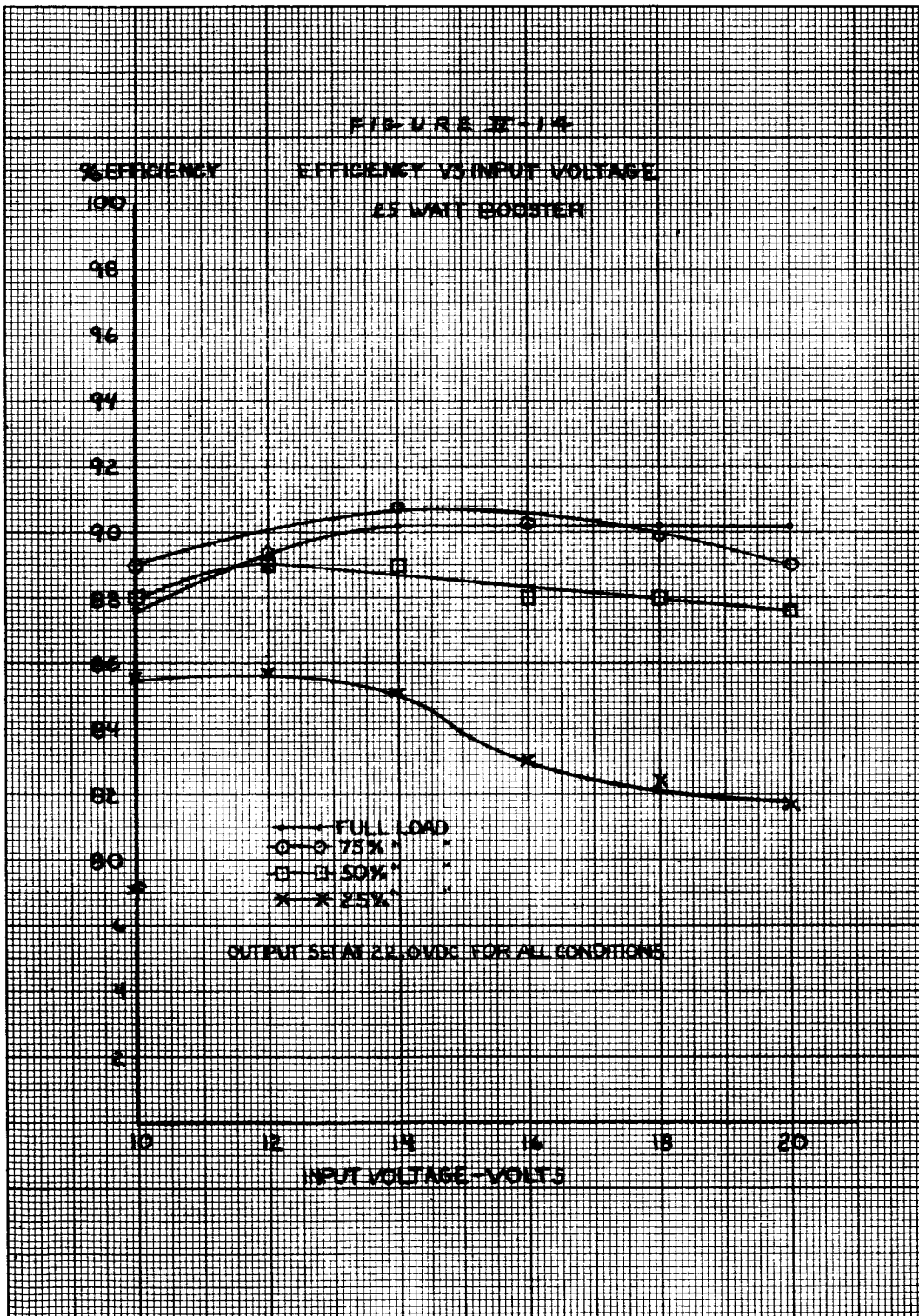


Input Ripple Current At Full Load - 15 Volt Input
Vertical Scale - 2.7 Amps/cm
Horizontal Scale - 10 μ sec/cm

Figure II-13 Input Ripple Current 10 Watt Booster

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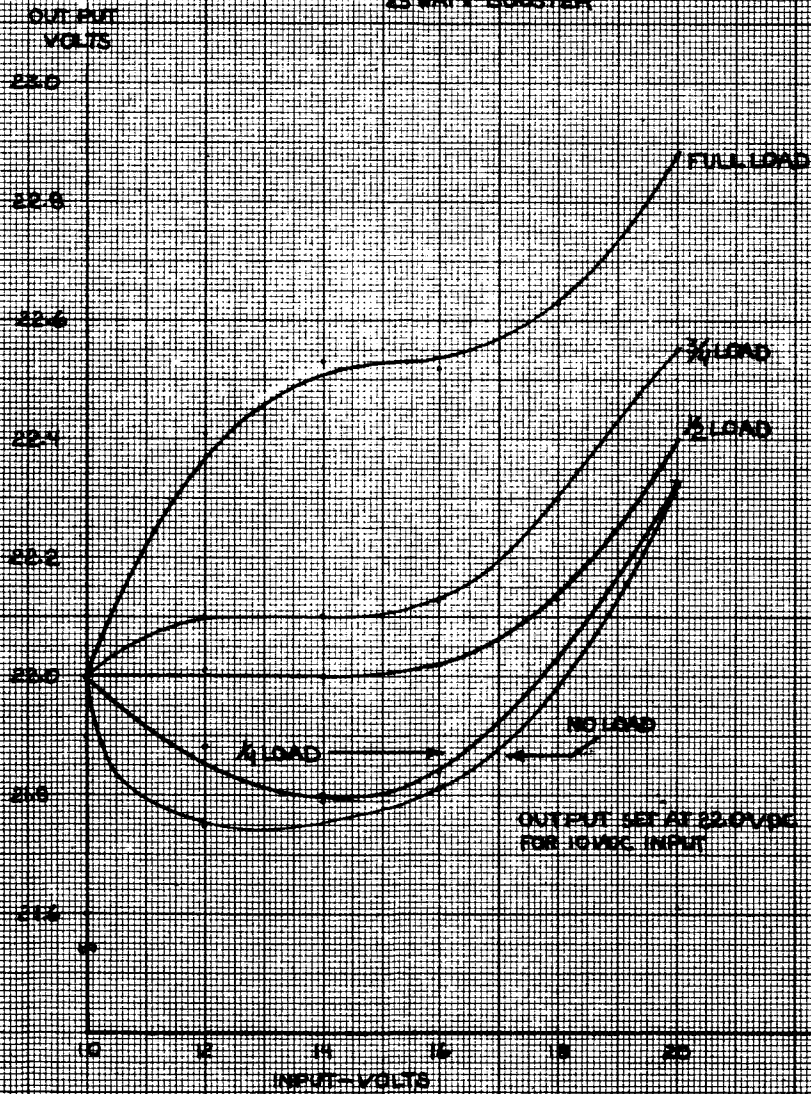
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FIGURE 3-15
OPEN LOOP VOLTAGE REGULATION
FOR LINE
25 WATT BOOSTER



OUTPUT SET AT 22.0VDC
FOR 10VDC INPUT

1) BLEEDER RES AT NO LOAD
10% OF FULL LOAD

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FIGURE II-16

OPEN LOOP VOLTAGE REGULATION
FOR LOAD
25WATT BOOSTER

OUTPUT
VOLTS

23.4

23.2

23.0

22.8

22.6

22.4

22.2

22.0

0

25

50

75

100

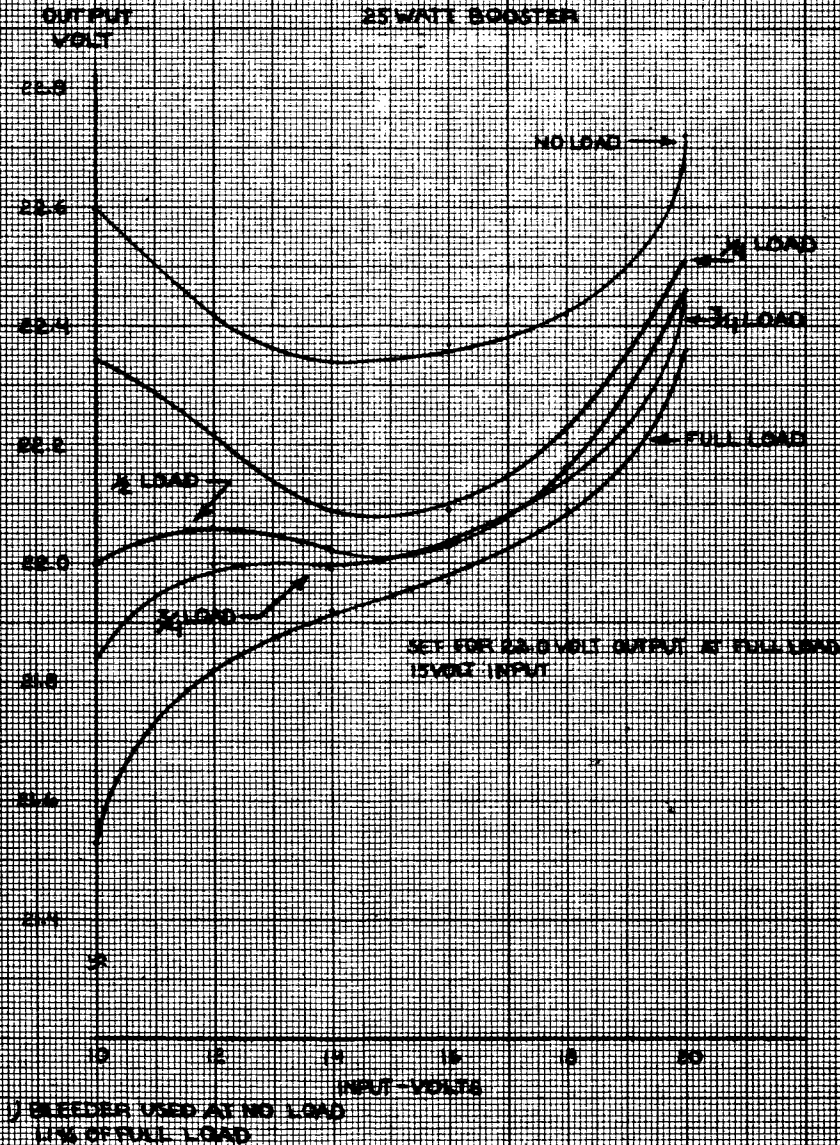
LOAD
% OF FULL LOAD

10 VOLT INPUT
12" " "
14" " "
16" " "
18" " "
20" " "

OUTPUT SET AT 22.0VDC
AT FULL LOAD

1) BLEEDER USED AT NO LOAD
1% OF FULL LOAD

FIGURE 3E-17
OPEN LOOP VOLTAGE REGULATION
FOR LINE AND LOAD
25WATT BOOSTER

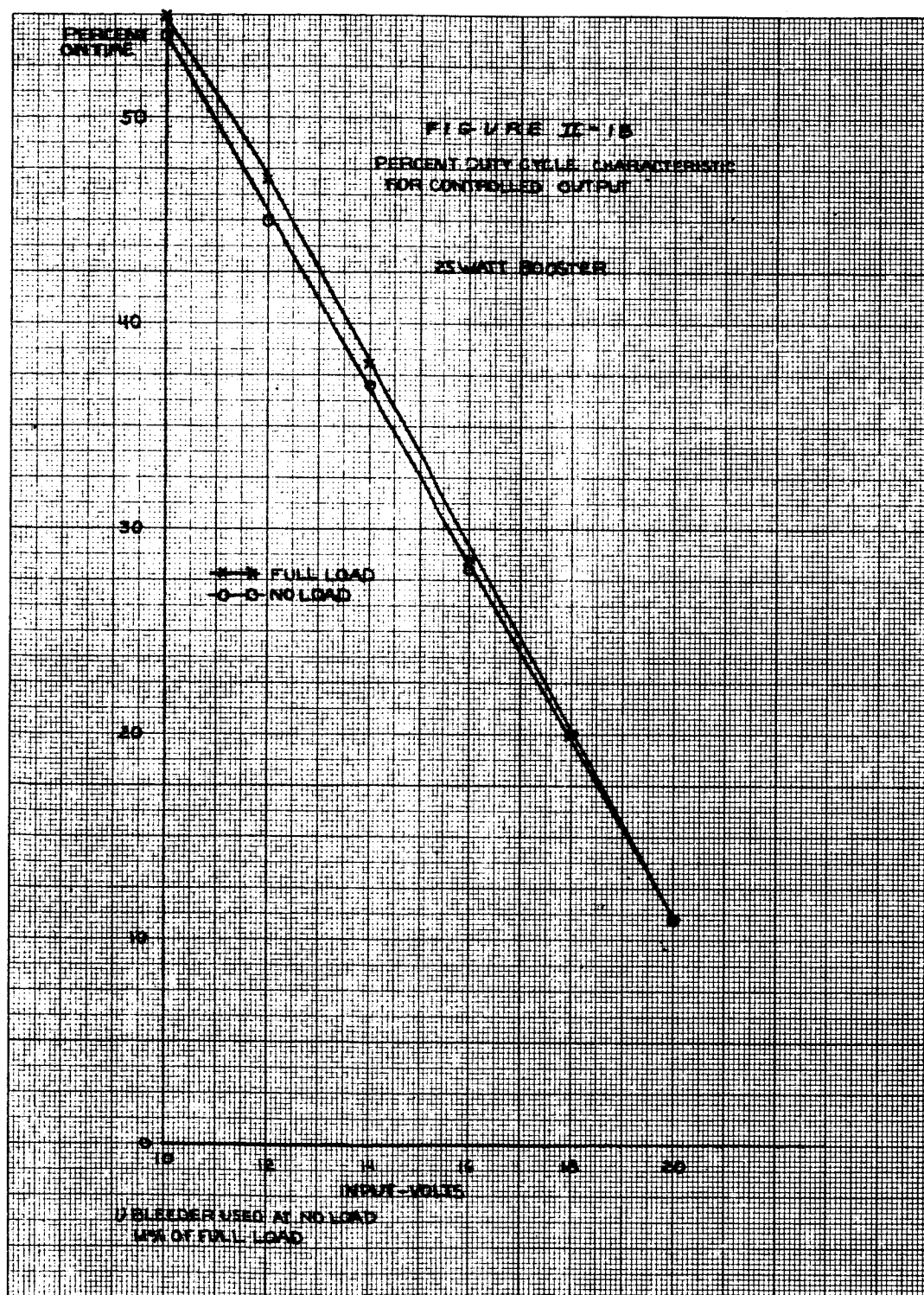


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FIGURE II-19
OPEN LOOP VOLTAGE REGULATION
VS TEMPERATURE

25 WATT BOOSTER

OUTPUT
VOLTS

24.0

23.6

23.2

22.8

22.4

22.0

21.6

21.2

20.8

20.4

20.0

19.6

OUTPUT SET AT 22.0VDC,
FULL LOAD AT 20°C

TEMPERATURE °C

FIGURE II-20
OUTPUT VOLTAGE STABILITY
25 WATT BOOSTER

OUTPUT
VOLTS

22.4

22.0

21.6

21.2

20.8

20.4

20.0

15 VOL INPUT - FULL LOAD

TIME - SECONDS

0

10

20

30

40

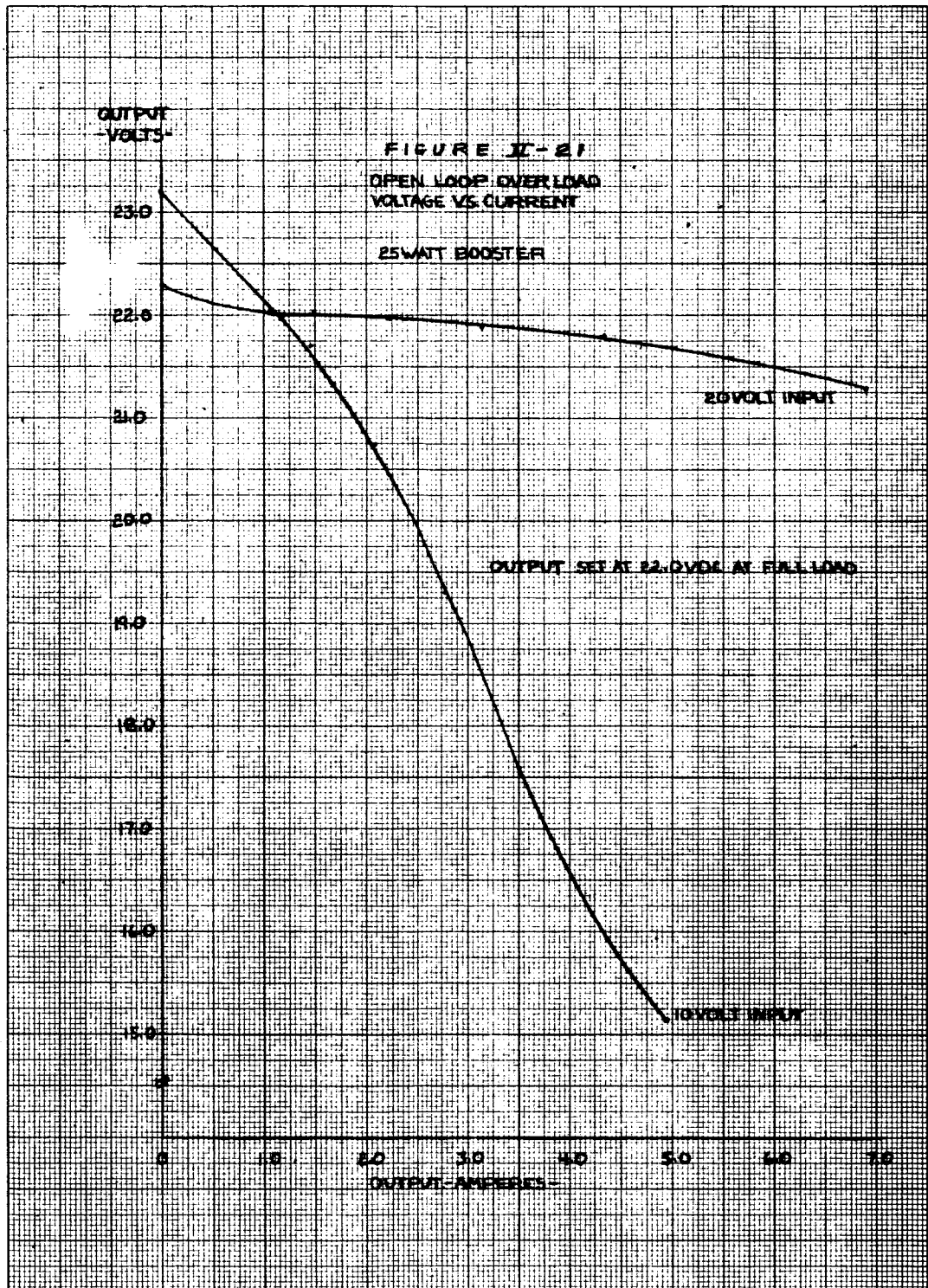
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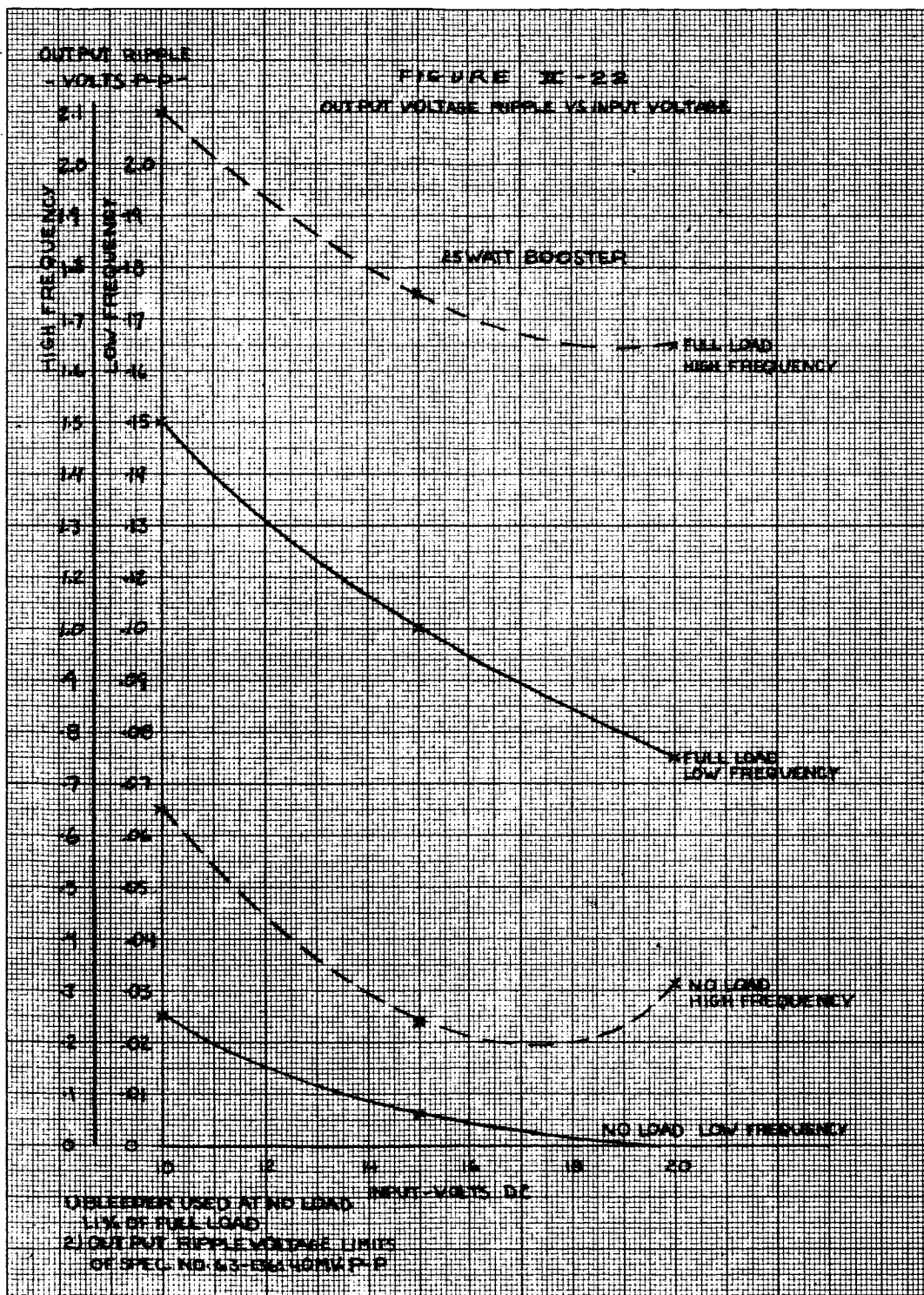
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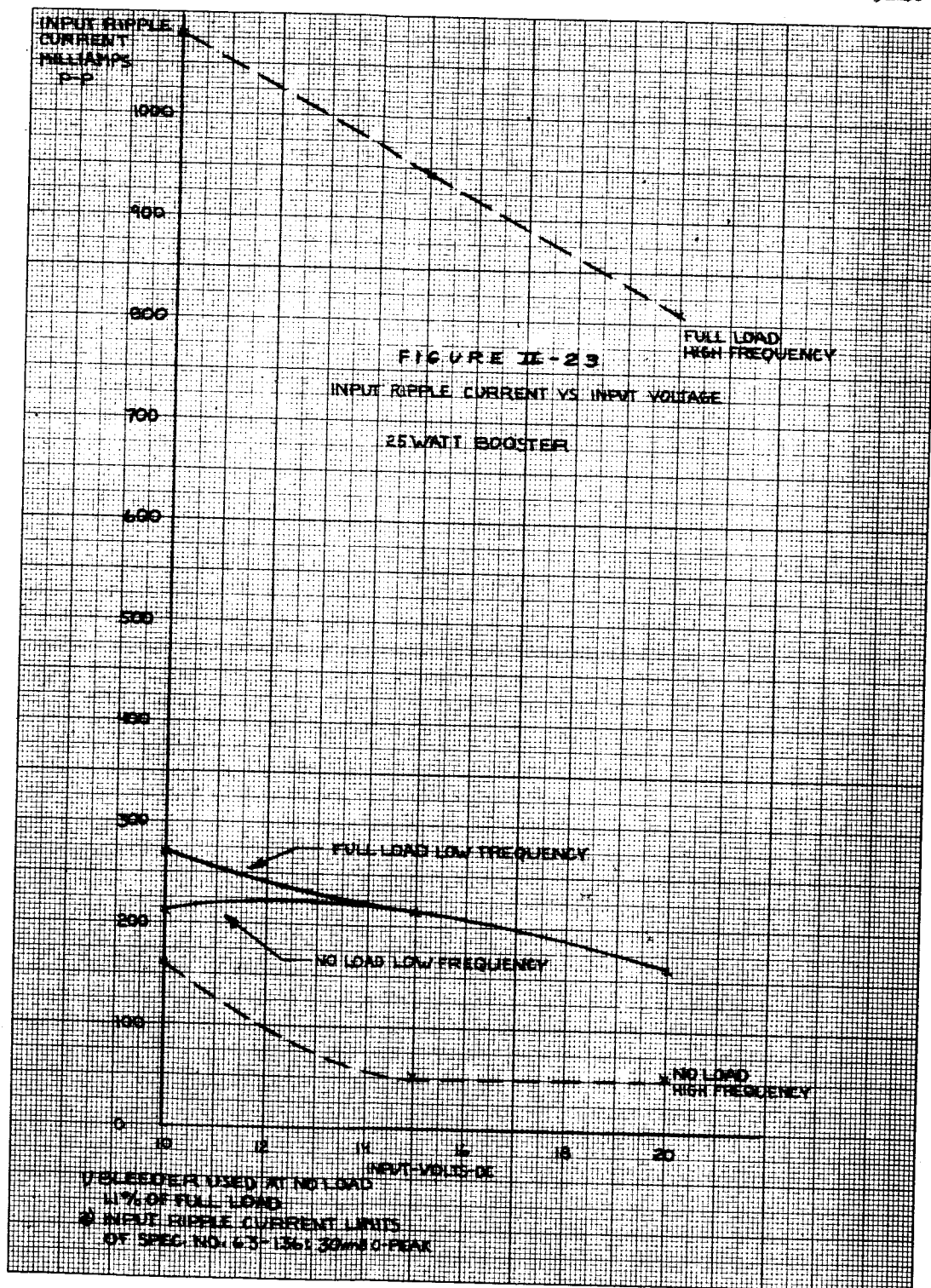
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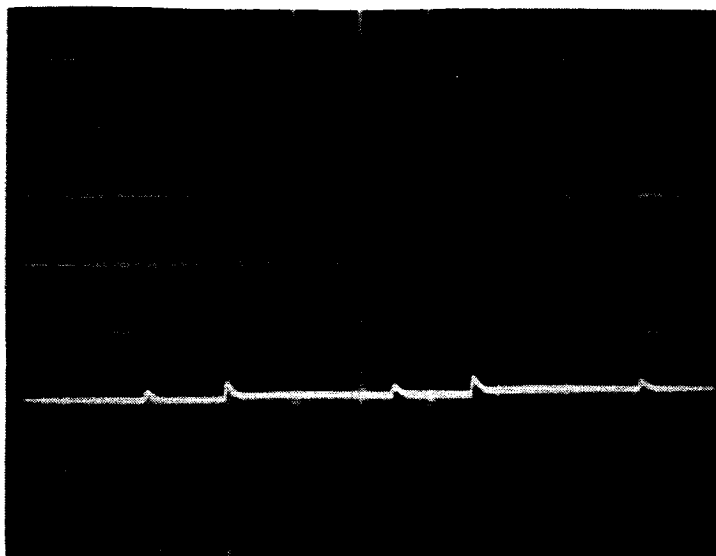
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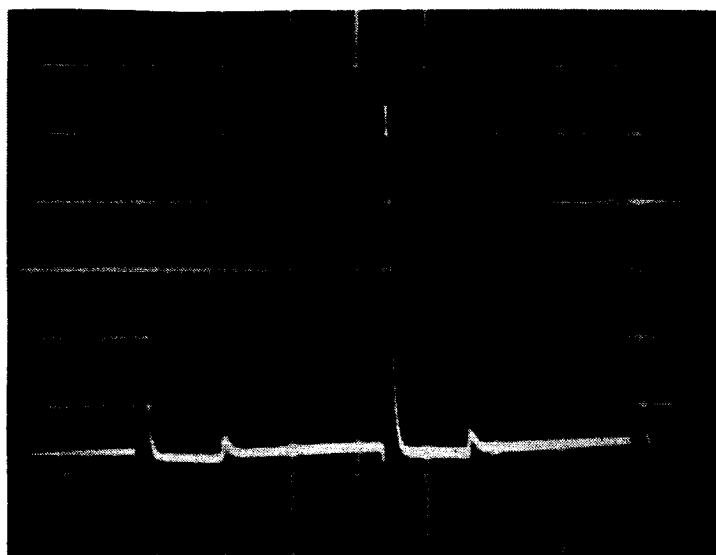
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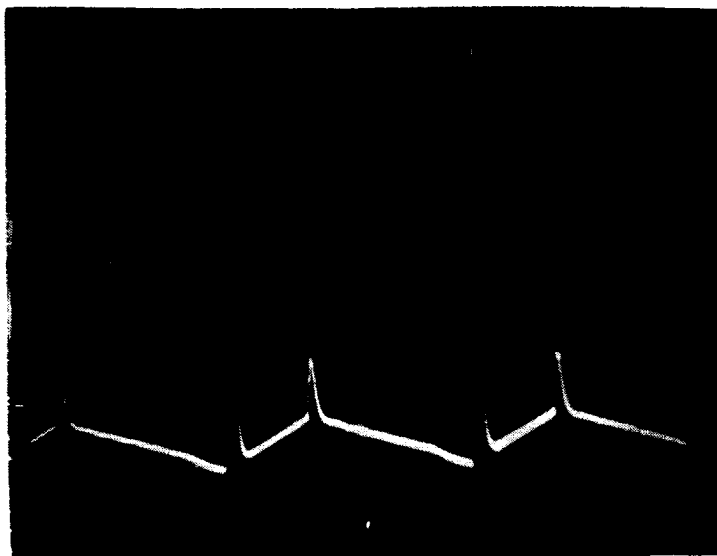


Output Voltage Ripple At No Load - 15 Volt Input
Vertical Scale - .1 Volt/cm
Horizontal Scale - 10 u sec/cm

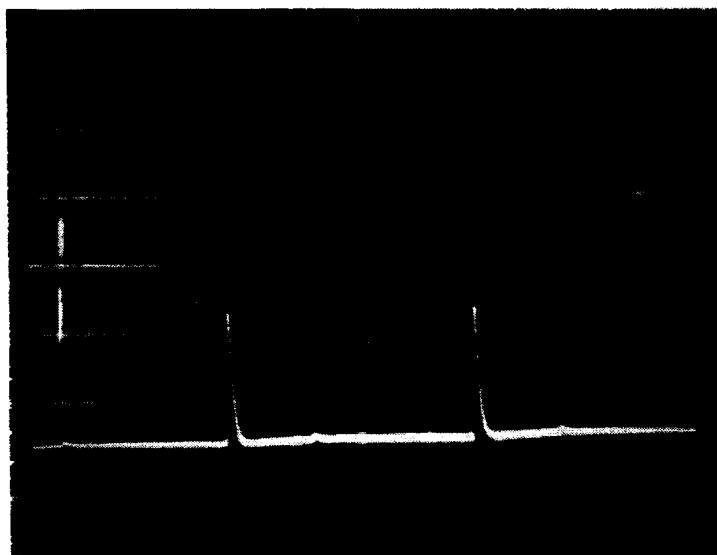


Output Voltage Ripple At Full Load - 15 Volt Input
Vertical Scale - 1.0 Volt/cm
Horizontal Scale - 10 u sec/cm

Figure II-24 Output Ripple Voltage 25 Watt Booster



Input Ripple Current At No Load - 15 Volt Input
Vertical Scale .27 Amps/cm
Horizontal Scale - 10 μ sec/cm

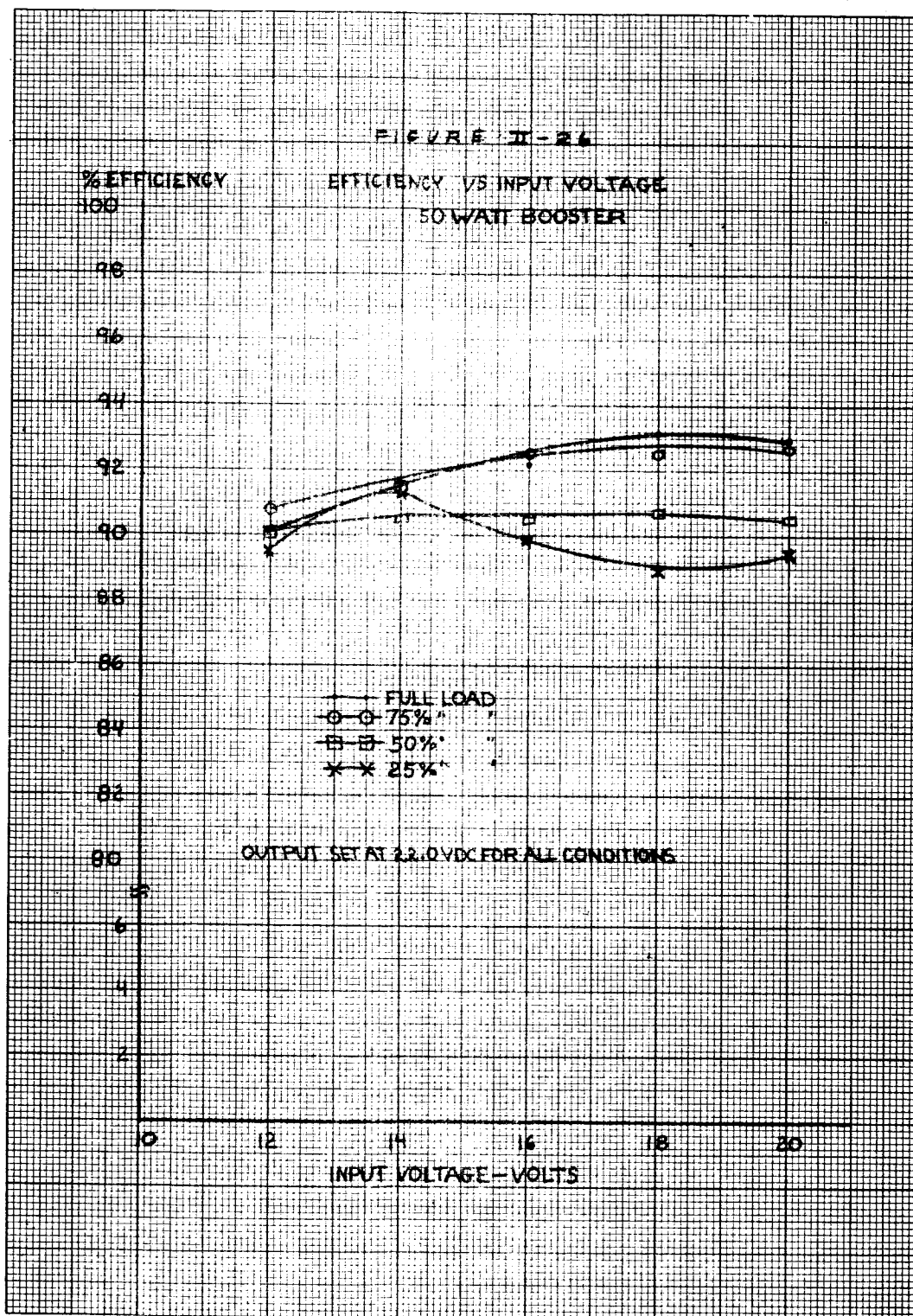


Input Ripple Current At Full Load - 15 Volt Input
Vertical Scale 2.7 Amps/cm
Horizontal Scale - 10 μ sec/cm

Figure II-25 Input Ripple Current 25 Watt Booster

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FIGURE II-27

OPEN LOOP VOLTAGE REGULATION
FOR LINE
50 WATT BOOSTER

OUT PUT
VOLTS

23.0

22.8

22.6

22.4

22.2

22.0

21.8

21.6

FULL LOAD

NO LOAD

NO LOAD

$\frac{3}{4}$ LOAD

$\frac{1}{2}$ LOAD

$\frac{1}{4}$ LOAD

OUTPUT SET AT 22.0VDC
FOR 12VDC INPUT

INPUT-VOLTS

1) BLEEDER USED AT NO LOAD
1/4% OF FULL LOAD

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FIGURE II-2B
OPEN LOOP VOLTAGE REGULATION
FOR LOAD
50WATT BOOSTER

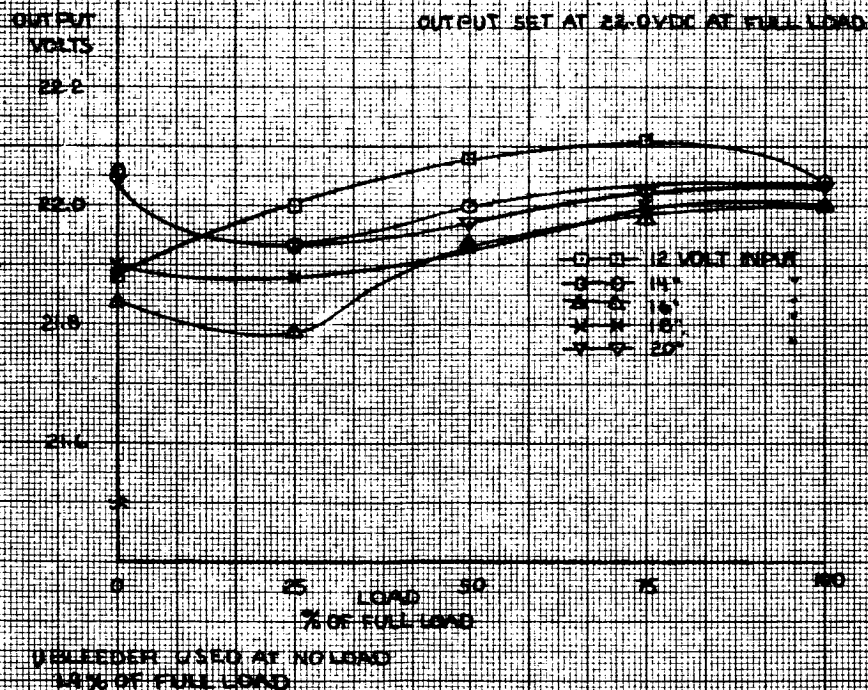
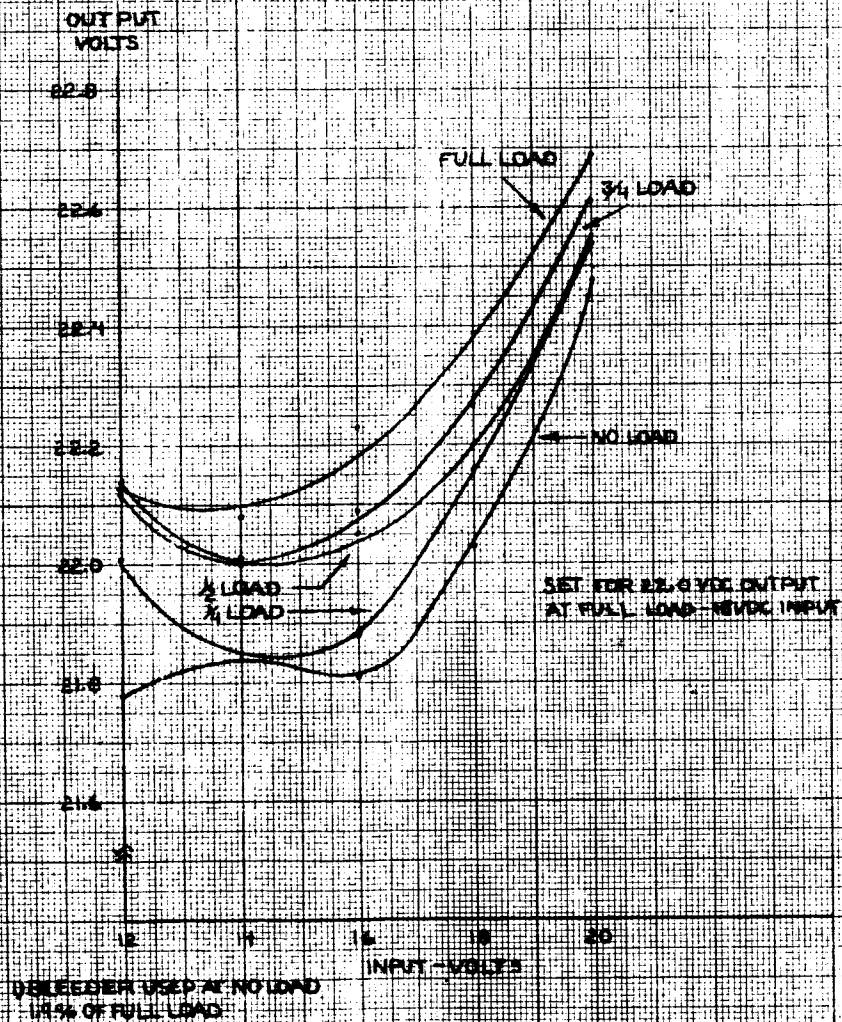


FIGURE II - 20
OPEN LOOP VOLTAGE REGULATION
FOR LINE AND LOAD
50 WATT BOOSTER

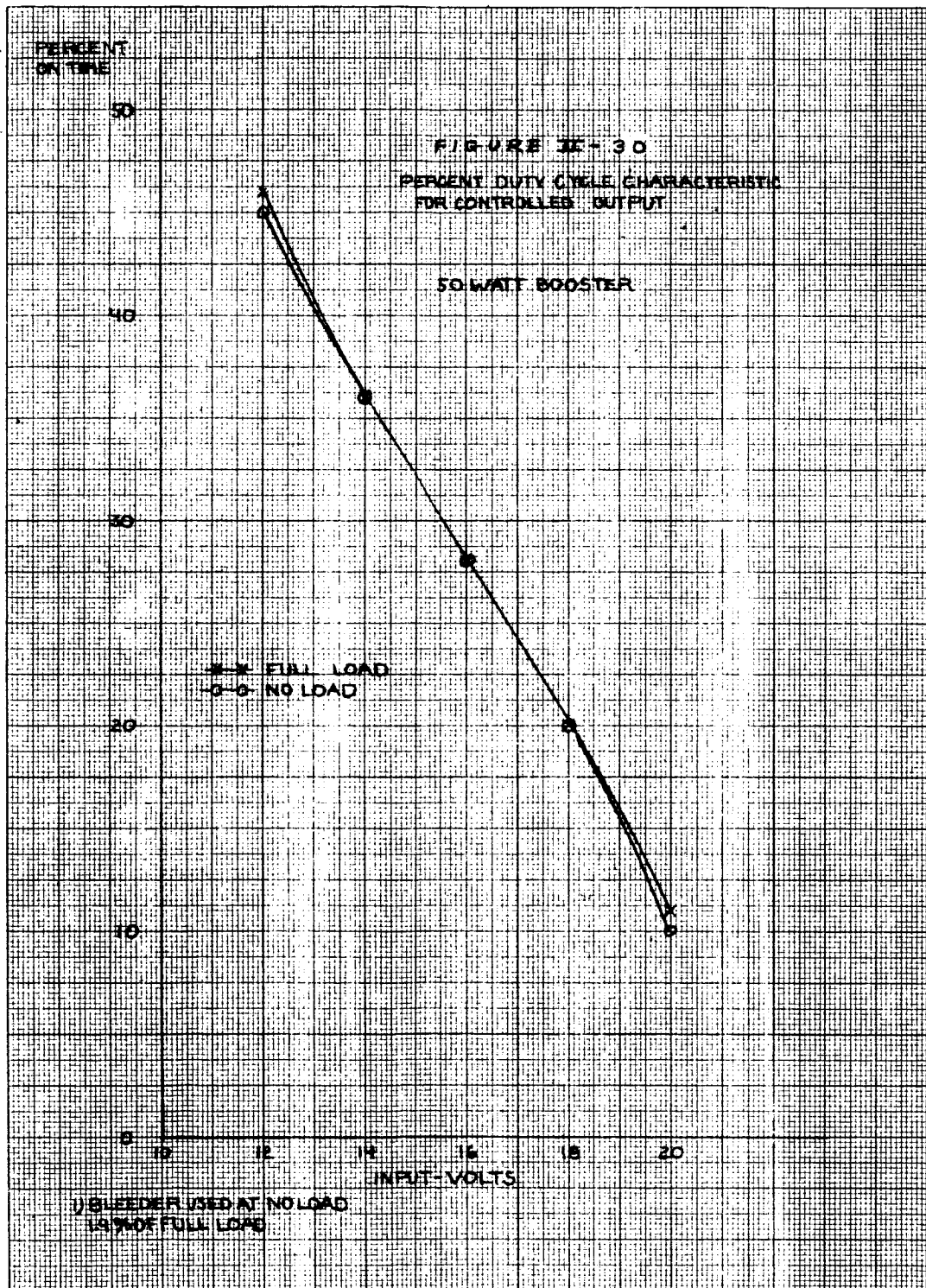


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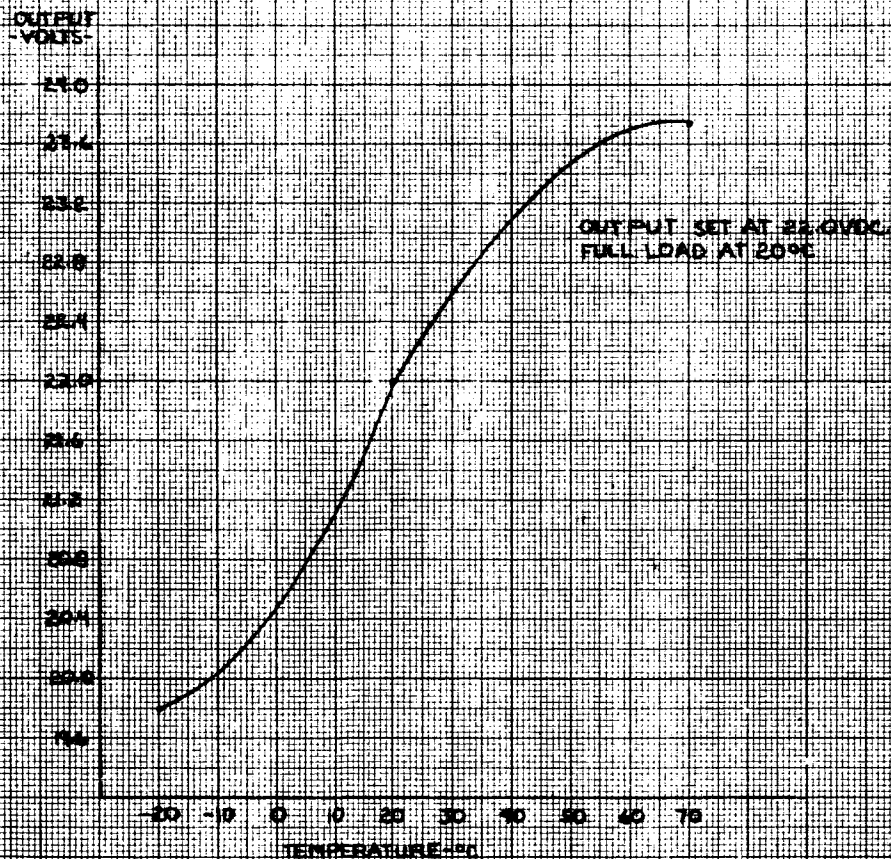
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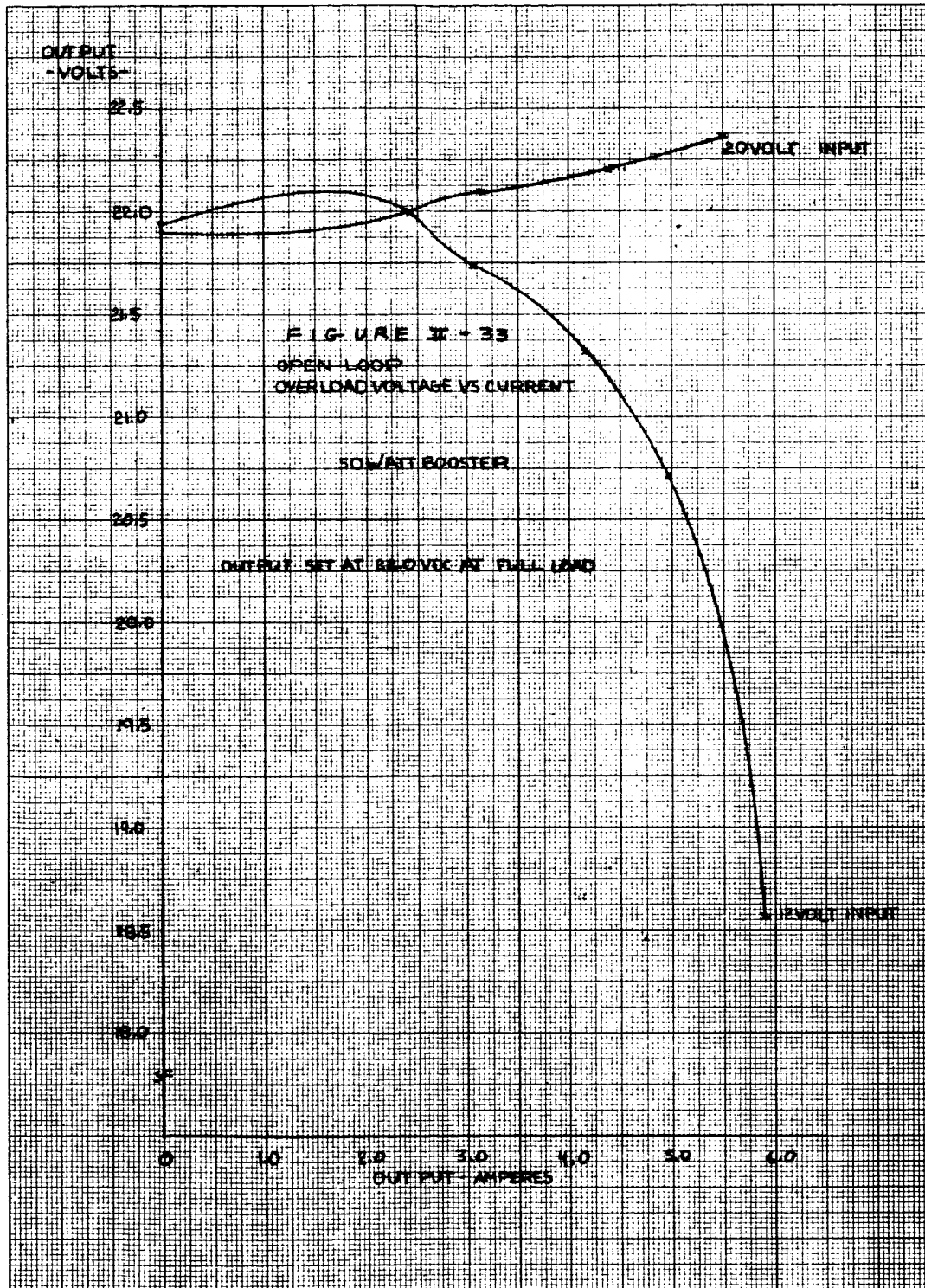


SOWATT EDOSTER



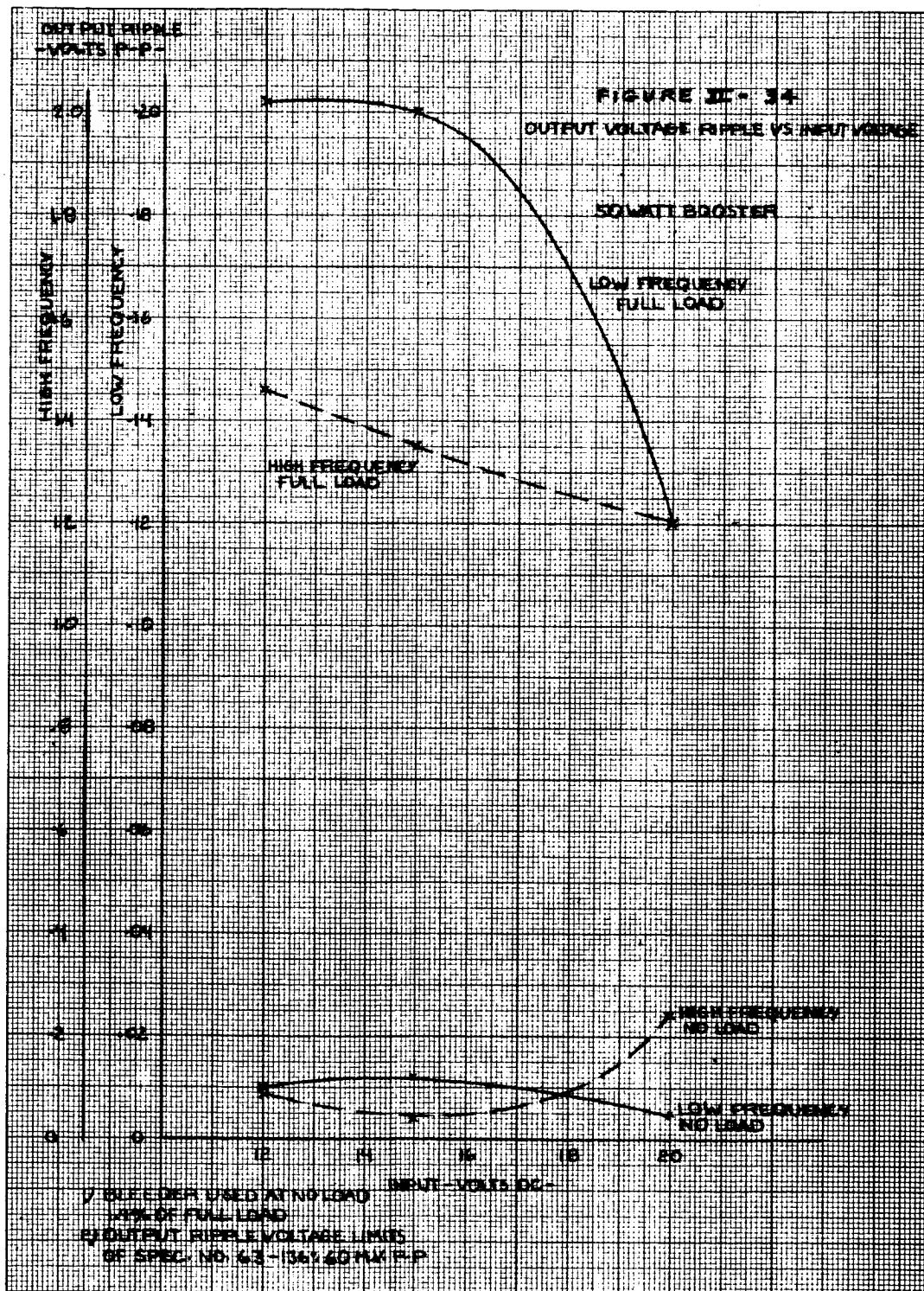
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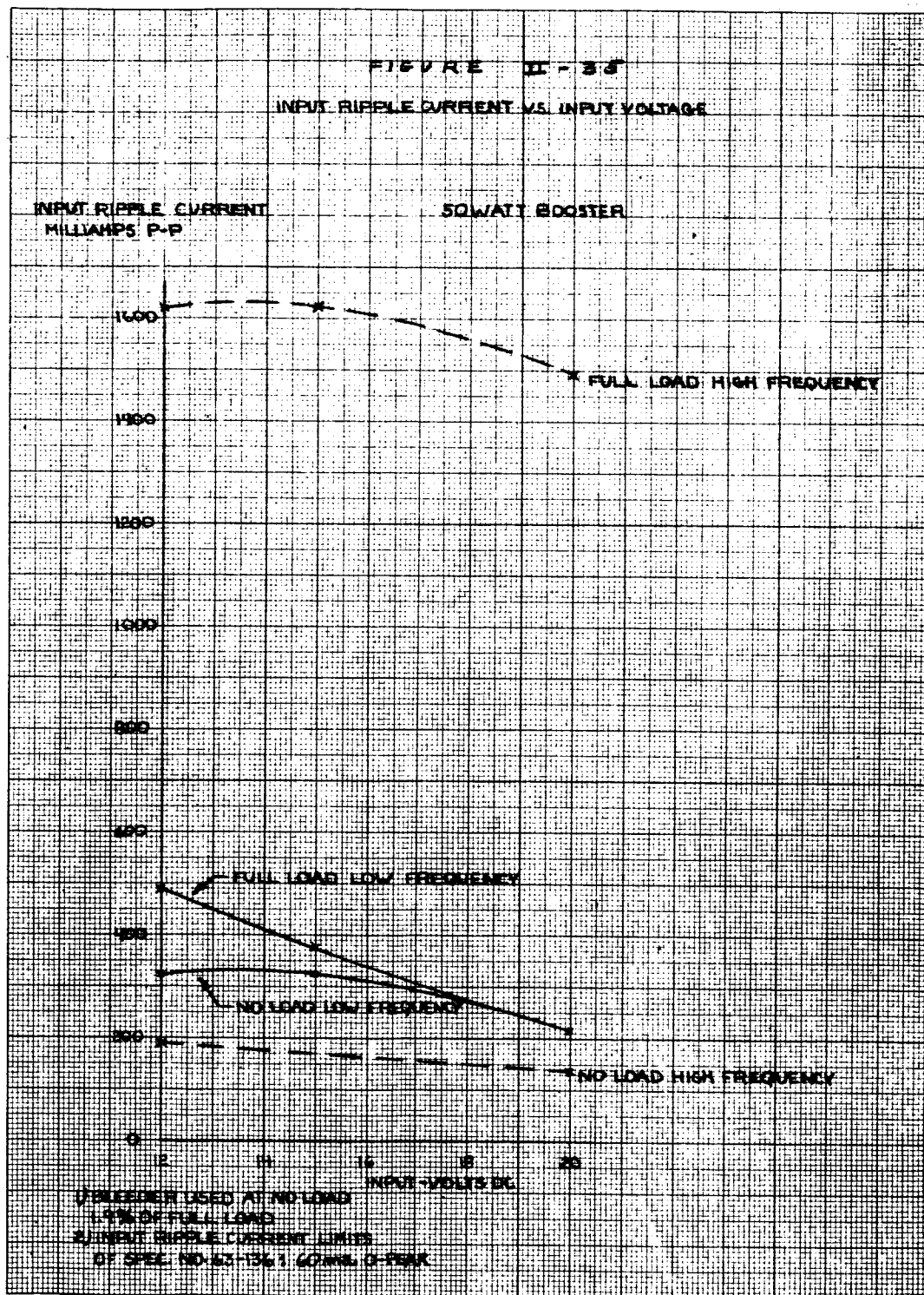
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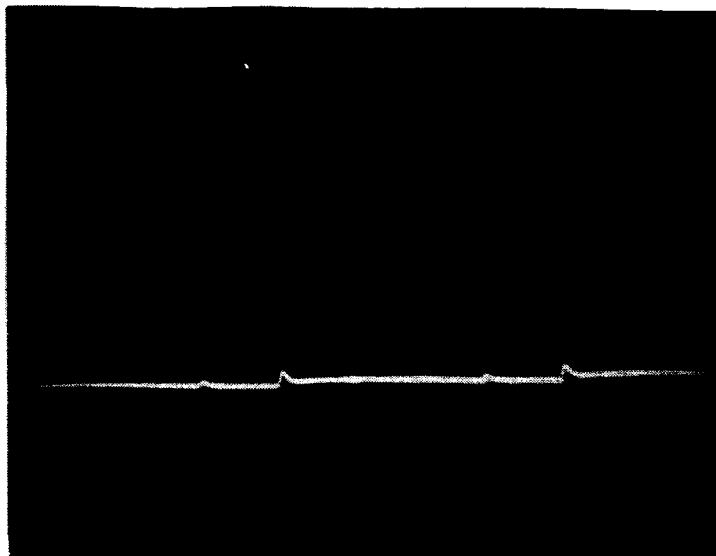


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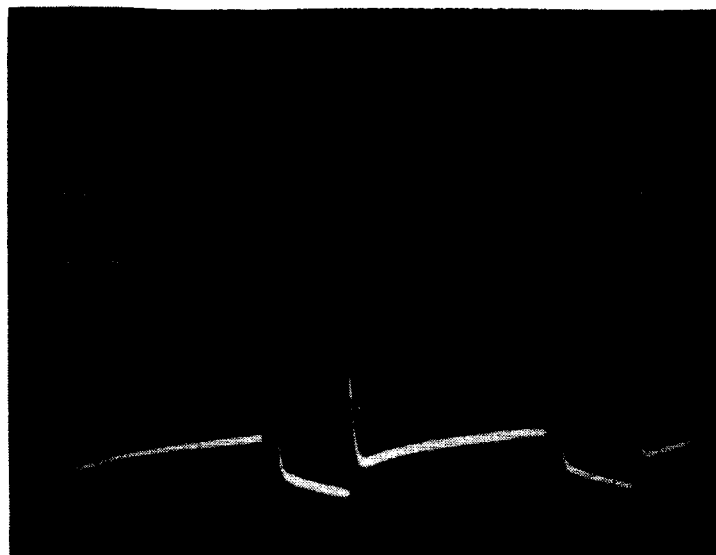
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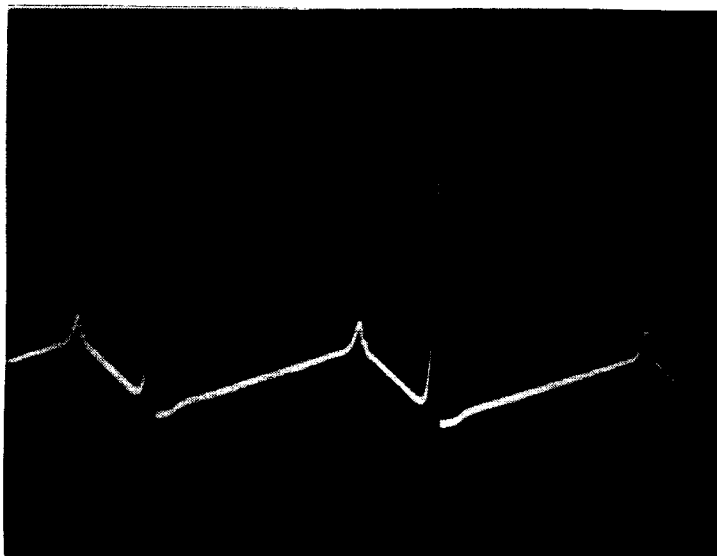


Output Ripple Voltage At No Load - 16 Volt Input
 Vertical Scale - .1 Volt/cm
 Horizontal Scale - 10 μ sec/cm

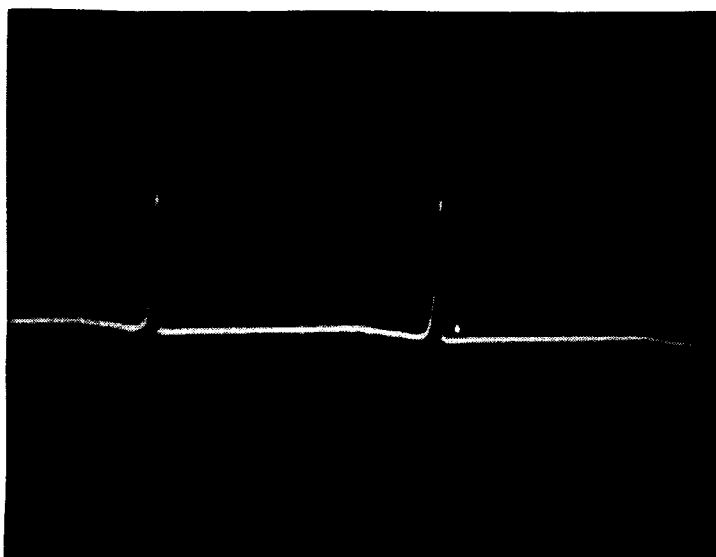


Output Ripple Voltage At Full Load - 16 Volt Input
 Vertical Scale - .2 Volt/cm
 Horizontal Scale - 10 μ sec/cm

Figure II-36 Output Ripple Voltage 50 Watt Booster



Input Ripple Current At No Load - 16 Volt Input
 Vertical Scale - .27 Amp/cm
 Horizontal Scale - 10 μ sec/cm



Input Current At Full Load - 16 Volt Input
 Vertical Scale - 2.7 Amps/cm
 Horizontal Scale - 10 μ sec/cm

Figure II-37 Input Ripple Current 50 Watt Booster

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20 X 20 PER INCH

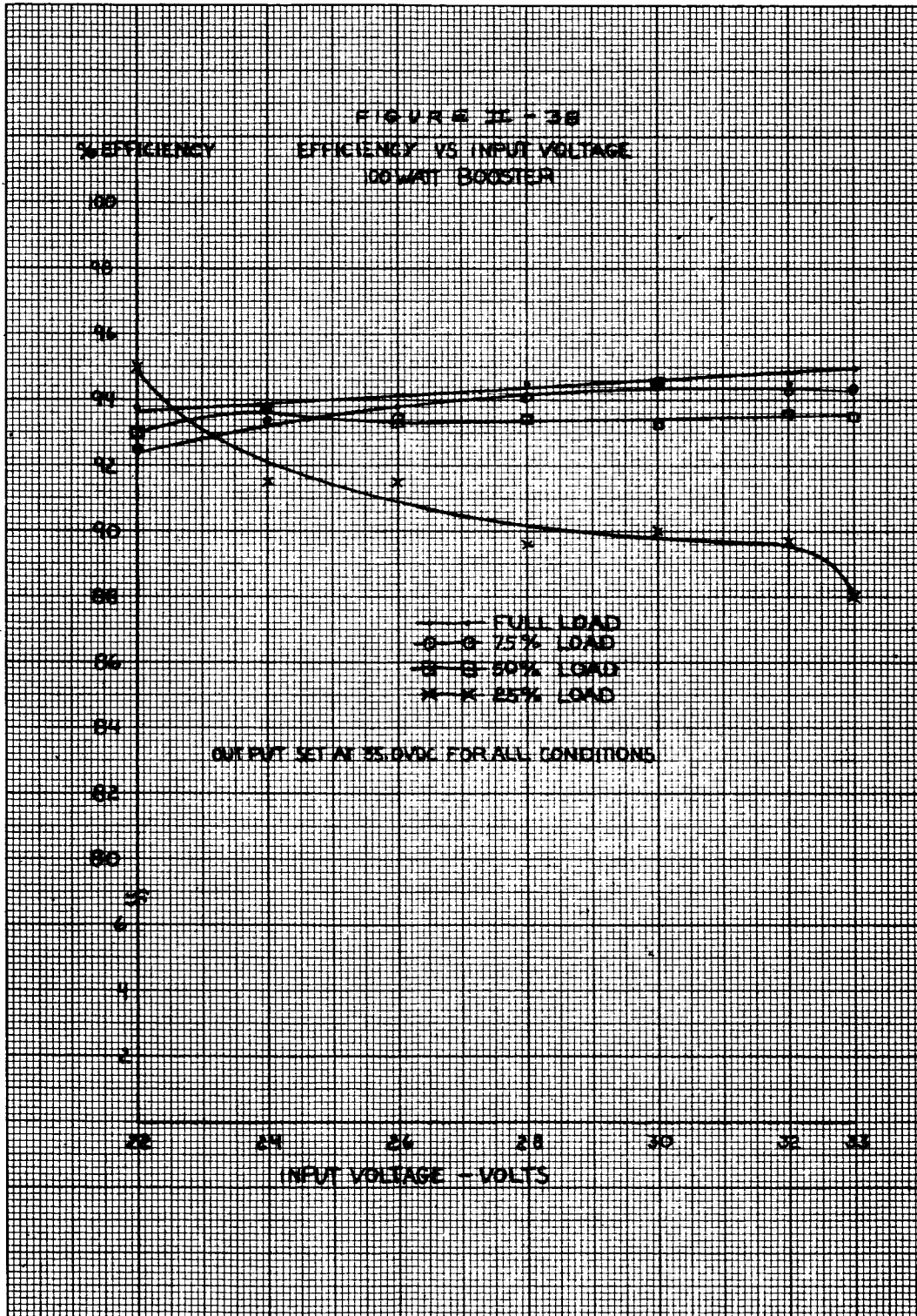
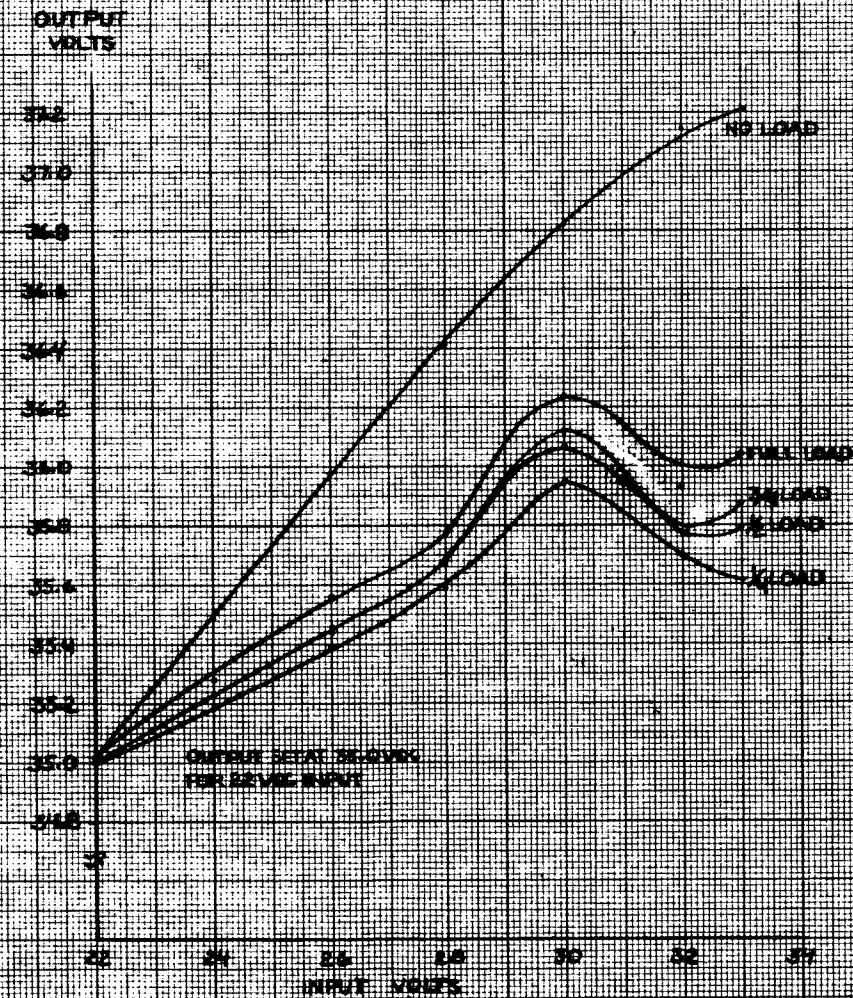


FIGURE II-39
OPEN LOOP VOLTAGE REGULATION
FOR LINE
100 WATT BOOSTER



RESERVED USED AT NO LOAD
25% FULL LOAD

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FIGURE II-4-0
OPEN LOOP VOLTAGE REGULATION
FOR LOAD
100 WATT BOOSTER

OUTPUT
VOLTS

35.0

34.8

34.6

34.4

34.2

34.0

33.8

33.6

33.4

OUTPUT SET AT 35.0VDC AT FULL LOAD

22 VOLT INPUT
24
26
28
30
32
33

0

25

50

75

100

% OF FULL LOAD

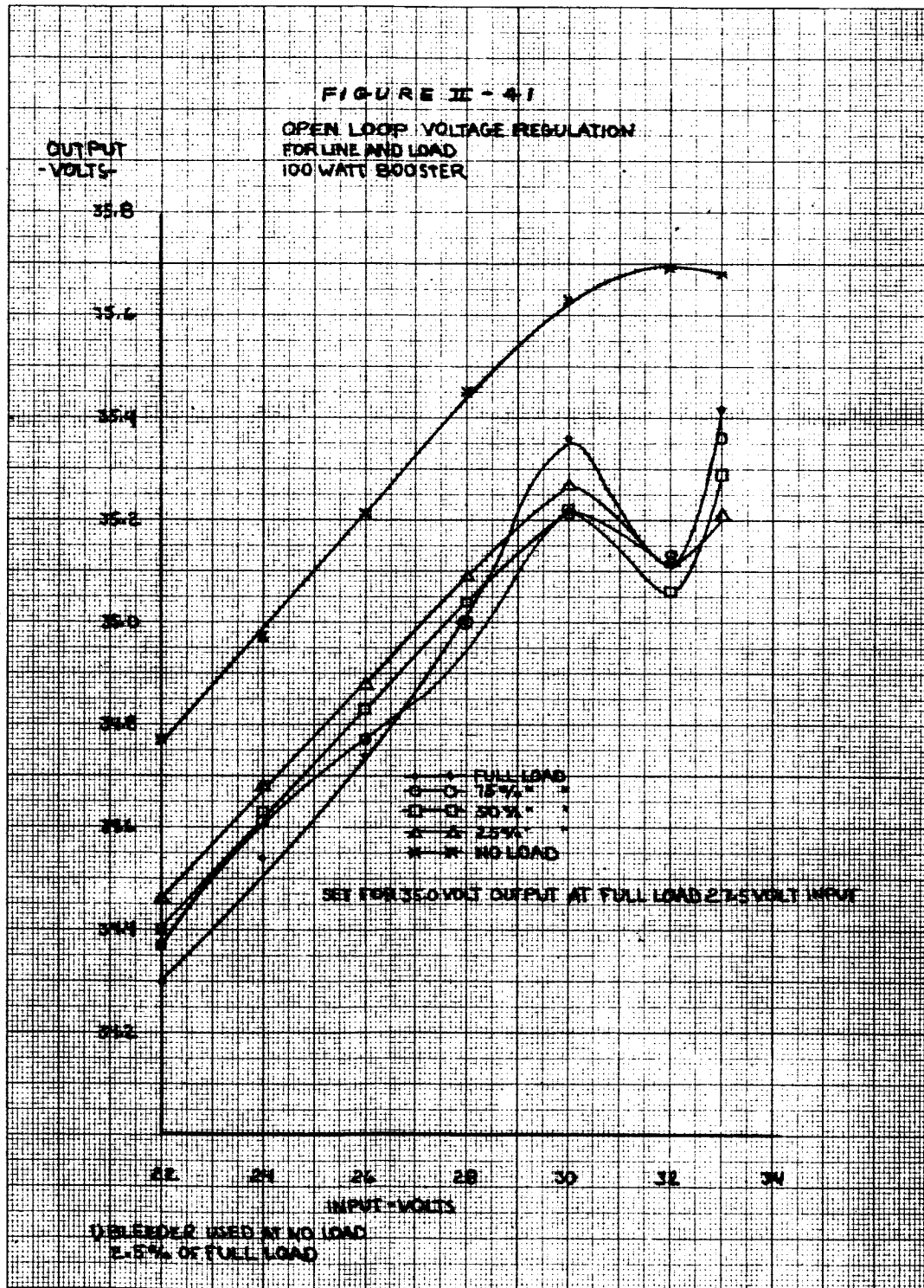
BLEEDER USED AT NO LOAD
2.5% OF FULL LOAD

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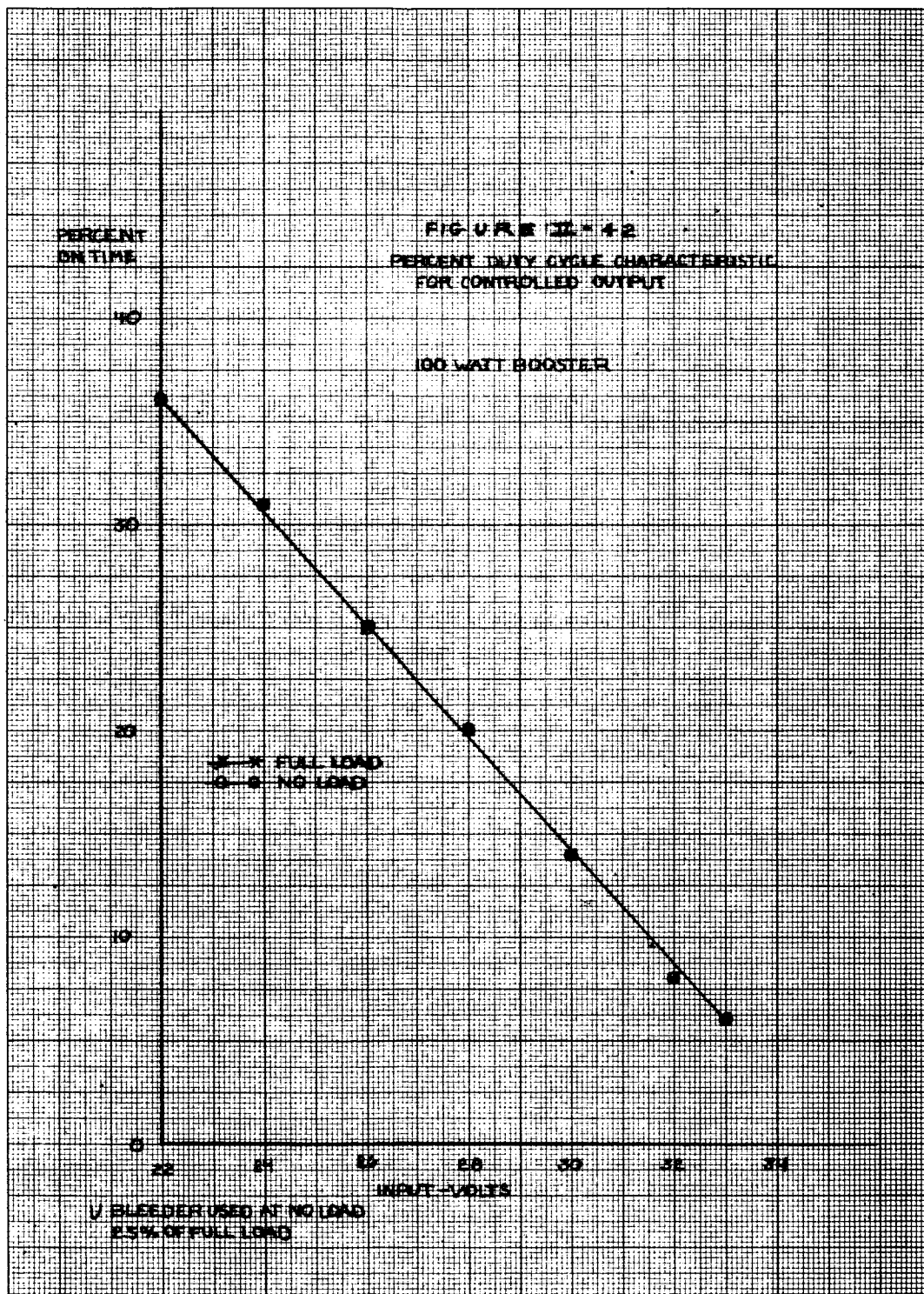
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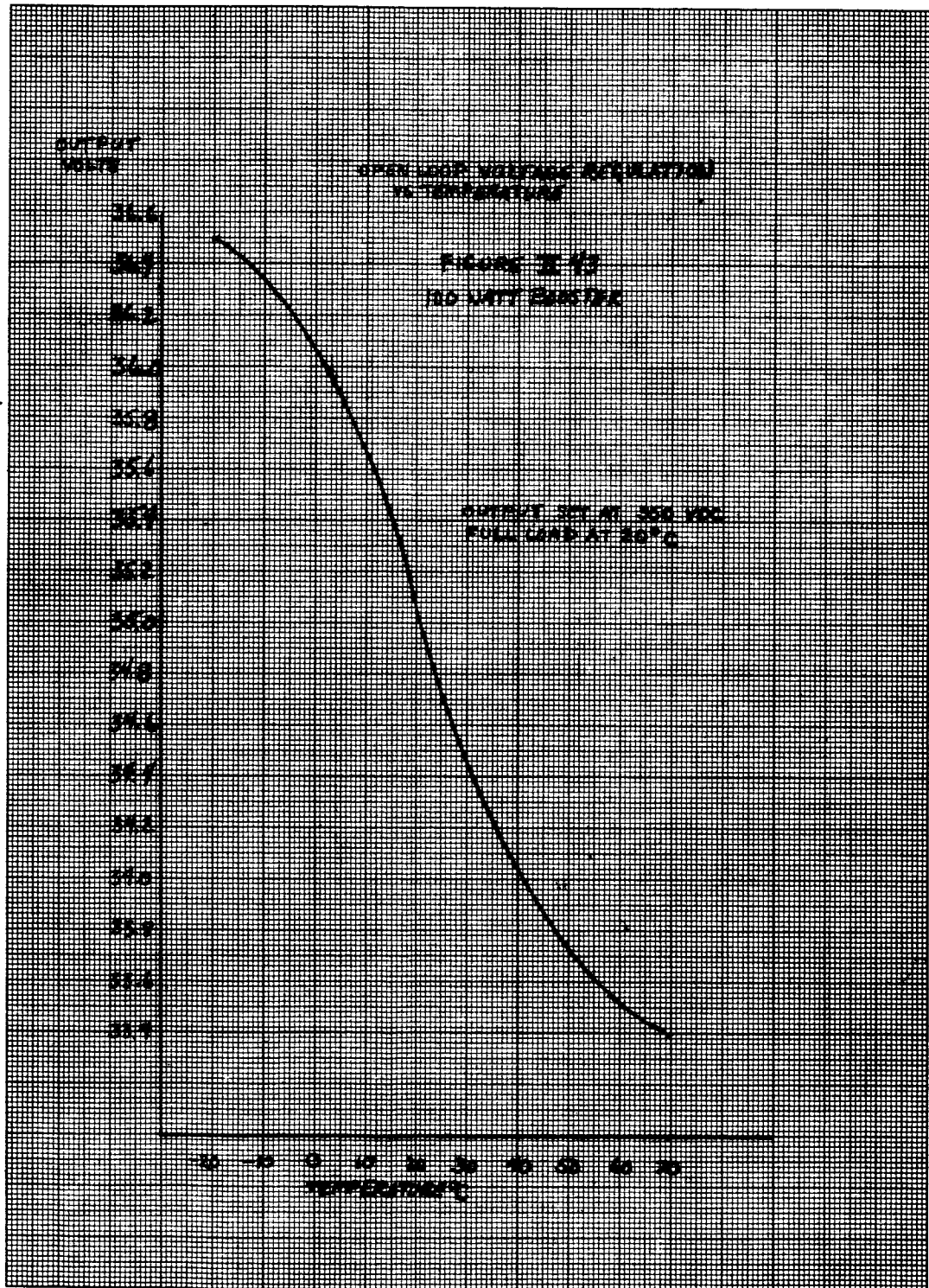


FIGURE II - 44
OUTPUT VOLTAGE STABILITY
100 WATT BOOSTER

OUTPUT
-VOLTS-

35.2

35.1

35.0

34.9

34.8

34.7

34.6

27.5 VOL WPM-FULL LOAD

TIME - HOURS

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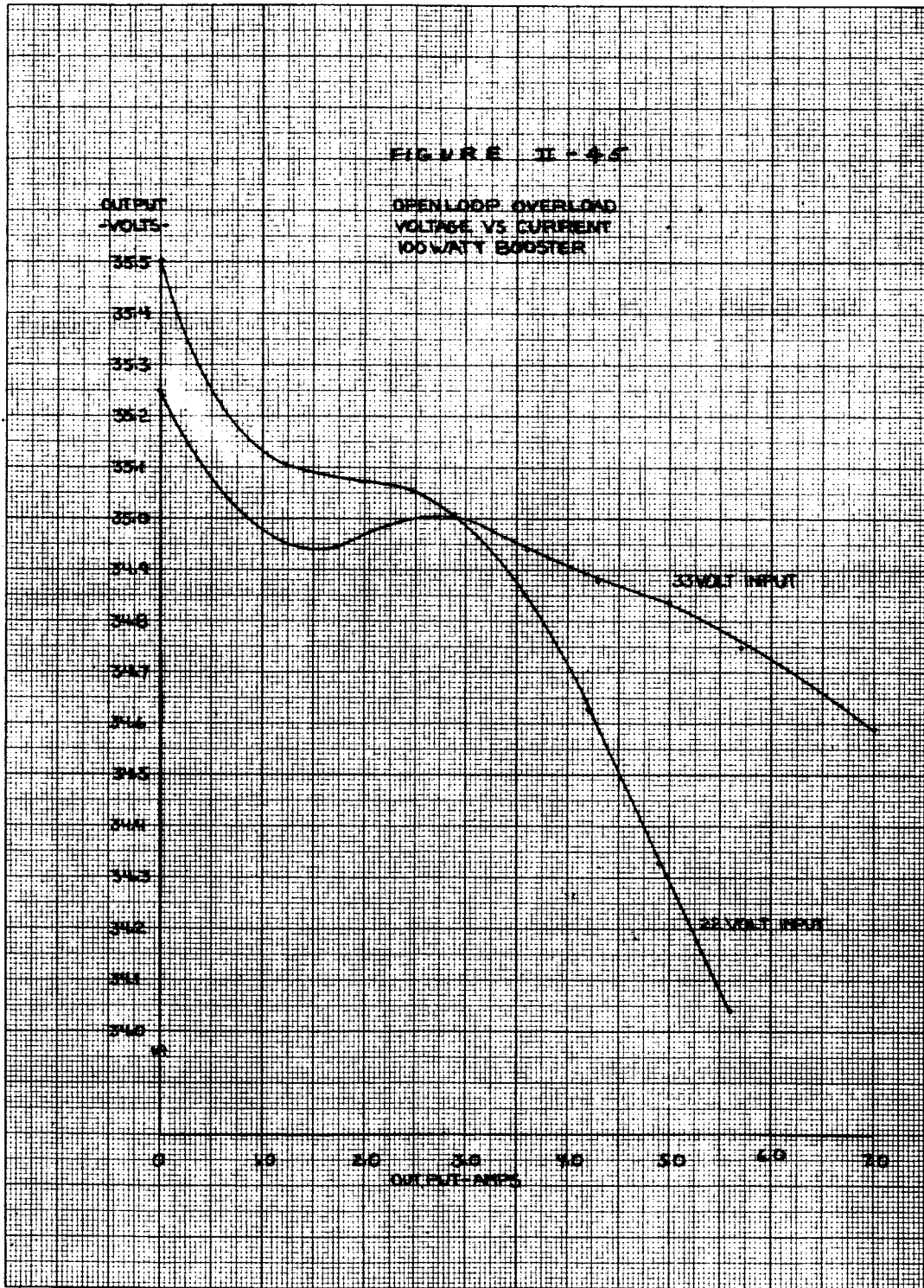
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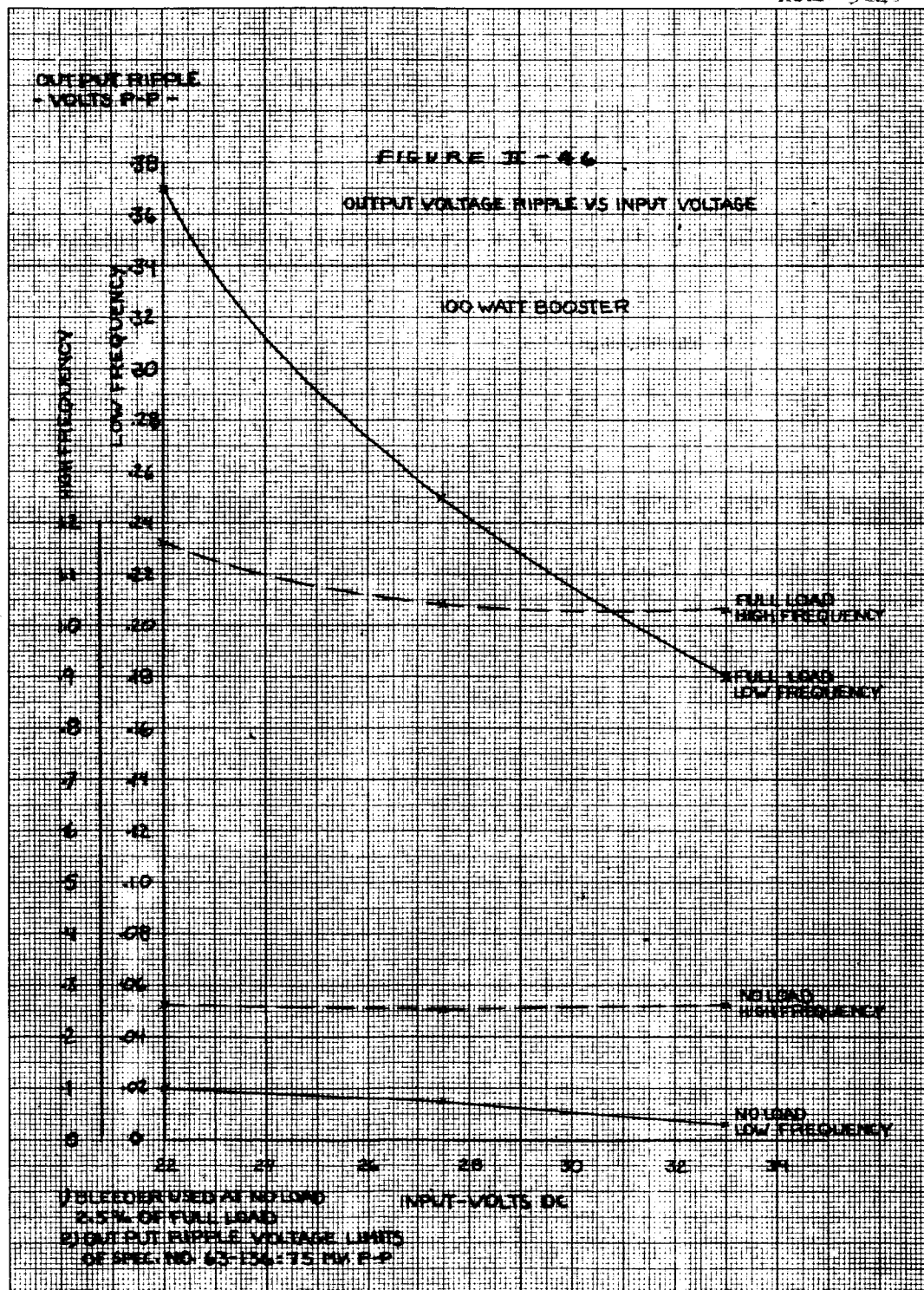
FIGURE II-45

OPENLOOP OVERLOAD
VOLTAGE VS CURRENT
100WATT BOOSTER



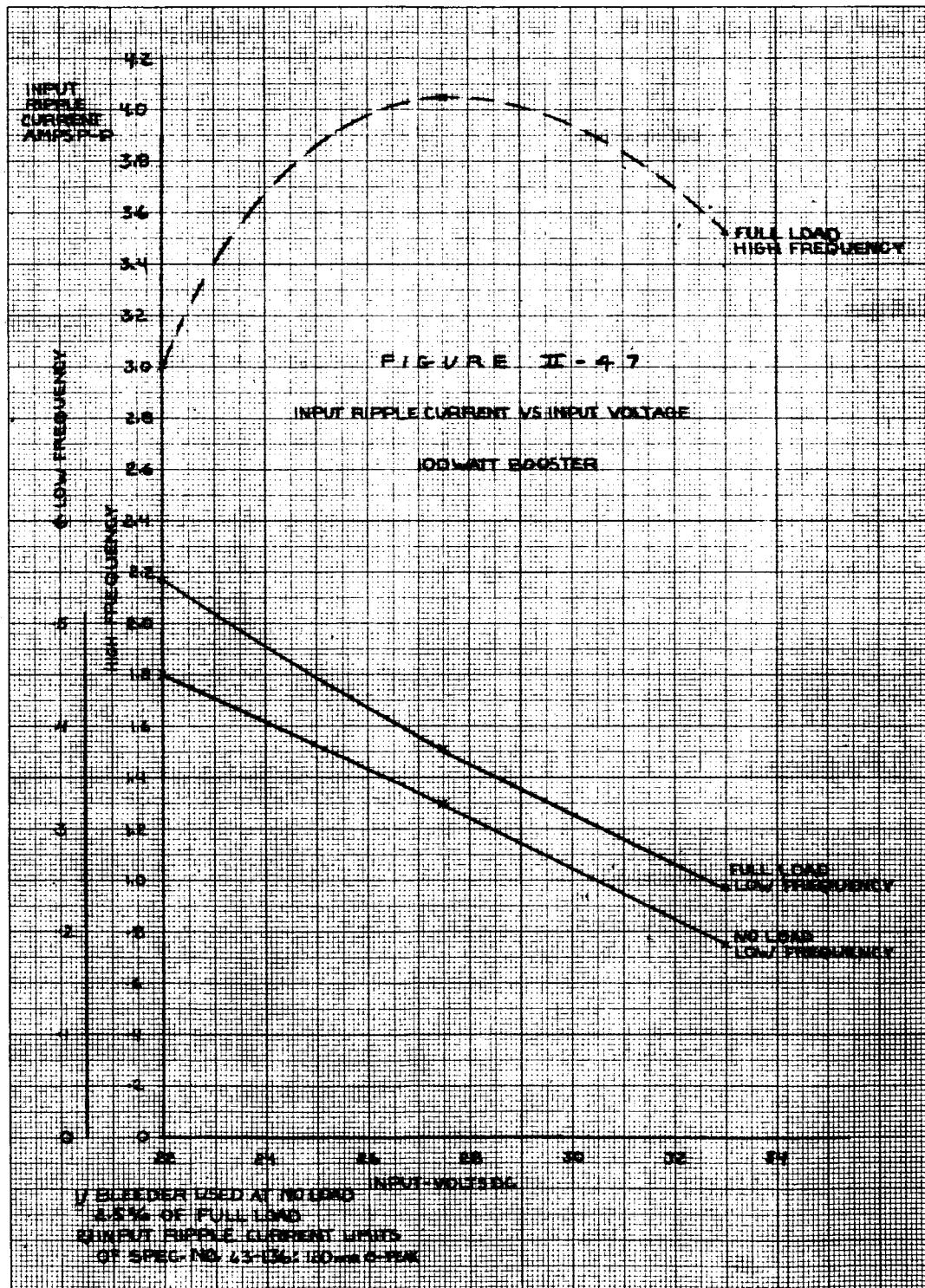
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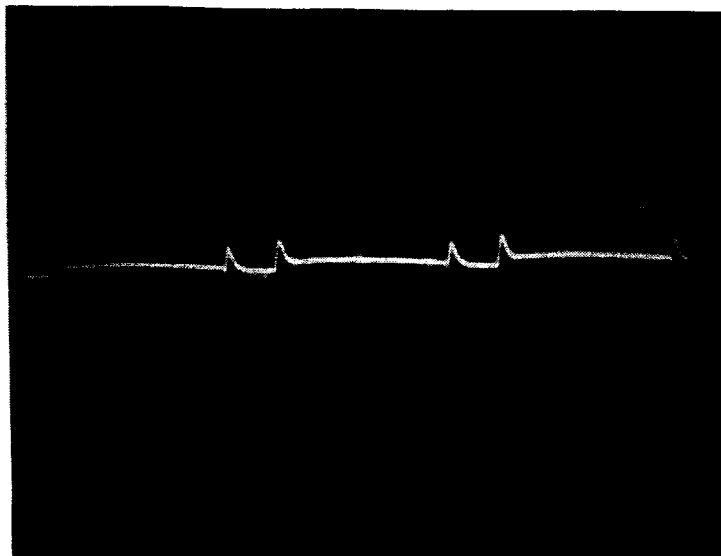
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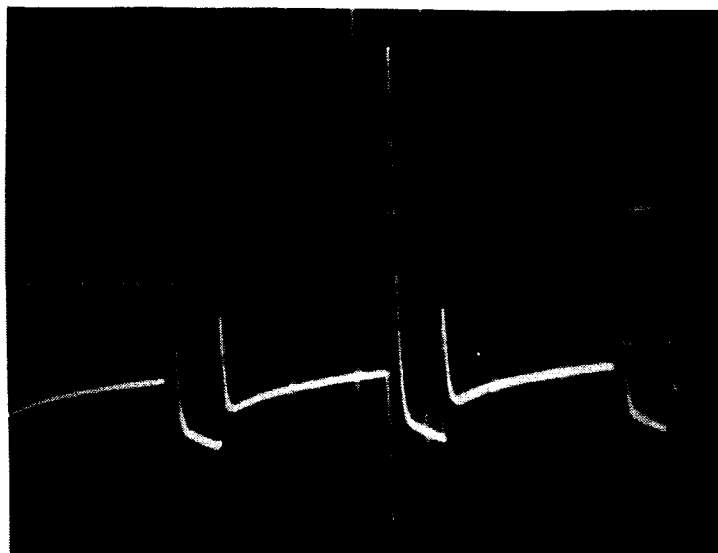
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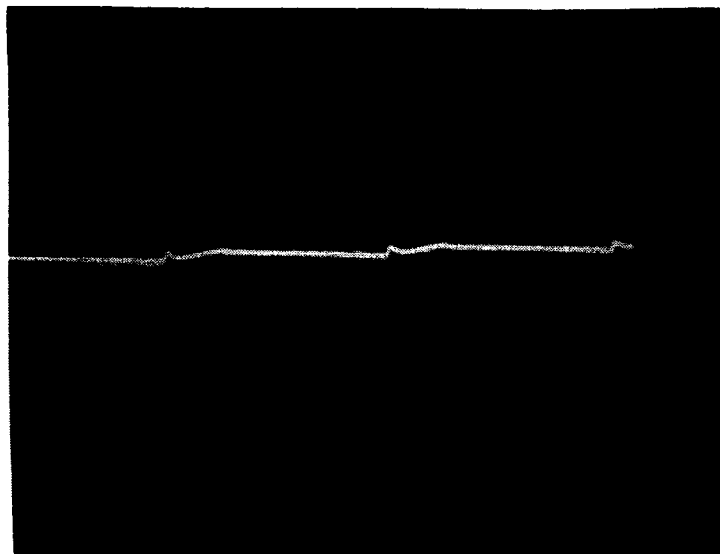


Output Ripple Voltage At No Load - 27.5 Volt Input
 Vertical Scale - .1 Volt/cm
 Horizontal Scale - 10 μ sec/cm

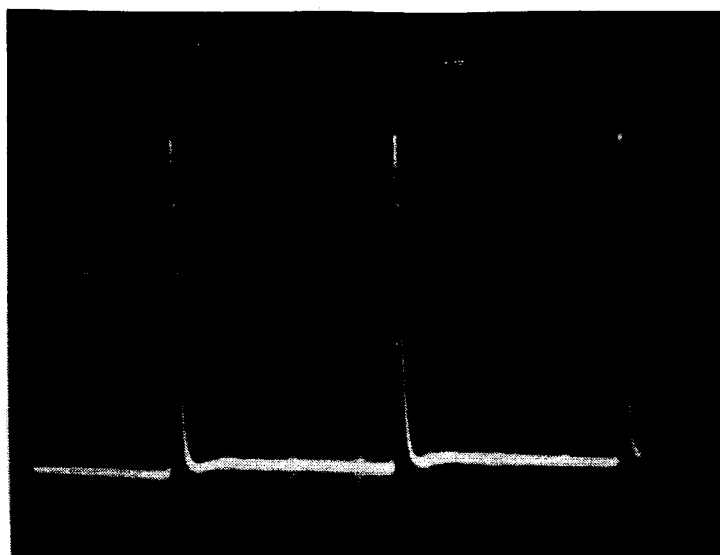


Output Ripple Voltage At Full Load - 27.5 Volt Input
 Vertical Scale - .3 Volt/cm
 Horizontal Scale - 10 μ sec/cm

Figure II-48 Output Ripple Voltage 100 Watt Booster



Input Ripple Current At No Load - 27.5 Volt Input
 Vertical Scale - 2.7 Amps/cm
 Horizontal Scale - 10 μ sec/cm



Input Ripple Current At Full Load - 27.5 Volt Input
 Vertical Scale - 2.7 Amps/cm
 Horizontal Scale - 10 μ sec/cm

Figure II - 49 Input Ripple Current 100 Watt Booster