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DEVELOPMENT AND FABRICATION OF A HIGH POWER SILICON SWITCHING TRANSISTOR

CONTRACT JPL-951303
- FINAL REPORT -
August 1965 to April 1966

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FOREWORD

This report describes the work accomplished under Contract No. JPL-951303, initiated by the Jet Propulsion Laboratory, California Institute of Technology, Pasadena, California. The work was performed at the Westinghouse Semiconductor Division, Youngwood, Pennsylvania.

The project was under the direction of Mr. T. C. New, Manager, Switching Devices Department. The principle investigator was Dr. P. J. Kannam, Advisory Engineer. Contributors include Messrs. P. M. Kisinko, F. G. Ernick and J. J. Steinmetz.

ABSTRACT

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High current (I_C = 100 amperes), low saturation ($V_{CE(sat)}$ = 0.2 volt) and low voltage (BV_{CEO} = 20 volts) transistors were fabricated. Two designs were investigated: (1) a modified simultaneously diffused structure; and (2) an epitaxial-diffused structure. The encapsulation was redesigned to allow the saturation requirement to be achieved. The feasibility of the subject transistor has been demonstrated with samples substantiating the objective specifications.

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I. INTRODUCTION

A. SPECIFICATIONS

Absolute Maximum Ratings

Collector to emitter voltage (BV_{CEO})	20 volts min.
Emitter to base voltage (BV_{EBO})	4 volts min.
Collector current (I_C)	100 amps min.
Base current (I_B)	15 amps min.
Collector dissipation, T_C = 100°C (P_C)	150 watts min.
Thermal resistance, junction to case (O_{JC})	0.5°C/W
Junction temperature range (T_J)	-65 to +175°C

Electrical Characteristics (100°C Case Temperature)

Characteristic	Test Conditions	Min.	Max.	Units
Breakdown voltage (BV_{CEO})	I_C = 100ma[1]	20		volts
Breakdown voltage (BV_{CEO})	I_{EB} = 100ma	1.5		volts
Collector cutoff current (I_{CEX})	V_{CE} = 20V V_{EB} = 1.5V		100	ma
Emitter cutoff current (I_{EBO})	V_{EB} = 1.5V		20	ma
DC current gain (h_{FE})	I_C = 75a V_{CE} = 1V	20		
Saturation voltage ($V_{CE(sat)}$)	I_C = 75a I_B = 5a		0.2[2]	volts
Saturation voltage ($V_{BE(sat)}$)	I_C = 75a I_B = 5a		1.4	volts
Total switching time ($t_d + t_r + t_s + t_f$)	I_C = 75a I_B = 5a V_{BE} = 1.5V on turn-off		15	μsec.

NOTES:

1. Manufacturer's standard specifying procedure acceptable.
2. A saturation voltage of 0.1 volt under the above conditions shall be a design goal.
3. Device is to be used in DC to DC converter of parallel configurations. Duty cycle is 50% and operating frequency may be up to approximately 5KC. Operating conditions are either fully saturated or cut off.

B. MAJOR DIFFICULTIES ENCOUNTERED

Three major problems were encountered and subsequently solved during the fabrication of this device.

1. The attainment of a low $V_{CE(sat)}$ in the epitaxial-diffused design was hindered by the effect of the R_{bb}'. To solve this problem, a controlled boron deposition in the P^+ diffusion process was initiated. This involves the deposition of a P^+ layer on top of the P^- base region before the emitter diffusion.

2. An early approach to a plain diffused device attempted to use $(NH_4)_2HPO_4$ and an inverse emitter mask to yield a "mesa" device. This created two difficulties: the $(NH_4)_2HPO_4$ converted the base region from P to N and if the phosphorus diffusion was done in a B_2O_3 atmosphere to prevent this inversion, the drive time was too short and there was no base width. Therefore, a modified single-diffused process was adapted. This is the process described in the report (note especially the section explaining the BBr_3 diffusion and P^+ drive).

3. At first it was felt that the package designed for the NASA (Contract NAS8-5335) 100-amp transistor might be used to encapsulate the subject device. Unfortunately, the high voltage drop in the package made this impossible and necessitated the designing of the package described in Section V.

II. DESIGN CONSIDERATIONS

A. DEVICE DESIGN - ELECTRICAL PARAMETERS

The subject device is a high-current, low-saturation, low-voltage transistor. Most of the design objectives for the proposed device are quite similar to those of standard transistors and do not require detailed consideration here since they are discussed extensively in the literature. The following discussion will therefore be confined to the main goal of obtaining the lowest possible saturation drop and the technical problems of making a large 100-ampere device.

1. Saturation Voltage

Perhaps the most critical design requirement is for an extremely low saturation voltage (0.1 volt) at a collector current of 75 amperes. In order to begin the design, it is necessary to examine the characteristics of a transistor operating under saturation conditions. The peculiar requirements placed on such a transistor will be considered in detail. A transistor in a typical common emitter circuit is shown in Figure 1 . Ordinarily, the collector junction, J_C, is reverse biased and the emitter junction, J_E, is forward biased by the supply voltages as shown. As the base current, I_B, is increased, the collector current, I_C, will also increase. However, if I_C is increased to the point where the $I_C R_L$ drop equals the E_{CC} supply voltage, then J_C is no longer reverse biased but forward biased as shown by the polarity marks. Thus, the saturation voltage, V_{CE}, is the difference between the collector junction voltage and the emitter junction voltage plus the ohmic drops across the collector, emitter and base regions. The ohmic drops can be made small by high doping of these regions. Thus, the important point now is to make the collector and emitter junction voltages equal so the difference between them is small and thus V_{CE} is small.

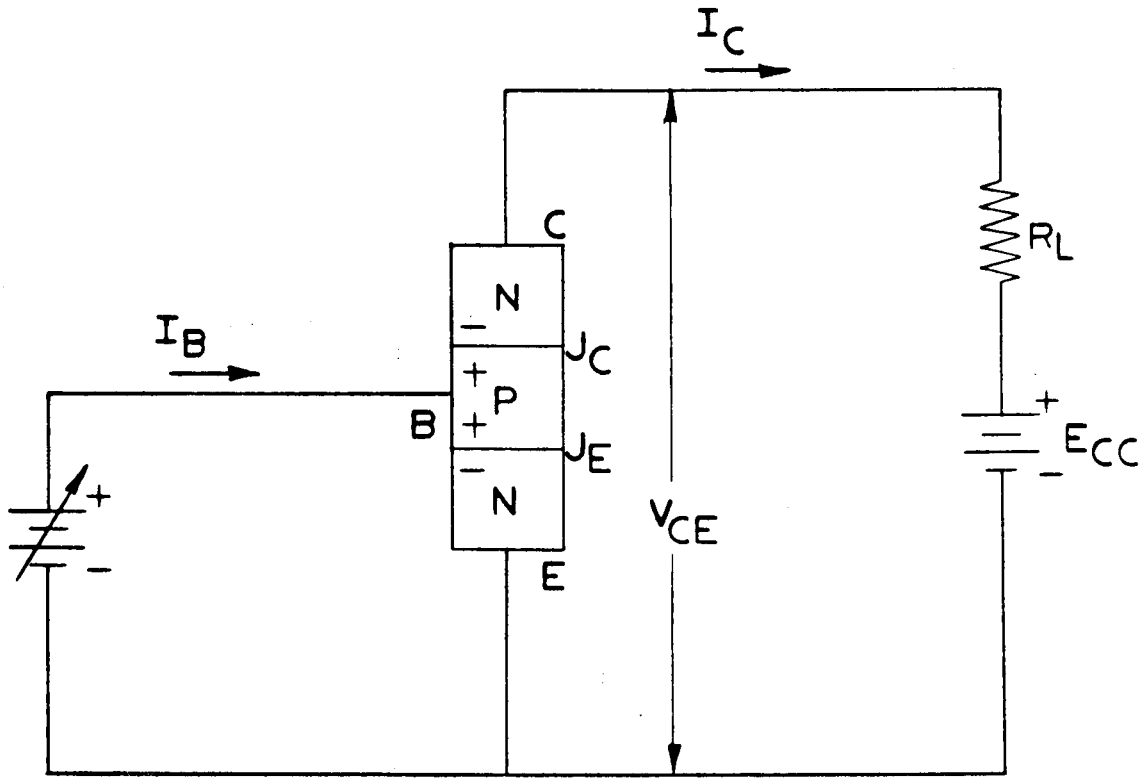

FIGURE 1: Transistor in Typical Common Emitter Circuit

The voltage drop across any junction is determined by the carrier density on each side of it. In a transistor with collector and emitter junctions adjacent to each other, this voltage is related to the normal and inverted alphas as given by Ebers and Moll[1]. Thus, making the collector and emitter junction voltages equal, requires equal doping in the emitter and collector regions. It is also essential to have a small base width so that the injected carrier density recombination loss from the emitter is small and almost the same at the collector. This is the same as keeping the base current small so that the collector and emitter currents are almost equal. Thus, the conditions at the emitter and collector will be nearly the same and the voltages will be alike. These are the reasons that a symmetrical transistor is favored, or rather required, for low saturation drop.

A second requirement for a low saturation voltage becomes evident when the equivalent circuit of an ordinary transistor with collector-base contact overlap is examined. The equivalent circuit and the overlap are shown in Figure 2 .

When V_{CC} in Figure 2 is less than V_{BE} minus the forward drop of the diode D, diode D will start to conduct and the current will start to flow through diode D. Thus, the external base current, I_{BT}, is no longer the only true base current, I_B, and an increase in V_{BE} in this mode will only pass more current through the diode. Thus, I_C is not affected by this action since only I_B can change I_C. The saturation voltage cannot be decreased further and thus V_{CE} is essentially clamped to V_{BE}.[2]

It is obvious that the voltage drop across R_{bb}' increases the saturation voltage if the impedance in the diode branch is low.

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(1) Ebers and Moll, PIRE, V. 42, p. 1761, Dec. 1954.
(2) H. G. Rudenberg, PIRE, p. 1304, June 1958.

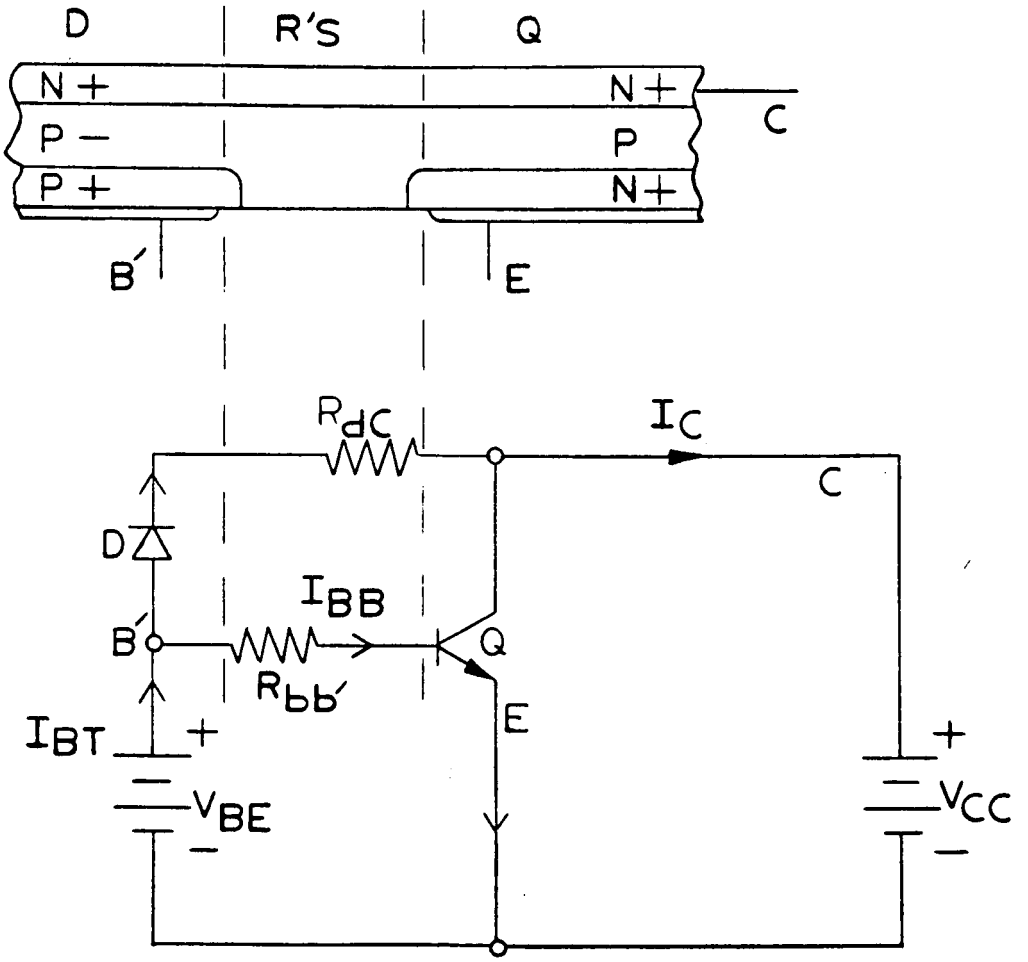

FIGURE 2: Equivalent Circuit and Collector-Base Contact Overlap

In summary, the above discussion indicates that this diode effect will be minimized if $R_{bb'}$ is eliminated and/or the diode equivalent drop is increased. At the same time, the forward and inverse alphas should be maximized. This requires heavy symmetrical doping for emitter and collector and a narrow but sufficiently highly-doped base region.

2. Current Gain

The current gain of a transistor can be written as

$$\alpha = \gamma \beta$$

assuming a collector efficiency of unity, where

γ = emitter efficiency
β = base transport factor.

The current transfer ratio is

$$h_{FE} = \frac{\alpha}{1 - \alpha} .$$

For transistors with fairly narrow base width, the transport factor is close to unity and, hence, the factor that influences most of the current gain is the injection efficiency γ. In the case of diffused transistors γ is mainly determined by surface concentrations, diffusion depths, lifetime of the minority carriers and the drift field intensity. The dependence of γ on these parameters can be determined by solving the steady state continuity equation for known boundary conditions. This analysis has been done at Westinghouse using a computer program. The pertinent equations for this program are given in the Appendix. The program computes the injection efficiency, the transport factor and current transfer ratio for given values of surface concentrations, diffusion length and junction depths, taking into consideration the effect due to drift field also. At low-level injection, the drift field is due to built-in concentration gradient, and at high level the drift field is mainly due

to the injection carriers. Another important area that needs consideration is the effect of lateral resistance on the current gain of the device. The base layer doping distribution should be maximized to achieve the lowest possible base resistance.

In general, emitter efficiency and current gain tend to increase with emitter current as recombination consumes less of the injected current, and to decrease at high current levels due to an effective increase of carrier concentration in the base (conductivity modulation). These effects combine to give a gain characteristic which is low at very low current, rises to a maximum at moderate currents, and falls off at high currents. Gain at very high current is determined largely by emitter edge length, since the transverse voltage drop across the base region leads to crowding of current to the emitter edges.(3) For the best utilization of total device area at high currents, the ratio of emitter edge length to emitter area must be reasonably large. Westinghouse power transistor designs employ multiple ring structures for this purpose. Other means of achieving this end in the industry include interdigitated or comb structures and various types of star structures. Theory and experience both indicate that the current density per unit of emitter edge length should be on the order of 4-5 amperes per inch. Thus, the subject 100-ampere transistor will require some 20-25 inches of emitter edge.

The control of gain at low and moderate currents can be achieved by suitable design of the overall emitter area and of emitter doping level. By increasing the total emitter area, recombination is made a dominant factor up to higher emitter currents; in this way, the peak of the gain curve is lowered in magnitude and shifted to higher current levels. The gain fall-off is thus reduced and saturation voltage is also minimized. The total emitter area should therefore be as large as physical limitations and switching time considerations permit.

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(3) Fletcher, N. H., "Some Aspects of the Design of Power Transistors," PIRE, V. 43, pp. 551-559, May 1955.

The fundamental emitter efficiency can be controlled by the emitter doping level or, in the case of a diffused emitter, by the relative depth of diffusion and the surface concentration, as is well known to the industry. In the subject device, the emitter efficiency will be controlled to the lowest level compatible with gain requirements; i.e., the doping level in the emitter will be high enough to achieve the desired gain, but no higher.

3. Voltage

A complete knowledge of avalanche breakdown characteristics and also the depletion layer properties is essential for the optimum voltage design of transistors. The steps that have to be taken for voltage design are the determination of the net impurity distribution across the device and the solution of the Poisson's equations for the appropriate boundary conditions. A detailed analysis has been made at Westinghouse with the aid of IBM-7094 computer to determine the voltage breakdown characteristics on all possible design parameters. The program written for this analysis computes the avalanche breakdown voltage and the voltage supported by the collector-base junction for the given values of:

a. depletion layer width
b. surface concentration
c. junction depth
d. base width

4. Switching Parameters

The factors that determine the speed of transistors are the delay time (t_d), rise time (t_r), storage time (t_s), and the fall time (t_f). The equations for these parameters are given in the Appendix. The switching characteristics can be determined by solving these equations and can be optimized to meet the 15 μsec. switching requirement. The parameters chosen to meet the saturation voltage, current gain and voltage requirements will also easily be able to meet the switching requirement.

B. SPECIFIC DESIGNS

Several designs of both the epitaxial transistor and the single-diffused version were developed. The finalized designs were: (1) modified single diffused with a diffused P^+ base; (2) epitaxial simultaneously diffused.

1. Modified Single Diffused

In order to achieve the desired profiles and electrical characters, the single-diffused device requires deep, uniform junctions, narrow base widths and high surface concentrations. All these conditions were satisfied by using a P-type substrate, diffusing a P^+ base and N^+ emitter-collectors. The analytical model is shown in Figure 3 and the doping profile in Figure 4.

2. Epitaxial Simultaneously Diffused Model

In this design a P-type epitaxial base is grown on a heavily doped N^+ substrate of high quality silicon. The surface is then masked and etched. This permits the emitter N^+ (phosphorous) to diffuse into the thin epitaxial base region simultaneously with the phosphorous dopant supplied by the substrate to diffuse into the other side of the base region. The cross-section structure of this model is shown in Figure 5 and its doping profile in Figure 6.

C. ENCAPSULATION

In both of the previously mentioned models, the topographical design is similar. The radially symmetrical design as used by the present Westinghouse-NASA 100-amp transistor was adopted initially since it

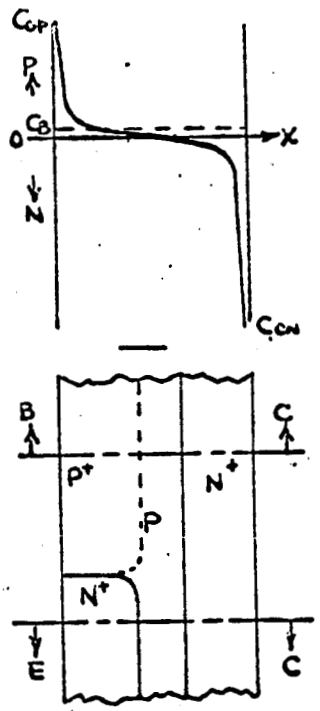

FIGURE 3: Analytical Model of Plain Simultaneously Diffused Transistors

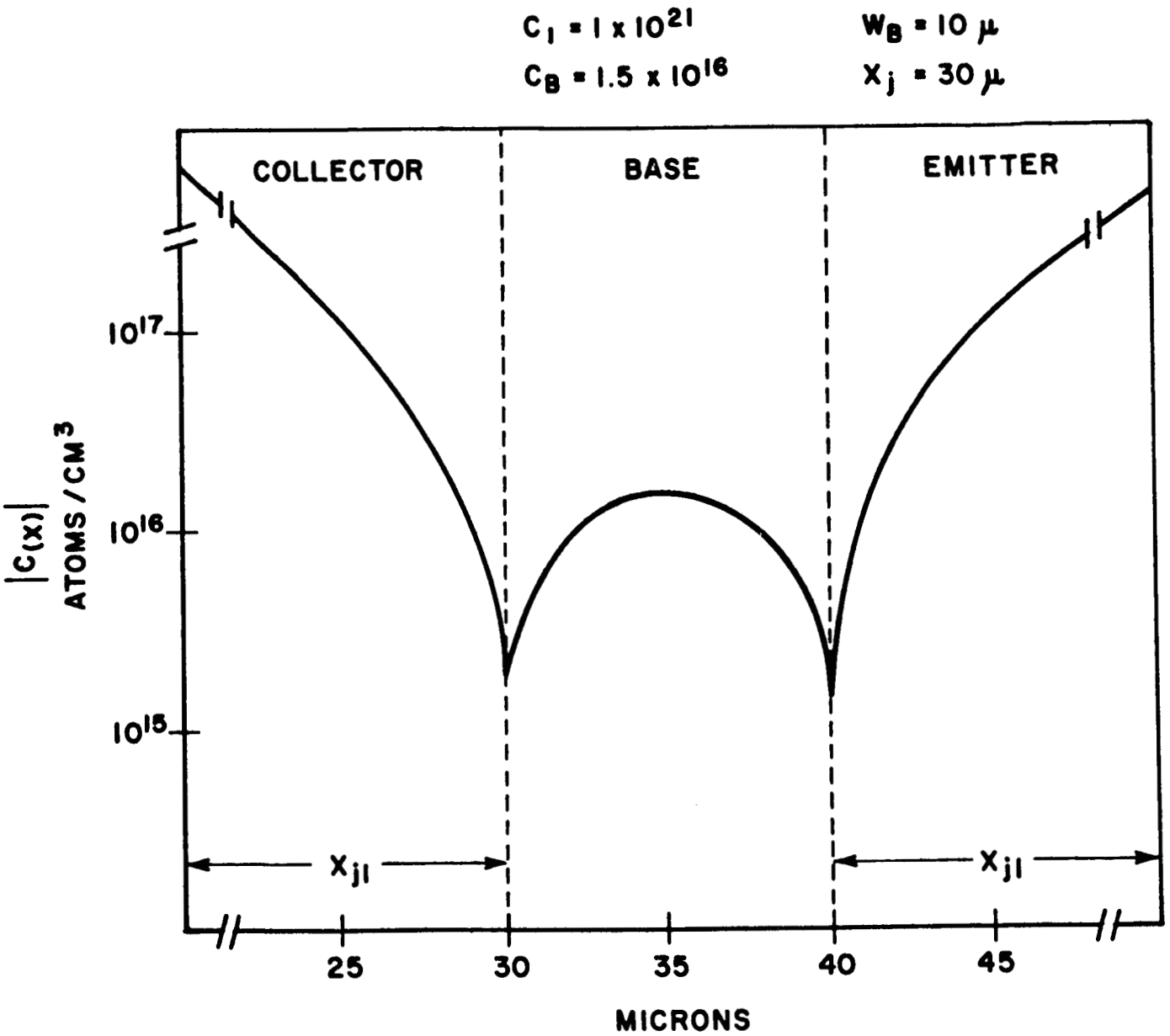

FIGURE 4: Doping Profile for Plain Simultaneously Diffused Transistor

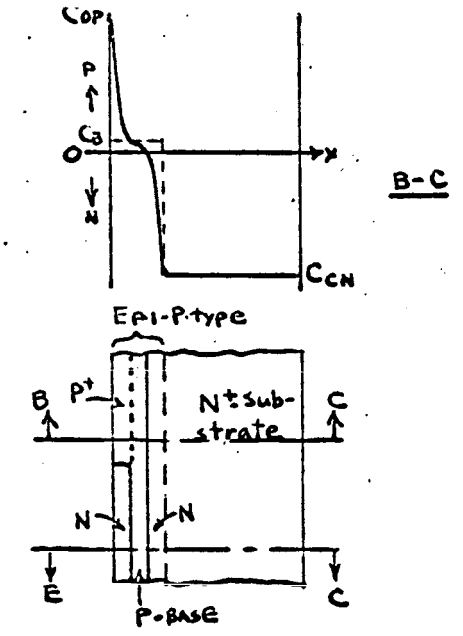

FIGURE 5: Cross-Section Structure of Epitaxial Simultaneously Diffused Transistor

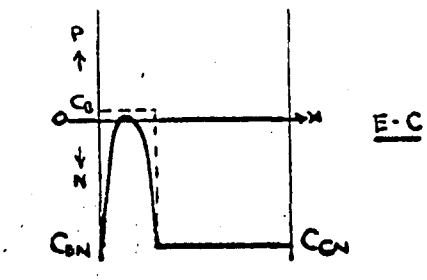

FIGURE 6: Doping Profile of Epitaxial Simultaneously Diffused Transistor

fits the encapsulation system already developed. However, it was found that a completely different package was necessary to minimize resistance.

The CBE design used here will permit free movement between the planar structure and the top and bottom contacts. The silicon wafer is bonded to a piece of refractory metal contact which has almost equivalent thermal coefficient of expansion as silicon. This silicon assembly, therefore, expands and contracts without undue bimetal bowing effect. The contacts are only sliding between surfaces under pressure when the assembly is cycled between temperature extremes. This wiping action takes place in an inert atmosphere within the encapsulation and constantly refreshes the surface for good thermal and electrical transfer.

The pressure applied to the silicon surface is closely controlled to be about an order of magnitude below the stress limits so that it can withstand substantial shock and vibration as proven by actual tests mentioned in Section V.

III. MATERIAL PREPARATION

A. BACKGROUND - EPITAXIAL DESIGN

The present method for producing silicon epitaxial overgrowth on silicon involves a crystallization from the gaseous phase by the aid of the chemical reaction between silicon tetrachloride and hydrogen at elevated temperatures. Similar such processes have been used for the past 100 years for the production of crystals.

The substrate on which oriented crystallization of a single crystal layer takes place need not consist of a crystal identical to the crystallizing substance. This follows from numerous facts concerning epitaxial overgrowth to which many investigations have been devoted since Frankenheim's[4] time. It is sufficient for the lattice of the substrate to possess the necessary metric and energy compatibility with the crystallizing substance or even for its surface to be compatible in metric and energy respects with at least one principal force of the crystallizing substance. The kinetics and regularities of such growth were thoroughly studied by Dankov[5] who formulated the principle of crystallographic correspondence.

The first stage in crystal growth from the vapor phase must be the formation of a nucleus. This is the smallest number of atoms capable of sustaining further growth, units smaller than this tending to evaporate. This requires molecules to condense into clusters and grow until a critical size has been passed. Clearly, if the pressure of the molecules is very high; i.e., if the vapor is supersaturated then there will be increased tendency for the molecules to condense into clusters and grow into nuclei. The supersaturation required for growth of a nucleus may be very high; indeed, it can be shown supersaturations of about 50% may be necessary. Supersaturation is usually defined as α where

$$\alpha = \frac{\rho}{\rho_o} - 1$$

(4) L. M. Frankenheim, Poggend. Ann., 37,516 (1936).
(5) P. D. Dankov, "Proc. of the Second Conf. on the Corrosion of Metals," 2, 120 (1943).

ρ = pressure of vapor

ρ_o = equilibrium vapor pressure of the condensed phase at that temperature.

Once formed, the nucleus begins to grow. Atoms from the vapor collide with the nucleus, diffuse over the surface until they either find a suitable site or fly off into the vapor again. Atoms condensing on the surface lose latent heat causing the surface to be at a higher temperature than the bulk of the crystal. Surface temperatures 100°C higher than the bulk temperature have been suggested by Wilman[6] as a factor contributing to the mobility of atoms on the surface.

Atoms condensing on the surface will prefer sites with a maximum number of nearest neighbors because at such sites the bonding energy is at a maximum. Occupation of such sites would produce close packed surfaces over the nucleus. At this point, further condensation becomes difficult. For further growth, sufficient atoms must come together to form an island "nucleus" on the close packed surface. Once formed, the island may grow laterally to the extremities of the surface and then for further growth another nucleus must be formed. This process is similar to the formation of the original nucleus.

The concept of growth by two dimensional nucleation has been considered by several workers and it is possible to estimate the rate of nucleation; i.e., the rate of formation on monolayer islands and also to estimate the degree of supersaturation required to cause detectable growth. The theoretical value of the latter is of the order of 25 to 50%. However, in practice, it has been found that crystals may grow at low supersaturation of about 1%. This anomaly was explained by Frank[7] who proposed the mechanism of crystal growth which follows. He pointed out that if atoms are added onto the steps of a screw dislocation, a close packed surface of the type described in the previous paragraph was never formed but instead a growth spiral resulted. It should be realized that the origin of dislocations and growth spirals is not completely understood. They may be

(6) H. Wilman, "Proc. Phys. Soc.," London, 1368, 474 (1955).
(7) F. C. Frank, "Disc. Faraday Soc.," No. 5, 48 (1949).

created in the nucleus by thermal agitation or mechanical deformation or introduced during subsequent development of the nucleus. This suggests that the dislocation density can be reduced if conditions during growth are made as free from fluctuations (thermal and mechanical) as possible.

Since the substrate acts as an initial "nucleus" in epitaxial overgrowth, it might be expected that the perfection of overgrowth would depend upon the crystallographic orientation of the substrate. This has been observed in germanium where it was found that the rate of germanium overgrowth was dependent on the substrate crystal orientation for the most densely packed faces <110> , <111> , and <100> . Owing to the strong bonding forces acting in the planes of these faces, condensing atoms will be oriented in the correct way.

The perfection of overgrowth also depends on the temperature of the substrate. It has been found that silicon overgrowths prepared at a substrate temperature of 1270°C show a high order of perfection while the overgrowths prepared at 1175°C are less perfect. These results suggest that during deposition, the high-surface mobility of silicon atoms attained at 1270°C is essential for good film perfection. The high-surface mobility of silicon atoms enables them to diffuse over the surface and to find correctly oriented positions.

A further requirement for the preparation of good epitaxial overgrowth is that the substrate must be free from surface defects. For example, in the case of silicon good epitaxial overgrowth cannot be obtained in the presence of a substrate surface oxide. The latter provides nucleation sites for polycrystalline growth.

In the epitaxial overgrowth of silicon, the deposited silicon is produced by the hydrogen reduction of halosilanes such as silicon tetrachloride, the reduction of which may be represented by the simple equation:

$$SiCl_4 + 2H_2 \rightleftharpoons Si + 4HCl.$$

This equation does not predict the observed yield of other chlorosilane compounds or the yield of high molecular weight polymers of the homologous series $(SiCl_2)_xH_2$, such as $Si_{10}Cl_{20}H_2$, found as a condensate on the reaction walls. To account for the reaction products, it is possible to formulate numerous equations which represent possible reaction mechanisms. The standard free energies for a few of these reactions have been calculated (See Table I), and it may be seen that all are thermodynamically possible. An investigation has been carried out to evaluate, by means of gas chromatography, the reaction products of the silicon tetrachloride and hydrogen reaction.

It has been found that the epitaxial overgrowth rate of silicon is effected by the hydrogen to silicon tetrachloride molar ratio and also the hydrogen flow rate. The causes for these effects are not understood completely. It has been suggested that owing to the relatively high activation energy found for the hydrogen-silicon tetrachloride reaction and reduction in growth rate found by increasing the molar ratio above 0.1 that the following mechanism is possible. First there is adsorption of a silicon subchloride, probably the free radical $SiCl_3$, on the substrate surface and this is followed by loss of chlorine by reaction with hydrogen. However, the occurrence of adsorption phenomena at high temperatures seems doubtful and until further work has been carried out, particularly on the identification of reaction products, the kinetics of the reaction of hydrogen with silicon tetrachloride will remain obsure.

B. REQUIREMENTS FOR EPITAXIAL GROWTH

The epitaxial surface requirements for the 100-amp transistors are stringent; no defects are tolerable over the entire large area active region. Small area devices can tolerate several defects since these units can be discarded. However, the presence of one defect in the 100-amp configuration would nullify the unit because of the resultant low voltage or short characteristics. It has been determined that all epitaxial defects originate at the substrate epitaxial layer interface and are dependent on surface cleanliness, substrate perfection and system purity.

TABLE I

Standard Free Energies for Typical Reactions

Reaction	Standard Free Energy for Reaction at 1533 Å (1270°C)
$SiCl_4 + 2H_2 \rightleftharpoons Si + 4HCl$	-1.9 Kcal/mol.
$SiCl_4 + Si \rightleftharpoons 2SiCl_2$	-2.2
$SiCl_2 + H_2 \rightleftharpoons Si + 2HCl$	-1.2

1. Substrates

The substrates used for the 100-amp devices are degenerate in that they are heavily doped with impurities. The doping level of the substrate was selected to obtain the designed saturation voltage characteristics. Heavily doped substrates inherently contain sufficient impurities to distort the crystal lattice. Distortions caused by precipitates or inclusions will not permit a sufficiently good lattice match for defect-free epitaxial growth. These distortions can be eliminated by careful selection of the parent crystal growth conditions and the type of dopant. Evaluation of the substrate material is accomplished by examination of the chemically polished surface prior to epitaxial growth. A chemically polished surface was employed for this device to insure a damage-free surface and to permit microscopic examination of the surface before growth was initiated.

2. Substrate Preparation

Preparation of the substrate material before epitaxial growth is a deciding factor in producing defect-free epitaxial layers. Heavy metal impurities, such as aluminum or iron, are retained by the substrate after the slicing and doping operations. These can give rise to foreign nucleation sites during the growth process. Wetting agents or solvents do not effectively remove these heavy metals. However, chemical techniques, such as reactive chloride acids, convert most heavy metals to water soluble metal chlorides and are easily removed by subsequent rinsing in deionized water.

3. Epitaxial System Purity

Epitaxial growth perfection is also dependent on system purity; that is, the environment in which the chemical reduction of the halide takes place.

a. Gas System -- The gases used in the epitaxial process must be of good quality. The hydrogen used for the reduction is passed through a Deoro unit to remove traces of oxygen and then through a dryer to remove water to a purity of less than 1ppm. All gases are filtered through submicron filters to remove foreign particles before they enter the reaction chamber.

The control of the gases, the valving and piping required to mix and dilute, switching and metering are all done in a system that is leak proof. The materials of construction are Teflon and quartz to maintain gas purity prior to the reaction chamber.

b. Reactor -- A horizontal RF heated epitaxial system was used for all the 100-amp device substrates (Figure 7). The susceptor was a pure grade of graphite coated with silicon carbide. The silicon carbide is deposited on the graphite under the same conditions required for epitaxial growth to insure a noncontaminating or defect contributing source.

The reactor tube was of quartz, and the susceptor is supported on a quartz sled. Reactor tube and susceptor loading is accomplished in a positive pressure hood to minimize dust or environmental particles from contaminating the surfaces of the slices.

c. Epitaxial Procedure -- The epitaxial procedure for the 100-amp device consists of heating the substrates to 1200°C in a filtered dry hydrogen atmosphere. Pure gaseous HCl is introduced to etch the substrates prior to growth. The reaction of HCl and silicon is the reverse of the deposition reaction and permits the removal of the last traces of work damage caused by chemical polishing.

$$4HCl + Si \longrightarrow SCl_4 + 2H_2$$

Sufficient silicon is removed to insure a latice match for the growth operation.

The HCl procedure is followed with a pure hydrogen treatment at 1200°C to clean out the reaction area of any chlorides which could act as nucleation sites. A P^+ layer deposition is then deposited to the desired thickness and is controlled to 0.1 ohm cm. P-type with diborane gas. After the P^+ deposition, the system is purged with pure hydrogen to remove the dopant and halide traces. The system is then cooled for the removal of the substrates.

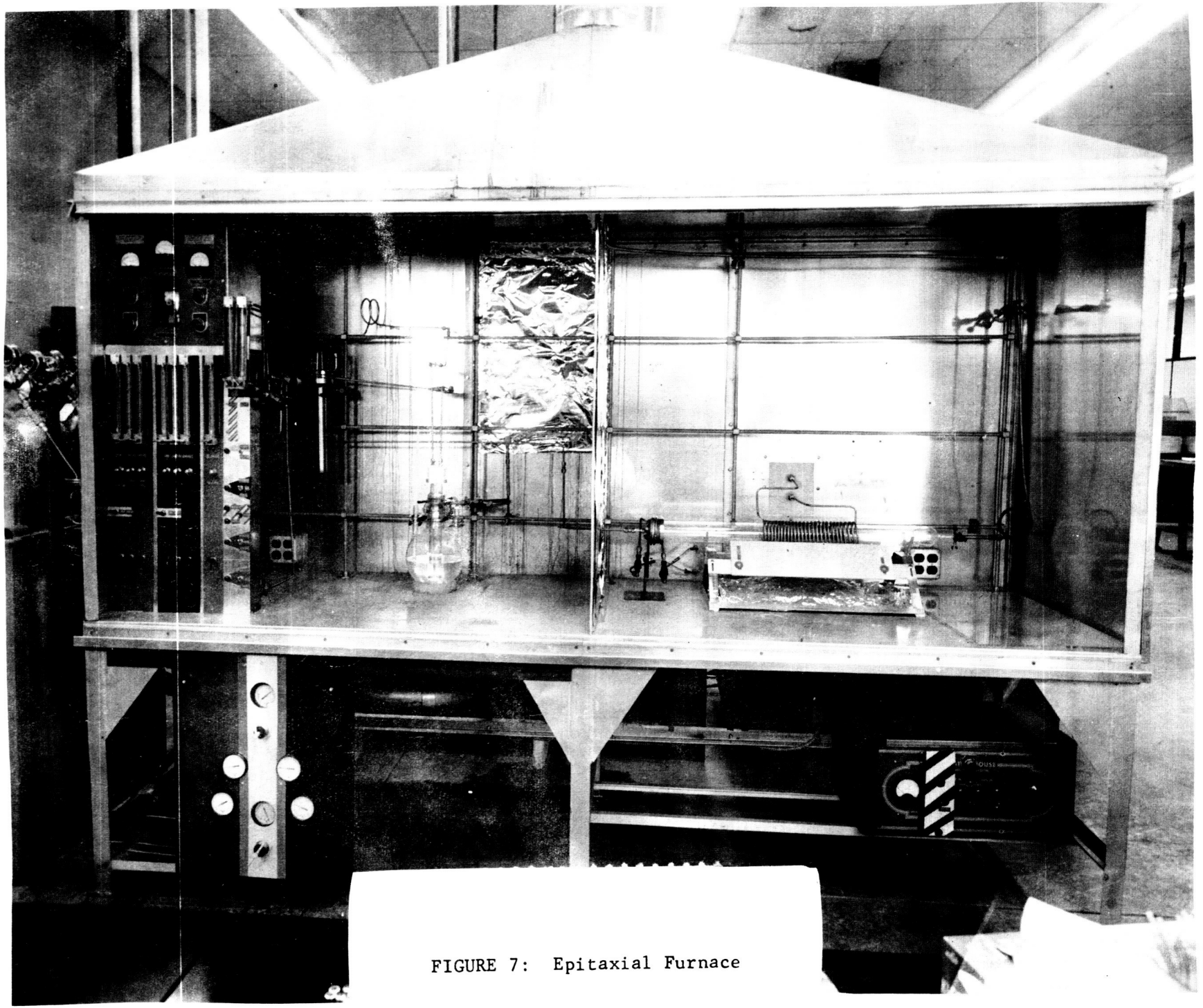

FIGURE 7: Epitaxial Furnace

C. MATERIAL REQUIREMENTS - MODIFIED SINGLE DIFFUSED DESIGN

Single Specifications:

P-Type
Resistivity 17 to 20 ohm-cm
Radial resistivity gradient - 15% (max.)
Diameter 0.937" $\pm$ 0.001"
Dislocation density 0 to 1500/cm^2
Orientation - within 2° of the (111)
Lifetime - 50 microseconds (min.)
Lineage - None
Other imperfections - None

D. EVALUATION OF MATERIAL

1. Conductivity

This measurement determines the majority carriers in the silicon crystal. Two methods are employed at this laboratory--thermoelectric cold probe method (See Figure 8) and the point contact rectifier method.

2. Resistivity

The resistivity is measured every inch down the length of each crystal to insure the accuracy of reading supplied by the supplier. A Fell's four point probe is utilized for this operation; a probe spacing of 0.025" is used. Figure 9 illustrates the assembled equipment employed for resistivity measurements.

3. Radial Resistivity Gradient

This measurement is made employing the equipment seen in Figure 9. This measurement is made on a silicon slice using a 0.025" Fell's four point probe. Readings are made in the center and at 1/2 radius, and the gradient calculated from the data obtained. This is to insure a uniform distribution of dopant atoms in the slice.

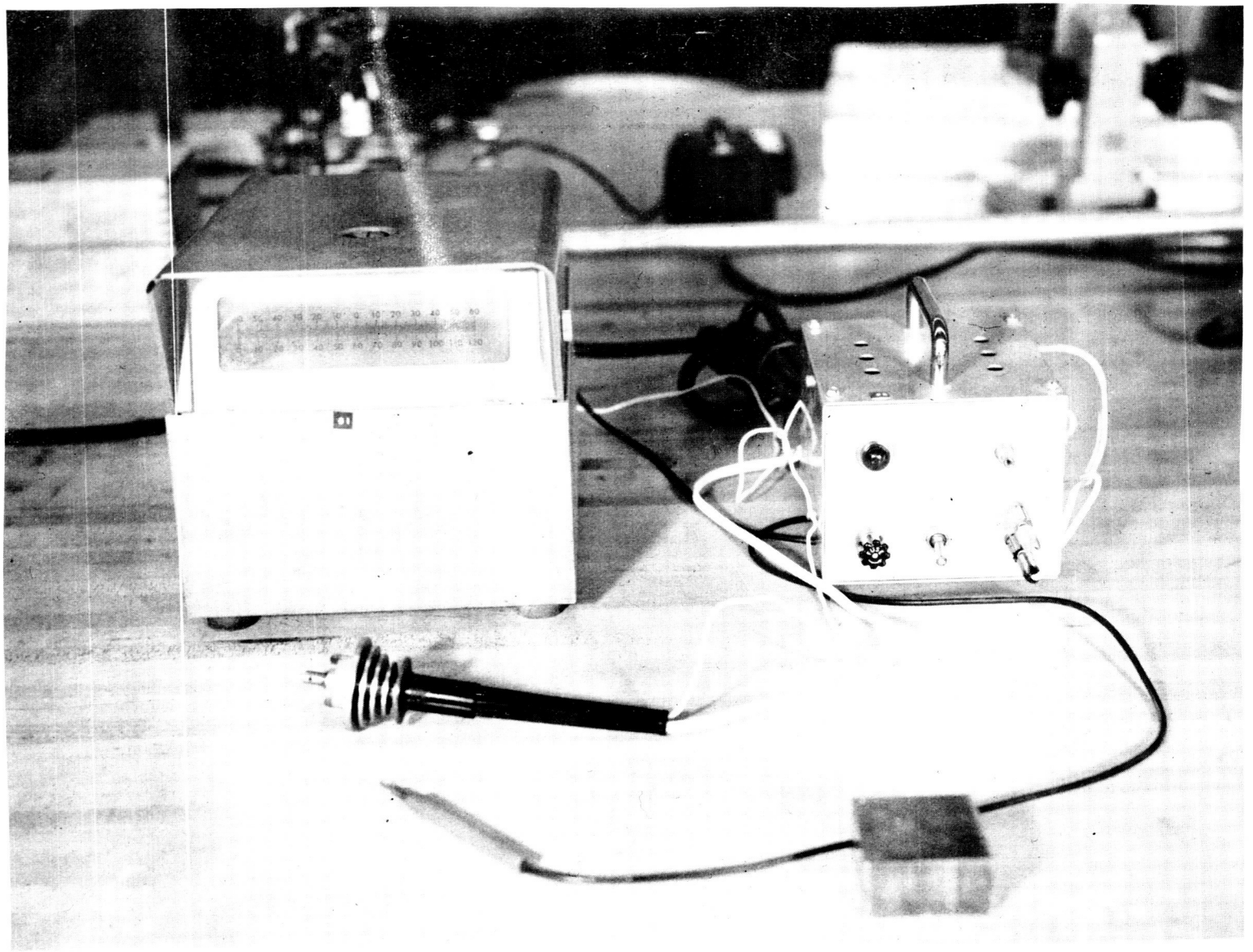

FIGURE 8: P-N Cold Probe

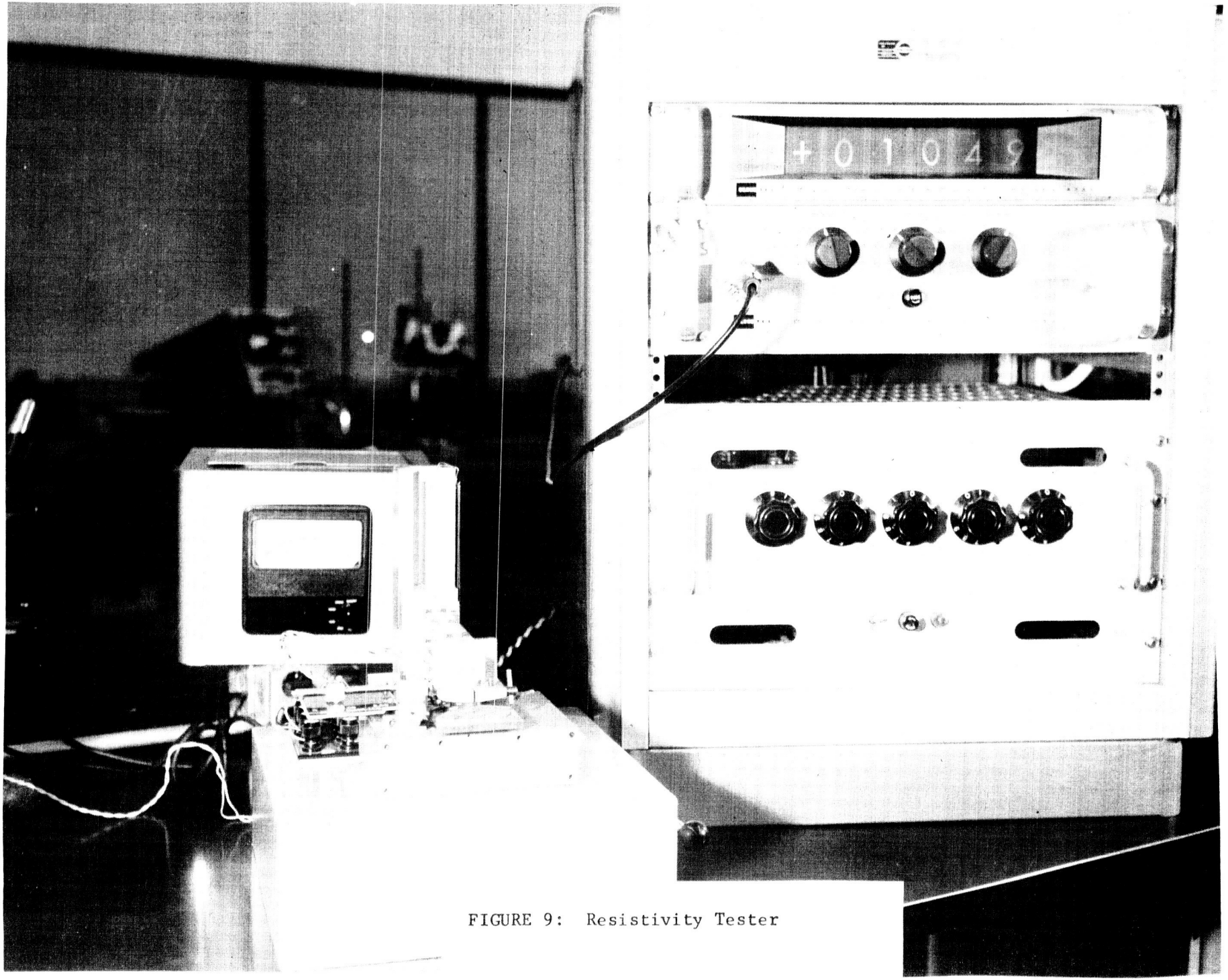

FIGURE 9: Resistivity Tester

4. Diameter

This material is centerless ground by the supplier to our specification. Buying the material to size eliminates the necessity of cavitroning, etching or sandblasting.

5. Dislocation Density

This parameter is checked on both the seed and the end of the crystal opposite the seed. These slices are etched in chromium trioxide to reveal the etch pits, and a count is then made to determine the number/cm^2. Figure 10 illustrates the microscope used to count the etch pits.

6. Orientation

A photograph of the orientation apparatus is shown in Figure 11. The primary objective is to insure that after sawing there will be a round slice of 0° on the (111).

7. Lifetime

The lifetime equipment is illustrated in Figure 12, which is a photo-conductive decay instrument. The crystal is first degreased, washed with pure water and dried, the ends of the crystal are then gold plated to insure good electrical connection when it is placed in the above equipment. Known lifetime standards are checked daily.

8. Lineage

One slice is taken from the end of the crystal opposite the seed. This slice is then lapped using 12 micron grit size. Following lapping it is degreased and cleaned. The slice is then placed in a mixture of HF, H_2O, and Cr_2O_3 (1:1:1) for 5 minutes. The etch pit count is then made at 200X and the count reported in etch pits/cm^2.

9. Other Imperfections

The slice used in (8) is then relapped to remove the etch and is then re-etched but in a 10% solution of sodium hydroxide for a structural

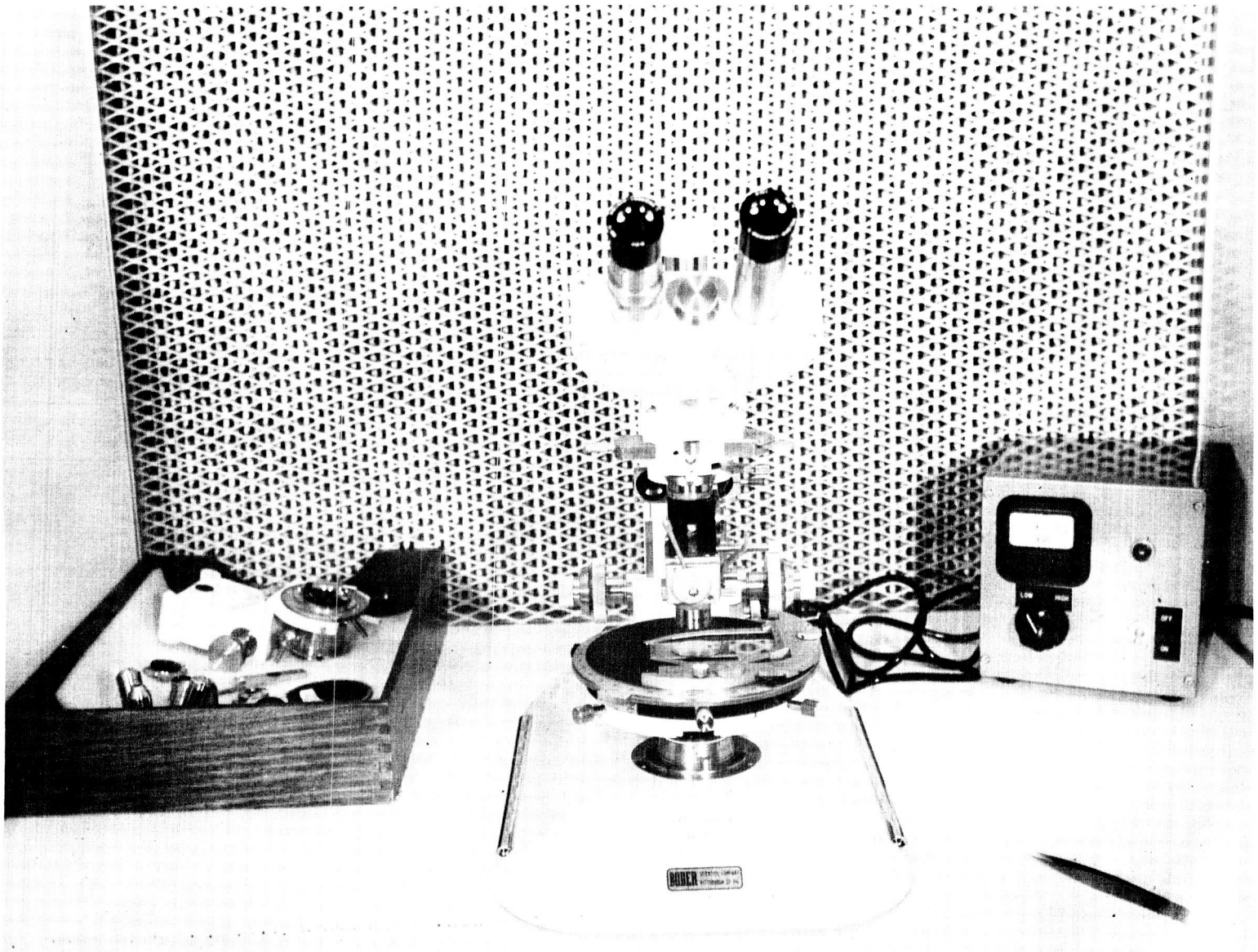

FIGURE 10: Normarski Interference-
Contrast Microscope

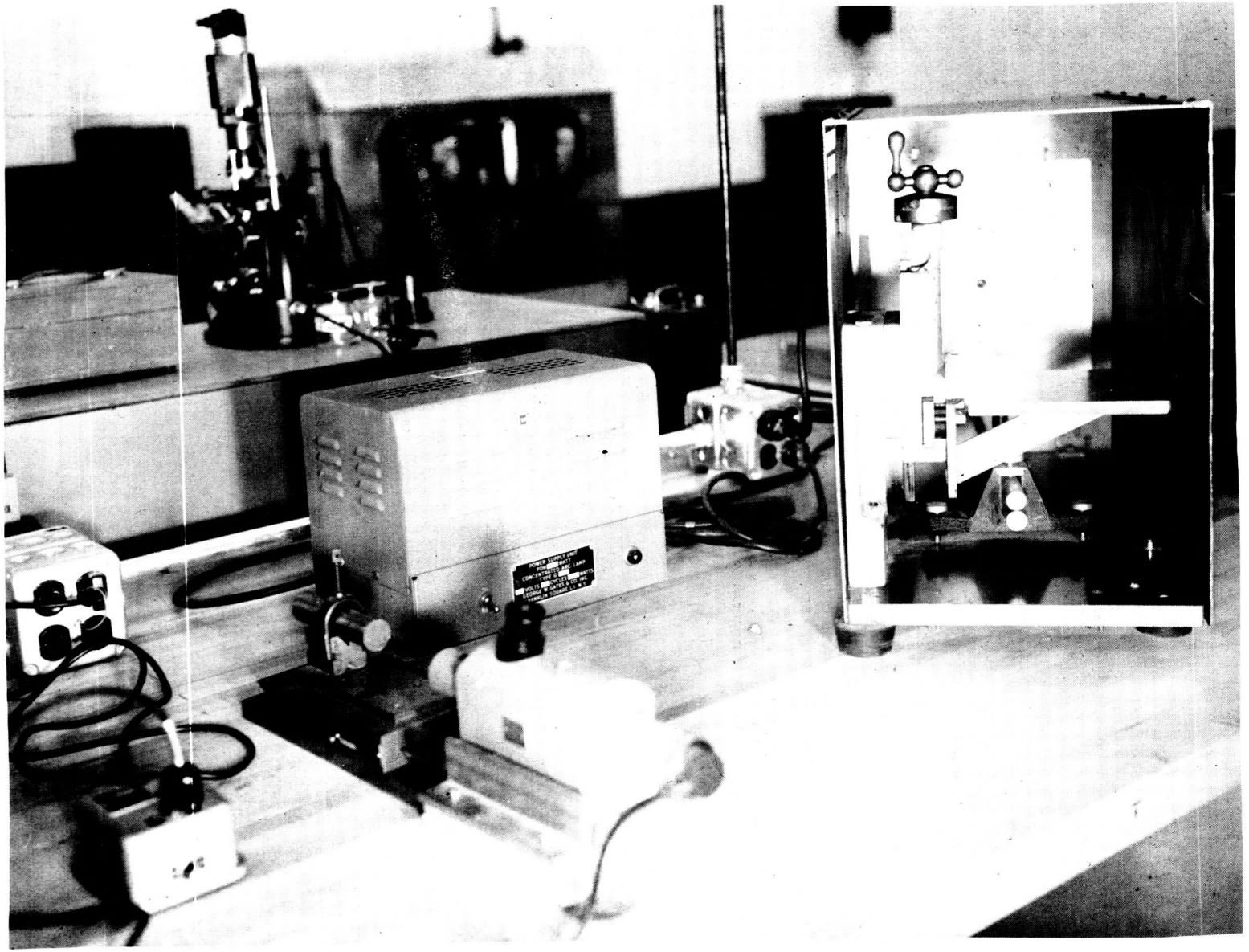

FIGURE 11: Orientation Checking Equipment

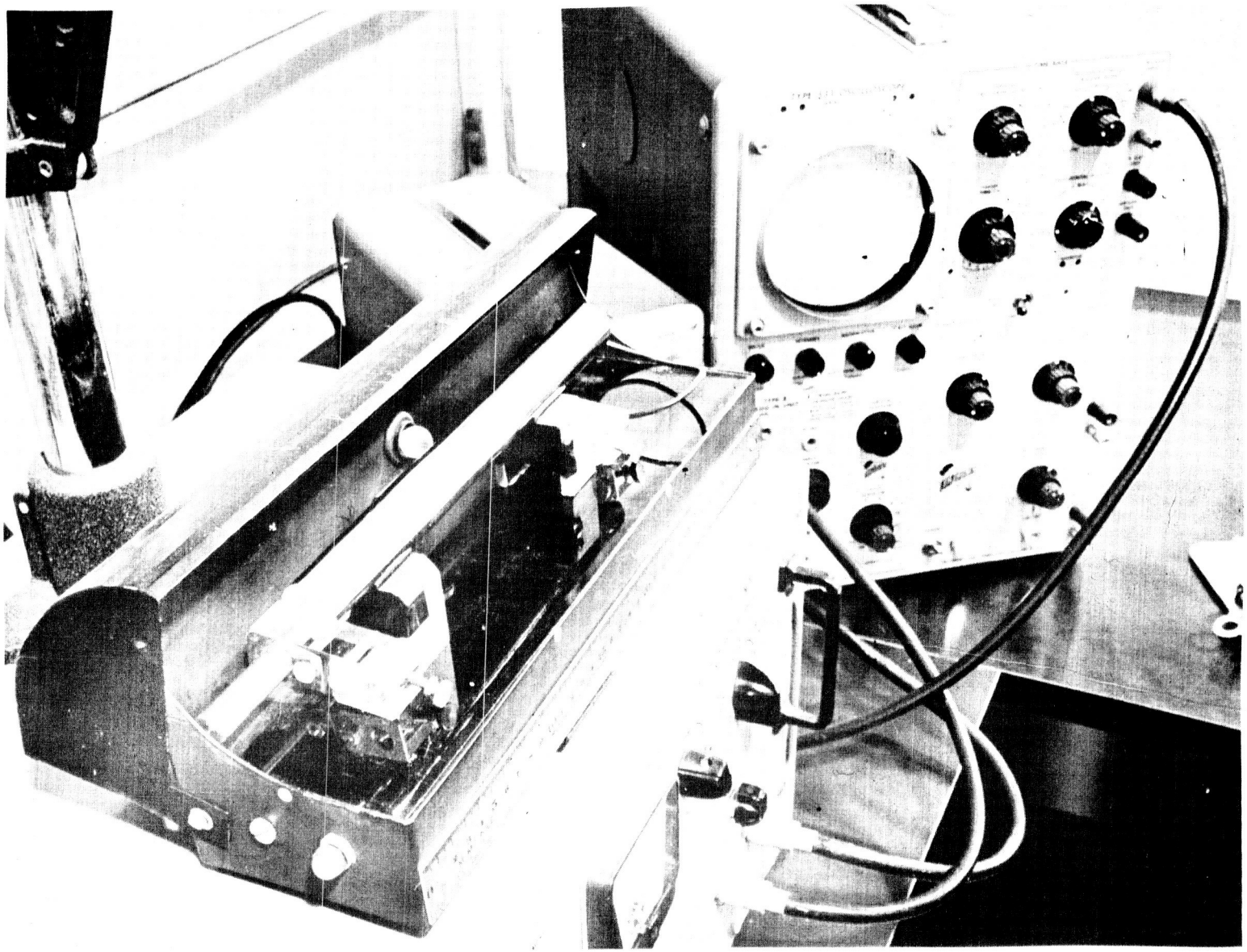

FIGURE 12: Lifetime Test Equipment

examination of the slice, where the primary imperfection might be twin-poly inclusions or slip.

E. MATERIAL PREPARATION

1. After the material has been evaluated and found to be in accordance with specification, it goes to the slicing area. Here the silicon crystal is sliced with a Hamco Saw (See Figure 13), which according to our investigation, gives the best surface finish.

2. The slices are then forwarded to the lapping area where approximately 2 mils are removed from each side of the slice with a Hoffman Planetary lapping machine (see Figure 14). The lapping slurry used is approximately 12 micron grit size, which leaves a mat surface.

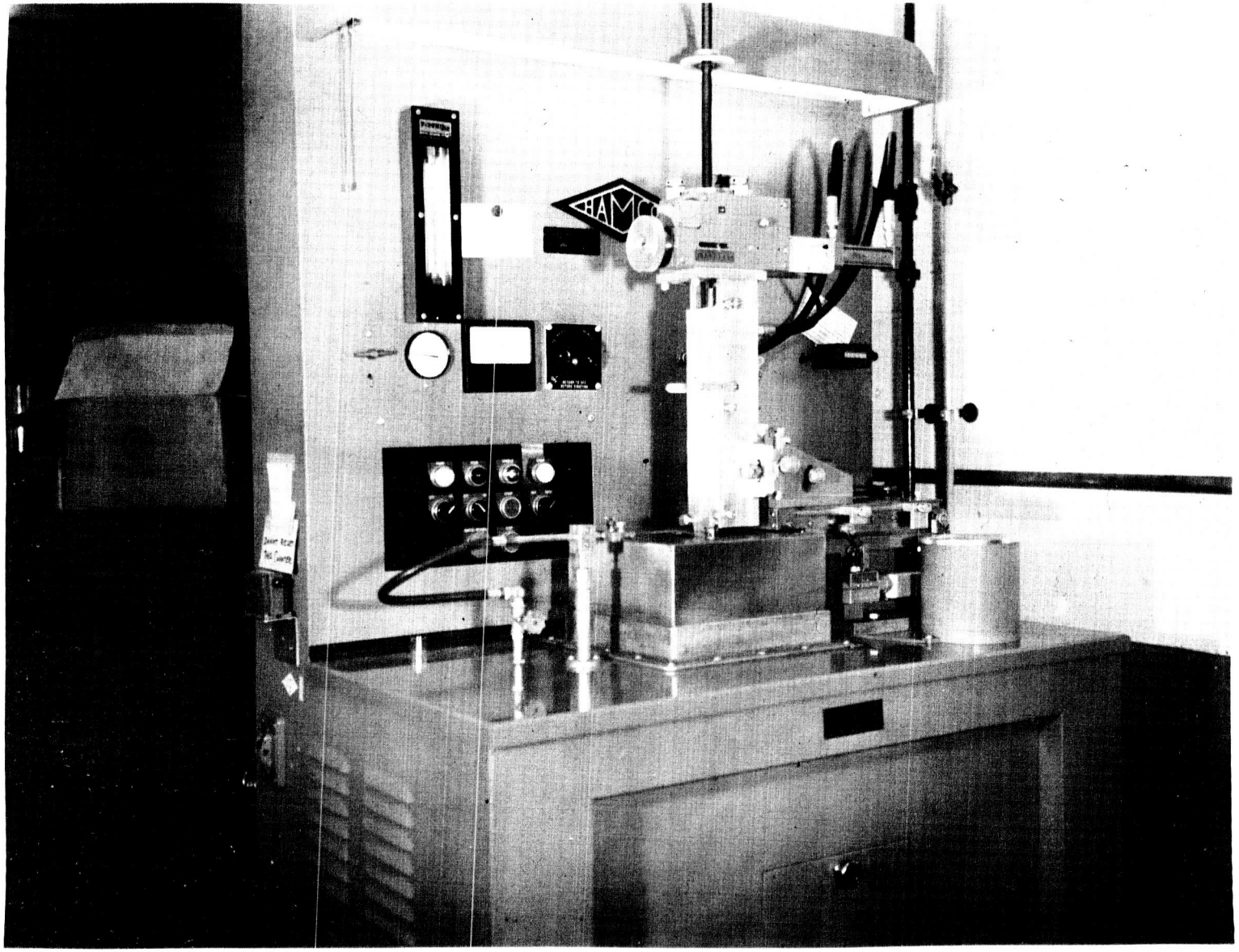

FIGURE 13: Hamco Cutting Saw

FIGURE 14: Planetary Lapping Machine

IV. DEVICE FABRICATION

Two major processes were used to fabricate 100A transistors for this contract. In Process A, the base emitter and collector are formed by diffusion. In Process B the base is grown epitaxially on the collector region and the emitter region is formed by diffusion. The details of these processes are given in Figures 15, 16 and 17.

A. PROCESS A - MODIFIED SINGLE DIFFUSED

1. Cleaning

The slices received from lapping must be given a thorough cleaning to remove all lapping oil and grit. This is accomplished by subjecting the wafers to five successive rinses in clean trichloroethylene. A quartz cleaning boat is used for this purpose. The wafers are first given a bulk (a maximum of 15) rinse in approximately 200 milliliters of T.C.E. They are then transferred to the quartz boat which is placed in a 600ml Pyrex beaker. The boat and wafers are covered with T.C.E. and the beaker is placed on a hotplate. After attaining a temperature of 65°C, the assembly is placed in an ultrasonic agitator for approximately five minutes. The T.C.E. is then decanted and the wafers are again covered with clean T.C.E. The heating and ultrasonic agitation are then repeated as outlined above. This complete cleaning cycle is repeated five times. After the fifth rinse cycle, the wafers are removed from the quartz boat and dried under a heat lamp. This is done by placing the wafers on filter paper which is located approximately 6" below a heat lamp. The wafers are dried under the lamp for 10 minutes.

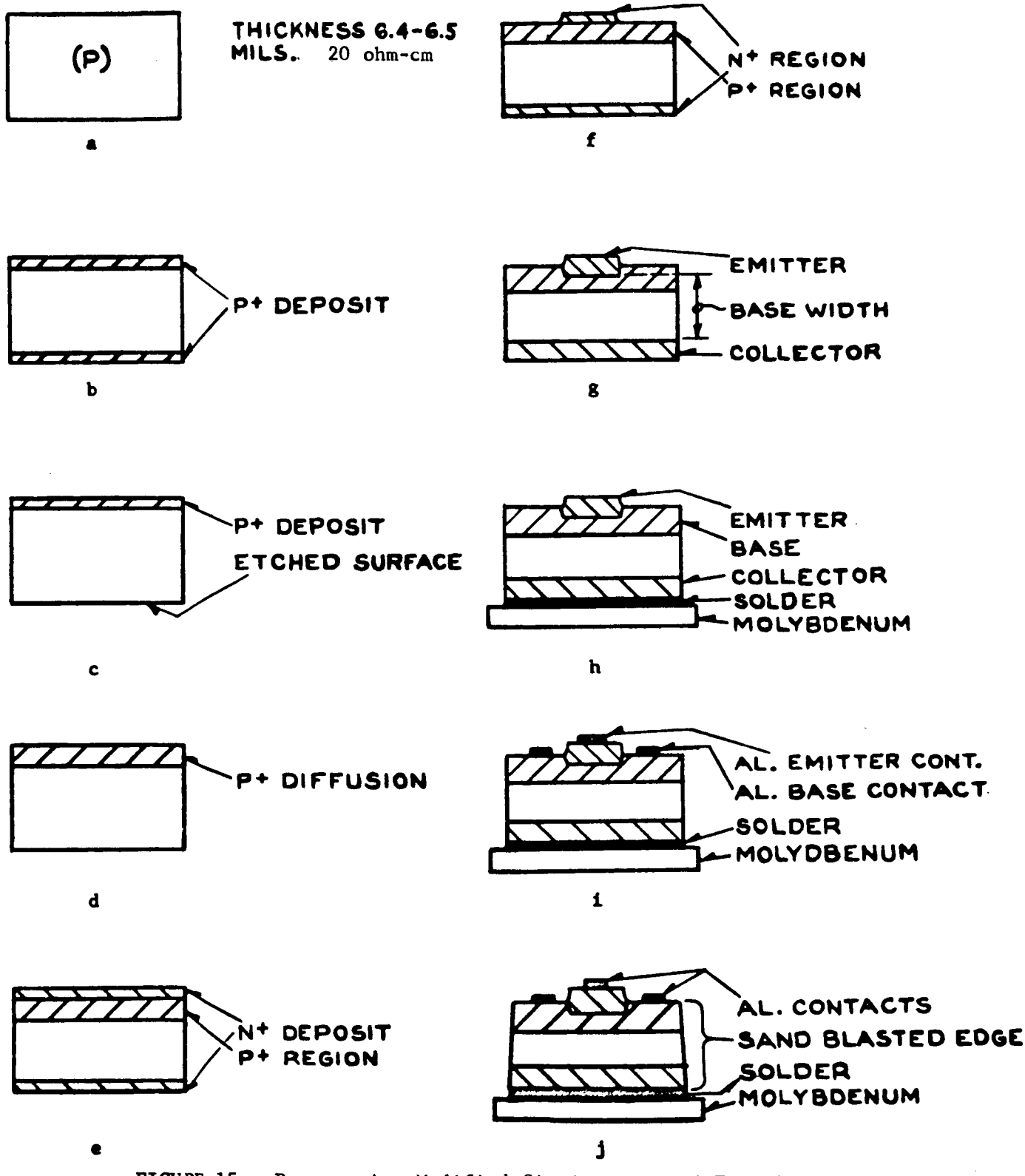

FIGURE 15: Process A - Modified Single Diffused Transistor

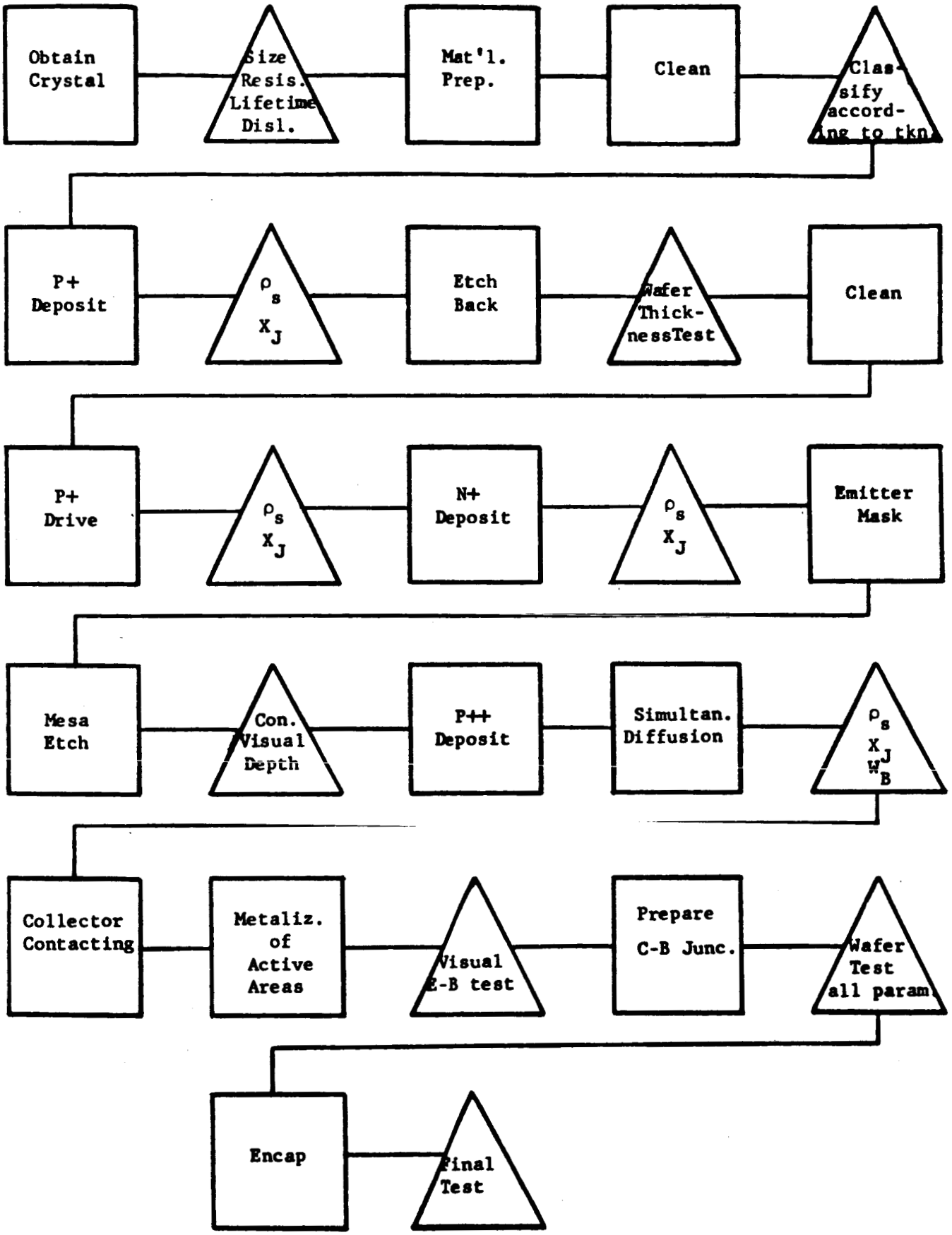

FIGURE 16: Process A - Flow Chart

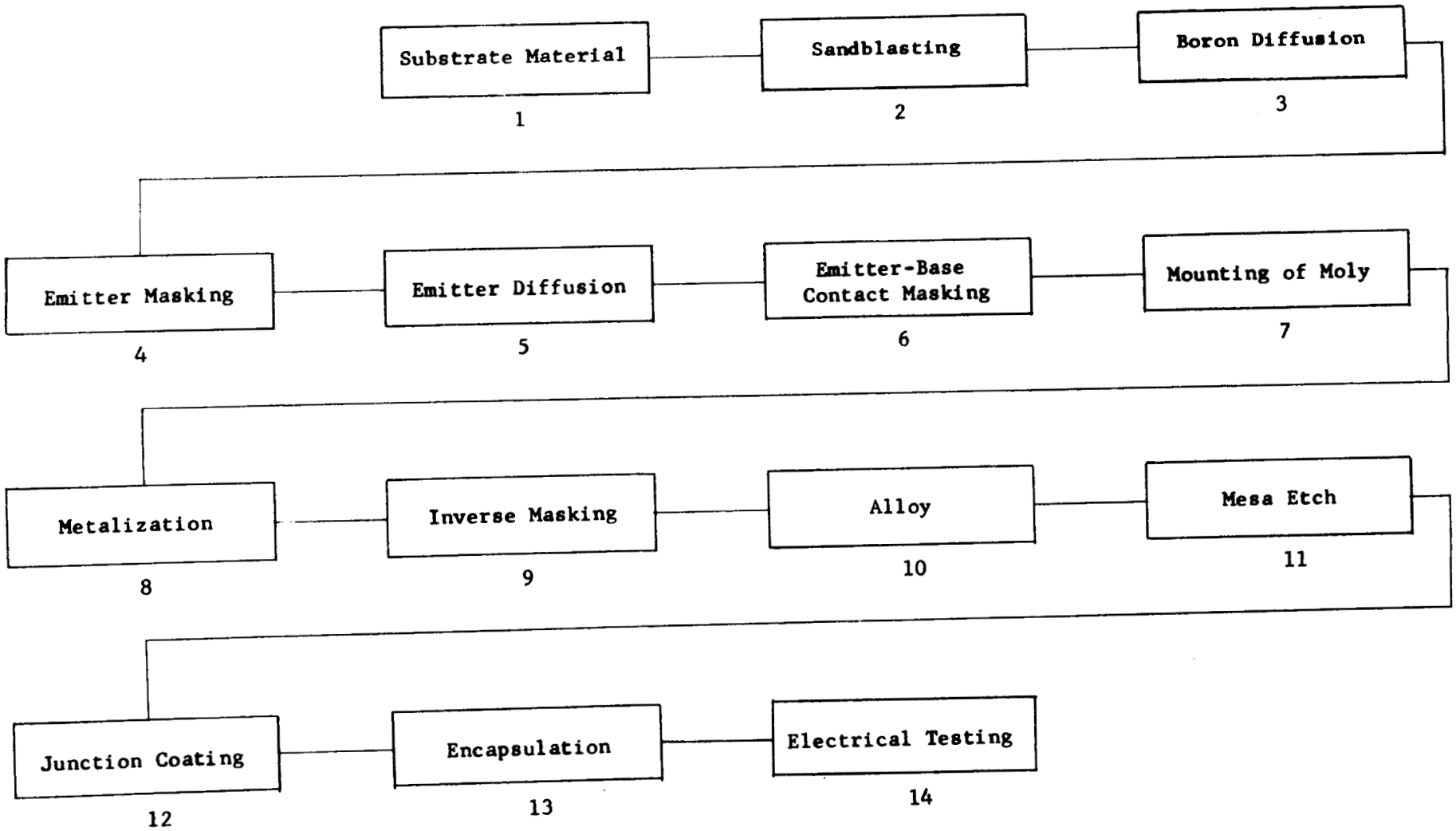

FIGURE 17: Process B - Flow Chart

It is imperative at this pcint that the exact thickness of the wafers be determined. This is essential because the base width resulting from wafers with different thicknesses will vary. Therefore, it is essential that the wafers be classified and sorted according to thickness. The wafers are grouped such that the members of the group are within 0.0001" of one another in thickness. After the wafers have been sorted and marked, a run consisting of any particular number of wafers can be started.

Once the run size has been determined, the wafers are given a thorough acid cleaning to remove any remaining organic and inorganic contaminants. The wafers are loaded into a quartz cleaning boat. The boat is lowered into a beaker which contains H_2SO_4 heated to 95°C. After 5 minutes the wafers are removed and rinsed in running deionized H_2O for 3 minutes. Next the wafers and boat are placed in a beaker of hot (80°C) HNO_3. They remain in the nitric acid for 15 minutes. This acid soak is followed by a 3 minute rinse in running D.I. H_2O. The slices are then placed in three successive beakers (for 5 minutes each) of hot (90°C) D.I. H_2O. Following the last hot water soak, the slices are rinsed in running D.I. H_2O for 3 minutes. Upon completion of the water rinse, the wafers are transferred to a polyethylene carrier which is submerged in D.I. H_2O. This is followed by a D.I. rinse for 5 minutes. The carrier case is then sealed and passed through a positive-pressure material pass-through into the diffusion room. Wafers cleaned in this manner are not permitted to stand for more than 4 hours prior to the subsequent diffusion step.

2. P^+ Deposit

Wafers which have been cleaned as described above are now ready for a P^+ deposition. The purpose of this diffusion is to deposit a layer of boron atoms on one surface of the crystal to a depth of approximately 1.2μ. This layer will subsequently be driven to a depth of approximately 25μ. Figure 1b is a drawing which illustrates this step in the fabrication of the device. The reason for the inclusion of such a layer in this device will be discussed in another section.

The deposition of this P^+ layer is done in the furnace shown in Figure 18. The furnace is continually maintained at a temperature of 1000°C. This temperature is held over a flat zone of 12". For the purposes of this deposition, a liquid source (boron tribromide, BBr_3) is used. Figure 19 is a drawing which depicts the source arrangement used for this deposition. The gases which are used to transport the BBr_3 vapors are nitrogen and oxygen.

The wafers to be deposited are removed from the plastic container with tweezers and blown dry with N_2 which passes through a 0.45μ millipore filter. The dried wafer is then placed on the P^+ deposit boat. After all the wafers have been dried in this manner with the N_2 jet and placed under the heat lamp, the boat is allowed to remain there for 5 minutes.

Prior to actually placing the wafer-holding boat into the diffusion furnace, the diffusion system must be purged. This is accomplished in the following manner: (1) the source is allowed to flow through the diffusion tube for 2 minutes; (2) the source gas is shut off and the system is allowed to set for 2 minutes; (3) 1 minute is allowed to load the boat which has been under the heat lamp; (4) the boat and wafers are permitted to remain in the flat zone for 2 minutes. This is to allow boat and wafers to reach the flat zone temperature before starting the diffusion cycle. (5) the carrier gas is allowed to flow through the BBr_3 source and through the diffusion tube for the prescribed time of the run; (6) at the conclusion of the run, the source is shut off and the wafers permitted to sit in the flat zone for an additional 2 minutes; (7) the boat is withdrawn and the wafers allowed to cool to room temperature.

Upon completion of the P^+ deposition cycle, it is essential that the surface concentration of the deposited layer be determined. This can be found most easily from the sheet resistivity (ρ_s) and depth (X_J) of the

FIGURE 18: P^+ Diffusion Furnace

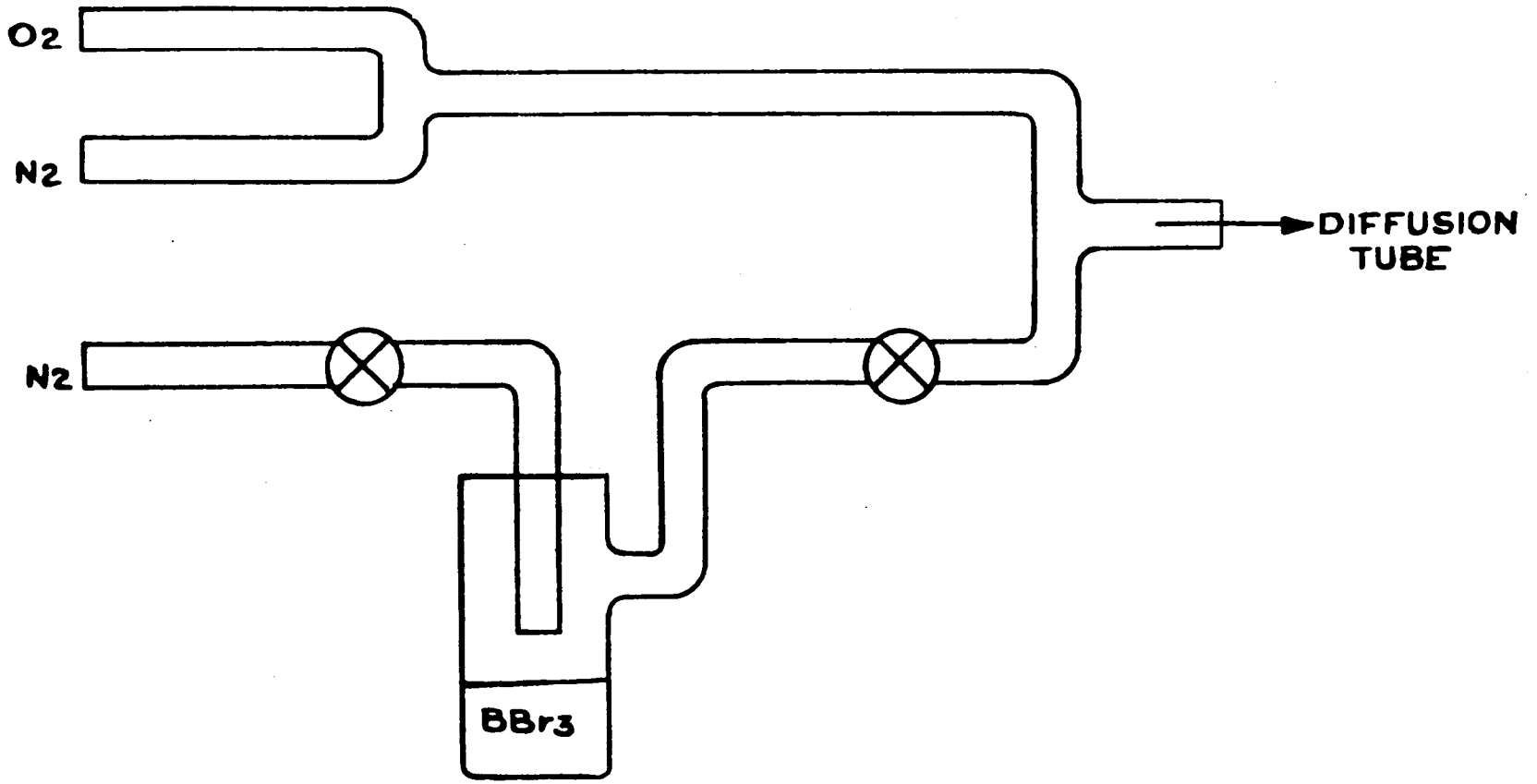

FIGURE 19: BBr_3 Source Arrangement for Deposition

layer. The surface to be tested must first have all the oxide on it removed. This oxide is etched by immersing the wafers in concentrated (48%) hydrofluoric acid for 2 minutes. After the HF etch, the wafers are rinsed in running D.I. H_2O for 3 minutes and dried under a heat lamp.

The dried wafer is then placed in the four-point probe and the sheet resistivity read.

The junction depth is determined by sectioning a portion of a deposited wafer on a 3° angle block. Such a portion is first mounted on the beveled part of the block with wax. After allowing the wax to harden, the operator polishes the sample on a polishing wheel. The wheel used for this purpose is covered with a polishing cloth and A.B.Metadi^{R} (Buehler Standard Company) fluid and diamond polishing compounds are used to attain a highly polished edge on the sample. The liquid and solid polishing materials are then removed by gently swabbing the sample with a warm, mild soap solution. This is followed with a thorough rinse under running D.I. H_2O (at least 1 minute). The sample is then blown dry with filtered nitrogen. It is now ready to be stained with the proper acid to delineate the junction. For this sample, concentrated HF (applied under a heat lamp) will bring out the junction. A photographic record of the interference fringes is then obtained for future reference.

The actual depth of penetration of the deposit layer can be calculated. Once the X_J and ρ_s are known, the surface concentration of the deposited layer can be determined from Irvin's[8] curves which relate surface concentration to effective conductivity which is defined as

$$\sigma_{eff} = \frac{1}{\rho_s X_J} .$$

(8) J. C. Irvin, "Resistivity of Bulk Silicon of Diffused Layers in Silicon," B.S.I.J., Vol. XLI, p.387, March 1962.

For the purposes of fabricating this device, it has been found that a minimum surface concentration of 1×10^{18} atoms/cc must be attained.

3. Etch Back

Those wafers which have been found to have the proper surface concentration of boron atoms are then stripped of any boron layer which may have been deposited on the back side of the wafer. Since the P^+ deposition is done on wafers that are lying flat on a quartz boat, the back side does not have as uniform a layer as the top surface. For this device, it is essential that no P^+ layer be diffused into the back (collector side of the wafer). To be certain of this, any P^+ region on the back side must be removed prior to the P^+ drive.

This removal is done by etching a thin layer of silicon from the wafer. The top surface must be protected from the etch. The wafer is mounted, top surface down, in molten apiezon wax. Care must be taken to see that the wafer is completely surrounded by the wax. This will prevent the acid etch from attacking the top surface where a uniform P^+ layer is desired. After the wax has cooled to room temperature (about 10 min.), the wafers are submerged in the etch. The chemical composition of the etch is:

150 HNO_3 (volume)
50 HA_c (volume)
30 HF (volume).

The etching step is followed by a thorough D.I. water rinse (approximately 3 minutes). After drying the slices with a jet of nitrogen, they are removed from the glass slide by heating the slide on a hot plate. The wax is removed from the wafer by swirling the wafers in hot T.C.E. This solvent rinse is repeated 5 times in hot, fresh T.C.E. They are then dried under a heat lamp. It is important that the wafer thickness now be determined for the wafers just etched.

The actual wafer thickness at this stage must be found for two reasons. First, it must be known in order to determine if all the P^+ region has been removed from the back of the wafer. Second, since the final base width will be determined by the wafer thickness and the junction depth of the N^+ regions, the wafer thickness must be known.

To eliminate the possibility of a thickness variation across a wafer or a testing error, 5 readings are taken on each wafer. Since all wafers have been given the same treatment up to this stage (i.e., same starting thickness, P^+ deposit, and back etch), they should all have the same thickness. However, those which differ by more than ± 0.00005 from that of the majority of those in the run are withdrawn and held until a subsequent run of such thickness is at this stage. They can then be added to this run and processed to fabricate devices. The wafers are then cleaned once again as in Section 1.

4. P^+ Drive

The purpose of the P^+ drive is to diffuse the P^+ layer to the proper depth on the emitter-base side of the wafer. At this stage of processing (the P^+ region will be driven deeper into the crystal during the simultaneous N^+ diffusion), the P^+ layer must be driven into the Si wafer to a depth of 20-25μ. This diffusion can be accomplished in about 10 hours at 1250°C. The diffusion is done in a O_2-N_2 atmosphere with no source present (since a P^+ layer had been deposited on the surface). The wafer handling is similar to that described for the P^+ deposit. Since no dopant is used in this drive cycle, the elaborate purge described for the P^+ deposit is eliminated. Upon completion of the drive cycle, the slices are withdrawn from the hot zone and allowed to cool to room temperature. Figure 1d illustrates a cross section of the wafer at this point in the process.

Both sheet resistivity and junction depth are again determined. The methods used are the same as those described above with the following parameters necessary for the wafers to be processed further:

X_J = 20-25μ
ρ_s = 0.8 - 1.0 ohm/□

Before proceeding to the next step (N^+ deposit) all the oxide grown during the P^+ drive must be removed from the wafers. This can be done by etching the wafers in hydrofluoric acid (48%) for 2 minutes. A thorough D.I. water rinse (5 minutes) follows the acid soak. The wafers are then passed into the diffusion room.

5. N^+ Deposit

The N-doped emitter and collector regions are deposited simultaneously on the wafer in an ammonium phosphate atmosphere. Figure 20 is an illustration of the set-up used to perform this operation. The solid source (ammonium phosphate) is contained in a quartz boat which is placed in an 800°C (±5°C) zone of the diffusion furnace. The slotted quartz boat holding the wafers in a vertical position is allowed to rest in the flat zone which is held at 1200°C.

After blowing the wafers dry with filtered nitrogen, they are placed in a slotted quartz diffusion boat. The loaded boat is placed under a heat lamp and allowed to set there for 5 minutes. The ammonium phosphate is placed in the quartz source boat and placed into a protective quartz sleeve. The sleeve is used to prevent splashing of the source onto the wafers. After the wafers have been under the heat lamp for 5 minutes, they are loaded into the furnace (1200°C zone). The source is immediately loaded into the 800°C zone and the carrier gases turned on. For this diffusion, a combination of nitrogen (75%) and oxygen (25%) is used. To achieve the desired phosphorus concentration, the diffusion cycle is 40

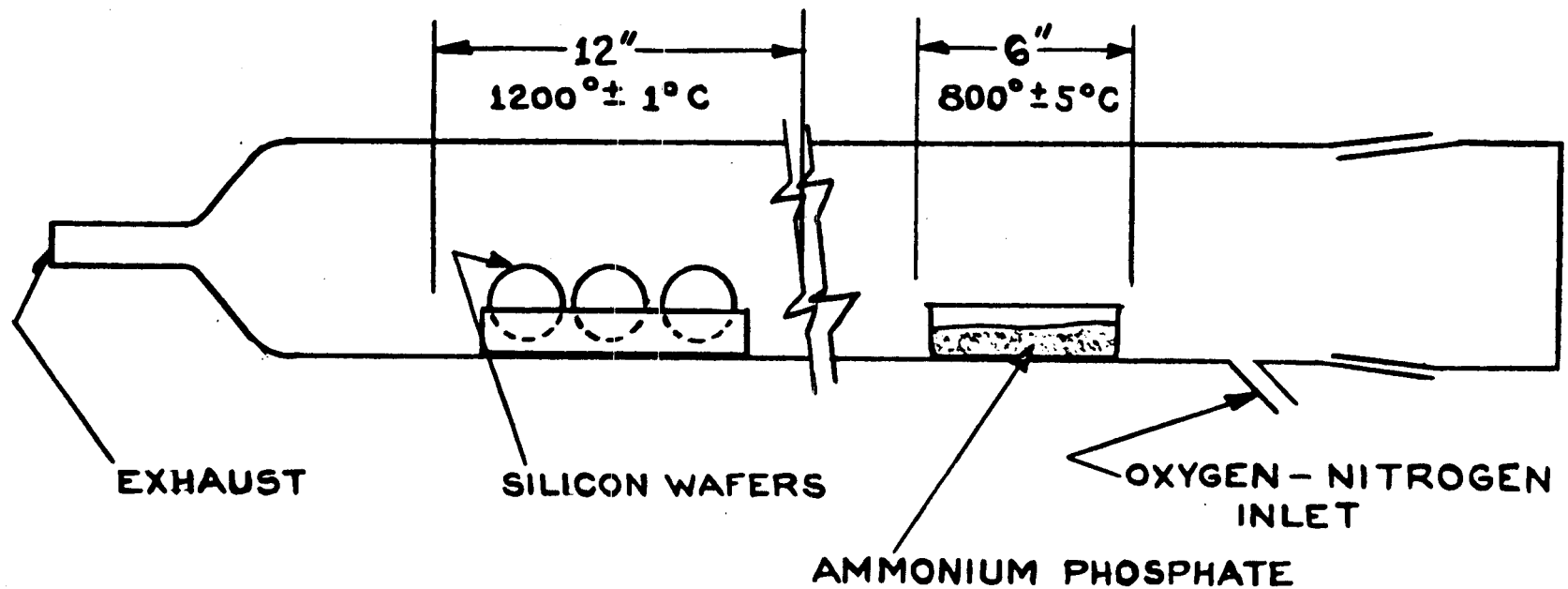

FIGURE 20: N^+ Deposition

minutes. It has been found that extreme care must be taken to properly clean the diffusion boat before each run. If the boat is not given the following cleaning, the diffused wafers were found to have a film on the surface which resulted in an uneven surface concentration of phosphate atoms. The film was in the form of small bubbles which were similar to soap bubbles.

To eliminate these bubbles, the quartz diffusion boats were given the following clean-up after each ammonium phosphate deposit: (1) the boat is placed in boiling deionized H_2O for 5 minutes: (2) rinsed in cold D.I. H_2O for 2 minutes; (3) blown dry with nitrogen; (4) placed in a 1:1 HNO_3:HF acid soak for 30 seconds; (5) rinsed in running D.I. H_2O for 5 minutes; (6) blown dry with nitrogen; (7) dried in a vacuum oven (120°C) for a minimum of 2 hours. This cleaning cycle was found to eliminate this source of a major problem.

It was also found that the ammonium phosphate must be kept very dry prior to its insertion into the source zone of the diffusion furnace tube. This was done by storing the tightly sealed bottle of ammonium phosphate in a desiccator. The source was only removed when a run was to be made and immediately thereafter returned to the desiccator. Efforts were made to keep at a minimum the ammonium phosphate exposed to the atmosphere prior to a run.

After removing the wafers from the N^+ deposit, the oxide is removed with hydrofluoric acid. As was described in Section 2, the sheet resistivity and junction depth are checked at this point. The resistivity must be 1.2-1.7 ohm/□ and the X_J should be 6-12μ for the wafers to be acceptable. Figure 1e shows what the wafer cross section should be at this point.

6. Emitter Mask

Those wafers which have been passed at the in-line test just described are ready for the emitter masking step. The purpose of this step is to

define the desired emitter geometry in the wafer. This is accomplished by exposing a photo resist film with ultraviolet light and subsequently etching the uncoated silicon with an acid etch.

In order to properly coat the wafers, they must be perfectly clean and dry. Since the wafers have just been removed from a high temperature furnace and etched with hydrofluoric acid, there will be no dirt on them. However, care must be taken in drying them. This is best done by first blowing the water rinsed wafers with filtered nitrogen. The wafers are then dried in a vacuum oven (120°C) for 10 minutes. A uniform film of photo resist is then applied using a high speed multi-head spinner (Figure 21). The resist is forced through a 7μ millipore filter onto the wafer. Excess resist is centrifuged from the surface by the spinner. For concentrated KMER, the wafer is spun at 4000rpm for 1 minute. The coated wafer is then placed in a 95°C air oven for 10 minutes. It is then ready for exposure to ultraviolet light.

All mask alignment and exposure is done on an alignment fixture similar to that shown in Figure 22. The coated wafer is placed on a self-leveling vacuum hold chuck which is a feature of the fixture. A flawless high resolution mask is placed in the fixture and the wafer brought up into contact with it. When contact and alignment have been completed, the ultraviolet light is used to polymerize the resist which is not protected by the opaque areas of the photographic mask. The unpolymerized resist is then removed by spraying the entire surface with resist developer (40 lbs/in^2) for 1 minute. This is then followed by an immediate spray with isopropyl alcohol (40 lbs/in^2 - 30 seconds) and then the wafer is blown dry with nitrogen. The entire photo resist image is then inspected on a high power microscope to detect any flaws or defects in the developed image. The following are checked: (1) holes in the resist; (2) ragged

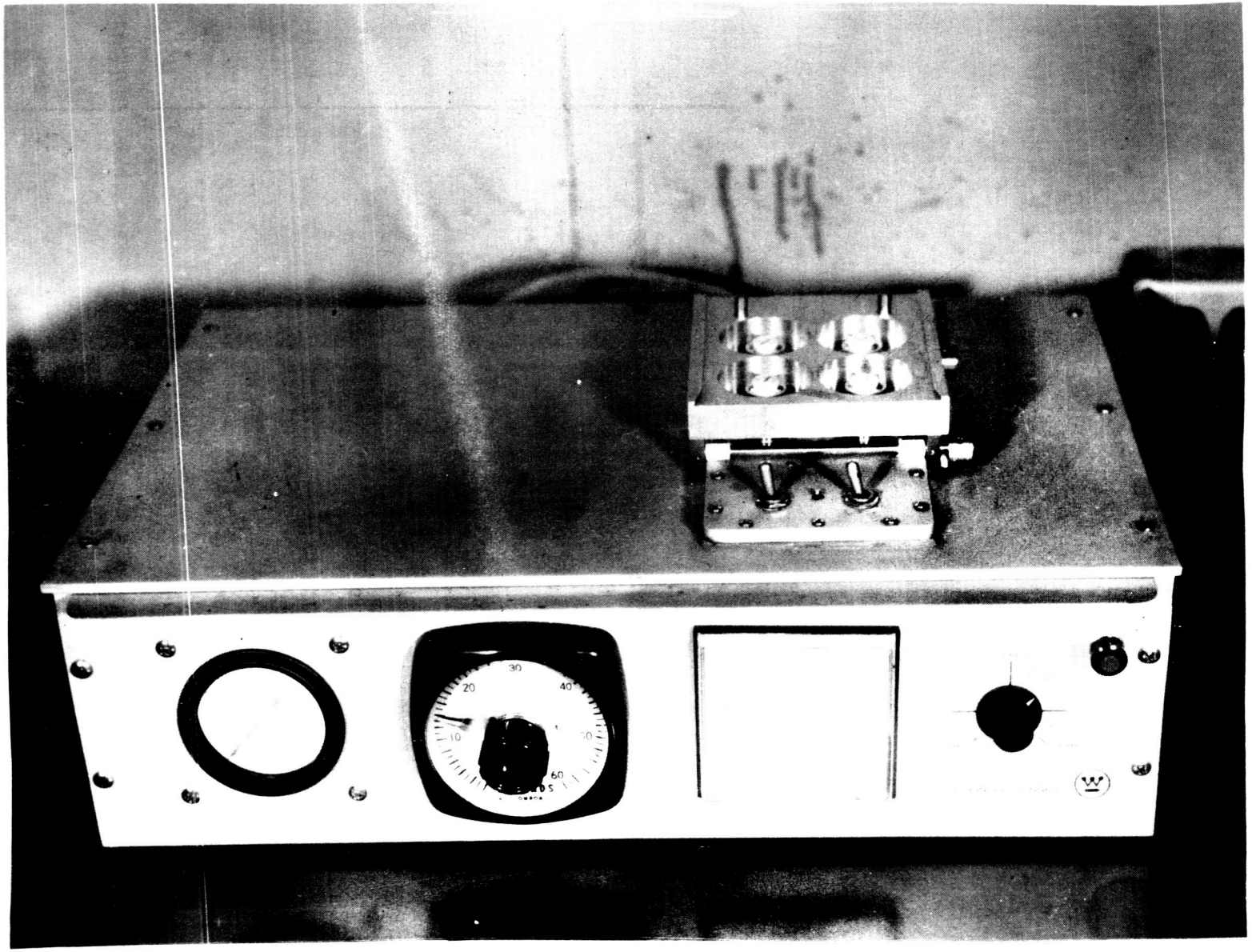

FIGURE 21: High Speed Multi-head Spinner

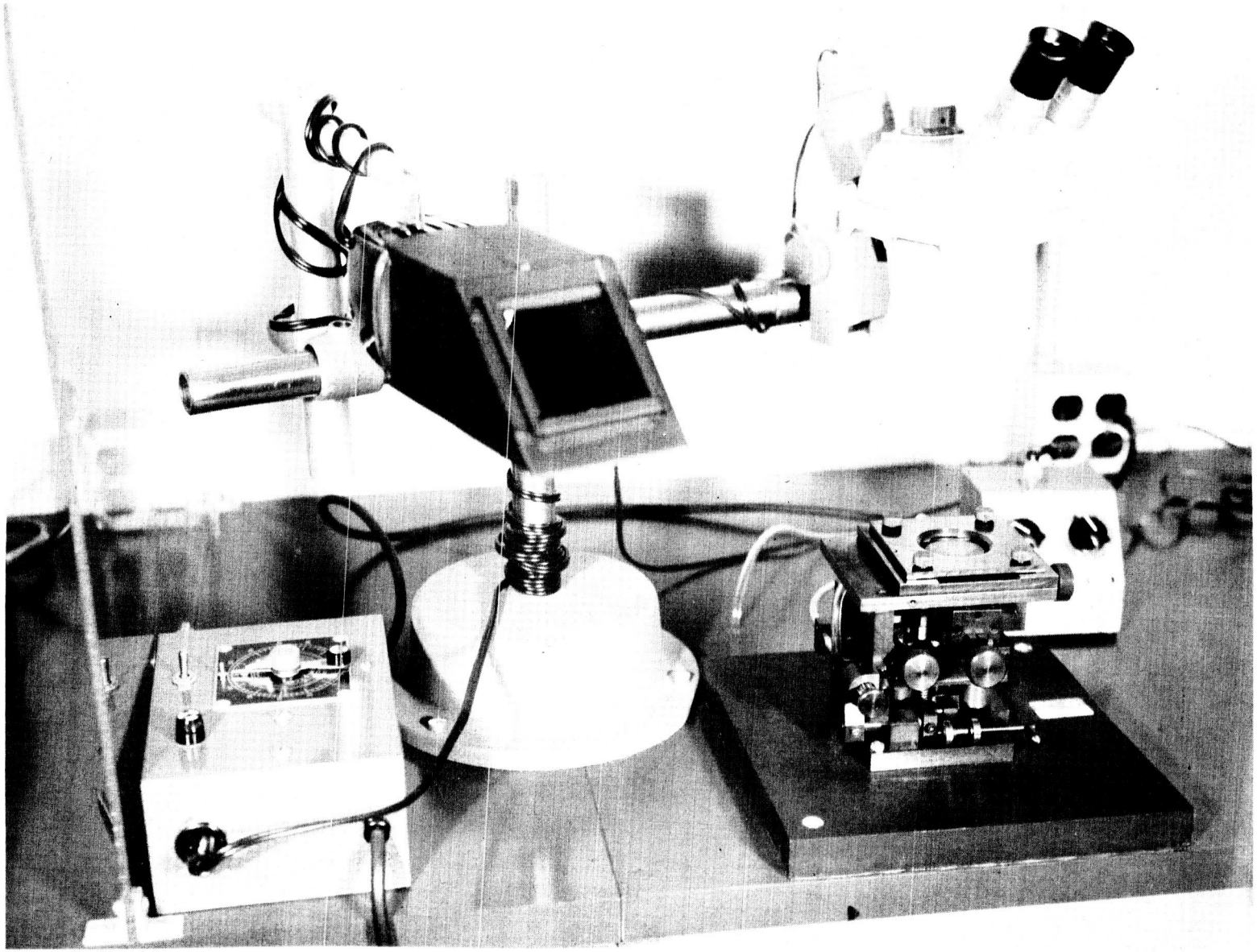

FIGURE 22: Mask Alignment Fixture

edge definition of the resist; (3) incomplete removal of the unpolymerized resist; and (4) improper alignment of the image on the wafer. The inspection is done at 20, 50 and 100X magnification. Those wafers which are defective are then sent to a stripping station to have the resist removed. These wafers can then be recoated, exposed and developed. All wafers which are acceptable are then placed in a 120°C oven for 20 minutes. Figure 1f illustrates the wafer at this stage of processing. All high resolution masks used in this process (emitter and metallization) are produced in-house at Youngwood. In addition to providing quick service, this facility provides a close design-product relationship. The initial concept is first transformed onto rubylith which is accurately cut on a Haagstreit coordinatograph. This enlarged version of the final design must then be scaled-down on a reduction camera to the desired size. Depending on the final size and initial artwork size, 2 or 3 reductions may be required. When a master slice has been produced on a 2" x 2" Kodak high resolution plate, prints can be made using a contact printer. These prints are used in fabricating the actual devices. Since the single device occupies the entire mask, no multiple array of images is required on the mask. However, if such were the case, the facility has a step and repeat camera capable of performing this task.

7. Mesa Etch

The wafers are now ready for the silicon etch which will remove portions of the N^+ layer to define the emitter and base regions. However, the N^+ layer on the collector side must be protected from the etch. This is done by mounting the wafer on a glass slide which is covered with black apiezon wax (see Section 3). After the wax has cooled and hardened, the wafer is etched for 1 1/2 minutes in the following silicon etch:

15 parts HNO_3
5 parts HA_c
3 parts HF.

This etch and time will be sufficient to remove the N^+ layer where the base region of the transistor will be. It is very important that all the N^+ layer be etched away in this region, otherwise an N^+ path will cause the base and emitter regions to be shorted. That this layer has been removed can be proven by probing the etched region with a hot probe. This is a P-N type probe that gives a quick check as to whether the slice is P or N type. If the N^+ layer has not been completely removed, the wafer may be etched further. When the etching is completed, the wafer is removed from the glass slide and the resist stripped off the emitter region. The glass slide is heated to melt the wax and the wafer is slid off into a beaker of hot trichloroethylene. After two subsequent rinses in hot T.C.E. to remove all apiezon wax, the wafers are placed in hot (80°C) J-100 resist stripper. This stripper has been found to be quite adequate as a commercial solvent stripper. The wafers are soaked two more times (10 minutes each) in fresh J-100 to completely remove all traces of the resist. A rinse in isopropyl alcohol is next. This is followed by a thorough D.I. H_2O rinse to remove all stripper from the wafers. The unetched emitter area is shown in the center of the wafer.

The wafers are again subjected to in-line tests to determine if they should be processed further. They are subjected to visual and conductivity tests. The visual inspection is designed to pick out wafers that have imperfections in the emitter geometry or base region. These may result from improper handling (subsequently scratching the resist image) or poor operation techniques (carelessly getting small blobs of wax on the base area before the area was etched). Wafers which have unetched areas in what should be the base region or etched areas within the emitter geometry must be rejected. It is useless to process them further. On a device such as this that occupies a whole wafer, one such imperfection will result in a zero yield for that slice. If a multiple array of devices (smaller area) were fabricated on each wafer, one or possibly even two such imperfections may not dictate the scrapping of a whole wafer.

The conductivity test is performed on all wafers to be certain that the N^+ layer has been removed from what will be the base region of the transistor. A 100% test (performed on all wafers) is done at this stage.

8. P^{++} Deposit

Prior to the simultaneous N^+ diffusion of the emitter and collector regions, a P^{++} deposit is made on the base area. The purpose of this deposition is threefold: (1) to provide an area of high P concentration to which a base contact is made; (2) to provide a high P concentration in the base region which will tend to retard the lateral diffusion in the emitter region, and (3) to provide a low resistivity region in the base to reduce R_{bb}'.

This deposit is done in a BBr_3 atmosphere similar to that described in Section 2. To help mask against this diffusion in the emitter and collector regions, the oxide grown during the N^+ deposition ($\sim$3000Å) is left intact on these regions.

9. Simultaneous Diffusion

The final emitter and collector regions are formed by simultaneously diffusing the N^+ layers into the crystal. This is done at 1250°C in an oxygen-nitrogen atmosphere.

The depth to which the emitter and collector are driven is determined by the wafer thickness and the base width desired. As a result of the simultaneous N^+ diffusions, the base width is the difference between the wafer thickness and the sum of emitter and collector depths:

$$W_B = T - (E_x + C_x)$$

where W_B = base width
T = wafer thickness

E_x = emitter depth

C_x = collector depth.

Since the wafer thickness and base width are known, the depths to which the emitter and collector are to be driven is readily determined. Once this fact is known, the length of time the slice must be exposed to a 1250°C temperature can be calculated. The following relationship is used to figure the diffusion time:

$$t = \frac{(X_J)^2}{4\ D\ \ln \frac{C_s}{C_x}}$$

where t = time in seconds

X_J = junction depth in cm

D = diffusion coefficient of phosphorus in Si at 1250°C

C_s = surface concentration after diffusion

C_x = background concentration of Si bulk.

It has been found that the best results (from a current gain standpoint) are possible when the high temperature cycle is followed by a "slow cooled" period. This "slow cool" restricts the cooling of the wafers from 1250°C to 850°C at a rate of approximately 50°C/hour. A special furnace was programmed to permit the hot zone to cool at this desired rate. Upon reaching the 850°C plateau, the furnace discontinued cooling and maintained this temperature level. This programmed cooling has two distinct advantages over just cooling by turning off the furnace. First, the rate at which wafers cool is constant from run to run. Secondly, when the lower temperature level is reached (850°C) the furnace zone is held at that point. This latter point is very important because if the furnace were just allowed to cool down to room temperature, the quartz tube might crack. This has been found to be the case when such tubes are heated to 1250°C and allowed to cool to room temperature. Often, the 850°C level

was reached at a time during the day when the people were not at work. Since the furnace held the zone at 850°C, the wafers could be left in the furnace until the next morning. They were then slowly withdrawn to room temperature. This programmed "slow-cooling" permits the crystal's original structure and perfection to be maintained. Crystal distortion which results from rapid quenching (1250°C to room temperature in less than 3 minutes) has been found to be detrimental to the gain of the device.

The method of preparing the wafers for this furnace is quite similar to that of any other diffusion cycle. However, in this particular case, the wafers are given a "flash" oxide etch between P^{++} deposition and the simultaneous diffusion. This etch consists of a 10 second dip in a weak hydrofluoric acid solution. The composition of the solution is 1 part HF (48%) to 10 part water. The purpose of this flash etch is to remove the heavily doped oxide from the emitter to minimize the possibility of inversion or compensation of the N-type emitter.

At the conclusion of the diffusion and slow cool cycle, the wafers are slowly brought to room atmosphere (850°C to room temperature in about 3 minutes). A thorough investigation is then made to determine exactly what physical characteristics are possessed by the wafers. The following parameters are checked: sheet resistivity of the base, collector, and emitter regions; junction depth of the emitter, collector and P^{+} regions; and final base width of the device. The sheet resistivity test is straightforward. To check for junction depths, a more elaborate process is involved. Because of the deep junctions, it is best to perform a 90° section through the device, as opposed to a shallow angle (3° or 5°) section. This perpendicular section is accomplished by mounting the sample in a plastic form. For this purpose, Laminac^{R} (American Cyanamid Company) is used. First the sample is held rigid in a position perpendicular to the support on which it is mounted. Next the Laminac, which has had its catalyst (60% methyl ethyl ketone peroxide in dimethyl phthalate)

added is poured around the sample. The solution is allowed to harden (3-5 hours). After complete hardening, the sample is ground and polished using successively Nos. 100 and 240 grit paper on a series of high speed wheels. The final polishing (using diamond paste as the grit) produces a scratch-free sample. After thoroughly cleaning to remove all final grit and oil, the plastic encapsulated sample is ready to be subjected to an acid stain which will delineate the P-N junctions. In this way, all junction depths and base width readings can be obtained. For the purpose here, a simple 45 second HF (48%) etch under an intense, white heat lamp is sufficient. Figures 23 and 24 show typical sections processed in this way. The actual measurements are then made using a Unitron microscope (100X magnification). Those runs which have not had the emitter and collector driven in sufficiently deep (W_B greater than 20μ) can be returned to the diffusion furnace to correct this situation. If the run has physical parameters within the process specifications, the oxide is stripped off both sides with concentrated HF (48%) and sent on to have the collector side mounted on moly.

10. Collector Contacting

Four factors are necessary for successful "hard soldering." These are: (1) removal of surface films; (2) attainment of a proper cycle of time, temperature and atmosphere; (3) planar control (flatness); and (4) surface finish (roughness). Each of these were acted on. The first was achieved by proper extensive cleaning methods; the second, by a high vacuum cycle; planar control, by a lapping operation; and the final factor, by an etching process.

Molybdenum is the base material used for this device. Supplied as punchings, its inherent properties are well known and its substitution was never considered. Through our Manufacturing facilities, punchings were supplied to our design group. As punching diameters increase, the allowable

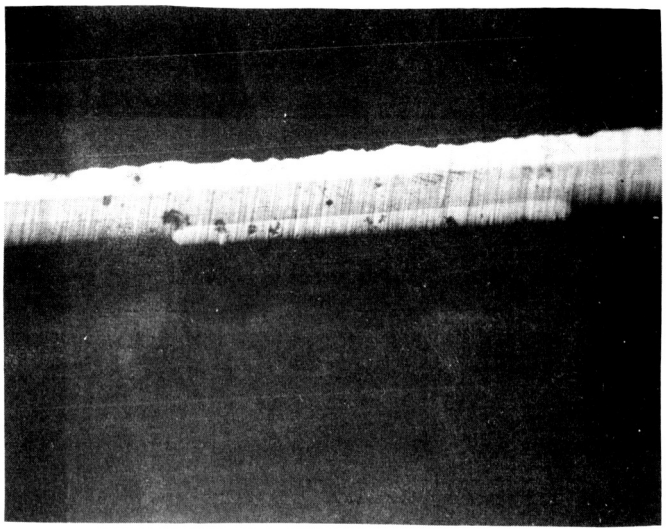

FIGURE 23: Typical Cross Section

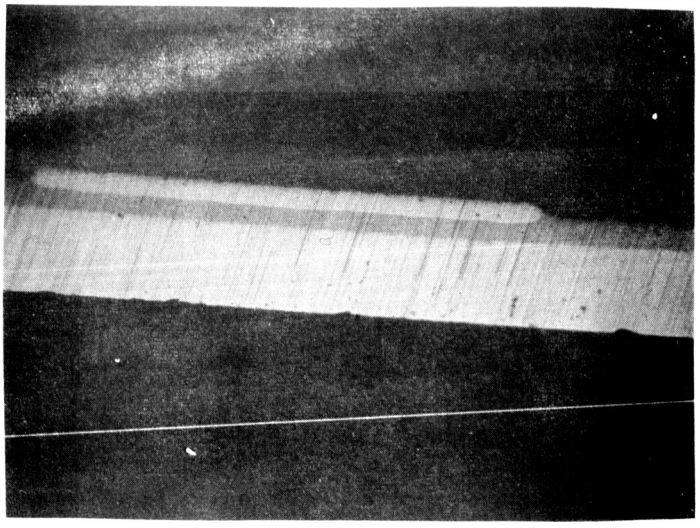

FIGURE 24: P^+ Delineation

bow is difficult to control. The standard allowance is .001" for diameters of .125 to .375". For the larger diameters necessary in this case, another operation was required. Punchings are lapped simultaneously on both sides. This operation decreased the bow to <.0005" with a 5μ finish. This finish appears as a mottled gray. These limits satisfy the planar and surface finish requirements.

The contacting cycle is accomplished in vacuum. The parts are vigorously cleaned and assembled in a "clean box" under exacting cleaning processes. The parts, after being thoroughly dried, must be used within several hours. Any delay will interfere with the process cycle and will severely limit good wetting. The vacuum equipment used is a horizontal vacuum tube (Figure 25); the heating source, an R.F. coil. The temperature is monitored from within the graphite boat. The equipment design allows for easy loading in entering the graphite boat and allows it to be set level. It is easily understood that this must be within 2° of the horizontal. When the tube is sealed, vacuum is applied and allowed to reach a value $>10^{-6}$ Torr. Power is applied allowing temperature to reach 860°C as shown in Figure 26. Power is switched off at this point; the vacuum is no greater than 5×10^{-3} Torr. Units are allowed to cool naturally in vacuum. They are removed from the tube when temperature has reached <100°C.

11. Metallization

Aluminum metallization is used on this device. The film is evaporated by conventional means by the use of tungsten filaments. The film on this large device is used for internal contacting and must be of the quality necessary for the compression bond leads. This necessitates ultra-high vacuum techniques for controlled rates of evaporation. The film must be pure aluminum, homogeneous in structure and of excellent uniformity. The pressures exerted by lead contacting will penetrate any irregularities

FIGURE 25: High Vacuum Contacting Furnace

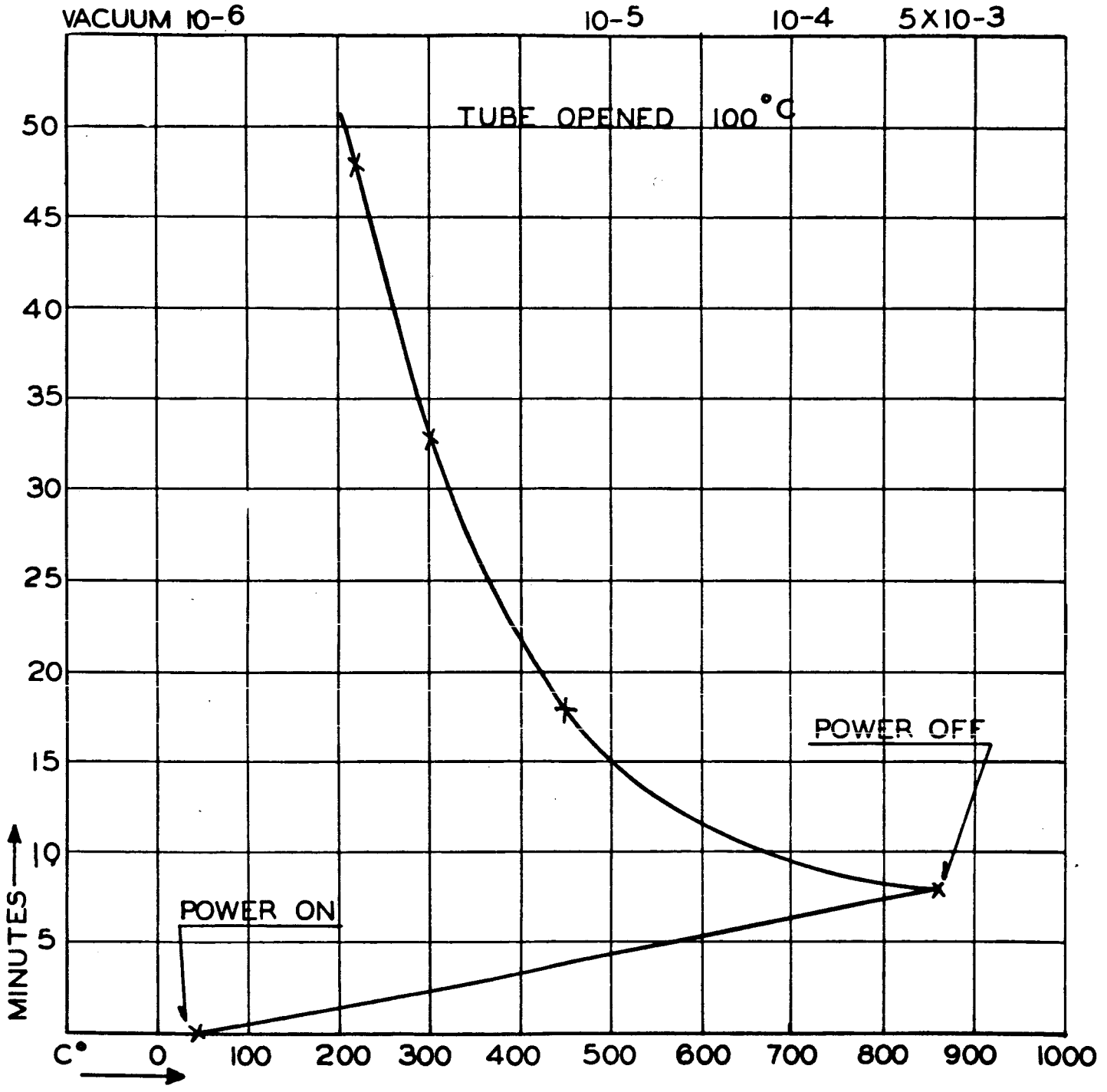

FIGURE 26: Contacting Cycle

and consequently will destroy the unit. After initial preparation, the units are entered in the evaporator for metallization. Units are mounted on a substrate heater and the filaments are charged with the necessary amount of aluminum slugs. The chamber is closed and the roughing cycle is begun. When the pressure of 5×10^{-3} Torr is reached, the high vacuum value is opened. The high vacuum manifold is very extensively trapped (liquid N_2) and vacuum of $>10^{-6}$ Torr is attained. The substrate heater is then switched on and the units are outgassed at 500°C for 10 minutes. At this time the pressure is again equalized and the substrate heater is turned off and the units allowed to cool to 100°C $\pm$ 10°. At this time the filaments are turned on and shields are removed when the oxides have been removed; virgin aluminum is evaporated.

At the end of the cycle the units are allowed to cool to room temperature still under high vacuum condition. At this time, the high vacuum valves are closed and N_2 (6 PPM H_2O) is entered to break the vacuum. Units are carefully removed and stored for further processing. Film thicknesses of 20 to 25KÅ are obtained. Variations of this quantity, if planar, have no effect on the device.

After the aluminum has been deposited over the entire wafer, it must be selectively removed from over the emitter periphery to eliminate emitter-base shorting of the device. This is done by coating the wafer with photo resist and polymerizing that portion where contact to the emitter and base is to be made (the process being quite similar to that outlined in Section 6). In this way, the unmasked area (the emitter edge) is chemically etched with a nitric-phosphoric acid solution that does not cause a break-down of the resist image.

Prior to stripping the resist from the aluminum contacts, the emitter-base breakdown voltage is read. This is done to check for the complete removal of all aluminum along the emitter periphery and to determine what electrical

characteristics can be expected of the devices. If the unit is short (V_{EBO} = short), it is given a short (3-10 seconds) flash etch in 15 parts nitric acid, 5 parts acetic acid and 3 parts hydrofluoric.

Experimental results show that such an etch is usually necessary and quite beneficial to devices fabricated by this simultaneously diffused method. The resist on the aluminum acts to mask the contacts from the vigorous silicon etch. Contact between the metal probes and the aluminum pads can be made by scratching the resist with the pointed probes. Since the edge of the device has not yet been sandblasted away, only the V_{EBO} can be checked at this point.

Those units which exhibit a sharp emitter-base breakdown voltage then have the photo resist stripped from the aluminum. This stripping is also similar to the method described in Section 6. Figure li illustrates the device at this point. All units are then inspected closely at 100X magnification to see that the resist has been completely removed. Those which are resist-free are ready to have the aluminum alloyed.

12. Alloying Cycle

As it is well known, the function of the alloying is to provide contact. The process is done in a continually purged quartz tube, the atmosphere is N_2. This gas, having dew point -92°F (3.5 ppm H_2O), is provided from a central source. The furnace (Figure 27) is continually at alloying temperatures which minimizes any variation in temperatures. A thermocouple of 610°C $\pm$ 2°C. After the temperature has been noted, the thermocouple assembly is moved to the entrance of the tube.

The metallized slices, aluminum side up, are carefully laid on the push rod platform. The platform is quickly returned to the center zone and allowed to remain 3 minutes $\pm$ 5 seconds. At the end of this time, the platform is just as quickly removed to the end of the tube. Here it is

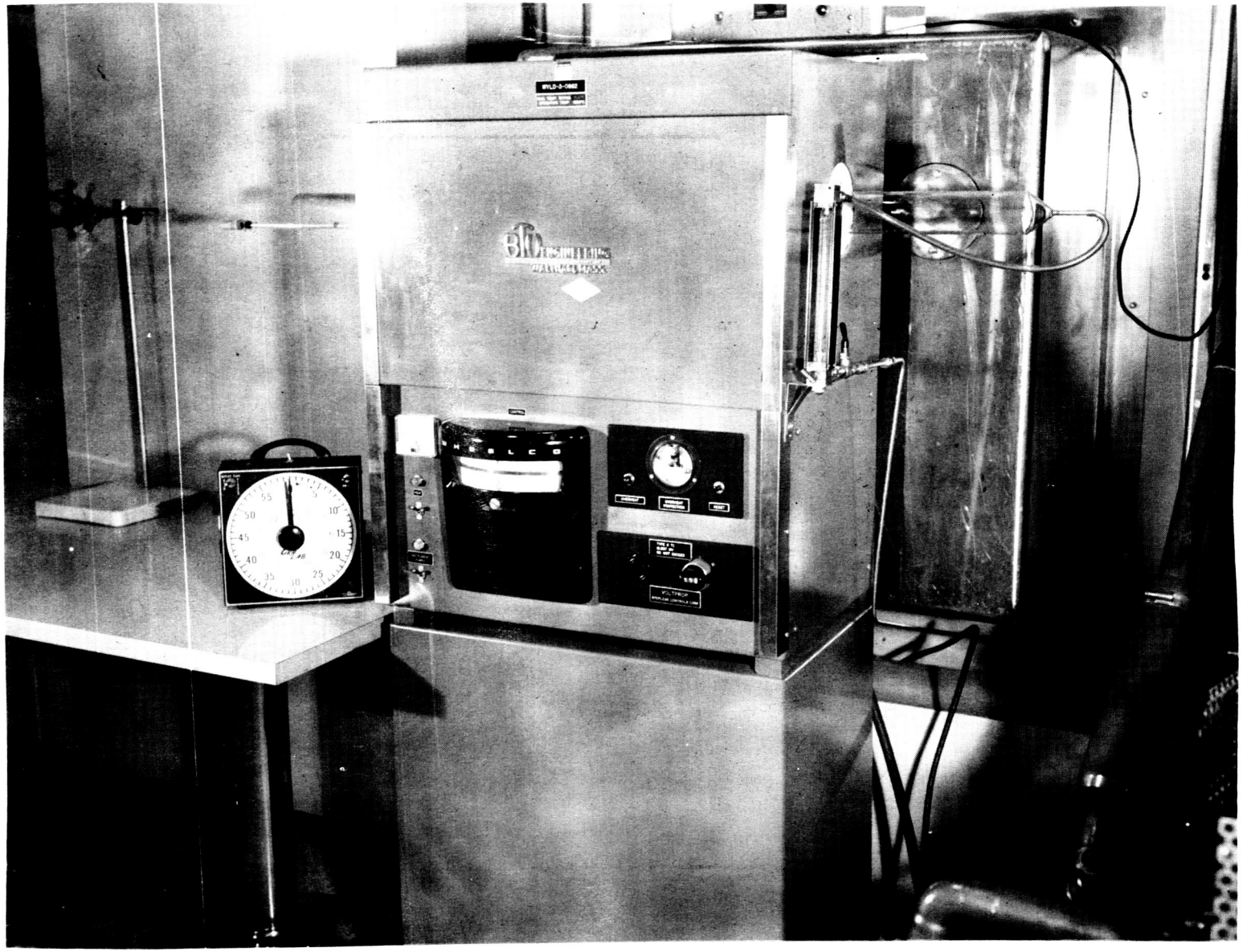

FIGURE 27: Aluminum Alloying Furnace

allowed to cool to <300°C. The slices are then carefully removed and stored. The assembly is then returned to the center of the tube where it remains, being purged and at temperature.

13. Preparation of Collector-Base Junction

As Figure 1 illustrates, the unit must have the edge cleaned up because of the wrap-around collector. This can be eliminated by removing that portion of the wafer which is causing the short. The device (which is soldered to a moly disc) is sandblasted at a high spinning speed while a stream of 9.5μ grit is directed at the silicon. By varying the angle of the nozzle, a beveled edge can be cut into the device. Figure 1 shows the device at the conclusion of this sandblasting step. Although a microscope is attached to this equipment to help determine when the edge removal is complete, a more definite test can be performed on a curve tracer. At this stage, all electrical parameters (voltages and gain) can be checked. Those devices which are not shorted are ready to have the sandblasted edge etched. This etching is to remove the damaged silicon along the collector-base junction. This etching involves directing a jet of 1:1:1 HNO_3:HAc:HF etch along the sandblasted edge as the device is rotating. After a thorough water rinse, the device is dried in a vacuum oven (150°C) for 2 hours. The etched junction is then coated with C1-1 and alizarin coating to protect and preserve the clean silicon junction during subsequent testing and encapsulation operations. The coating is cured for 16 hours at 225°C.

14. Wafer Test - Pre-encapsulation

Prior to encapsulating the units, they are given a thorough electrical test to determine which units should be processed further. The following parameters are checked:

V_{CEO}	$V_{CE(sat)}$
V_{CBO}	B at 1/2A, 1A and 2A
V_{EBO}	

Units exhibiting a V_{CEO} >20 volts are then sent to be encapsulated.

B. PROCESS B - EPITAXIAL-DIFFUSED

1. Epitaxial Base Growth

The details of the epitaxial process are given in the section on material preparation (Section III).

2. Oxidation

After growing the base regions epitaxially, the slices were directly transferred to the oxidation furnace. The oxide layer was deposited at a temperature of 1000°C for 120 minutes to give an oxide thickness of 4000 Å.

3. Sandblasting

The purpose of the sandblasting was to cut the size of the wafer from 1 inch to .93 inch, which was the size of the moly. The slices were mounted with wax on a copper stud and sandblasted to the size of the moly.

4. Emitter Masking

The slices were coated with a uniform film of Kodak Metallic Etch Resist (KMER) using a high speed spinner. (The speed of the spinner was 3000 revolutions per minute and the wafer was spun for 45 seconds.) The coated wafer was placed in an oven and baked for 10 minutes at 95°C. One of the slices from each group was used to fabricate control transistors. The wafer was placed on a self-leveling alignment fixture. The emitter mask was placed in the fixture and the wafer was brought in contact with it. The mask shown in Figure 28 was used for the large area 100A transistor. When the contact and the alignment were completed, an ultraviolet light was used to polymerize the resist which was not protected by the opaque areas of the mask. The unpolymerized resist was then removed by spraying the entire surface with resist developer for 30 seconds. This was then followed by a spray of isopropyl alcohol for 30 seconds. The wafer was blown dry with nitrogen for 30 seconds. The

142-1B

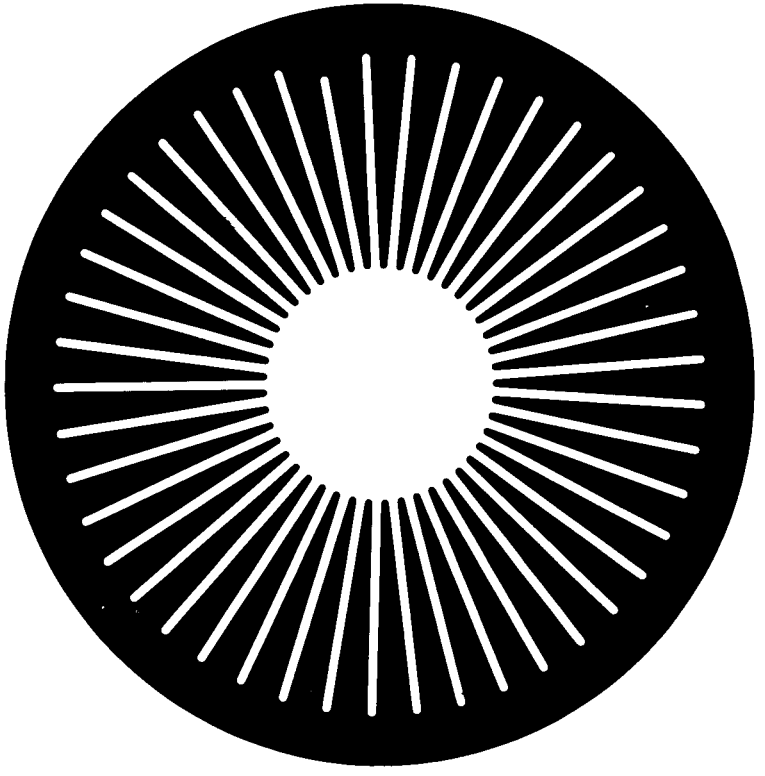

FIGURE 28: Emitter Mask for Large Area 100A Transistor

entire pattern was then inspected under a high power microscope. The slices that showed defective patterns had the photoresist stripped off and were recoated with photoresist and the above process was repeated. These wafers were then baked in an oven for 30 minutes at 150°C. The oxide was then etched to expose the area for the emitter diffusion. It was etched for 5 minutes using a solution containing ammonium fluoride and sulfuric acid in the ratio 6:1. It was then rinsed with deionized water and blown dry with nitrogen. The photoresist was then removed from the top of the slices by placing it in hot sulfuric acid (500°C) for 20 minutes. It was then rinsed with deionized water for 5 minutes and placed in hot deionized water (400°C) for 20 minutes. Finally the slices were blown dry with nitrogen. The slices were then ready for emitter diffusion.

5. Emitter Diffusion

Before emitter diffusion, the slices were given the diffusion cleaning previously explained. The diffusion furnace was maintained at a temperature of 1150°C over a flat zone of 12 inches.

The wafers to be deposited were removed from the plastic container with tweezers and blown dry with N_2 which passed through a millipore filter. The dried wafer was then placed on the N^+ deposit boat, which was located under a heat lamp. After all the wafers have been dried in this manner with the N_2 jet placed under the lamp, the boat is allowed to remain there for 5 minutes.

Prior to actually placing the wafer-holding boat into the diffusion furnace, the diffusion system had to be purged in the following manner: (1) The source was allowed to flow through the diffusion tube for 2 minutes; (2) The source gas was shut off and the system allowed to set for 2 minutes; (3) 1 minute was allowed to load the boat which has been

under the heat lamp; (4) the boat and wafers were permitted to remain in the flat zone for 2 minutes. This was done to allow boat and wafers to reach the flat zone temperature before starting the diffusion cycle; (5) the carrier gas was allowed to flow through the $POCl_3$ source and through the diffusion tube for 50 minutes; (6) at the conclusion of the run, the source was shut off and the wafer permitted to sit in the flat zone for an additional 2 minutes; (7) the boat was withdrawn and the wafer allowed to cool to room temperature.

Upon completion of the N^+ deposition cycle, it is essential that the surface concentration of the deposited layer be determined. This was found from the sheet resistivity (ρ_s) and depth (X_j) of the layer.

The oxide was etched by immersing the wafers in concentrated (48%) hydrofluoric acid for 2 minutes. After the HF etch, the wafers were rinsed in running deionized H_2O for 3 minutes and dried under a heat lamp.

The dried wafer was then placed in the four-point probe and the sheet resistivity read. The junction depth was done by sectioning a portion of a deposited wafer on a 3^o angle block. Such a portion was first mounted on the beveled part of the block with wax. After allowing the wax to harden, the samples were polished on a polishing wheel. The liquid and solid polishing materials were then removed by gently swabbing the sample with a warm, mild soap solution. This was followed with a thorough rinse under running deionized H_2O (at least 1 minute). The sample was then blown dry with filtered nitrogen. It was now ready to be stained with the proper acid to delineate the junction. A photographic record of the interference fringes was then obtained (Figure 29) and thus junction depth was directly measured.

The surface concentration of the deposited layer was determined from Irvin's curves.

FIGURE 29: Photograph of Interference Fringes

6. Emitter-Base Contact Masking

The contact areas on the slices were exposed using the emitter base contact mask. The mask used for the large area 100A transistor is shown in Figure 30. The photomasking and the etching were done as described above. The slices were then mounted on glass plates with the collector side exposed. They were then sandblasted and cleaned to the epitaxial layer on the collector side. The slices were now ready to mount on moly.

7, 8, 9. Collector Contacting, Metallization, and Alloying

These steps are identical to those described under Process A.

10. Mesa Etching

The collector-base junction was exposed by mesa etching. The mesa mask used for the 100-amp transistor is shown in Figure 31. The photomasking, oxide etching and the removal of photoresist were done exactly as described before.

11. Junction Coating

The exposed junction of the 100-amp was carefully coated with glycerin and baked in an oven for 16 hours at 800°C. After 16 hours, the transistors were removed from the oven, were allowed to cool and were tested for electrical characteristics. Those transistors that showed good electrical characteristics were used for encapsulation.

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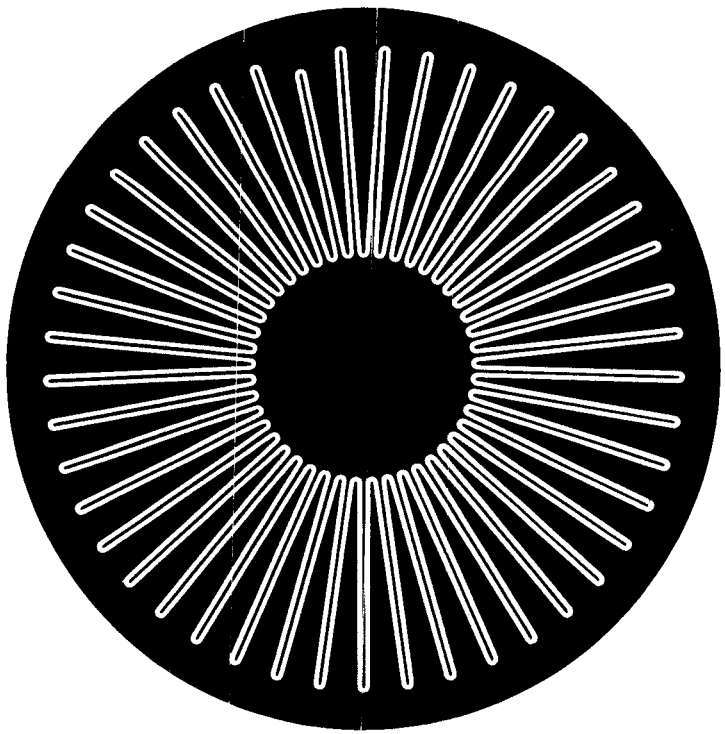

FIGURE 30: Emitter-Base Contact Mask

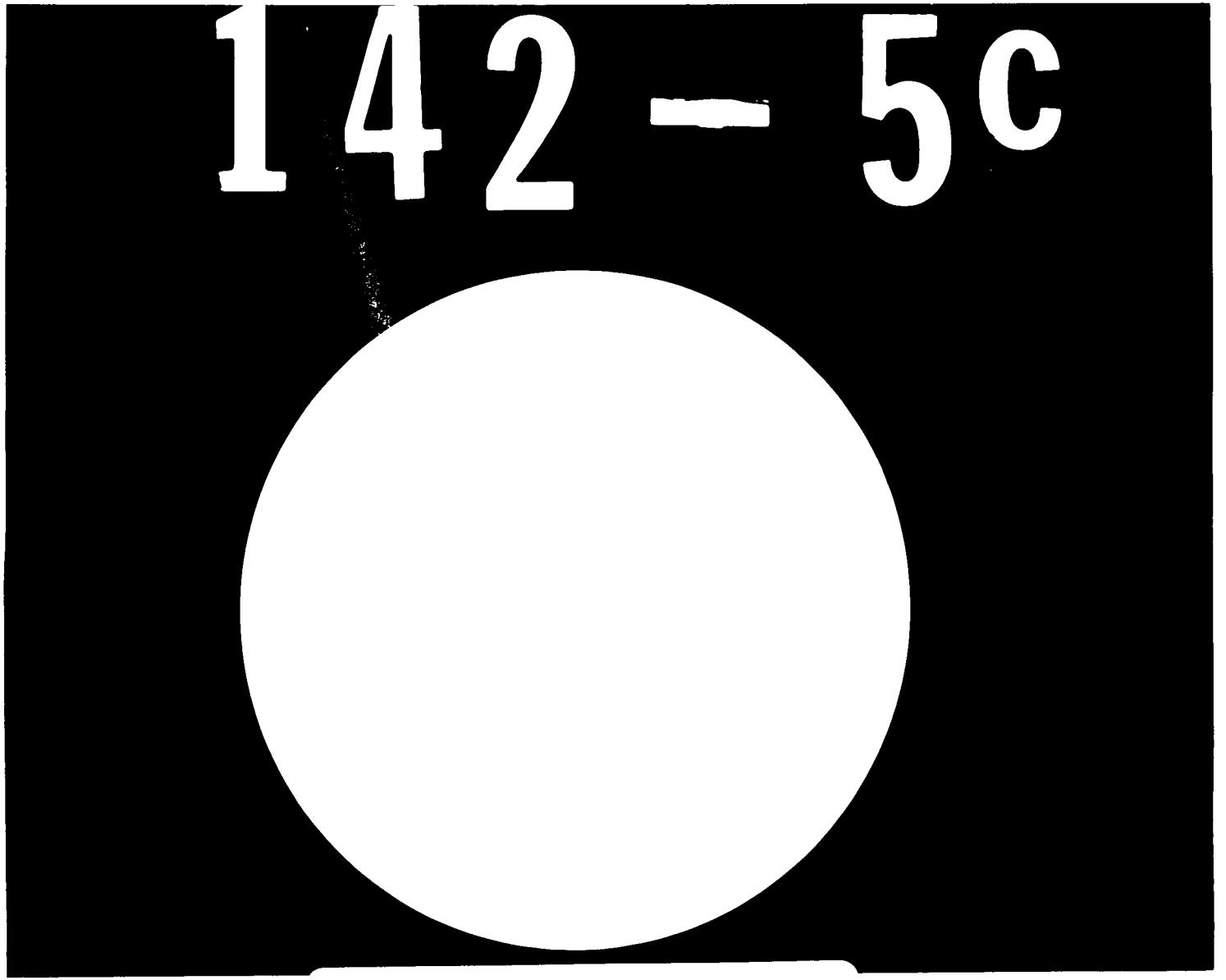

FIGURE 31: Mesa Mask
100A Transistor

V. ENCAPSULATION

A. CUSHIONING MATERIAL

It has long been recognized that excessive localized stresses on a compression bonded device will cause downgrading or even complete failure of the device. Due to the narrow emitter contacting surface, the subject device was especially subject to excessive localized stresses.

In order to spread the compression force required for encapsulation over the whole surface of the device, a search was made for a material with mechanical, electrical and thermal characteristics suitable for intimate contact with the surface of the device. One material that was readily available and uniquely suited to the requirements was Teflon*, type TFE (polytetrafluorethylene).

The literature[9] shows that parts made of TFE deform in time at a decreasing rate. This property can best be explained by the concept of "Apparent Modules of Elasticity." This concept takes into account the initial deformation for an applied stress plus the amount of deformation that occurs with time. At a given compressive force and temperature the initial deformation of TFE occurs within the first few hours. The deformation then levels off to a point where it is negligible.

The electrical properties of TFE in the required thickness far exceed the electrical characteristics of the device. Sleeving of Teflon is

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* Registered trademark of E.I. DuPont de Nemours and Company.

[9] Teflon fluorocarbon resins, Mechanical Design Data, Plastics Department, E.I. DuPont de Nemours and Company, Wilmington, Del. Fluorocarbon Plastics - Materials and Process Manual, Materials in Design Engineering, February 1964.

already being used as lead wire insulation inside many of the Westinghouse transistors and controlled rectifiers.

The above-mentioned literature shows that TFE is useful from -267°C to +260°C. This far exceeds the rating of the subject device. Since TFE is enert to almost all chemical reactants it is an ideal substance to mate to the entire surface of the device.

B. DEVICE COMPONENTS

The components of the subject device are shown in Figure 32. Following is a brief description of each:

Base - Machined from P.D. 135 provides a threaded stud to attach to a heat sink, a good thermal path from basic fusion to heat sink, and a pedestal on which the basic transistor is mounted.

Integral Case - Externally it provides the hex to hold or tighten the device to a heat sink and the weld projection to which the ceramic-metal seal is welded. Internally it locates the compression components and contains the groove for the retaining ring that maintains force on the device.

Silver Braze - Means for attaching the silver disc to the pedestal.

Silver Foil - Provides the mounting surface for the collector side of the basic fusion. It is brazed to the pedestal of the base and then machined flat. A second silver foil is used as a cushioning disc to allow intimate contact between the silver foil on the pedestal and molybdenum of the basic device, thereby lowering the contact resistance.

Emitter Contact Assembly - (Figure 33) Consists of a teflon washer with a thin silver foil wrapped around the O.D. to make contact to the emitter lead on top and the narrow contact surface of the device.

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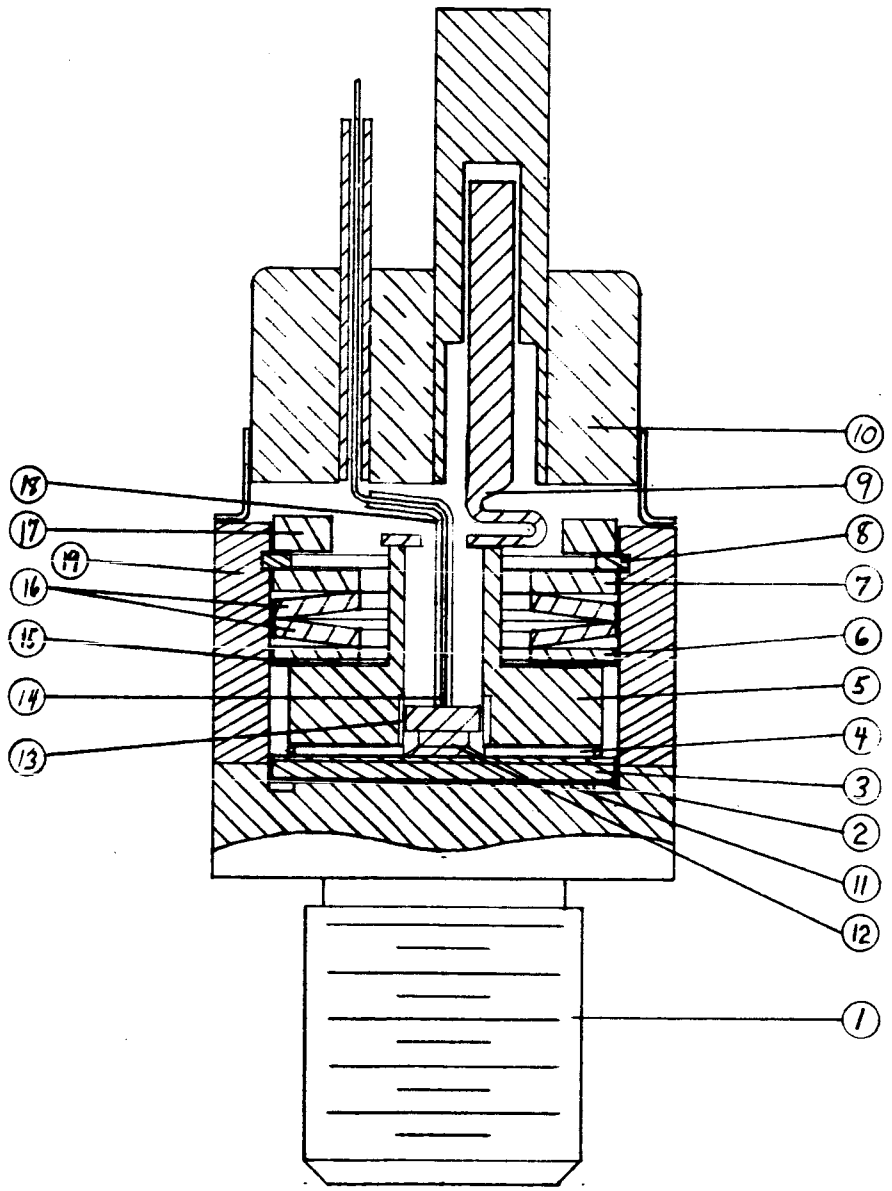


1. base
2. silver foil
3. basic transistor
4. emitter contact
5. emitter lead
6. flat washer
7. flat washer
8. retaining ring
9. silver emitter lead
10. ceramic-metal seal
11. silver pedestal
12. base contact
13. Teflon insulation
14. base lead wire
15. mica insulation
16. Belleville springs
17. molecular sieve
18. base lead insulation
19. integral case

FIGURE 32: Components of 100-Amp Encapsulation

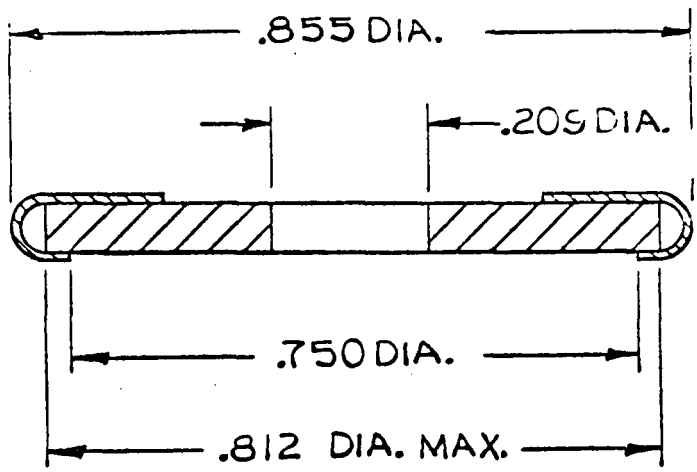


FIGURE 33: Details of Emitter Contact

Emitter Lead - (Figure 34) Made up of three distinct regions. The first which transfers force to the top of the emitter contact assembly and makes contact with it, the center tube which encloses and locates the base contact components and carries the emitter current and voltage part way to the ceramic-metal seal, and the silver ribbon and rod which provides the connection between the emitter tube and ceramic-metal seal.

Base Contact - (Figure 35) A silver button with a reverse chamfer which allows the teflon of the emitter contact assembly to flow over and up the chamfer, thereby holding it in place and providing the force to assure proper contact.

Base Lead Wire - Provides the connection between the base contact and ceramic-to-metal seal.

Base Contact Insulation - Insulates the base contact from the emitter lead and helps locate the base contact.

Base Lead Wire Insulation - Insulates the base lead wire from the emitter and collector portions of the device.

Mica Insulation - Isolates the emitter and collector regions of the device.

Flat Washer - Provides a flat bearing surface for the Belleville washers; and by exchanging washers of various thicknesses, the proper force may be maintained on the device.

Belleville Springs - Used in this device as two in series to provide the required force on the device.

Flat Washer - A .060" thick steel washer used to maintain the force on the device after it is removed from the press.

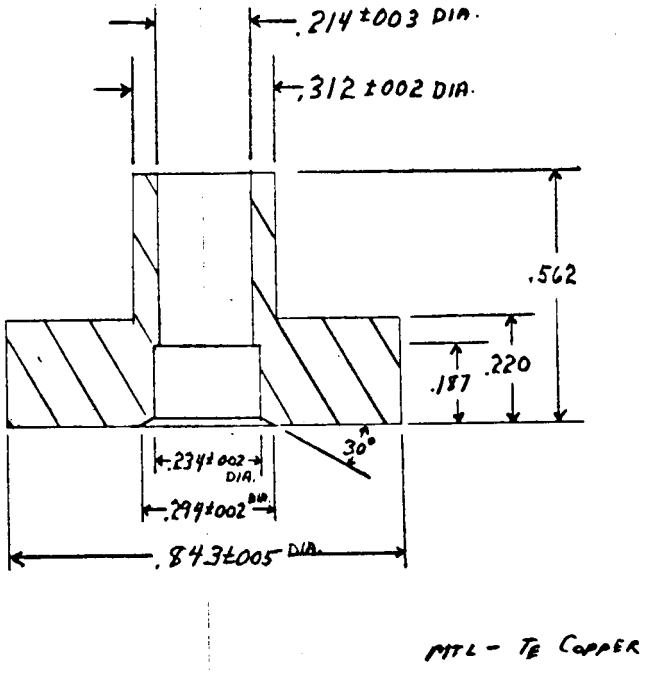
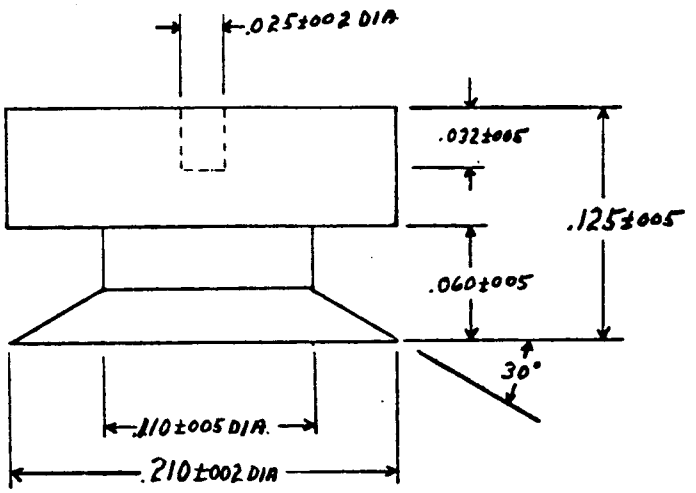


FIGURE 34: Emitter Lead



NOTE - NO BURR OR PROJECTION ON BOTTOM SURFACE

MTL - SILVER

FIGURE 35: Base Contact

Retaining Ring - When force is applied to the device in the press, the retaining ring is snapped in place in a groove in the inner wall of the integral case. This ring prevents the springs from relaxing when force is removed.

Molecular Sieve - A moisture getter that is placed in the device to prevent downgrading due to moisture contamination.

Ceramic-to-Metal Seal - Welded to the integral case, it provides a hermetic seal and the means of attaching external leads to the emitter and base.

C. CONTACTING ELEMENTS

The characteristics of teflon mentioned above have been put to good use in the design of the base and emitter contacting elements of this device.

The emitter contacting element is shown in detail in Figure 33. It consists of a washer of teflon with a silver foil wrapped around the outside diameter so that contact is made on the bottom with the emitter contact area of the basic transistor and on the top to the larger emitter lead. The foil was formed around the outside diameter of the teflon washer in the form of an arch to conform to the stress-strain characteristics of the teflon.

When force is applied to the teflon, it deforms plastically and elastically in all directions to conform to the configuration of the surfaces which oppose it. This deformation takes place at a decreasing rate so that in a short period of time a semi-rigid state is reached that transmits the force of the Belleville washers evenly over the whole surface of the transistor element.

Evidence of the deformation has been observed on contacts removed from devices by the impression of the surface of the basic transistor on the mating surface of the teflon washer.

The base contact (Figure 35) was designed to make use of the inward expansion of the emitter washer. By machining a reverse chamfer on the base contact, the emitter teflon was guided over this chamfer so that a part of the force applied to the emitter by the Belleville washers was used to apply force to the base contact. A teflon sleeve was inserted into the inside diameter of the emitter lead to isolate the loose contact.

It was very important that in designing the collector contact, to keep in mind that it is through this contact that the heat generated within the basic fusion flows to be dissipated in the base and heat sink. This required that the molybdenum mounting disc of the basic fusion and the base be in intimate contact. To enhance the intimate contact between the basic fusion and the base, a lead soft silver disc was placed between them. The purpose of this disc was to fill as many voids (due to lack of flatness and surface finish) as possible in both the molybdenum mounting disc and pedestal surface.

Upon examining the foil after disassembly, the imprint of the molybdenum and the base surface irregularities were clearly visible; indicating that the silver foil was performing as intended.

D. PRE-ENCAPSULATION PROCEDURE

All components except the mica insulators are thoroughly degreased in trichlorethylene. The mica is baked and stored in vacuum at 150°C for 12 hours prior to assembly.

1. A silver disc was placed inside the integral case and seated on the pedestal of the base.

2. A basic transistor element was seated on the silver foil.

3. The teflon insulating sleeve was placed over the base contact.

4. A teflon insulating tube was placed over the base lead wire.

5. The base lead was inserted through the inside diameter of the emitter teflon contact, centered, and the insulating sleeve (step 3) was seated against it.

6. The emitter lead was placed over the gate lead wire and the base contact and teflon insulation seated in the counterbore of the inside diameter.

7. Mica, a .035" thick flat washer, two Belleville springs in series with bottom washer concave, and a .060" thick flat washer were seated in turn on the top of the fusion.

10. The base with the loose assembly was placed in a Carver Laboratory Press and a force of 700-900 lbs. was applied.

11. The retaining ring was snapped in place and the pre-encapsulated device removed from the press.

E. FINAL ENCAPSULATION PROCEDURE

For the final encapsulation procedure, the parts involved were prepared as follows. The ceramic-metal seal was leak tested, degreased, and baked in vacuum at 175°C for 4 hours. The molecular sieve was baked at least 16 hours in vacuum at 300°C. They were then stored in vacuum at 150°C. The pre-encapsulated assembly was baked in air at 175°C for 4 hours prior to the final encapsulation.

All components in this section are shown in Figure 32.

Procedure

1. The molecular sieve was placed over the leads and seated inside the integral case on the snap ring.

2. The base lead wire was guided through the base lead connector as the ceramic-metal seal was placed over the emitter lead and seated on the weld ring.

3. The base lead wire was pinch welded inside the connector.

4. The ceramic-metal seal was resistance welded to insure hermeticity of the assembly.

5. The emitter lead connector was then crimped in place.

6. The device was leak tested and plated with nickel.

The final encapsulation was then complete and the devices were ready for final electrical testing.

VI. TEST RESULTS

A. ELECTRICAL TESTS

Electrical tests were performed at various stages of the fabrication.

1. Voltage

The voltage capability of the 100-amp transistor was tested before encapsulation and the units that showed poor voltages were rejected. The transistors that showed good voltages were encapsulated and the electrical tests were again performed to insure the encapsulation step had not degraded the units. The electrical circuits used to measure the collector-emitter breakdown voltage (V_{CEO}) and the sustaining voltages are given in Figures 36 and 37.

Voltage measurements were also made at different temperatures. The units were stacked in a temperature controlled oven and the voltage reading was taken at 25°C and 100°C. The results are shown in Table II.

2. Saturation Voltage

The saturation voltages were measured by using a Dynatron pulse tester. The circuit used to measure the collector-emitter saturation voltage, $V_{CE(sat)}$ and the base-emitter saturation voltage, $V_{BE(sat)}$, is shown in Figure 38. A pulse width of 300μsec and a duty cycle <2% was used for the test. In the common emitter circuit, the base drive = 1.5 X_B was applied. The collector current was driven up to 20A, 40A, 60A and 75A and the $V_{CE(sat)}$ and $V_{BE(sat)}$ were read directly. The specified base drive, I_B = 5A, was also applied to measure $V_{CE(sat)}$ at 75A. The results of the tests are given in Table III.

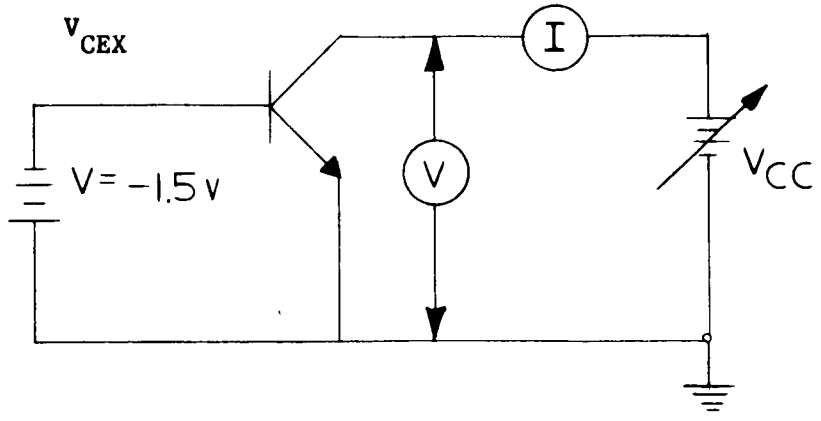


FIGURE 36: Collector-Emitter Sustaining Voltage Test Circuit

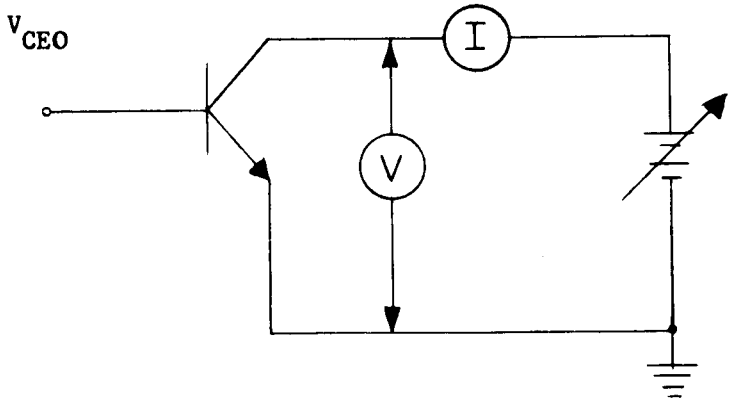
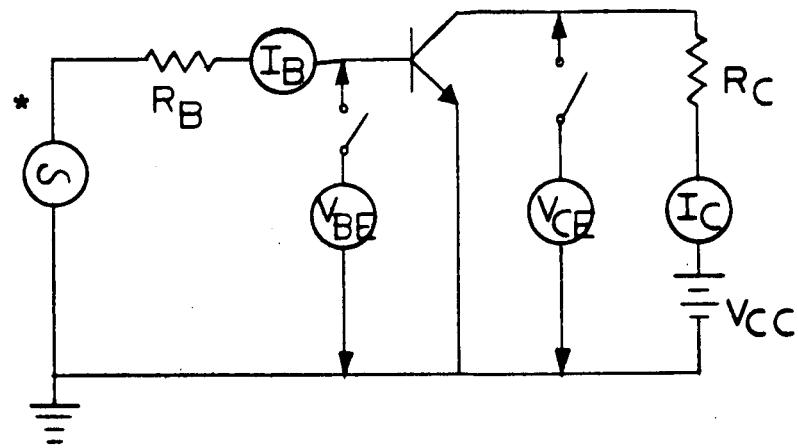


FIGURE 37: Collector-Emitter Breakdown Voltage Test Circuit

TABLE II

BREAKDOWN VOLTAGE AND SWITCHING CHARACTERISTICS (Single Diffused)

	25°C				100°C				25°C					
Unit No.	V_{CBO} V/ma	V_{CEO} V/ma	V_{EBO} V/ma	V_{CEX} V/ma	V_{CBO} V/ma	V_{CEO} V/ma	V_{EBO} V/ma	V_{CEX} V/ma	t_d µs	t_r µs	t_{d+r} µs	t_s µs	t_f µs	t_{s+f} µs
84-10-1	5/5 14/100	4/10 5/100	2/5 4/27	5/10 6/100	10/5 20/10	2/10 7/100	 33/5	3/10 8/100	0.4	1.6	2.0	5.1	2.5	7.5
84-1	20/.02 46/5	20/.02 34/10	 20/5	20/.04 36/10	20/2 24/5	20/7 21/10	2/5 2/100	20/.39 30/10	0.4	1.6	2.0	5.5	2.0	7.5
81-10-1	18/5 26/100	2/10 8/100	3/5 16/100	2/10 8/100	3/5 6/100	1/10 2/100	1/5 4/100	2/10 3/100	.5	2.0	2.5	3.0	7.0	10.0
84-1B	3/5 6/100	1/10 2/100	1/5 4/100	2/10 3/100	20/2 28/5	20/2 39/10	--- 1/5	20/1.8 39/10	.5	1.5	2.0	7	2.5	9.5
88-1	6/5 16/100	6/10 13/100	--- 	7/10 13/100	6/5 20/100	7/10 13/100	2/5 4/80	8/10 14/100	.4	1.8	2.2	5.0	7.0	12.0
84-5-1	76/.01 ---	73/.01 ---	2/5 4/66	20/.01 77/10	11/5 14/100	2/10 6/100	--- 4/1.4	2/10 6/100	.4	1.6	2.0	4.5	1.5	6.0
83-2	4/5 13/100	--- 4/100	--- 4/5	--- 4/100	3/5 13/100	1/10 6/100	--- 4/5	--- 6/100	.3	1.7	2.0	4.0	2.0	6.0
87-1	14/5 22/100	1/10 2/100	 24/5	 1/100	4/5 14/100	--- 2/100	--- 6/5	--- 2/100	-	-	-	-	-	-
84-51A	12/5 18/100	--- 5/100	--- 23/5	--- 5/100	79/5 ---	76/10 ---	4/7.8 ---	80/10 ---	.4	1.6	2.0	7.5	10.5	18
75-B	2/5 6/100	--- 2/100	2/5 4/56	--- 2/100	--- 7/100	--- 4/100	--- 4/37	--- 3/100	.4	2.1	2.5	3.5	4.0	7.5



*Pulse test, duty cycle $\leq$ 2%, pulse width = 300μsec. In the common emitter circuit, the specified I_B (2X overdrive) is applied, the collector supplied is driven until 100A is across the collector-emitter. $V_{CE(sat)}$ and $V_{BE(sat)}$ is a direct reading.

FIGURE 38: $V_{CE(sat)}$ and $V_{BE(sat)}$ Test Circuit

TABLE III

SATURATION VOLTAGE TEST RESULTS (Single Diffused)

Unit No.		I_C = 20A I_BX 1.5		I_C = 40A I_BX 1.5		I_C = 60A I_BX 1.5		I_BX 1.5		I_C = 75A I_B = 5A	
		$V_{CE(sat)}$	$V_{BE(sat)}$	$V_{CE(sat)}$	$V_{BE(sat)}$	$V_{CE(sat)}$	$V_{BE(sat)}$	$V_{CE(sat)}$	$V_{BE(sat)}$	$V_{CE(sat)}$	$V_{BE(sat)}$
81-10-1	25°C	.10	.71	.18	.84	.38	.95	.30	1.06	.27	1.12
	100°C	.10	.60	.21	.75	.30	.95	.35	1.70	.30	1.70
84-1	25°C	.10	.75	.18	.85	.29	.98	.35	1.08	.34	1.09
	100°C	.10	.60	.29	.72	.35	.92	.42	1.02	.42	1.07
84-10-1	25°C	.05	.68	.20	.78	.30	.82	.37	.89	.20	.96
	100°C	.15	.52	.18	.63	.21	.72	.29	.80	.21	.88
84-1B	25°C	.08	.95	.12	1.28	.18	1.50	.23	1.6	.28	1.70
	100°C	.13	.62	.20	.74	.31	.92	.48	1.2	-	1.22
88-1	25°C	.12	.70	.19	.83	.42	.95	.38	1.08	.32	1.10
	100°C	.13	.60	.22	.82	.35	.89	.41	1.0	.39	1.02
84-5-1A	25°C	.10	.61	.23	.75	.34	.83	.29	.92	.19	.99
	100°C	.10	.51	.18	.62	.22	.75	.28	.83	.20	.90
83-2	25°C	.10	.69	.13	.79	.44	.86	.32	.91	.22	.93
	100°C	.19	.51	.12	.68	.31	.72	.40	.79	.25	.86
87-1	25°C	.10	.65	.28	.75	.40	.82	.32	.91	.20	1.02
	100°C	.13	.52	.50	.65	.40	.73	.40	.75	.28	1.0
84-5-1	25°C	.10	.76	.22	.90	.32	1.02	.48	1.10	.40	1.13
	100°C	.10	.83	.28	1.2	.40	1.59	.52	1.62	.61	1.55
75-B	25°C	.10	.65	.21	.73	.50	.80	.54	.85	.16	.93
	100°C	.10	.50	.22	.60	.26	.69	.32	.72	.20	.89
*33-8	25°C	.12	.68	.35	.78	.72	.85	.79	.92	.22	.98
	100°C	.15	.55	.29	.68	.51	.75	.65	.82	.26	.90

*Epitaxial Design

3. Current Gain

The current transfer ratio (h_{FE}) at low current level was tested with a Tektronix curve tracer and the corresponding reading at high current level was made with a Dynatron pulse tester. The electrical circuit used is shown in Figure 39. In the common-emitter circuit, the specified voltage (1V) was applied between the collector and the emitter; and then the specified collector current of 20A, 40A, 60A and 75A was applied. The base current was then measured and the forward current transfer ratio was calculated using

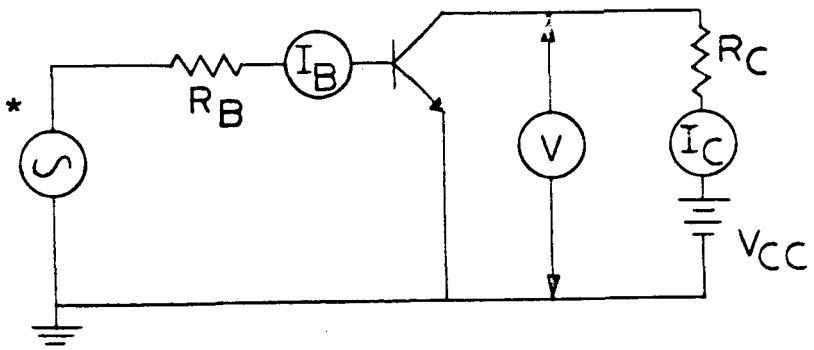
$$h_{FE} = \frac{I_C}{I_B}.$$

The results are shown in Table IV. This Table gives the current transfer ratio as a function of collector current for a number of typical units. Figure 40 shows h_{FE} of three transistors as a function of collector current. It is seen from the Figure that h_{FE} is fairly uniform over the operating range of collector current; this is essential to minimize the switching characteristics.

4. Switching Tests

The switching tests of the transistors were performed using the circuit shown in Figure 41. The test conditions are also given in this Figure. The typical display for the switching test is shown in Figure 42. The device was mounted on an appropriate heat sink. $I_{B(on)}$ and $I_{B(off)}$ was measured for each test, since I_B in each case might vary with input impedance. V_{CE} was applied until I_C was measured to be 20A. Because of the limitation of the circuit, the switching measurement was conducted only up to 20A. The results of the tests are given in Table I.

The electrical characteristics of the five final transistors delivered to JPL are shown in Table V.



*Pulse test, duty cycle $\leq$ 2%, pulse width = 300μsec. In the common emitter circuit, the specified voltage (4V) is applied between the collector and emitter, the specified collector current (1-100A) is applied. The base current is then measured. The forward current transfer ratio is calculated as $h_{FE} = \frac{I_C}{I_B}$.

FIGURE 39: Circuit to Test Current Transfer Ratio

TABLE IV

RESULTS OF CURRENT RATIO TESTS (Single Diffused)

Unit No.	h_{FE} at 25°C				h_{FE} at 100°C			
	20A	40A	60A	75A	20A	40A	60A	75A
81-10-1	47.5	41	35.5	30	44	48	30.5	25
84-1	35	34.2	30	26.8	32	40	26	23.4
84-10-1	71.5	74.5	62	59	127	82	65.5	62.5
84-1B	38.6	26.6	22.2	19.6	22.5	21.2	17.6	15
88-1	49	40	35.5	28.6	69	44	33.0	26.8
84-51A	110	73.5	54.5	45.5	122	68.0	57.0	42.0
83-2	69	48.2	43.5	34	90	53	40.0	32.0
87-1	210	173	136	105	257	165	113	84.5
84-5-1	30.4	28.2	24.6	22.7	29.5	26.3	21.4	17.5
75-B	126	97.5	75	68	125	90	68	57.5
*33-2	200	173	146	100	271	200	160	130

*Epitaxial Design

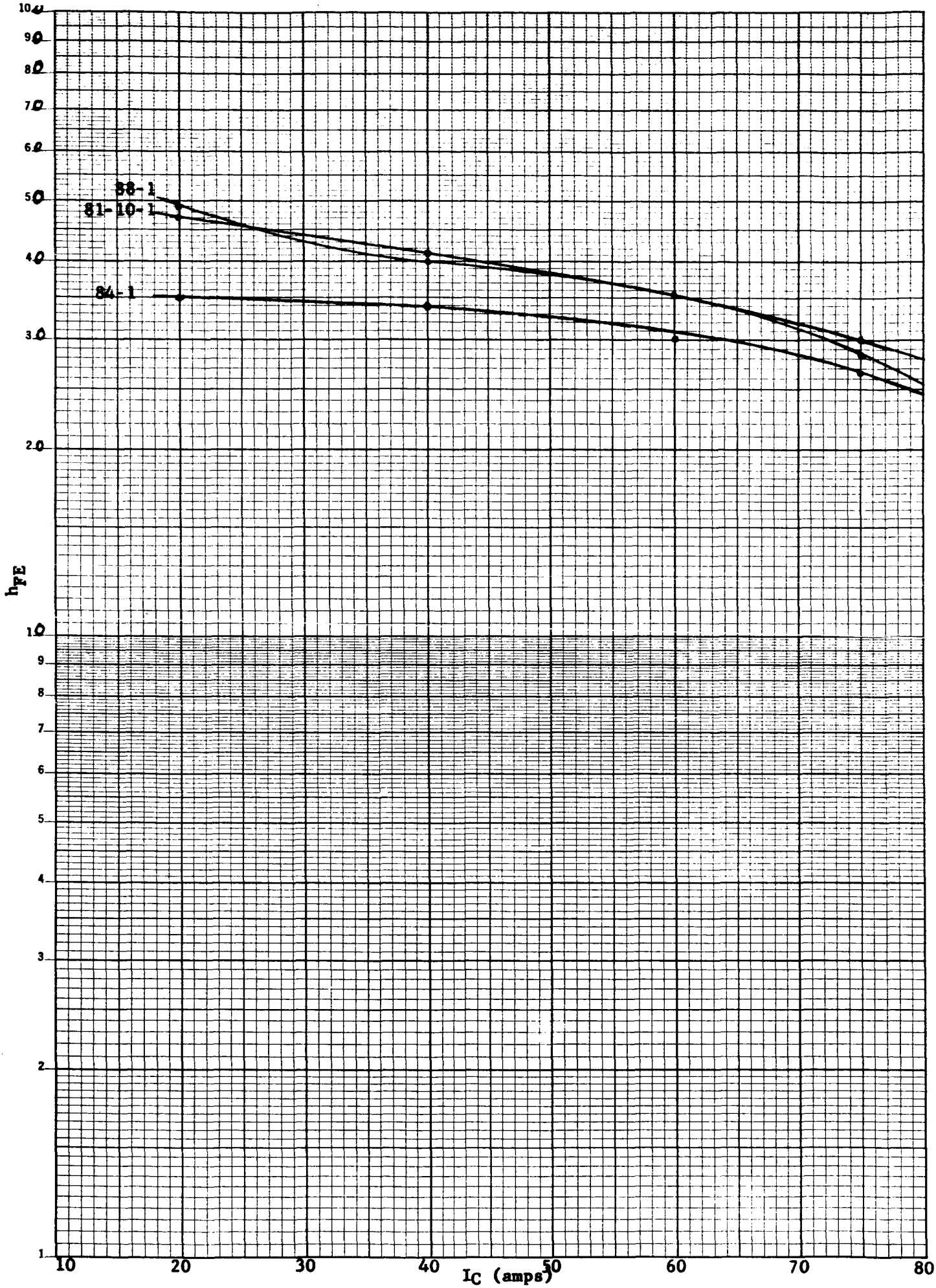
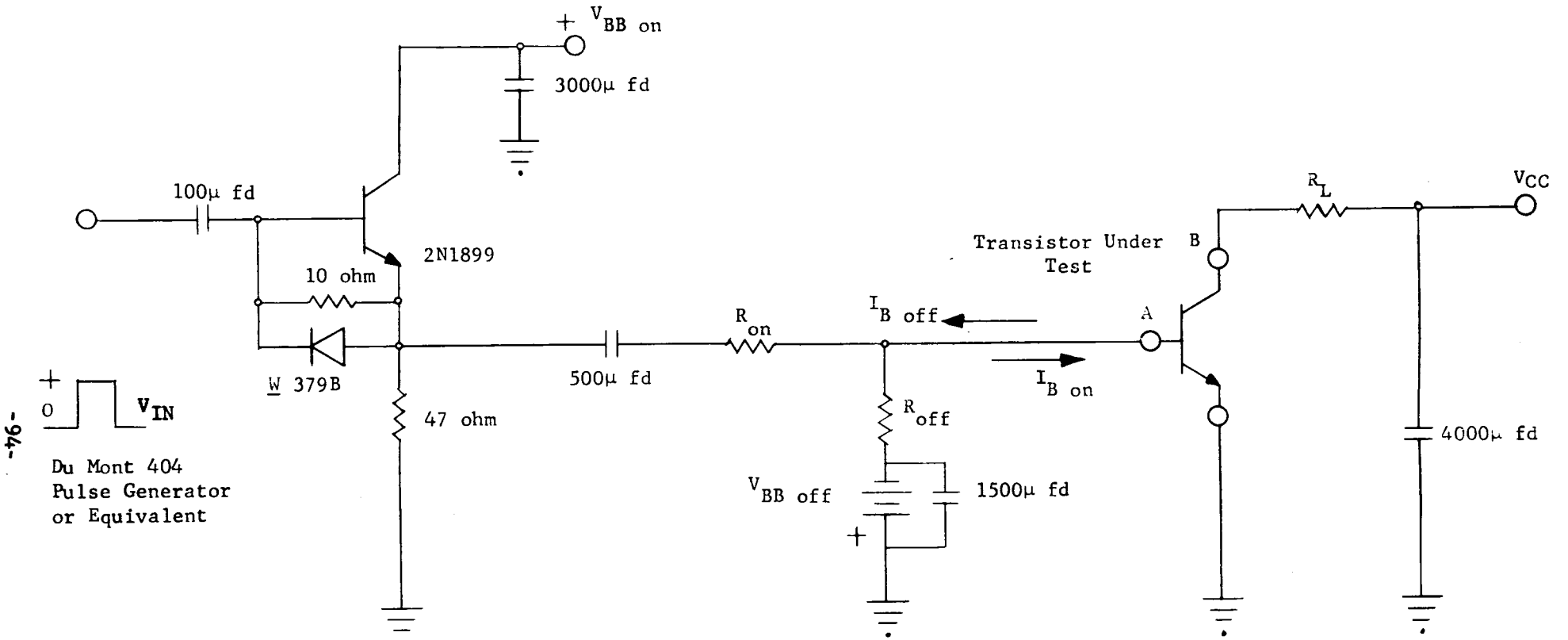


FIGURE 40: h_{FE} As a Function of Collector Current



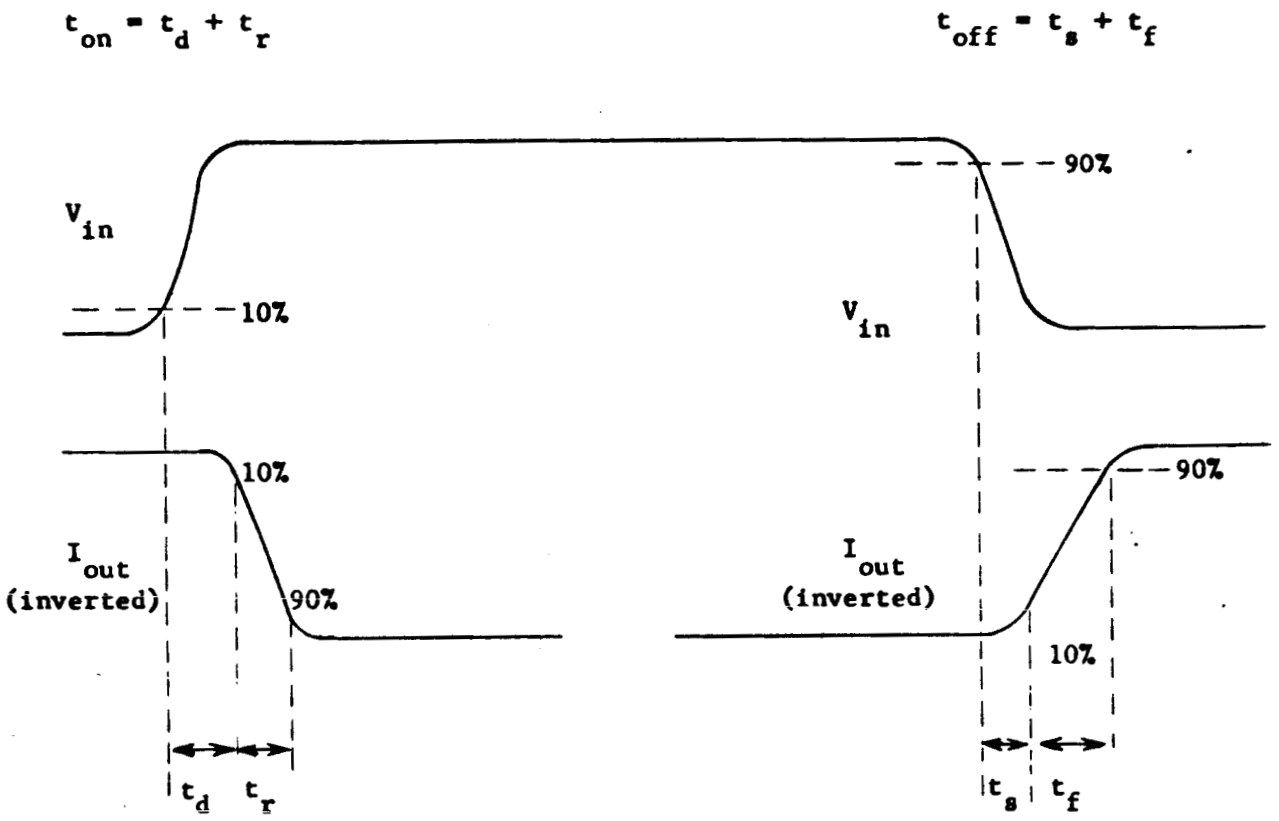
I_B(ON) and I_B(OFF) measured at Point A with Tektronix Type 131 Current Probe Amp.

I_C measured at Point B with same Probe.

FIGURE 41: Switching Test Circuit

TRANSISTOR TEST CONDITIONS

V_{CC}	=	12V	Input Pulse
R_L	=	.55 ohm	cps rep.rat = 10 cps
I_C	=	20A	μ sec pulse width=20μsec
$I_{B\ on}$	=	3A	
$I_{B\ off}$	=	3A	
R on	=	3.9 ohm	
R off	=	6.8 ohm	
V_{BB} on	=	40V	
V_{BB} off	=	15V	



Test procedure: Device is mounted on appropriate heat sink. $I_{B(on)}$ and $I_{B(off)}$ is measured each test for purpose of adjustment. (I_B in each case may vary with input impedance.) V_{CC} is applied until specific I_C is measured, then switching is measured as described above.

FIGURE 42: Test Conditions and Typical Display for Switching Test

ELECTRICAL CHARACTERISTICS OF FINAL TRANSISTORS
DELIVERED TO JPL

TABLE V

Unit No.	V_{CBO}	V_{CEO}	V_{EB}	$V_{CE(sat)}$ I_B = 5A I_C = 75A	$V_{BE(sat)}$	h_{FE} 20A	h_{FE} 40A	h_{FE} 60A	h_{FE} 75A	t_{on} at 20A μs	t_{off} μs	
84-5-1A	5/17 10/105 15/125 20/200	5/75 10/550	4/20	.19	.99	110	73.5	54.5	45.5			25°C
										2.0	18.0	
	18/100	5/100	4/7.8	.20	.90	122	68	58	42.5			100°C
75-B	5/3 10/9 15/20 20/100	5/150 10/300 15/500 17/600	4/56	.16	.93	126	97.5	75	68			25°C
										2.5	7.5	
	6/100	2/100	4/37	.20	.89	124	91.0	68	61.5			100°C
83-2	5/50 10/100 15/175 20/250	5/90 10/200 15/300 20/450	4/5	.22	.93	69	48.2	43.5	34			
	13/100	4/100	4/5	.25	.86	90	53.5	40.0	32.0			
84-10-1	5/5 10/9 15/20 20/200	5/125 10/800 12/1200	4/27	.20	.96	71.5	74.5	62	59			25°C
	20/10	7/100	33/5	.21	.88	127.0	82.0	65.5	62.5			100°C
81-10-1	5/.1 10/.3 15/1	5/30 10/180 15/1000	16/100	.27	1.12	47.5	41	35.5	30			25°C
										2.5	10.0	
	26/100	8/100	4/100	.30	1.7	43.5	38	30.5	25			100°C

VII. CONCLUSIONS AND RECOMMENDATIONS

The success of this project proved that Westinghouse leads the semiconductor industry in the precise control of equipment, materials and processing. It demonstrated the feasibility of fabricating high current and low saturation voltage devices in large area epitaxial slices and also on plain silicon crystal. This was accomplished on a small scale, engineering level; it now remains to establish the processes for the large scale production of such a device.

More specific recommendations include:

1. A program to test the device's secondary breakdown.

2. A special circuit should be designed to test switching characteristics at current levels up to 100 amperes.

APPENDIX

1. Voltage Design

The net impurity density for a Gaussian distribution for a single-diffused transistor is

$$C(x) = C_1 \, e^{-X^2/4D_1t_1} - C_B \tag{1}$$

where

C_1 = surface concentration

C_B = background concentration

D_1 = diffusion coefficient

t_1 = diffusion time

$$\frac{d^2V}{d_X{}^2} = - \frac{qC(x)}{K\epsilon_o} \tag{2}$$

where

q = electronic charge

K = dielectric constant

ϵ_o = permittivity of free space

When a voltage is applied at a junction, the depletion layer extends to both sides of the junction. The depletion layer width as a function of voltage at the collector base junction can be calculated by solving Equation 2 for given boundary conditions.

The avalanche breakdown characteristics can be calculated from the empirical formula[1]

$$1 - \frac{1}{M} = \int_o^w \alpha(E)\, dx \tag{3}$$

where

M = avalanche multiplication factor

w = depletion layer width

The ionization rate α can be written[2] as

$$\alpha (E) = a\ e^{-b/E} \qquad (4)$$

where

$a = 9 \times 10^{15}\ cm^{-1}$

$b = 1.7 \times 10^{6}$ (volt/cm)

The junction breaks down in the avalanche mode when the integral in Equation 3 becomes unity. A computer program has been written to solve the preceding equations. The program computes the voltage supported by the collector base junction as a function of depletion layer width and the avalanche breakdown voltage. Several problems were solved over a wide range of parameters.

2. Current Gain Calculations

The steady state continuity equation is

$$(q - R) - \nabla . I = 0 \qquad (1)$$

(q-R) = net rate of generation of particles
(rate of generation - rate of recombination)

I = particle current

The electron current due to diffusion and drift field in a P-type base is

$$I_N = - D_n \nabla N - \mu NE \qquad (2)$$

where

N = excess minority carrier (electron density)

E = electric field intensity

μ = mobility

It can be assumed that

$$R = \frac{N}{\gamma_n}, \quad q = 0 \tag{3}$$

where

γ_n = the lifetime of minority carriers

Substituting Equation (3) and (2) in (1) and assuming one-dimensional case, we get the steady state continuity equation for excess minority carrier in P-type base as

$$\frac{d^2N}{d_X^2} + f \frac{dN}{dx} - \frac{N}{L_n^2} = 0 \tag{4}$$

where

$$L_n^2 = \frac{1}{D_n \gamma_n}, \quad f = \frac{qE}{KT} \tag{5}$$

The general solution of Equation 4 is

$$N = e^{-fx/2} \left[A e^{\alpha x} + B e^{-\alpha x} \right] \tag{6}$$

where

$$\alpha^2 = \frac{f^2}{4} + \frac{1}{L_n^2}$$

The excess minority carrier current density is

$$J_N = -q I_N = q D_N \frac{dN}{dx} + q \mu_n NE \tag{7}$$

The coefficient in Equation 6 can be evaluated with known boundary conditions at the edge of the depletion layer of the model shown in Figure I-10 and current density can be determined from Equation 7. A similar type of equation can be derived for the minority carrier density J_p in the N-type emitter.

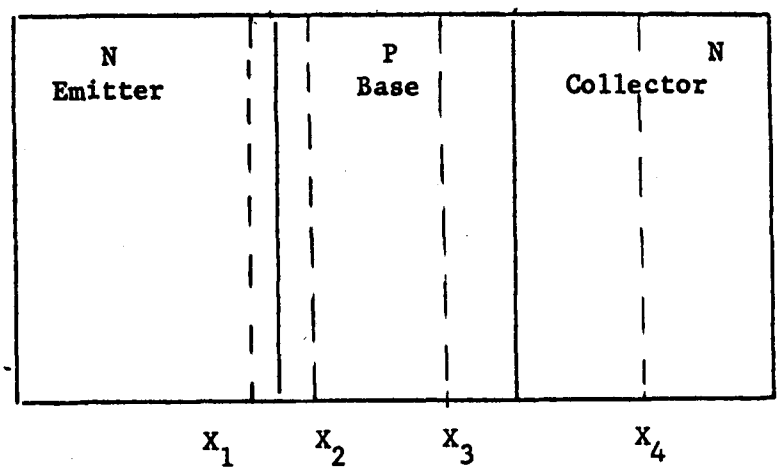


Figure I-10
Analytical Model

Thus, the injection efficiency of the emitter base junction is

$$\gamma = \frac{J_{N(X2)}}{J_N(X_2) + J_{P(X_1)}} \tag{8}$$

and the transport factor is

$$\beta = \frac{J_{N(X_3)}}{J_N(X_2)} \tag{9}$$

and the current gain is

$$\alpha = \gamma \beta \tag{10}$$

assuming a collector efficiency of unity. Thus, the current transfer ratio

$$h_{FE} = \frac{\alpha}{1 - \alpha} \tag{11}$$

The above treatment can also be extended to PNP transistor. The preceding equations were solved with the aid of a computer program, and the dependence of h_{FE} on other device parameters was established.

3. Switching Time

The equation for delay time is

$$t_d = \frac{2}{I_B} C_{Te} V_{BE}^{1/2} + C_{TC} (V_{CC} + V_{BE})^{1/2} - V_{CC}^{1/2} \quad (1)$$

where

I_B = base drive current

C_{TE} = emitter transition capacitance

C_{TC} = collector transition capacitance

V_{CC} = supply voltage

V_{BE} = emitter base voltage in 'off' condition

and the equation of rise time is

$$t_R = h_{FE} \left(\frac{1}{W_T} + 1.7 R_2 C_{TC} \right) \ln \frac{h_{FE} I_B}{h_{FE} I_B - 0.9 I_C} \quad (2)$$

where

h_{FE} = current transfer ratio

W_T = angular current-bond-width frequency

C_{TC} = collector transition capacitance

I_B = base drive

I_C = collector current

The switching characteristics can be determined by solving the above equations.

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1. Miller, S. L. "Avalanche Breakdown in Germanium," PHYSICAL REVIEW, Vol. 99, pp. 1234-1241, August 1955.

2. Masergian, J. "Determination of Avalanche Breakdown in P-N Junction," JOURNAL OF APPLIED PHYSICS, Vol. 30, pp. 1613-1614, October 1959.