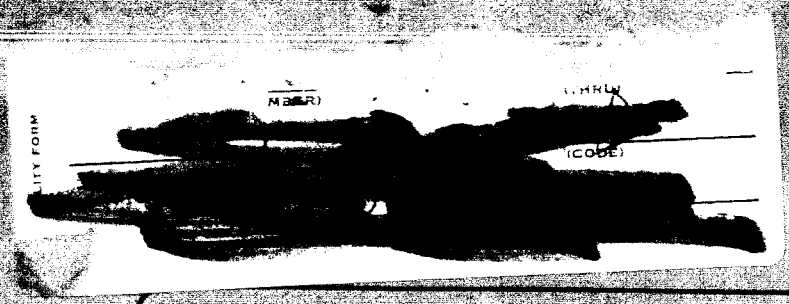

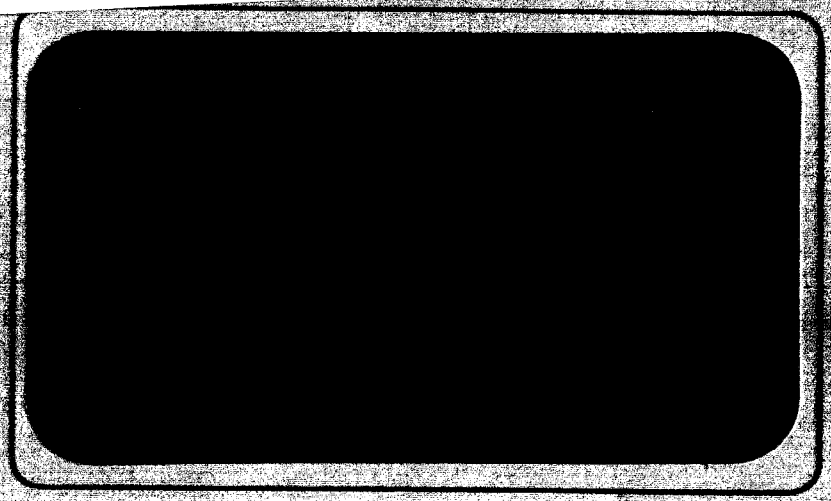

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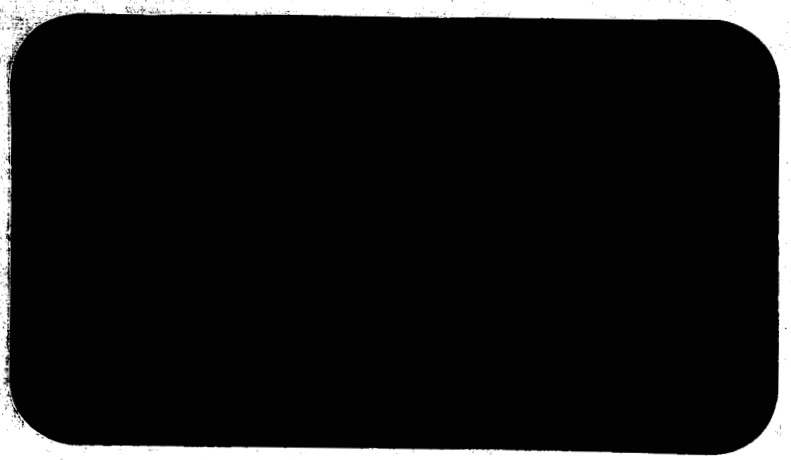

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[redacted]

Solid-State Circuit Development

Assignment 61 501
MEL R&D Phase Report 283/64
April 1965

By
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ABSTRACT

Reported here are the final design changes to a silver-cadmium battery sensing and switching circuit developed at MEL for satellite electric power systems. This circuit is designed to continuously monitor the terminal voltages of an active and a standby battery and the individual cell voltages in the active battery. When minimum voltage conditions are met, the circuit switches electrical load from the active to the standby battery. This circuit also allows solar cells, when energized, to supply load current and battery charging current.

Also described is a circuit designed to control the charge current into recently developed nickel-cadmium cells with control electrodes ("three-terminal" cells). The potential on the control electrode of a cell is the input signal to this circuit which, in turn, determines when and how the charge current is to be changed. At present this is a laboratory instrument only but will be made suitable for satellite applications in later developments.

ADMINISTRATIVE INFORMATION

The work described in this report was accomplished under NASA Contract S 12730-G as amended, (2) 4 Feb 1963, and (3) 18 Oct 1963.

REFERENCE

(a) MEL R&D Phase Report 61 501 of 17 Jan 1964

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SOLID-STATE CIRCUIT DEVELOPMENT

1.0 INTRODUCTION

This report will describe the developments in circuit design work on two developmental tasks being performed at MEL on NASA Purchase Order S-12730-G.

The previous phase report, reference (a), describes the needs for and initial development work performed on a sensing and switching circuit for silver-cadmium batteries. This report will describe further improvements and additional work performed on this circuit to date. Also included in this report is a description of the design and development work performed on a circuit for controlling charge current in recently developed nickel-cadmium cells with control electrodes ("three-terminal" cells). A separate, more detached report in the charge circuit for the three-terminal cells will be prepared at the completion of this development. In its present form this circuit constitutes a laboratory instrument only. In the future it will be temperature compensated and otherwise made suitable for specific satellite applications.

2.0 SILVER-CADMIUM BATTERY SENSING AND SWITCHING CIRCUIT

2.1 Problem Background. The silver-cadmium battery sensing and switching circuit is being developed for use in satellite power systems. Two silver-cadmium batteries, or packs of cells, supply electrical power for the satellite during periods of darkness when the solar cells are not energized. The purpose of the circuit under development is to monitor the individual cell voltages and the overall battery voltage of each battery while one supplies electrical power and the other is on standby. When predetermined minimum conditions in the battery supplying power are reached, the circuit interchanges the roles of the two batteries. It also allows each battery to be charged during periods of sunlight when the solar cells are able to supply power to the satellite.

2.2 Basic Circuitry. The sensing and switching circuit for the silver-cadmium battery, reproduced here (Figure 1) with changes, appeared in reference (a). There also was a detailed

description in that report. In Figure 1, the components shown with an asterick (*) have values and/or positions that are different from the same numbered items in Figure 3 of reference (a). The numbering of components in the figures of both reports coincides so that comparison is easy.

2.3 Circuit Changes.

2.3.1 Previously the gate biasing voltage dividers for Silicon Controlled Rectifier 2 (SCR_2), SCR_3, and SCR_5, SCR_6 had been connected in series. It was found, however, that at low temperatures, if SCR_2 (or SCR_5) was biased on, then there was a chance that the biasing divider for SCR_3 (or SCR_6) might be current starved due to leakage into the gate of SCR_2 (or SCR_5). Therefore, the dividers were separated and connected in parallel as shown in Figure 1. The dividers are now Resistor 8 (R_8), Sensistor 1 (TCR_1), R_{12}, for SCR_3; R_9, Thermistor 3 (TH_3), in parallel with ($\|$), R_{10}, R_{11} for SCR_2; R_{21}, TCR_2, R_{25} for SCR_6; R_{22}, TH_6, $\|$ R_{23}, R_{24} for SCR_5. The form of temperature compensation in the gate-biasing dividers for SCR_3 and SCR_6 were modified by the use of sensistors (TCR) instead of thermistors (TH). By incorporating these changes, the total circuit loss is increased by only 1.5 milliwatts (mw) (0.5-ma* drain in the new gate dividers).

2.3.2 The lower cell-voltage limit requirement for battery switching has been changed by NASA since the last phase report. The previous requirement of 0.9 volt was lowered to 0.8 volt. Therefore, the cell detector diodes (D_1, D_2 and D_5, D_6) were changed. Now D_1 and D_5 are 1N457's, and D_2 and D_6 are 1N191's. This change was in accordance with the adjustments section of Appendix B of reference (a).

The temperature compensating networks (R_3, R_4, $\|$ TH_1, R_5 and R_{16}, R_{17}, $\|$ TH_4, R_{18} of Figure 3, reference (a)) at the output of the cell detectors have been eliminated in favor of a single compensating network at the output of the drive flip-flop.

*Abbreviations used in this text are from the GPO Style Manual, 1959, unless otherwise noted.

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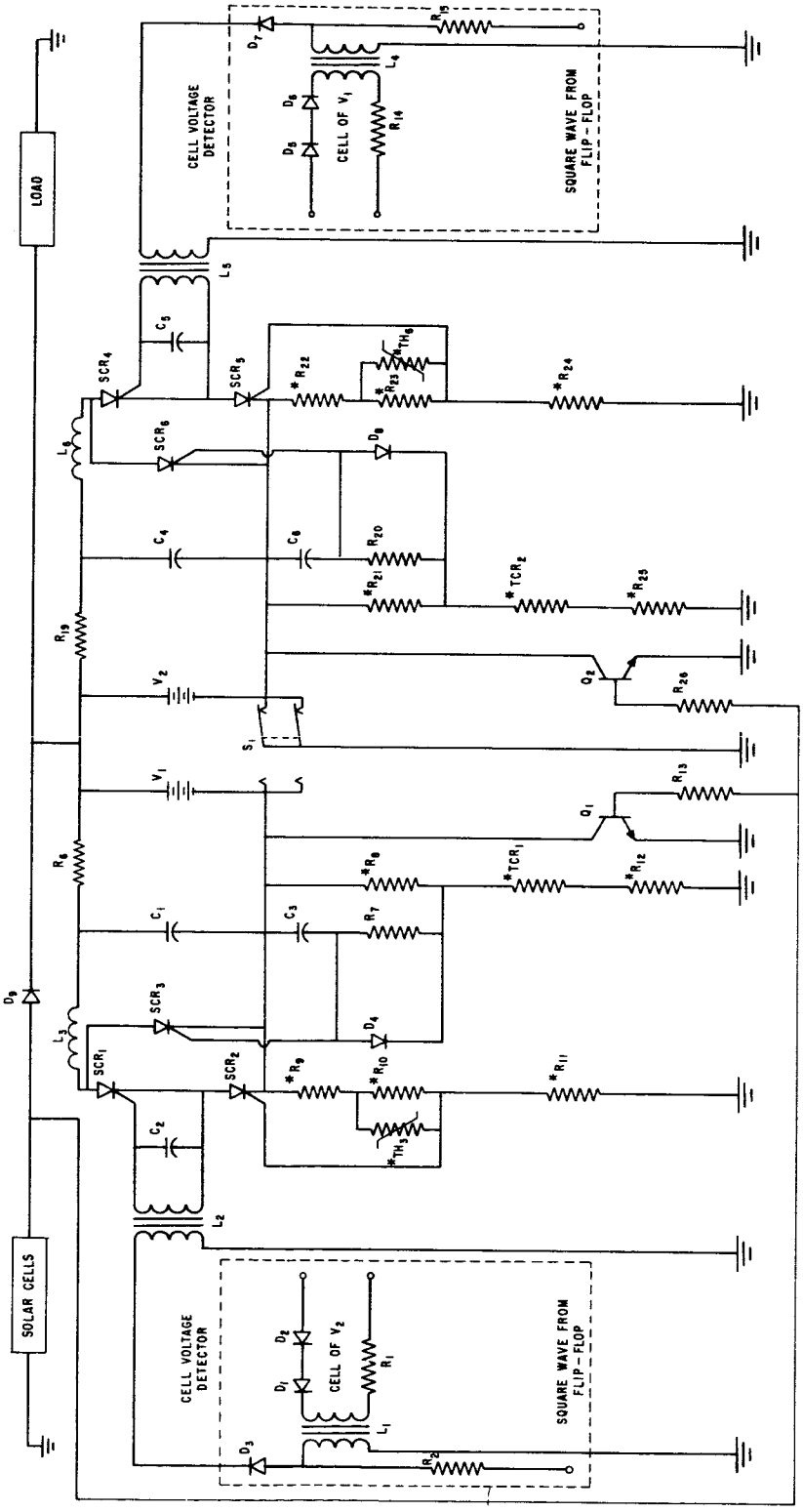

Figure 1
Silver Cadmium Battery Switching Circuit

Parts List
For Silver-Cadmium Battery
Switching Circuit

R_1 , R_{14} - 470 Ω
R_2 , R_{15} - 10K
R_6 , R_{19} - 100K
R_7 , R_{20} - 10K
R_8 , R_{21} - 1.7K
R_9 , R_{22} - 1.8K
R_{10}, R_{23} - 2.8K
R_{11}, R_{24} - 3K
R_{12}, R_{25} - 1.4K
R_{13}, R_{26} - 40K
R_{27} - 316K
R_{28} - 100Ω
R_{29} - 500Ω Potentiometer
R_{30} - 301Ω

All Resistors 1% ¼ watt

C_1, C_4 - 50 μf
C_2, C_5 - .03 μf
C_3, C_6 - 200 μf
C_7 - 82 μf

L_1, L_4 - Core, Sprague D452-2U-F1, 600 turns each winding
L_2, L_5 - Transformer - United Transformer Corp. Di-T 36
L_3, L_6 - Relay coils
S_1 - Relay contacts Potter & Brumfield SL11DB 12 volt

TH_3, TH_6 - Thermistor 1K 4.8% T.C.
TCR_1, TCR_2 Sensistor 6.8K; TH_7 - Thermistor 3K 4.8% T.C.

D_1, D_5 - IN457
D_2, D_6 - IN191
D_3, D_7 - IN457
D_4, D_8 - IN92
D_9 - IN1117

SCR_1, SCR_2 - 2N2324
SCR_3, SCR_4 - 2N2324
SCR_5, SCR_6 - 2N2324

Q_1, Q_2 - 2N657
Q_3, 2N2905; Q_4 - C624 (FET) Crystalonics

V_1, V_2 - 13 cell silver cadmium battery

Figure 1 (Cont)

2.4 Final Drive Flip-Flop Circuit. A final drive flip-flop has been selected for this circuit as shown in Figure 2. This flip-flop has an output pulse of 4.4 volts, 78 msec wide approximately every 55 seconds. The pulse frequency output can be varied by changing R_{27}. Lowering R_{27} will increase the frequency of pulse occurrence. Increasing R_{28} will increase the pulse width, and increasing the divider on R_{29} will increase the pulse amplitude. The combination $R_{30} \| TH_7$, R_{29} temperature compensates the flip-flop output over the operating range of -10 to +60 C. The loss in this flip-flop is approximately 12 mw for 78 msec out of each minute.

2.5 Summary and Conclusions. In its present condition, the silver-cadmium battery sensing and switching circuit is complete. Performance characteristics will be confirmed by a complete series of temperature tests on this circuit as a whole before the project will be considered concluded.

3.0 CIRCUIT FOR CONTROLLING CHARGE CURRENT

The development of a circuit for controlling charge current in three-terminal nickel-cadmium cells is a task which was initiated after the last phase report was issued. These three-terminal cells are a recent development whose characteristics are similar to those of other nickel-cadmium cells, but in addition have a separate terminal whose potential (with respect to the negative cell terminal) is a function of the charged state of the cell. The circuit is designed to monitor the third terminal potential of each cell in a group of five while they are being charged. As the potential rises for any one of the cells in the group, the circuit begins reducing the charge current to the series group of cells so that when the third terminal potential of any cell reaches a predetermined maximum, the charge current will have been reduced to a preset trickle charge.

In its present form this circuit is to be used as a laboratory instrument. With additional detectors, it will accommodate virtually any number of cells. In further developments this circuit will be temperature compensated and otherwise made ready for satellite applications.

A detailed description of the operation of this control circuit is included in Appendix A of this report.

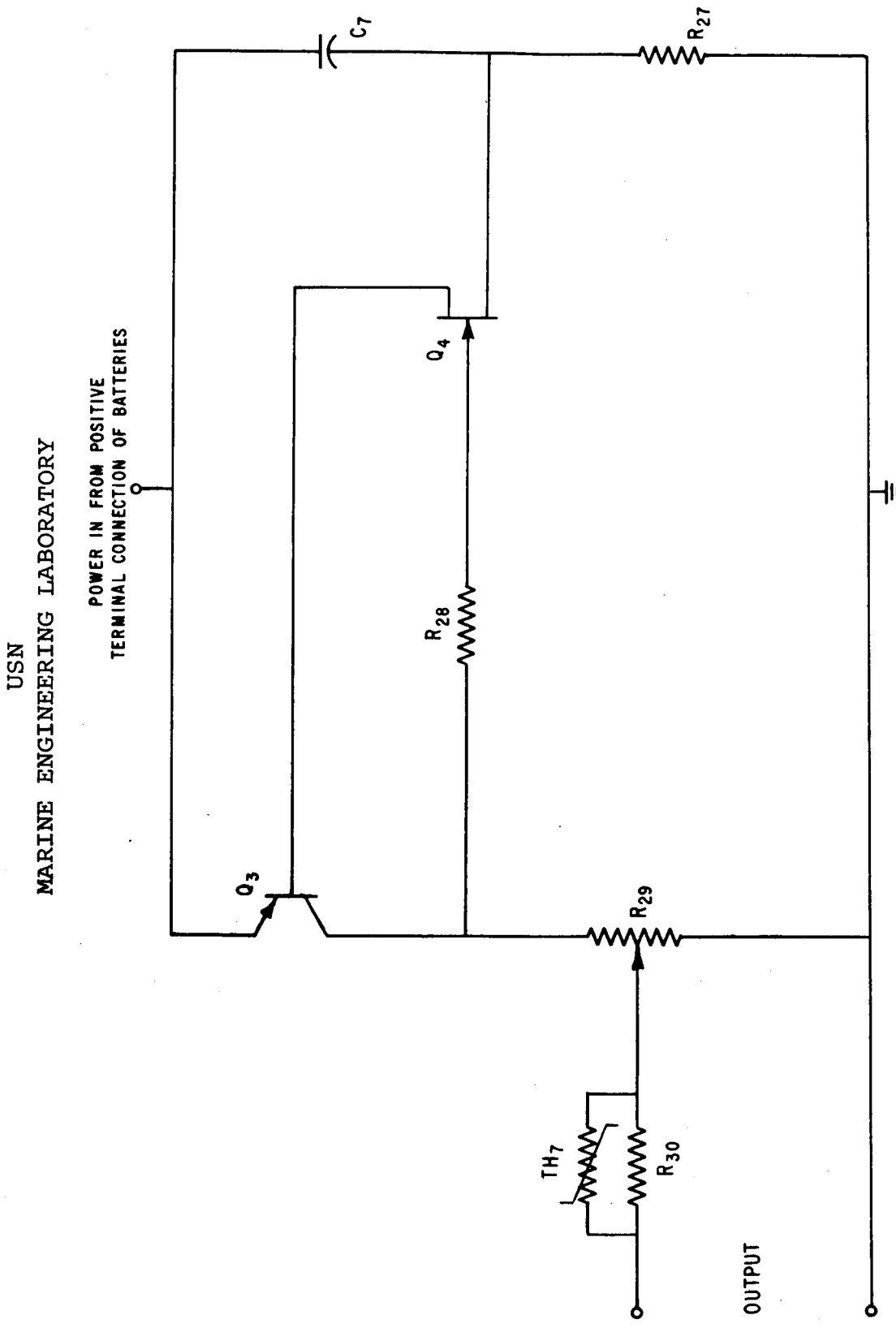

Figure 2
Drive Flip-Flop for Silver Cadmium Battery Switching Circuit

The entire charge current control circuit is shown in Figure 1-A. This circuit was specifically designed to be used with three-terminal, nickel-cadmium cells manufactured by two different companies. The characteristics of the third terminal potential of the cells from these two manufacturers are not the same. For circuit-design purposes the chief difference is that the third-terminal potential of the cells from Company B does not increase at the same rate as that of the cells from Company A. This means that the circuit controlling the charge current must have two modes of operation, one each for the cells of each manufacturer. A selector switch is provided for choosing the mode of operation desired.

3.1 Theory of Operation. The circuit consists of five sections: a power supply, a square wave driver, a detector section containing a detector for each cell, a current control, and a time delay section. The power supply converts 115 volts, 60-cycle ac to 10 volts dc ± 1 percent regulated for input and load variations. This is the bias supply for the remaining sections. The square wave driver provides a 500 cps, 4-volt (positive only) square wave for the detector. Each detector samples the third-terminal potential for its cell 500 times a second and translates this information to a d-c level. Each detector has an input impedance greater than 500 ohms and yields complete isolation between cells and between its cell and the following circuitry. The current-control section uses the d-c level from the detectors to decrease the battery charging current from full charge to a trickle charge as a cell's third-terminal potential increases. The charge current being controlled is derived from an external supply. The time delay section, when used, causes the initial decrease in charging current to be delayed by 5 minutes after a cell's third-terminal potential reaches the level which would normally cause the charge current to begin decreasing. The highest third-terminal potential of each group of cells governs the charging rate of the group.

3.2 The A Mode. When used in conjunction with the cells from Company A (selector switch in Position A), the circuit admits a full charging current into the five cells when they are in a discharged state. As any one cell nears its fully charged condition, its third-terminal potential begins to increase from zero. When this potential reaches approximately 125 millivolts (mv), the charge control section of the circuit begins to decrease the charging current into the cells. As

any cell's third-terminal potential increases above 125 mv, the charging current decreases linearly, until the current is reduced to a trickle charge when the third-terminal potential of any cell has reached 250 mv. If the third-terminal potentials continue to increase, the circuit will remain in this trickle charge condition until the cells are manually disconnected. If all third-terminal potentials fall below 250 mv, the charge current will increase linearly and again be controlled by the highest third-terminal potential.

3.3 The B Mode. With the selector switch in the B position, the circuit will allow a full charge current into the five discharged cells. However, in this mode when the third-terminal potential of any cell increases to 125 mv, a 5-minute time delay is initiated. For the next 5 minutes, a full charge current will continue into the cells regardless of the condition of their third-terminal potentials. At the end of 5 minutes, control of the charging current will be returned to the cell with the highest third-terminal potential. If this potential is still 125 mv, the full charge current will continue; if it is between 125 and 250 mv, the charging current will decrease to a value proportional to it; if it is above 250 mv, the charging current will immediately reduce to its trickle charge level. That is, at the end of the 5-minute time delay, the operation of the circuit in the B mode is identical to the A mode, with respect to the third-terminal potentials. In either mode of operation, the respective cells, after the charge current has been reduced to trickle charge level, should have been charged to approximately 110 percent of their capacity.

4.0 SUMMARY OF REPORT

4.1 As stated previously, the silver-cadmium battery sensing and switching circuit development project will be considered concluded after final temperature tests have been completed.

4.2 The charge current control circuit for the three-terminal nickel-cadmium cells project has been completed for the laboratory instrument phase, and two prototypes have been delivered to NASA, Goddard Space Flight Center, Code 636.2. Several of these instruments have been produced by a manufacturing firm at NASA's request and are now being used in their three-terminal battery testing program at NAD,

Crane, Indiana. In later developments this curcuit will be temperature compensated and otherwise made suitable for satellite applications.

Appendix A

Circuit Description of Charge Current Control Circuit

This appendix refers to Figure 1-A and describes the stage by stage operation and adjustments in the main portions of the charge-current control circuit for three-terminal nickel-cadmium cells.

The power supply is a standard bridge rectifier, filter, and series voltage regulator. It consists of Q_{10} and Q_{11}, D_9 through D_{15}, R_{23} through R_{29}, C_8, L_1 and T_3. It converts 115 volts, ±10 percent 60-cycle ac to 10 volts dc ±1 percent regulated for a load variation of 100 percent.

The drive flip-flop is a standard type. It consists of Q_5 and Q_6, D_7, R_{10} through R_{13}, C_3, and C_4. It provides a 500-cycle, 4-volt positive square wave to the detectors as a sampling signal.

Each detector consists of Q_4, D_4 through D_6, R_6, R_8, C_2, and T_1. Resistor R_9 is a 47-ohm leakage resistor from the third terminal to the negative terminal of each cell as specified by NASA. These detectors have a d-c input resistance greater than 500 ohms, and because of the transformers, T_1, leave the third terminals (control electrodes) of the cells completely isolated from each other. The OR circuit formed at the output mode of the detectors effectively isolates the detector outputs from each other. If a cell is in a discharged condition, its third-terminal potential is virtually zero; thus, no dc flows through D_6, R_8, and the dc side of T_1. For the square wave sampling signal in the a-c side of T_1, this path appears as a high impedance. Therefore, the energy of the square wave is stored in C_2, since the path through D_5 and C_2 is a lower impedance. This allows C_2 to maintain a d-c voltage level sufficient to bias Q_4 on in a near saturation state. As the nickel-cadmium cell charges up, its third-terminal potential increases, thus allowing a low dc to flow through D_6, R_8, and the d-c side of T_1. As this current increases (with an increasing third terminal potential), the dynamic impedance of Diode D_6 decreases, thus lowering its reflected impedance as seen by the square wave. As this impedance decreases, more energy is dissipated through T_1 and less is stored in C_2. This will lower the d-c voltage maintained by C_2 and will cause Q_4 to travel through its active region toward cutoff. When Q_4 is near saturation, its collector voltage is held at less than 1 volt, but as it moves through the active region toward cutoff, its collector voltage increases from less than 1 volt toward a maximum of

10 volts (the bias supply). With Diodes D_4 of the five detectors connected at their cathodes, they act as an OR circuit, meaning that the highest anode voltage is the voltage which appears at the cathode connection of the diodes. Therefore, this is the d-c output level of the detector stage.

The current control stage simply inverts a changing d-c voltage level and converts this to a changing d-c output from an external current supply. This section consists of Q_1 through Q_3, Q_{12}, D_1 through D_3, R_1 through R_5, C_1, SCR_1, S_1, and S_2. With Selector Switch S_1 in the A position, the time delay section is deactivated. A rising detector output voltage (caused by a third-terminal potential rising above 125 mv) will bias the darlington pair Q_{12}, Q_3 on from cutoff toward saturation, thus lowering the collector voltage of Q_{12}, Q_3. As the collector voltage of the darlington pair decreases, the base current of Q_2 is decreased, thus reducing its collector current. A decreasing collector current in Q_2 is the same as a decreasing base current in Q_1. If the base current of Q_1 is reduced, its collector current is reduced proportionately, thus decreasing the charging current from the external supply into the five nickel-cadmium cells. This will be reduced to trickle charge level when any third-terminal potential reaches 250 mv.

The time delay section is simply a unijunction-transistor timing circuit adjusted to yield an output pulse 5 minutes after being activated. It consists of Q_7 through Q_9, D_8, R_{14} through R_{21}, R_{30}, C_5 through C_7, C_9, T_2, SCR_2, and SCR_3. With Selector Switch S_1 in the B position, the 10-volt supply is connected to the time-delay circuit, but it is not activated until SCR_2 has been gated "on." Also with S_1 in this position, the emitter of Q_3 will not be connected to ground until SCR_1 has been gated "on." When any third-terminal potential reaches 125 mv, the detector output voltage is at a level sufficient to gate on SCR_2, through the field effect transistor Q_9, thus activating the time delay circuit. So far in this B mode, Q_3 has been unable to control the remaining portion of the current control section, since its emitter is floating. Therefore, the standing bias condition on Q_2 maintains the charging current at full charge. Five minutes after the activation of the time delay circuit, its output pulse through T_2 will gate on SCR_1, thus allowing the detector output, through Q_{12}, Q_3, to control the value of charging

current into the five cells. The same pulse which gated on SCR_1 also gated on SCR_3, enabling the energy stored in C_9 to turn off SCR_2 and deactivate the time delay circuit. Now the value of the charging current will depend on the detector output and its control will be the same as that described above for the A mode.

There are a number of adjustments possible in both the detector and the current control sections. The value of the third-terminal potential at which the charging current begins to decrease (or at which the time-delay circuit is activated in the case of B mode) can be varied by adjusting R_7. Increasing R_7 will allow the third-terminal potential to rise to a value greater than 125 mv before the charging current begins to decrease. Decreasing R_7 will have just the opposite effect. As this adjustment is made, the value of the third-terminal potential at which the charging current reaches trickle charge level is varied also, with the difference between the two potentials remaining essentially the same. Variable Resistor R_5 is included as a calibration adjustment. It is generally set when the circuit is first used to account for any difference in the gain of Q_3 from its design value. It is set in conjunction with the initial R_7 adjustments and afterwards only if Q_3 is ever replaced. Its value will be in the neighborhood of 50 kilohms. The trickle charge value can be varied from less than 1 to greater than 2 amperes by adjusting R_1. By increasing R_1, the value of the trickle charge will be decreased and vice versa. Adjustments to R_1 are made only when S_2 is depressed. Switch S_2 is a normally closed pushbutton switch. Depressing S_2 allows the trickle-charge current to be adjusted without any effects from the rest of the control circuitry. The value of the full charging current can be varied from 5 to 15 amperes by adjusting R_2. Increasing R_2 will decrease the full charge current value, while decreasing R_2 will increase the full charge current value. When the full charge current is adjusted with R_2, the current limit on the external current supply should also be set for this value. When R_2 is being adjusted, it is preferable to keep Q_1 in saturation. If R_2 is adjusted for the desired full-charge current, and as a result the collector to emitter voltage of Q_1 becomes greater than 0.4 to 0.6 volt, then the output voltage of the external current supply should be reduced to return to this condition. This is done in order to minimize the

power dissipated by Q_1. The maximum power consumed by the full control circuit from the 10-volt bias source is 250 mw (at a setting of 2-ampere trickle charge with a corresponding full charge level of 15 amperes).

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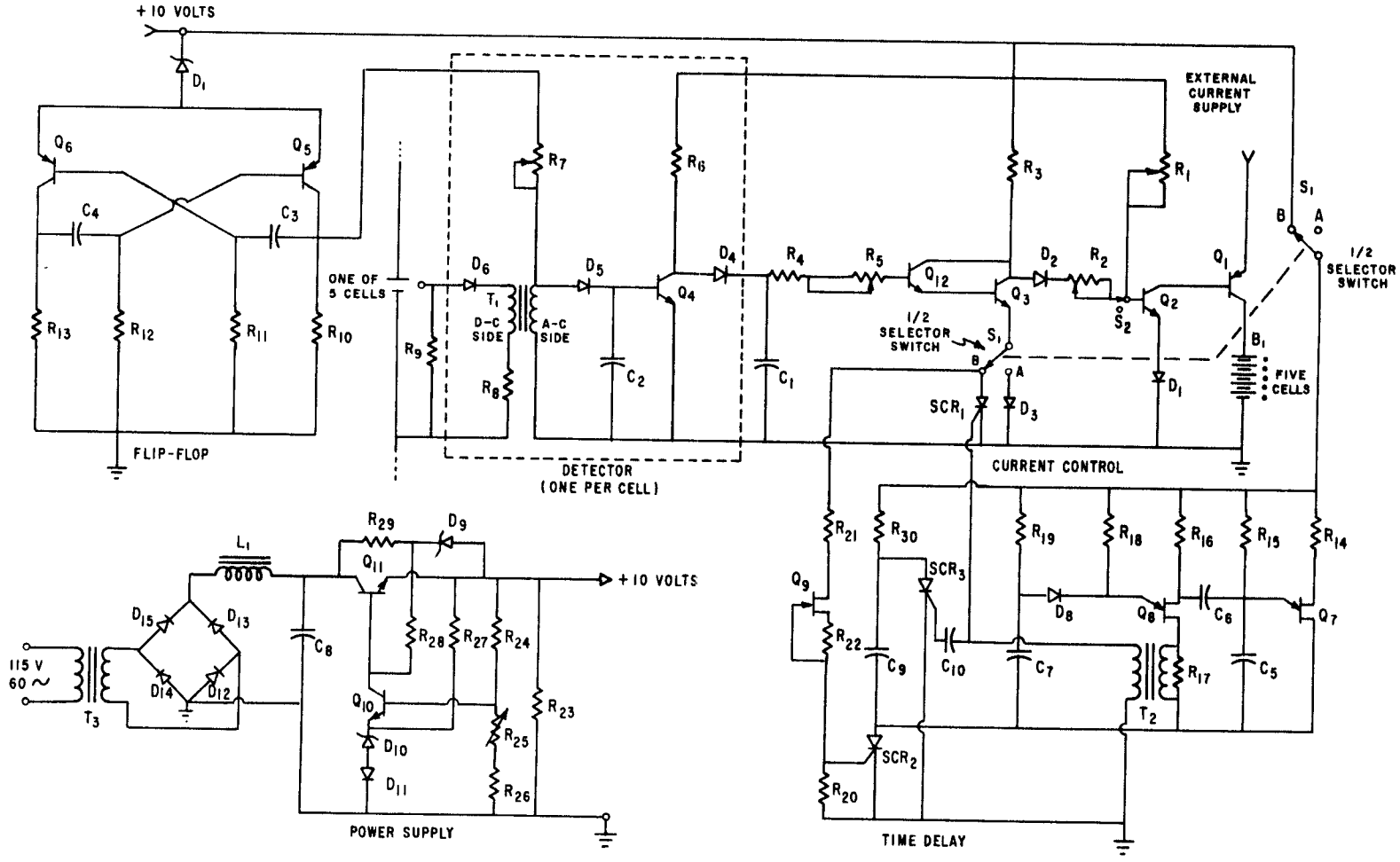

Figure 1-A
Charge Current Control Circuit

MEL Report 283/64

Parts List For Charge Current Control Circuit

R_1 - 100K Potentiometer
R_2 - 5K Potentiometer
R_3 - 549Ω
R_4 - 1.7 Meg
R_5 - 2 or 5 Meg Potentiometer
R_6 - 10K
R_7 - 20K Potentiometer
R_8 - 470Ω
R_9 - 47Ω Specified By NASA
R_{10} - 10K
R_{11} - 47K
R_{12} - 47K
R_{13} - 10K
R_{14} - 51Ω
R_{15} - 100K
All Resistors ¼ watt

C_1 - 1 µf
C_2 - 10 µf
C_3 - 0.033 µf
C_4 - 0.033 µf
C_5 - 0.033 µf
C_6 - 0.1 µf
C_7 - 10 µf
C_8 - 7000 µf - Sprague Electric 36D1070T
C_9 - 10 µf
C_{10} - 0.005 µf
All Capacitors 10 WVDC or More

D_1 - IN4005
D_2 - JAN IN457
D_3 - IN4005
D_4 - JAN IN457
D_5 - JAN IN457
D_6 - IN191
D_7 - IN752A (ZENER)
D_8 - JAN IN457 (ZENER)
D_9 - IN752A (ZENER)
D_{10} - IN752A (ZENER)
D_{11} - IN457
D_{12} - IN4005
D_{13} - IN4005
D_{14} - IN4005
D_{15} - IN4005

S_1 - DPDT Switch
S_2 - Spring-loaded push-button switch - normally closed

R_{16} - 51 Ω
R_{17} - 100 Ω
R_{18} - 5 Meg
R_{19} - 30 Meg
R_{20} - 4.7K
R_{21} - 19.6K
R_{22} - 1K
R_{23} - 220Ω
R_{24} - 620Ω
R_{25} - 1K Potentiometer
R_{26} - 1K
R_{27} - 2K
R_{28} - 3.9K
R_{29} - 510Ω
R_{30} - 100K

L_1 - 2h Choke
Chicago Standard C-23

T_1 - 1:1 Transformer (Toro
Sprague Electric R11

T_2 - Interstage Transform
U.T.C. Dot-36

T_3 - Filament Transformer
Knight 6-K-48 HF

Q_1 - 2N2152 (Wakefield Hea
Sink NC 421 F

Q_2 - 2N1720 (Wakefield Hea
Sink NC 302 M

Q_3 - 2N1613
Q_4 - 2N338
Q_5 - 2N1303
Q_6 - 2N1303
Q_7 - 2N491 (UJT)
Q_8 - 2N494C (UJT)
Q_9 - FE-202 Amelco Semiconduc
Q_{10} - 2N335
Q_{11} - 2N1613(Wakefield Heat Sink NF 213)
Q_{12} - 2N338

SCR_1 - 2N1871 or 2N2324
SCR_2 - 2N2324
SCR_3 - 2N2324

Figure 1-A (cont)