NASA TECHNICAL NOTE

NASA TN D-3477

POWER SWITCHING IN DIGITAL SYSTEMS

by Rodger A. Cliff

Goddard Space Flight Center
Greenbelt, Md.

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION • WASHINGTON, D. C. • JULY 1966

POWER SWITCHING IN DIGITAL SYSTEMS

By Rodger A. Cliff

Goddard Space Flight Center
Greenbelt, Md.

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

For sale by the Clearinghouse for Federal Scientific and Technical Information
Springfield, Virginia 22151 – Price $1.00

ABSTRACT

In many applications, particularly spacecraft, it is important to minimize power consumption. Turning off the power to parts of a digital system when they are not in use reduces overall power drain. Also, data transfer between sections of a digital system can be accomplished without gates by appropriate switching of power supply voltages. This reduces power drain and complexity by eliminating the need for many gate functions. With power switching, integrated circuits can be used in applications which would otherwise require discrete component circuits because of power constraints. The optical aspect computer of the Anchored Interplanetary Monitoring Platform spacecraft is an example of the saving that power switching can produce; power drain is reduced from 1.3 watts to 0.3 watts. This computer would have been impractical without the use of power switching.

CONTENTS

POWER SWITCHING IN DIGITAL SYSTEMS

by
Rodger A. Cliff
Goddard Space Flight Center

INTRODUCTION

It is important that digital systems in spacecraft, and many other applications, for that matter, dissipate as little power as possible. The power system of a spacecraft consists of batteries and solar cells, both of which are heavy. Unfortunately, the cost of the rocket to launch a spacecraft increases steeply with increasing payload weight. Therefore it is imperative to conserve power wherever possible. One very useful method of reducing power consumption is to turn off the various parts of a digital system when they are not in use. This method is particularly useful for systems with integrated circuits, since most integrated circuits consume more power than their discrete component counterparts. For instance, compare a typical integrated circuit flip-flop which consumes 3 mw with a discrete component flip-flop which consumes 500 μw. Power switching permits using integrated circuits, with their size and weight advantages, in applications which would previously have been restricted to discrete components by power dissipation constraints.

THE AIMP OPTICAL ASPECT COMPUTER

The Anchored Interplanetary Monitoring Platform (AIMP) spacecraft is a small payload of about 200 lbs. which is scheduled to be put into orbit about the moon during 1966. This spacecraft will investigate the interplanetary magnetic field, solar plasma flux, interplanetary dust distributions, solar and galactic cosmic rays, and the magnetohydrodynamic wake of the earth in the vicinity of the moon.*

This spacecraft is spin-stabilized by rotation about its axis of largest moment of inertia. Spacecraft orientation and position at any instant are determined by an optical aspect system. This system makes optical measurements on the earth, the moon, and the sun. Data from these measurements are collected and stored in a subsystem called the optical aspect computer.

Because the spacecraft is small, the weight, size, and particularly the power consumption of all subsystems are severely limited. Only 4.3 watts of average power is allowed for the five

*Madden, J. J., "AIMP Summary Description," GSFC Document X-672-65-313, August, 1965.

scientific experiments. All of the instruments together, including the optical aspect system, are allowed 1.3 watts average. The optical aspect system itself is allotted 950 mw average. Since the optical aspect computer is only one-third of the optical aspect system, its power consumption must be in the neighborhood of 300-400 mw.

In order to meet the power consumption requirements, the optical aspect computer uses power switching techniques to great advantage. This subsystem contains a 120-bit shift-register buffer memory and 105 bits of data accumulators. There are two modes of operation. In Mode I, data are collected in the accumulators and then transferred in parallel to the buffer memory. The buffer memory stores this information until it is time to shift the data out into the telemetry system. In Mode II, serial data are read into the buffer memory, stored, and then shifted out into the telemetry system. Figure 1 shows these two modes of operation.

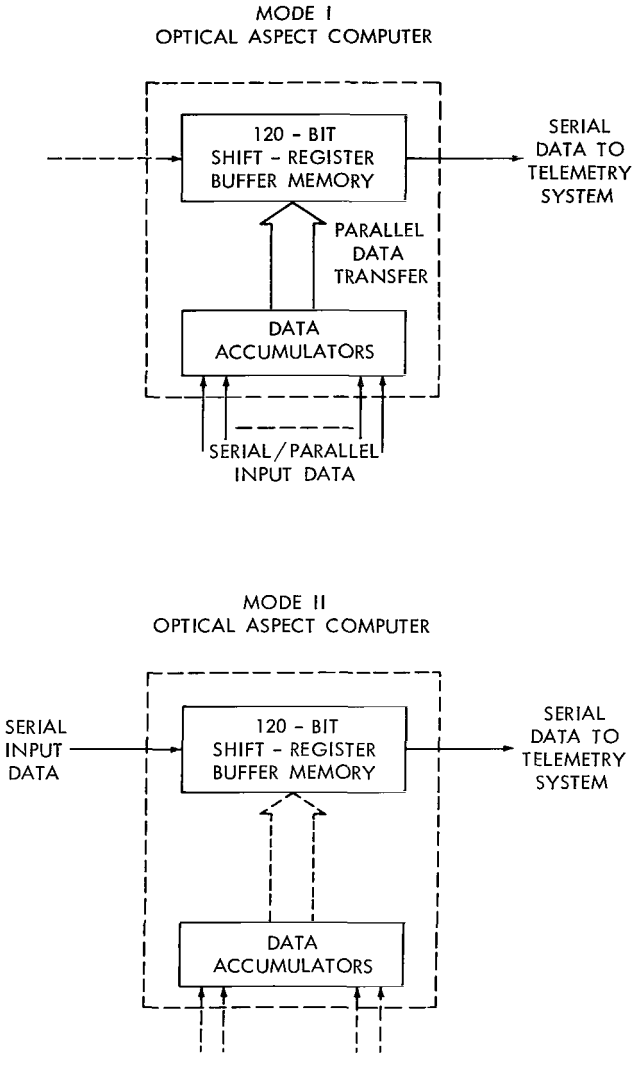

Figure 1—AIMP Optical Aspect Computer.

Power Savings In the AIMP Optical Aspect Computer

The power savings which can be obtained by using power switching are outlined in Table 1. In either Mode I or Mode II, there is a constant dissipation of about 100 mw. This power is consumed by amplifiers for synchronization signals which come from the telemetry system. No savings can be realized here because these circuits must always be energized.

The buffer memory, however, has a duty cycle ratio of 1/8 in Mode I and a duty cycle ratio of 3/8 in Mode II. When it is energized, it consumes 600 mw. This means a saving of 525 mw can be obtained in Mode I, and a saving of 375 mw can be obtained in Mode II if the buffer is de-energized when not in use. Turning off the power to the data accumulators, which consume 320 mw, produces a similar saving. In Mode I, the duty cycle ratio of the accumulators is 1/4; hence, 240 mw can be saved by using power switching. In Mode II, the accumulators are not used at all; therefore, 320 mw can be saved.

Table 1

Power Savings Resulting from Power Switching in AIMP Optical Aspect Computer.

Load Category	Power Drain Without Power Switching	Duty Cycle Ratio	Power Drain with Power Switching	Power Savings
Mode I				
Always on	100 mw	1	100 mw	0
Buffer Memory	600 mw	1/8	75 mw	525 mw
Accumulators	320 mw	1/4	80 mw	240 mw
Data Transfer Gates	320 mw	0	0	320 mw
Total	1340 mw		255 mw	1085 mw
Mode II				
Always on	100 mw	1	100 mw	0
Buffer Memory	600 mw	3/8	225 mw	375 mw
Accumulators	320 mw	0	0	320 mw
Data Transfer Gates	320 mw	0	0	320 mw
Total	1340 mw		325 mw	1015 mw

Hardware Savings In the AIMP Optical Aspect Computer

The Data Transfer Gates entry for both modes in Table 1 represents a double saving which results from using power switching. Because the parallel data transfer between the data accumulators and the buffer memory is controlled by switching the power, no data transfer gates are required. (For an explanation of how this works, refer to the paragraph Data Transfer By Power Switching.) This not only saves 320 mw, which would be dissipated in the gates, but also saves 105 gates—a significant decrease in complexity.

The AIMP optical aspect computer would have been impractical without the use of power switching. Not only would it have consumed too much power, it would not have met size and weight requirements. The use of power switching reduced the average power drain of the computer from 1.3 watts to about 300 mw—a saving of more than 4 to 1. It also eliminated 105 gates, thus making it possible to construct the computer in a single package. This reduced weight and volume and also increased reliability by eliminating a large number of inter-package connections. Furthermore, the power saving was great enough to permit building the computer with monolithic integrated circuits in order to reduce the weight and size still further.

POWER SWITCHING CIRCUITRY

Series Power Switch

Some sort of power switch circuit is necessary if parts of a system are to be turned on and off. Figure 2 shows a series power switch. When the control voltage is at ground, Q_2 is cut off,

and therefore so is Q_1. The switched power is off, and no power is dissipated in the switch or in the part of the system fed from the switched power. On the other hand, when the control voltage is positive, Q_2 turns on and saturates Q_1, thereby turning on the switched power. If the switched power has a low duty cycle ratio, then considerable power may be saved by using these switches.

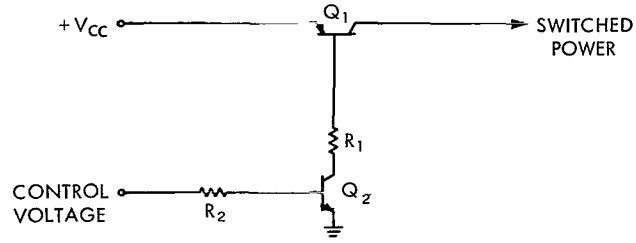

Figure 2—Series power switch.

Risetime Control

Several improvements need to be made to the simple series switch before it is applied to power switching in a complex digital system. First, a capacitor, C_R, can be added as shown in Figure 3 to control the risetime and fall time of the switched power. Figure 4 shows the control and power waveforms before the capacitor has been added, and Figure 5 shows the same waveforms after the capacitor has been added. The settling time of the circuits being turned on and off by the power switch can be minimized by an appropriate choice of the rise and fall times of the switched power.

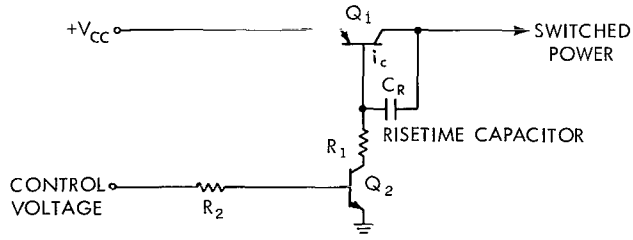

Figure 3—Series power switch with risetime control.

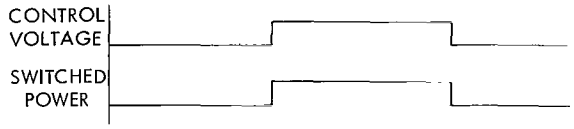

Figure 4—Series switch waveforms.

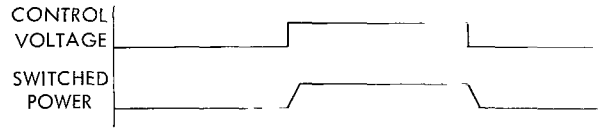

Figure 5—Controlled risetime.

Reset Output

A second improvement is made by providing a reset output so that every time the switched power is turned on, a reset pulse is available to set the digital circuitry to the proper initial conditions. The circuit is shown in Figure 6. Notice that the reset output is obtained with the addition of only one transistor and one diode, which operate as follows. During the time that the switched power is turning on, current flows from the collector of Q_1 through the emitter and base of Q_3 and discharges C_R. As long as the voltage at the collector of Q_1 (the switched power) continues to rise, the current through the base of Q_3 continues to flow into C_R, and

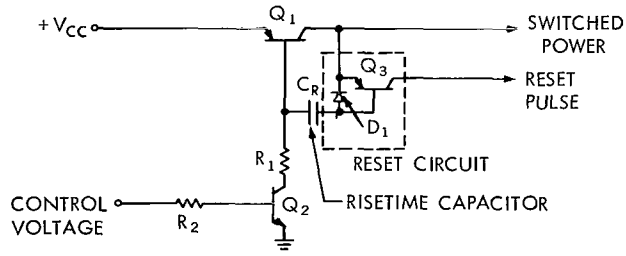

Figure 6—Series power switch with risetime and reset output.

Q_3 is turned on. Therefore, the reset output follows the rise of the switched power output. When the switched power reaches its maximum value, C_R is fully discharged, the base current of Q_3 ceases, Q_3 turns off, and the reset output returns to ground. Figure 7 shows the waveforms. The diode D_1 is provided to recharge C_R when the switched power is turned off again.

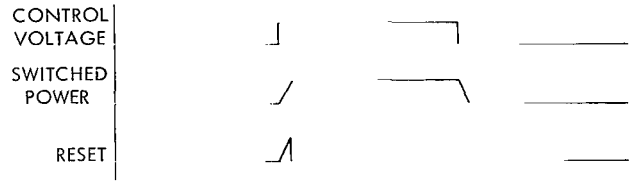

Figure 7—Reset added.

Turn-Off Delay

The usefulness of the series power switch can be increased by adding circuitry to delay the turn-off of the switched power. If information is to be transferred between two parts of a digital system, the power must at some time be on in both parts simultaneously. It is often convenient, however, to have the same event which turns off the power to one section of a system also be the event which turns on the power to the next section. Turn-off delay in the power switches relaxes the restriction that control signals must overlap. This can greatly simplify the logic which generates the control signals.

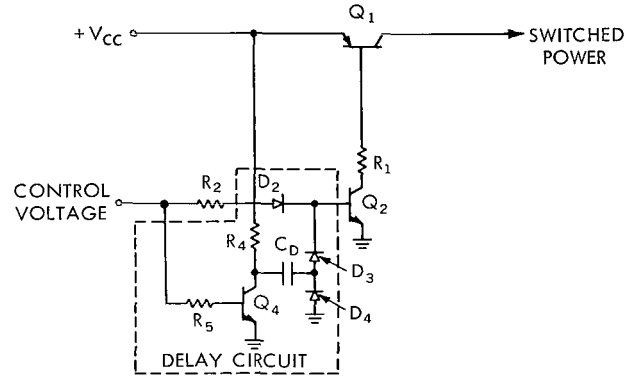

Figure 8—Series power switch with turn-off delay.

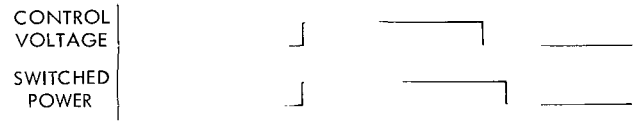

Figure 9—Turn-off delay.

Figure 8 shows how turn-off delay is obtained. When the control signal is at ground and the switched power is off, C_D is charged, and no current flows anywhere in the circuit. Then, when the control input goes positive, Q_2 is turned on through R_2 and D_2, thus turning on Q_1 and the switched power. Q_4 is also turned on, discharging C_D through Q_4 and D_4. The steady state reached when C_D has discharged continues until sometime later when the control signal returns to ground. The base drive to Q_2 through R_2 and D_2 ceases; but now, Q_4 has ceased conducting, and base drive to Q_2 continues through R_4, C_D, and D_3. Therefore, the switched power stays on, even though the control input is at ground again. When C_D becomes fully charged, current stops flowing through it to the base of Q_2, and Q_2 turns off. That turns off Q_1, which turns off the switched power. The delay time is determined by the time constant R_4 C_D. Figure 9 shows the control and power waveforms.

The Complete Power Switch

The complete power switch circuit appears in Figure 10. Risetime control, reset output, and turn-off delay are all provided. Figure 11 shows the control, switched power, and reset waveforms.

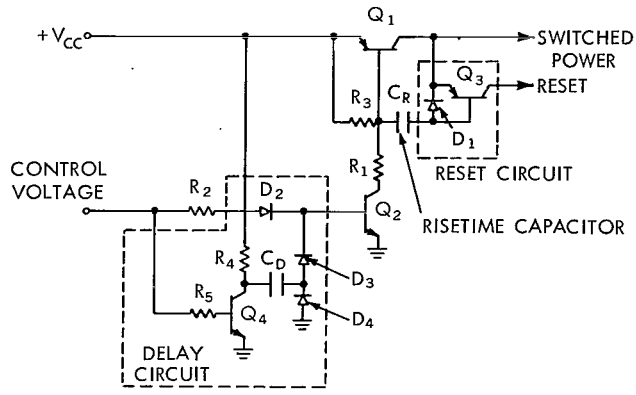

Figure 10—Complete power switch circuit.

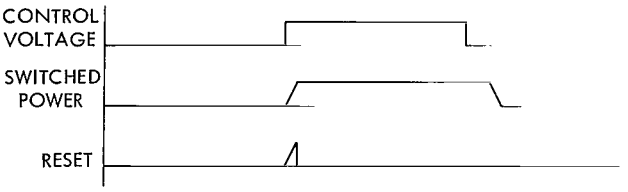

Figure 11—Complete circuit.

Observe that when the control voltage goes positive, the switched power and the reset output rise together. Then when the switched power reaches full value, the reset turns off, and computation can begin. After computation is complete, the control voltage returns to ground. During the turn-off delay interval, data resulting from the computation are transferred from the section of the system controlled by this power switch into the next section. At the end of the turn-off delay interval, this power switch turns off, and no further power is dissipated in it or in the section of the system which it controls.

Data Transfer by Power Switching

Let us consider the use of power switching in a little more detail. We will assume that we have a digital computer with two sections, labeled A and B in Figure 12. Each section has its own power switch, and each power switch has an appropriate control input. The important waveforms are shown in Figure 13. When the Control A voltage goes positive, Computer Section A is turned on and reset. Then data enter Section A, and computation occurs. After the computation in Section

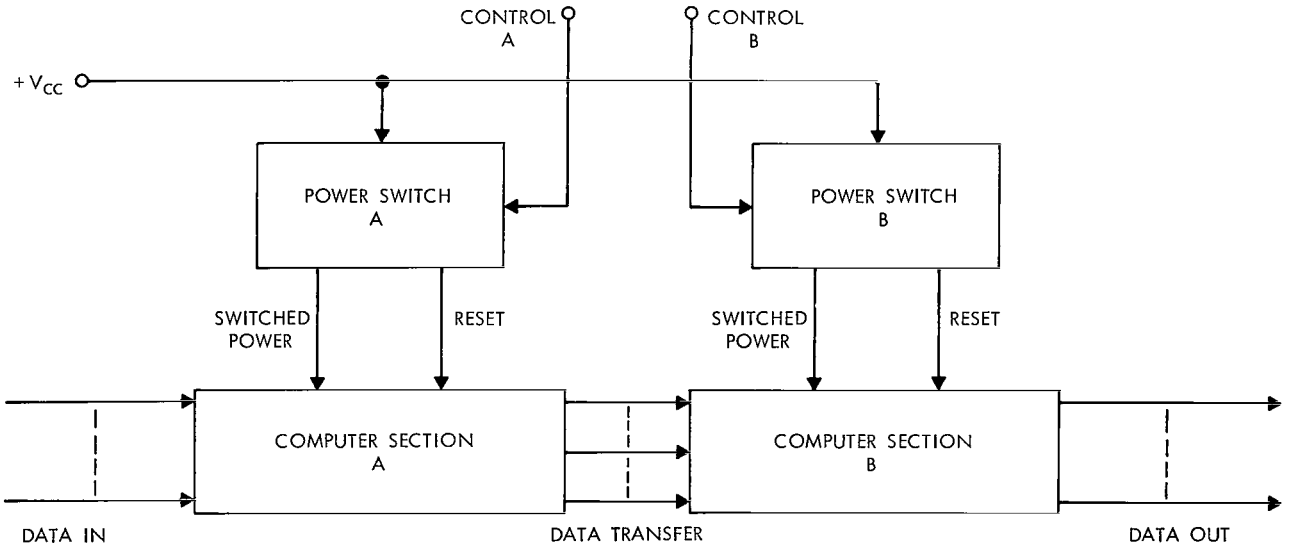

Figure 12—Power switches in digital system.

A is complete, Control A returns to ground, and Control B goes positive. Computer Section B is turned on and reset. The power to Section A is still on because of the turn-off delay in Power Switch A.

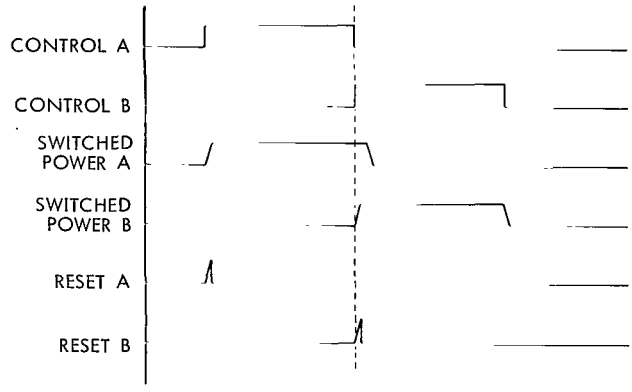

Figure 13—Power switch waveforms in digital system.

Figure 14 shows how the data transfer from Section A to Section B through the action of the power switches. One stage of a register is shown in the dashed box labeled Section B. When the power to Section B is turned on, the Reset B signal insures that this register stage will be in the "0" state if there is a "0" (no voltage) at the output of Section A. On the other hand, if the output from Section A is a "1" (+ voltage), then as soon as the Reset B signal is removed, the register stage is set to the "1" state. When the power to Section A is turned off at the end of the turn-off delay interval, Section A has no further effect on Section B, and computation can proceed in Section B.

These techniques are not limited to a system with two sections, of course. Any number of sections may be cascaded, or even connected into recirculating loops. Not only can power switching be used to reduce average power consumption, but also it can be used to eliminate the need for many data transfer gate circuits.

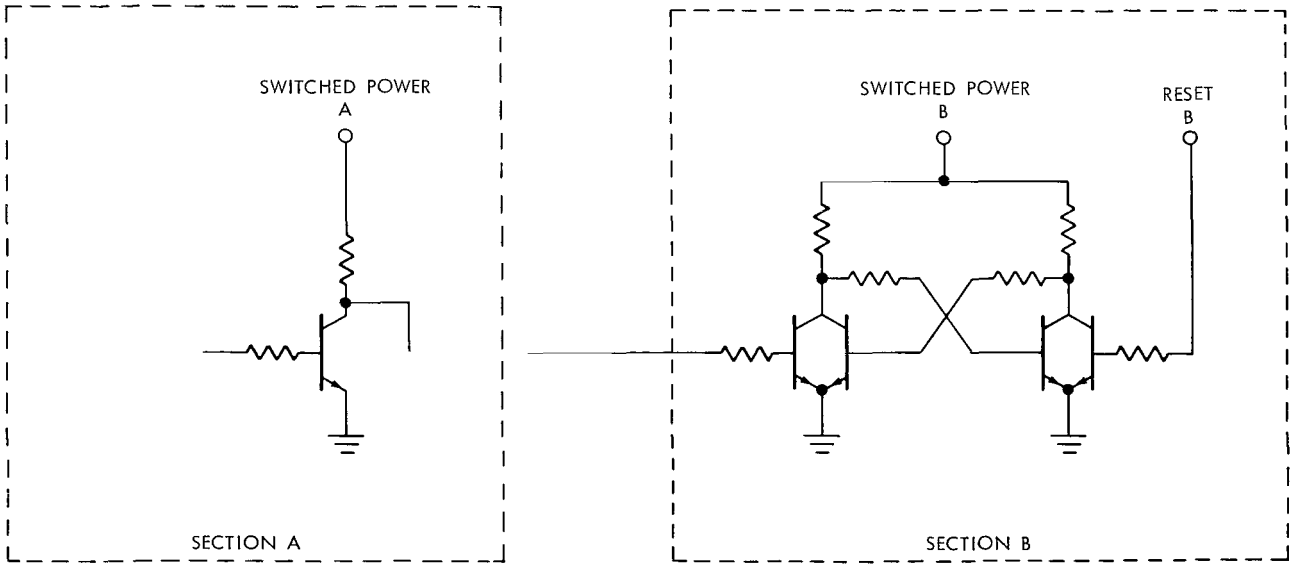

Figure 14—Data transfer.

SUMMARY

Power switching is a valuable technique because it reduces average power consumption. At the same time, it permits the elimination of many gate functions. This has the secondary advantage of reducing complexity. Power switching is particularly attractive where computation can be done sectionally and where large amounts of data are transferred between sections in parallel.

(Manuscript received January 7, 1966)

"The aeronautical and space activities of the United States shall be conducted so as to contribute . . . to the expansion of human knowledge of phenomena in the atmosphere and space. The Administration shall provide for the widest practicable and appropriate dissemination of information concerning its activities and the results thereof."

—NATIONAL AERONAUTICS AND SPACE ACT OF 1958

NASA SCIENTIFIC AND TECHNICAL PUBLICATIONS

TECHNICAL REPORTS: Scientific and technical information considered important, complete, and a lasting contribution to existing knowledge.

TECHNICAL NOTES: Information less broad in scope but nevertheless of importance as a contribution to existing knowledge.

TECHNICAL MEMORANDUMS: Information receiving limited distribution because of preliminary data, security classification, or other reasons.

CONTRACTOR REPORTS: Technical information generated in connection with a NASA contract or grant and released under NASA auspices.

TECHNICAL TRANSLATIONS: Information published in a foreign language considered to merit NASA distribution in English.

TECHNICAL REPRINTS: Information derived from NASA activities and initially published in the form of journal articles.

SPECIAL PUBLICATIONS: Information derived from or of value to NASA activities but not necessarily reporting the results of individual NASA-programmed scientific efforts. Publications include conference proceedings, monographs, data compilations, handbooks, sourcebooks, and special bibliographies.

Details on the availability of these publications may be obtained from:

SCIENTIFIC AND TECHNICAL INFORMATION DIVISION

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

Washington, D.C. 20546