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METHODS FOR DETERMINING BLOOD FLOW THROUGH INTACT VESSELS OF EXPERIMENTAL ANIMALS UNDER CONDITIONS OF GRAVITATIONAL STRESS AND IN EXTRA-TERRESTRIAL SPACE CAPSULES

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SUMMARY

This is the final report covering the research conducted on methods for determining blood flow through intact vessels of experimental animals under conditions of gravitational stress and in extra-terrestrial space capsules. Much of the work of this project was devoted to the understanding of the basic principles and limitations of measuring blood flow utilizing the technique of Faraday. Since the latter stages of research were entirely given to the development of a stable, accurate blood flowmeter, this report is devoted only to an accurate account of it.

The project was not limited to the study of blood flowmeters, but encompassed several other investigations, some of which were purely physiological in nature. These researches, including those blood flow studies which led to the final flowmeter development, have already been reported[1-10] in entirety. Included are:

Experimental and analytical studies of auto-regulation of the myocardial vascular bed and the relation of organ blood flow to levels of physiologic activity;[1,2,4,5,6,7]

An investigation of the hemodynamics of blood flow through the liver;[2,8]

A preliminary examination of the conceptual basis, construction, refinement and use of an electrical analogue of the pulmonary circulation;[2,9]

The theory and prototype construction of an implantable blood oxygen saturation sensor and hermatocrit sensor utilizing optical backscatter techniques;[3]

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[1] For numbered references, see Sec. IV.

An experimental design of the assessment of the effects of sustained space flight on physiologic performance;[3]

An analysis of orbiting systems for sustained (30 - 90 day) orbital studies of primates;[3]

Fundamental flowmeter studies[1,2,3,10] such as the effects of radial asymmetry of flow profile on the indication of electromagnetic flowmeters;

Development of preliminary model blood flowmeters including results;[1,2,3]

Development of a flight model blood flowmeter and its use on Rhesus monkeys with chronically implanted probes.

As previously stated, this final report deals only with the development of a stable, accurate electromagnetic blood flowmeter. Although time did not permit the use of the device chronically implanted in animals, it was adequately demonstrated with one of the preliminary models that the techniques, devised to obviate the effects of artifact signals, did work. These signals have adversely affected similar flowmeters. Some difficulty was experienced with the probe magnet driver circuit and a better design is indicated.

The use and refinement of the techniques employed in this meter are recommended to other researchers engaged in blood flow studies.

AUTHORIZATION

The research summarized in this report was performed in the Biomedical Engineering Laboratory of the Electronics Research Laboratories of Columbia University. This report was prepared by D. Porter.

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I. GENERAL INTRODUCTION

Experience with the Flowmeter Model A previously described[1] has vindicated the basic condition upon which it was based - that the magnetic field, though alternating rapidly should be constant during the time that the electrode signal is sampled and averaged. If this condition is met, then any signal at the electrodes which is synchronous with the sampling program will be solely a consequence of flow and not the result of the probe acting as a transformer. Experience with the earlier model has indicated that transformer action can be rendered negligible, as by means of split electrode leads and a balancing potentiometer, only in a static and therefore unrealistic environment. The mere presence of the hand near a probe which had been balanced in a saline bath would induce a shift from zero indicated flow to as much as 20 per cent of maximum rated flow. There is some evidence that this "proximity effect" can be reduced by making the field more uniform but this leads to probes of intolerable bulk.

Once the idea of residual magnetic coupling in the probe was accepted, the manner in which the associated electronic circuits in the Flowmeter Model A converted these coupled signals (proportional to the rate-of-change of flux) into the equivalent of flow induced signals was investigated. Circuits were devised which displayed a high degree of immunity to coupled signals (spikes) having amplitudes of several hundred times that of the maximum average flow signal likely to be produced in vivo. Construction of a Flowmeter Model B was undertaken with a view to demonstrating the most versatile of these circuits and to determining thereby those values of certain parameters which are optimum in practice.

In special applications, where, for example, a fixed repetition rate or only a single probe is required, adequate precision may be afforded by the simplest circuits discussed here. In any case the design of a flowmeter of minimal complexity may now be contemplated with a foreknowledge of the precise mechanism of the residual errors to be expected and the cost of reducing them.

II. METHODS OF ARTIFACT COMPENSATION

A. RECEIVER AND ARTIFACT PROBLEMS

1. Review of the Receiver Problems

The electromagnetic blood flowmeter depends for its operation upon the fact that a voltage is induced in a conductor when it moves in a magnetic field. In the device to be described, the moving conductor is blood and an electromagnet produces the field. Connections to the blood are provided indirectly through the blood vessel walls by means of electrodes which are an integral part of the magnet support structure. The completely sealed assembly is called a probe.

The flow-induced component of the electrode signal is usually very small compared to the galvanic, EKG, EMG, equivalent amplifier drift and other noise components. The receiver amplifiers required to bring the flow component up to a measurable size would be saturated by the sum of the other components unless these components were attenuated sufficiently. Such attenuation may be accomplished by high-pass coupling. This is feasible because the flow component can be translated upward in frequency, by modulation, independently of the others. This independent modulation can be achieved because the flow component alone is strictly proportional to the magnetic field. The required alternating field can be produced by an appropriate current in the electromagnet, and the flow component separated with great precision by synchronous demodulation. The foregoing is summarized in Fig. 1.

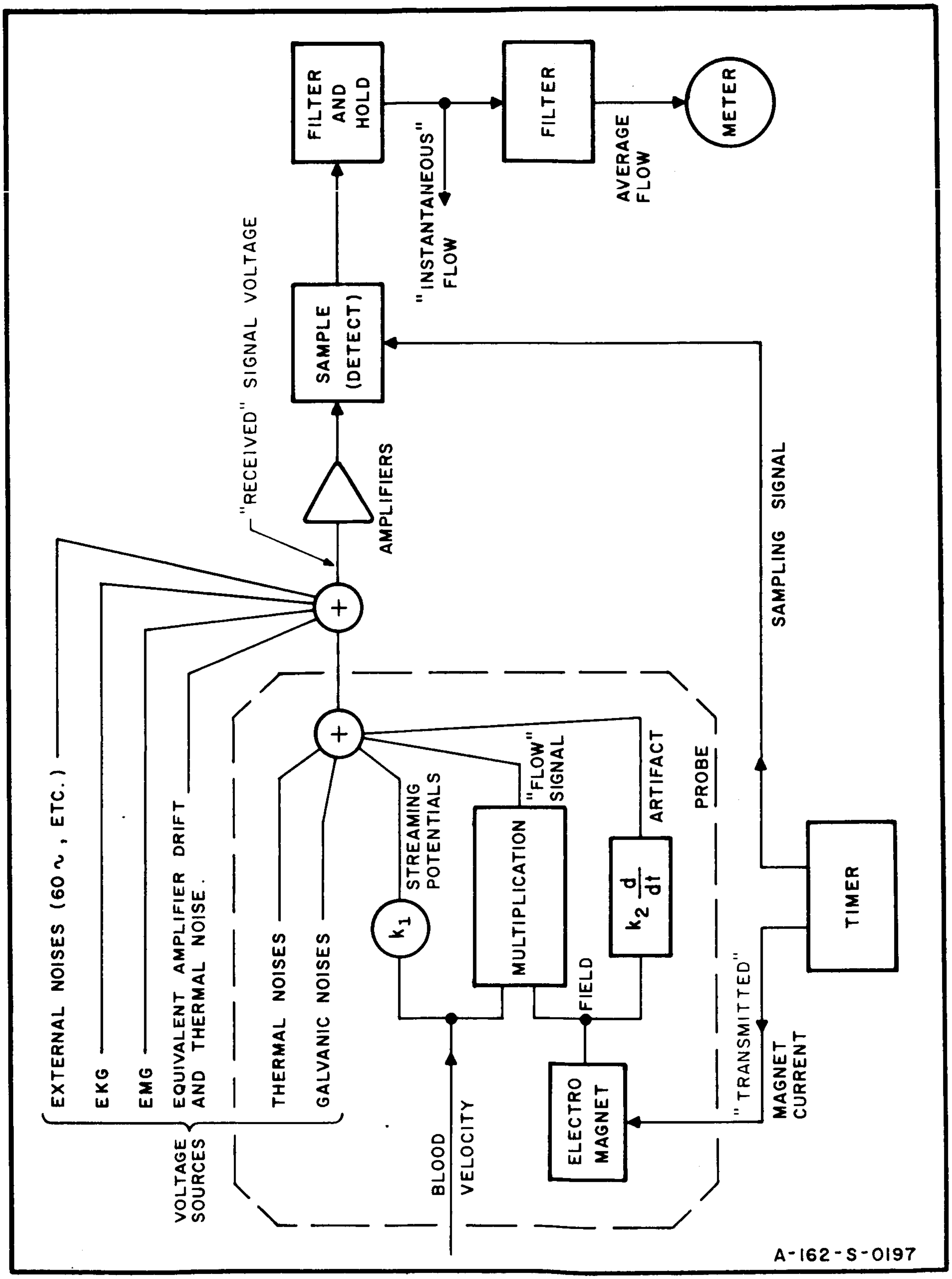


FIG. 1 GENERAL PLAN FOR FLOW MEASUREMENT.

The changing field induces an undesired signal in the inevitable loop (see Fig. 2) formed by the electrode leads. This signal can be minimized under static conditions if the probe has a split electrode lead connected to the ends of a potentiometer used to balance out the induced signals. But in vivo the orthogonality of the magnetic axes of the electromagnet and the electrode loop is rapidly and continuously being disturbed.

So, while the alternating field enables the separation of the flow signal from the overpowering noise, it also produces a signal, the artifact, at the electrodes which is (1) proportional to the rate-of-change of magnet flux, (2) has an unpredictable envelope, and (3) is objectionable because it is itself capable of saturating amplifiers, and, being synchronous, it can give rise to false indications of flow. It will be shown that these objectionable qualities can be negated.

Since an error-free indication of flow cannot be obtained during the time that the magnetic flux is changing, this time must be minimized. One can do no better in this respect than to apply the maximum permissible voltage to the electromagnet until the change is complete. If the inductance of the electromagnet is constant and its resistance is negligible,then a current waveform which is trapezoidal can be shown to be optimum. Whatever the shape of the voltage applied to the magnet, or induced as a result at the electrodes at this time, it will be called a "spike" or in the latter case, an artifact. A signal proportional to the derivative of the spike may also appear as a result of stray capacity, but this has been found experimentally to be without effect upon flow measurement.

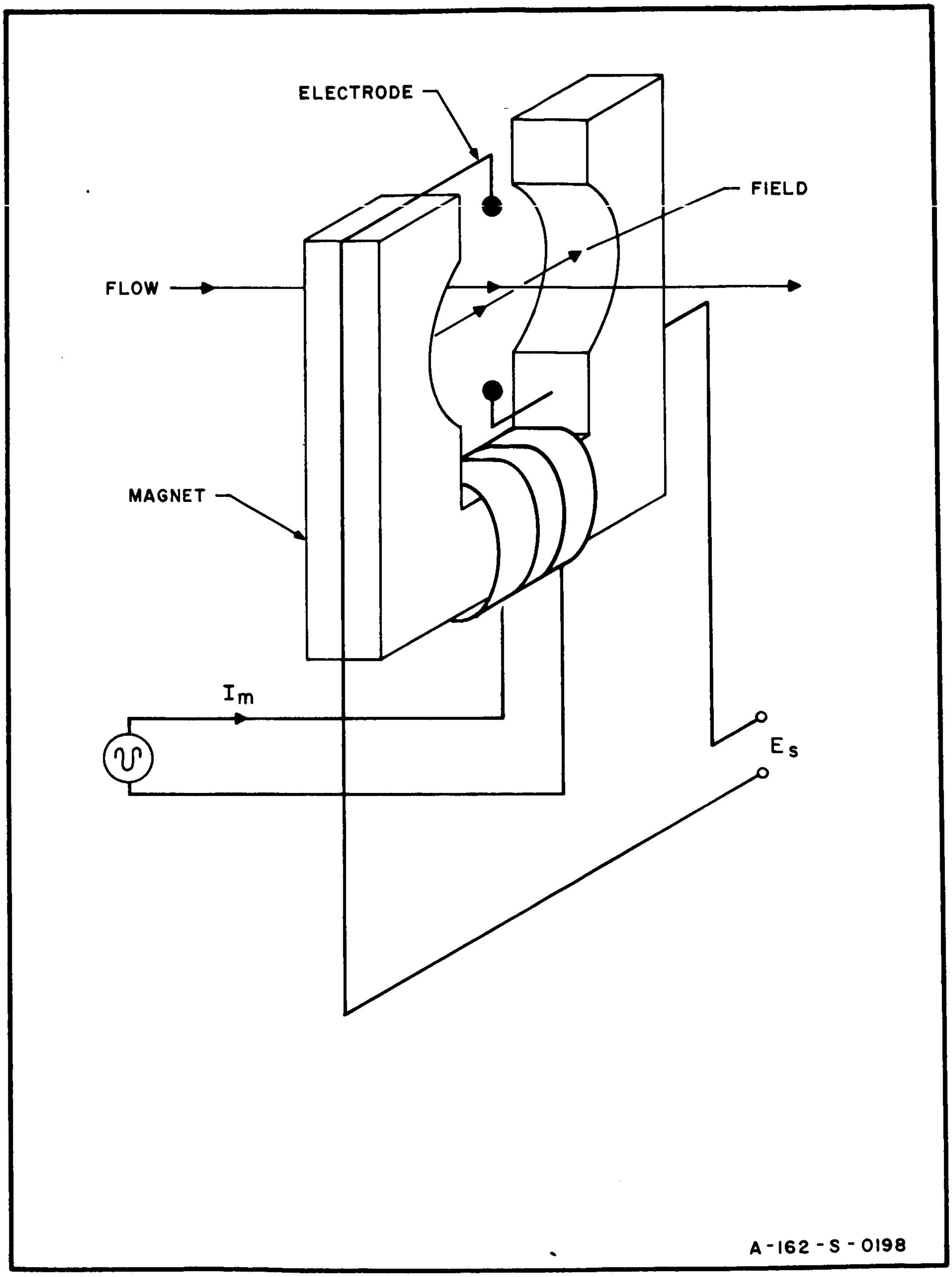


FIG. 2 PROBE GEOMETRY

2. Effects of the Artifact

Modulation of the flow signal does permit high-pass coupling in the electrode-amplifier-sampler chain and thereby minimizes the time during which amplifier saturation occurs as a response to useless DC and low-frequency signals, but the output of a high-pass network after the end of an input spike approaches zero asymptotically. This suggests that the start of the sampling interval should be delayed to allow for appreciable decay of the unwanted signal or "tail." It is important to utilize as much as possible of the "non-spike" time for sampling and averaging the "flow" signal. Averaging (or filtering) is important because the signal is corrupted by high frequency noise, and by signals roughly proportional to the derivative of the low frequency noise. (The cause of the latter will be detailed in the general discussion of demodulators (Section III-C.3).)

In simple cases tails may be called negative or positive according to whether they result from high-pass or low-pass networks as illustrated in Fig. 3. Under typical conditions the errors stemming from the use of such high-pass networks as are necessary can be as great as 20 per cent of full scale, while those resulting from the high frequency limitations of amplifiers (low-pass errors) are easily made negligible.

B. COMPENSATION TECHNIQUES

1. Compensation by Sampling Network

In this scheme the spike which appears along with its tail at the output of the high-pass is switched into a similar network and the results are subtracted as shown in Fig. 4. The a priori knowledge of spike arrival time is employed to preconnect the composite signal to a network

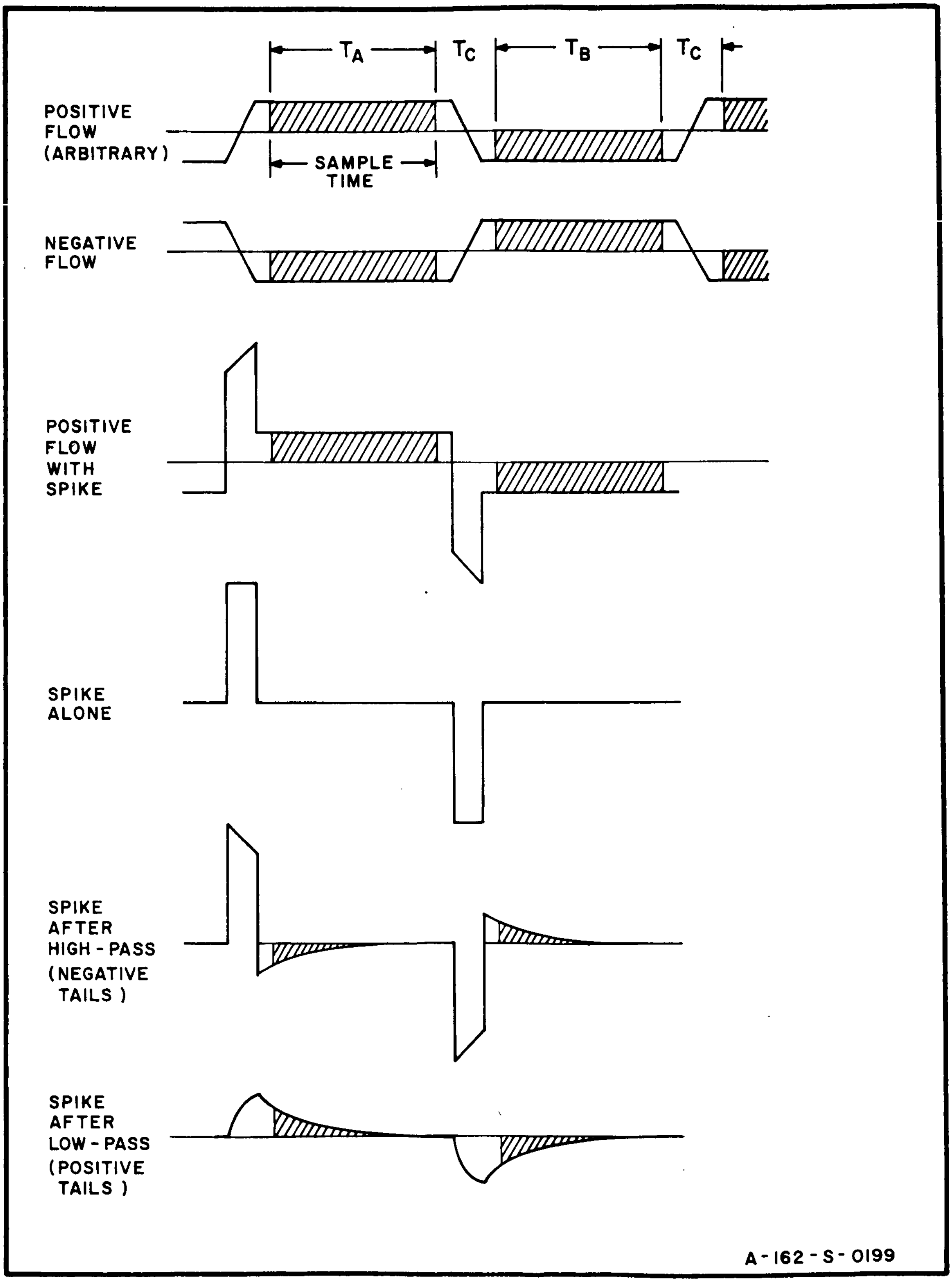


FIG. 3 FLOW SIGNALS, SPIKES AND TAILS.

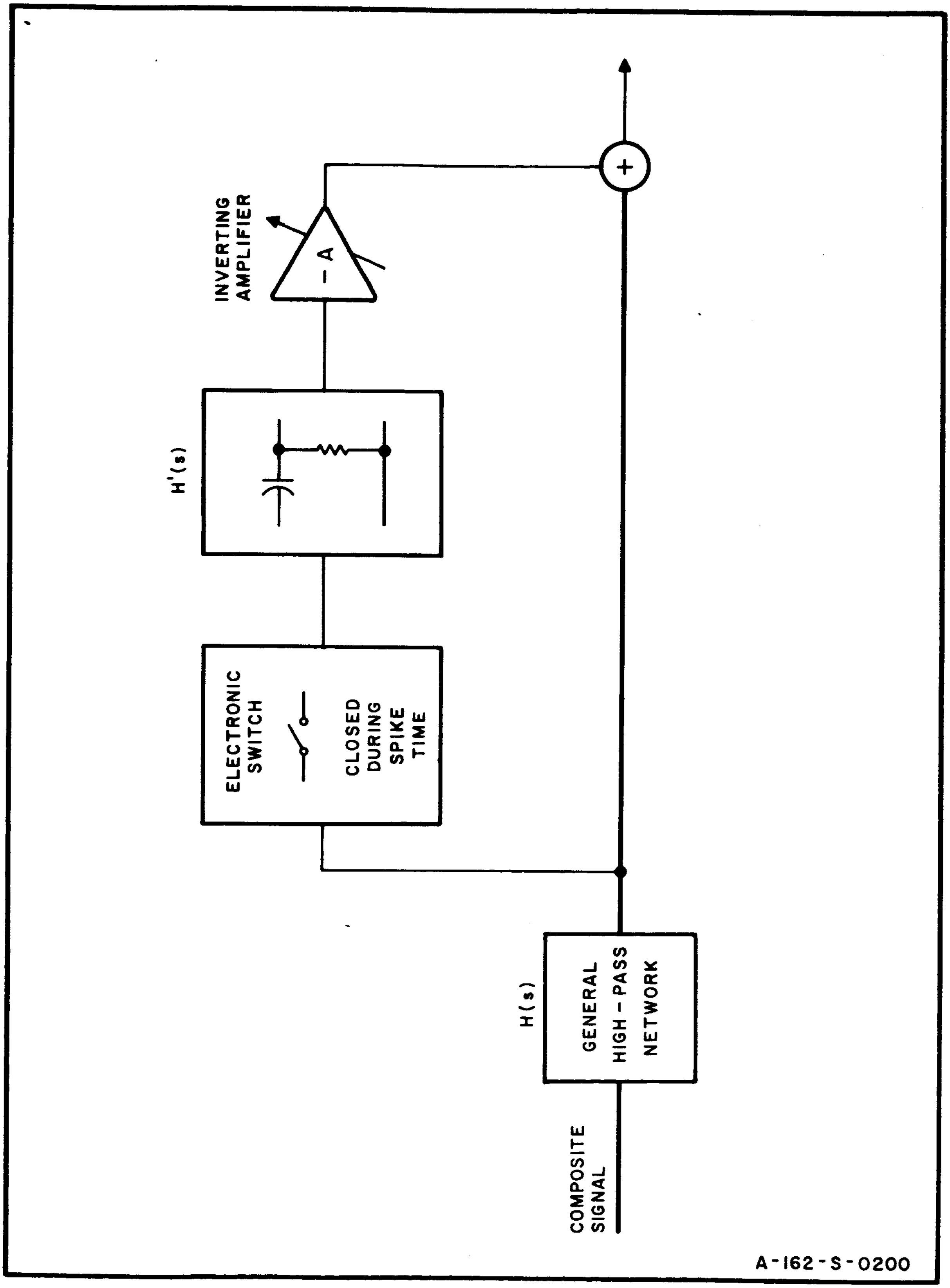


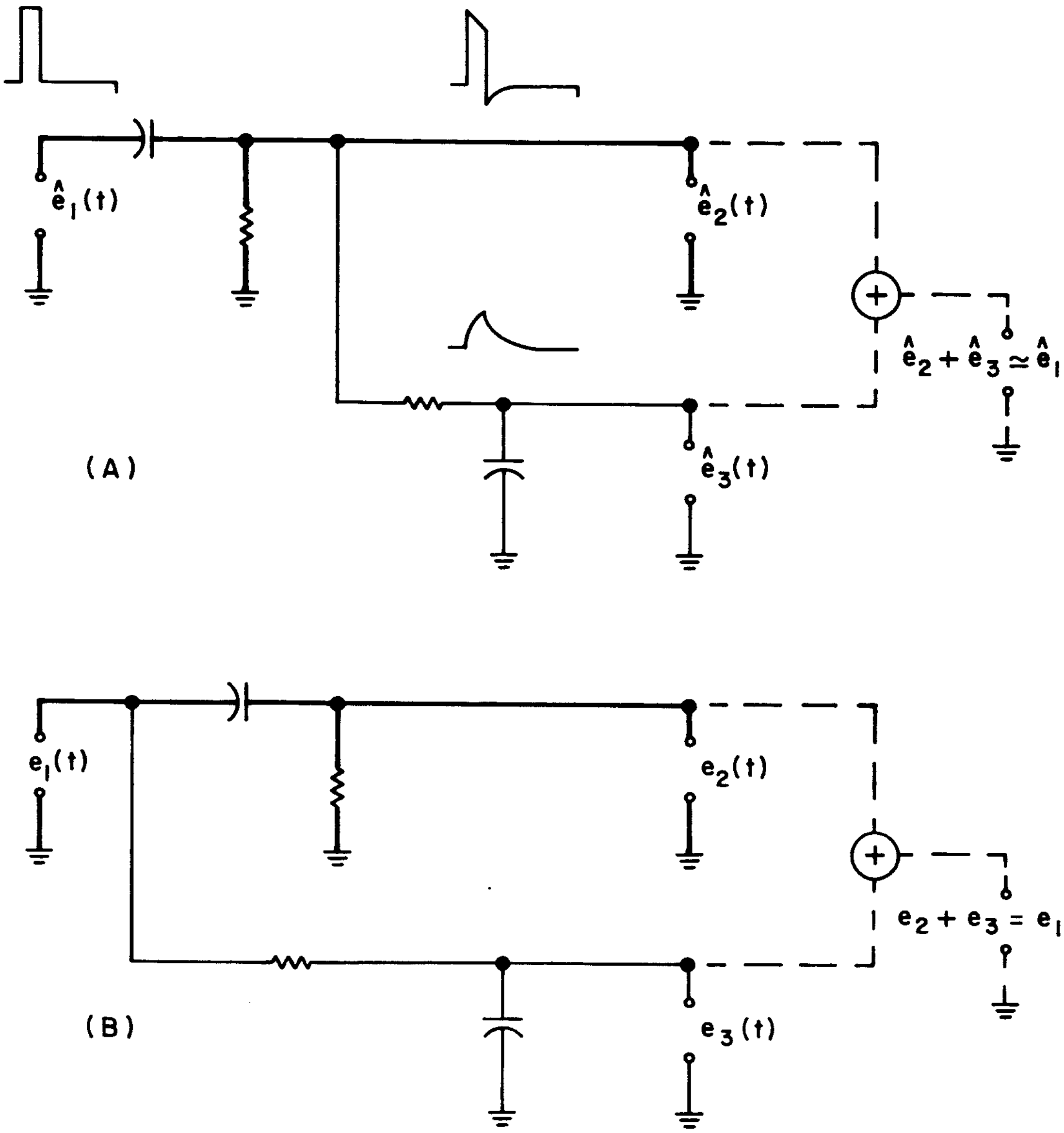
FIG. 4 A COMPENSATOR OF THE SAMPLING-NETWORK TYPE .

H'(s) which then produces a tail, proportional to the spike area, which is simultaneously subtracted from the original signal. When the transient pulse is relatively narrow and the distortion of this pulse is due almost exclusively to the high-pass characteristic of H(s) the adjustments necessary for the tails produced by H(s) to be cancelled in effect by those produced by H'(s) are not especially critical. This scheme has the further advantage that the spikes tend to cancel each other. This may permit high-pass coupling of the resulting signal without further compensation. Moreover, it reduces the compliance which is required of succeeding stages because of the artifact (spike) signal alone.

2. Compensation by Passive Network

Under the conditions of (a) constant repetition (carrier) frequency and (b) constant spike width a positive-tail-making low-pass network may be found which will compensate for a negative tail, caused by previous high-pass network(s), and vice versa. The compensating network is simply placed anywhere in the signal chain. Though the determination of the proper time-constant for the network may be computationally outrageous, it is experimentally trivial - a single RC low-pass network having been found sufficient to compensate precisely for the sequence of seven high-pass interstage networks in the Model A Flowmeter[1] under the stated conditions. Typically, the average value of the output over the sampling interval is zero, while the function, except at one point, is not.

Fairly good results may also be obtained with the type of circuit suggested by Fig. 5(A) which, for signals



NOTE :

$$E_2(S) = \frac{S}{S+A} E_1(S) \quad \text{AND} \quad E_3(S) = \frac{B}{S+B} E_1(S)$$

$$A = B \implies E_2 + E_3 = E_1$$

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FIG. 5 (A) HIGH-PASS NETWORK WITH SIMPLE COMPENSATOR AND (B) DISTORTIONLESS NETWORK RESEMBLING (A) .

which are narrow spikes, produces output waveforms corresponding very closely to those of the network shown in Fig. 5(B). The latter network can be made absolutely distortionless by setting the two RC products equal. This scheme, in comparison with the preceding one, has the advantage of being more simple but the disadvantage of being more critical in adjustment. In principle, a network could be found which would allow some variation in conditions (a) and (b) for a given error tolerance. However, this is a problem in time-domain synthesis which may leave one, after much speculation and computational labor, far from an optimal solution except in a limited range of conditions.

3. Compensation by Active Network

The response of a linear network to a rectangular pulse has a tail unless, of course, the network is "flat," i.e., equivalent to pure amplification (and/or time delay which we shall ignore). Hence, one way to compensate for tails is to insert an inverse network somewhere in the signal channel. If, in Laplace transform notation, the existing network is described by $H(s)$, then $F(s)$ must be found such that $H(s) \cdot F(s) \equiv 1$. If the low-frequency attenuation of a high-pass network is compromised by the addition of r_1 shown in Fig. 6, the compensator may take the very practical form also shown. The conditions for e_4 to be exactly equal to Ke_1, assuming that A is real are:

$$\alpha_2 = \frac{A+1}{A} \alpha_1$$

$$\beta_2 = \beta_1 - \frac{1}{A} \alpha_1 \quad .$$

The assumption is quite valid if A represents a DC amplifier because the contribution of this amplifier to the total

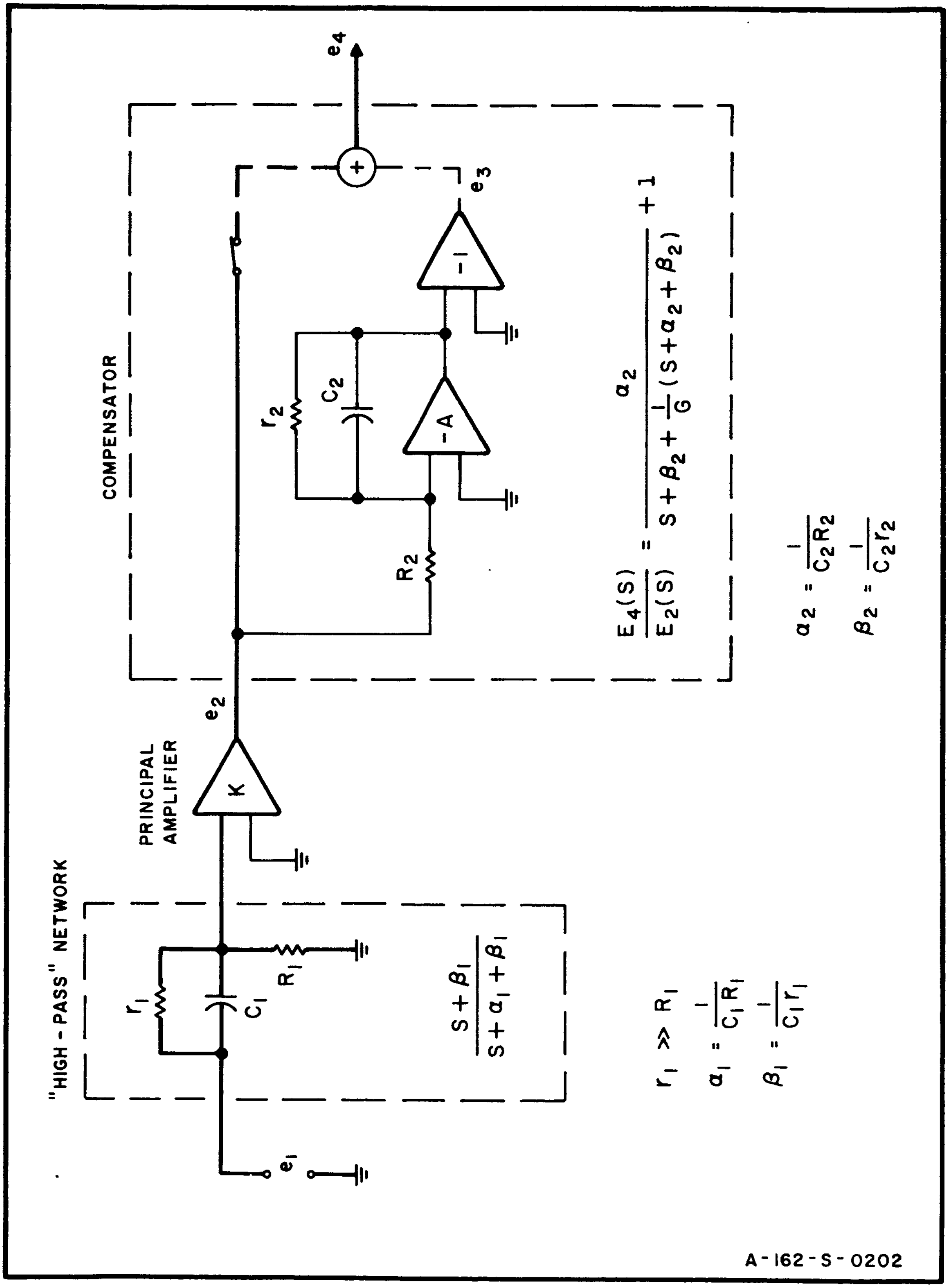


FIG. 6 COMPENSATION BY INVERSE NETWORK WITH OPTIONAL ARTIFACT GATING

ouput diminishes with frequency and therefore the amplifier bandwidth need not be very great. Note that because the relative signal levels in this circuit are as given below,

	ARTIFACT	LOW FREQUENCY NOISE	(FLOW SIGNAL)
e_2	Large	Small	(Large)
e_3	Small	Large	(Small)

most of the artifact signal may be eliminated by means of an electronic gate inserted where a switch is shown in the figure. The linearity and gain stability of the gate, if used, are important because the gate is in the path of most of the flow information. In other respects this scheme depends for its precision upon the same factors as does the precision of an analog computer.

What the preceding circuit lacks is the capability for handling signals having a relatively large bias, i.e., a streaming potential. (See Fig. 1.) Circuits with such capability were suggested by a study of the inverses to strictly high-pass networks such as the following:

NETWORK	INVERSE
Single high-pass: $H(s) = \frac{s}{s+\alpha}$	$F(s) = 1 + \frac{\alpha}{s}$
Double high-pass: $H(s) = \frac{s}{s+\alpha}\,\frac{s}{s+\beta}$	$F(s) = 1 + \frac{\alpha+\beta}{s} + \frac{\alpha\beta}{s^2}$

Each of these inverse networks is "realizable" to a high degree of precision by means of integrators. The first corresponds to the network of Fig. 6, where $r_1 \to \infty$. This implies that $\beta_1 \to 0$ and either $\beta_2 \to -\frac{1}{A}\alpha_1$, which is impossible, or $A \to \infty$, in which case $\alpha_2 \to \alpha_1$ and $\beta_2 \to 0$.

The last condition requires that $r_2 \to \infty$ and thus the compensator contains an integrator. The presence of an integrator in the path of the meandering electrode signal does not aggravate the problem of amplifier limiting, but actually relieves it as will be explained next.

The high-pass elements were introduced originally to prevent the system from being overloaded by galvanic, low frequency noise, streaming, and perhaps amplifier drift potentials. Each integrator in the inverse network tends to restore these potentials. If this were all it did it would serve no useful purpose. Limiting must be accepted. In practice, the limit voltage of an amplifier is set somewhat below that at which saturation of active elements would occur, by means of an auxiliary biased-diode feedback path.* The effect of ideal limiting of an integrator in an inverse network will be described by example.

Suppose that an integrator has an input signal which would cause its output to exceed its limit voltage in the manner suggested by the dotted line in Fig. 7. Limiting takes place from T_1 to T_2 (during which time the compensator does not function as an inverse network and tails may appear). But integration is resumed as soon as the input polarity, and therefore the output direction, reverses (at T_2). Afterward, the integrator continues to perform as it would have if limiting had been prevented by initially offsetting the output voltage by an exactly sufficient amount as shown by the dashed line. The effect of the limiter is therefore to reset the integrator to a new initial condition which is optimum for the type of signal being encountered. Since tailing errors are eliminated except during the time

* Described in Section II-C.2.

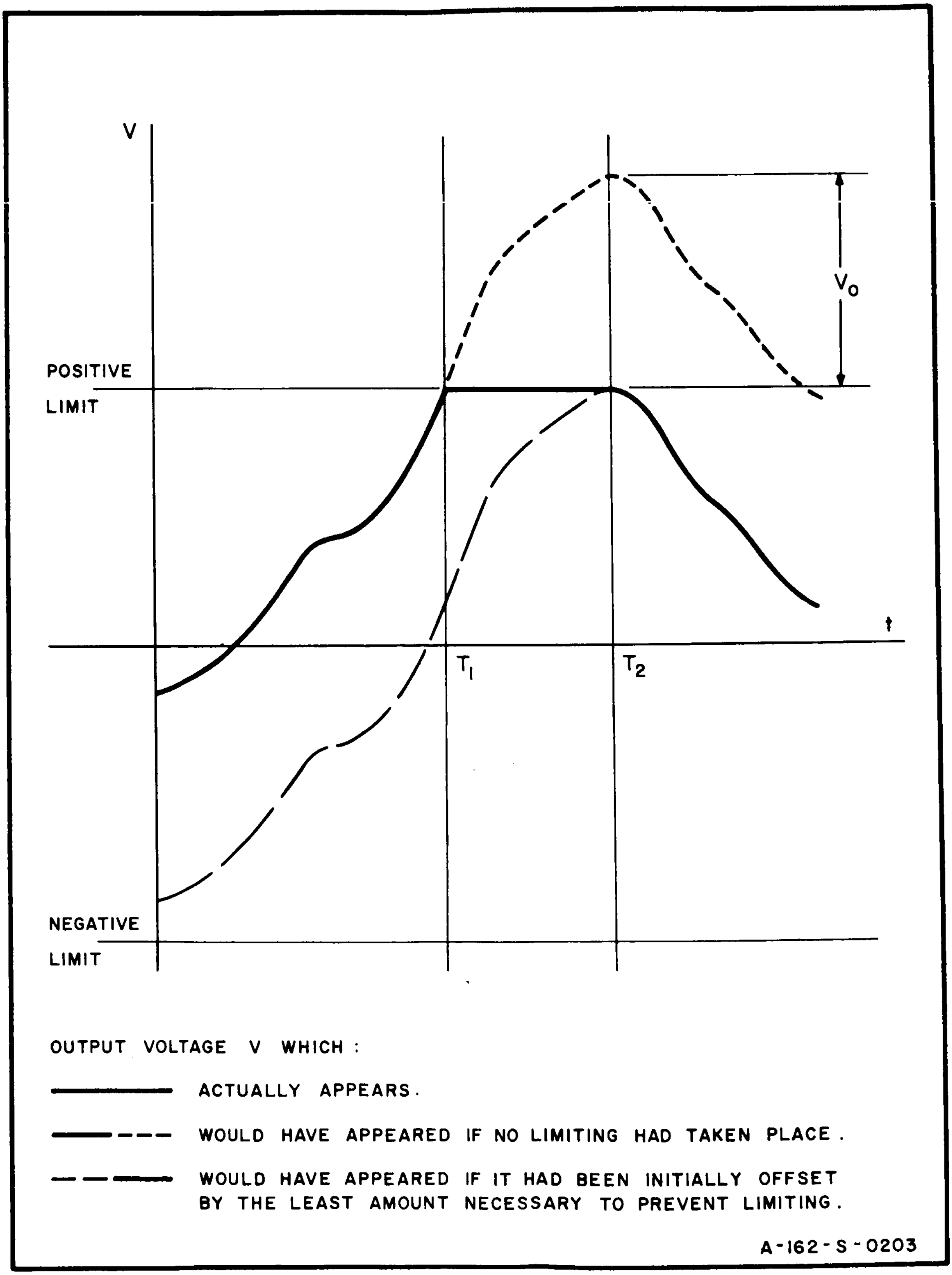


FIG. 7 OUTPUT VOLTAGE OF INTEGRATOR WITH EXCESSIVE INPUT.

that noise crests exceed the limits, these limits should be set as high as is practicable.

In general the highest order of integration required in the inverse network is equal to the total number of cascaded high-pass stages in the network, or, more formally, to the order of the transmission zero at zero frequency. The second order case is of particular interest because of its applicability to the design of the flowmeter. An example of such a doubly high-pass coupled amplifier-compensator combination, having a low frequency response limited only by the gain of the amplifiers used for integration, is shown in Fig. 8. The first high-pass network consists of C_1 and R_1; the second, C_2, and R_3 in parallel with R_4. These correspond to the factors in the network function

$$H(s) = \frac{s}{s+\alpha} \cdot \frac{s}{s+\beta} .$$

In the compensator, there is an adder with three inputs corresponding, from top to bottom, to the three terms in the inverse function

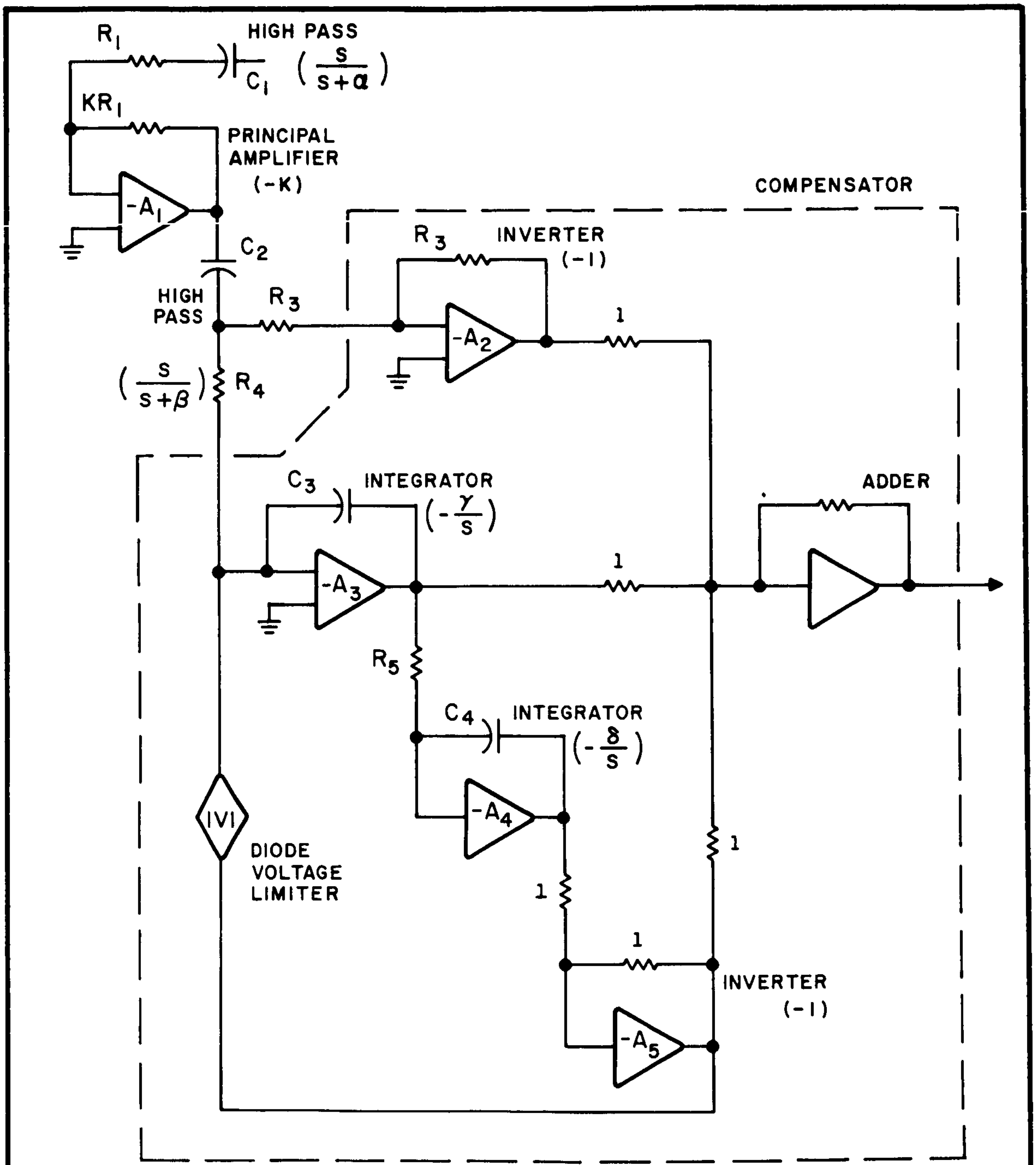
$$F(s) = 1 + \frac{\gamma}{s} + \left(\frac{\gamma}{s} \cdot \frac{\delta}{s}\right) .$$

A single diode voltage-limiter serves both integrators in a manner which has been found to be very satisfactory in practice.

C. IMPLEMENTATION OF A COMPENSATED SYSTEM

1. The Compensator

After its effectiveness had been demonstrated, an active-network type compensator was chosen for the Model B flowmeter. It was found necessary for it to be of second



COMPENSATOR CONDITIONS :

$\gamma = \alpha + \beta$ $\qquad \delta = \dfrac{\alpha\beta}{\alpha+\beta}$ $\qquad A \longrightarrow \infty$

WHERE

$\alpha = \dfrac{1}{C_1 R_1} \qquad \beta = \dfrac{R_3+R_4}{C_2 R_3 R_4} \qquad \gamma = \dfrac{R_3+R_4}{C_3 R_3 R_4} \qquad \delta = \dfrac{1}{C_4 R_5}$

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FIG. 8 SECOND ORDER COMPENSATOR EMPLOYING DISTINCT INTEGRATORS.

order because two cascaded DC feedback amplifiers are required to produce sufficient over-all gain, bandwidth and precision, and the DC offset of each must be nullified. But it was demonstrated that the same properties as those of the second order compensator previously described are obtainable with fewer amplifiers. The design procedure for this compensator was not exhaustive with respect to the choice of network configurations but it is described here because of the neatness of the result.

The requirement that the compensator perform independently of the amount of offset voltage at its input is satisfied by the assumed configuration of Fig. 9(A). The transfer function $G(s)$ must be a solution of the equation

$$\frac{s}{s+\alpha}\left(\frac{s}{s+\epsilon} + G(s)\right) = 1$$

and it is assumed to be obtainable by means of a single amplifier in the general feedback configuration of Fig. 9(B). The details of network synthesis are given in Appendix 3, and Fig. 10 shows the result.

In summary, the inverse-network schemes eliminate tailing error independently of spike or sampling duration. They are unique among the schemes considered in that they cause the flow indication to be independent of repetition rate.

2. Auxiliary Circuits

In the flowmeter circuits some uncommon diode configurations appear in conjunction with signal amplifiers. One of these, the voltage bridge, referred to in Section II-B.3., is used as an additional feedback path to limit an

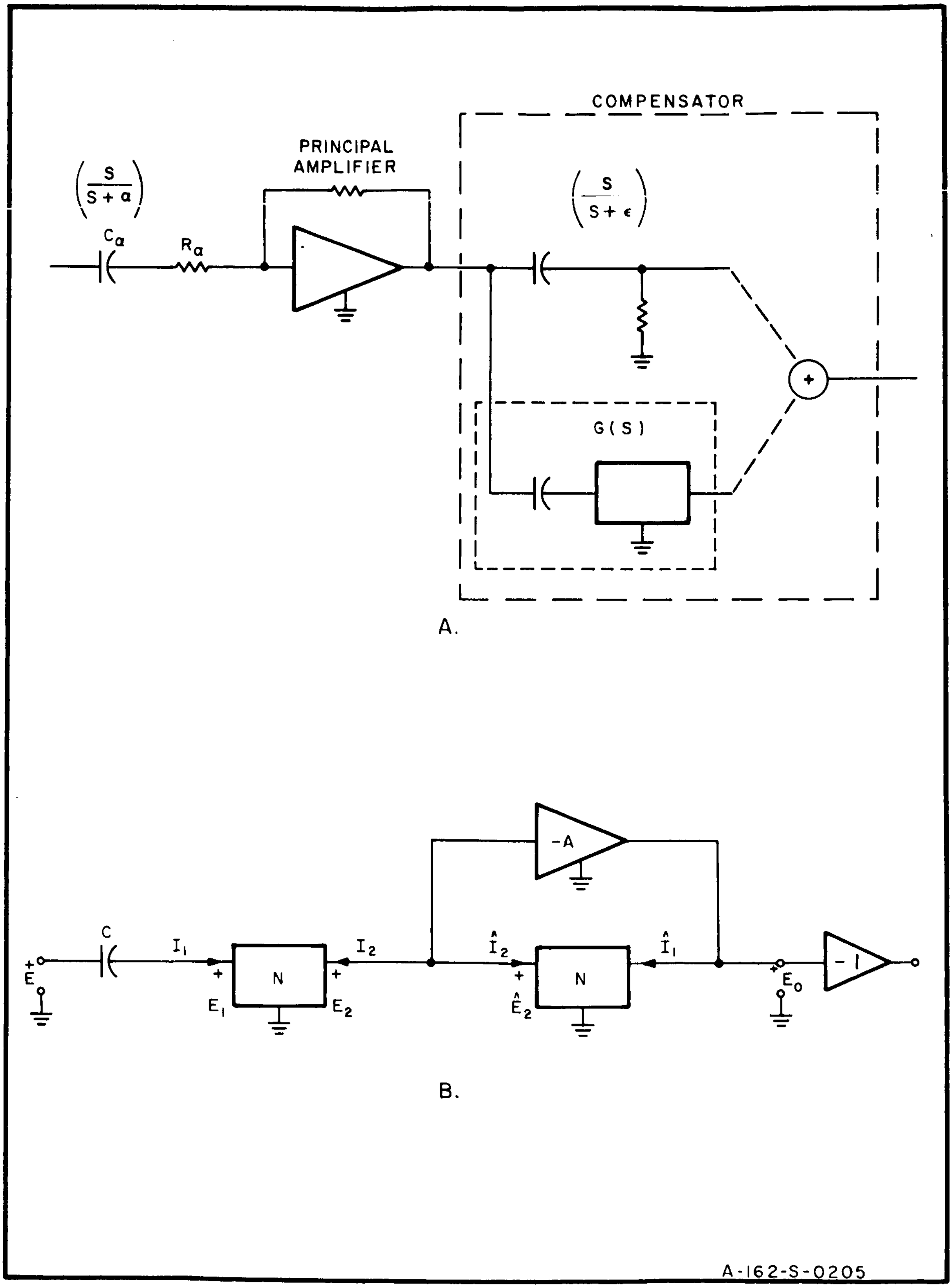


FIG. 9 A. ASSUMED FORM OF COMPENSATOR CONTAINING UNSPECIFIED NETWORK G(S)
B. ASSUMED FORM OF G(S).

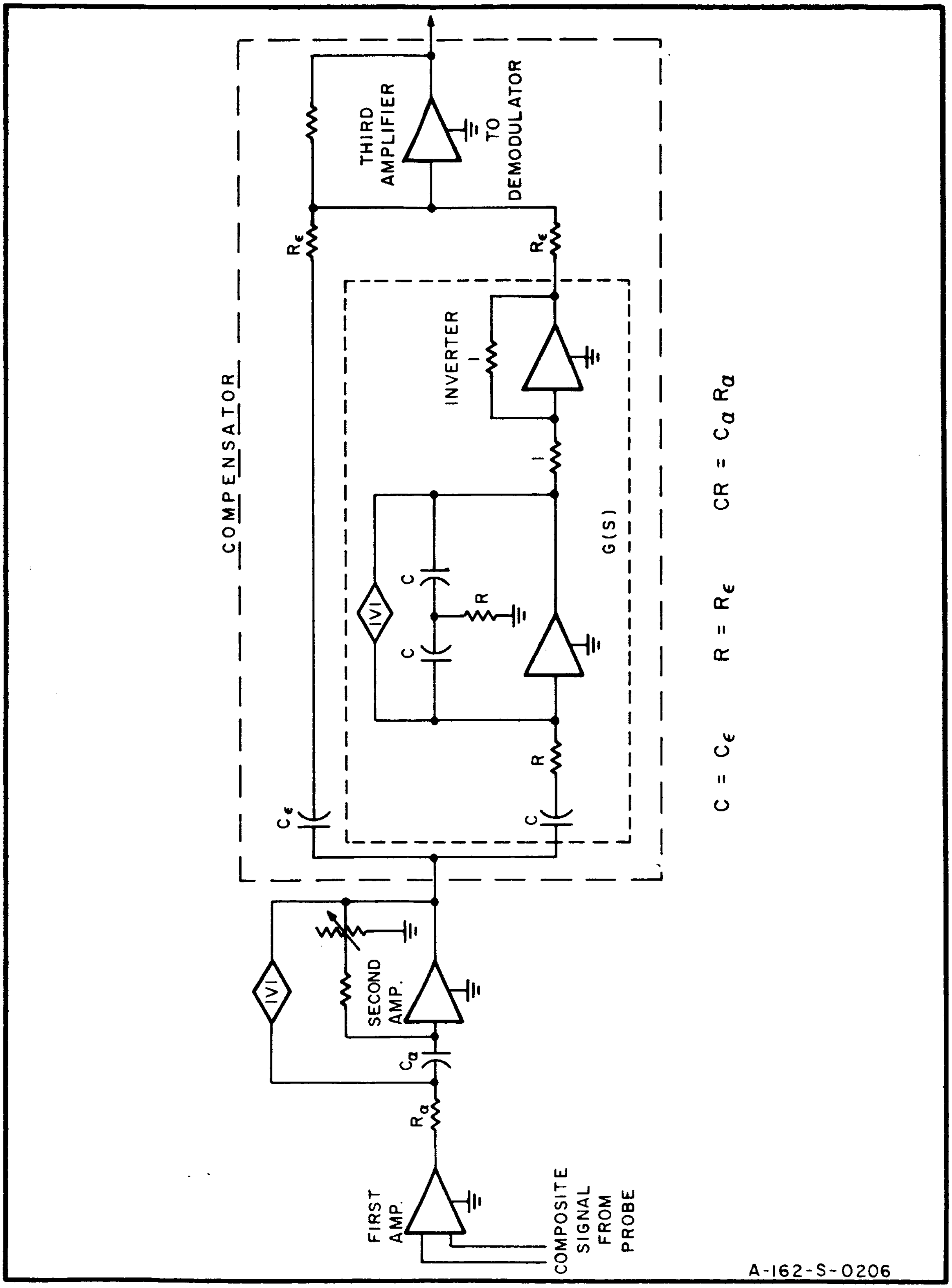
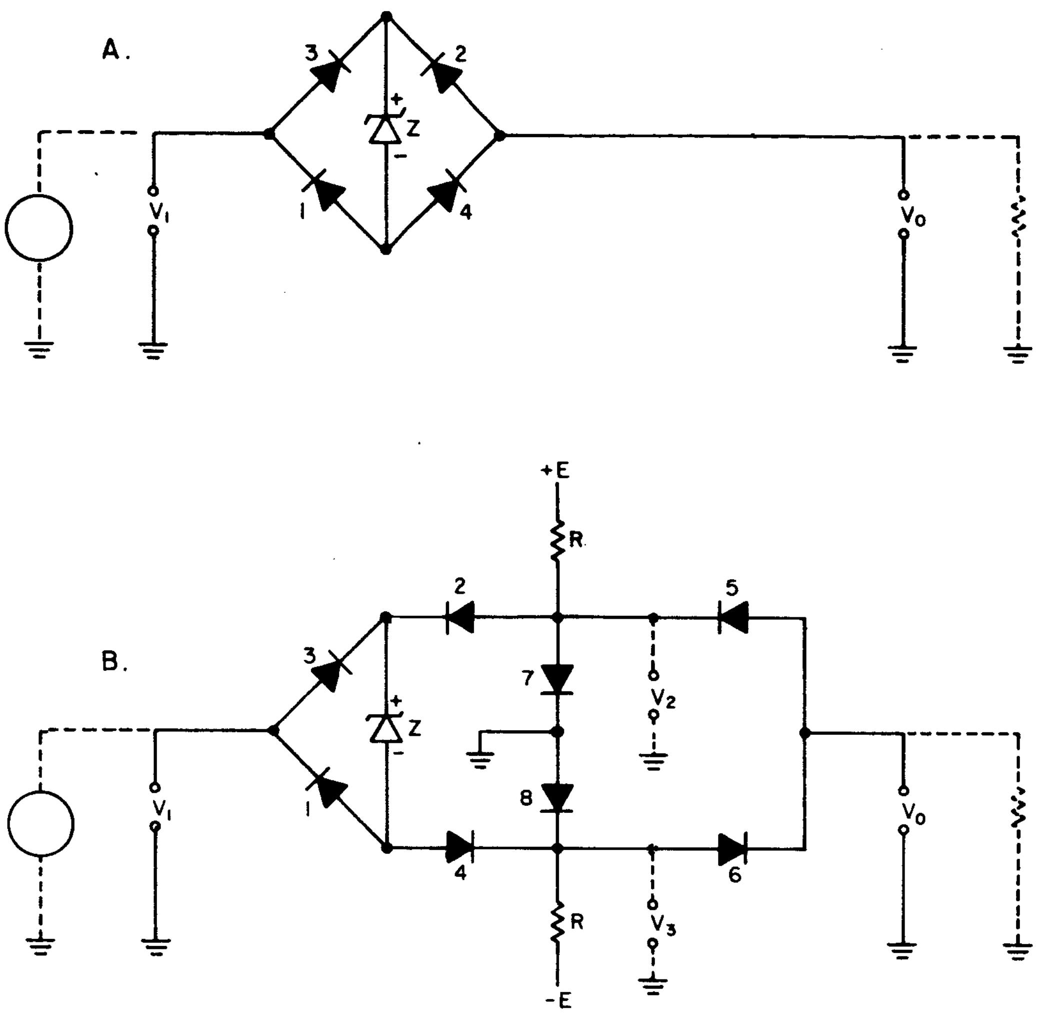


FIG. 10 THE FINAL FORM OF THE FLOWMETER COMPOSITE SIGNAL AMPLIFIER SYSTEM.

amplifier input when the output would otherwise exceed the limit voltage. This prevents saturation of the active elements (transistors) of the amplifier. If saturation is allowed to occur there may be damage to components, excessive time required for recovery and/or oscillatory behavior as a result of network parameters being disturbed. Of course, for this limiter to be effective, the amplifier must be stable under the condition of unity feedback.

A simple voltage bridge is shown in Fig. 11(A). For small input voltages the input and output terminals are isolated except for the reverse leakage and reactance of the Zener diode (and one output diode). Above a certain fixed voltage, determined principally by the Zener diode, the output differs from the input by this voltage. This relationship is described by the table in Fig. 11(B) if V_2 and V_3 are ignored and v_5 and v_6 are considered to be zero. The various v's are actually nonlinear functions of current but for most purposes they may be considered constant, i.e., 0.6 volts for silicon and 0.25 volts for germanium devices in forward conduction.

The circuit of Fig. 11(B) may be used to prevent the diode reverse currents from seriously compromising the precision of an amplifier feedback path. Its mid-range attenuation is very high because it is a ladder configuration in which series and shunt elements are respectively represented by diode reverse leakage and forward conductance. In the case of either A or B in Fig. 11, V_0 will be the amplifier input (or error) voltage and V_1 its output voltage. It is possible for circuit A to be admissible when its output is shunted by a current bridge, to be described next. This may be desirable when the latter is necessary for some other reason.



V_1	V_2	V_3	V_O
$V_1 < -\mathcal{V}_1 - \mathcal{V}_Z - \mathcal{V}_2 - \mathcal{V}_5$	$V_1 + \mathcal{V}_1 + \mathcal{V}_Z + \mathcal{V}_2$	$-\mathcal{V}_8$	$V_1 + \mathcal{V}_1 + \mathcal{V}_Z + \mathcal{V}_2 + \mathcal{V}_5$
$-\mathcal{V}_1 - \mathcal{V}_Z - \mathcal{V}_2 - \mathcal{V}_5 < V_1 < -\mathcal{V}_1 - \mathcal{V}_Z$	$V_1 + \mathcal{V}_1 + \mathcal{V}_Z + \mathcal{V}_2$	$-\mathcal{V}_8$	0
$-\mathcal{V}_1 - \mathcal{V}_Z < V_1 < \mathcal{V}_3 + \mathcal{V}_Z$	$+\mathcal{V}_7$	$-\mathcal{V}_8$	0
$\mathcal{V}_3 + \mathcal{V}_Z < V_1 < \mathcal{V}_3 + \mathcal{V}_Z + \mathcal{V}_4 + \mathcal{V}_6$	$+\mathcal{V}_7$	$V_1 - \mathcal{V}_3 - \mathcal{V}_Z - \mathcal{V}_4$	0
$\mathcal{V}_3 + \mathcal{V}_Z + \mathcal{V}_4 + \mathcal{V}_6 < V_1$	$+\mathcal{V}_7$	$V_1 - \mathcal{V}_3 - \mathcal{V}_Z - \mathcal{V}_4$	$V_1 - \mathcal{V}_3 - \mathcal{V}_Z - \mathcal{V}_4 - \mathcal{V}_6$

NOTES: $\mathcal{V}$ = FORWARD CONDUCTION VOLTAGE OF ORDINARY DIODE.
$\mathcal{V}_Z$ = AVALANCHE VOLTAGE OF ZENER DIODE.
—◇M— IS SYMBOL USED FOR EITHER TYPE.

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FIG. 11 VOLTAGE BRIDGES: A. SIMPLEST TYPE.
B. BRIDGE HAVING HIGH ATTENUATION BELOW CONDUCTION THRESHOLD.

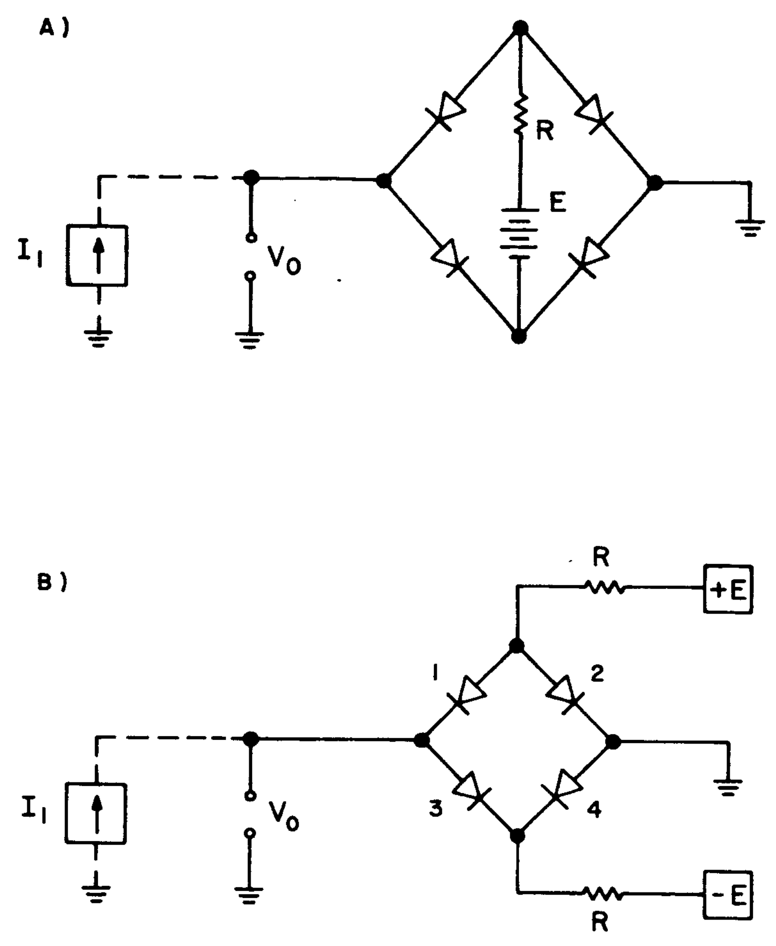
The current bridge, Fig. 12, is effectively a two-terminal device having the property that the voltage between the input and reference (or ground) terminals is very nearly zero until the input current exceeds some fixed amount. If it is capacitively coupled to an amplifier output, it may be used to develop an inhibitory input voltage when the amplifier output voltage rate-of-change (slewing rate) exceeds this current, that is, when

$$\left| C \frac{dV}{dt} \right| > \frac{E}{R} .$$

It is worth noting that the avalanche voltage of a Zener diode is specified only at a given current. This current can be supplied by means of a current bridge on the output of the simplest voltage bridge, or inherently by the circuit of Fig. 11(B). In either case the effective limit voltage will be determined by a Zener diode operating at the current for which the diode voltage was specified by the manufacturer.

The current bridge has another very useful property. A voltage applied to the input terminal will, in effect, cause a current to flow in the ground circuit in a direction determined by the input polarity and of a magnitude determined by the corresponding resistance and effective supply voltage. The current may be established with great precision by making the supply voltage large in comparison with the uncertainty in diode voltage drop.

A current bridge is used to generate a trapezoidal voltage of great precision. The bridge input terminal is connected to a square-wave voltage source and its reference terminal is connected not to ground but to the input terminal



$0 < E$

I_1	V_0
$I_1 < -\frac{E}{R}$	$\left(I_1 + \frac{E}{R}\right) R$
$-\frac{E}{R} < I_1 < \frac{E}{R}$	$-v_1 + v_2 = v_3 - v_4 \simeq 0$
$\frac{E}{R} < I_1$	$\left(I_1 - \frac{E}{R}\right) R$

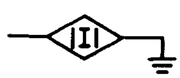
SYMBOL 

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FIG. 12 A. SIMPLE CURRENT BRIDGE.
B. PRACTICAL FORM OF CURRENT BRIDGE.

of an operational amplifier. The amplifier feedback path consists of a parallel combination of a capacitor and two Zener reference diodes oppositely oriented. These diodes not only have an exceedingly small temperature coefficient at the current established by the bridge, but, being composite, do not conduct in the reverse direction. The bridge current and the feedback capacitance precisely determine the trapezoid slope, while the reference diodes determine its upper and lower limits.

The voltage bridge of Fig. 11(B) may be applied as a feedback limiter even in conjunction with amplifiers of large bandwidth; for example, the second amplifier of Fig. 10. Here the bandwidth must be great to hasten the decay of positive tails (Fig. 3), and the composite signal, especially its artifact or spike component, may be very large. But the bridge must be applied carefully in this case for reasons which are easily overlooked.

Let us assume that the amplifier shown in Fig. 13(A) is the second amplifier of the flowmeter, but that its input comes from an unspecified source capable of being inhibited (or limited) by means of a voltage bridge on the amplifier output. Assuming that the amplifier requires negligible signal current, the summing network input and feedback currents may be equated:

$$I = \frac{V_1 - v}{\frac{1}{Cs} + R_1} = \frac{V_0 + v}{R_2} .$$

Now suppose that a spike appears which does not exceed the limit voltage V at the amplifier output. This spike is transmitted through the high-pass network C1, R1, and

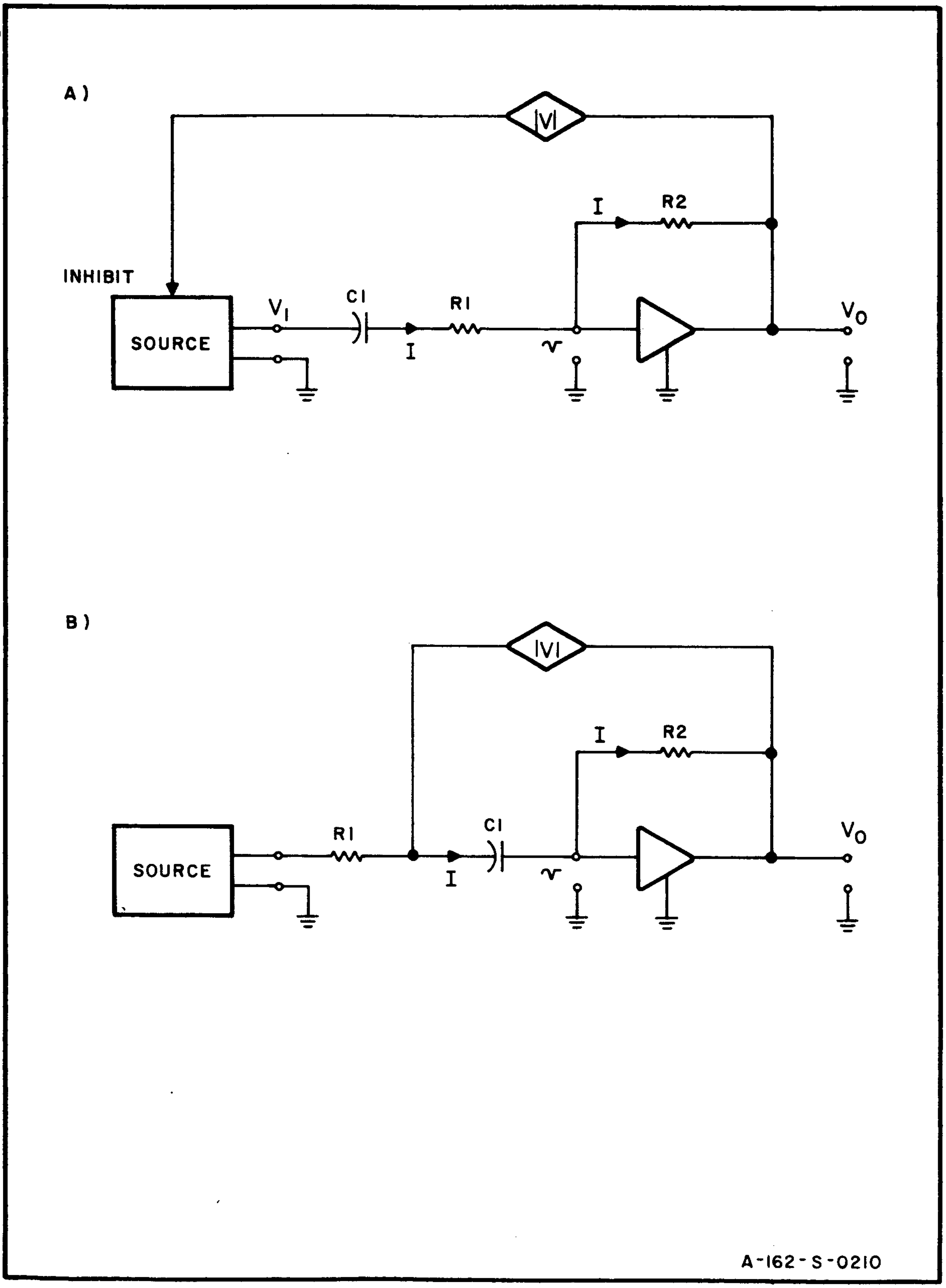


FIG. 13 A. IDEALIZED LIMITER CIRCUIT ENCOMPASSING HIGH-PASS NETWORK.
B. SUCCESSFUL PRACTICAL VERSION OF SAME.

appears at the amplifier output with a tail which results from C1 being charged by the input current. This current is proportional to the amplitude K of the input signal $KV_1(t)$. The output voltage V_o is a linear function of this current. The subsequent compensator networks act upon this voltage to produce another voltage which by addition nullifies the tails. If limiting did take place, the tails would still be nullified. The crucial condition is that for the compensation to be effective V_o must be proportional to the capacitor current. If the voltage bridge were simply connected across R_2, and limiting took place, this condition would not be satisfied. But it is satisfied handily by the circuit of Fig. 13(B). Limiting takes place when the second amplifier output voltage differs from that at the capacitor by the limit voltage V. The capacitor voltage depends upon the offset voltage of the first amplifier (Fig. 10) which in practice remains less than 10 per cent of the maximum output capability of the second amplifier. It is therefore possible to set the limit voltage so that at least 90 per cent of the output voltage capability of the second amplifier is utilized.

3. Demodulators

The demodulator is required to recover the flow signal by inverting and adding the stored average of a sample of the composite signal taken during one half cycle of the flow signal to that taken during the other half cycle. This must be done despite the fact that the alternating signal of interest is superimposed upon low-frequency-noise and spikes which may be one hundred times its maximum possible average amplitude, or one hundred thousand times the smallest quantity that the system must resolve.

Any circuit which will function as a demodulator of the flow signal may be described by appropriate conditions upon the switches of Fig. 14. Circuit IA employs two grounded capacitors which are charged by electronically switching them alternately to the composite-signal source through a series resistor. The demodulated flow signal then appears as the difference between the capacitor voltages, i.e., $V_1 - V_3$. These RC networks tend to average out high frequency noise by acting as low-pass filters. This circuit, though simple and straightforward, is difficult to implement. The voltage sources are charged capacitors. When one is not connected to the signal source it is being discharged at a rate proportional to its terminal voltage which in the worst case will be high and to the conductance of the subsequent circuit. The effect of this discharging is to add to the demodulated flow signal an alternating one which may be of much greater amplitude unless the repetition rate and/or load resistance is made very high, and will not be of zero average value unless the time constants of the two halves of the circuit are equal. Moreover, the subtraction must be performed by inverting one signal and adding the result to the other. But a small error in the gain of the amplifier inverting a large signal will result in an error which is large relative to the difference signal which is sought. The precision required of such an inverting amplifier is probably not attainable.

In circuit IB, the inversion is performed at the input. A smooth response to constant flow is obtainable by addition but not by direct resistive summation (Kirchoff addition), although the feasibility of the latter might seem to follow from the following observations. If two

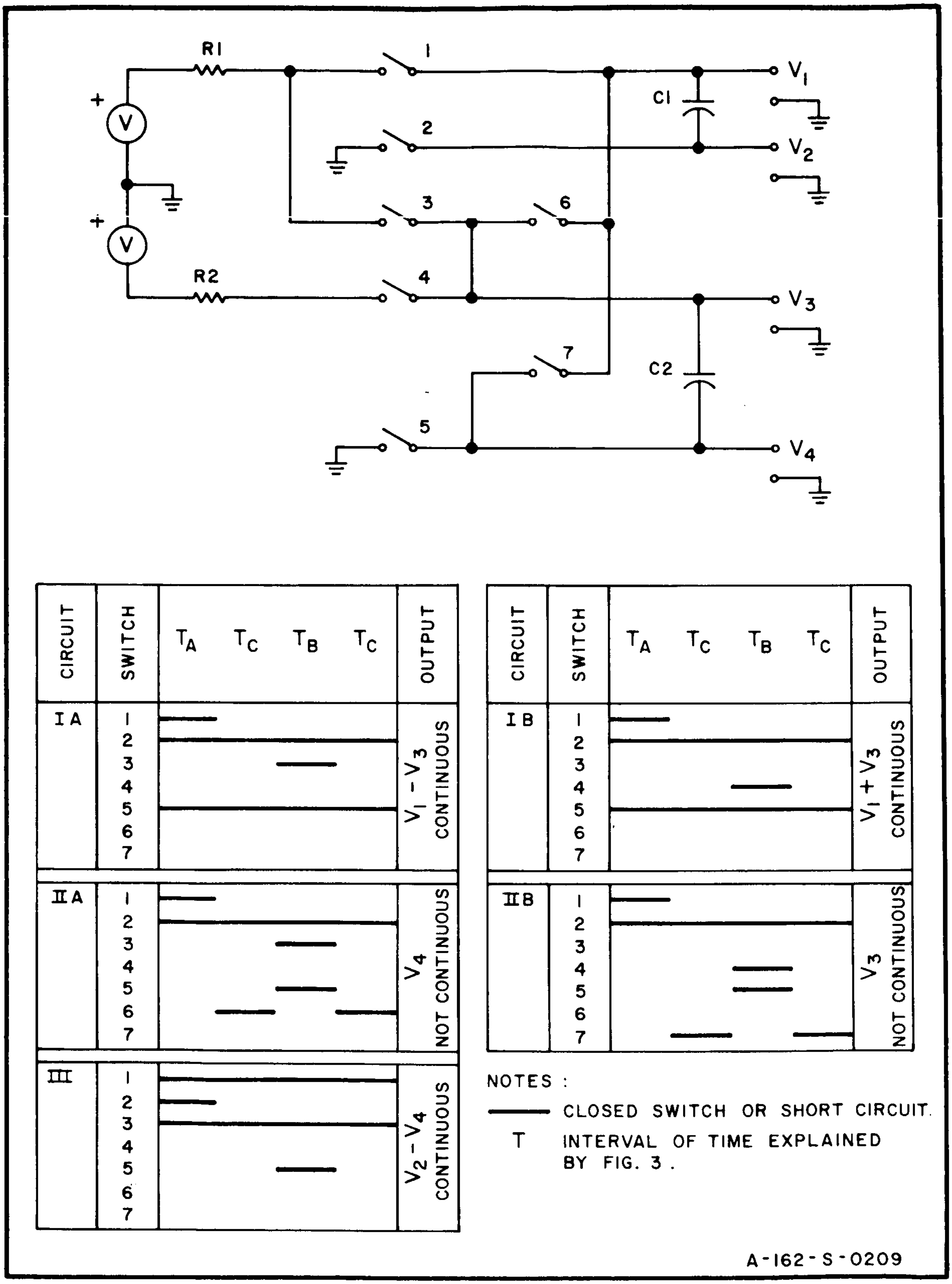


FIG. 14 GENERALIZED DEMODULATOR CIRCUIT .

identical grounded capacitors C1 and C2 having arbitrary terminal voltages are connected by two identical resistors in series, the arithmetical average of the capacitor voltages remains at the junction of the two resistors even though the capacitor voltages are changing as a result of current flow through the resistors. The junction voltage is $(V_{C1} + V_{C2})/2$ because of the simple resistive voltage divider. The changes in capacitor voltages are equal and opposite: each is equal in magnitude to $|1/C_1 \int Idt|$. But in practice, as in the preceeding case, one capacitor voltage decreases in magnitude during the time that the other does not. The same type of AC output component is produced, but a mean value of zero for this may be easier to obtain because of the symmetry of the circuit. However, the problem of precise signal inversion is only slightly less acute before demodulation than it is after.

In circuit IIA each capacitor is charged as before, but the subtraction is performed by joining their upper terminals. At this time the difference voltage appears as V_4. Because it is small and directly proportional to the information sought, extraordinary amplifier gain stability is not required as in the preceeding methods. But the flow information is discontinuous and must be stored. Circuit IIB is included only for completeness.

The remaining circuit III requires subtraction of low-level signals and requires only switches which have one side grounded. This means that the switching may be done by means of low-level switching transistors characterized by low off-set and drift voltages, and that the base current for each of these need not be supplied by a transformer secondary as it would be if the switches were required to be "floating." The disadvantage of this method is that during T_c when both switches are open an immense artifact can appear as a common mode signal. It is not practicable to build a precise differential amplifier having very high input impedance which will reject such a signal. Disconnecting the demodulator from the source during this time by means of a floating switch, would cause the demodulator input to be practically indeterminate (all switches open); short-circuiting the input would introduce a sudden step as great as the DC level there. But limiting the source voltage (and its rate-of-change) to whatever the switches (and isolation amplifiers) can handle by means of feedback from the isolation amplifier outputs to the input of the demodulator driver amplifier is quite practicable.

Figure 15 shows the general form of the demodulator which was adopted after the considerations above. There is shown a driver amplifier, the switched RC network which performs the demodulation, two very high impedance, small-signal, isolation amplifiers, and a feedback system for the limitation of signal voltages and their rates of change.

While one of the switches is closed its associated capacitor and the resistor R constitute a low-pass filter, with the capacitor voltage tending toward the average value of the composite signal E_o. The other capacitor terminal voltage remains fixed at the value acquired during the previous half cycle. Except for the noise components, the difference between these voltages is the analog in magnitude and polarity of the magnitude and direction of flow. In general, there will be a current $(E_o - E_1)/R$ flowing when the switch is opened, at which time each switch voltage E_α, E_β will jump by the identical amount $E_o - E_1$ and then each, offset by a fixed amount, will follow E_o.

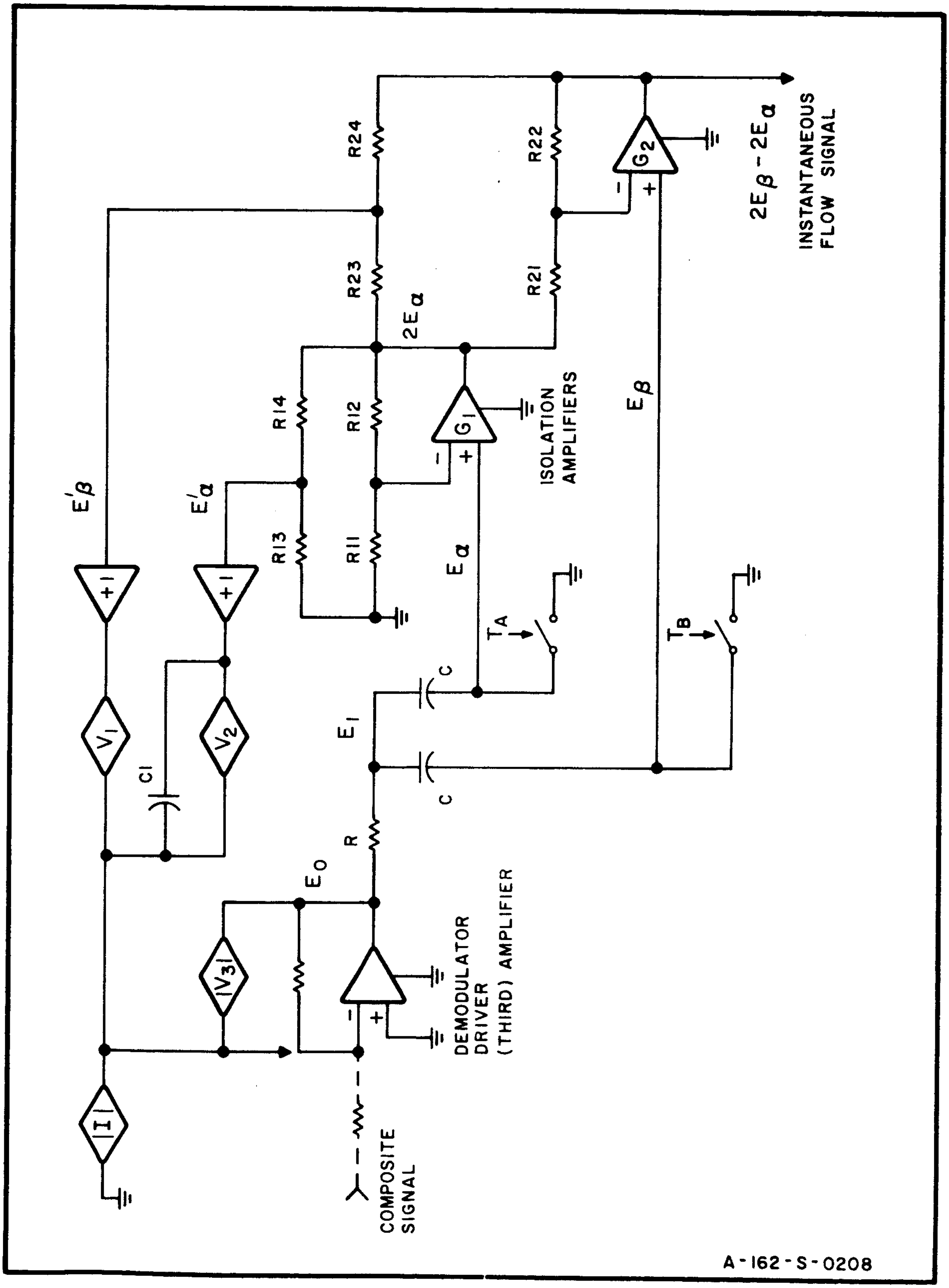


FIG. 15 FORM OF DEMODULATOR WHICH IS MOST PRACTICABLE.

Typically E_o is limited in magnitude by the voltage bridge marked V_3 to about 30 volts, and it can change by almost twice this much if it is near one limit when a spike arrives, while the voltage across the switching transistor must be limited to 5 volts. This can be accomplished by limiters acting upon signals from the isolation amplifiers.

An isolation amplifier circuit consists of a difference amplifier, and, a feedback resistor R_2 and an input resistor R_1 which meet at the amplifier (-) input terminal.

If R_1 is grounded, the overall gain is:

$$\frac{e_o}{e_1} = \frac{R_1 + R_2}{R_1 + \frac{1}{G}(R_1 + R_2)}$$

where e_o is the output voltage and e_1 is the voltage at the (+) input terminal. For equal resistances and sufficiently high internal gain it may be assumed that the signal e_1 is doubled and that a signal applied to R_1 is inverted by the circuit. Hence referring to Fig. 15, E_α appears doubled at the output of the first isolation amplifier and reappears at the junction of R_{13} and R_{14}, which are equal, and at the voltage bridge marked V_2 and the capacitor C1. When the Zener current in V_2 and/or the current in C1 exceeds that in the current bridge ($|I|$), the excess signal at the driver amplifier input is nullified in a manner which will be discussed in Section III-A.2 on the Third Amplifier.

The second isolation amplifier inverts the output of the first and adds to it twice the value of its input E_β

to form the "instantaneous" flow signal. E_β is recovered by means of a summation by equal resistances R_{23} and R_{24} and actuates another limiting circuit when it exceeds V_1. All necessary slew-rate limiting is provided by C1, since this type of limiting is only required when both switches are open and during this time E_α and E_β vary identically.

The demodulator responds to high-frequency noise and flow information in essentially the same manner as a simple low-pass filter. Its response to low-frequency phenomena is quite different. Suppose that the input is a positive-going ramp of very moderate slope beginning during T_A (Fig. 3). The output follows this ramp to the end of T_A and remains constant until the beginning of T_B when it becomes negative-going. It is, therefore, trapezoidal with a peak-to-peak amplitude and average value proportional to the slope of the ramp and to the sampling time. The polarity of the average is positive or negative according to the direction of the ramp. In other words, low frequency noise is acted upon as though by a differentiator followed by a low-pass filter, and it may be decreased by increasing the sampling rate. It may also be decreased by lowering the cut-off frequency of the filter but this would decrease the information bandwidth.

4. <u>Timing</u>

The timing generator produces a periodic unidirectional pulse C of such duration as to straddle the slope time of the trapezoid. The leading edge of C, slightly delayed, triggers a binary which produces a square wave A and its complement A'. Another binary produces a square wave like the first but slightly delayed. One of its outputs causes the trapezoid signal to be generated. One demodulator switch is closed by A inhibited by C, the other by A' inhibited by C. The switch closure times are called T_A and T_B, respectively, and the time when both are open is called T_C. The C pulse ensures, by opening both switches before the (delayed) trapezoid is generated, that there can be no demodulator capacitor current due to the artifact signal.

III. IMPLEMENTATION OF GENERAL-PURPOSE LABORATORY FLOWMETER MODEL B

A. AMPLIFICATION OF COMPOSITE SIGNAL

1. First Amplifier

The pre-amplifier used in the blood flowmeter is a high impedance, direct-coupled unit employing a pair of 2N2586 input transistors (Q1,2) specifically designed for low noise in small signal applications. Its schematic diagram is given in Fig. 16. It is a conventional two stage differential amplifier with push-pull feedback (R18,19,20,21) in which high gain, high gain stability, high input impedance and low noise are obtained as a result of careful attention to circuit details of which no single one is dominant.

An average input stage emitter current of 0.5 ma in each transistor is determined by a precise constant-current source (Q6, R13, 14, 15, 16, 17) in the common emitter circuit. This current is somewhat higher that that which would be optimum if minimum noise were the only consideration, but it provides higher current gain (typically greater than 100) greater bandwidth and better thermal stability, than the optimum current which is approximately 0.3 ma. The noise penalty is roughly 1 db. The precision of the emitter current source, the power supply voltage and the collector load resistances (R4, 10) is sufficient to hold the collector-emitter voltage to about 2.5 volts. This low value eliminates noise contributions by majority carriers distributing the momentum derived from the collector-base

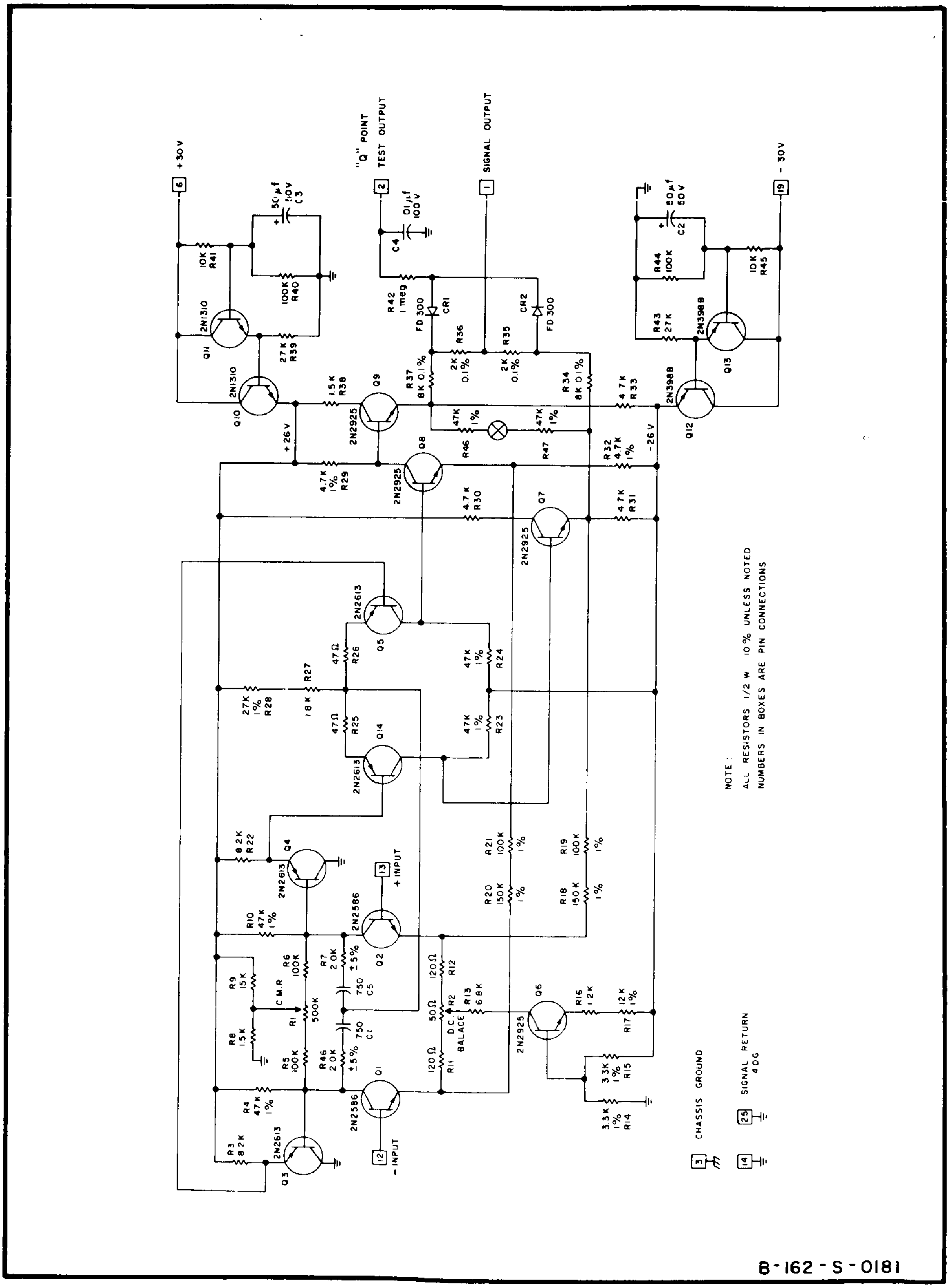


FIG. 16 FIRST AMPLIFIER , CODE 7,2 I

voltage, or more precisely, from the junction gradient, throughout the lattice in the collector region. This effect becomes measureable beyond about 5 volts.

The DC stability is enhanced by the insertion of a small resistance in series with each emitter (R11, 12). These reduce the gain of the difference amplifier, for an input signal source of low internal resistance, from 500 to roughly 120. The differential input impedance is raised from about 5,000 ohms to roughly 20,000 ohms (open loop). Gain variation as a function of the temperature is about 0.03 per cent per degree centigrade with the resistors added, against 0.1 per cent per degree centigrade without them.

A small potentiometer (R2) in the emitter circuit is used to control DC current balance and a variable load (R1, 5, 6) in the collector circuit is used to control relative gain of the input transistors. The latter enables the differential mode response to a common mode signal to be minimized. For this reason it is labeled CMR (Common Mode Reject). Once achieved, it does not disturb DC balance because two resistors (R8, 9) establish at its arm a fixed voltage equal to the average voltage at the collectors.

The output of the first stage is coupled to the second stage by emitter followers (Q3, 4; R3, 22) which provide impedance matching between stages. These maintain the first stage gain while providing the low source impedance necessary for high second stage gain. The emitter followers are 2N2613 low noise PNP germanium transistors. The advantages of their being PNP's are twofold. The type of noise previously described is kept low by the low base-collector voltage which results from simply grounding their collectors. Input impedance is heightened by making full use of the supply voltage and consequent high resistances (R3, 22) in the emitter circuit for a given current. The current actually present is just sufficient for the necessary bandwidth. That the 2N2613 is considerably more noisy than the 2N2586 is of no consequence since the signal levels at this and all subsequent points are more than 100 times larger than those at the amplifier input.

The second stage is a differential amplifier consisting of two 2N2613's (Q5, 14) with local emitter feedback (R25, 26) to raise input impedance and improve gain stability. The emitter resistors were chosen to provide a stage gain of about 180. This is obtained with an operating current of 0.4 ma in each load resistor (R23, 24), hence -7VDC at each collector. A base voltage of +3VDC is fixed by the previous stage. Higher than previous base-collector voltages here are admissible because local noise is relatively insignificant and they are desirable because signal amplitudes are much greater. The average of the collector currents is fixed primarily by the common emitter resistance (R27, 28).

One second-stage (Q14) collector is coupled to feedback (R18, 19) and output (R34, 35) resistors by emitter follower (Q7,R31) having a collector resistor (R30) to limit dissipation. The other second-stage (Q5) collector is similarly coupled to feedback resistors (R20, 21) by emitter follower (Q8, R32) having a collector resistor (R29) identical to that at the emitter. The signal appears inverted at this collector and is coupled to other output resistors (R36, 37) by emitter follower (Q9, R33) also having a collector resistor (R38) to limit dissipation. These three emitter followers employ silicon planar transistors which, despite their low cost, have high current gain. The last two, by virtue of this gain and the large amount of local feedback (degeneration) provided, do not compromise the overall gain stability of this amplifier, even though they are outside the main feedback loop. The main feedback paths are provided by pairs of resistors (R18, 19) (R20, 21) which may be bypassed to ground at the junction of each pair for AC gain measurements, while stable operating conditions are maintained by the remaining low frequency feedback.

The equivalent circuit for the amplifier output is a generator, producing a voltage equal to one-half of the sum of the voltage at one second stage collector and that at the other half after inversion, and a series resistor having a resistance equal to that of the parallel combination of output resistors. The precision of these resistors must be very high. They constitute part of the input network for the subsequent (Second) feedback amplifier. The four output resistors (R34, 35, 36, 37) constitute a divider between one output transistor (Q7) emitter which is at -8VDC and the other (Q9) which is at +8VDC. They provide taps which back-bias two diodes (CR1, 2) which are joined at a series resistor (R42). The resistor is bypassed by a capacitor (C4) to prevent noise or coherent signals from entering the First Amplifier box and may be switched to a voltmeter which returns to ground. For this test the amplifier input terminals are grounded by the switch. The voltmeter will read zero unless the amplifier output "Q" (quiescent) voltage has drifted more than a couple of volts off zero. Another resistive divider (R46, 47) provides an independent output at a tip-jack for monitoring purposes.

The open loop frequency response of the amplifier has a single negative slope from five to one hundred KC as a result of a series RC circuit (C1, R46) (C5, R7) shunting each first stage collector and from one hundred KC on as a result of stray capacitance at the output of the second stage. It was found that the behavior of first-stage inter-collector networks is not predictable unless they are symmetrical and their center point is joined to the common emitter point of the following stage. The closed loop frequency response is flat to about 400 KC and its step response exhibits no overshoot. Details of the frequency response are shown in Fig. 17. The closed loop gain is 800.

The long term peak-to-peak noise is 6 MV or 1 MV rms. This is equivalent to 1.3 μv referred to the input or less than 0.1 μv/100 cps. If we assume a low frequency noise corner at about 1.5 kc and a low frequency noise slope between 3 db and 6 db per octave, the resultant midband noise may be estimated at 0.7 μv/100 cps or less.

Common mode input impedance (closed loop) is greater than 1 megohm at 500 cps and the differential mode input impedance under the same conditions is about 1 megohm, i.e., 500,000 ohms each side to ground. Common mode rejection with no source resistance imbalance is at least 117 db. The common mode rejection with 1000-ohm source imbalance is 87 db at 500 cps and 67 db at 5,000 cps.

It is estimated that closed-loop gain will remain fixed within about 0.25 per cent for a 40° change in ambient temperature, neglecting the temperature coefficients of the feedback resistors. Long term drift is primarily determined by resistor stability and should be negligible.

Electronic filters, one (Q10, 11; R39, 40, 41; C3) in the positive and another (Q12, 13; R43, 44, 45; C2) in the negative power supply lines are necessary to suppress

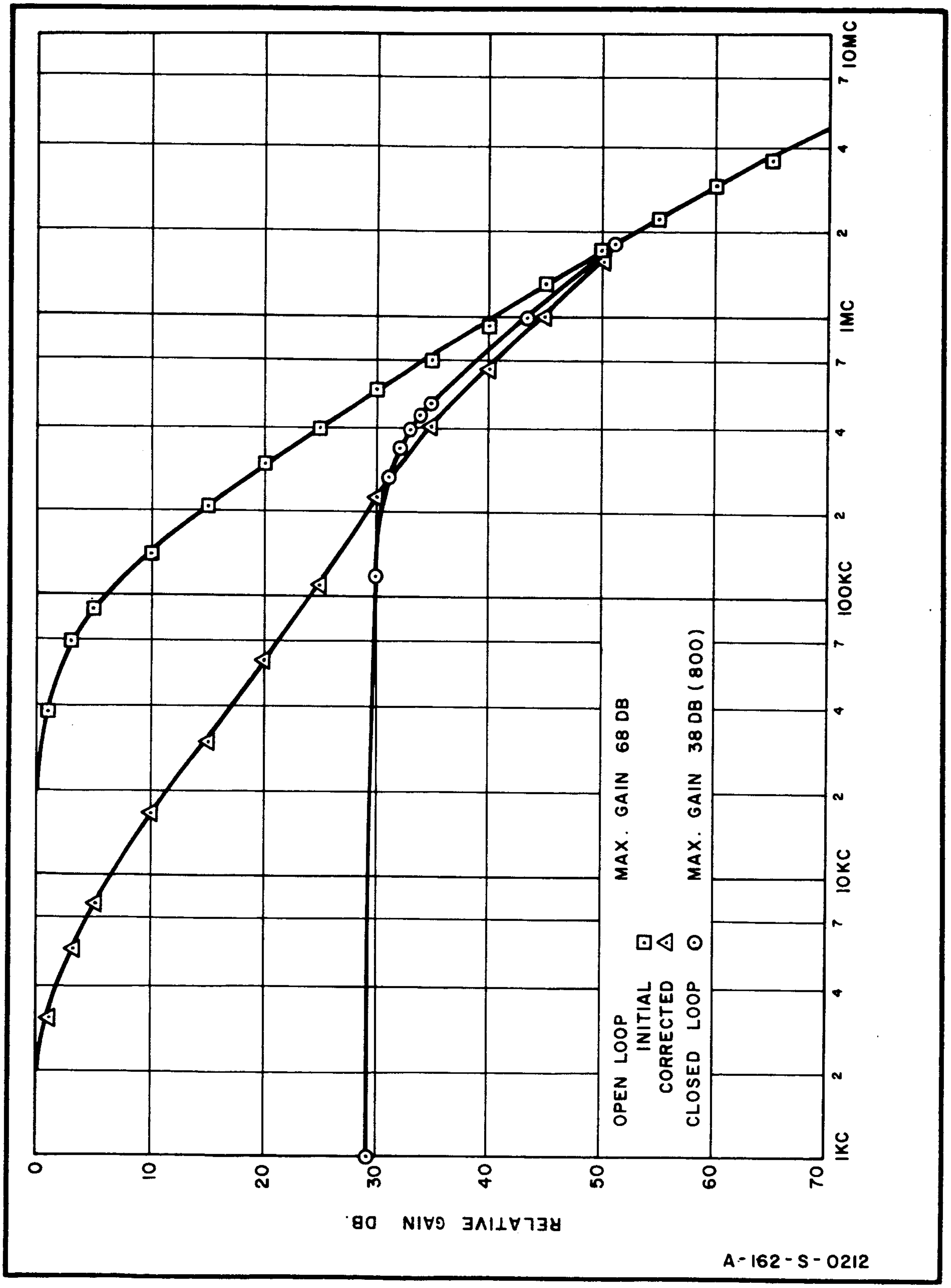


FIG. 17 FIRST AMPLIFIER FREQUENCY RESPONSE.

errors in indicated flow due to coherent ripple. The four-volt drop from 30 to 26 volts is just sufficient for proper operation of the cascade emitter followers in each filter.

2. <u>The Second and Third Amplifiers</u>

The Second and Third Amplifier schematic diagrams are given in Figs. 18 and 19. The descriptions which follow pertain to either amplifier unless one is specified.

The amplifier begins with two transistors (Q1, 2) in a differential configuration. Each has a series emitter resistance (R8, 9) to raise its input impedance and to improve its DC stability. From the junction of these two resistors to the -60 V supply there are two resistors (R10, 11) in series. One of these (R11) is normally of much less resistance than the other, and by its proper choice the current in this circuit may be set precisely.

Differential changes in first stage collector voltages may be introduced by means of a potentiometer (R1) in the collector load (R2, 5) circuit. By this means the quiescent value of the amplifier output voltage may be set to zero during open-loop tests. The collectors are coupled to the second stage by two emitter followers (Q3, 4), and coupling capacitors (C2, 6) each bridged by a Zener diode (CR1, 2) with a resistor (R7, 17) in series. By the proper choice of these resistors the voltage drop across the capacitor may be set very close to 55 volts, even though the 50-volt Zener has a 10 per cent tolerance. These resistors serve another purpose. They act in conjunction with their capacitors as a low pass filter to suppress noise generated in the Zener diodes. The common current for the emitter followers and the Zener diodes comes from resistors (R19, 23) connected to the negative 60-volt supply. The collector

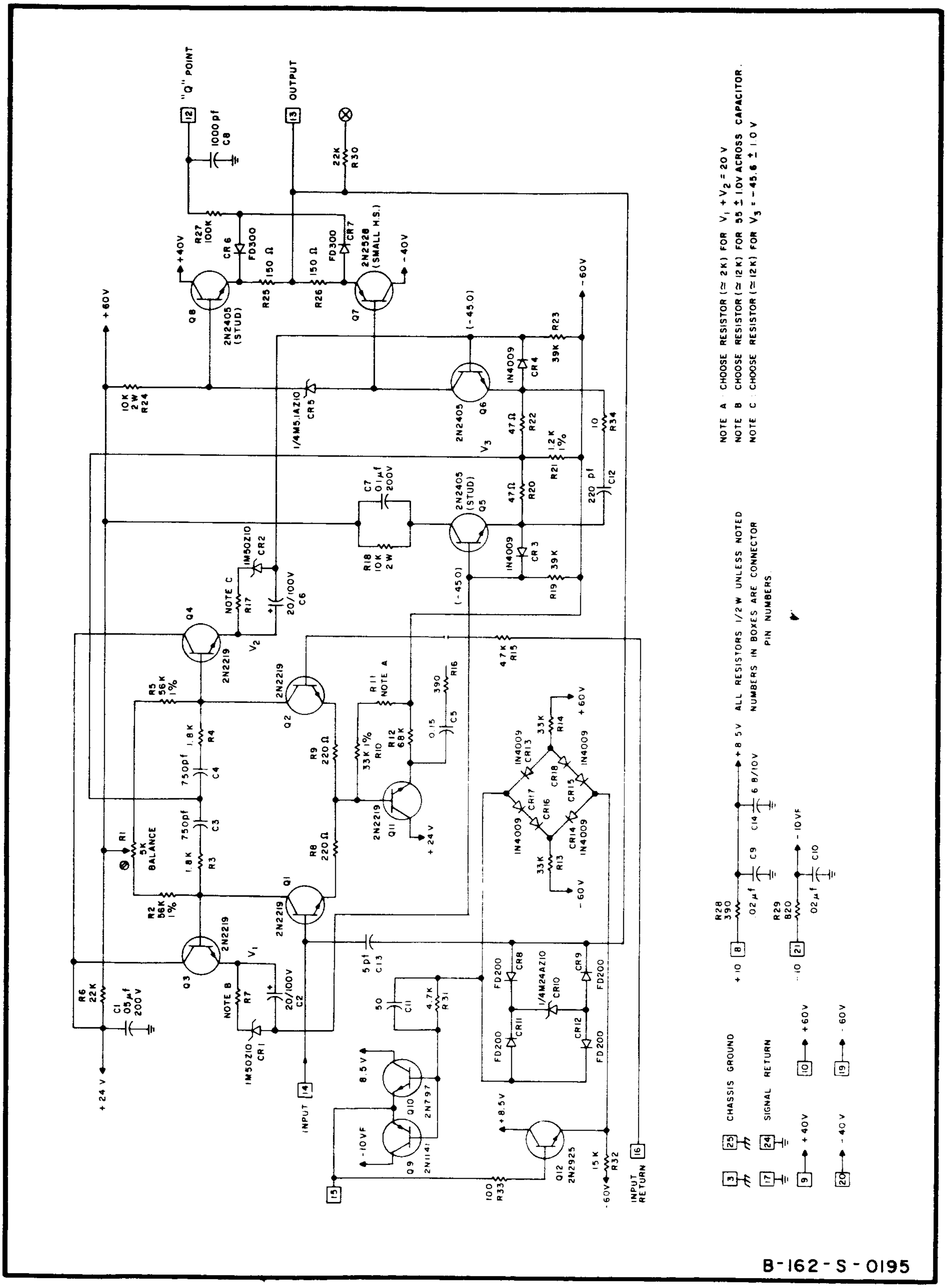


FIG. 18 SECOND AMPLIFIER , CODE 3,4 K

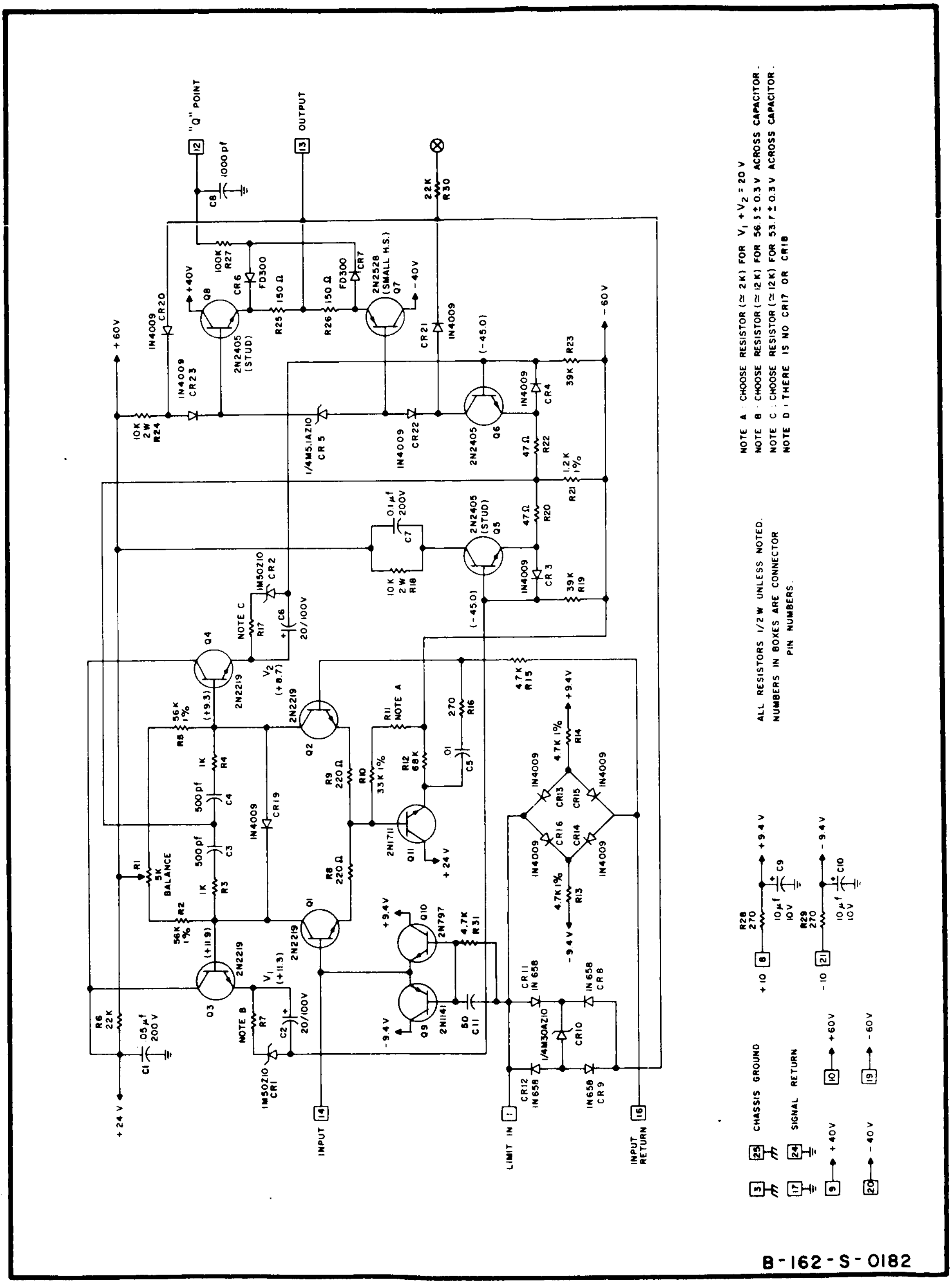


FIG. 19 THIRD AMPLIFIER, CODE 3,6 D

voltage (24 VDC) for these and one other emitter follower used for frequency response correction is supplied by series resistor (R6) and shunt capacitor (C1) from the +60 V regulated supply. The four type 2N2219 transistors used in the circuits described above were chosen for their large gain-bandwidth product and low parasitic capacitance. Those in subsequent circuits were chosen for their higher voltage and/or power rating.

The second stage is also a voltage amplifier employing two 2N2405 transistors (Q5, 6) having their base-emitter junctions protected by shunting diodes (CR 3, 4) because of the high voltages and large capacitances in the associated circuits. The individual emitter resistors (R 20, 22), which are employed for the same reasons as those in the first stage, join a common emitter resistor (R 21) - which must be of good precision - connected to the negative supply. Precision is important here because the voltage drop across this resistor is small compared to that across the collector loads (R 18, 24), and therefore a small change in emitter resistance will result in a large change in collector voltage. The notes in Figs. 18 and 19 describe how the proper quiescent conditions may be set up. When this is done properly, both second stage collector voltages will be near zero. The amplifier output voltage is taken from just one of them (Q 6); the other is simply bypassed. Since the differential input signal ensures that the sum of the signal currents at the collectors will be near zero it is proper for the bypass capacitor (C7) to return to the positive collector power supply. The Zener diode (CR5) in series with the output collector provides two output voltages which differ by 5.1 volts. The more positive of these is connected to the base of an NPN transistor (Q8) having a positive collector supply voltage, while the more negative is connected to the base of a PNP transistor (Q7) having a negative collector supply voltage. The emitters are joined by two 150 ohm resistors (R25, 26) in series through which a quiescent current of 13 ma flows. The junction of these two resistors is the output terminal. Their voltage drops are used to back-bias two diodes (CR6, 7) in a circuit (R27, C8) used to sense the quiescent output voltage as in the First Amplifier. The complementary emitter followers provide an output circuit of low idling current yet high signal output current and voltage capability. A test jack connected to the output through a resistor (R30) is provided for monitoring purposes.

Output voltage is limited by an overall internal feedback path, that is, a voltage bridge (CR8, 9, 10, 11, 12) of a type which is described in conjunction with Fig. 11(A), shunted by a current bridge (CR13, 14, 15, 16; R13, 14) which is described with Fig. 12(B).

The Second Amplifier current bridge is not connected to ground. Rather it is made to follow the voltage at another point $\boxed{15}$ by means of an emitter follower (Q12; R32, 33). This point is analogous to the junction of R1 and C1 in Fig. 13(B). The additional diodes in the current bridge (CR17, 18) of Fig. 18 are used to cancel the junction drop in the emitter-follower (Q12) which drives it, thus producing a voltage at the top of the bridge which is nearly identical to that at the base of its driver.

The complementary emitter followers (Q9, 10; C11; R31) do not conduct because their base-emitter voltages are nearly zero, unless the feedback current through the Zener diode (CR10) exceeds that of the current bridge. When this happens they supply that current to the input necessary to inhibit any further increase in output voltage. They are protected against possible excessive current in their base-collector junctions from the amplifier output through the voltage bridge by a resistor (R31) which is bypassed by a capacitor (C11) at high frequencies. The low-voltage sources for these followers are decoupled (R28, 29; C9, 10,(14)) to isolate the amplifier input from power-supply noise voltages.

The Second Amplifier inhibitory feedback current does not interfere with the restoration of the signal in the Compensator which follows. It is fed back to the point $\boxed{15}$, mentioned above, for reasons which are discussed in connection with Fig. 13(B).

The Third Amplifier has its output current limited to about 40 ma for the protection of its output emitter-followers and subsequent circuits.* It is limited in the positive direction to

$$(V_{CR21} + V_{CR22} + V_{CR5} - V_{BE8})/\ R_{25} + (I_{R24})$$

and in the negative direction to

$$(V_{CR20} + V_{CR23} + V_{CR5} - V_{BE7})/\ R_{26} + (I_{CE6} - I_{R24})$$

where any V is the voltage drop in a junction designated CR for diode or BE for base-emitter followed by the diode or transistor number. The output transistor (Q6) of the second stage may contribute excessive collector-emitter

* The Demodulator may be switched (see Fig. 30, S1n) from ground, to Third Amplifier, to precision potentiometer (R79), by means of switch contacts which must make-before-break to prevent interruption of flow information. The potentiometer and the Demodulator low-level choppers both need protection.

current I_{CE6} to the amplifier output because of the low value of its emitter resistance (R21, 22) unless its base voltage is limited in the positive direction. This limiting is accomplished by means of a diode (CR 19) between the first-stage collectors. If the circuits are adjusted as described in the Notes of Fig. 19, the diode will limit effectively, but will not interfere with normal signals.

The problem of adequately tailoring the frequency response of the Second and Third Amplifiers is especially difficult because: (1) the tails which result from very large spike inputs must be exceedingly brief and/or very minute lest they cause significant errors in indicated flow, (2) the feedback factor of the Second Amplifier is subject to change over a 20-db range,by means of switches,to accommodate probes of different gains, which implies careful control of open-loop phase and gain over a wide range, and (3) it is not sufficient to tailor the amplifier phase and gain characteristics, however carefully, to prevent tails, because the very networks which do this may cause saturation of active elements and severe distortion by limiting the possible rate-of-change of the amplifier to a value less than that required to reproduce the spike. Such limiting has the following explanation.

At some point in the amplifier there will be a collector (or emitter) load resistance R connected to some maximum available power supply voltage E_B. A signal of some amplitude E_S will be required to change by ΔE_S in a certain time Δt. But the point is shunted by a capacitance C (with possibly a low resistance in series) to shape properly the high frequency loop gain and phase. It follows that unless:

$$\frac{\Delta E_S}{\Delta t} \leq \frac{E_B - E_S}{RC} = \frac{I}{C}$$

the transistor (or other active element) will be cut off and the amplifier will be nonlinear. It does not help to increase the available current I by decreasing R, for then it would be necessary to increase C to obtain the same frequency response. Two things can be done: decrease E_S and ΔE_S by moving the network to an earlier stage or change the network, but general RC networks give rise to similar problems and inductors are generally not feasible.

The necessary voltage rates-of-change were obtained in the Second and Third Amplifiers by placing the two required lag networks in the first stage. One (C3, 4; R3, 4) in the collector circuit is conventional except perhaps for its being symmetrical and its center point being connected to the common emitter point of the next stage. Only with such a connection was the high-frequency behavior of the amplifier predictable. The other network consists of an emitter follower (Q11; R12) which couples, through a high-pass network (C5; R15, 16), the input stage (Q1, 2) common emitter (R8, 9, 10) signal to that input (Q2) base which is not the amplifier summing junction. At low frequencies the maximum possible stage gain is realized because this base is neutral. As frequency increases, a greater proportion of the input base signal appears at its emitter return (R8, 9), thereby decreasing the signal current in the input stage. The high common emitter resistance (R10, 11) ensures that the sum of the stage collector currents remains near zero. Therefore the stage still functions as a good phase splitter. The stage gain decreases by subtraction of effective input signal rather than by the process of shunting the path of the signal after amplification. Signal voltage amplitudes approaching the quiescent collector-emitter voltage would be required to saturate the stage. The reason the input stage signal could not be made to decrease specifically with frequency by the simplest of all means, a shunt network at the input summing junction, is that in this application the equivalent resistance to ground at this point is not a constant determined by the summing resistances. When feedback limiting occurs it drops practically to zero.

The open and closed loop frequency response data for the Second and Third Amplifiers are given in Figs. 20 and 21. The networks were designed to maximize the closed loop bandwidth at the required gain without introducing overshoots. Because the required Second Amplifier gain must cover a 20-db range*, its open loop frequency characteristic was further refined by an RC lead network (C12, R34) between the second stage collectors which takes effect above 8 megacycles and another (C13) in the feedback path.

3. The Compensator

The correspondence between the basic amplifier-compensator circuit of Fig. 10 and that of Model B Flowmeter is as follows:

Basic Circuit Fig. 10	Flowmeter	
	Figure	Components
R_α	16	R34,35,36,37
Third Amplifier	19	All
Input Resistor R_ϵ (AC)	30	R96
Input Resistor R_ϵ (DC)		R95
Feedback Resistor	-	R94
Second Amplifier Feedback Network	-	R1-66,74

* See Section III-D.1, for reference to Second Amplifier feedback attenuator.

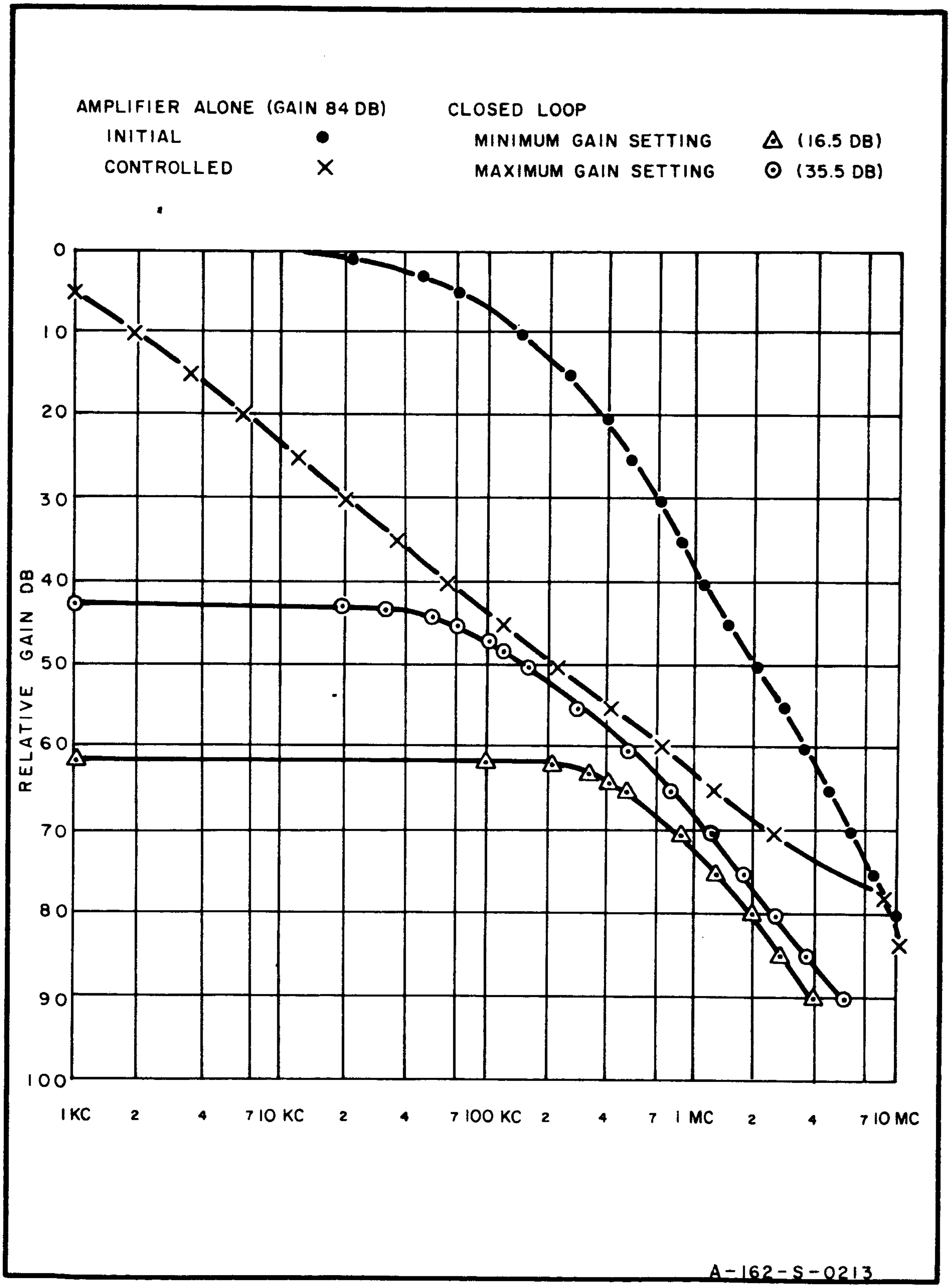


FIG. 20 SECOND AMPLIFIER FREQUENCY RESPONSE

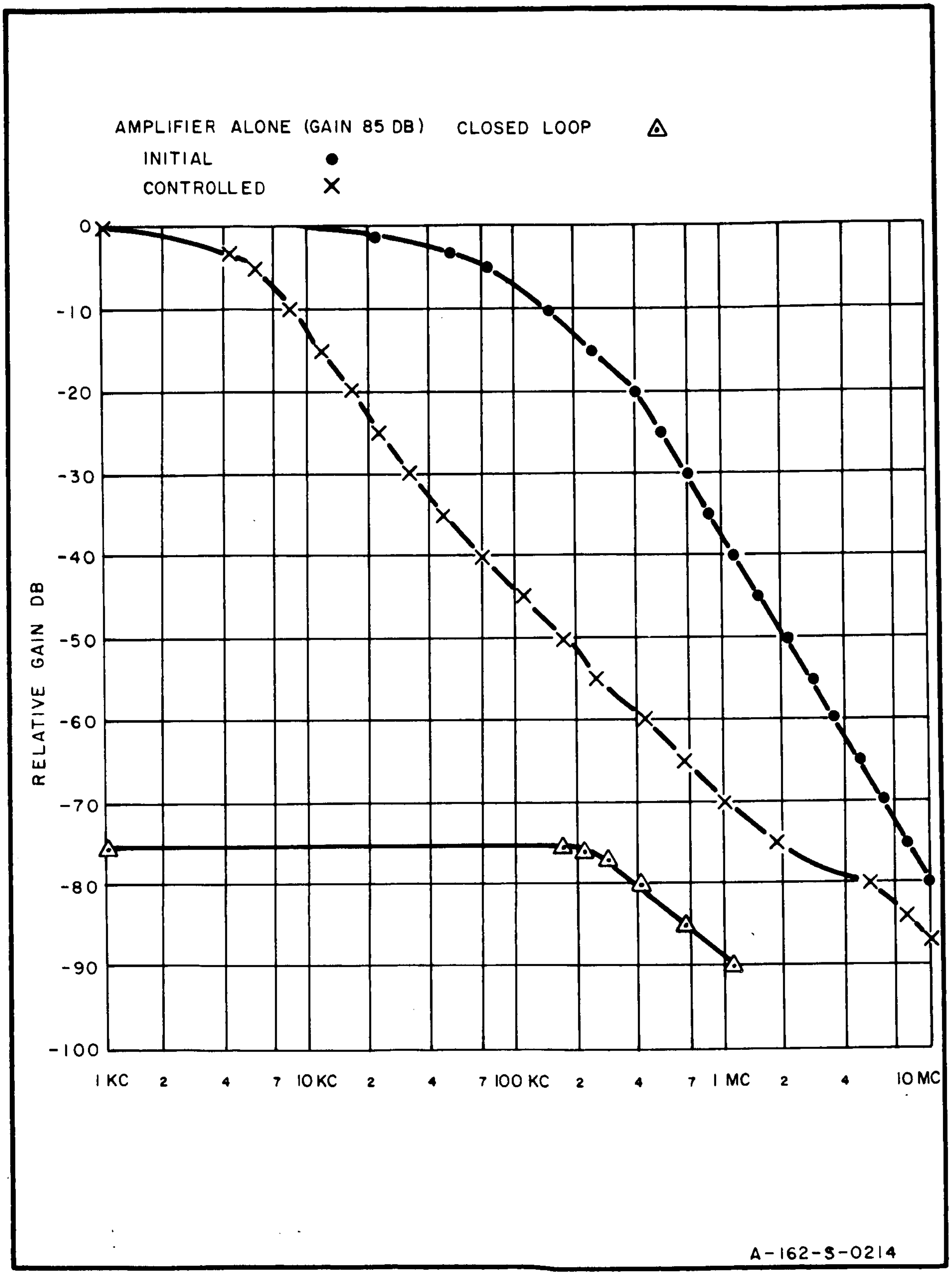


FIG. 21 THIRD AMPLIFIER FREQUENCY RESPONSE

Basic Circuit Fig. 10 (Cont'd.)

C_α	22	C4
C_ϵ	-	C7
C,R Input	-	C3, R5
C,R Feedback	-	C1,2;R13
Inverter Input Resistor	-	R20
Feedback Resistor	-	R22
Voltage Bridge	-	CR1,2,3,4,6,7,9,10;R9,10 (see Fig. 11B)

The actual Third Amplifier and its summing resistors are external to the box marked Compensator which is described by Fig. 22.

The capacitors of high precision (C1,2,3,4,7) required for signal coupling and compensation are made up of 2.0 μf ±1.0 per cent units brought up to 2.02 μf ±0.1 per cent by means of additional capacitors where necessary. Those two (C1,2) comprising part of an amplifier feedback network are shunted by 10-megohm resistors (R11,12) so that the settling time will be reasonable whenever it is necessary to adjust the DRIFT control (R1). The shunt resistance is too high to compromise the desired network behavior noticeably. Drift is cancelled by setting the amplifier output voltage close to zero. The control circuit (R1,3,4) provides a lesser range but higher resolution than that recommended by the amplifier manufacturer.

The Amplifier is a Fairchild type A00-4 described in Appendix A. It is connected to a complimentary emitter-follower (CR12; Q1,2; R6,7,8) necessary to supply a feedback current equal to the maximum possible input current. This current is the maximum peak-to-peak output voltage of the Second Amplifier divided by R_5. The follower must also supply the inverter input resistor (R20) current and the voltage bridge (CR1,2,3,4,6,7,9,10; R9,10) clamping current.

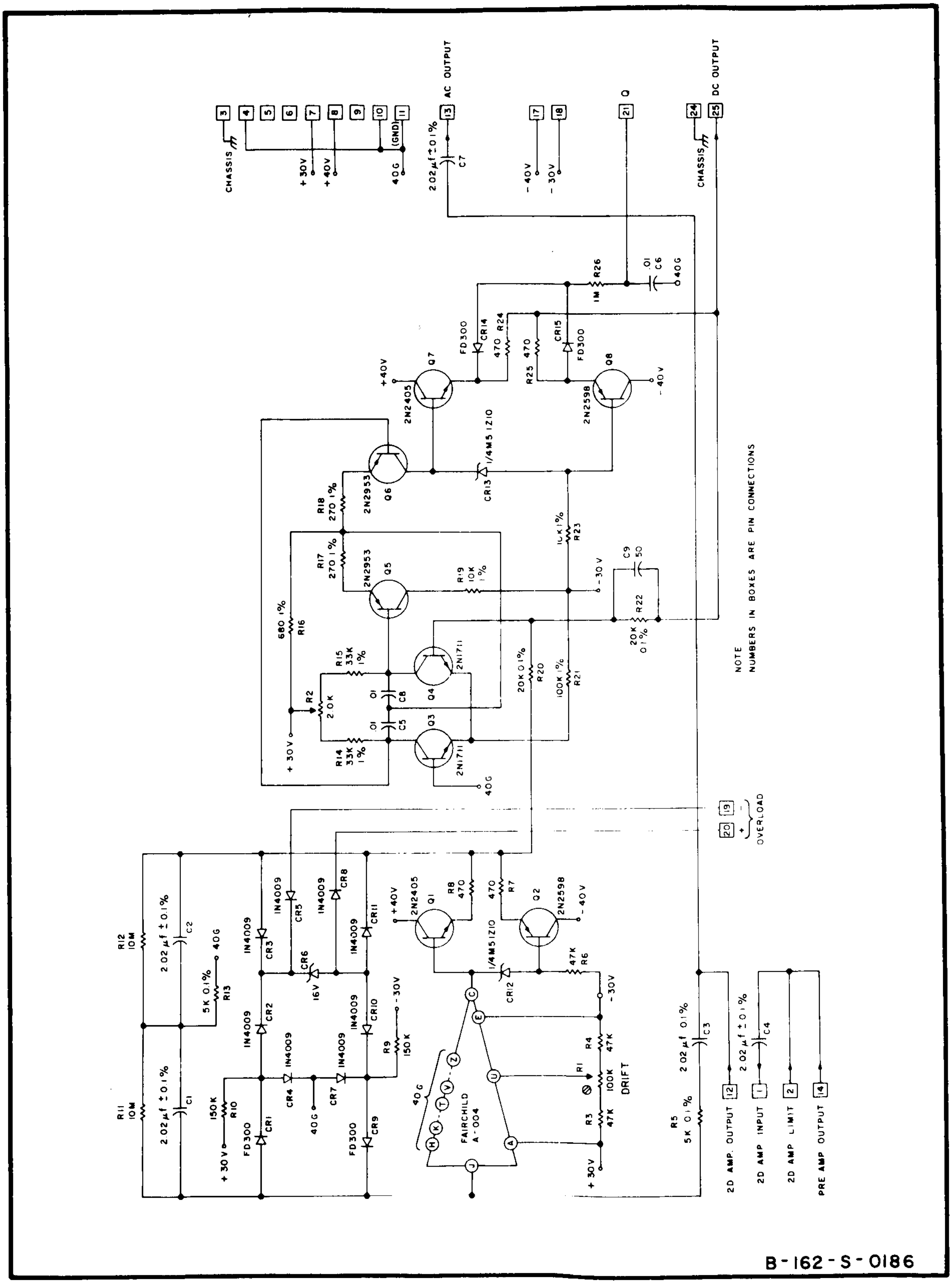


FIG. 22 COMPENSATOR , CODE 9,4 J

The bridge is like that of Fig. 11(B). The FD 300 diodes (CR 1,9) connected to the amplifier input were chosen for their exceedingly low leakage. Two diodes (CR 5,8) connect the voltage bridge to an overload indicator, described in Sec. III-D.1, which flashes a light when this or any similar amplifier is within about one half volt of being limited.

The inverter amplifier consists of an NPN differential input stage (Q 3,4) with a total input current of 0.3 ma established by a common emitter resistor (R 21). The amplifier output may be zeroed during open-loop tests by means of a potentiometer (R 2) which introduces a differential collector load (R 2,14,15) across which there is an average drop of 5 volts.

The direct coupled PNP stage (Q 5,6) which follows has individual emitter resistors (R 17,18) to raise input resistance and improve DC stability. Its average current is fixed principally by that of the first stage and by the second-stage common emitter resistor (R 16). The precision of the resistors mentioned above and the collector loads (R 19,23) ensure that the zero signal collector voltages will be near zero. A Zener diode (CR 13) in series with one collector provides the difference voltage necessary to maintain an idling current of 4.5 ma in the amplifier complimentary emitter-follower output circuit (Q 7,8; R 24,25) and back bias for the output voltage threshold circuit (CR 14,15; R 26; C 6) used in conjunction with an external voltmeter to sense when the inverter output quiescent (Q) voltage is more than a couple of volts off zero. Since by virtue of the input (R 20) and feedback (R 22) resistors this output is normally the precise negative - except for its own offset voltage - of the preceding amplifier output, the Q test serves to check both amplifiers. No special precautions are necessary to make this offset negligible in effect.

The measured maximum open-loop gain of the inverter amplifier is 63 db minus 6 db for the feedback network. Since very little bandwidth is required in this circuit a single corner was introduced at 1 KC by means of symmetrical first stage inter-collector capacitance (C 5,8) with the center point returned to the common emitter point of the second stage. A feedback capacitor (C 9) is necessitated by the high summing network resistance and parasitic capacitance at the input transistor (Q 4). With the value chosen there are no overshoots in either frequency or time response, and the bandwidth is much greater than is necessary. The detailed frequency response curves are given in Fig. 23.

B. TIMING AND DEMODULATING

1. Time-Logic Generator

The repetition rate of the flowmeter processes may be changed without affecting the precision of the signal amplifying or demodulating circuits. Raising the rate will reduce the effect of low frequency noise, as pointed out in Section II-C.3, and will raise the information bandwidth but it will reduce the time (T_A or T_B) per half cycle (see flow signals, Fig. 3) during which information is being received. The least possible interval between information samples is fixed by the probe magnet: its inductance, its required current (which must be reversed) and its maximum allowable voltage. The nominal value of this interval in practice is 100 microseconds. The optimum repetition rate in any case will surely lie somewhere in the frequency range provided, 200 to 1000 cps.

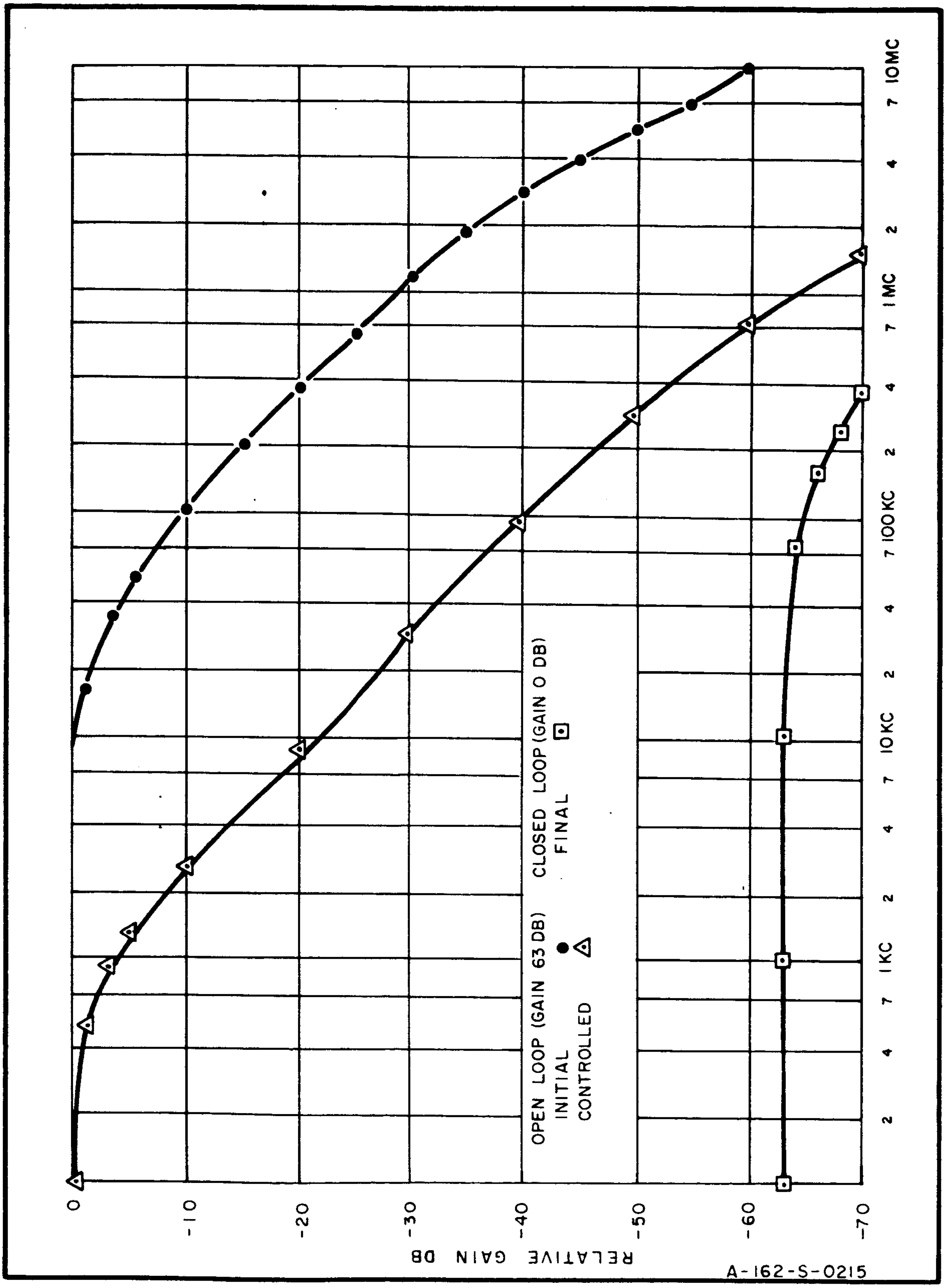


FIG. 23 INVERTER FREQUENCY RESPONSE

The timing schedule outlined in Section II-C.4 is carried out by the circuits of Fig. 24. The repetition rate is determined by a relaxation type oscillator. A capacitor (C 17) is charged through an adjustable resistor (R 1,48) marked FREQUENCY and when its voltage reaches a critical proportion of the supply voltage (+10 VDC) it is discharged by current from the emitter of the N-type unijunction transistor (Q 15) to which it is connected. A resistor (R 47) in series with base B2 is commonly employed to provide compensation for temperature induced frequency variations. Positive pulses across the base B1 resistor (R 54) drive the base of a grounded-emitter amplifier (Q 16; R 35) into conduction through an isolating resistor (R 52). The resulting negative pulse coupled by capacitor (C 12) to a diode (CR 17) back biased by a divider (R 36,53) triggers a monostable multivibrator (Q 17,18; R 37,38,39,46,55; C 13,14) which produces the positive "C" pulse across one collector load (R39) of a width which, in conjunction with the regulated supply voltage, is set by the RC charging circuit (C 13, R 38) to about 120 microseconds. At the other collector load (R 37) a negative pulse is formed which begins discharging a capacitor (C 16) through a resistor (R 40). The capacitor is connected to the input base of a two-transistor regenerative comparator (Q 19,20; R 41,42,49,57,58; C 9) which after about 5 microseconds causes the current in the common emitter resistor (R 58) to be transferred from the first transistor to the second, causing a negative pulse at the second collector, which, coupled by capacitance (C 15) to diodes (CR 18,19) back biased by a portion of the (10V DC) supply voltage determined by two resistors (R 43,56), triggers a bistable multivibrator (Q 21,22; R 44,45,50,51,59,60; C 10,11). The multi produces at its collectors the complementary square

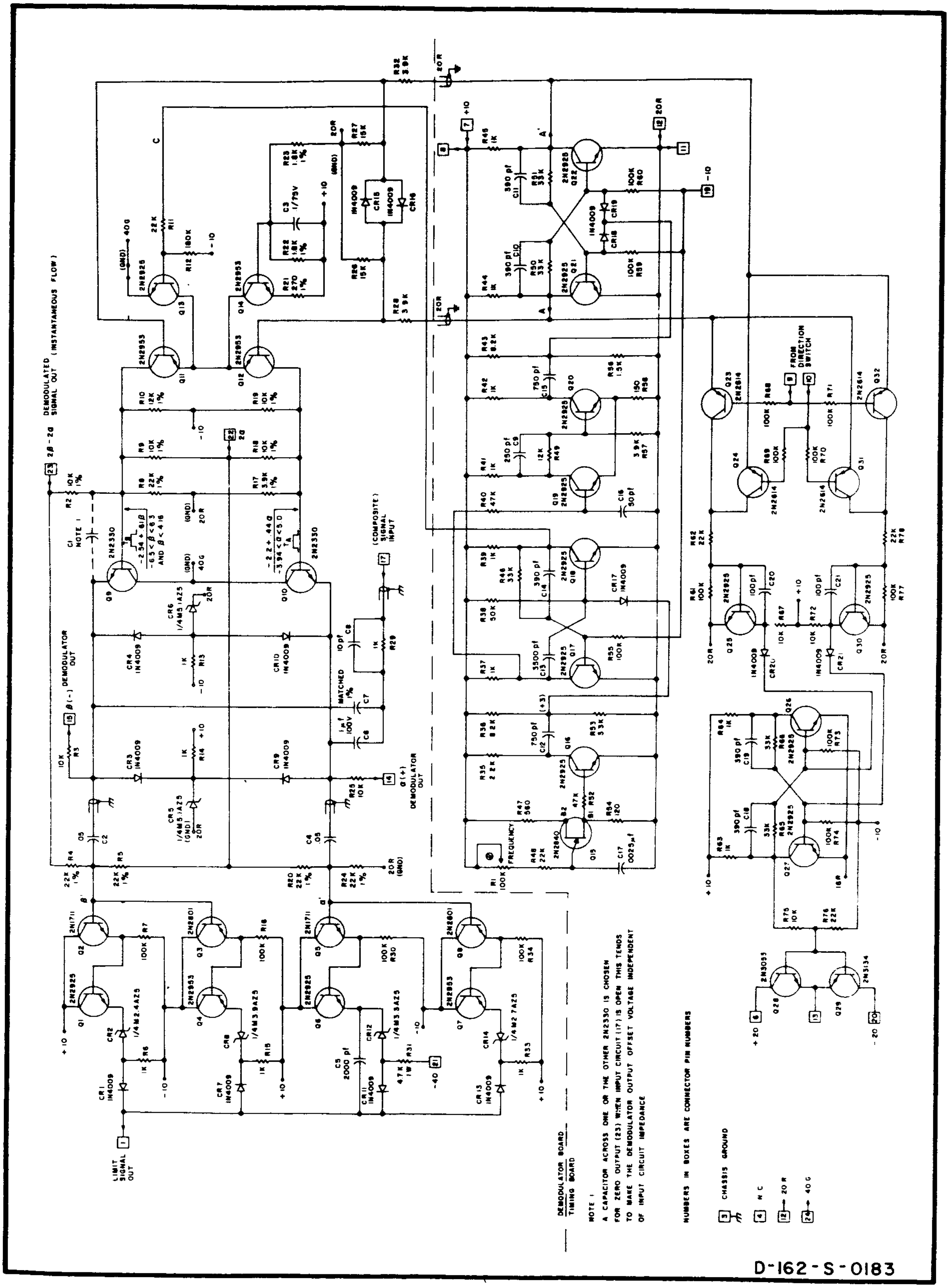


FIG. 24 TIME - LOGIC AND DEMODULATOR CIRCUITS , CODE 5,4 F

waves A and A' used to actuate the demodulator. They are also used to initiate development of a trapezoidal voltage of one relative phase or the other depending upon the position of the DIRECTION switch on the front panel. (The switch wiring is shown in Fig. 30).

The DIRECTION switch connects either terminal $\boxed{9}$ or $\boxed{10}$ to +10VDC and the other terminal to ground. If $\boxed{9}$ is grounded, two switching transitors (Q 23,32) will have sufficient current in their base resistors (R 68,71) to conduct A when positive to one delay circuit (Q 25; R 61,62, 67; C 20) and A' when positive to another (Q 30, R 72,77, 78, C 21). If $\boxed{10}$ is grounded, two analogous switching circuits (Q 24, 31; R 69, 70) connect A and A' to the delay circuits in the opposite manner. When the input to a delay circuit goes positive it quickly short-circuits its collector to ground (20R). When the positive input current ceases, the collector voltage rises at a rate determined by the collector-base capacitance and the base-emitter conduction voltage and shunt resistance. Each delay circuit collector is connected by a diode (CR20, 21) to one base of a bistable multivibrator (Q26,27; R63,64,65,66,73,74; C18,19). The rising collector voltage forces one diode and one transistor in the multi into conduction which readily drops out the second transistor current because the second diode had already been back-biased. A resistive divider (R75,76) on one multi collector provides a square wave which is roughly symmetrical with respect to ground. This is coupled out to the Trapezoid Generator by means of complementary emitter followers (Q28,29).

2. <u>Demodulator</u>

The demodulator circuit diagram is contained in Fig. 24. The base current for the NPN demodulator switching transistors (Q 9,10), also called choppers, comes from a pair of PNP transistors (Q 11,12) having a 10 ma constant current supply (Q 14; R 21,22,23; C 3) in their common emitter circuit which can be short-circuited by another transistor (Q 13) driven through a resistive divider (R 11,12) by the C pulse. Which of the PNP pair conducts the constant current, in the absence of the C pulse, is determined by their relative base voltages. These may differ by the forward conduction voltage of either one of a pair of oppositely oriented shunt diodes (CR 15,16) bridged between identical resistive dividers (R 28,26) (R 32,27) on the A and A' multi outputs. The dividers in each case above are used to bias the signals and limit their current appropriately.

The choppers (Q 9,10) are operated in the inverted mode (collector and emitter interchanged) to minimize their offset voltages. Only if there is a change in the difference between these voltages will there be an error in indicated flow attributable to these choppers. Such errors have not been observed.

Two important currents flow in the chopper ground circuit which returns to 40G (see Fig. 30). One of these is the chopper switching current which is constant because of its source (Q 14; etc.), and because it always flows in the chopper (collector) ground circuit either through one or the other base-collector junction or through the short-circuiting transistor (Q 13). The other is the composite signal current (through R 29; C 6 or C 7) from the Third Amplifier. This amplifier is referenced to the point 40G.

The basic demodulation scheme is described in Section II-C.3. The correspondance between components of Fig. 15 in that section and those in the actual flowmeter is as follows:

Basic circuit, Fig. 15	Flowmeter	
	Figure	Components
Current bridge $\|I\|$ Voltage bridge $\|V_3\|$	19	CR 13,14,15,16; R 13,14 CR 8,9,10,11,12 Q 9,10 R31, C11
Demodulator Driver		All others
R	24	R 29
C,C		C 6,7
Switch (T_A)		Q 10
Switch (T_B)		Q 9
R 13,14		R 24,20
R 23,24		R 5,4
E_β Amplifier, limiter (+)		Q 1,2; R 6,7; CR 1,2
(-)		Q 3,4; R 15,16; CR 7,8
E_α Amplifier, limiter (+)		Q 5,6; R 30,31, CR 11,12
(-)		Q 7,8; R 33,34; CR 13,14
C 1		C 5
(R 11,12)	(25)	(R 11,20)
(R 21,22)		(R 30,31)
(Isolation amplifiers)		(All others)

The success of the demodulator described by Fig. 24 depends upon certain circuit features not yet mentioned. Foremost of these is the condition that there be very low leakage current in the demodulator capacitors (C 6,7) and in their associated circuits. This condition is satisfied by the using of Mylar capacitors, planar silicon chopper transistors and isolation amplifiers of extremely low (0.4 microampere) input current. This low current is achieved in the Instantaneous Flow Amplifiers, used for isolation, at the expense of bandwidth which insofar as flow information is concerned need only be about 100 cps. But bandwidth of a high order is required in the feedback-limiter path involving the Instantaneous Flow Amplifiers for the prevention of chopper overvoltage. Limiting here is very critical; the choppers will avalanche when the emitter-base voltage exceeds about 6 volts; the design maximum peak-to-peak flow signal is 4 volts.

In order not to compromise the response of the limiter circuit, direct transmission at high frequencies is provided by three capacitors (C 8,4,2). These are equivalent to the following additions to Fig. 15: a capacitor across R, one between E_α and E'_α points and one between the E_β and E'_β points. The first compensates for the inevitable stray capacitance to ground and does not interfere with demodulation because it is small. The effect of amplifier input capacitance has been reduced by series resistors (R 3, 25), which are not shown in Fig. 15. The second and third connect points which would be of identical voltage if the bandwidth of the Instantaneous Flow Amplifiers were unlimited. To show that the currents which result from the finite bandwidth f_o have negligible effect upon indicated flow, assume that the shorting of a chopper in Fig. 15 at T_B has introduced a step $E_\alpha(t)$ equal to the peak-to-peak flow voltage E_F. Then

$$E_\alpha - E'_\alpha = E_F \, e^{-2\pi f_o t}$$

The current which would flow in the circuit if there were a capacitor between the E_α and E'_α points would be I which is less than

$$\frac{E_F}{R} e^{-2\pi f_o t}$$

because of the capacitor voltage drops in the current path. R is the resistance R_{13} and R_{14} in parallel. Therefore, the change in flow voltage ΔE_F which occurs in a half period T as a result of I flowing through the two C's in series is

$$\Delta E_F = \frac{2}{C} \int_o^T I \, dt \leq \frac{2E_F}{RC} \int_o^T e^{-2\pi f_o t} dt$$

$$\leq \frac{2E_F}{RC} \int_o^\infty e^{-2\pi f_o t} dt = \frac{2E_F}{RC} \frac{1}{2\pi f_o} .$$

Substituting for R_{13}, R_{14} and C the values of the analogous components (R 24,20; C 6,7) in Fig. 24 and assuming a closed loop cut-off frequency of one megacycle for the amplifier,

$$\Delta E_F \simeq 3 \times 10^{-5} E_F .$$

The effect of the limited bandwidth of the instantaneous Flow Amplifier is therefore small and, being proportional to the flow signal is equivalent to a reduction in demodulator gain.

Double emitter followers ensure that the α' and β' dividers (R4,5)(R20,24) are negligibly affected by limit current. The second emitter in each follower supplies the limit current and the minimum current required by the Zener diode for reliable operation at the limit voltage. At all other voltages the emitter current is not important except in the case of the emitter follower (Q6; R31; CR12) chosen to limit the output voltage rate-of-change of the Third Amplifier (the demodulator driver) to a value that will not overtax the Instantaneous Flow Amplifiers during T_C (Fig. 14) when both demodulator switches are open. In this case a higher emitter resistance (R31) and supply voltage (-40 VDC) is used. For remaining emitter-follower functions see chart above.

Some of the Demodulator offset voltage may be attributed to the fact that the chopper transistors do not have the same base-emitter parasitic capacitance. Unless the capacitance is matched the demodulator offset is sensitive to input impedance. This impedance changes when the demodulator input is switched to circuits other than the output of the Third Amplifier for certain purposes. (See S1n, Fig. 30). To render the demodulator less sensitive in this respect, base-emitter capacitance (C 1) is added to one chopper if necessary to make the offset voltage approximately the same whether the input $\boxed{17}$ is open- or short-circuited.

Three conditions must be avoided in order for the chopper transistor to be an open circuit. The base shall not be positive with respect to the collector (ground) or the emitter (α or β) or more than 5 volts negative with respect to the emitter. Either of the first two conditions will turn the transistor "on" and the third may cause the base-emitter junction to avalanche. These provisos can be satisfied by making the base voltage of the "off" chopper a linear function of its emitter voltage, and depending upon the limiter already described to restrict the emitter voltage. The appropriate functions are constructed by resistive summation from Instantaneous Flow Amplifier outputs (as in the case of α' and β'), -10 VDC and ground. One chopper, (Q10) with emitter voltage α, has base voltage $-2.2 + .44\alpha$ established by three resistors (R17,18,19), the other, (Q9) with emitter voltage β, has base voltage $-2.54 + .61\beta$ established by four resistors (R2,8,9,10). For base-emitter voltages between -5.0 and 0.0, α may lie between -3.94 and + 5.0, and β between -6.5 and +4.16. Under constant maximum average forward flow conditions α will be switched from 0.0 to +.5 volts and β from -.5 to 0.0. The measured limit voltages were

	α	β
Forward	+4.4	-4.9
Reverse	-3.6	+3.7

Therefore, the maximum forward-flow peak may be greater than eight times its average before limiting can occur. The chopper emitters are also protected against turn-on and turn-off transients in excess of about 6 volts from the Third Amplifier by a set of Zener and ordinary diodes (CR 3, 4,5,6,9,10; R 13,14).

C. FLOW-SIGNAL PROCESSING

1. The Instantaneous-Flow Amplifier

The unit known as the Instantaneous Flow Amplifier consists of two isolation amplifiers with their summing networks connected as shown basically in Fig. 15 (G 1,2; R 11, 12,21,22). Each accepts flow voltage information from charged capacitors and reproduces it at its output without significantly influencing the charge. The actual summing networks (R 11,20,30,31) are shown in Fig. 25 where it may be seen that each isolation amplifier comprises two completely symmetrical push-pull stages of voltage amplification with emitter followers for interstage and output coupling. A description of one isolation amplifier follows; the other is identical except for its output circuit.

The amplifier input resistance is inherently high: the feedback signal at one base of the first stage is nearly identical to the input signal at the other. If it were identical the stage could be bisected. Then the input conductance would be the sum of the output conductance (h_{ob}) of the first-stage transistor (Q 1) and half that of the current-source transistor (Q 9). The equivalent resistance is estimated at greater than one megohm.

The amplifier input current is only about 0.4 microamperes: the minimum rated current gain at the collector current of 0.068 ma is about 200.

The amplifier drift is very small: the maximum temperature coefficient for differential changes in base-emitter voltage is less than 10 microvolts/^{o}C. This is the result of the two first-stage transistors (Q 1,2), which are of diffused planar silicon construction, being integral parts of a single six-terminal package (designated 2N2920).

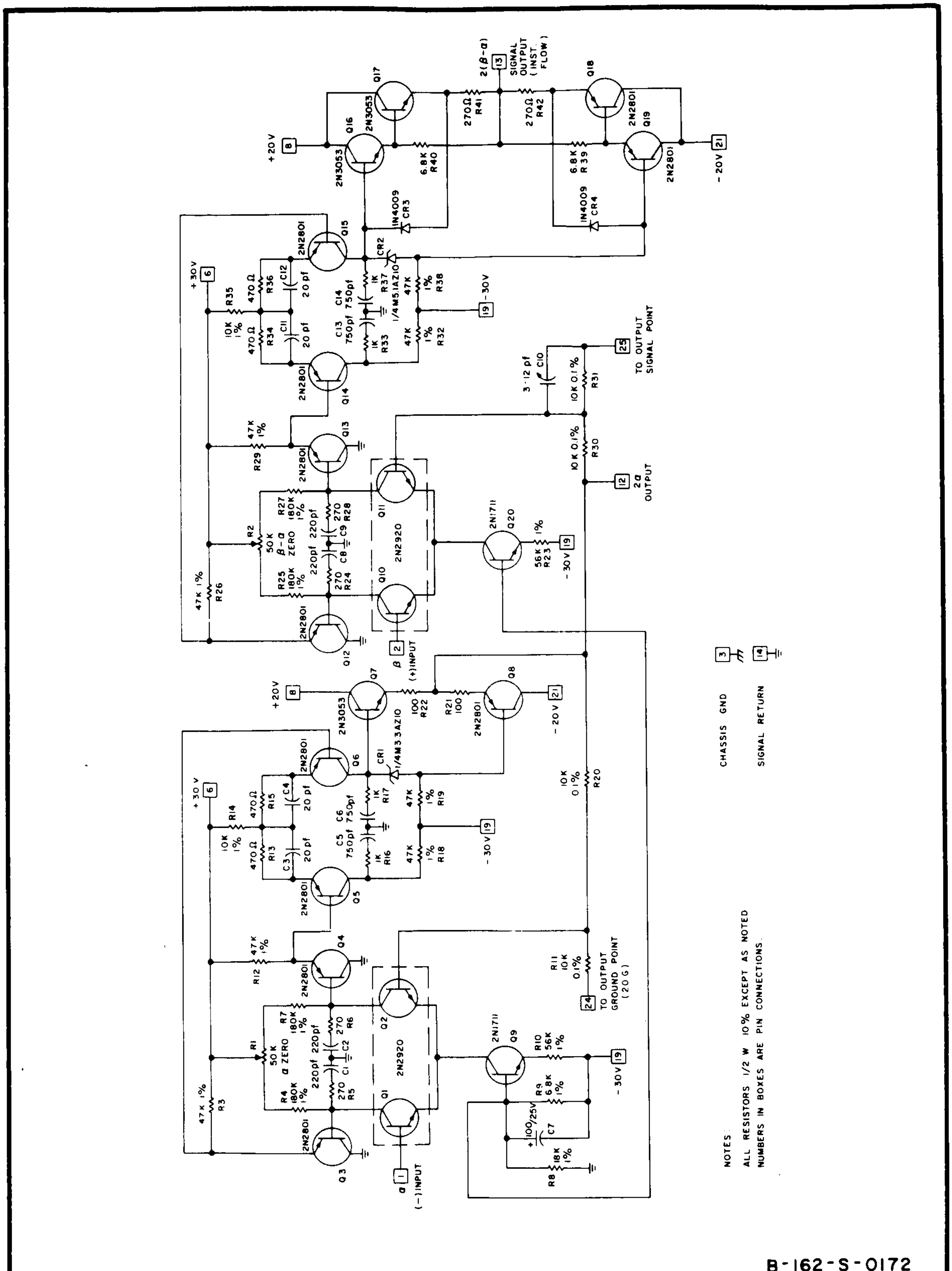


FIG. 25 INSTANTANEOUS - FLOW AMPLIFIER , CODE 5,2 E

A constant current source (Q 9; R 10) which shares a divider (R 8,9; C 7) with the second amplifier maintains a first-stage common emitter current of .136 ma. This results in a quiescent 16.5 volts at the collectors. Differential changes in collector loads (R 1,4,7) may be introduced by means of the ZERO control (R 1) to compensate for the offset voltage of the amplifier and that of the chopper in the Demodulator. Emitter followers (Q 3,4; R 3,12) couple the first stage to the second. The resistance looking into the second stage is raised to more than 15K ohms by individual emitter resistances (R 13,15); looking into the emitter followers it is more than 330K ohms. The precision of the common emitter resistance (R 14) and the collector loads (R 18,19) of the transistors (Q 5,6) in the second stage is such that the quiescent collector voltage remains near zero. A Zener diode in series with the collector of a second-stage transistor (Q 6) provides the difference voltage for the output emitter-follower.

The first isolation amplifier output complementary emitter-follower (CR 1; Q 7,8; R 21,22) has an idling current of 10 ma and is simple. The second amplifier follower (CR 2; Q 16,17,18,19; R 39,40,41,42) has an idling current of 5 ma and it is compound. Two diodes (CR 3,4) prevent its output current from exceeding about 17 ma.

Each amplifier has three symmetrical shunt networks for the control of its open loop frequency response. One of these (C 1,2; R 5,6), between the first-stage collectors, causes a 20 db/decade negative gain slope from 5 kc to 250 kc. Another (C 5,6; R 16,17), between the second stage collectors has the same effect. Another (C 3,4) between the second stage emitters causes a positive gain slope above one megacycle which, in the vicinity of the one megacycle crossover point sufficiently compensates for the large ultimate negative slope beyond 5 megacycles. The controlled response is shown in Fig. 26.

The common mode signal rejection ratio of the complete Instantaneous Flow Amplifier at low frequencies is primarily a measure of summing network precision since the amplifier error signal is about $10^{-4} \times$ the input and the summing resistor tolerance is $\pm 10^{-3}$. At high frequencies the rejection ratio is less because one signal goes to the second isolation amplifier directly and the other does so through the first where the high frequency content of the signal is lost.

As a result, transient jiggles proportional to spike amplitude appear in the Instantaneous Flow signal at the times when the spike begins and ends. The high-frequency ratio is improved by a small capacitor (C 10) across the second feedback resistor (R 31). The effects of poor high-frequency common mode rejection are mitigated by restricting the maximum possible rate of change of input voltage as is done by the limiter circuit through the Demodulator (Fig. 24; C 4,5; Q 5,6; etc.) and the Third Amplifier (Fig. 19, Q 9, 10; etc.).

Remote sensing is employed to establish the demodulated flow signal across its output jack. The output voltage of the Instantaneous Flow Amplifier is twice the difference between its two input voltages $\boxed{1}$, $\boxed{2}$ and it is best defined between two points. One is the point where the feedback resistor meets the output of the second isolation amplifier and the other is where the input resistor of the first meets ground. In fact any voltage applied to the

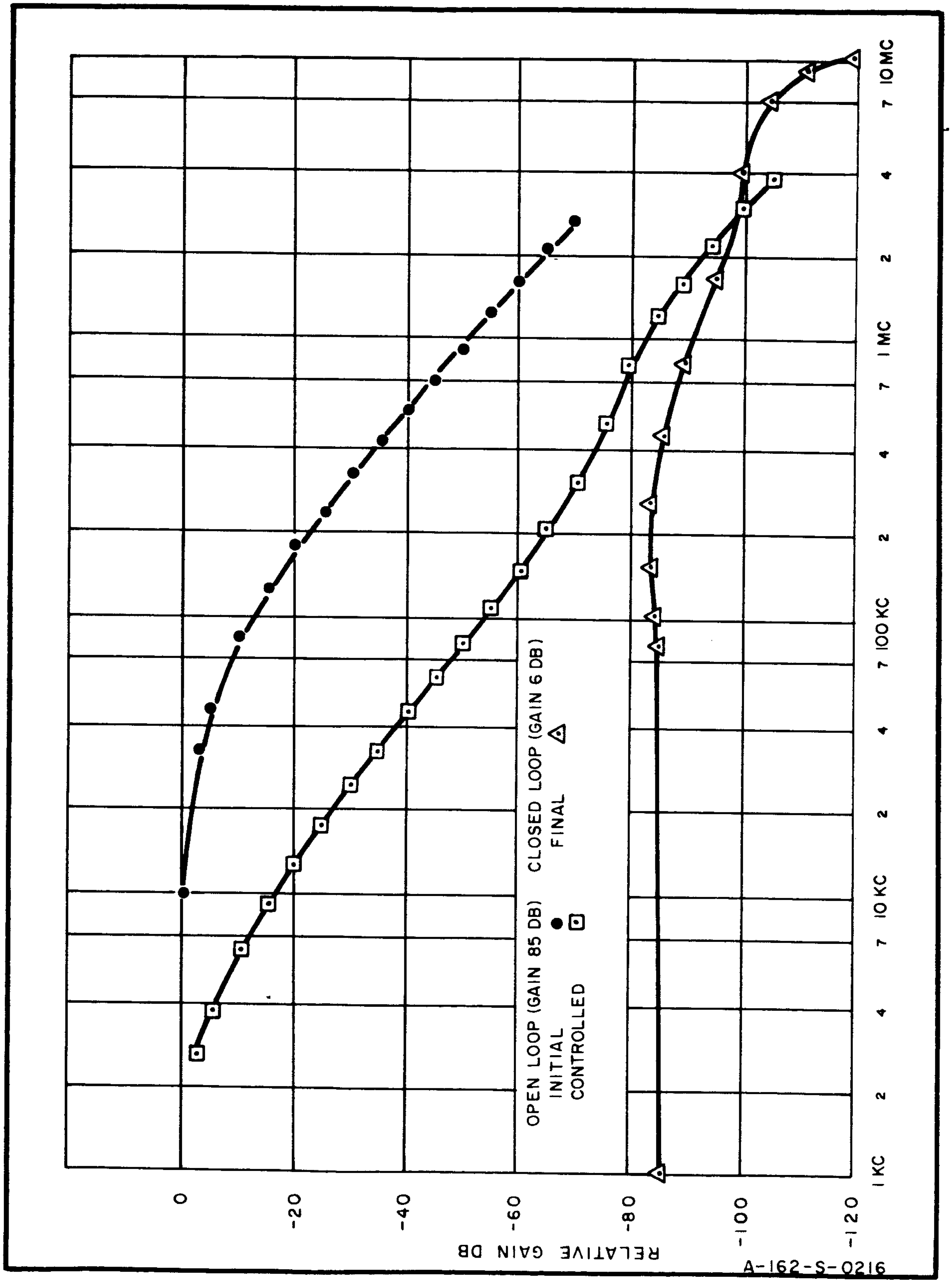


FIG. 26 INSTANTANEOUS-FLOW AMPLIFIER FREQUENCY RESPONSE

first input resistor reappears at the second feedback resistor (after two inversions). The output circuit $\boxed{13}$, therefore, is connected to the front panel INSTANTANEOUS FLOW jack (Fig. 30) where it joins the feedback circuit $\boxed{25}$, and the input circuit $\boxed{24}$ is grounded at the jack. As a result the flow signal at the jack cannot be corrupted by internal or external ground-loop currents. This ground point is designated 20G. In effect, the common-mode signal rejection property of the Instantaneous-Flow Amplifier permits a local ground point to be established which in theory is as good as a central ground point and in practice is better by virtue of ground leads being shorter.

2. Average-Flow Amplifier

The Average-Flow Amplifier circuit is a low-pass filter with a gain of precisely 10. Its filter cut-off frequency of .02 cps may be shifted to approximately 0.2 cps by pressing the RAPID AVERAGE switch on the Flowmeter front panel. The corresponding rise times are 8 and 0.7 seconds.

The circuit consists of a Fairchild type A00-4 amplifier, described in Appendix A, connected, as shown in Fig. 27, to an emitter-follower (Q 1; R 6) which supplies the current to the AVERAGE FLOW output jack (Fig. 30) on the front panel and to a feedback network. The normal feedback path is a resistor (R3) of high precision and a capacitor (C1) of low leakage in parallel. In the event of excessive signal at the input resistor (R 2), the output is limited by supplementary feedback through a voltage bridge (CR 1-9; R 4,5), somewhat like that described in connection with Fig. 11B. In the positive direction the limit is set primarily by a Zener diode (CR 6); in the negative direction by the forward

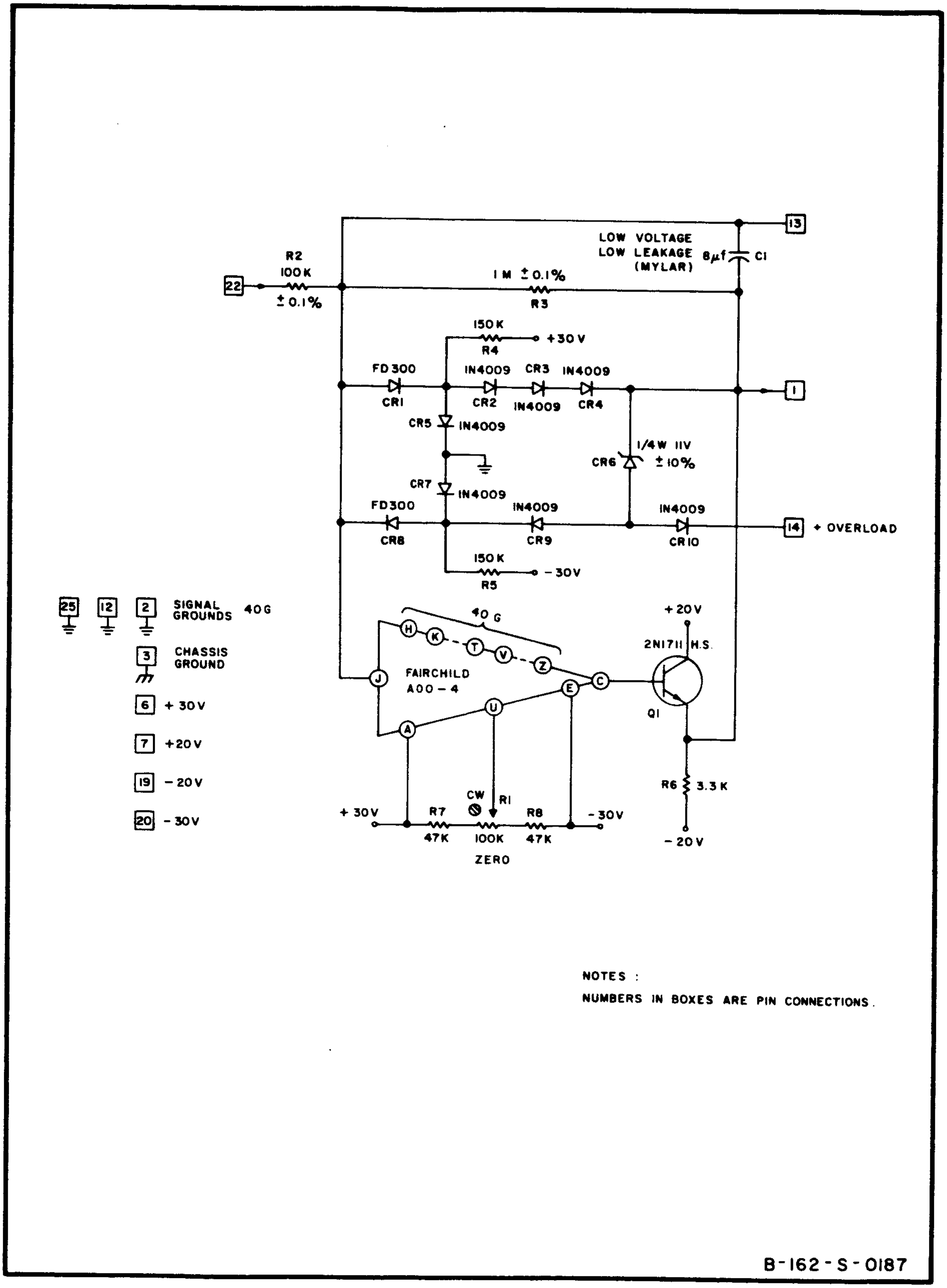


FIG. 27 AVERAGE - FLOW AMPLIFIER , CODE 9,2 M

conduction voltage drops of two ordinary silicon diodes (CR 3, 4). Another diode (CR 10) connects this circuit to the overload indicator circuit described in Sec. III-D.1. The OVERLOAD lamp will light when the Average Flow Amplifier output is within about one-half volt of being limited in the positive direction. (A negative overload will be evidenced by a reversal of the Flow Indicator.)

The ZERO control circuit (R 1,7,8) is essentially that recommended by the amplifier manufacturer but it has a smaller range and consequently higher resolution.

The RAPID AVERAGE switch raises the cut-off frequency of the circuit by simply shunting the input and feedback resistors by others of one-tenth their resistance. The circuit details are shown in Fig. 30 (S8; R103,104).

3. <u>Integrators</u>

In the Flowmeter one integrator is used to measure the volume of a sample by integrating the output of the Instantaneous Flow Amplifier and another to measure the duration of the sample by integrating a constant. The integrators start simultaneously because each is controlled by (a separate set of contacts on) a single switch. Those parts which are common to the two integrators are indicated by identical symbols in Figs. 28 and 29.

Each integrator employs a Fairchild Type A00-4 amplifier described in Appendix A. The DRIFT control circuit (R 1,2,3) is of narrower range than that recommended by the manufacturer but it has proven satisfactory in all four applications of these amplifiers in the Flowmeter. A voltage bridge (CR 1-7; R 5,6) provides feedback to limit the output voltage before the amplifier can be overloaded (See Section II-C.2, Fig. 11-B). An additional diode (CR 8) leads to the

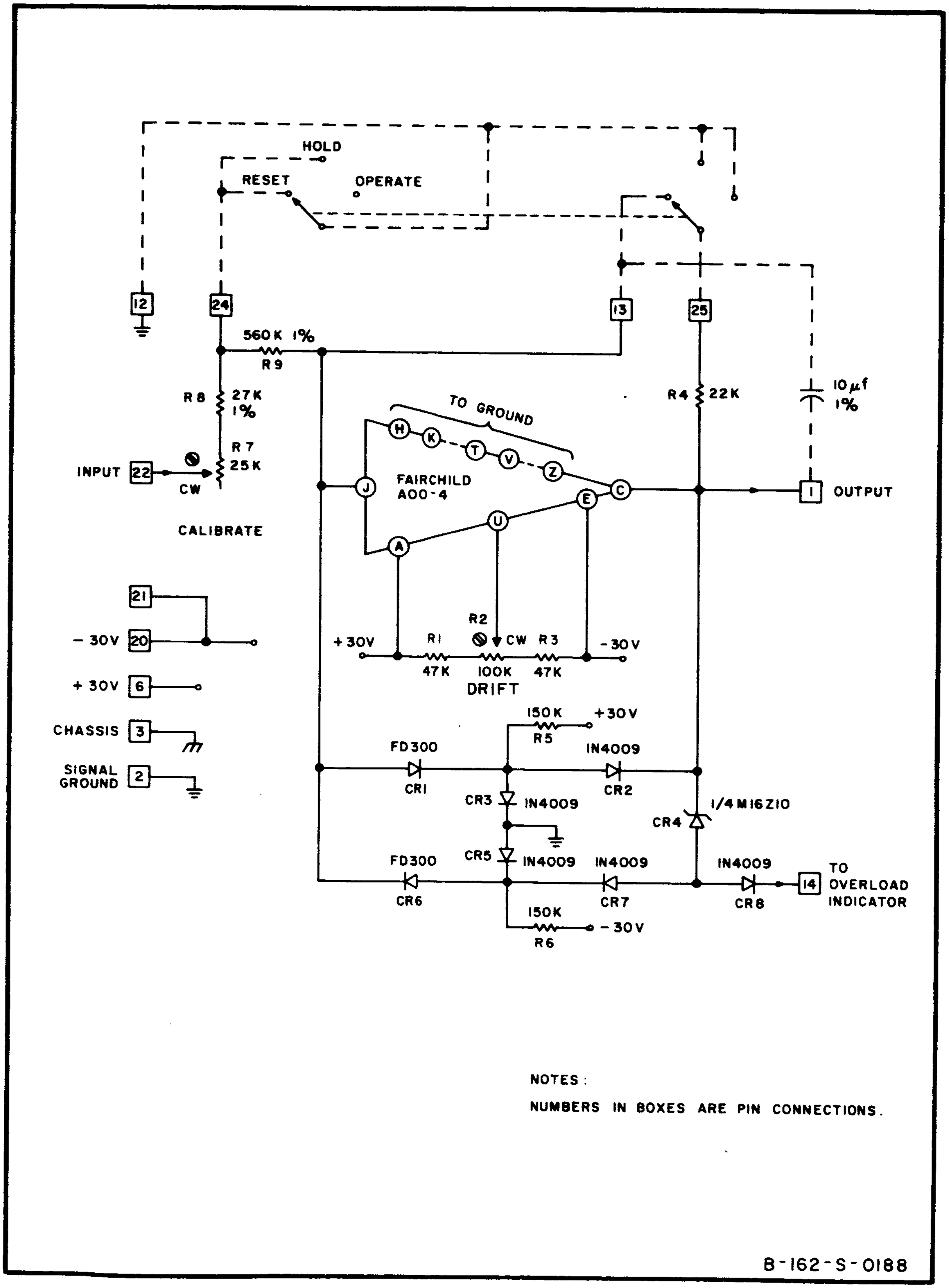


FIG. 28 INTEGRATOR, VOLUME, CODE 7,8 N

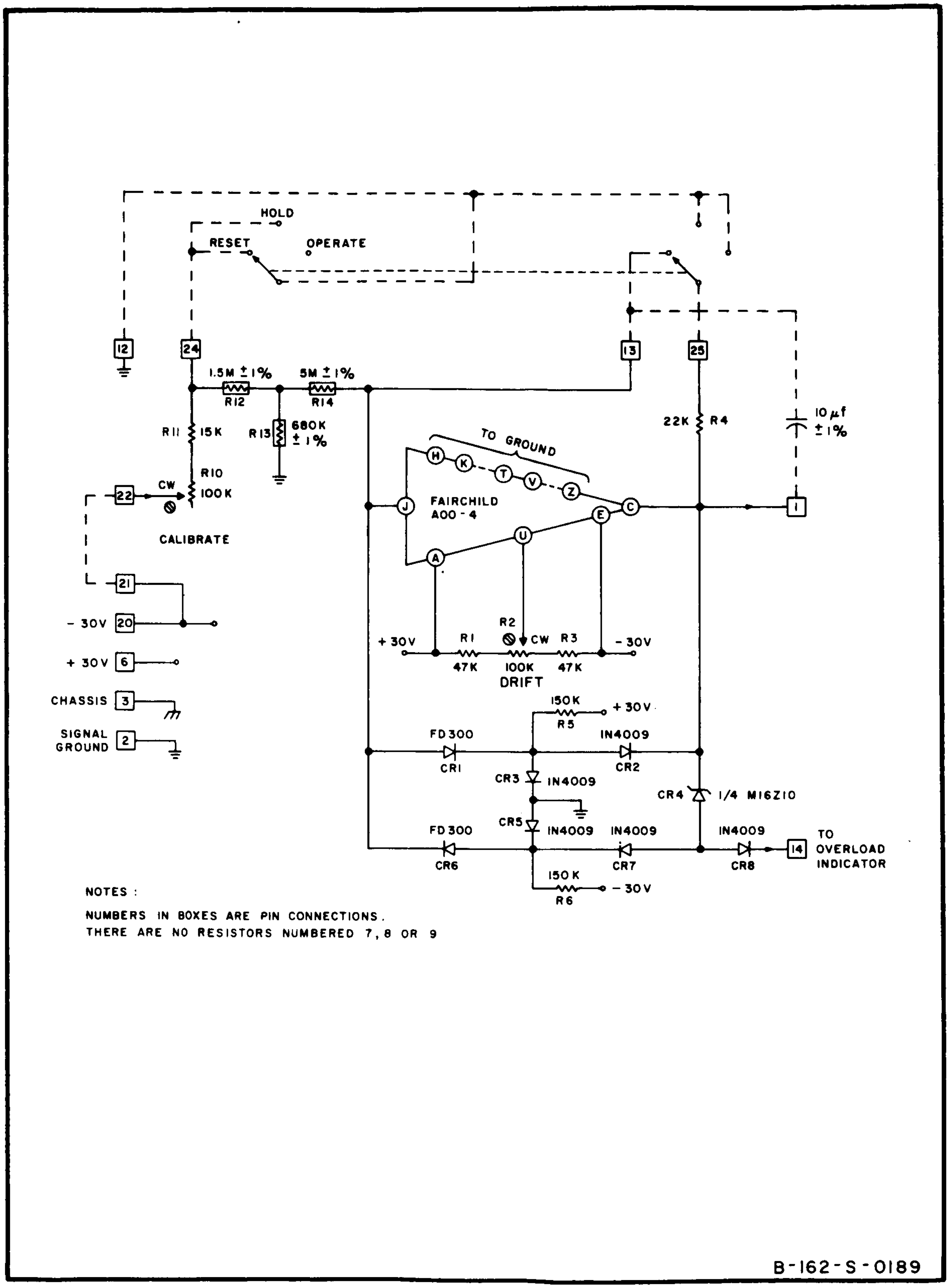


FIG. 29 INTEGRATOR , TIME , CODE 7,6 L

OVERLOAD indicator, described in Sec. III-D.1, which lights when the output is within about one-half volt of being limited.

The integrator is controlled by a switch (S 3 in Fig. 30) on the Flowmeter front panel. In the RESET position the input network is shorted and the capacitor is discharged through a resistor (R 4). In the HOLD and OPERATE positions this resistor is grounded. This makes the integrator operation independent of any possible leakage path between switch contacts.

a. Volume

Each size probe has a maximum average flow rating. The Flowmeter gain may be adjusted in each case (by means of thumbwheel switches which are set to positions corresponding to a number on the probe) to produce a signal of precisely one volt at the output of the Instantaneous Flow Amplifier when the probe is subjected to the rated flow. It is this signal which is integrated. The correct indication is obtained by appropriate attentuation between the integrator and the indicating voltmeter.

The input circuit for the integrator used in volume measurement may be found in Fig. 28. In order to achieve the desired 10 V out in one minute with a feedback capacitor of 10 microfarads and 1 volt in, the input resistance must be

$$R = \frac{(1 \text{ volt})(60 \text{ seconds})}{(10 \text{ volt})(10^{-5} \text{ farads})} = 600 \text{ K ohms}.$$

A CALIBRATE control (R 7) with a ±2% range is provided in the input network (R 8,9) which enables the integrator scale factor to be set very precisely despite the ±1% tolerance on capacitance and resistance of the components. The first two resistors (R 7,8) in the series limit the current to an insignificant value when the network is shorted by the switch.

b. Time

The integrator for time derives its input from the precisely regulated -30 VDC supply. As shown in Fig. 29 the required current:

$$I = \frac{(10 \text{ volt})(10^{-5} \text{ farads})}{(60 \text{ seconds})} = \frac{10}{6} \text{ microamperes}$$

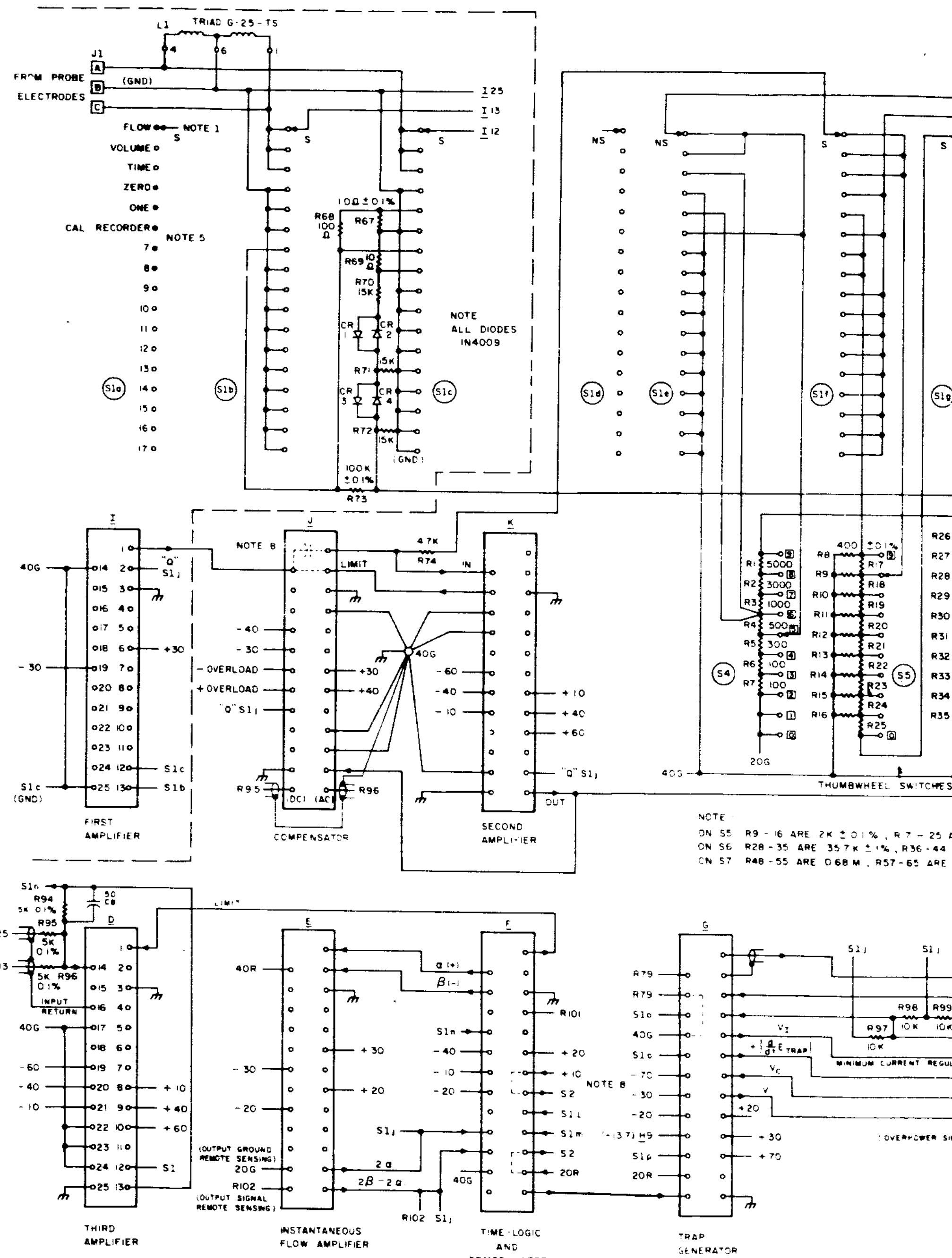
is obtained in a 5 megohm input resistor (R 14) by an attenuator (R 10,11,12,13) using standard resistance values. A CALIBRATE control (R 10) with a ±2.5% range enables precise calibration. Current limiting, when the input network is shorted, is provided by the first two resistors (R 10,11).

D. FLOWMETER OPERATING MODES

1. Inter-Unit Signal Circuits and Overload Indicator

Exclusive of power supplies and regulators there are 12 major units described individually in this report. Their signal interconnections will be described with reference to Fig. 30. At the upper left hand corner is the connector (J 1) for the probe electrode circuit. At the right center are the connections to the Voltmeter-Indicator and the Instant Flow and Average Flow jacks (J 2,3) for the outputs to external recorders. At the bottom center is the connector (J 4) for the probe electromagnet. For simplicity the various units have been designated by letters. The letters are underscored to distinguish them from symbols.

In the first three positions of the master switch (S 1) the electrodes are connected to the First Amplifier (I).



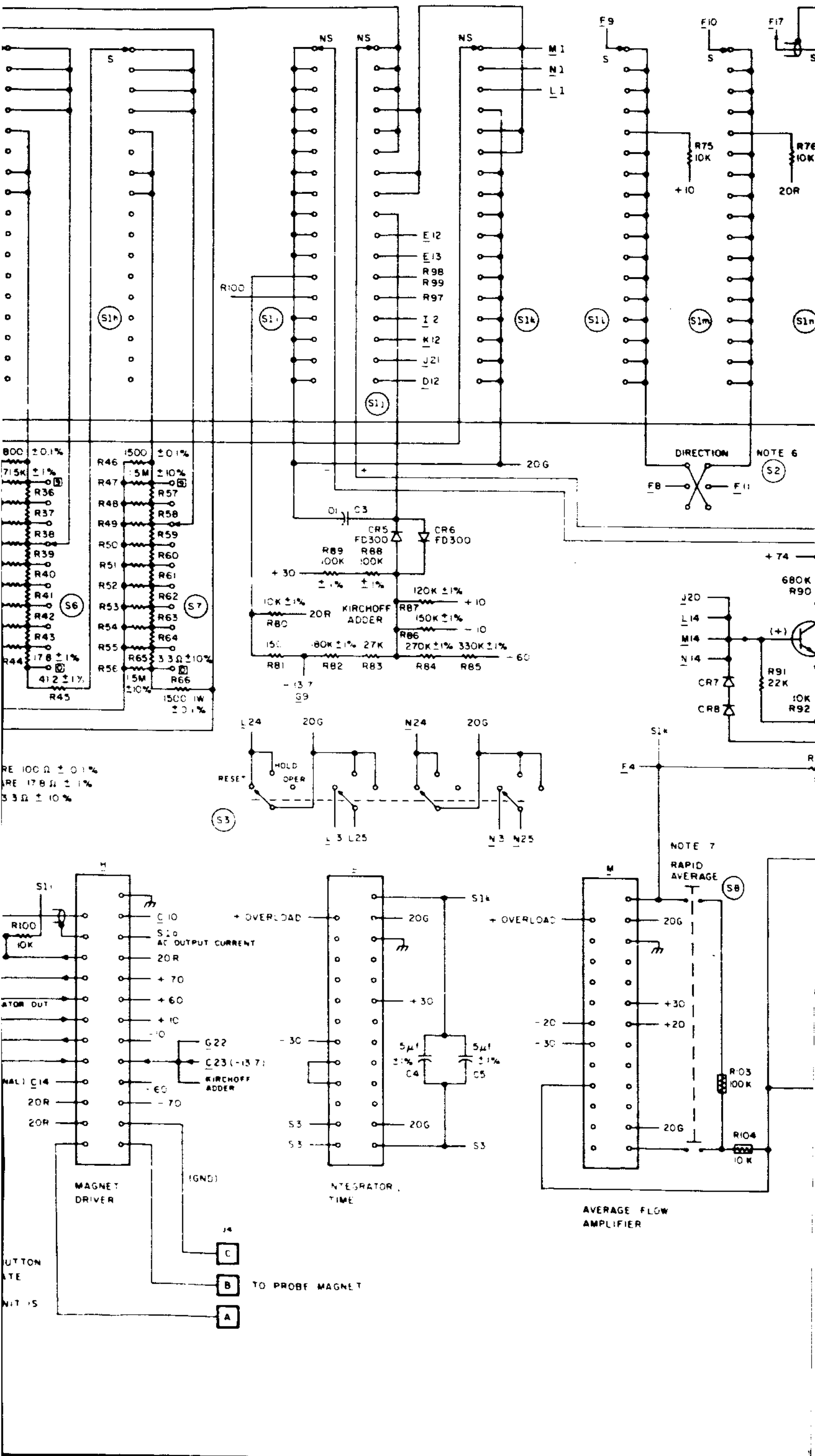
NOTES

1 - SWITCH SECTIONS MARKED S ARE SHORTING TYPES (MAKE - BEFORE - BREAK)
SWITCH SECTIONS MARKED NS ARE NON - SHORTING TYPES (BREAK - BEFORE - MAKE)
2 - UNDERSCORED LETTER REFERS TO UNIT (CONNECTOR)
3 - THERE ARE THREE IMPORTANT SIGNAL GROUND POINTS 40G LOCATED BETWEEN J AND K
20G LOCATED BETWEEN J2 AND J3
G LOCATED IN H ON COPPER SHIELD NEAR INPUT TERMINAL
4 - CHASSIS
5 - MASTER SWITCH (S1) MARKINGS ARE BLACK EXCEPT NUMERALS 7 & 8 GREEN AND INDEX DOTS 1,4,5,6,7,8 RED

6 - GREEN
7 - RED WITH RED PUSH
8 - DOTTED LINES INDIC
CIRCUITS WHICH ARE
COMPLETED WHEN
PLUGGED IN

81

ELECTRONICS RESEARCH LABORATORIES



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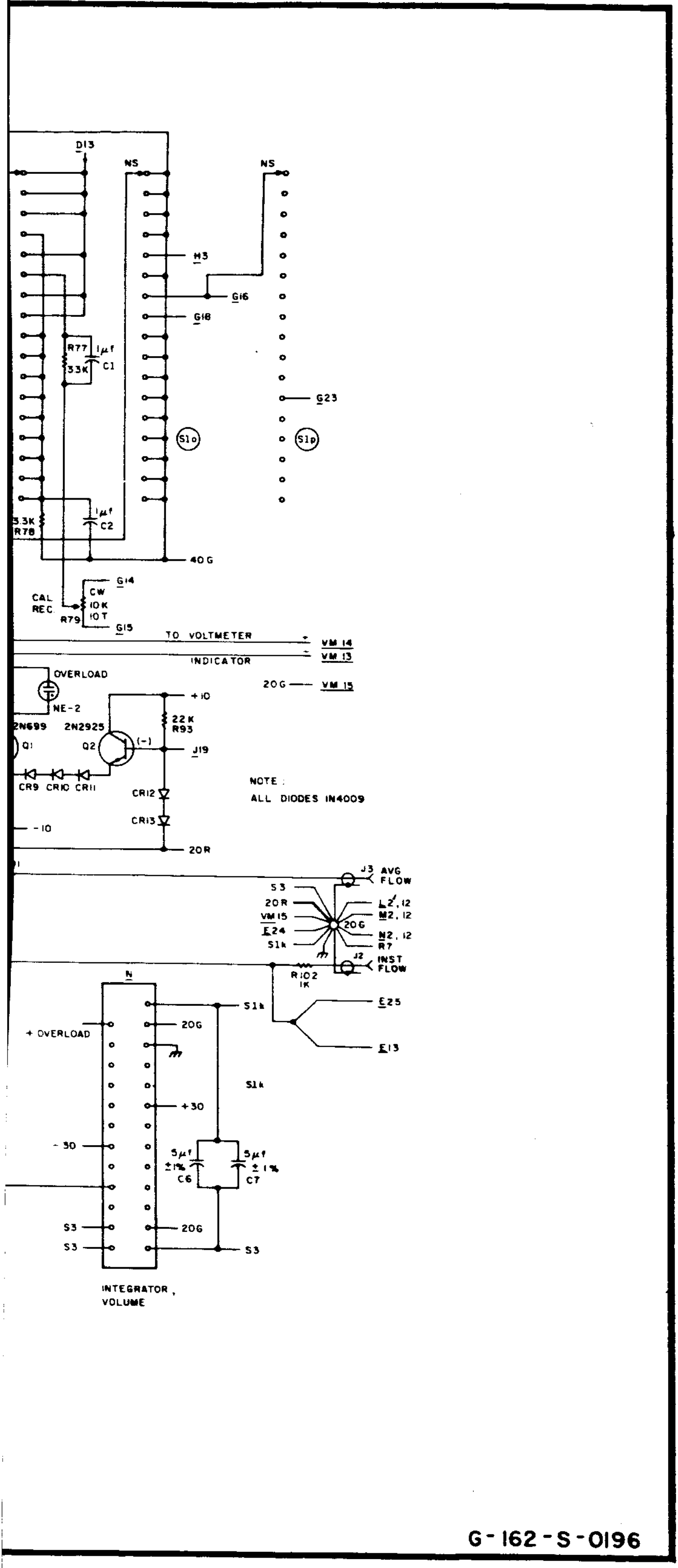


FIG. 30 INTER-UNIT AND SWITCH DIAGRAM

The output I 1 - J 14 corresponds to the junction of R 1 and C 1 in Fig. 13B. The limit signal is brought to this junction by means of an internal jumper J 2 - J 14. The capacitor corresponding to C 1 is located in the compensator and connected from J 1 to J 14. The remaining Compensator and Second Amplifier connections will be shown to correspond to Fig. 10. The Second Amplifier output goes to an attenuator (R8-66), which is set up by means of three thumb wheel switches (S 5,6,7), and returns by way of a feedback resistor (R 74) to the Second Amplifier summing junction K 14. The attenuator design considerations are covered in Appendix D. The other Second Amplifier output (K 13) goes to the Compensator (J 12). The so called Compensator unit has two outputs to the Third Amplifier input resistors. J25 corresponds to the inverter output and J13 corresponds to the junction of C_ϵ and R_ϵ in Fig. 10.

The Third Amplifier output D13 is connected to its feedback resistor (R94) and, in the first three positions of S1n, to the Demodulator input F17 which corresponds to R in Fig. 15. In the interconnections between the Demodulator and the Instantaneous Flow Amplifier, α and β in Fig. 30 correspond to E_α and E_β in Fig. 15. The Instantaneous Flow Amplifier connections to its output jack (J2) are explained in section III-C.1. The voltage established there is the input to the average flow amplifier M22 and the Volume Integrator N22 but there is a current limiting resistor (R 102) <u>in series with the jack</u>. The average flow signal M1 goes to its jack (J3), through a current-limiting resistor (R101), and to the master switch (S1k). In the Flow position of S1 the average flow signal is attenuated (R1-7), according to a thumbwheel switch (S4) position which corresponds to the diameter of the probe lumen, before going through the switches (S1e,j) to the Voltmeter-Indicator* positive terminal. In the second position of S1 the output of the VOLUME Integrator (N1) is read, after attenuation in exactly the same manner. It is important that the Voltmeter-Indicator return (through S1i) to the proper ground point (20G) for all DC output circuits.

The volume and time integrators are started simultaneously by the same switch (S3), as described in Section III-C.3. The integrator output L1, when S1 is in the TIME position, passes through this same attenuator (R1-7) but in this case the attenuation factor is fixed at 10. Thus when the time integrator reaches 10 volts at the end of one minute the Voltmeter will read 1.000 for the time in minutes. That this attenuator has an appropriate tap is simply a coincidence.

The electrode circuit return to ground is through a center-tapped inductor (L1). The total inductance is 1800 henries. At the lowest repetition frequency contemplated for the flow meter (100 cps) the impedance of this inductor is 1.1 megohms. The DC resistance from either side to ground is 2750 ohms. In the first 3 positions of the master switch (S1) the only thing that changes is the quantity read out by the Voltmeter-Indicator. Flow information is not interrupted because the only switch sections which could do so are of the make-before-break variety. Beyond position three there is no flow computation as such. In position four, the ZERO position, the inputs to the First Amplifier are grounded, the Second Amplifier gain is at a minimum (maximum feedback), the Demodulator input is grounded through a current limiting** resistor (R78) which is by-passed (C2), and the Voltmeter again reads the output of the Average Flow Amplifier but

* The Voltmeter is described in Appendix B.
** See Section III-A.2, for further discussion of current limiting in this circuit.

without any attenuation. The purpose of the Zero test is to prove that there is no bias either in indicated flow or volume as a result of DC drift in the system.

In the fifth position of S1, marked ONE, a signal proportional to magnet current is taken from the Magnet Driver H3 through a switch (S1o), precisely attenuated (R67,68,73) in the shielded compartment for the First Amplifier and applied (S1c) to one input of the First Amplifier (I12) while the other input (I13) is grounded. The complete attenuator (R8-66) is switched (S1f,g,h) into the Second Amplifier feedback path. The Third Amplifier (D13) is switched (S1n) to the Demodulator input (F17) and the Average Flow Amplifier output is switched (S1e,k) through a fixed point on the divider (R 1-7) to the Voltmeter. If there is any defect in the flow measuring system the meter will fail to read 1.000. The Voltmeter will indicate forward flow whatever the position of the DIRECTION switch (S2): the Time-Logic terminals (F9,10) which in all other positions of S1 go to +10 VDC and ground (20R) through the DIRECTION reversing switch (S2) are switched there (S1 ℓ,m) directly in this (S1) position by make-before-break contacts. These contacts prevent interruption of flow information between the first three positions of S1. The magnet drive reversing circuit is described in Section III-B.1.

Connected to the .500 volt Trapezoid Generator output (G14,15) is a ten turn potentiometer (R79) marked CALIBRATE RECORDER with its arm connected to a current-limiting resistor (R77). The resistor, which is shunted by a capacitor (C1), is switched (S1n) in the sixth position to the Demodulator input (F17). The Average Flow (M1) signal is switched (S1k) to the first thumbwheel (S4) attenuator (R1-7) which is set according to the diameter of the probe lumen. The attenuator output is switched (S1e,j) to the Voltmeter-Indicator. The voltage at the Instantaneous Flow or the Average Flow jack will then be that which would result from a flow of the magnitude indicated. The magnitude may be set to any amount between zero and the maximum average flow rating of any given probe.

In position 7 of S1 the 12V peak-to-peak trapezoid signal (G16) is switched (S1o) to the attenuator (R67,68,73) and thence (S1b,c) to both of the First Amplifier inputs (I12,13). Second Amplifier gain is at maximum because its feedback attenuator (R8-66) is switched (S1f,g,h) in completely. The Demodulator input (F17) is switched (S1n) to the Third Amplifier output and the Voltmeter-Indicator is switched (S1j) directly to the Average Flow Amplifier output (M1). Because the common mode signal at the First Amplifier input terminals is (12 mv) more than 1000 times the maximum average flow signal from the weakest and the gain of subsequent composite signal and Voltmeter circuits is maximized, a common mode rejection ratio of 120 db may be readily verified. For this ratio the Voltmeter will indicate about 13 mv. The ratio may be maximized by means of the CMR potentiometer in the First Amplifier (See Section III-A.1).

In position 8 rectangular pulses proportional to the derivative of the trapezoid from the Trapezoid Generator (G18) are switched (S1σ) to a ladder network of series silicon diode pairs (CR1,2)(CR3,4) and shunt resistors (R69,70, 71,72). The diodes in each pair are in parallel and oppositely oriented so that they constitute an open circuit for signals of less than about one-half volt magnitude. The network output is switched (S1c) to one First Amplifier input (I12) and the other input (I13) is grounded (S1b). It simulates an artifact signal 530 times greater than the maximum average flow signal from the least sensitive probe that the Flowmeter can use, with a base line which is truly zero because of the diodes. The Second Amplifier gain is set to maximum (S1f,g,h; R8-66) as it would be for the least sensitive probe. The Third Amplifier output (D13) is switched (S1n) to the Demodulator (F17) and the Average Flow Amplifier (M1) is switched (S1j) directly to the Voltmeter. The meter reading will be a measure of the imperfection of the compensating networks and limiters.

The remaining positions correspond to different Voltmeter connections. In position 9 the voltmeter input is bypassed (C3) to keep out noise while it is connected through a pair of parallel low-leakage diodes (CR5,6), oppositely oriented to a Kirchoff adder (R82,83,84,85,86,87, 88,89), that is, to a junction connected to each of five other points by a path of different conductance. Each of the 5 points is the output terminal of a different power supply. When the voltage V at the junction,

$$V = \frac{\sum_{n=1}^{5} V_n G_n}{\sum_{n=1}^{5} G_n} ,$$

differs from its normal value of zero by about 0.2 volts the Voltmeter indication will differ noticeably from zero. If this is due to a change in the voltage ΔV_k of the k'th supply, then

$$\frac{\Delta V_k}{V_k} > 0.2 \frac{\sum_{n=1}^{5} G_n}{V_k G_k} .$$

For the actual network

$$\Sigma G_n = 26.5 \text{ micro-mhos}$$

and the minimum detectable single power supply error in each case is as follows:

V_k	G_k	$\frac{\Delta V_k}{V_k}$ (%)
+30	5.00	3.5
+10	8.33	6.4
-10	6.67	8.0
-13.7	4.83	11.0
-60	1.67	5.3

As explained in Sec. III-E.2, the $\pm$ 60 VDC supplies are linked together, and so are the $\pm$ 30 VDC supplies, in such a way that if the voltage of one of a pair declines, then so does the voltage of the other. Hence, in the 9th position of S1 the failure of any supply in the system can be detected.

In position 10 the Demodulator input (F17) remains grounded (40G) through the switch (S1n) while the Voltmeter (+) is switched (S1j) to the (2α) output of the first isolation amplifier (E12). If the offset voltages of this amplifier and its chopper (Fig. 24, Q10) do not cancel one another, the Voltmeter will not indicate zero.

In position 11 the conditions are the same as 10 except that the Voltmeter (+) is switched (S1j) to the (Instantaneous Flow) output of the second isolation amplifier (E13) and will not indicate zero unless all amplifier and chopper (Fig. 24; Q9,10) offsets cancel one another. This is the final test of the zero reference for the Instantaneous Flow signal. The final such test for Average or Indicated Flow is made in the (S1) ZERO position.

In position 12 the voltages proportional to the currents in each half of the Magnet driver output stage (Fig. 44, R45,53) are averaged by two identical resistors (Fig. 30; R98, 99) and switched (S1j) to the Voltmeter (+) which returns by switch (S1i) to a divider (R80,81) on the -13.7 VDC reference point for the stage. In this test the probe electromagnet need not be connected because the trapezoid signal is stopped by switching (S1p) the input (G23) to the output (G16) of its amplifier. Proper average current will result in zero indication.

In position 13 the Voltmeter is switched (S1i,j) through isolating resistors (R97,100) between the Magnet Driver output-stage emitter resistors (Fig. 40; R45,53) which are identical. Unless the average current in each half of the output stage is identical to that of the other, the Voltmeter will not indicate zero. The probe electromagnet must be connected for this test.

In positions 14,15,16 and 17 the Voltmeter negative is switched to ground (S1i) and its positive is switched (S1j) to the output points (I2, K12, J21, D12) of the First and Second Amplifiers, the Compensator, and the Third Amplifier (Figs. 16, 18, 22, 19), respectively. In each case the quantity measured will ultimately be zero unless the quiescent operating point of some unit is not right. The last two quantities depend upon the compensator integrator which may require as much as two minutes to settle.

The remaining components in Fig. 30 are the capacitors (C4,5,6,7) for the Time and Volume integrators (Figs. 29, 28) and the OVERLOAD indicator circuit.

The overload indicator circuit inputs (J19,20; Fig. 22),(L14; Fig. 29), (M14; Fig. 27), (N14; Fig. 28) are each connected through a diode to one or the other end of a Zener diode in a voltage bridge such as that described in connection with Fig. 11B, q.v. In this circuit, the onset of current in the Zener diode is marked by the passage of the voltage at one (or the other) end of the diode through zero. (The input voltage V_1 must then rise by an additional 2d, that is two more diode drops before output current begins).

In the overload indicator, Fig. 30, one transistor (Q1) base is clamped (CR7,8; R91) to -2d (the magnitudes of the individual junction forward conduction drops will not be distinguished) and the other (Q2) base is clamped (CR12,13; R93) to +2d. As a result of the drop in the base-emitter junction of the latter transistor and the drops in three diodes (CR9,10,11) the emitter voltage of the first transistor (Q1) is the same as its base voltage (-2d) and the transistor does not conduct. It will conduct if its base voltage goes (from -2d) past -d or if the other base voltage goes (from +2d) past +d. This transition will occur and the OVERLOAD lamp will light in response to current from a voltage bridge when the amplifier associated with the bridge is within 2d or about 1.2 volts of being limited. A shunt resistor (R90) prevents the lamp from responding to leakage current in the driving transistor (Q1).

2. <u>Operating and Testing</u>

Flow information from the probe electrodes is not processed by the Model B Flowmeter except within the range of the first three positions of the master switch. Flow information is not interrupted between these positions, but the electrodes are disconnected beyond them. Within this range a valid measure of volume, or cumulative flow, in any desired time interval up to one minute may be obtained by flipping the integrator switch at the left of the Indicator from RESET to OPERATE for the desired time and then to HOLD. The time in minutes may be monitored by leaving the master switch in the third or TIME position after which the volume in liters may be read in the VOLUME position. The integrator switch should be returned to RESET position. At any time the flow in liters/minute may be read in the FLOW position of the master switch. To get an immediate indication of average flow, push the RAPID AVERAGE button. Use the knob under the Indicator to shift the decimal point appropriately. The remaining positions of the master switch do not relate to actual flow.

The OVERLOAD lamp will light for a few seconds when the Flowmeter is first turned on and will flash occasionally on the crests of input noise. It will persist only if the integrators have been left on or there is a circuit abnormality.

Each probe will have a maximum average flow rating determined by its diameter. This is the magnitude of flow which, if the receiver gain is properly set, will cause the signal at the Average Flow output jack of the Flowmeter to have its maximum possible value of 10 volts. The corresponding Indicator reading is determined by the setting of the first thumbwheel switch which should correspond to the first digit of the code number on the probe. The remaining three digits correspond to the remaining thumbwheel settings which determine the gain, arrived at experimentally, for which 10 volts is obtained as a result of the rated flow. The relationship between first thumbwheel setting and flow rating follows. The corresponding probe diameters (not yet determined) will be about as indicated below:

First Thumbwheel setting	Maximum average flow indication (liters/minute)	Estimated probe diameters (mm)
9	10.0	12.0
8	5.0	9.5
7	2.0	7.0
6	1.0	5.0
5	0.5	3.7
4	0.2	2.7
3	0.1	2.0
2	0.0	—
1	0.0	—
0	0.0	—

If there is any appreciable bias in the flow or volume indication, as a result of drift in the system, it will be revealed by a non-zero indication in the ZERO position of the master switch.

If there is any appreciable error in flow measurement anywhere in the Flowmeter system except the probe it will be revealed by an indication other than 1.000 in the ONE position.

In the CALIBRATE RECORDER position of the master switch the dial of the same name may be used to simulate any average flow up to the rated maximum. At the maximum clockwise setting of the dial, there will be -1.000 volts at the Instantaneous Flow jack and +10.00 volts at the Average Flow jack.

<u>To completely test and operate the system, proceed as follows</u>:

1. Install probe.
2. Dial in probe code number.
3. Turn on.
4. Check ZERO.*
5. Check ONE.
6. (Optional) Set up external recorders using CALIBRATE RECORDER switch position and dial.
7. Read FLOW (and/or record Instantaneous and/or Average Flow).** Reverse DIRECTION switch if necessary.
8. Switch Indicator to TIME.
9. Flip integrator switch from RESET to OPERATE.
10. At any time not to exceed one minute flip integrator switch from OPERATE to HOLD.
11. Note time.
12. Read VOLUME.

The integrators may be tested as follows:

a. Flip integrator switch from RESET to HOLD.
b. Observe VOLUME and TIME after one minute. Return switch to reset.
c. Set master switch to CALIBRATE RECORDER.
d. Set CALIBRATE RECORDER dial to maximum clockwise.

---

* If the master switch position is marked by a red dot, the reading may be hastened by pressing the RAPID AVERAGE button which is also red.

** Recording may be done uninterruptedly in any of the first three positions of the master switch.

e. Flip integrator switch from RESET to OPERATE, and at the end of one minute,* to HOLD.

f. Read 1.000 for TIME.

g. Read (rated maximum average flow for probe) × (TIME) = VOLUME

To maximize common-mode signal rejection, switch to position 7.** Adjust CMR control on top of First Amplifier for minimum indication. The rejection ratio is approximately 10,000/Indication.

To check artifact rejection, switch to position 8. There is no adjustment. The error voltage is to be compared with the maximum average flow (full scale) value of 10.0 volts.

If the indication is non-zero in position 9, the power supply voltages should be checked. Remove top from Voltmeter. Connect input terminal to power supply test jack. Switch Voltmeter from NORMAL to + or - to read voltage. Adjust where necessary if control is present. Switch back to NORMAL.

To zero demodulator and DC amplifier system set master switch to 10. Adjust α on Instantaneous-Flow Amplifier for zero. Switch to 11. Set $\beta-\alpha$ on same Amplifier for zero. Switch to ZERO. Adjust Zero control on top of Average-Flow Amplifier for zero indication.

In position 12 set Minimum Current control on the Trapezoid Generator for minimum indication.

If any of the following positions give a non-zero indication make the corresponding adjustments.

---

* Use stopwatch or other timepiece with a sweep second hand.

** The green digit indicates that the DIRECTION switch may be used to reverse the reading.

Position of master switch	If non-zero indication connect voltmeter to	Adjustment
14	First Amplifier	Zero control on end (accessible through hole in front panel)
15	Second Amplifier	None
16	Compensator	Drift control (Wait several minutes)
17	Third Amplifier	None

E. POWER SUPPLY SYSTEM

1. Unregulated DC Power Sources

There are four DC power systems shown in Fig. 31, which are transformer-coupled to the 115 volt 60 cycle power line. One of these (F4; T1; etc.) is a part of the Voltmeter-Indicator described in Appendix B. A second (F3; T2) supplies +70 VDC (CR1,4; R1; C1) and -70 VDC (CR2,3; R2; C2) to flowmeter circuits and the 60 Volt Regulators (Sec. III-E.2). It also provides the two floating 14 VDC sources (CR5,6; C3,4) (CR7,8; C5,6) essential to the operation of the Regulators. These are "stacked" upon the regulator outputs and one such stack (+74) is used as a source for the OVERLOAD INDICATOR. A third (F1; T3) is analogous to the second, supplying +40 VDC (CR9,12; R3; C7) and -40 VDC (CR10,11; R4; C8) to Flowmeter circuits and 30 Volt Regulators while supplying the latter with two floating 14 VDC sources (CR13,14; C9,10) (CR15,16; C11,12). A fourth (F2; T4,5) required two transformers to achieve the proper secondary voltage with commercially available components. It supplies +20 VDC (CR17,20; R5; C13) and -20 VDC (CR18,19; R6; C14) to Flowmeter circuits and the +10, -10 and -13.7 VDC Regulators which are of lower precision than

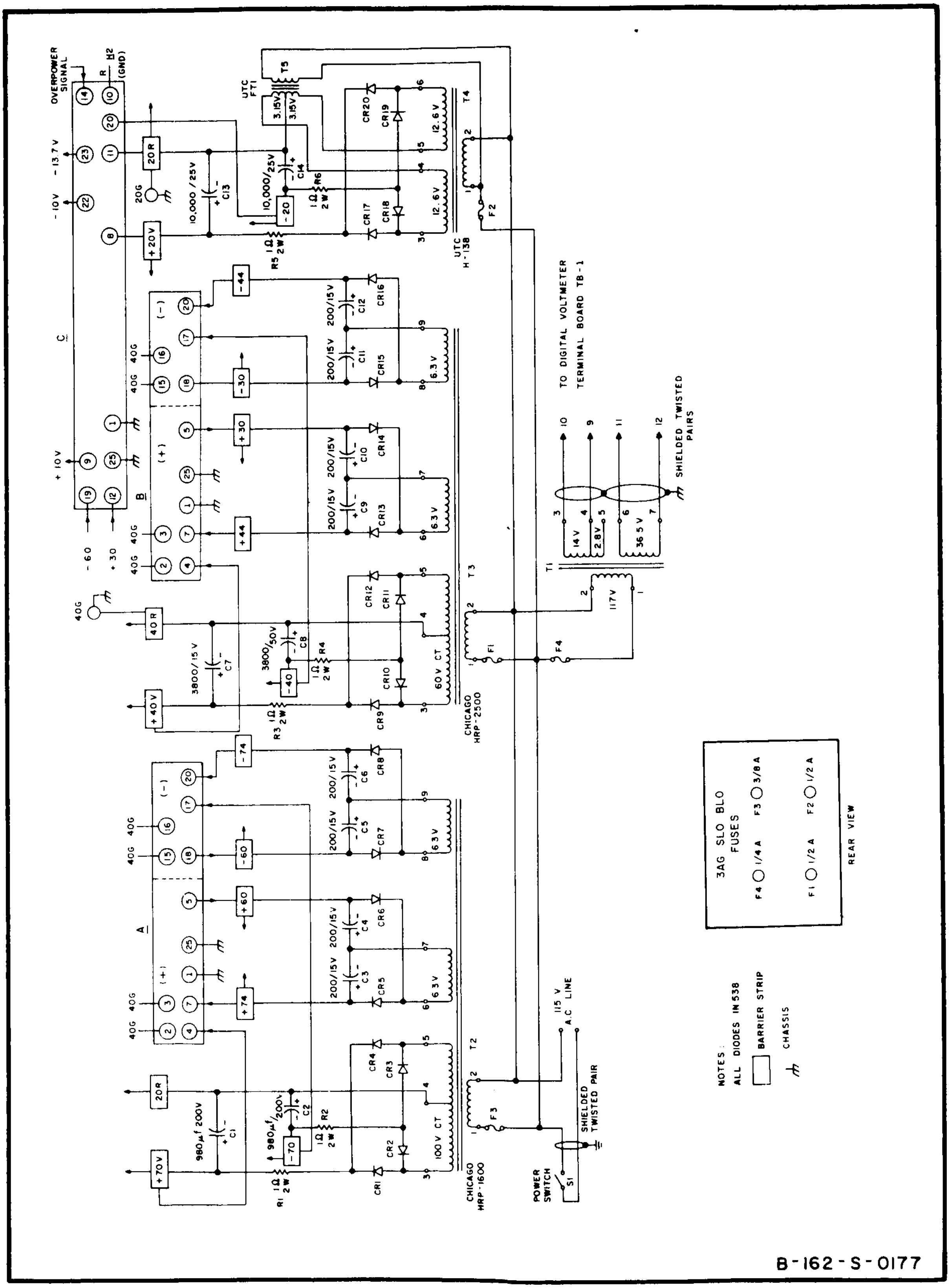


FIG. 31 UNREGULATED POWER SUPPLY CONNECTIONS

those mentioned above. All of these supplies are controlled by a single ON-OFF switch (S1). The actual unregulated voltages are 73, 43 and 22 VDC for an input voltage of 115 VAC.

2. Regulators

a. Regulators of High Precision

Each of the four high precision regulators, Figs. 32, 33, 34, 35, employs the same circuit configuration which will be described next. Regulation is accomplished by means of a series pass-transistor (Q1) which derives its base current from a double Darlington-connected current amplifier (Q4,5; R9,10,12,13). This amplifier is connected to the output of a difference amplifier (Q7,8; R20; R6; R5, 15) which compares a portion of the output determined by a resistive divider (R2,7,21) with a reference voltage determined by a temperature-compensated Zener diode (CR1) with one end connected to the regulated voltage and the other through a current fixing resistor (R19) to ground. The constancy of this current is an important factor in determining the output voltage stability. The DC gain of the difference amplifier is large by virtue of positive feedback (R17,18) which is adjusted to reduce the output resistance of the supply to such a small (positive) value that the no-load to full-load voltage change is less than 0.01%. The transient response (step-load excursion and recovery) is affected by a small capacitor (C4) shunting the positive feedback path: the difference amplifier provides a high speed relatively-low-gain amplification for rapid but imprecise transient response while as a result of low-pass ($\ll$ 3 KC) positive feedback slow but very precise recovery is ultimately achieved.

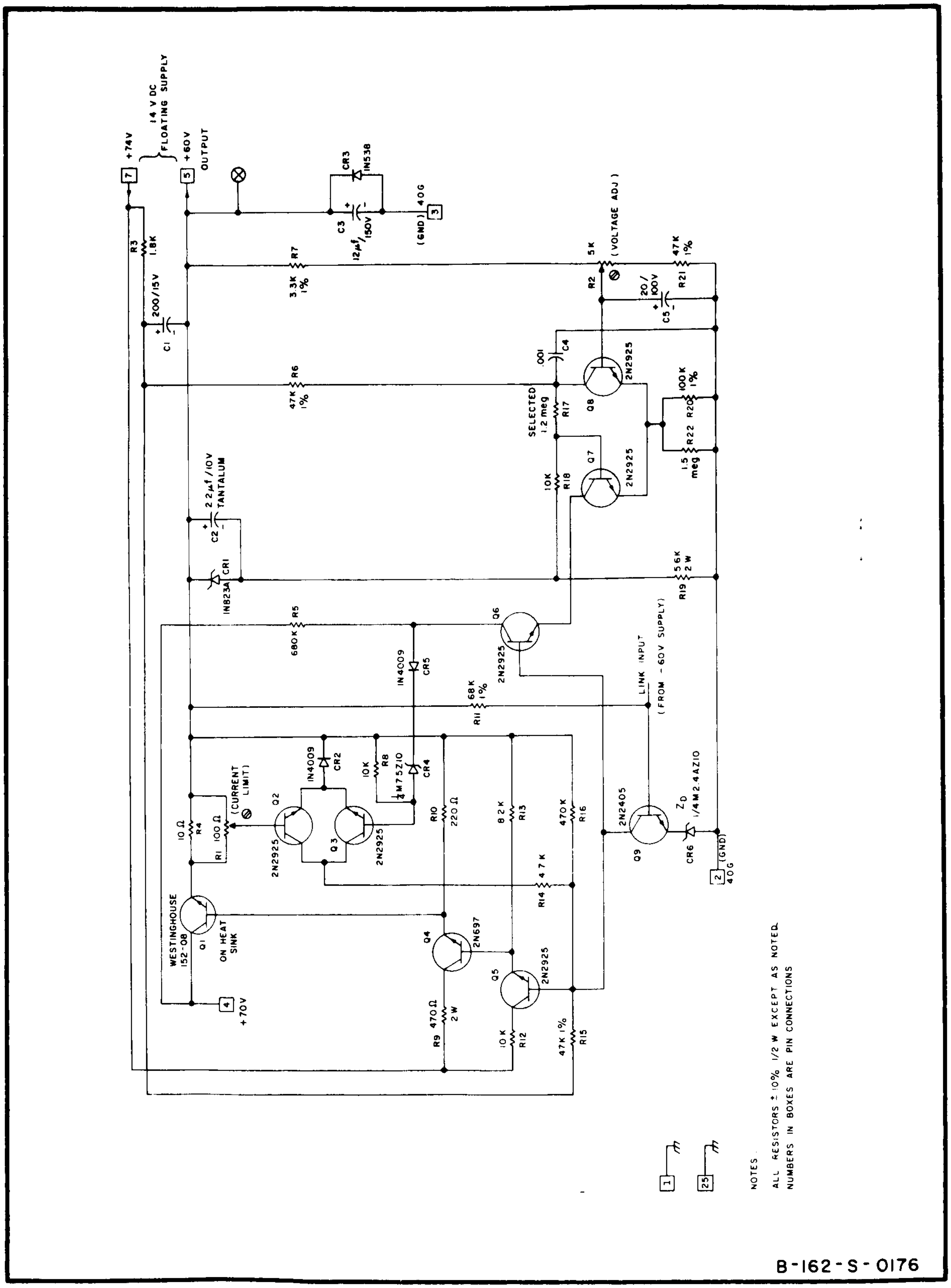


FIG. 32 +60V POWER SUPPLY REGULATOR , CODE 1,2 A

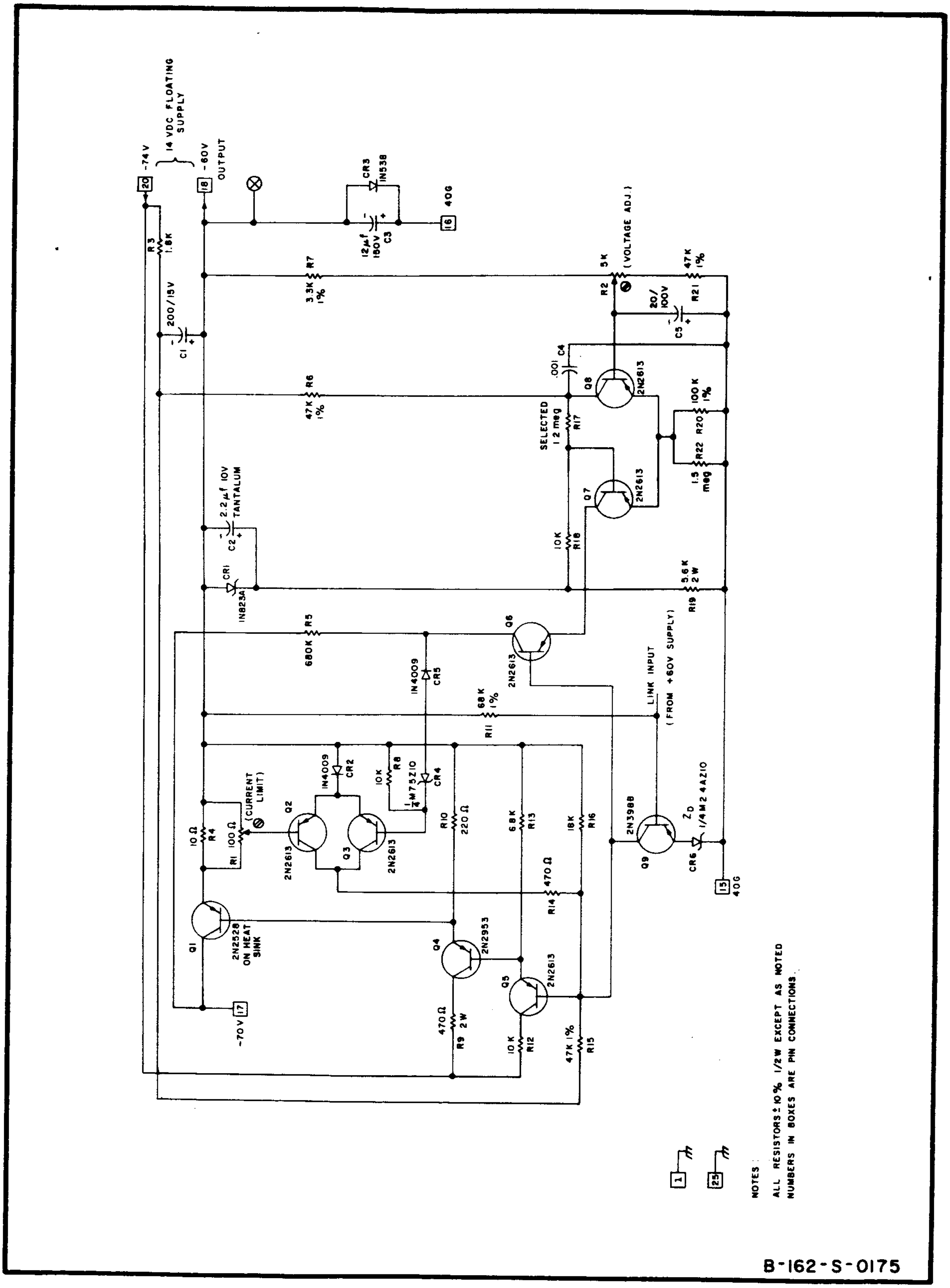


FIG. 33 -60V POWER SUPPLY REGULATOR, CODE 1,2 A

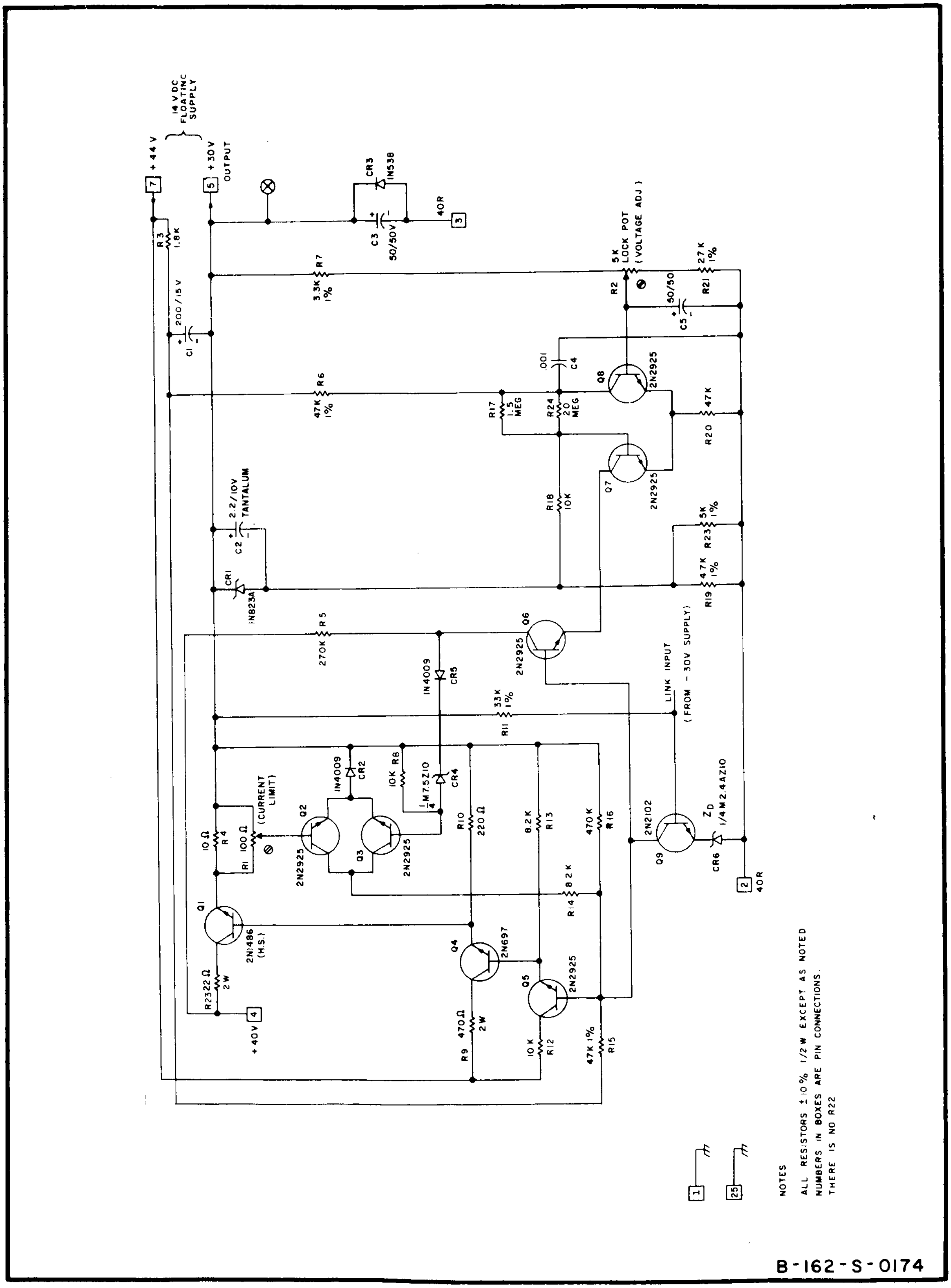


FIG. 34 +30V REGULATOR , CODE 1,4 B

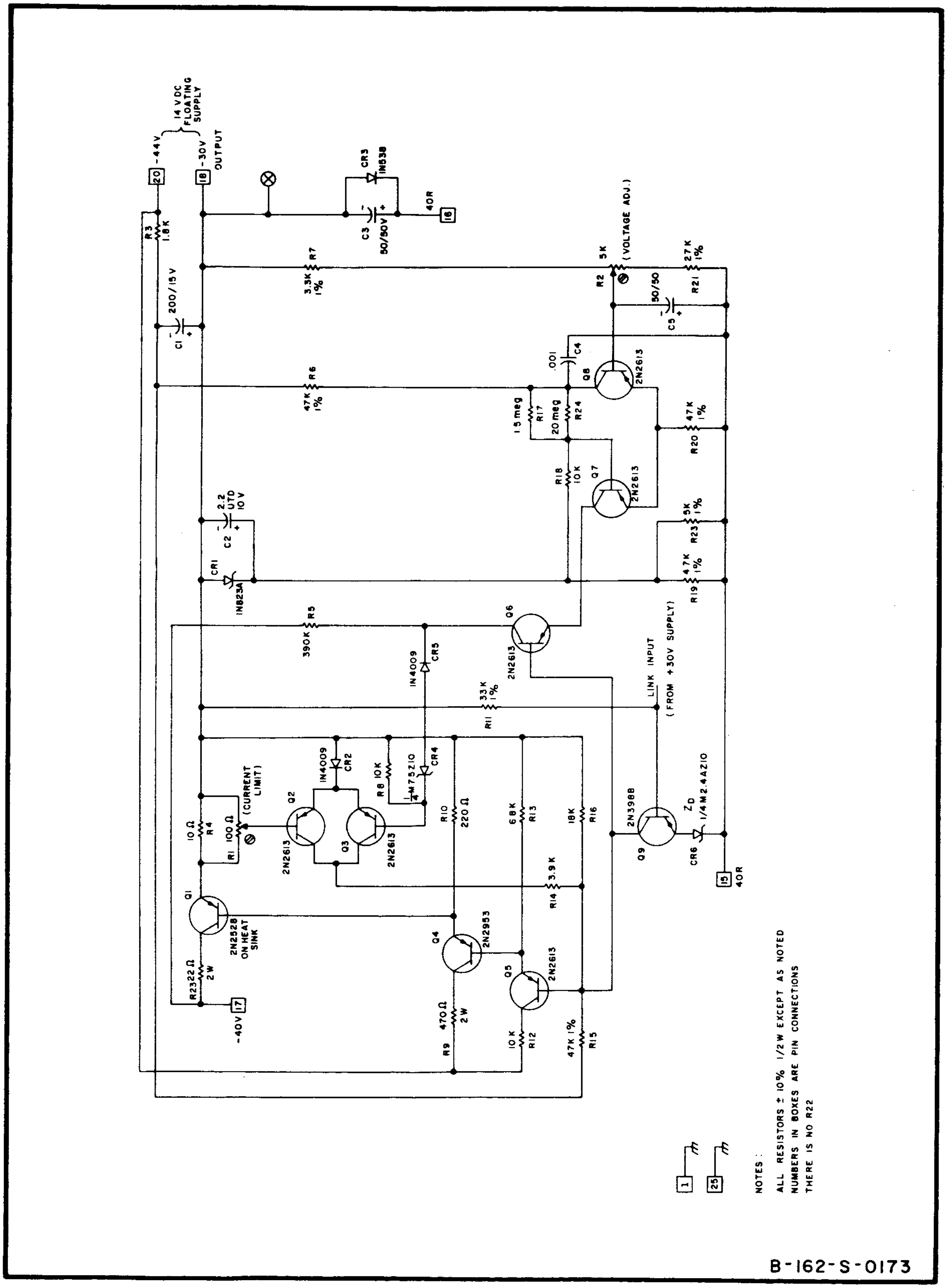


FIG. 35 -30V REGULATOR, CODE 1,4 B

A 14 VDC floating auxiliary supply (See Fig. 31), connected to the output, provides the offset voltage required to operate the difference amplifier and the Darlington amplifiers for the pass-transistor. Such an auxiliary supply overcomes two disadvantages of the more conventional arrangement in which auxiliary power is taken from the main unregulated power input. One advantage is that, under normal operating conditions, the difference between the floating supply voltage and the output voltage will vary only by the same percentage as the incoming line voltage. In the conventional arrangement the difference between the fixed output voltage and the main unregulated input voltage to the regulator is subject to much larger percentage variation, with the result that the operating points of all the transistors (except the pass transistor) are subject to very wide variations. Line voltage regulation is considerably improved by the use of a floating supply.

A second advantage is that under overload or short circuit conditions the floating supply keeps the transistor operating points fixed despite wide variations in output voltage (down to zero) which permits stable, predictable operation of the special overload protection circuitry described below. An RC filter (R 3;C 1) is introduced between the principal collector resistors (R 6,15) of the difference amplifier and the auxiliary supply. This is to reduce the 120 cps ripple voltage at the Regulator output.

There are three separate protective systems in each regulator to protect both the regulator and the load circuits from damage under abnormal operating conditions. The first of these systems is a current limiter. This is designed to limit output current to such a value that neither the pass-transistor nor the external circuits may be damaged. A 10 ohm resistor (R 4) in series with the emitter of the pass-transistor (Q 1) provides a voltage drop proportional to output current. Since this current sensing resistor is inside the voltage feedback loop it does not raise the output resistance of the regulator appreciably. A portion of the voltage derived from the current-sensing resistor determined by a potentiometer (R 1) is applied across a series circuit consisting of the base-emitter junction of a transistor (Q 2) and a silicon diode (CR 2) used to provide a voltage-current characteristic which has a sharper knee than that of the transistor junction alone.

When the sensed voltage (i.e.,output current) reaches the value required to overcome the sum of the transistor (Q 2) base-emitter and diode turn-on barrier voltages, base current begins to flow in the base-emitter circuit and therefore in the collector circuit. The collector current flows in the base circuit of the first Darlington amplifier (Q 5;R 15,16) through a resistor (R 14) thus reducing the output current available. Any increase in output current sharply increases the current to the limiter transistor (Q 2) due to the nonlinearity in the base current/base voltage curve. Furthermore, the base current for the first Darlington is supplied by a constant 14 V source through a resistor (R 15) in which the current does not change as the output voltage falls toward zero. Therefore, the current limiting action is quite sharp despite the simplicity of the limiter.

At the onset of current limiting, the difference amplifier (Q 7,8, etc.) tends to compensate for any decrease in output voltage and, because of its high gain, rapidly cuts off the side (Q 7) that is connected to the first Darlington. The loss of collector current on one side (Q 7) of the difference amplifier is sensed by another transistor (Q 6) with its base-emitter junction in series with this (Q 7) collector. The collector of this other transistor (Q 6) is connected to a resistor (R 5) with its other end connected to the unregulated DC input to the regulator. Under normal operating conditions this transistor is saturated and this resistor (R 5) is simply part of the collector load of the difference amplifier. However, when current limiting results in loss of collector current on one side of the difference amplifier this other transistor cuts off, and its collector resistor (R 5) can supply current through a Zener diode (CR 4) to a transistor (Q 3) in parallel with the current limiter transistor (Q 2). The Zener diode is used to insure that actual cutoff has occurred before the transistor (Q 3) paralleling the normal current limiter (Q 2) begins to operate. A conventional diode (CR 5) in series with the Zener diode prevents current flow in the reverse direction to the one described under normal operating conditions.

The composite current limiter described above has two different sources of base current to two different transistors, either of which can subtract base current from the first Darlington amplifier and thus reduce the output current capability. Since the second such circuit draws this current from the unregulated input source the current available rises as the difference between regulator input and output voltage increases i.e., as the output voltage drops due to overload. Thus under increasing overload, the current limiting which gives rise to the E/I characteristic shown in Fig. 36(A), gives way to current limiting of a type shown in Fig. 36(B), in which the output current decreases as the output voltage decreases.

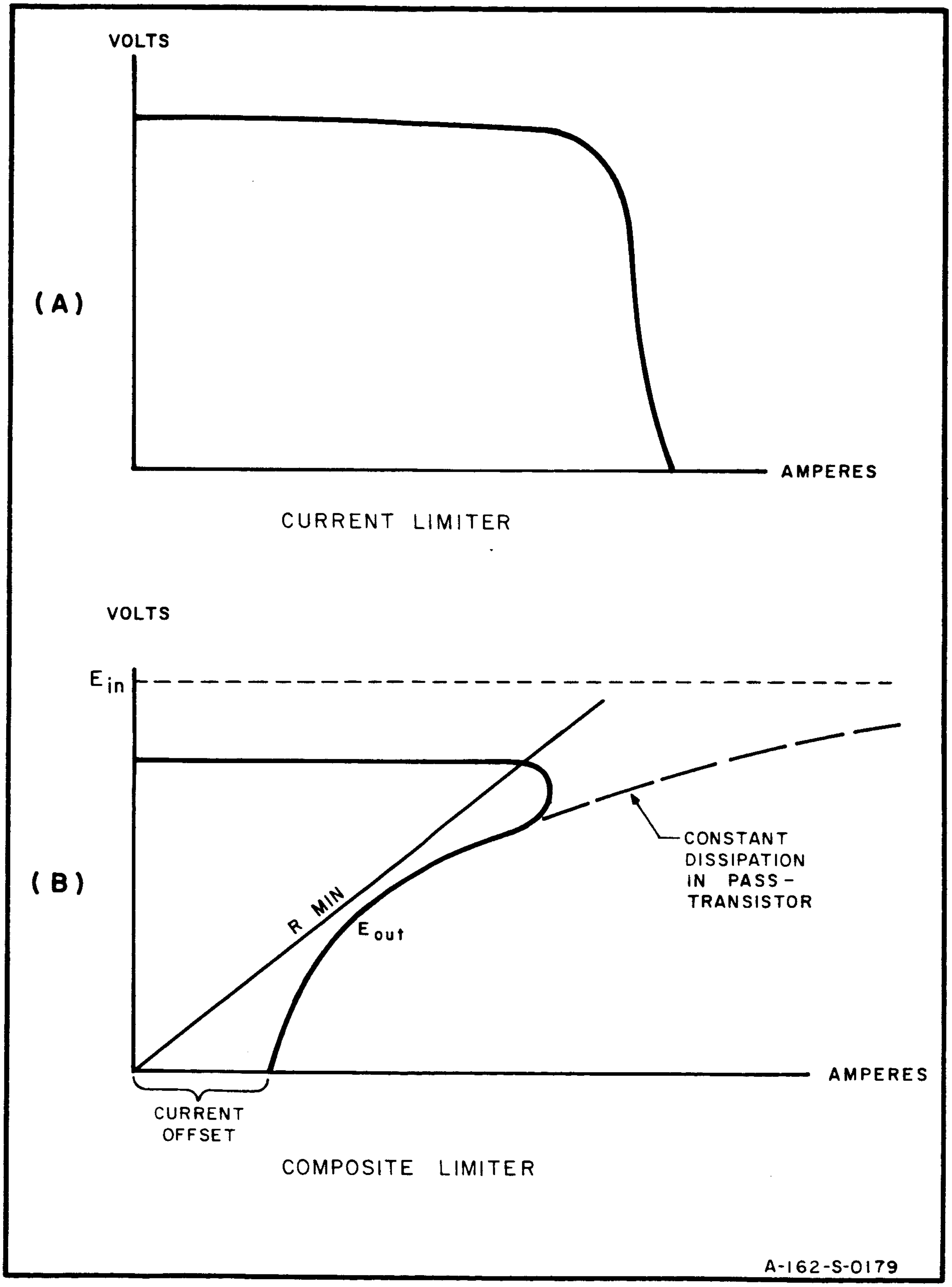


FIG. 36 REGULATOR CURRENT-LIMITER TRAJECTORIES

The operation of the second current limiter in reducing the output current as the output voltage drops results in the first current limiter rapidly dropping out of operation. The second current limiter draws a base current which increases rapidly as the output voltage drops. This rate is roughly controlled by the resistor (R 5) supplying base current (the transistor current gain and its variation with current also affect the shape of the curve).

The use of two different transistors for the two current limiting systems is a practical convenience. While one transistor would operate, receiving base current from two different sources, the great difference in source impedance of the two networks would require isolating diodes. Two transistors provide isolation more simply and provide smoother operation than a conventional current limiter.

The pass-transistor dissipation equals output current times,the difference between unregulated input voltage and regulator output voltage. Given a fixed input voltage, (which for safety's sake is chosen to be the input voltage at maximum permissible line voltage),the E/I output curve which gives a constant dissipation (equal to the dissipation for maximum rated output current) is a hyperbola ($E \times I = W$, a constant, where $E = E_{in} - E_{out}$). This hyperbola ideally intersects the zero voltage axis at $I = W/E_{in}$. It is highly desirable that the regulator provide some current across a short circuit to insure the ability of the system to start up under capacitive loading. The auxiliary (hyperbolic) current limiter (Q 3) is normally driven to saturation to prevent the effects of temperature on current gain from altering the selected short circuit current. The short circuit output current is set by adjusting the value of the resistor (R 14) between the current limiter common collector point and the base of the first Darlington amplifier, (Q 5), thus limiting the total amount of base current which can be removed.

The selection of the shut-down trajectory and the short-circuit current must, in addition, satisfy one important requirement. A load line drawn through the origin and representing the minimum rated load resistance must not intersect the approximately hyperbolic shut down curve. If this should happen, the lower intersection point would represent a stable state alternate to the desired state and on the removal of a short circuit the supply would "latch up" at this alternate stable point, rather than reset fully.

One final current path exists at the base of the first Darlington amplifier. A transistor (Q 9) is connected between this point and the power supply return line through a Zener diode (CR 6). The base of this transistor is connected to the analogous point in the regulator of the same voltage but opposite polarity. This links the regulators together so that if one in a pair shuts down so does the other.

As long as both voltages in either pair have nearly the same magnitude the common point is near ground potential and the transistor (Q 9) is cut off. If, however, one of the output voltages is reduced, by regulator malfunction or external overload, the transistor associated with the other supply of the pair is biased in the forward direction and draws current from the base of the first Darlington amplifier. This reduces the regulator output and prevents the difference in voltage magnitudes from exceeding a fixed amount (dead band). These (Q 9) transistors reduce the voltage applied to any stage to the extent that its bias decreases. The external circuits are designed to use the ±30 V and ±60 VDC regulator outputs as pairs with one line providing power; the same voltage of opposite polarity providing bias. If this were not the case a more complicated intercomparison technique would be required for complete protection.

In practice a dead-band is desirable, that is, a finite error band over which the shutdown circuit does not operate. A dead-band of almost three volts is provided by the addition of a 2.4 V Zener diode in series with the emitter of the adder transistor. This is convenient in practice for two reasons. Given a moderate dead band the output voltage of either regulator in a pair is independently adjustable under normal operating conditions. Under overload the supply actually overloaded is noticeably lower than the paired supply, simplifying trouble shooting.

The precision regulators are usually set within ±0.5 V of the nominal output value. Current limiting is set for approximately 200 ma for the ±30 V regulators, and 100 ma for the ±60 V regulators with the voltage fall rate and short circuit current adjusted to prevent latch-up. Short circuit current is on the order of 10% to 20% of maximum current. Transient overshoot is held to 100 mv or less. Response time is relatively slow, approximately 0.2 msec, due to the low cutoff frequency of the positive feedback loop of the difference amplifier, but the shunt capacitor (C 3) insures a low output impedance at high frequencies. Ripple and noise of the regulator output are less than 0.2 millivolts peak-to-peak.

A diode (CR 3) is shunted across the output of each regulator to prevent its terminal voltage from being reversed by other supplies in the event of its failure.

The temperature compensated Zener diode and a differential error amplifier combination provides a thermal coefficient estimated at about 0.01% per degree centigrade for slow changes in ambient temperature. Long term drift is not well established but previous experience indicates 1% per month initial aging with perhaps an improvement by a factor of 100 after several months of operation.

b. Regulators of Low Precision

Low voltage regulator circuits are shown in Fig. 37. The +10 VDC regulator consists of a two stage Darlington-connected emitter-follower (Q 6,7;R 1,2,3,4,6,8, 10,11) which supplies output current taken from the 20 VDC line at a voltage determined by a tap on a resistive divider (R 5,7,9;C 2) on the very precise ±30 VDC Regulator. The tap is connected to the input (Q 6) base. The double emitter-follower current gain renders the divider voltage essentially independant of load current. Series collector resistors (R 1,2,3,4,6) protect the transistors against damage in the event of short-circuit. A series resistor (R 8) protects the input base in this event. A shunt diode (CR4) prevents the output voltage from being reversed by other supplies should this supply fail.

The -10 VDC regulator is similar in form. The reference voltage is derived from a voltage divider (R 21,22,24;C 1) connected to the -60 VDC regulator.

The reference voltage for the -13.7 VDC regulator is also derived from the -60 VDC Regulator by means

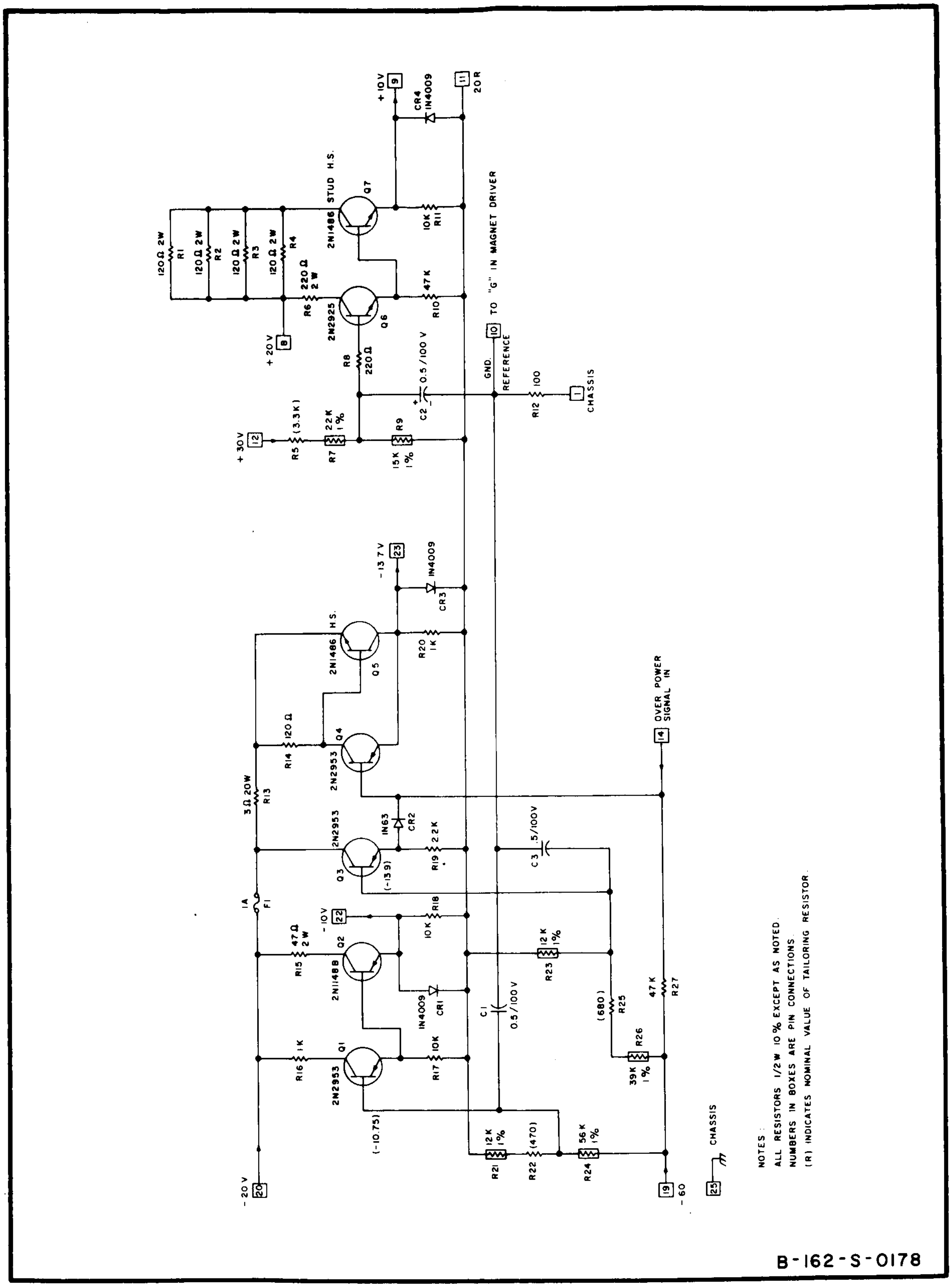


FIG. 37 LOW VOLTAGE REGULATORS , CODE 3,2 C

of another divider (R 23,25,26) and an emitter-follower (Q 3;R 19). The input base of the regulator input transistor (Q 4) is clamped through a diode (CR 2) to the reference emitter follower (Q 3) by current through a resister (R 27) to the -60 VDC. In the event of an overload condition the clamping current is overcome by a current (the overpower signal) from the Magnet Driver for which alone this regulator was built, and the terminal voltage drops immediately. The PNP - NPN pair of transistors (Q 4,5) protected by resistors (R 13,14) and a fuse (F 1) in their collector circuit and having a (14 ma) shunt load resistor (R 20) and anti-reversal diode (CR3) at its output will supply the 0.6 amperes required by the Magnet Driver output stage.

The most critical application of these low-voltage supplies is as a source for the Magnet Driver. The reference dividers are therefore by-passed to a neutral point (G in Figure 44) in this unit. In the event that this unit is removed for testing an adequate ground path is provided locally by means of a resistor (R 12).

F. GENERATION OF THE MAGNETIC FIELD

1. Review of the Transmitter Specifications

The probe electromagnet must be supplied with an alternating current of precisely controlled magnitude which remains very constant over a major portion of a half cycle. This is accomplished in the Flowmeter by generating a trapezoidal voltage and using this as the input to a feedback amplifier; the feedback being driven from the probe current. Since the electromagnet is essentially an inductor, the voltage at its terminals will take the form of rectangular pulses with a magnitude determined by the change in current, the inductance, and the slope of the trapezoid. The amplifier must have large bandwidth and voltage compliance to produce these pulses and must in addition be capable of large output current.

2. Trapezoid Generator

The schematic diagram for unit called the Trapezoid Generator is in Fig. 38. The trapezoidal voltage is generated by a feedback amplifier in response to a rectangular current input. The feedback network consists of a capacitor (C 2) and a voltage limiter (CR 1,2) in parallel. The current source in this case consists of a diode current bridge (CR 3, 4,5,6; R 11,30). The reference terminal of the bridge is connected to what is essentially the summing junction of the feedback amplifier. The input to the bridge is a ±2.5 V square wave from the Time Logic generator. When the input is positive a current determined by +30 VDC and the series resistor (R 11) flows into the summing junction. When the input is negative an identical current flows out of the summing junction. When the current reverses the output voltage progresses linearly from one limit value to the other at a rate determined by the input current and the feedback capacitor (C 2). When the limit is reached all of the current flows in the reference diode that does the limiting. The current chosen is that for which the temperature coeficient of the reference diode is less than 50 part per million per degree C^{o}. The other reference diode does not conduct in the reverse direction because, fortunately, these diodes are composite.

The junction of the reference diodes (CR 1,2) and the current bridge may be called the summing junction for the feedback amplifier. However, the input base for the amplifier is offset negatively by about 7 volts as a result

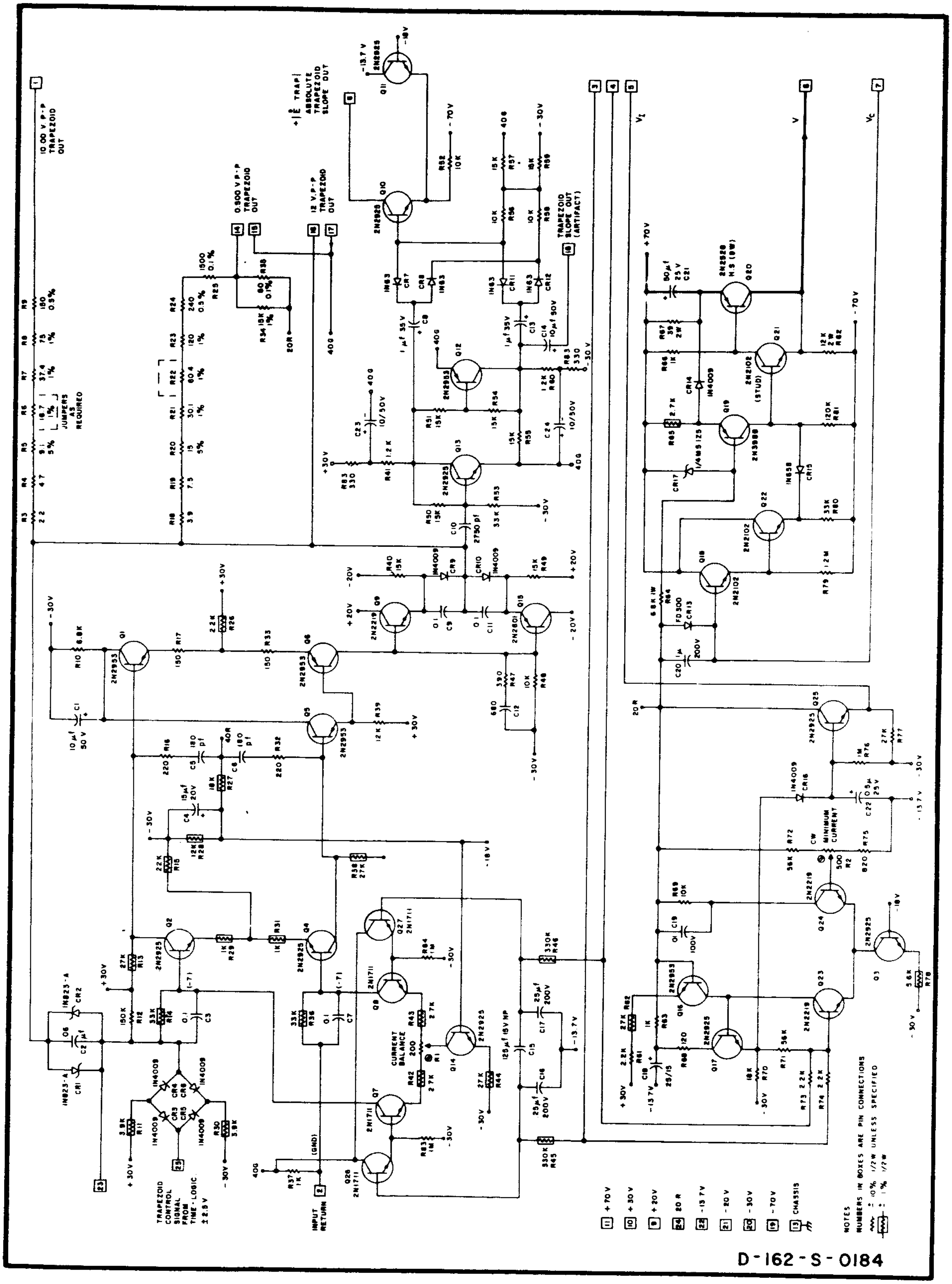


FIG. 38 TRAPEZOID GENERATOR , CODE 5,6 G

of current flowing in a series resistor (R 14) which is bypassed (C 3), and the reference base is similarly offset (R 36;C 7). The offsetting currents come from a difference amplifier (Q 7,8) which responds to the unbalance current in the output transformer of the Magnet Driver. A voltage proportional to this unbalance current reaches the bases of the difference amplifier (Q 7,8) through a low pass filter (R 45,46;C 15,16,17) and a pair of emitter followers (Q 26, 27;R 83,84). The individual emitter resistances (R42,43) meet at the Driver Amplifier CURRENT BALANCE CONTROL (R 1). The reference voltage (-18 VDC) for the common-emitter constant-current source (Q14;R 44) comes from a divider (R 27,28;C 4) on the -30 VDC supply. This divider is also connected to other circuit points. The current for one side of the balancing circuit comes through a resistor (R 12) from the +30 VDC supply. This prevents the trapezoid slopes from being dissimilar. The current for the other side comes from a neutral point in the magnet driver through terminal $\boxed{2}$. An alternate path is provided through a resistor (R 37) to ground so that this circuit is operable should the magnet driver not be plugged in. The voltage gain of the filter-amplifier is about 10.

Emitter resistors (R29,31) are also used to raise the input resistance of the first stage (Q 2,4) of the feedback amplifier. These return to -30 VDC through a common resistor (R 15) which was chosen along with the collector resistors (R 13,38) to provide an average collector voltage of +17 volts.

One half of the second stage (Q 1;R 10,17;C 1) is driven directly. The other half (Q 6;R 33,48) is driven by means of an emitter follower (Q 5;R 39). This arrangement keeps to a minimum the reactive loading of the first stage.

Complementary emitter followers (Q9,15) are used at the output of this amplifier because they are highly efficient. These must produce a ±6.2 volt trapezoidal signal across a resistive load of about 750 ohms. They must also supply the feedback current which changes almost instantaneously from 7.5ma in one direction to 7.5ma in the other direction. If they were connected conventionally one would be cut off while the other is conducting. Because of the inevitable signal delay in the amplifier a sudden jump in feedback current would introduce that voltage jump at the output necessary to throw the other emitter follower into conduction. The output waveform would then have a section of very great slope at the beginning of each transition. The voltage induced in the probe electromagnet as a result of this step would surely exceed the compliance of the Magnet Driver. Such an output step in the present instance is avoided by utilizing the time during which the output voltage is constant to bring the "off" emitter follower into conduction. If the output is positive, one transistor (Q 9) supplies the output current through a diode (CR 9) while the other (Q 15) is brought into conduction by charging the capacitor (C 11), by means of which its emitter is connected to the output, through a resistor (R 49) connected to the positive supply. For a negative output, during which the other transistor (Q 15) is conducting through its diode (CR 10), the first transistor (Q 9) is brought into conduction by a similar mechanism (C 9;R 40).

The open-loop gain of the amplifier is 54db. The feedback factor in this application is unity when one of the reference diodes (CR 1,2) is conducting and decreases at 20db/decade below 670 cps when neither is conducting because of the slope-determining circuit (C 2;R 11 or R 30).

The first-stage networks (R 13,16;C 5)(R 32,38;C 6) establish a single slope from 33kc to 4Mc and the second-stage network (R 47,48;C 12) establishes another from 33kc to 600kc. The overall result is shown in Figure 39.

There is DC gain from the output of the Trapezoid Generator to the final stage of the Magnet Driver. The purpose of the current balance servo (Q 7,8) is to cause the trapezoidal voltage to be generated with that small average voltage necessary to maintain an average current of zero in the magnet driver output transformer. It must do this despite the fact that each of the reference diodes (CR 1,2) in the trapezoid generator has a ±10 per cent voltage tolerance. The servo was placed at the beginning of the trapezoid generator for two reasons: first,this is a convenient point to obtain that high impedence level below which the low-pass filter (R 45,46;C 15) would be impracticable. Second, it takes advantage of the voltage gain and stabilizes the operating points of the first three stages of the Magnet Driver. The impedence level of these stages is necessarily quite low because the bandwidth required of them is large.

The trapezoidal voltage goes to four different places. It goes to the 1000 ohm precision input resistor for the magnet driver through a set of seven series resistors (R 3-9) having resistance ratios which are to each other as powers of 2. By appropriately short-circuiting the unneeded resistors the peak-to-peak voltage at the input resistor may be set to within ± 1/10 of a per cent of 10.00 volts, provided only that the reference diode (CR 1,2) voltages are within their tolerance. (The largest values of compensating resistance require the smallest tolerance.) Another output through set of binary resistors (R 18-24)

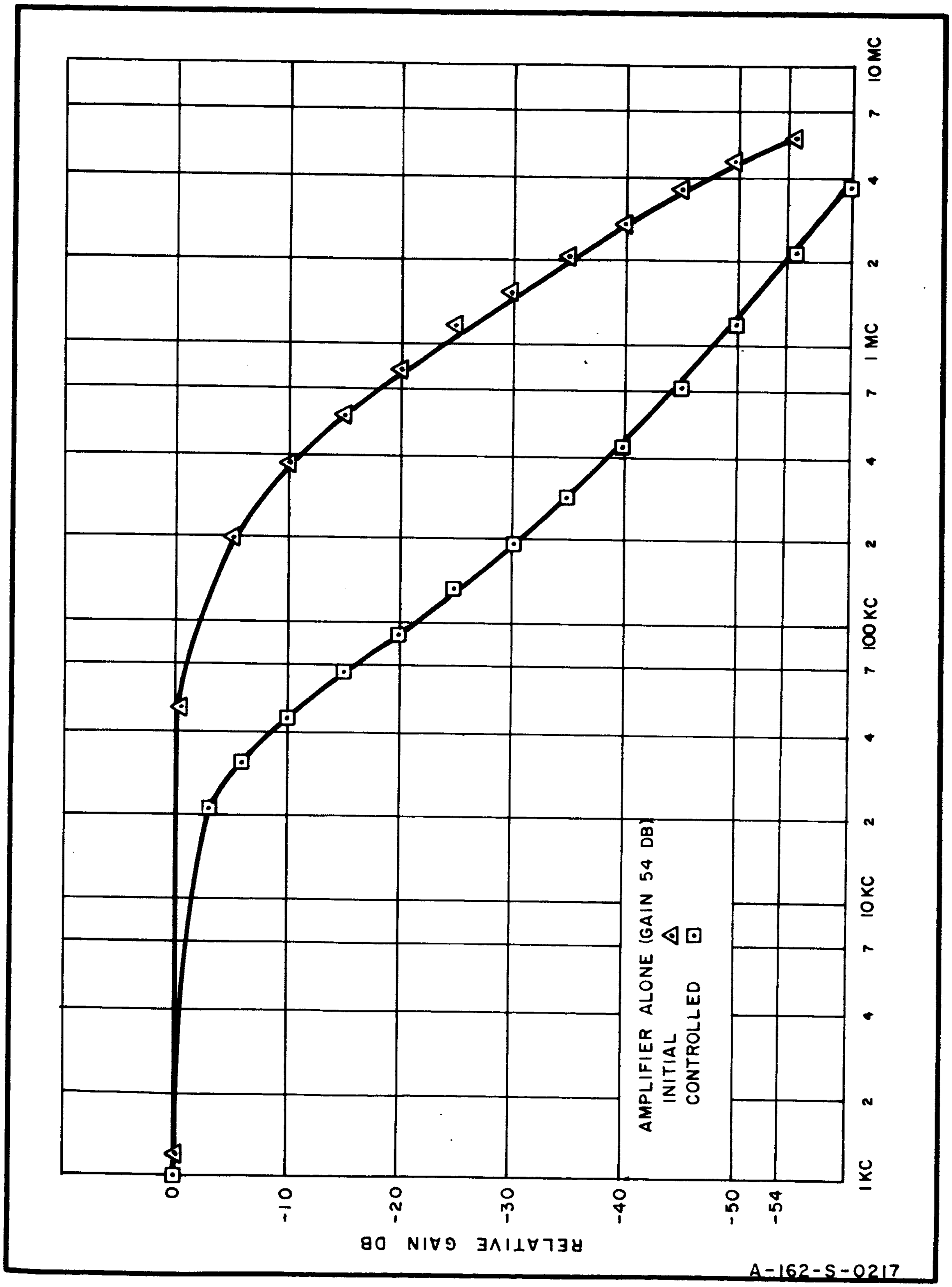


FIG. 39 TRAPEZOID GENERATOR AMPLIFIER FREQUENCY RESPONSE

enables the voltage on a divider (R 25,34,35) to be set so that a trapezoid of 0.500 volts peak-to-peak appears across a ten-turn linear potentiometer (on the Flowmeter front panel)which may be used to simulate the flow signal which would result from any given amount of flow in a given probe. Thus it is possible to make appropriate gain adjustments in external equipment connected to the Instantaneous Flow or Average Flow output of the Flowmeter. (This potentiometer is shown as R 79 in Fig. 30.) A third output may be switched through an attenuator to both inputs of the First Amplifier. The C.M.R. control in this amplifier enables the response of the Flowmeter to a large common mode signal to be set to zero. A fourth output is connected to a differentiator (Q 13;R 41,50,53;C 10). The differentiated output is connected through a capacitor (C 8) to a pair of rectifier diodes (CR 7,8). It is also connected to an inverter (Q 12; R 51,54,60) having an output circuit shunted by a resistance (R 55) identical to that of the differentiator load, and capacitively coupled (C 13) to another pair of rectifier diodes (CR 11, 12). The rectifiers are so connected as to produce at one output load resistor (R 56) negative pulses of magnitude proportional to that of the trapezoid slope; and at another (R 58), positive pulses of the same magnitude. After each pulse, each output returns to -15 VDC established by a divider (R 57,59) on the -30 VDC supply. The negative magnitude cuts off a current source (Q 10,R 52) during pulse-time. The current thus diverted is taken up by a transistor (Q 11) with its base connected to the -18 VDC divider (R27, 28;C 4). The current source is connected through connector pin $\boxed{6}$ to the Magnet Driver where it determines the time during which certain output transistors may be driven into conduction. The derivative signal at the inverter (Q 12) output is coupled by means of a capacitor (C 14) through a switch and some pulse-forming circuits to one input of the First Amplifier. This enables the Flowmeter to be tested for its immunity to very large spike inputs. The remaining circuits in Fig. 38 pertain directly to the Magnet Driver and will be discussed in that connection.

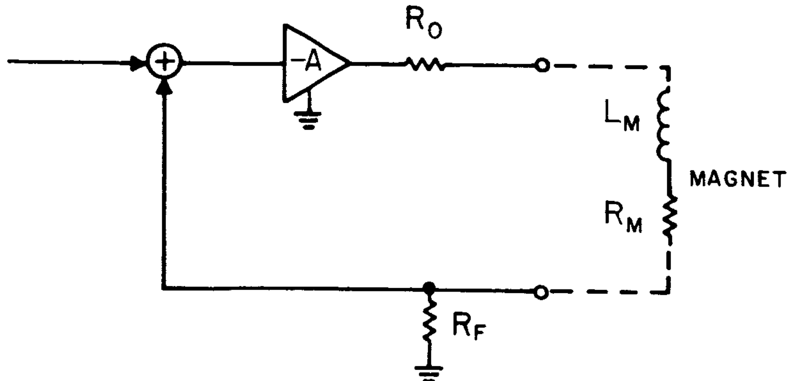
3. <u>Magnet Driver Networks</u>

The Magnet Driver is required to establish a current of 0.5 ampere ±0.1% in the probe electromagnet within a few microseconds of the time that the trapezoidal input voltage attains its constant value in either direction. If a magnet driver has an output resistance of R_o ohms and the electromagnet inductance is L_m henries, then the time-constant of the electromagnet circuit is

$$= \frac{L_m}{R_o + R_m}$$

where R_m is the magnet resistance. For a time-constant of one microsecond and the design-maximum inductance of five millihenries, $R_o = 5K$ ohms. The driver is then equivalent to a 2500 volt generator with this internal resistance. Both the high equivalent resistance and the high precision are attainable by means of a feedback amplifier.

A suitable configuration is shown below



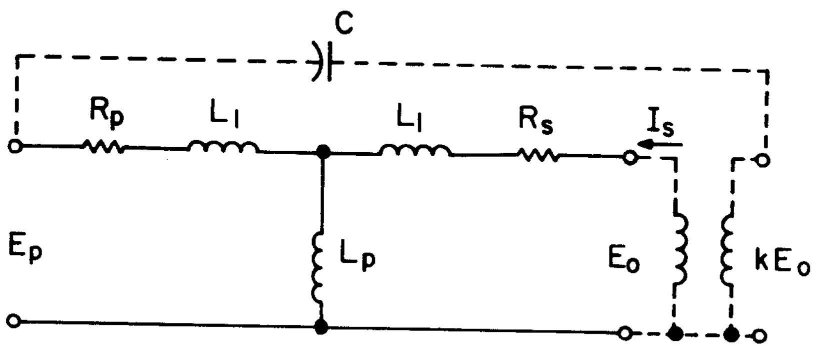
The amplifier output resistance R_o is shown explicitly. A low resistance R_f in series with the magnet is used to provide a feedback voltage proportional to magnet current. The impedance Z presented to the magnet is given by

$$Z = R_o + (1 + A)R_f \quad .$$

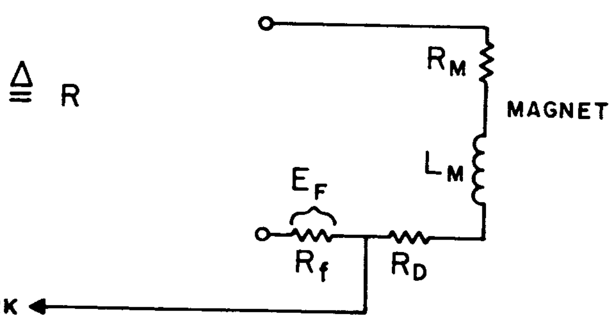
(This can be derived by replacing the magnet by a one volt source and examining the resulting current.) Because the efficiency of the driver improves as R_f is reduced, R_f should be less than the magnet resistance R_m. The achievement of a high effective R_o is complicated by the fact that in practice an amplifier output transformer is required, so the problem is essentially that of stabilizing a transformer coupled feedback amplifier with a loop gain of about 5000.

The advantages of transformer coupling are that the probe electromagnet may be isolated from the high voltage DC supplies, which the driver output stage requires, and that two connecting wires suffice to provide an output voltage which can be balanced with respect to ground by simply splitting the secondary winding. Balancing helps to minimize coupling of the magnet drive signal into the electrode circuit as a result of stray capacitance. The disadvantages are that the nonlinearity (saturability) of amplitude response and the complexity of frequency response of transformers greatly complicate the task of achieving good stability in a wide-band feedback amplifier. The overall Magnet Driver response that was sought may be found by looking ahead to Figure 43.

In preliminary experiments with high-quality audio transformers (UTC A-20, A-28) it was found that shunt resistance would be necessary to damp out a variety of high-frequency resonances. This necessary external resistance therefore obviates the need for the usual shunt resistance in the transformer equivalent circuit. The equivalent circuits used are shown below.



$$R_S + R_M + R_D + R_f \triangleq R$$



The first question to be settled was whether or not the transformer phase shift could be determined from its amplitude-frequency response, because phase shift is much more difficult to measure than amplitude at the highest frequencies of interest (10 Mc). The phase can be determined if all of the zeros of transmission are located in the left half-plane. Such may not be the case if there is capacitance from primary to secondary, for in the current equation for the input node of the circuit given above,

$$-I_p + (E_1 - E_0)\,Y_{21} + (E_1 - kE_0)Cs = 0$$

$$(Y_{21} + Cs)E_1 - (Y_{21} + kCs)E_0 = I_p \quad ,$$

where the admittance parameters are those of the T section of the transformer equivalent circuit, the transfer admittance

$$y_{21} = -\,(Y_{21} + kCs)$$

may have a zero for $Re(s)$ positive if k happens to be negative. In the transformer that was wound for this purpose primary-secondary capacitance was eliminated by shielding the primary winding from the core by means of the outermost core laminations and additional pieces of insulated shim stock, all connected together at one point.

The C-I type core from a UTC A-20 transformer (the core chosen for the ease with which it could be assembled) was tested by applying a low frequency (60 cps) primary current and observing secondary voltage. With a primary inductance of 120 mhy distortion was not severe for primary current less than 0.1 amp. The magnetizing current is equivalent to the current in L_p of the equivalent circuit. With a probe connected and a secondary current which is trapezoidal, the current in L_p builds up monotonically during each half cycle. Since the trapezoid has a constant slope, the secondary current waveform becomes more nearly square as the repetition period is increased. To determine the magnetizing current which results at the end of a long period it is sufficient to examine the ratio of primary to (known) secondary currents when the secondary current is a step. The currents are in the inverse ratio of their impedances:

$$\frac{I_p(s)}{I_s(s)} = \frac{(L_1 + L_m)s + R_s + R_m + R_D + R_f}{L_p s} = \frac{(L_1 + L_m)s + R}{L_p s} ,$$

substituting

$$I_s(s) = \frac{I_o}{s} ,$$

and transforming

$$i_p(t) = I_o \left[\frac{R}{L_p} t + \frac{L_1 + L_m}{L_p} \right] .$$

In the worst case the electromagnet resistance and inductance have their maximum values. Substituting,

$$R_m = 5 \qquad L_m = .005 \qquad I_o = 0.5$$

$$R_D^* = R_f = 1 \qquad R_s = 1.4 \qquad L_p = .122 \qquad L_1 = .0008$$

$$i_{p\ max} = 0.5 \left[\frac{8.4}{.12} t_{max} + \frac{.0058}{.12} \right] = 0.1 \quad \text{and}$$

$$t_{max} = \frac{0.2 - .048}{70} = .0022 .$$

* R_D was included so that the secondary current could be measured independently of R_f.

With this transformer the repetition rate should not be less than about 250 cps. The details of transformer construction are given in Figure 40.

Two properties of the loaded transformer are of interest. One is the impedance $\hat{Z}_{pt}$ looking into the primary (neglecting capacitance);

$$\hat{Z}_{pt} = \frac{L_p(2L_1 + L_m) + L_1 L_m + L_1^2}{L_p + L_1 + L_m} \times$$

$$\frac{S^2 + \dfrac{L_p(R_p + R) + L_1(R_p + R) + R_p L_m}{L_p(2L_1 + L_m) + L_1 L_m + L_1^2} S + \dfrac{R_p R}{L_p(2L_1 + L_m) + L_1 L_m + L_1^2}}{S + \dfrac{R}{L_p + L_1 + L_m}}$$

$$R = R_s + R_D + R_f + R_m \quad .$$

This is well approximated by:

$$Z_{pt} = \frac{2L_1 + L_m}{1 + L_m/L_p} \; \frac{S^2 + \dfrac{R_p + R}{2L_1 + L_m} S + \dfrac{R \; R_p/L_p}{2L_1 + L_m}}{S + \dfrac{R}{L_p + L_m}} =$$

$$\frac{2L_1 + L_m}{1 + L_m/L_p} \; \frac{(S + S_1)(S + S_7)}{S + S_3}$$

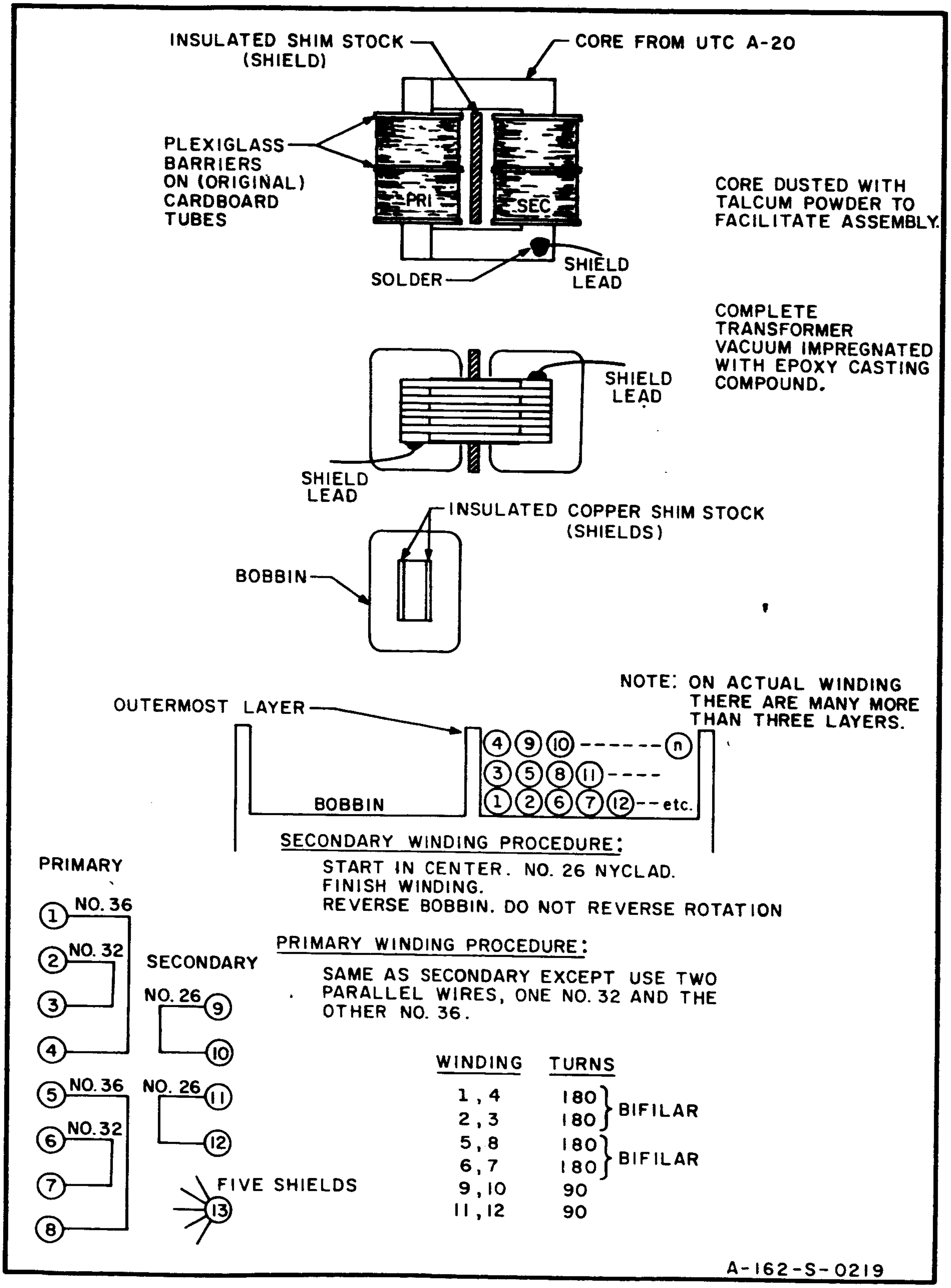


FIG. 40 OUTPUT TRANSFORMER CONSTRUCTION DETAILS

where, the zeros are approximately

$$S_7 = -\frac{R_p + R_s + R_D + R_f + R_m}{2L_1 + L_m}$$

$$S_1 = -\frac{(R_s + R_E + R_f + R_m)R_p/L_p}{2L_1 + L_m}\frac{1}{S_3} = \frac{R_p}{L_p}\frac{R_s + R_D + R_f + R_m}{R_p + R_s + R_D + R_f + R_m} .$$

The other is the voltage transfer ratio $\hat{T}_{21}$ between the voltage across the primary and the voltage across the feed-back or current sensing resistor R_f .

$$\hat{T}_{21} = \frac{E_f}{E_p} = \frac{L_pR_f}{L_p(2L_1 + L_m) + L_1L_m + L_1^2} \times$$

$$\frac{S}{S^2 + \frac{L_p(R_p + R) + L_1(R_p + R) + R_pL_m}{L_p(2L_1 + L_m) + L_1L_m + L_1^2} S + \frac{R_p\ R}{L_p(2L_1 + L_m) + L_1L_m + L_1^2}}$$

or, approximately,

$$T_{21} = \frac{R_f}{2L_1 + L_m}\ \frac{S}{(S + S_1)(S + S_7)} .$$

The ratio of feedback voltage to primary current is

$$Z_{pt}\ T_{12} = \frac{L_p\ R_f}{L_p + L_m}\ \frac{S}{S + \frac{R_s + R_E + R_f + R_m}{L_p + L_m}} .$$

Using actual transformer parameters,

$$R_p = 3.6$$

$$Z_{pt} = \frac{.0016 + L_m}{1 + 8.2\, L_m} \; \frac{(s + s_1)(s + s_7)}{s + s_3}$$

$$T_{21} = \frac{1}{.0016 + L_m} \; \frac{s}{(s + s_1)(s + s_7)}$$

$$Z_{pt}\, T_{21} = \frac{1}{1 + 8.2\, L_m} \; \frac{s}{s + s_3}$$

$$s_7 = - \frac{7 + R_m}{.0016 + L_m} \qquad s_3 = - \frac{3.4 + R_m}{.122 + L_m}$$

$$s_1 = - 30 \, \frac{3.4 + R_m}{7 + R_m}$$

L_m	R_m	s_1	s_3	s_7	$\frac{.0016 + L_m}{1 + 8.2\, L_m}$	$\frac{1}{.0016 + L_m}$
0	0	$2\pi 2.2$	$2\pi 4.5$	$2\pi 685$	.0016	625
.0022	3	$2\pi 2.8$	$2\pi 8.2$	$2\pi 420$	.0037	263
.005	5	$2\pi 3$	$2\pi 10$	$2\pi 276$	.0054	179

A Bode plot of $Z_{pt}\, T_{21}$ for an average probe is given in Figure 41. Also given is the desired low frequency response of the amplifier, and that of two lead networks which, in cascade with the output circuit, would effect the desired response. In what follows, the approximate manner in which the various networks contribute to the amplifier response (without overall feedback) will be outlined.

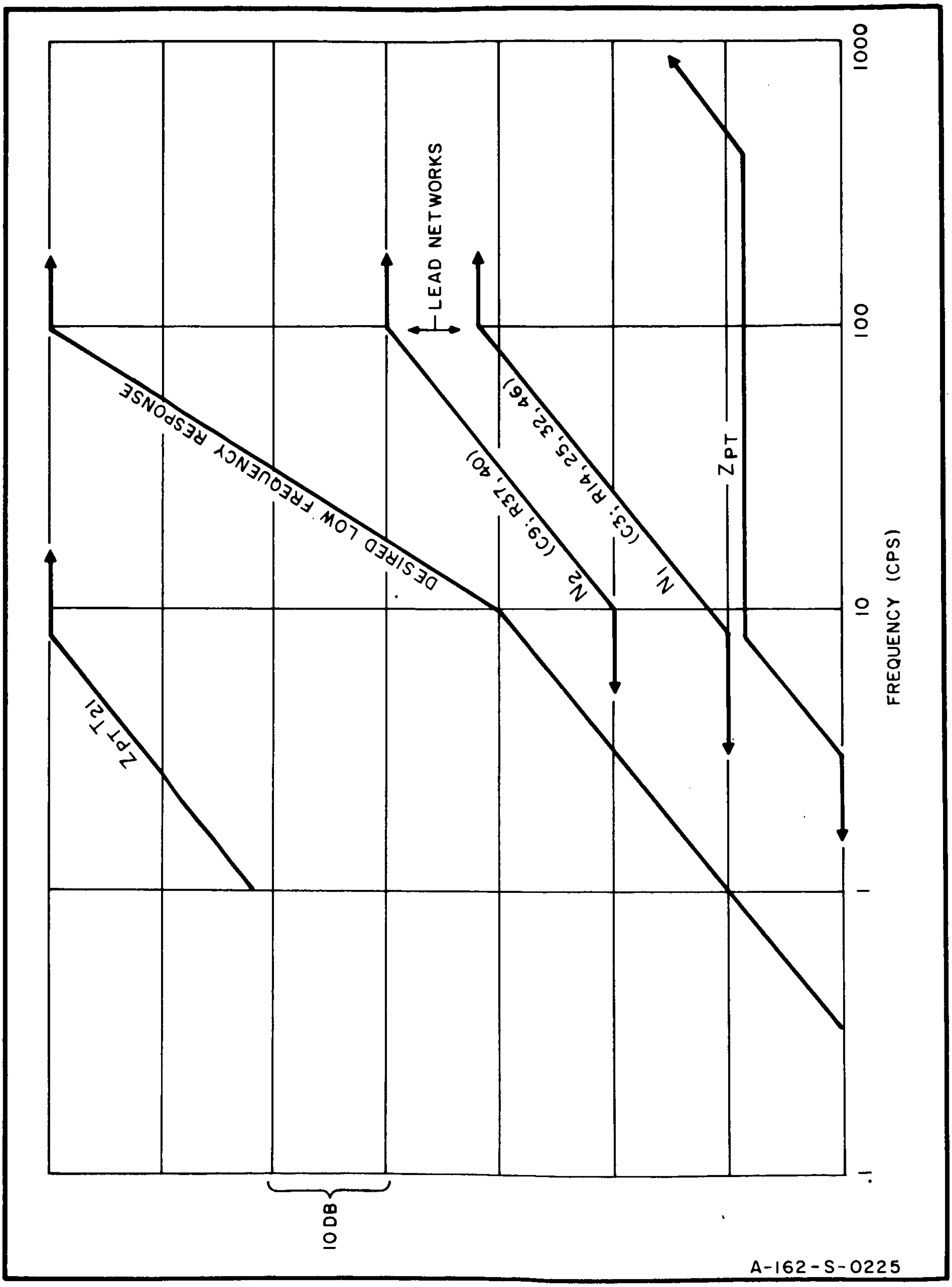


FIG. 41 MAGNET DRIVER LOW-FREQUENCY BODE DIAGRAMS

The desired high-frequency response of the amplifier (before the overall feedback loop is closed) is similar to the low-frequency response of Figure 41 in reverse, that is, flat to 10 kc, descending at 40 db/decade (double negative slope) to 100 kc and at 20 db/decade (single negative slope) thereafter. Figure 41 shows that anywhere beyond 420 cps $Z_{pt}\ T_{21}$ could be made to fall at 20 db/decade by simply preventing Z_{pt} from rising, as by means of a shunt resistor. The high frequency behavior of Z_{pt} is very much like an inductor having a reactance of 230 ohms at 10 kc. A shunt resistor of this value would cause a single negative slope overall at this frequency but would not be desirable because of the amount of current it would require from the amplifier during a (50 volt) magnetizing pulse. But an equivalent resistance can be achieved by means of local feedback. In practice it is most convenient to provide feedback to the emitter of the second transistor, used essentially for voltage amplification, in the configuration shown in Figure 42. Since the primary voltage E_p is much greater than the emitter voltage, the feedback current is principally E_p/Z_f. Most of this flows in the emitter and therefore the collector circuit. Z_{21} is simply the collector load resistance or 2.3 K in mid-band. The current gain Y_{21B} is about .25. Hence the equivalent shunt resistance

$$\frac{E_p}{I_o} \simeq \frac{Z_f}{(2300)(.25)} \simeq \frac{Z_f}{600}$$

is much lower than Z_f and the current which is diverted from the probe and into the <u>feedback</u> resistor is negligible compared to that which would flow in the equivalent shunt resistance.

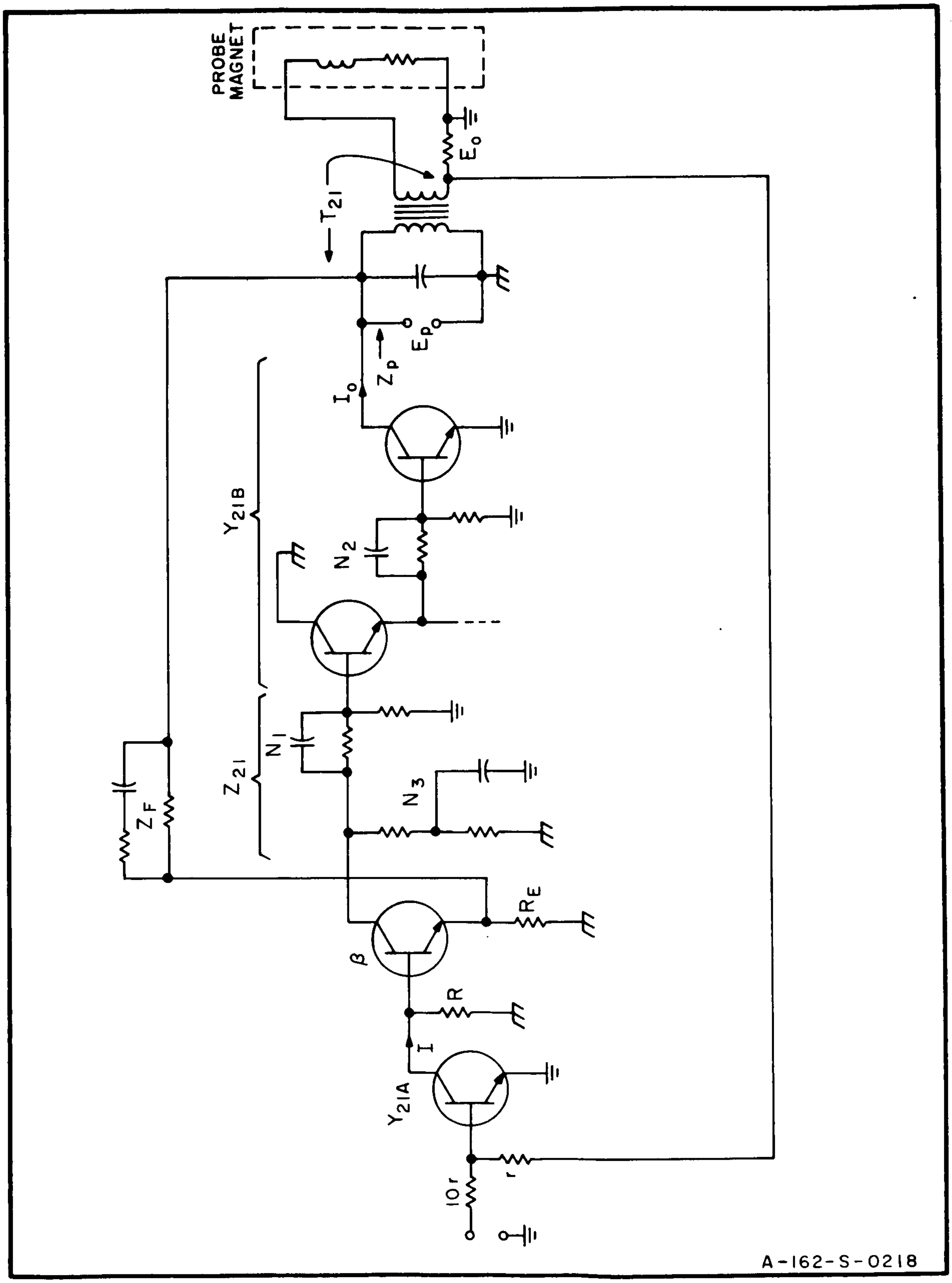
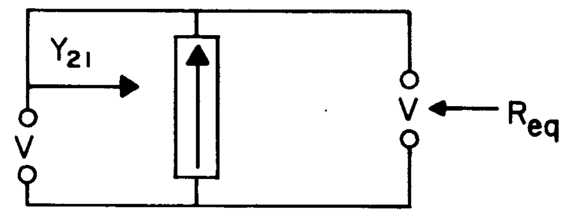


FIG. 42 SIMPLIFIED SCHEMATIC DIAGRAM OF MAGNET DRIVER

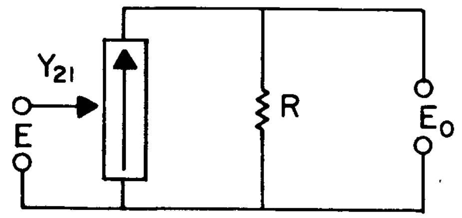
One general property of the circuit is of interest when the stability of this minor loop is considered and that is the condition for unity loop gain. If V is applied to the output of this circuit as shown below:



the resulting output current is $I = VY_{21}$ and the resistance is:

$$R_{eq} = \frac{V}{VY_{21}} = \frac{1}{Y_{21}} .$$

If E is applied to the input of the circuit loaded by R,



the output voltage $E_o = EY_{21}R$. For unity loop gain with the output tied to the input

$$E_o = E \qquad \text{or} \qquad R = \frac{1}{Y_{21}} = R_{eq} .$$

Hence the local feedback path can be ignored at frequencies for which the primary impedance of the (loaded) transformer is less than R_{eq} (230 ohms).

The high-frequency descent of the minor loop response may be established by parasitic (and/or deliberate) shunt capacitance at the output. A total of 100 pf will place the gain crossover point at 7 Mc. With this addition, the expression for primary impedance is

$$Z_p = 10^{10} \frac{(S + S_1)(S + S_7)}{(S + S_3)(S + S_{12})(S + S_{12}^*)}$$

where $S_{12} = 2\pi(210 + j260 \times 10^3)$.

The extra 20 db decrease in gain required from 10 to 100 kc is obtained by the configuration shown for Z_f in Figure 42. The impedance should be 600(230 ohms) or 140 k ohms at 10 kc, dropping to one-tenth that value at 100 kc. A constant output resistance is obtained by making Z_{21} decrease in the same manner (see N3 in Figure 42). This value of resistance had been shown to be very effective in damping out high-frequency transformer resonances. The low frequency descent is taken care of by the shunt inductance of the transformer loaded by the probe. The amplifier low-frequency response is therefore simply proportional to $Z_{21}Y_{21B}Z_pT_{21}$. Hence the low frequency lead networks N_1 and N_2 described by Figure 41 may simply be incorporated into $Z_{21}Y_{21B}$, as shown in Figure 42, despite the encompassing feedback. The theoretical response curves for the complete Magnet Driver circuit are given in Figure 43.

The following tabulation summarizes the results of a slightly more detailed analysis of the frequency sensitive

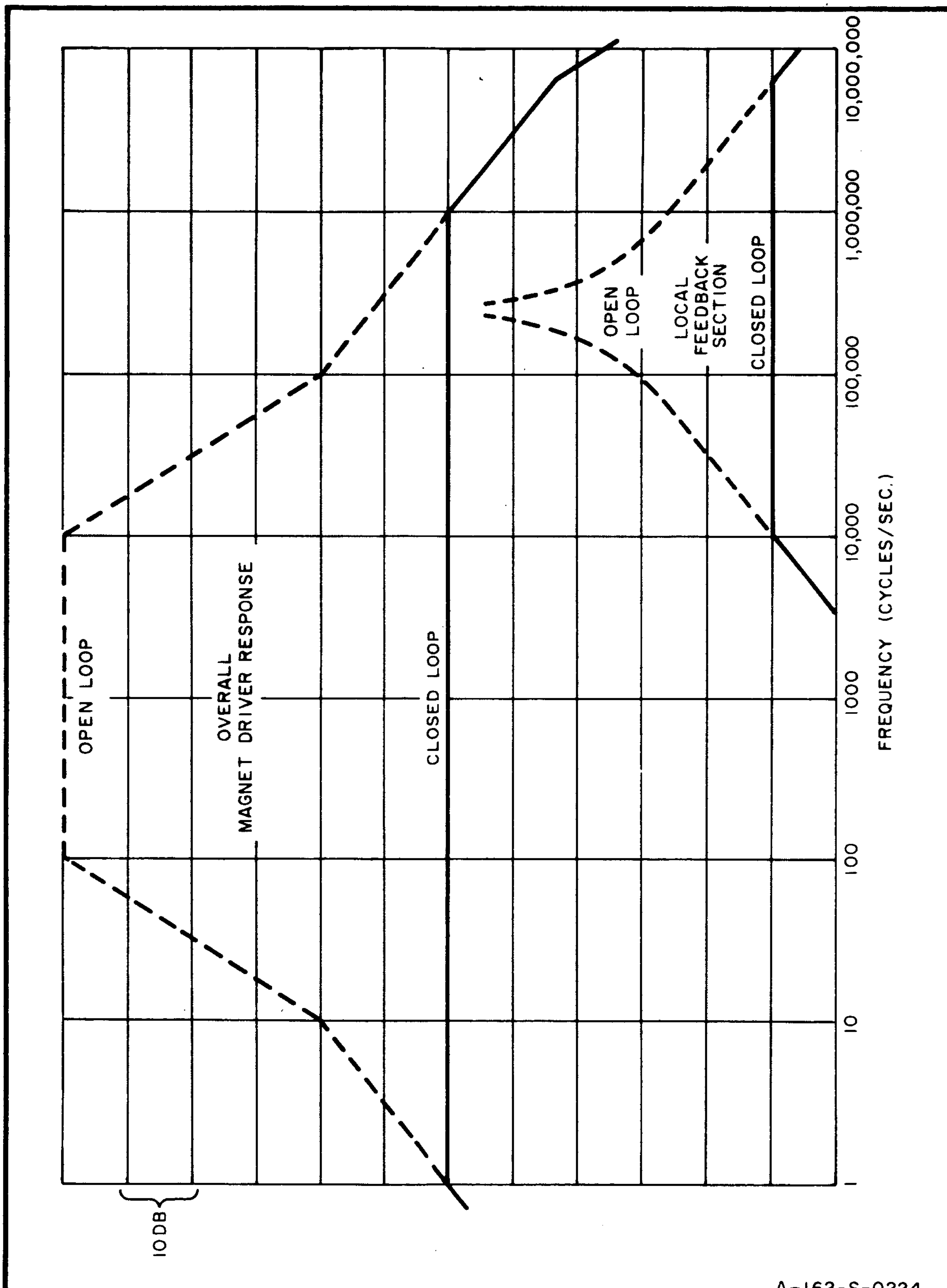


FIG. 43 MAGNET DRIVER ASYMPTOTIC RESPONSE CURVES

circuits illustrated in Figure 42 for the Magnet Driver. The assumptions made are that the transistor collector admittance and base-emitter resistance are both zero.

$$\frac{E_p}{I} = RZ_p \frac{(\beta + 1)R_E - \beta Z_{21}Y_{21B}(R_E + Z_f)}{\beta Z_{21}Y_{21B}R_E Z_p + (\beta + 1)R_E(Z_f + Z_p) + R(R_E + Z_f + Z_p)}$$

Forward gain of complete driver $= \frac{1}{11} Y_{21A} \frac{E_p}{I} T_{21} = G$

Loop gain of complete driver $= \frac{10}{11} Y_{21A} \frac{E_p}{I} T_{21} = HG$

Overall gain $\quad \frac{G}{1 + HG} = \frac{\frac{1}{11} Y_{21A} \frac{E_p}{I} T_{21}}{1 + \frac{10}{11} Y_{21A} \frac{E_p}{I} T_{21}}$

$$Y_{21A} = K_1$$

$$Z_p = K_4 \frac{(S + S_1)(S + S_7)}{(S + S_3)(S + S_{12})(S + S^*_{12})}$$

$$Z_{21} = K_2 \frac{(S + S_2)(S + S_{10})}{(S + S_5)(S + S_8)}$$

$$Y_{21B} = K_3 \frac{S + S_4}{S + S_6}$$

$$Z_f = K_5 \frac{S + S_{11}}{S + S_9}$$

$$T_{21} = K_6 \frac{S}{(S + S_1)(S + S_7)}$$

$K_1 = .39$

$K_2 = 230$

$K_3 = .25$

$K_4 = 10^{10}$

$K_5 = 14{,}000$

$K_6 = 263$

$R = 1000$

$\beta = 50$

$R_E = 70$

$s_1 = 2\pi 2.8$

$s_2 = s_3 = 2\pi 8.2$

$s_4 = 2\pi 10$

$s_5 = s_6 = 2\pi 100$

$s_7 = 2\pi 420$

$s_8 = s_9 = 2\pi 10^4$

$s_{10} = s_{11} = 2\pi 10^5$

$s_{12} = 2\pi 210 + j2\pi 2.60 \times 10^5 \qquad j = \sqrt{-1}$

4. Magnet Driver

The circuits in the unit known as the Magnet Driver are described by Fig. 44. For test purposes this unit may be operated by itself. It has facilities for the local control of the average current and balance of its output stage. Precise control of these quantities is important because the output stage is operated very near its maximum rated power and the transformer can withstand very little magnetizing current. For the generation of a trapezoid signal at full power this unit must operate in conjunction with all the components of the trapezoid generator Fig. 38, some of which are not concerned with the generation of the trapezoid at all but are parts of several systems used to maintain proper operating conditions in the Magnet Driver output stage.

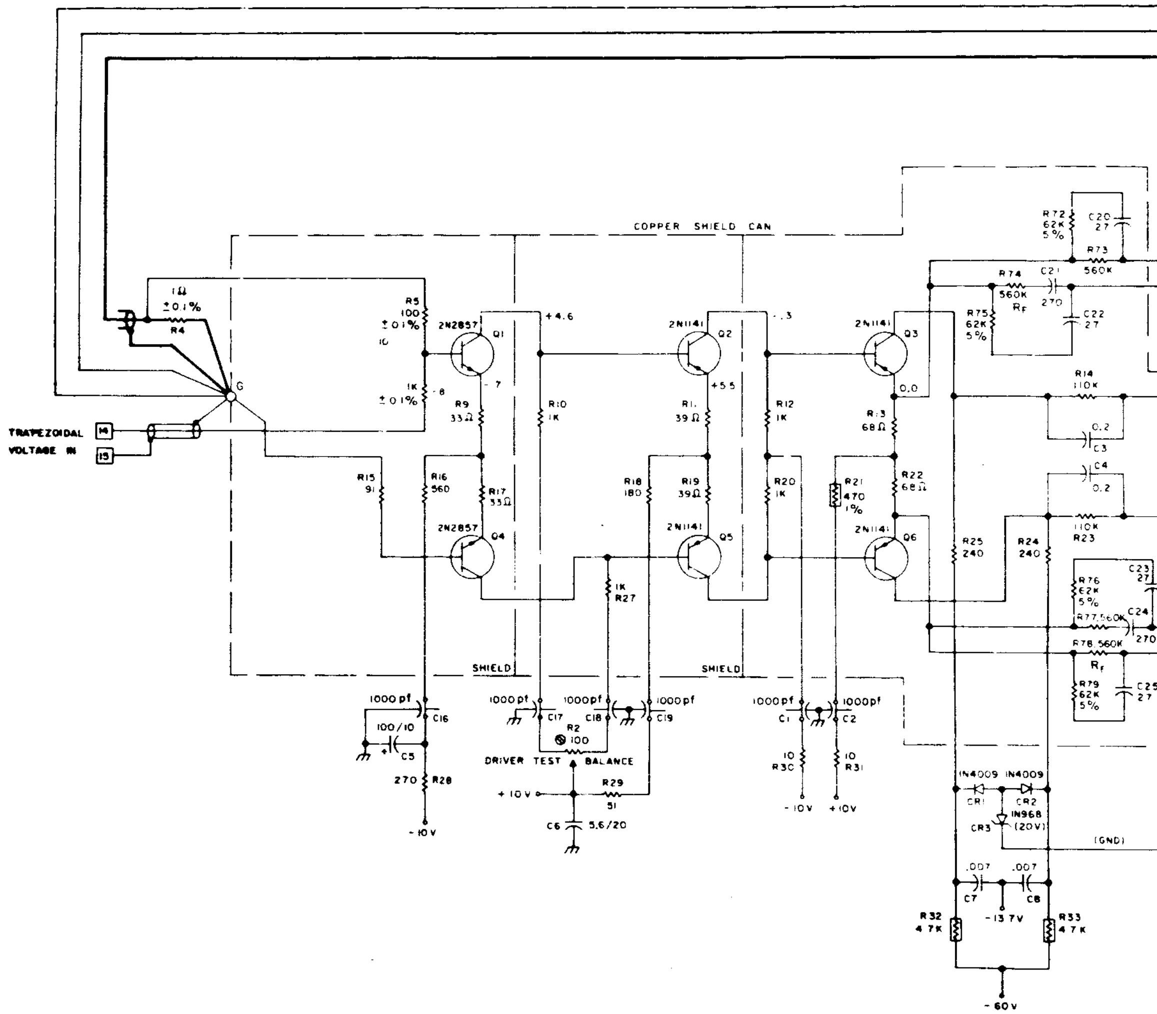
The Magnet Driver is a feedback amplifier which compares a trapezoidal voltage input with a voltage proportional to output current, subjects the sum to what is essentially three stages of voltage amplification and two stages of current amplification before the last stage which drives the output transformer. Special circuits are used to supply the magnet current from a low voltage supply when the magnet voltage is small and a high voltage supply when the magnet voltage is large. A servo adjusts the output of the high voltage supply so that it is just sufficient for the minimum voltage requirements of the high-voltage driver transistors to be met. Part of the servo which does this is to be found in the Trapezoid Generator (Fig. 38). The servo which establishes the driver output stage minimum current is also to be found there. Another servo in the Magnet Driver shuts down the low voltage supply whenever, as a result of an oversized input signal, the Magnet Driver output stage might be overloaded.*

The 10.00 VP-P trapezoidal input signal is applied to a summing resistor (R 8) and the feedback signal to another (R 5) which joins the first at the base of one transistor (Q 1) of a pair in the first stage. The base of the other (Q 4) returns to a special ground point (G) through a resistor (R 15). The base-ground resistances are equalized to promote DC stability.

The output transformer (T 1) circuit is symmetrical. There are two split primary (driver) windings, and a split secondary, the outer ends of the latter being connected to the probe electromagnet and the inner ends being grounded through identical resistors (R 4,54). The voltage across each of these resistors is a measure of output current. One of them (R 4) is connected to the feedback resistor (R 5) and the other is used in an output-current monitoring circuit, (the ONE test described in Sec. II-D.1).

The first stage input resistance is raised by the insertion of emitter resistors (R 9,17) which return through a common resistor (R 16) and a decoupling filter (C 5,16;R 28) to the negative supply. The collector loads consist of a fixed part (R 10,27) and a variable part (R 2) labeled DRIVER TEST BALANCE used to obtain average current balance in the output stage when testing the Magnet Driver independently of the balancing servo in the Trapezoid Generator unit.

* In the present state of the art the bandwidth requirements of the Magnet Driver can only be met with transistors having very small junctions requiring extraordinary protective circuits.



1 CHASSIS GROUND ON COPPER BOX

5 + 70 V

6 + 60 V

7 + 10 V

8 − 10 V

9 − 13.7 V

10 − 60 V

11 − 70 V

NOTES

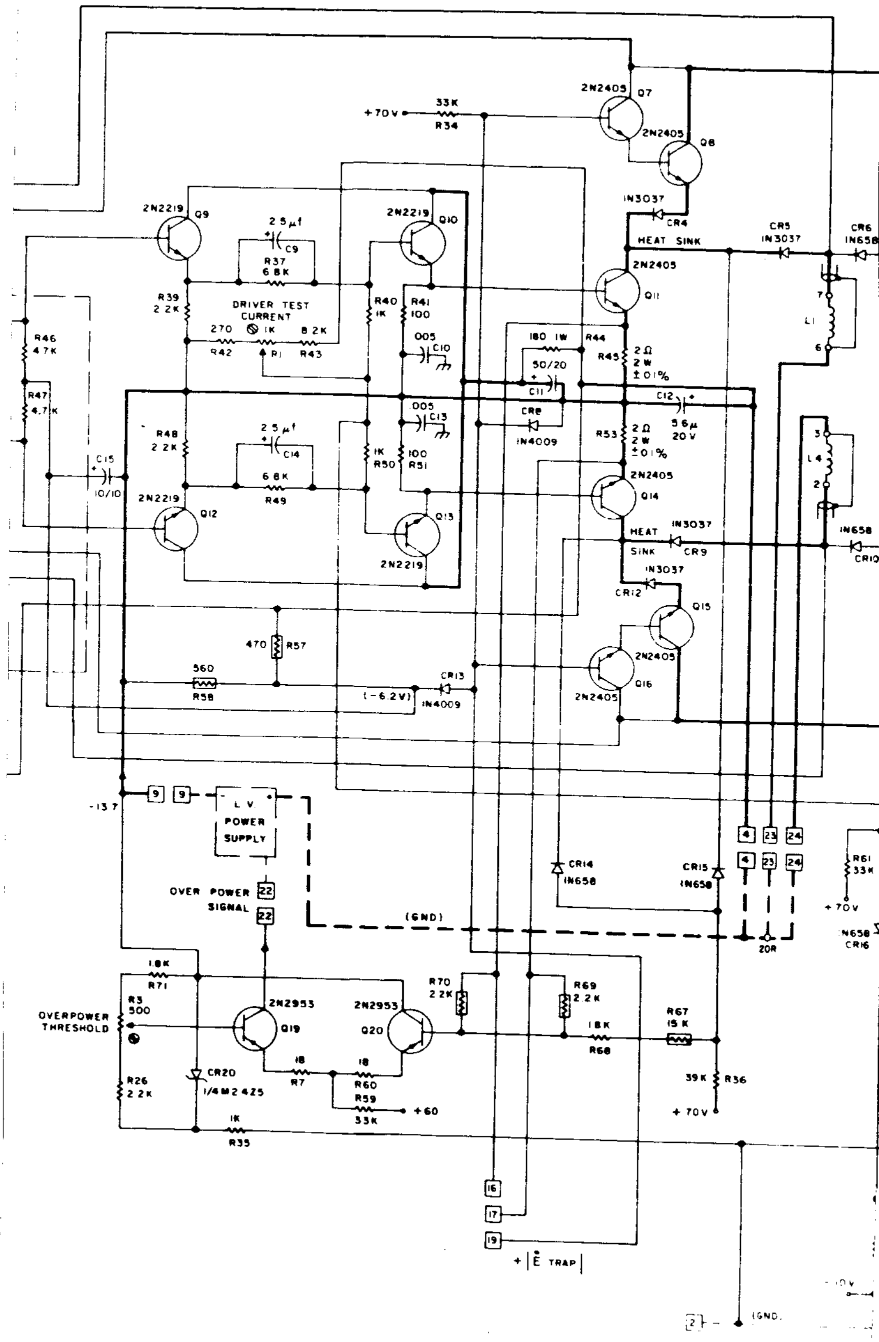
NUMBERS IN BOXES ARE PIN CONNECTIONS

— RESISTORS 1/2 W ± 10% EXCEPT AS NOTED

— RESISTORS 1/2 W ± 1% EXCEPT AS NOTED

137 0

Y- ELECTRONICS RESEARCH LABORATORIES



137 (2)

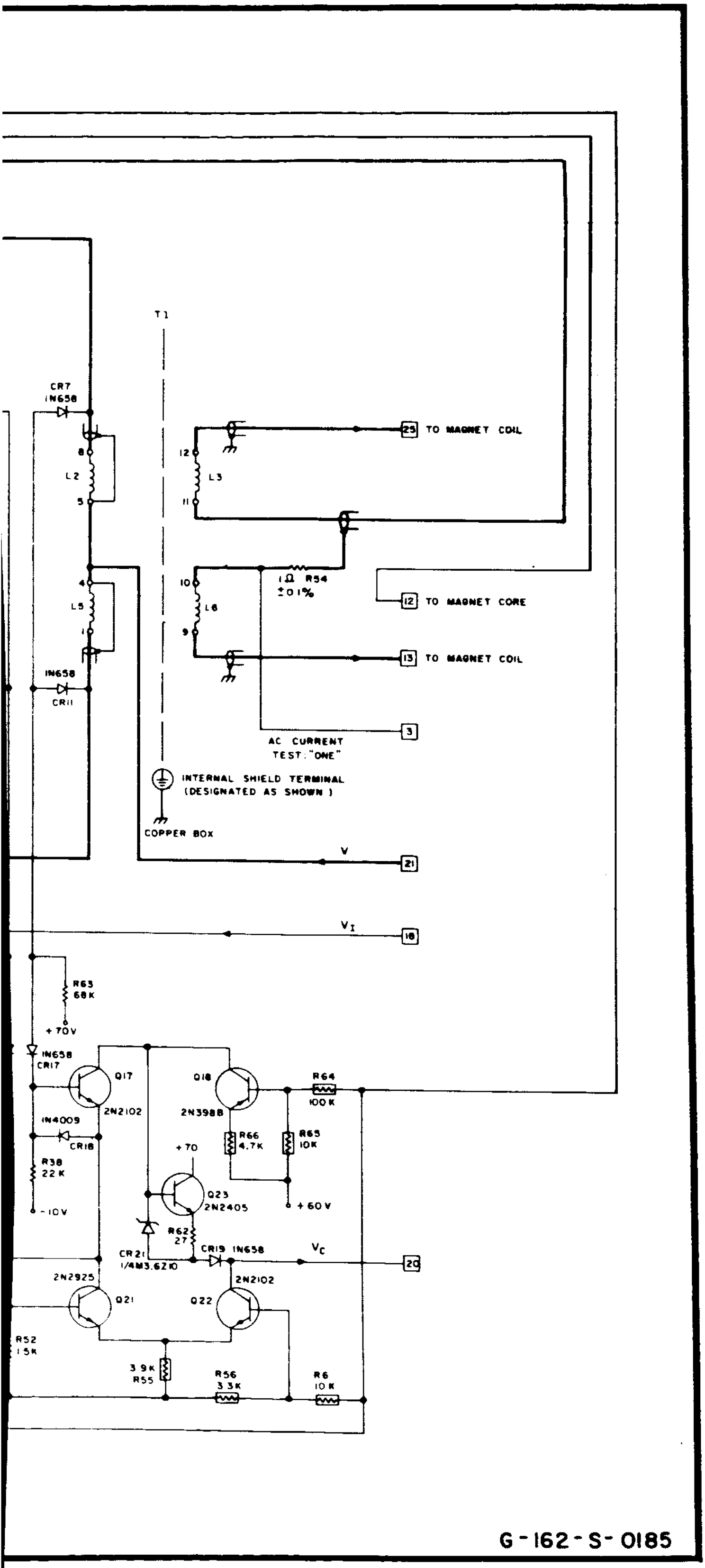


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FIG. 44 MAGNET DRIVER SCHEMATIC DIAGRAM, CODE 5,8 H

3

The variable part is shunted by capacitors (C 17,18) to preclude interfering signals.

The second stage transistors (Q 2,5) also have individual emitter resistors (R 11,19) which return through a common resistor (R 18) and a decoupling filter (C 19;R 29) to the positive supply which is shunted by a nearby capacitor (C 6). The collector loads (R 12,20) return to the negative supply through a decoupling filter (C 1;R 30). (These correspond to R in Figure 42.) Another filter (C 2;R 31) is in the positive supply lead to the common emitter resistor (R 21) of the third stage. The filter resistors reduce the Q's of the self resonant loops formed by interconnecting the power supply feedthrough capacitors. (The transfer function for the first two stages corresponds to Y_{21A} in Figure 42.)

The third stage transistors (Q 3,6) have individual emitter resistors (R 13,22) across which there appears not only the signal derived from the base input but a feedback signal derived from the output transformer primaries. (These resistors correspond to R_E in Figure 42.) This local feedback is used to improve the overall frequency response of the transformer. It is equivalent in effect to resistors shunting the transformer. It is used because equivalent shunt resistors would require too much driving current.

The third stage collector circuit consists of a high-frequency lag network (R 24,25,32,33;C 7,8) followed by a low-frequency lead network (R 14,23,46,47;C 3,4). (These networks correspond to N_3 and N_1,respectively in Fig. 42.)

The high supply voltage necessary for large low-frequency gain in this stage could cause the transistors to avalanche under unusual signal conditions, were the collector voltages not restricted by shunt diodes (CR 1,2,3).

The signal reference point for the circuits up to and including the bases of the third stage is ground (G). For those after them it is the (negative) low voltage supply (-13.7 VDC). The first three stages have an unbalanced input to balanced output mid-band voltage gain of 4,000. (The transfer function of the remaining stages corresponds to Y_{21B} of Fig. 42.)

The next stage has an input resistance of about 60 K ohms and consists of emitter-followers (Q 9,12;R 39,48) driving low-frequency lead networks (C 9,14;R 37,40,49,50) which return to the DRIVER TEST CURRENT potentiometer (R 1) in a divider circuit (R 42,43). This potentiometer determines the average current of the output stage if the Trapezoid Generator unit is not in place. The potentiometer voltage is normally overridden by this unit. The next stage emitter-followers (Q 10,13;R 41,51) derive their collector voltage from the same point as those of the previous stage, a series resistor (R 44) which limits the maximum possible dissipation of these stages in the event of abnormally large signals. This point is by-passed, by means of a capacitor (C 11), to the signal reference point (-13.7 VDC) for the final stages.

One or the other of the next pair of transistors (Q 11,14) supplies the signal current to the transformer (T 1) through a diode (CR 5 or CR 9) during the time that the (trapezoidal) signal into the Magnet Driver is constant. The turns ratio (secondary to half-primary) is 1:1. The voltage drop due to the 0.5 ampere secondary current in the secondary resistance (1.4 ohms) plus the current sensing resistance (2 ohms) plus the magnet resistance (R_m ohms) is $1.7 + 0.5\ R_m$ (volts). The drop due to the 0.5 ampere plus the maximum allowable magnetizing current of 0.1 ampere flowing in the primary resistance (3.6 ohm) and the (2.0 ohm) emitter resistance (R 45 or R 53) is 3.36 volts. There will be a drop of 0.9 volt in the diode. The total drop is 5.96 + 0.5 R_m volts. For the lowest design value of probe resistance (1 ohm) the transistor peak dissipation will have its maximum value of 4.3 watts. For the highest design value of probe resistance (5 ohms) the collector-ground voltage will have a minimum value of -7.26 volts. This condition should bring the auxiliary circuit (CR 4;Q 7,8 or CR 12; Q 15,16) to the threshold of conduction.

Nearly all of the current which is diverted from the first primary flows in the second primary, which together with the first constitutes a bifilar winding. When the trapezoid slope becomes non-zero, there is a sudden drop in voltage on the side which begins to conduct and all of the current flows in the second primary through the auxiliary circuit. A servo establishes a voltage V on the second primary which is just large enough so that the least value of auxiliary transistor (Q 8 or Q 15) collector voltage V_{CE} will be just sufficient for the (0.5 ampere) peak current which the transistor must supply. To do this the servo senses the least value of either auxiliary collector voltage and appropriately raises or lowers the charge in a capacitor which determines the value of V. The capacitor is physically located in the Trapezoid Generator unit. It is connected to pin $\boxed{20}$ of Fig. 44 where its stored voltage V_c appears.

Until a magnetizing spike comes along, V_c does not go positive because the anode of the series charging diode (CR 19) is grounded by a clamping transistor (Q 17) and it does not go negative because the discharge transistor (Q 22) is cut off. The spike causes either CR 6 or CR 10 to conduct, removing the current through R 61 from CR 16 (which would then normally be cut off) and from R 52. This cuts off Q 21 causing a discharge current of 0.5 ma to flow through Q 22. The current is determined by a base voltage divider (R 6,56), the base-emitter drop, the -10 VDC supply and the emitter resistor R 55.

If V is not large enough, either CR 7 or CR 11 will conduct, removing some (or all) of the R 63 current from CR 17 and the base of Q 17. (If all of this current is removed, the R 38 current flows in the catcher diode CR 18.) A 1.0 ma constant-current source (Q 18,R 64,65,66) causes the Q 17 collector voltage to rise, causing current from an emitter follower (Q 23) through an emitter resistor (R 62) and an isolating diode (CR 19) to flow into the capacitor, thus raising V_c and consequently V. This current is limited to about 12 ma. It cannot exceed the sum of the 1.0 ma constant current, and the difference between the Zener (CR 21) and transistor (Q 23) base-emitter voltages divided by R_{62}. This current was chosen after the considerations relating to the waveform at this point.

The transformer primary waveform is easily derived from the voltage ratio T_{21} (Fig. 42) and the 1.0 volt p-p output trapezoid e_o, which during spike time is just a ramp.

$$e_o(t) = 10^4 t \qquad\qquad E_o = 10^4 \frac{1}{S^2}$$

$$E_p = \frac{E_o}{T_{21}} = \frac{10^4}{S^2} \frac{1}{263} \frac{(S + 2\pi 3)(S + 2\pi 420)}{S}$$

(See Sec. III-F.3 to find the expression for T_{21})

$$= 38 \left(\frac{1}{S} + \frac{2660}{S^2} + \frac{50,000}{S^3}\right)$$

$$e_p(t) = 38 + 1.01 \times 10^5 t + 9.5 \times 10^5 t^2 \qquad 0 < t < 10^{-4} .$$

For a typical electromagnet of 2.2 mh inductance with a trapezoidal current having a ramp of 100 microseconds, the primary voltage during spike time would consist of a 38-volt rectangular pulse with a 10-volt ramp upon it. But the ramp is actually 3 volts greater because during this time the current is delivered to the second primary which has about 6 ohms more resistance than the first primary. (Finer wire was used for the second in an attempt to make the most efficient use of the transformer winding space.)

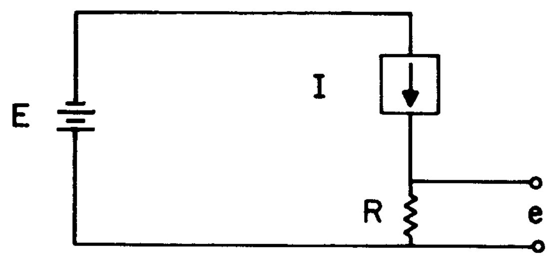
If we assume that under the condition of equilibrium the auxiliary collector voltage shall not fall more than one volt below some threshold value, then the time below threshold $T = 1.0\text{v}\,\frac{10^{-4}\text{sec}}{13\text{v}} \simeq 8 \times 10^{-6}$ sec . The integral of the charging current over this period should be equal to that of the discharge current or (0.5 ma)(10^{-4} sec). Hence the average charging current should be about 6.5 ma and the peak current perhaps twice that.

The capacitor to be charged is shown as C 20 in Figure 38. It is shunted by a low-leakage diode (CR 13) to prevent the voltage at this point from becoming indefinitely negative, if the Magnet Driver is not plugged in, as a result of the base current in the emitter follower (Q 18; R 79) used as a first buffer. There is a second buffer (Q 22;R 80) with enough quiescent current to be undisturbed by the constant-current source (Q 19;CR 17;R 64,65) which clamps the input base of a compound emitter-follower (Q 21, 20;R 66,67;C 21) to the output of the second buffer through a diode (CR 15). Should the average current supplied by the compound emitter-follower (to the auxiliary transistors in the Magnet Driver) become excessive, a diode (CR 14) conducts, removes the constant current, and the output voltage V drops because of current through a resistor (R 81) to the negative supply. A load resistor (R 82) establishes a minimum output current for testing in the absence of Magnet Driver current. The latter consists of a ramp of current from 0 to 0.5 ampere during the latter half of each sloping part of the Trapezoid. Most of the ramp current is supplied by the capacitor (C21). The capacitance is sufficient to prevent the voltage V from dropping during this normal condition but small enough to offer protection to the auxiliary transistors in the event of prolonged overload. Although the peak power is high, the average power in the auxiliary transistors is low enough so that heat sinks, and their inevitably large stray capacitance, can be avoided.

The auxiliary transistors are further protected by the trapezoid magnitude circuit (see Q 10, Fig. 38) described in Sec. III-F.2 which keeps them from conducting except during slope time. During this time the input bases of these, Fig. 44, transistor (Q 7,8,15,16) circuits, instead of being clamped to -13.7 VDC through one diode (CR8), are clamped to a more positive voltage established by a divider (R 57,58) through another diode (CR 13) as a result of current through a resistor (R 34) connected to the positive supply. A capacitor (C 15) bypasses the divider to the output section signal reference point, -13.7 VDC.

In the event that the feedback circuit is interrupted, as by removing the magnet connector, every signal amplifier will be driven to saturation. In this case it is necessary immediately to reduce the output of the -13.7 VDC supply. In fact, even starting transients (when the equipment is turned on) may make this action necessary. The circuit to be described does this automatically to the extent necessary to keep the instantaneous dissipation in the low-voltage driver transistors (Q 11,14) below 4.4 watts.

Each transistor to be protected is represented below:



as a current source across which there is a voltage drop E-e.

$$E - e = E - RI$$

$$(E - e)I = EI - RI^2 \triangleq W \text{ (transistor dissipation)}$$

$$I^2 - \frac{E}{R}I + \frac{W}{R} = 0$$

$$I = \frac{E}{R} - \sqrt{\frac{E^2}{4R^2} - \frac{W}{R}}$$

R represents the resistance (R_{45} or R_{53}) which has been placed in series with each emitter for the purpose of sensing transistor current. For R = 2 ohms and $W \leq 4.4$ watts, the relationship between the supply voltage E and the current I is given by

$$I \leq \frac{E}{4} - \sqrt{\frac{E^2}{16} - 2.2} \quad .$$

This relationship is shown in Fig. 45 together with a linear approximation which passes through the point at which transistor dissipation is greatest in this application. For a magnet of least resistance (1 ohm) the transformer voltage drop at maximum current is (at the end of the constant part of the trapezoid):

	Resistance	Current	Voltage
Drop across magnet	1.0	.5	0.5
" " sensing resistor	2.0	.5	1.0
" " secondary	1.4	.5	0.7
" " primary	3.6	.6	2.16
" " diode	-	.6	0.9
Total			5.26

In this worst case $E_{w\ max} = 13.70 - 5.26 = 8.44$ (volts)

$I_{max} = 0.6$ (amperes)

The equation for the chosen linear approximation is:

$$15.3\ I + E = 17.6\ .$$

It is obtained as a resistive summation of the voltage at the Fig. 44 transistor (Q 11 or Q 14) collector and the voltage drop in the emitter resistor (R 45 or R 53) of the transistor which is conducting by means of summing resistors (R 67,68,69,70). The transistor which is conducting will be the one with the less positive collector voltage and hence it will be connected to the summing resistor (R 67) through a diode (CR 14 or CR 15) because of the current through a resistor (R 36) from the positive supply. When one transistor is conducting heavily the other is cut off. The current I on the conducting side causes the emitter voltage to rise to 2 I volts. The voltage at the summing junction with respect to - 13.7 volts is:

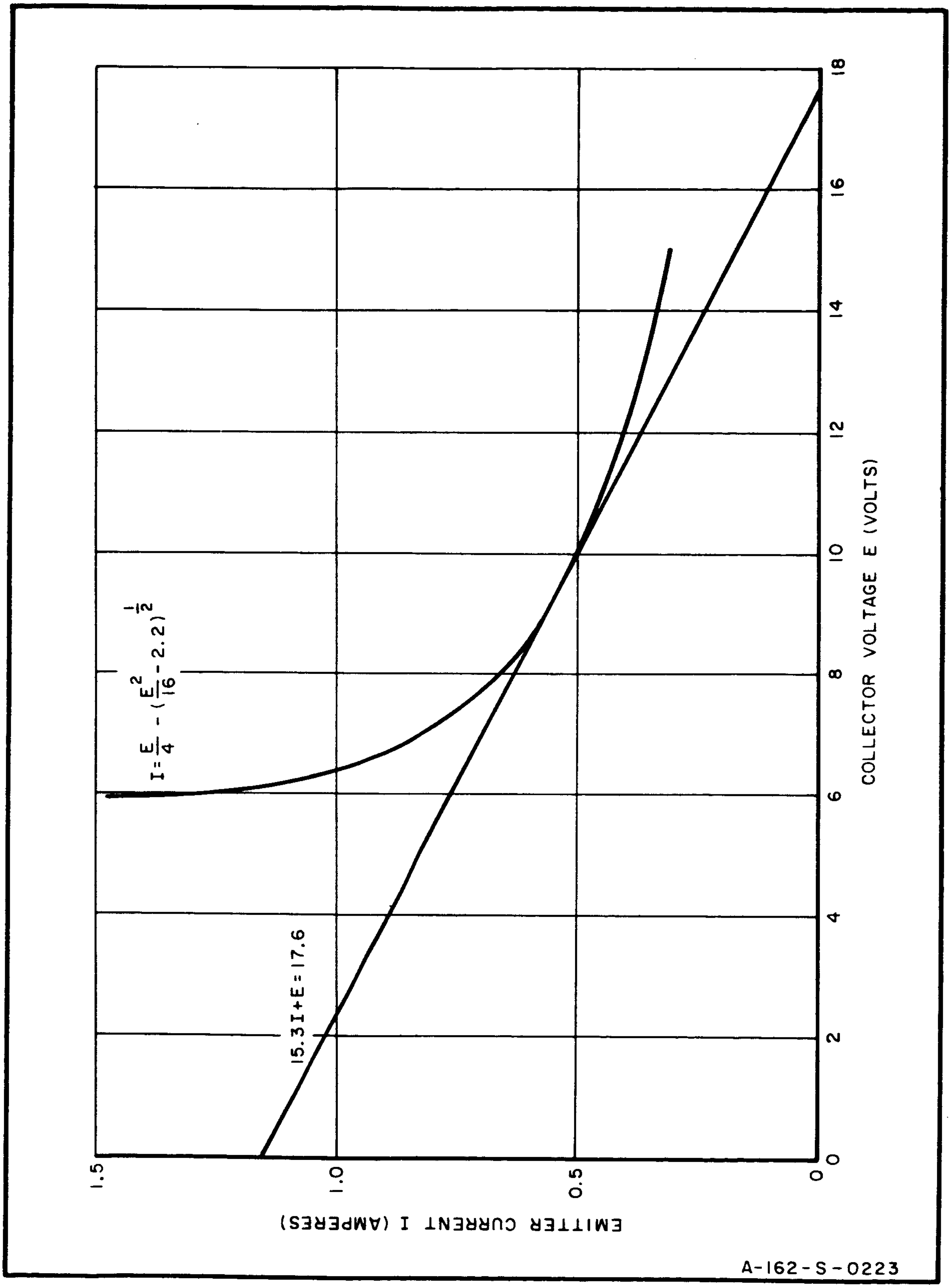


FIG. 45 OUTPUT TRANSISTOR CONSTANT-POWER LOCUS AND A LINEAR APPROXIMATION

$$\frac{2I \frac{1}{R_{69}} + E \frac{1}{R_{67} + R_{68}}}{\frac{1}{R_{69}} + \frac{1}{R_{70}} + \frac{1}{R_{67} + R_{68}}} = \frac{.910I + .0595\ E}{.9695}$$

$$= .939\ I + .0613\ E,$$

where R_{69} and R_{70} may be interchanged. When this sum exceeds (.939)(.600) + (.0613)(8.44) = 1.08 (volts) the supply voltage (-13.7 VDC) should decrease.

The sum is compared with a fixed voltage from an adjustable divider (R 3,26,71) across a Zener diode (CR 20) by means of a difference amplifier (Q 19,20;R 7,59,60). The Zener current is established by means of a resistor (R 35) to ground. As the sum exceeds the OVERPOWER THRESHOLD potentiometer (R 3) voltage, the (Q 19) collector current increases. When this current exceeds that in R 27 of Fig. 37 the supply voltage decreases as shown by the linear graph in Fig. 45.

The -13.7 VDC supply is shunted by a capacitor (C 12) in the Magnet Driver where it is also bypassed to either side of the copper shield box by two low inductance ceramic capacitors (C 10,13).

The internal feedback loop is completed by four circuits (C 20;R 72,73)(C 21,22;R 74,75)(C 23,24;R 76,77) (C 25;R 78,79) each corresponding to Z_f in Fig. 42. Series capacitors (C 21,24) prevent the average current in the third voltage amplifier (Q 3,6) from being affected by changes in the second primary supply voltage V. The impedance of each is less than one-tenth that of its associated resistor at the corner frequency above which the feedback circuit first becomes effective. Four feedback paths, identical in effect, are provided to make the amplifier frequency response independent of which half of which primary is receiving the greater signal current. Each has an impedance four times that computed for Z_f in Fig. 42.

Two more feedback systems remain to be described. Each acts upon voltages proportional to the Magnet Driver output transistor currents. These voltages which appear, in Figure 44, at the emitter resistors (R 45,53) of the low-voltage output transistors (Q 11,14), are brought over to the Trapezoid Generator unit where the feedback components are located. They appear on pins $\boxed{3}$ and $\boxed{4}$ of Fig. 38 and go to two different circuits. One of these circuits maintains driver output-stage average-current balance to prevent saturation of the Magnet Driver output transformer. The other sets the minimum or crossover current for this class B stage.

The current signals pass through a low-pass filter (C 15,16,17;R 45,46) to a difference amplifier. The description of this amplifier begins in Sec. III-F.2.

The differential voltage gain of the filter-amplifier combination is

$$\frac{33K}{2700 + 100} = 11.8 \quad .$$

The trapezoid amplifier converts this differential signal to an unbalanced one of the same magnitude. The gain from the trapezoid generator to the summing junction of the Magnet Driver depends somewhat upon the resistance (determined by jumpers on R3 - 9) necessary to reduce the nominal 6.2 Zener (CR 1,2) voltage to precisely 5 V at the Magnet Driver input summing resistor, but is approximately

$$\frac{100}{1240 + 100} = .075 \quad .$$

At low frequencies the transfer admittance from input summing junction (voltage) to output (current) is 8 and the voltage gain to the 2 ohm current sensing resistor (Fig. 44:R 45 or 53) is 16. The loop gain of the balancing-loop servo is (11.8)(.075)(16) = 14 = 23 db below the cut-off frequency (.005 cps) of the filter. The loop gain is flat to .005 cps; descends with a single slope through the gain crossover point (-23 db), at .07 cps; reaches -66 db at approximately 10 cps; rises with single slope to -46 db at 100 cps; and thence descends with a single slope. The closed-loop rise time of the balancing servo is 2.3 seconds.

The remaining feedback system establishes the minimum or "crossover" current of the class B output stage. This current occurs from the time one half of the output stage goes into conduction until the other is cut off. During this time the average of the voltages across the Fig. 44 emitter resistors (R 45,53) is constant. Fig. 38 shows how the average is obtained by two resistors (R 73,74) and fed into a difference amplifier (Q 23,24, etc.), where it is compared to a fixed voltage from the MINIMUM CURRENT potentiometer (R 2) in a divider circuit (R 72,75) on the -13.7 VDC source. The amplifier has a constant-current source (Q 3,R 78) in the common emitter circuit and another (Q 16; R 61,62) in the output collector circuit which enables a high gain to be achieved in one stage. The other collector has a dummy load (R 69) which is bypassed (C 19). The output collector is coupled by means of an emitter follower

(Q17; R70) and an isolating diode (CR16) to a storage capacitor (C22) which has an essentially constant-current discharge path through a resistor (R76) to the negative supply. The emitter follower is capable of high peak currents which are nevertheless limited by means of a collector resistor (R68) for its protection. (The collector current peaks are decoupled (R63; C18) from the power supply.) It also provides a small amount of local feedback through a resistor (R71). In normal operation the current minima cause the capacitor charge to be restored. The capacitor voltage is emitter-follower (Q25; R77) coupled to the bases of the drivers, Figure 44 (Q10, 13) of the final amplifier stage in the Magnet Driver, thereby, determining the operating point for this stage and hence its minimum current.

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9. Shaw, R. F., Skalak, R., and Marple, N. B., "A Bioengineering Approach to the Characterization of Vascular Beds: Electrical Analogues and the Pulmonary Circulation," Columbia University Electronics Research Laboratories, Memorandum Report M-2/100, February 1962.

10. Goldman, S. C., Marple, N. B. and Scolnik, W. L., "Effects Flow Profile on Electromagnetic Flowmeter Accuracy," Journal of Applied Physiology 18, 652, 1963.

V. APPENDICES

A. OPERATIONAL AMPLIFIER

Four commercially available operational amplifiers are used in the Flowmeter Model B. These are used in the Volume and Time integrators, the Compensator and the Average Flow Amplifier.

Specifications for the A00-4 Operational Amplifier, which were developed by the Fairchild Semiconductor Instrumentation Division of the Fairchild Co., of Palo Alto, California, are reproduced in this appendix.

TYPE A00-4

OPERATIONAL AMPLIFIER

SPECIFICATION FOR

This device is a chopper stabilized, DC amplifier featuring high input impedance, large open loop gain, and low input voltage (and current) drift. The solid state chopper requires no external drive or power. Silicon semiconductors are used throughout. Conformity to this document is assured by stringent testing. Each amplifier is operated 100 hours and then tested.

CONTENTS

PREPARED BY

M. A. MacDonell

Circuit Evaluation

Department

FAIRCHILD SEMICONDUCTOR, INSTRUMENTATION

844 Charleston Road, Palo Alto, California

I. STATEMENT OF SPECIFICATIONS

1. Gain Characteristics (Open Loop):

1.2	DC Voltage Gain:	Greater than 5,000,000
1.3	Gain-bandwidth (at unity gain):	Greater than 2,000,000

The gain is rolled off at approximately 6 db per octave.

1.3.1 Measurement Method (page 4)

2. Input Characteristics (Referred to Summing Junction):

2.1	Equivalent input DC voltage Temperature Coefficient:	Less than 10µvolts/°C averaged between -20°C and +80°C.

2.1.1 Measurement Method (page 5)

2.2	Input Impedance:	970,000 ohms at DC 500,000 ohms up to 50cps (typical)
2.3	Equivalent input noise:	Less than 100µvolts RMS, 10cps to 1000cps. (Referred to summing junction with $R_F = R_{1N} = 100,000$ ohms.)

2.3.1 Measurement Method (page 5)

2.4	Initial equivalent input offsets:	DC voltage offset less than 200µvolts; DC current offset less than 2.0n amps; (Offsets may be adjusted to zero by an external potentiometer supplied by the user. See Page 7.)

2.4.1 Measurement Method (page 6)

2.5	Drift per eight hours:	±50µvolts (at a constant temperature.) Referred to input (R_{in} = 1K R_f = 100K)

2.5.1 Measurement Method 2.4.1 (page 6)

3. Output Characteristics:

3.1	Maximum Voltage Swing:	±20V
3.1.1	Measurement Method 1.3.1 (page 4)	
3.2	Maximum Load Current:	2mA at ±20V 7mA at ±10V
3.3	Output Impedance:	Less than 30 ohms open loop
3.4	Maximum capacitive Load:	.001µf x forward gain
3.4.1	Measurement Method (page 6)	
3.5	Slewing Rate	4.8 Volts/µsec minimum
3.5.1	Measurement Method (page 7)	
3.6	Stability:	Amplifier shall not oscillate with output short circuited to the input (Pin C to Pin J).

4. Power Requirements:

+30V 30mA 1% regulation (Plus Load Current)

-30V 30mA 1% regulation (Plus Load Current)

No chopper drive is required. Change in equivalent input voltage due to power supply variations: ±40µV/% change. (R_f = 100K R_{in} = 1K.)

5. Package

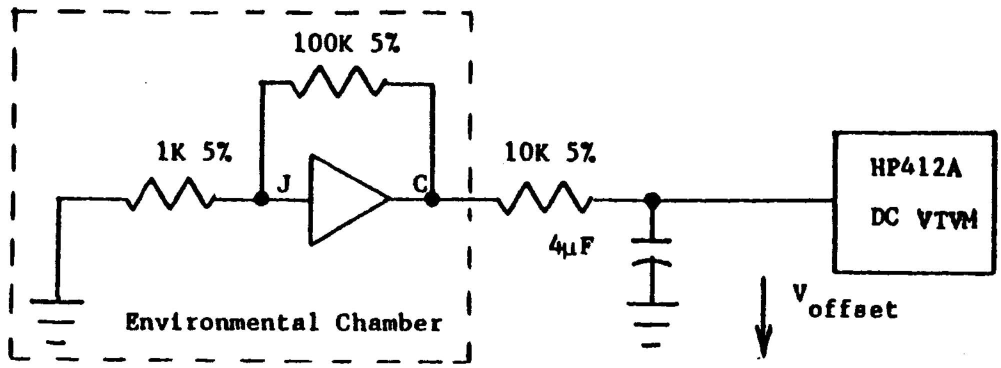
Metal shielded module, 4-5/8" x 4-7/8" x 1", to mate with 22 pin connector (supplied with amplifier).

6. Temperature Range

-20°C to +85°C for operation

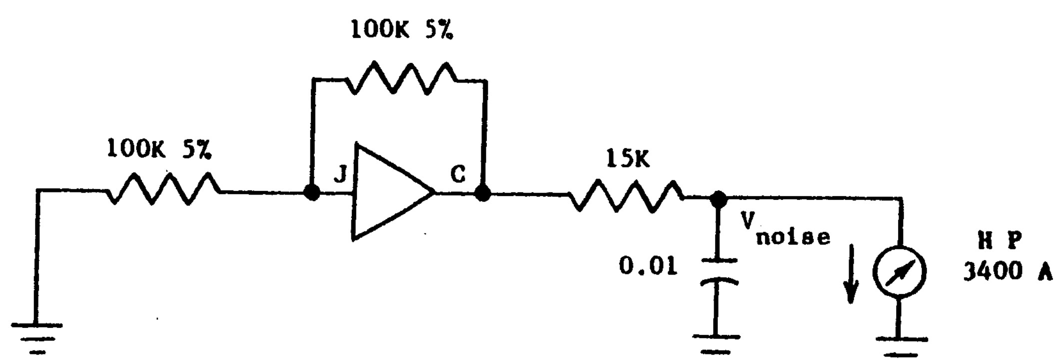
-55°C to +85°C for storage

2.1.1 Temperature Coefficient



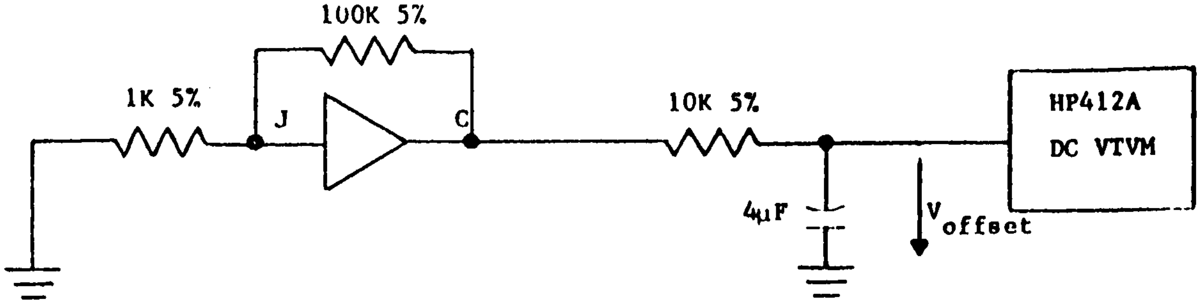
Measure and record offset after amplifier has been in -20°C environment for one hour. Measure and record offset after amplifier has been in +85°C environment for one hour. The change in offset must not exceed 105mv, (1.05/mv at summing junction).

2.3.1 Noise

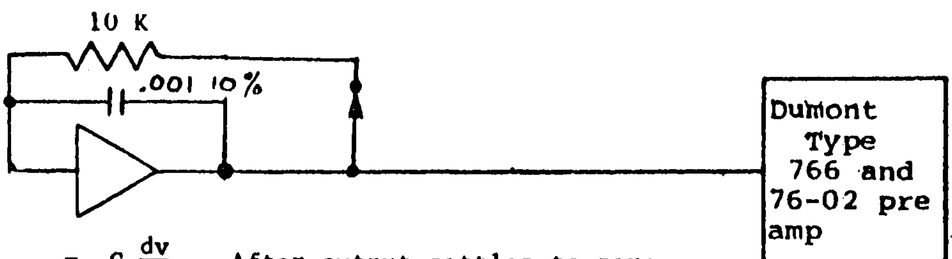


Measure and record V_{noise}. It must not exceed 200μVRMS.

2.4.1 Adj. Offset Voltage, Room Temperature: Off-set shall not exceed 200μV referred to input (20mV at output).

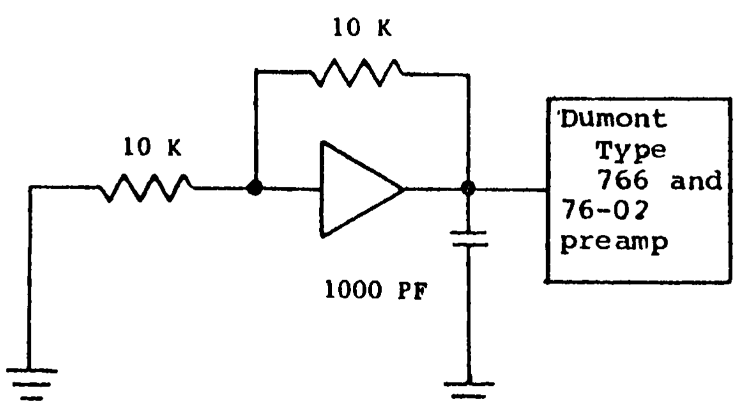


Current Offset:

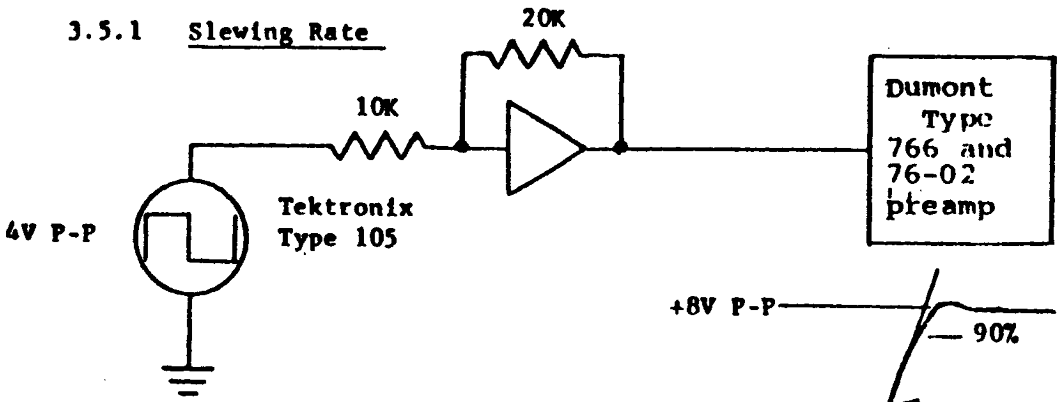


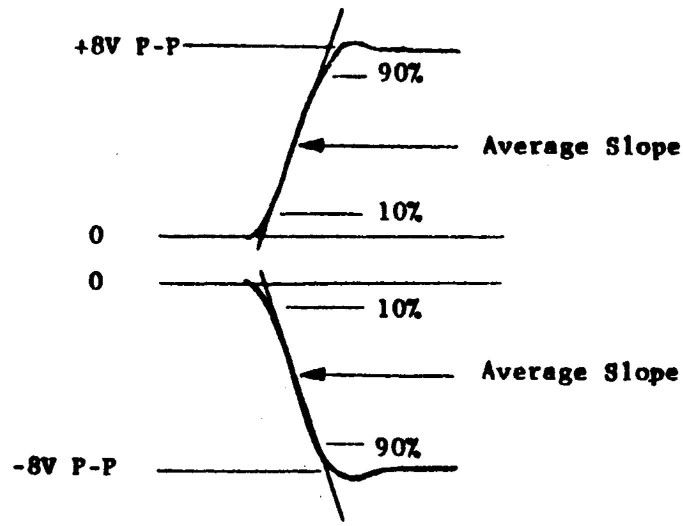
$I_{OFFSET} = C\frac{dv}{dt}$. After output settles to zero open switch and measure $\frac{dv}{dt}$

3.4.1 Maximum Capacitive Load: Amplifier shall not oscillate



3.5.1 Slewing Rate





The Average Slope shall not be less than 4.8V/μsec in either case.

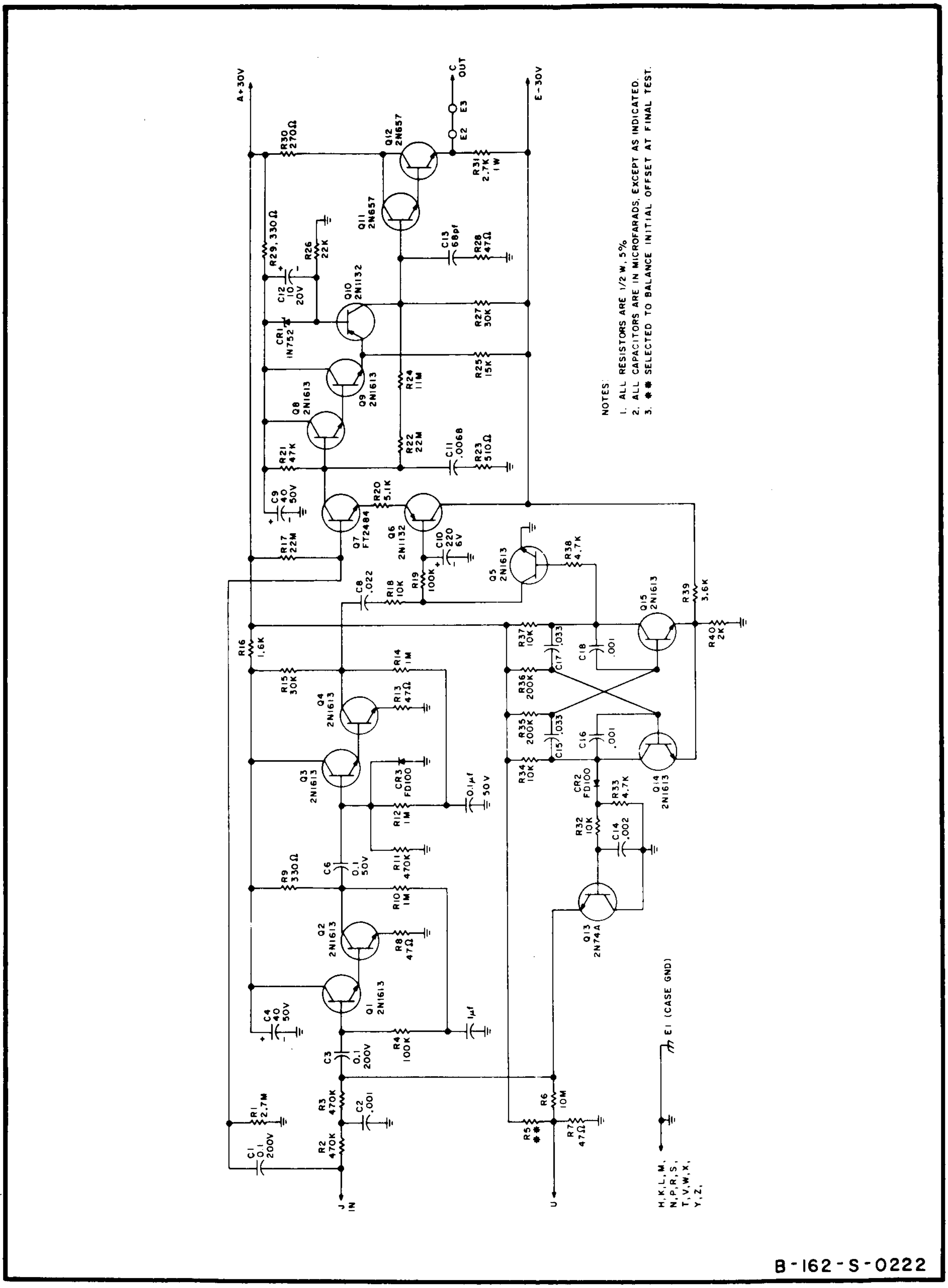


FIG. A-1 OPERATIONAL AMPLIFIER SCHEMATIC

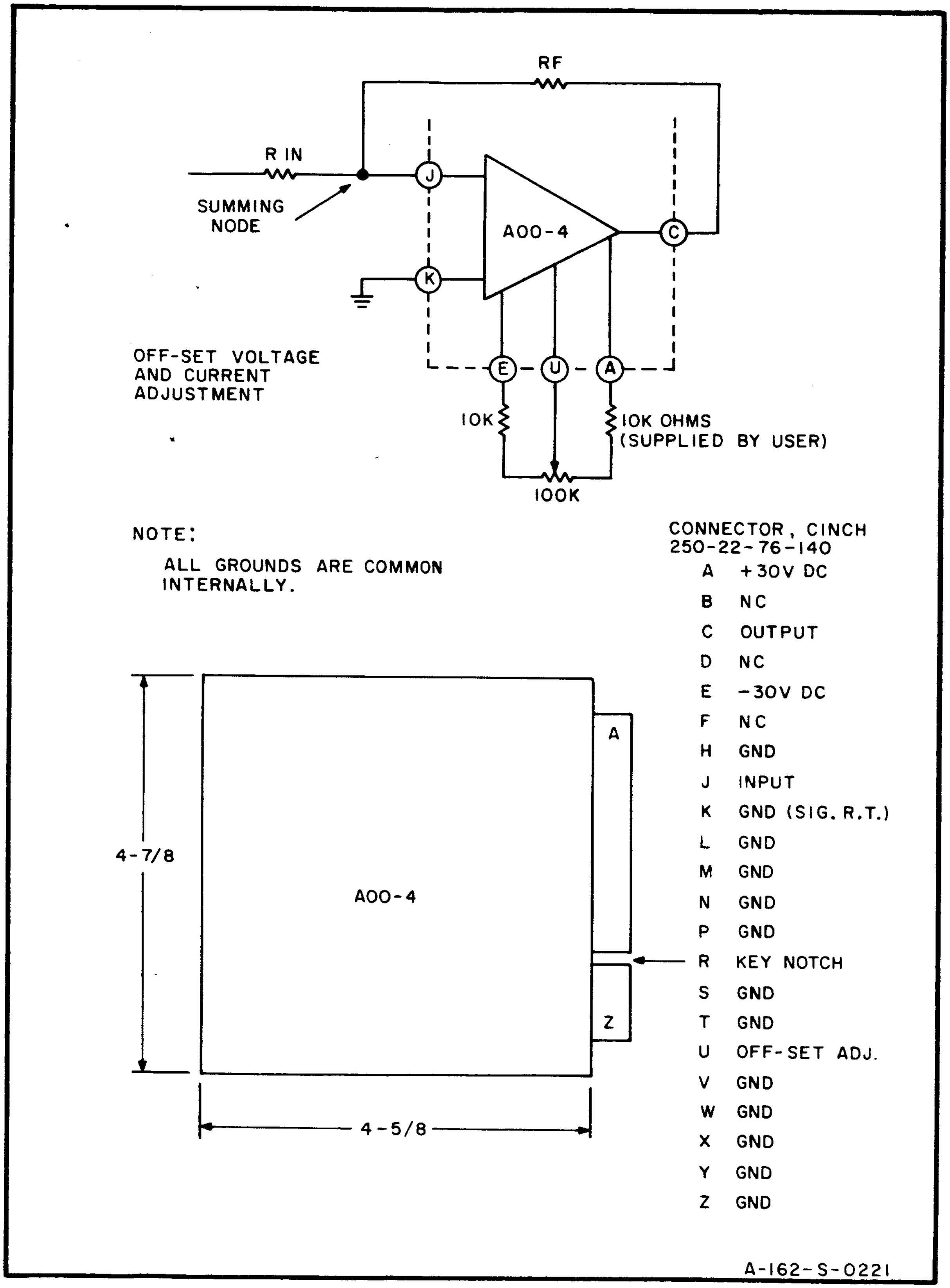


FIG. A-2 OPERATIONAL AMPLIFIER OUTLINE

B. VOLTMETER-INDICATOR

Flowmeter output information of three different types is displayed in numerical form by means of a servo-type voltmeter driving an in-line set of decimally inscribed cylinders. These are: the measured quantities, Average Flow rate, integrated flow or volume, and integration time; quantities which verify the precision of the proceeding; adjustable simulated flow rate for calibration of recorders; and quantities which serve as diagnostic aids in the event of equipment failure. In addition, the meter may be switched, in either polarity, to an external test lead for the measurement of DC voltages throughout the system. A schematic diagram of the voltmeter and the added switch circuit may be found in Fig. B-1. This is followed by a general description and a set of specifications and adjustment procedures. The latter are required only in the event of a component failure.

This appendix incorporates in part a reproduction of specifications by the United Systems, Corp., Dayton, Ohio.

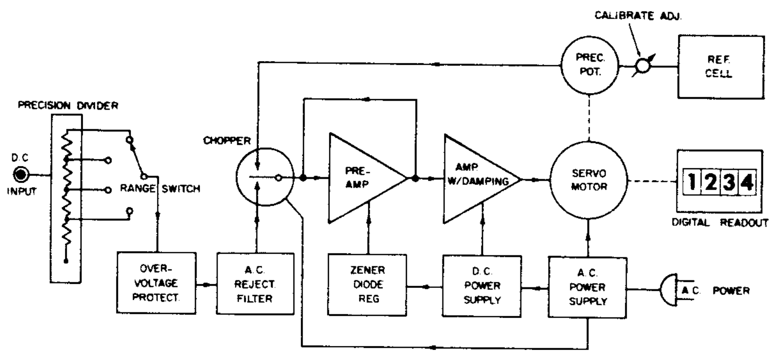
GENERAL DESCRIPTION

The DigiTec indicators are precision, transistorized, servo-balancing, potentiometer type instruments. In the various ranges offered they are capable of accurately indicating DC voltage digitally from 0.1 MV to 1000 V.

The operational description of the DigiTec is as follows:

The voltage under measurement, after passing through the divider, protection circuit and filter, is fed to one side of the chopper comparator. The opposite side of the comparator is fed from the motor-driven precision potentiometer which derives its voltage from either: (a) a temperature compensated Zener circuit, or (b) a carefully aged and calibrated reference cell(s).

The output of the chopper comparator provides an AC signal whose amplitude and phase is a function of the difference in magnitude and polarity of the DC voltages presented to the opposite side of the chopper input.



This AC signal then passes through a high impedance pre-amp to the power amplifier which incorporates a special damping feature. This damping effect makes possible extremely high slewing speeds with negligible overshoot and hunting at the null position.

The servo-motor, upon receiving this amplified signal, drives the balancing potentiometer (and digital indicator) in the direction to cancel the difference voltage seen across the chopper comparator. When this voltage difference becomes zero, the voltage indicator will accurately present the voltage under measurement in digital form.

Modular systems composed of the "elements" described in this manual will afford the characteristics defined below.

GENERAL SPECIFICATIONS.

1.	POWER REQUIREMENTS:	115 V, 60 cycle, 25 watts. (220V, 50 cps on overseas models)
2.	READOUT:	Digital, illuminated, 1000, 2000, or 4000 digits, full scale.
3.	ACCURACY:	± 0.1% Zener reference units (60° to 115° F). ± 0.2% Hg cell reference units (60° to 115° F).
4.	LINEARITY:	0.05% all units.
5.	RESOLUTION:	0.05% of full scale.
6.	INPUT IMPEDANCE:	<u>Single range</u> - essentially infinite at balance, 500 K before balance. * <u>Multi-range</u> - 2.2 meg. at balance, 500 K before balance.
7.	AC REJECTION:	50 DB at 60 cycle. (Except 40 DB at 60 cycle for 0.1 V reference units.)
8.	BALANCING TIME TO FULL SCALE:	3.5 sec. 1000 digits. 4.5 sec. 2000 digits. 7.5 sec. 4000 digits.
9.	OVERLOAD PROTECTION:	<u>Single Range</u> - to 500 volts, either polarity. <u>Multi-Range</u> - to 1250 volts on any but lowest range; 500 volts on low range.

*(Except 100K before balance on .1 V reference unit.)

OPERATION

OPERATING PROCEDURE

For Multi-Range instruments set Range Selector to the desired range. If voltage is unknown, set to highest range and downrange as required. Indication of "Full Scale Limit" for any range is evidenced by reading in excess of "1020" on "1000" digit instruments.

SENSITIVITY ADJUSTMENT

Sensitivity is adjusted by a Trimmer Potentiometer, R31, located on the Amplifier Board. (Refer to outline drawing of Amp-Ref unit.) Turning "CW" increases sensitivity, "CCW" decreases sensitivity.

CALIBRATION

A. GENERAL PROCEDURE AND PRECAUTIONS.

1. The DC voltage supply used for calibration should be stable and accurate to at least .01% for "Z" models and .02% for others.

2. For maximum accuracy, calibration should be accomplished in a draft free area at 70° to 80° F.

3. Use a non-metallic screwdriver for all adjustments.

4. Connect instrument to 110 to 115V - 60 CPS power supply with Terminal 15 (TB1) connected to ground. (Refer to Interconnecting Wiring Diagram).

5. Turn instrument on and allow to warm up for at least 30 minutes prior to calibration.

6. All calibration adjustment pots are locked at the factory against inadvertent movement with a drop of Glyptol. There will be a slight resistance to motion until this spot is broken.

B. REFERENCE VOLTAGE ADJUSTMENT. (Locate Calibrate Adjustment on Ref. Board. See Outline Drawing of Amp/Ref unit).

1. For Multi-range instruments, set Range Switch to lowest voltage range.

2. Carefully Zero instrument with Input Terminals shorted. (TB1-1 to TB1-2).

3. Apply accurately known "Standard" voltage of proper value to produce full scale reading to Input Terminals with Positive lead connected to TB-1 and Negative lead connected to TB1-2.

4. Turn "Calibrate Adjustment" as required until "Standard" reading is observed. Note: Calibrate Adjustment is located on Reference Board. (See outline drawing of Amp-Ref unit). (R14 on Mercury Cell Models and R51 on Zener Models).

5. Para. B-1 thru B-5 completes the calibration adjustment for a single-range unit. For a multi-range unit this completes the calibration of the <u>lowest range</u> and also sets the span for all additional ranges.

6. If an instrument with Mercury Cell Reference cannot be calibrated properly (meter reads high and cannot be lowered to "Standard" voltage), replace Mercury Cell. See instructions on Mercury Reference Cell replacement.

C. DIVIDER ADJUSTMENT - MULTI-RANGE INSTRUMENTS

1. Proceed with "Reference Voltage Adjustment".

2. Divider Adjustment Trimmers are located below Range Switch on Remote Readout Units (See outline drawing of Series 3693-3602 Readouts).

3. Lowest (or base) range has already been set in Para. B.1-5. Set Range Switch to next highest range. Carefully zero instrument with Input Terminals shorted.

4. Apply accurately known voltage to Input Terminals of proper value to produce full scale reading. Adjust Trimmer R44 as required to produce desired reading.

5. Repeat with remaining ranges. R45 sets 3rd highest and R46 the highest range. Divider Adjustments are not inter-acting. Any range may be reset without disturbing the others.

D. FACTORY RECALIBRATION

USC offers complete and prompt recalibration service at nominal charge. This includes replacement of "Reference Cell". The recalibration will be conducted with .01% standards traceable to N.B.S.

MAINTENANCE

LUBRICATION

NO lubrication is required by the mechanical components used in the instrument. Oil or grease applied may only serve to accumulate dirt and impair operation.

CLEANING

To clean display wheels: Loosen screw holding Lamp Socket and swing up. Use damp cotton swab followed by dry swab to clean characters. (Never use solvents or abrasives.)

COMPONENT REPLACEMENT OR REPAIR

1. Carefully check applicable Schematic Wiring Diagrams before making any repairs. When replacement parts are procured from USC, the following data must be furnished.

    a. Model and Serial Number.

    b. Part Stock Number (See Parts List).

2. USC offers complete and prompt repair at nominal charge.

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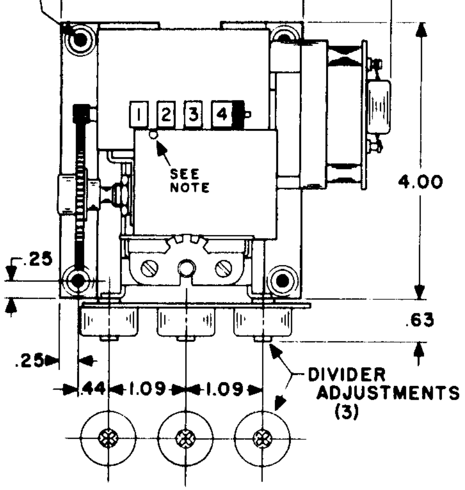
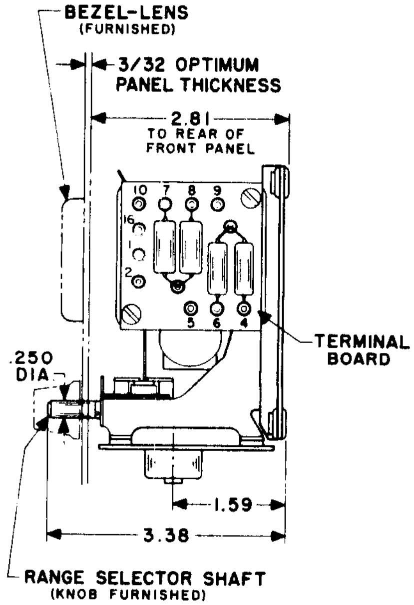
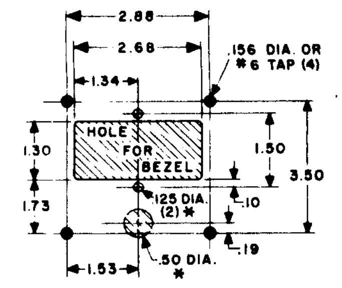




SERIES 3693

REAR MOUNTING

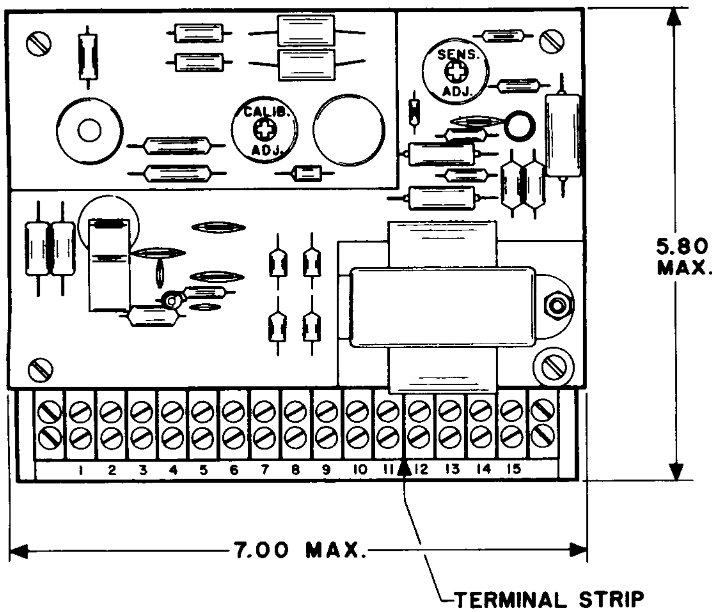


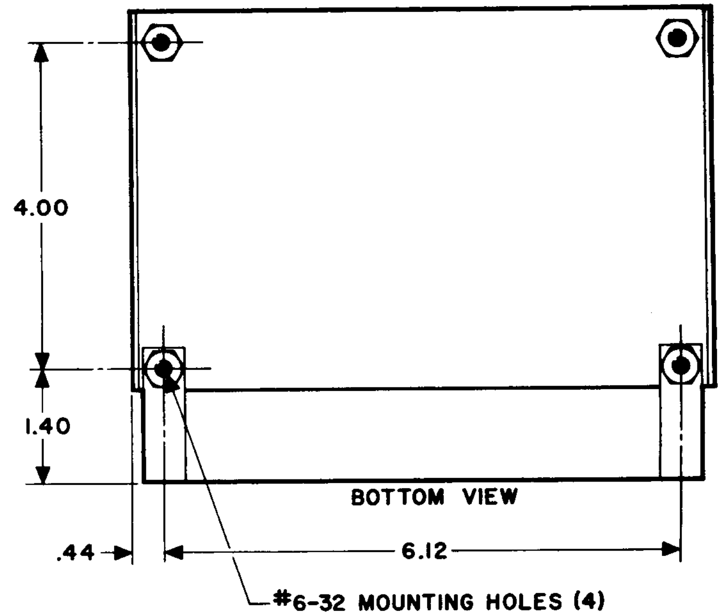
*FRONT PANEL HOLES

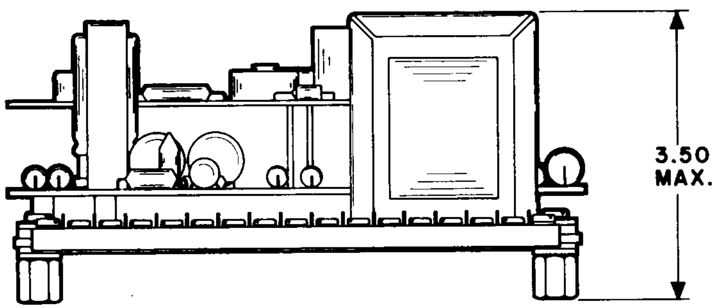
INSTALLATION HOLES

ORDERING INFORMATION	
SERIES NO.	VOLTAGE RANGES
3693-1	1.000, 10.00, 100.0 & 1000.
3693-2	2.000, 20.00, 200.0 & 1000.
3693-4	4.000, 40.00, 400.0 & 1000.

NOTE:
ILLUMINATED DECIMAL POINT SHIFTS WITH RANGE SELECTOR SETTING

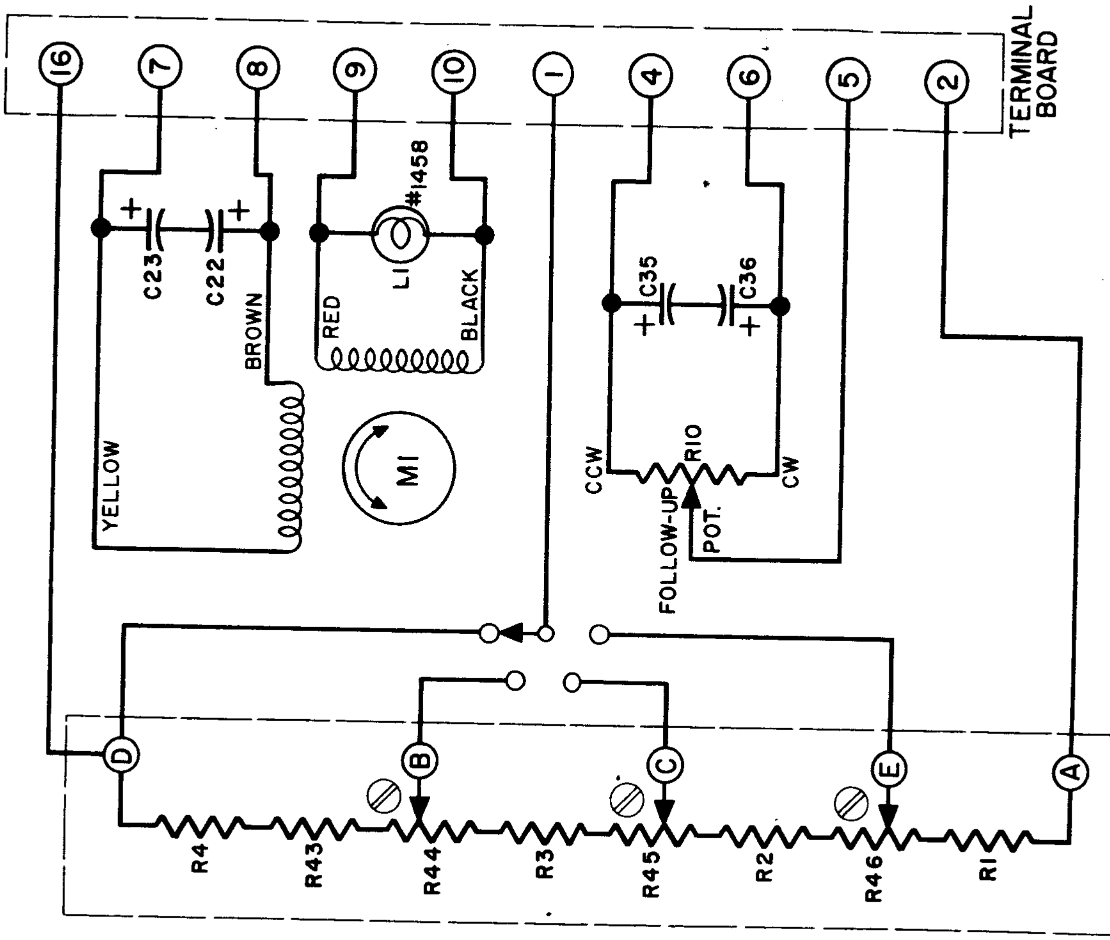




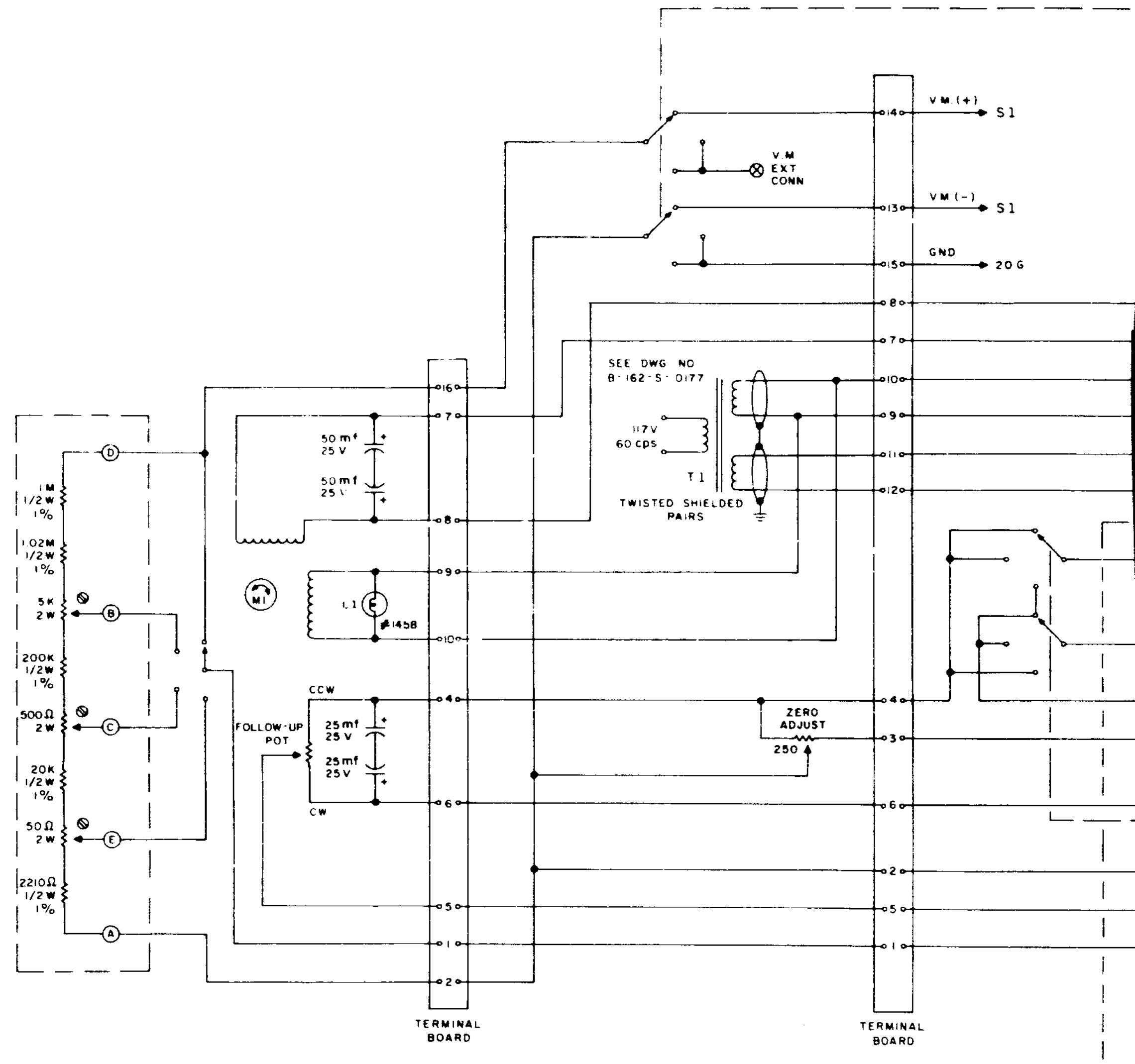


REMOTE AMPLIFIER & REFERENCE UNIT
SERIES 3765

ORDER NO.	REFERENCE VOLTAGE	REFERENCE SOURCE
3765-1	0.1 V	HG CELL
3765-2	0.1 V	ZENER
3765-3	1.0 V	HG CELL
3765-4	1.0 V	ZENER
3765-5	2.0 V	HG CELL
3765-6	2.0 V	ZENER
3765-7	4.0 V	ZENER



MULTI-RANGE DISPLAY UNITS
SERIES NO. 3693



MULTI-RANGE DISPLAY UNITS SERIES NO. 3693

NOTES

ALL RESISTORS 1/2W 5% EXCEPT AS NOTED.

F/168

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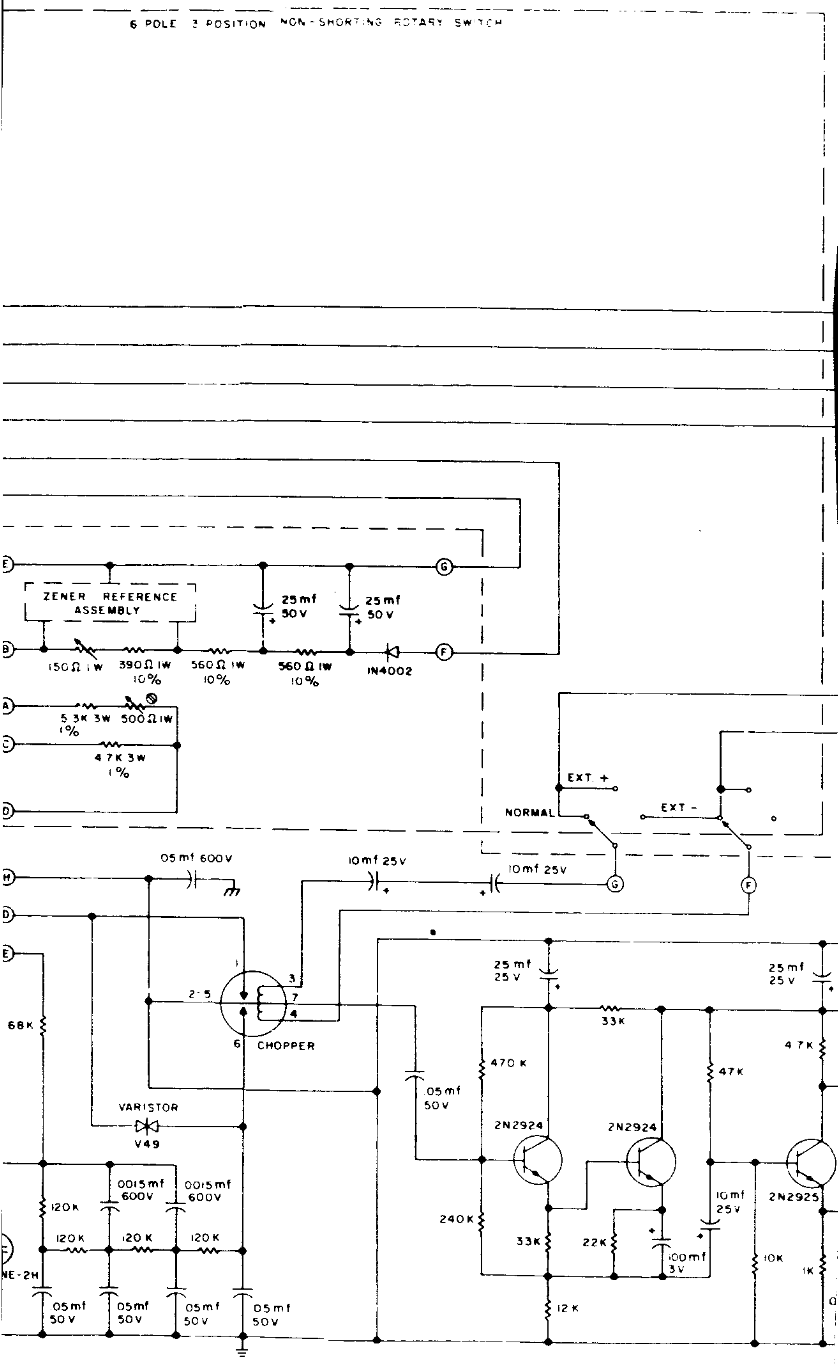
– ELECTRONICS RESEARCH LABORATORIES



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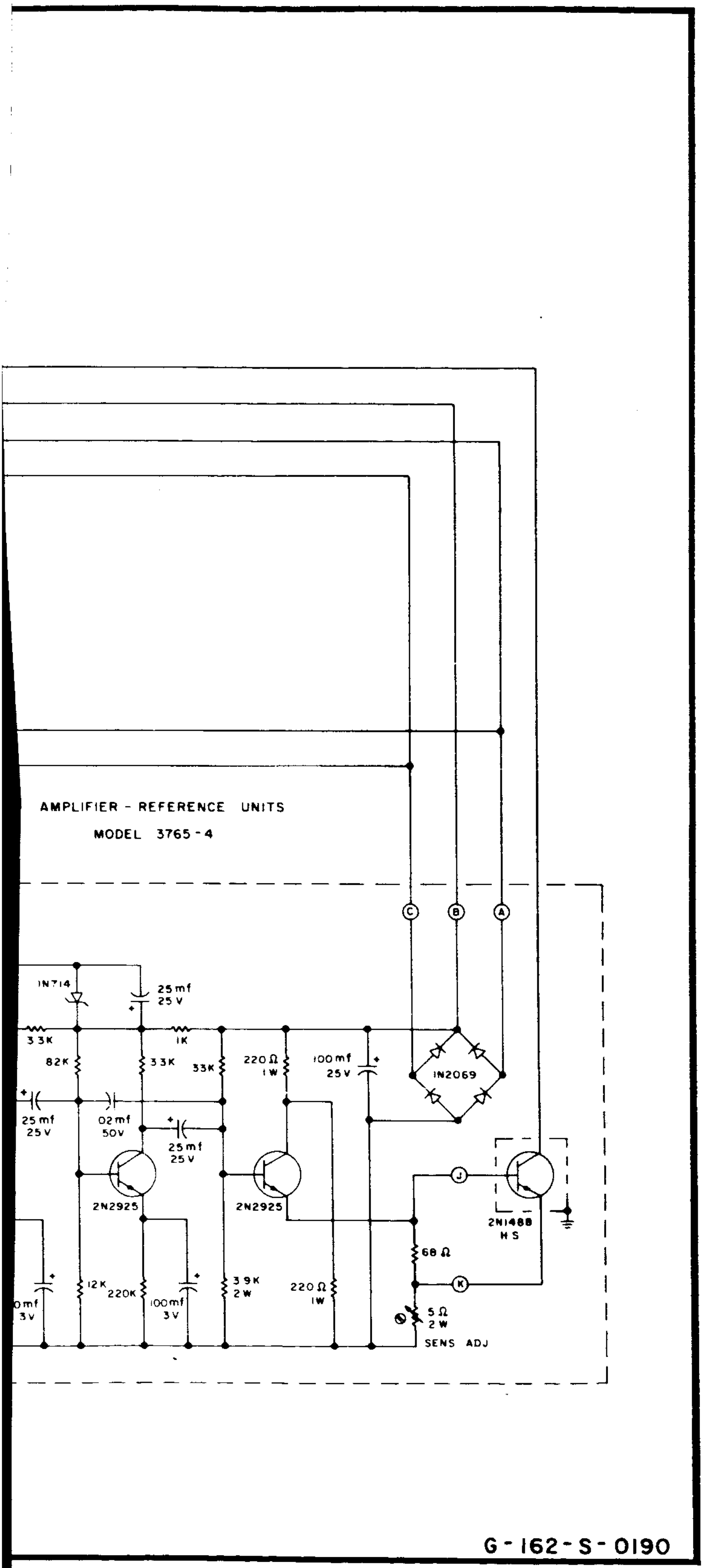


FIG. B-1 VOLTMETER - INDICATOR

C. DETERMINATION OF SECOND ORDER COMPENSATOR

The assumed form of the compensator is shown in Fig. 9. The voltage transfer function for the complete system is given by

$$\frac{s}{s+\alpha}\left(\frac{s}{s+\epsilon} + G(s)\right) \triangleq 1$$

from which

$$G(s) = (\alpha + \epsilon)\,\frac{s + \frac{\alpha\epsilon}{\alpha+\epsilon}}{s(s+\epsilon)} \tag{1}$$

where α and ϵ are respectively given and arbitrary reciprocal time-constants. The assumption that the amplifier gain A is so great that the output voltages $E_2 = \hat{E}_2$ of the networks N and $\hat{N}$ are negligible enables the voltage transfer function E_o/E_1 to be conveniently expressed in terms of the network Y parameters. We have $I_2 = -\hat{I}_1$ or $y_{21}E_1 = -\hat{y}_{21}E_o$ from which

$$\frac{E_o}{E_1} = -\frac{y_{21}}{\hat{y}_{21}}\ . \tag{2}$$

By inspection of the figure

$$E_1 = E \frac{\frac{1}{y_{11}}}{\frac{1}{y_{11}} + \frac{1}{Cs}}$$

which may be written

$$\frac{E_1}{E} = \frac{s}{s + \frac{y_{11}}{C}} \quad . \tag{3}$$

Multiplying (2) and (3) we obtain

$$-G(s) = \frac{E_0}{E} = - \frac{y_{21}}{\hat{y}_{21}} \frac{s}{s + \frac{y_{11}}{C}} \quad . \tag{4}$$

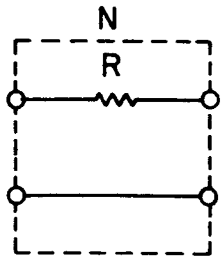
We proceed to assume a network N, and then attempt to synthesize an $\hat{N}$ having the property, derived from (4), that

$$\hat{y}_{21} = \frac{y_{21}}{G(s)} \frac{s}{s + \frac{y_{11}}{C}}$$

or more specifically by using (1),

$$\hat{y}_{21} = \frac{y_{21}}{\alpha + \epsilon} \frac{s(s + \epsilon)}{s + \frac{\alpha\epsilon}{\alpha + \epsilon}} \frac{s}{s + \frac{y_{11}}{C}} \quad . \tag{5}$$

If the input network is as shown below, then



$$y_{11} = \frac{1}{R} \tag{6}$$

$$y_{21} = -\frac{1}{R} \tag{7}$$

and, using (5),

$$\hat{y}_{21} = \frac{-1}{(\alpha + \epsilon)R} \frac{s^2(s + \epsilon)}{(s + \frac{\alpha\epsilon}{\alpha + \epsilon})(s + \frac{1}{RC})} .$$

Let

$$\frac{1}{RC} = \epsilon \tag{8}$$

then

$$-\hat{y}_{21} = \frac{1}{(\alpha + \epsilon)R} \frac{s^2}{s + \frac{\alpha\epsilon}{\alpha + \epsilon}} .$$

By performing the indicated division we obtain $-\hat{y}_{21}$ in the following form:

$$-\hat{y}_{21} = \frac{s}{(\alpha + \epsilon)R} - \frac{\frac{\alpha\epsilon}{(\alpha + \epsilon)^2 R} s}{s + \frac{\alpha\epsilon}{\alpha + \epsilon}}$$

where we distinguish the positive and negative parts by writing

$$-\hat{y}_{21} = \hat{y}_{21p} - \hat{y}_{21n} \quad .$$

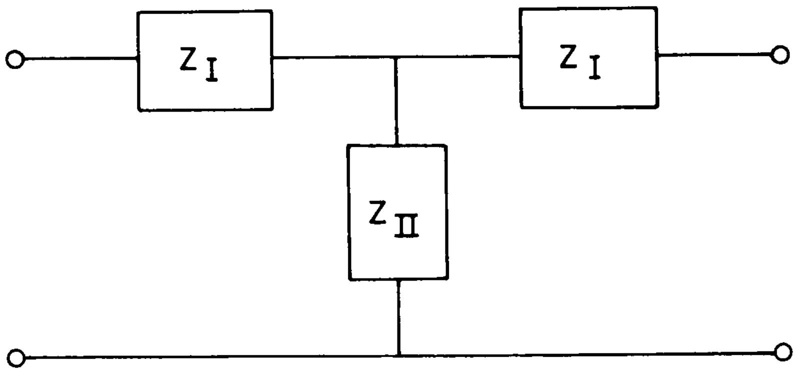
Assume: that the network is symmetrical

$$\hat{y}_{11} = \hat{y}_{22}$$

that

$$\hat{y}_{11} = y_{21p} + y_{21n}$$

that the network is a T as shown below



Then, by the application of standard network formulas and, (6) and (7),

$$Z_I = \frac{1}{\hat{y}_{11}-\hat{y}_{21}} = \frac{1}{2\hat{y}_{21p}} = \frac{(\alpha + \epsilon)R}{2s}$$

$$Z_{II} = \frac{-\hat{y}_{21}}{|y|} = \frac{\hat{y}_{21p} - \hat{y}_{21n}}{4\hat{y}_{21p}\,\hat{y}_{21n}} = \frac{1}{4\hat{y}_{21n}} - \frac{1}{4\hat{y}_{21p}}$$

$$= \frac{s + \frac{\alpha\epsilon}{\alpha + \epsilon}}{4\,\frac{\alpha\epsilon}{(\alpha + \epsilon)^2 R}\,s} - \frac{(\alpha + \epsilon)R}{4s}$$

$$= \frac{s + \frac{\alpha\epsilon}{\alpha + \epsilon} - \frac{\alpha\epsilon R}{(\alpha + \epsilon)R}}{4\,\frac{\alpha\epsilon}{(\alpha + \epsilon)^2 R}\,s}$$

$$= \frac{1}{4\,\frac{\alpha\epsilon}{(\alpha + \epsilon)^2 R}} = \frac{(\alpha + \epsilon)^2}{4\alpha\epsilon}\,R \quad .$$

If in addition to condition (8) we set

$$\epsilon = \alpha$$

then we obtain the particularly simple result:

$$Z_I = \frac{1}{Cs}$$

$$Z_{II} = R \ .$$

Then

$$G(s) = \frac{y_{21}}{\hat{y}_{21}}\,\frac{s}{s + \frac{y_{11}}{C}} = \frac{\frac{1}{R}\left(s + \frac{1}{2RC}\right)}{\frac{C}{2}\,s^2}\,\frac{s}{s + \frac{1}{RC}}$$

$$= \frac{2}{RC} \frac{s + \frac{1}{2RC}}{s(s + \frac{1}{RC}} = 2\alpha \frac{s + \frac{\alpha}{2}}{s(s + \alpha)} \quad .$$

The complete compensator transfer function is

$$\frac{s}{s + \alpha} + \frac{2\alpha}{s} \frac{s + \frac{\alpha}{2}}{s + \alpha} = \frac{s + \alpha}{s} \quad .$$

D. ATTENUATOR SYNTHESIS

It is required that (1) the closed-loop gain of the Second Amplifier be adjustable easily and predictably to within 0.1 per cent of any number between about 6 and 60, (2) that the maximum output voltage range be about $\pm$ 30V, (3) that the minimum bandwidth be 50 kc, (4) that the step response be without overshoots and (5) that the input be high-pass coupled and that the time-constant of the input coupling network be independent of gain. (5) suggests (6) that the gain be controlled by adjustable feedback. (4) and (6) imply (7) that the open-loop frequency response decrease at no greater rate than 20 db/decade over the 20 db range of interest. (3) and (7) imply (8) that the closed loop cut-off frequency will be at least 500 kc at the lowest gain setting, which suggests that the attenuator impedance level should not be too high on account of stray capacitance while (2) suggests that it should not be low. (1) suggests that a multi-turn linear potentiometer should not be used because its proportional resolution depends upon its setting and (2) and (8) suggest that it would be unsatisfactory because the frequency response of such potentiometers is poor unless the resistance is low. In short, what is needed is an attenuator of several thousand ohms impedance which is adjustable over a 10:1 range by steps of ratio 1.002 or less and which has a bandwidth of at least several megacycles. Such an attenuator was not found to be commercially available so it was constructed as a sequence of ladders.

The Second Amplifier feedback path contains such ladder attenuators. If the resistance looking into the ladder directly is the same as that seen looking into it through an added section, it is known as the iterative resistance R_o. If, in a typical Pi section of the ladder, the series resistance is R_A and the shunt resistances are each $2R_B$, then the gain k and iterative resistance are

$$k = \frac{2R_BR_o}{2R_BR_o + R_AR_o + 2R_AR_B} \quad \text{and} \quad R_o = 2R_B\left(\frac{R_A}{4R_B+R_A}\right)^{\frac{1}{2}} .$$

Having chosen R_o and k we can find

$$R_A = \frac{1 - k^2}{2k} R_o \quad \text{and} \quad R_B = \frac{1 + k}{2(1-k)} R_o .$$

If the ladder is terminated at each end by R_o, then the resistance looking into any node, with respect to the common (ground) node, is $R_o/2$. If the attenuator is connected to a voltage source through an input resistance R_o and terminated by R_o, then the attenuation may be varied by means of the simplest possible type of selector switch connected to the nodes, while the equivalent source resistance $R_o/2$ between switch arm and ground may serve as the input resistance of another attenuator. Ten-section ladders, cascaded in any order, with gain ratios (k) differing by powers of 10 may have their attenuation specified in decimal notation. For the coarsest range (most significant digit), the section gain should be $k_1 = (K)^{0.1}$ where K is the required ratio of maximum to minimum attenuation. For the next range the section gain should be $k_2 = (k_1)^{0.1}$, etc. The insertion-loss (minimum attenuation) of this type of attenuator is high but it is such that the least overall gain required (6) is obtained with nearly equal input and feedback resistors.

In Fig. 30, the Second Amplifier (K 13) is the voltage source, R66 is the input resistor and R46 is the terminating resistor for the attenuator (R47-65,S 7) which is first and which has the finest increments. Those first, second (R26-45;S 6) and third (R8-25;S 5) attenuator parameters of interest are shown below.

Attenuator	R_A	$2R_B$	$\frac{2R_BR_o}{2R_B + R_o}$	R_o	$\frac{R_o}{2}$
First	3.3	1.5M		1500	750
Second	17.8	71.5K	750 + 41.2	800	400
Third	100	4000	400	$\left(\frac{4000}{9}\right)$	222.2

The lowest resistance presented to the Second Amplifier is about 1840 ohms (in the minimum overall gain condition). The lowest value of resistance required, relative to R_0, is R_A in the attenuator for the least significant digit. This resistance was maximized by letting its attenuator be the first in the series of three. The first has the highest R_0 . Various tricks were used to save resistors (R_8 is the parallel resistance of $2R_B$ and R_0 for its ladder) and to shift the required resistances to those of commercially available resistors (as by the addition of R45). The ratio of maximum to minimum attenuation is slightly less than 10:1 and the least increment is slightly over 0.2 per cent. These compromises were deemed preferable to adding another decade. Make-before-break thumbwheel switches, should have been used but were not available at the time of construction.

E. PROBE CONSTRUCTION

The electromagnetic probe developed for the present system uses a direct current reversed approximately 400 times per second to energize its magnet. This square wave produces a non-fluctuating magnetic field during a portion of each half cycle.

Currents circulating in the conducting environment surrounding the probe have a wave shape similar to the voltage across the magnet coil. Any movement of the artery within the lumen or of the probe with respect to the neighboring bodies changes the current paths and the resulting artifact voltages.

The peak value of the voltage spike can be minimized during probe assembly by properly orienting the magnetic field with respect to the electrode axis.

Poor electrical insulation or shielding can inject an artifact into the signal leads that duplicates the magnet voltage curve, Fig. E-1c, or the magnet current curve, Fig. E-1b. In either case the probe is useless unless such sources of error are eliminated by means of carefully chosen materials and great care in probe assembly.

Several magnet designs were evolved in an effort to meet the requirements of heat dissipation, saturating magnetic core, voltage breakdown of magnet insulation, and leakage flux outside the useful air gap.

The pancake type of coil envelopes a fairly large segment of the lumen, thereby cutting down the waste flux. However, the mean radius of magnet turn is very large, making

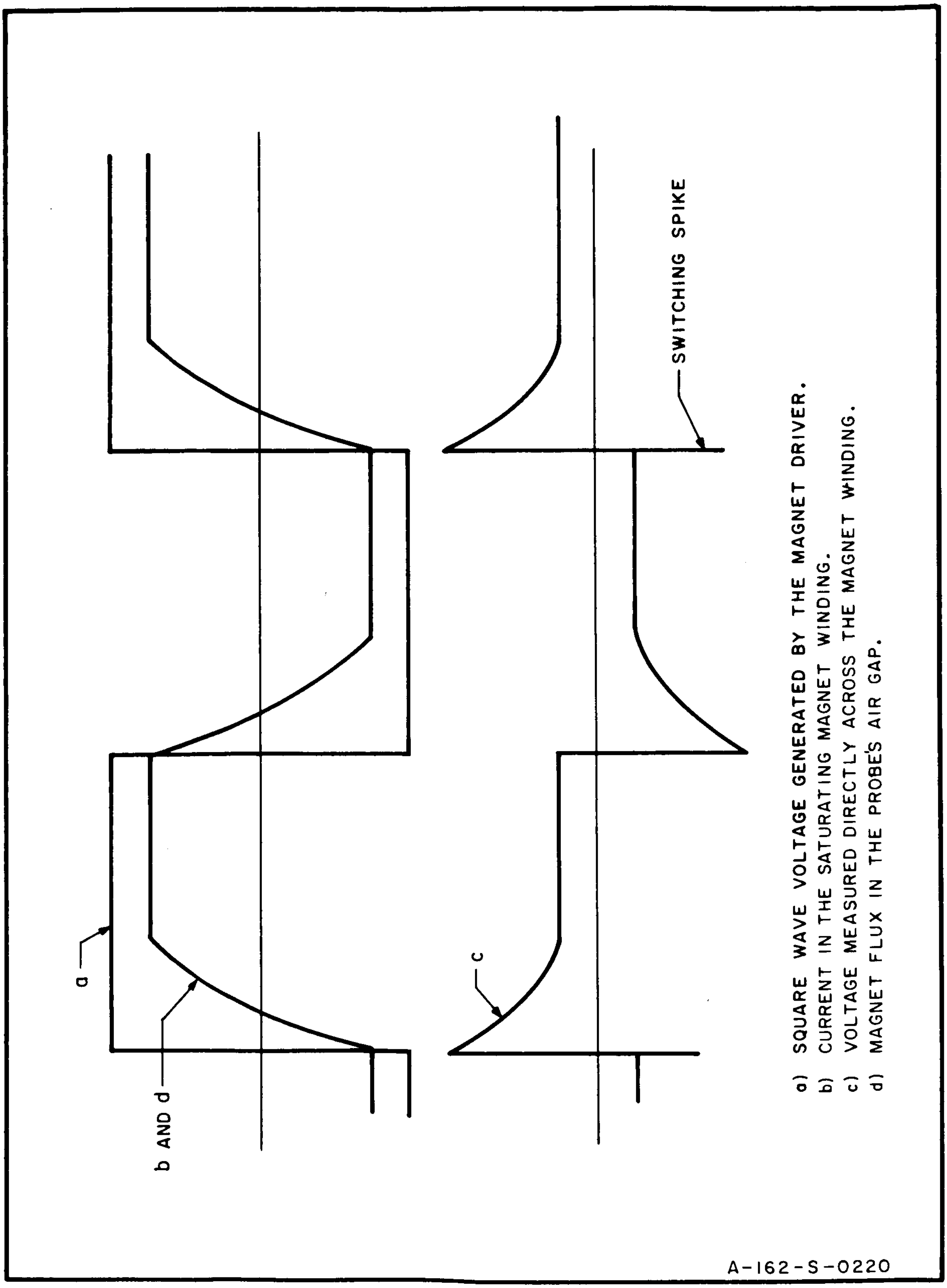


FIG. E1 SATURABLE MAGNET WAVEFORMS

the wire resistance and heat dissipation at least one order of magnitude too high. The large pancake coils lend themselves mainly to coreless construction and non-saturating magnets.

To minimize heat dissipation, the mean length of magnet turn must be small. This calls for a minimum magnet core area inside the magnet coil which in turn requires a material with a high flux density (B) before saturation. Deltamax (Arnold Eng. Co.,) was found to be a rather ideal core material. In addition to having the above properties, it saturated very sharply (very square loop) and was easily bent to shape for fabrication.

The signal output of the probe is limited by the attainable flux density which is limited by the allowable physical size and permissible heat dissipation. One hundred gauss in the useful air gap seemed to be a maximum practical flux density, in a 12-mm lumen for a one (1) watt dissipation in the magnet. The generated voltage tends to be independent of the lumen size. The voltage increases with the length of the (fluid) conducting path but any increase in lumen diameter causes a decrease in flux density.

When the square wave of applied voltage - and the resulting magnetic field - reverse polarity, a large induced voltage results. The induced voltage and resulting currents produce errors (artifacts) which the probe and circuit design should minimize. In fact, any fluctuations in magnet strength will induce corresponding voltages by transformer action.

The velocity signal output from the probe may be accompanied by artifacts due to the pickup-electrodes surface condition, and the existence of induced currents in and about the probe in a normal conducting environment.

It is desirable to minimize the time required to bring the magnetic flux up to its maximum steady value. In principle this can be done by means of a nearly constant-current source, which is difficult to build, or by means of a less sophisticated source which drives the core into saturation.

Since a current regulator was not available during the early phase of probe development, the major design effort was toward the rapid attainment of a constant flux density by means of a saturable core.

The effect of a saturating magnetic core is best described in Fig. E-1. Since the self inductance of the magnet drops as the current increases, the time constant determined by the effective inductance and resistance in the circuit also drops. The result is that the flux, current and voltage waveforms approach their final values in a manner which is more abrupt than the asymptotic approach in the non-saturating case.

By using a very square loop core material such as Deltamax, and a reasonable amount of current overdrive, the inductance falls to approximately 25 per cent of its unsaturated value and a flat topped square magnetic field results.

The ideal "U" shaped magnet has a distributed winding on a tapered core. But the advantages of distributed over bobbin-wound structures do not compensate for the increased construction difficulties.

With 100 gauss as the design flux density in the useful air gap, it was found that the maximum size saturable core was 1/16 in. X 1/8 in. and that 300 ampere turns were necessary for full saturation. Iron filing test patterns showed many flux leakage paths; approximately 80 per cent of the total field bypassed the useful air gap.

In a three coil magnet, each coil is surrounded by its own leakage flux and, at saturation, parts of the core have a permeability equal to that of air. By increasing the core area at the pole faces and between coils the total flux was increased and it was better confined to the useful flux path. Moreover, additional saturation and squareness of magnetic field was obtained. The penalty paid for this additional saturation is the increased mutual inductance. For a field of 100 gauss, heat dissipation and magnetic saturability tend to be independent of lumen size in the range of 5.0 to 15.0 mm.

Full saturation of the core became and remained the one most important design criterion and most tests of a partially assembled magnet were directed toward this end. A General Radio 650A impedence bridge, with an externally adjustable direct current source, was used to measure magnet inductance at all stages of assembly. Measurements of field strength were made at various points in the magnet structure at the design maximum current of 0.5 ampere. By using DC excitation, an RFL model 1890 gaussmeter could be used to indicate field strength directly. In contrast to this simple measurement, if square wave magnet drive is used, the current waveform is quite unknown, and the <u>peak</u> flux density can only be read with gaussmeter-oscilloscope instrumentation.

A high degree of saturation is also obtainable by closing the useful air gap to zero, while reading the inductance and losses (Q) of the magnet on the impedance bridge.

An example of the variation in coil saturation and field strength can be seen in the data for Deltamax core magnet D-2.

The individual coils consist of 200 turns of #30 heavy Teflon (TFE) magnet wire (Thermal Wire of America) layer wound on a bobbin having a 1/8" X 1/16" core opening (Cosmo Plastic #B-1454). Each coil measured approximately 0.95 mh on a closed Deltamax core.

The 3 coil assembly D-2, has 13 strips of Deltamax (.004" thick each) for a core. The ends of the core were fanned out to become pole faces about a tube with 12 mm lumen. The magnet parameters varied with DC current as follows:

(a) L(0) = 10.5 mh, Q = 17

L(.3)= 3.4 mh, DQ = 4.1

L(.5)= 1.08 mh, DQ = 1.25

where L(i) is the inductance at a DC current of i amperes. These measurements show a high degree of saturation and consequent drop of inductance and "Q," as the design maximum magnetizing current is approached.

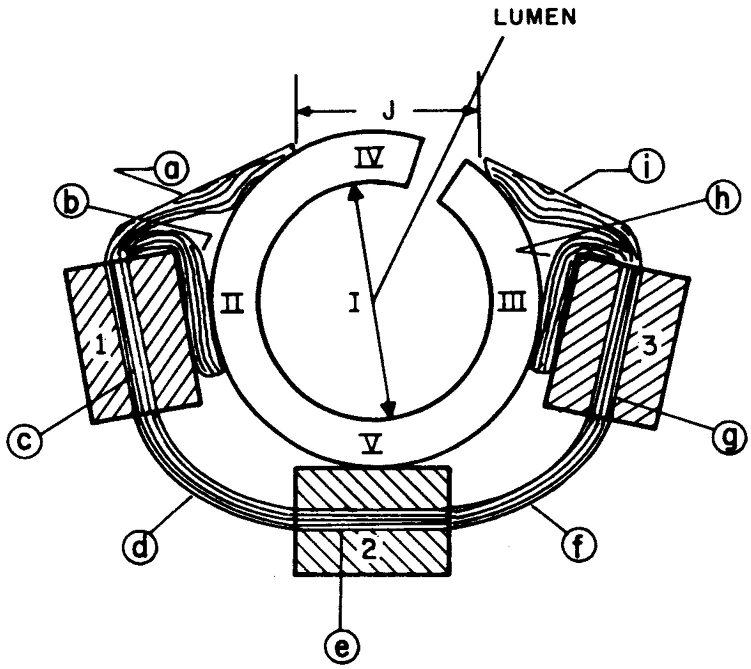
When this same magnet assembly (D2) had the ends of the magnet pole trimmed so that the air gap cross section was reduced, less total flux traversed the gap and poorer saturation was obtained:

(b) L(0) = 9.5, Q = 17.

L(.3) = 4.12, DQ = 6.3

L(.5) = 1.23, DQ = 1.42

To ensure non-saturation of the pole faces, they were padded, that is, additional layers of Deltamax strips were inserted as shown below

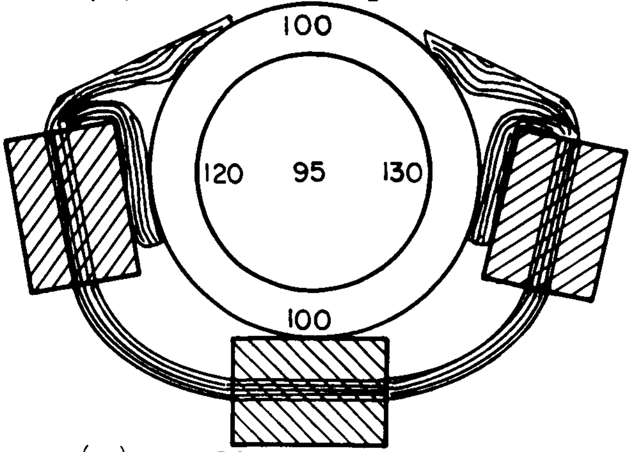


5 layers each in positions (b) and (h) ; 5 layers each in positions (a) and (i) . This added core material gives the pole faces at least 75 per cent more area than the saturated areas within the coil positions (c) , (e) and (g) . The higher permeability of the unsaturated sections produces slightly more flux which in turn saturates the magnet a little more as shown by the following results:

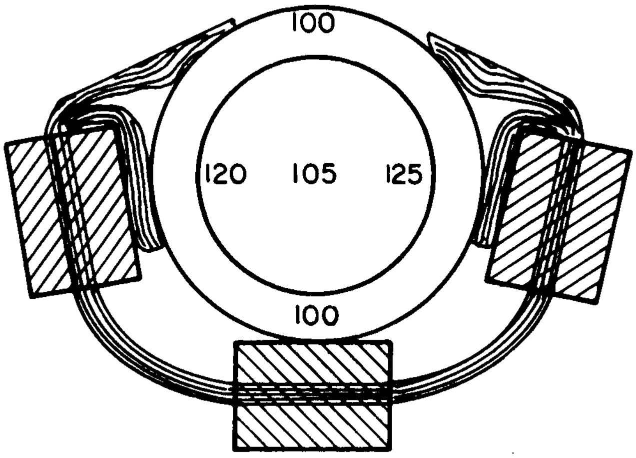
(c)	L(0) = 10.8 mh,	Q = 17.5
	L(.3) = 3.4 mh,	DQ = 4.2
	L(.5) = 1.05 mh	DQ = 1.18

The flux density during the previous tests was as follows:

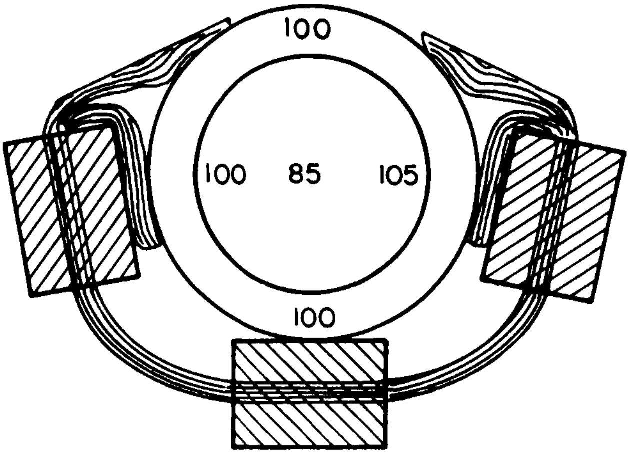
(a) Untrimmed pole ends.



(b) Trimmed pole ends.



(c) Padded pole ends.



The gaussmeter proved to be an invaluable tool for checking the flux distribution and its changes with Deltamax additions to various positions in the core. Figure (c) shows the most uniform flux pattern but not the most saturated core in anticipation of the case where a controlled (square wave) current driver would be available. The Deltamax core was the same as in (c) above but only 2 of the 3 coils were energized. The center coil was disconnected. The flux density dropped about 15 per cent (at .5 amp) and the inductance is as follows:

L(0) = 4.75 mh, DQ = 8.8

L(.3) = 3.45 mh, DQ = 6.7

L(.5) = 1.42 mh, DQ = 2.4

L(.6) = .82 mh, DQ = 1.3

The magnet did not saturate fully until .6 amps.

Magnet assemblies through D-7 had the same type bobbin (Cosmo B-1454) with a 1/16 X 1/8 in. core space and had no more than 115 gauss average could be obtained for a saturating core. For higher flux densities a larger bobbin would be required.

Assembly D-8, with a 1/8 X 1/8 core area, was tested using Deltamax strips inside of four-200 turn bobbins (Cosmo B-1530). The flux density increased but so did the inductance as follows:

L(0) = 27.5 mh, Q = 22

L(.5) = 3.3 mh, DQ = 2.6;

average flux density increased from 115 gauss to 150 gauss. Resistance increased from a 4.5 to 7.9 ohms. The very large L(0) inductance and lack of thorough saturation for L(.5) made this size of core and coil impractical to drive from the available magnet drivers. No further tests were performed with the large coil bobbin.

Magnet assemblies using the 3 adjacent coil configurations appear to be consistent and practical for saturating magnets with the following characteristics:

(1) 100 gauss air gap flux density

(2) approximately 1 watt magnet dissipation (.5 thru 4.5 ohms)

(3) 5 mm to 15 mm lumen size.

The following materials are required for the construction of a 12 mm probe:

PARTS LIST

Core material - 3 in. of .004 X .250 in. taken from core type A-2 100

68 in. of .004 X .125 in. taken from core type 3 T-5515-D4-AA

Obtained from Arnold Eng. Co.;

3 bobbins

Cosmo Plastics Co., B-1454;

#32 heavy Teflon coated wire

Thermal Wire of America type HT;

Masking tape

3M Co., #202;

Silicone tubing .062 in. ID .125 in. OD

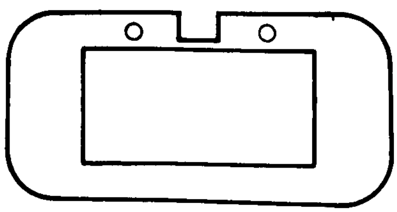
Ronthor Reiss Corp., Silatube Grade S-2000;

Braid from alpha #1200 for shielding cables

Alpha wire type B-100° MIL W 16878D

The procedure is as follows:

Drill #60 holes in each bobbin as shown below:



Wind bobbins: Layer wound HT heavy Teflon coated #32 wire

2 bobbins 200 turns

1 (center) bobbin 150 turns.

Secure end of winding with masking tape;

Clean core ultrasonically in carbon tetrachloride.

Cut core material

1	piece	7-1/2 in.	(7-1/2)	Deltamax	.004 X	.125
13	pieces	3-1/2 in.	(45-1/2)	Deltamax	"	"
20	pieces	3/4 in.	(15)	Deltamax	"	"
			(68)			
2	pieces	1-1/2 in.		Deltamax	.004 X	.250

Insert core with long strip outermost
placing bobbins as shown in Fig. E-2 and adding 10 small strips to each side to increase cross section area of pole pieces.

Wrap core with .250 X 1.5 in. pieces between bobbins.

Form and trim pole pieces. See Fig. E-3

Connect bobbins, noticing that two are placed and connected similarly and one is reversed both mechanically and electrically.

The bobbins are wound with 30 heavy (Double) Teflon wire on a nylon bobbin. Since the Teflon magnet wire (TFE) is not pin-hole-free, the assembly must be adequately embedded in epoxy. Careful layer winding is necessary to avoid shorted turns in a material as soft as Teflon. The heavy Teflon wire gave maximum turns in the bobbin but (most im-

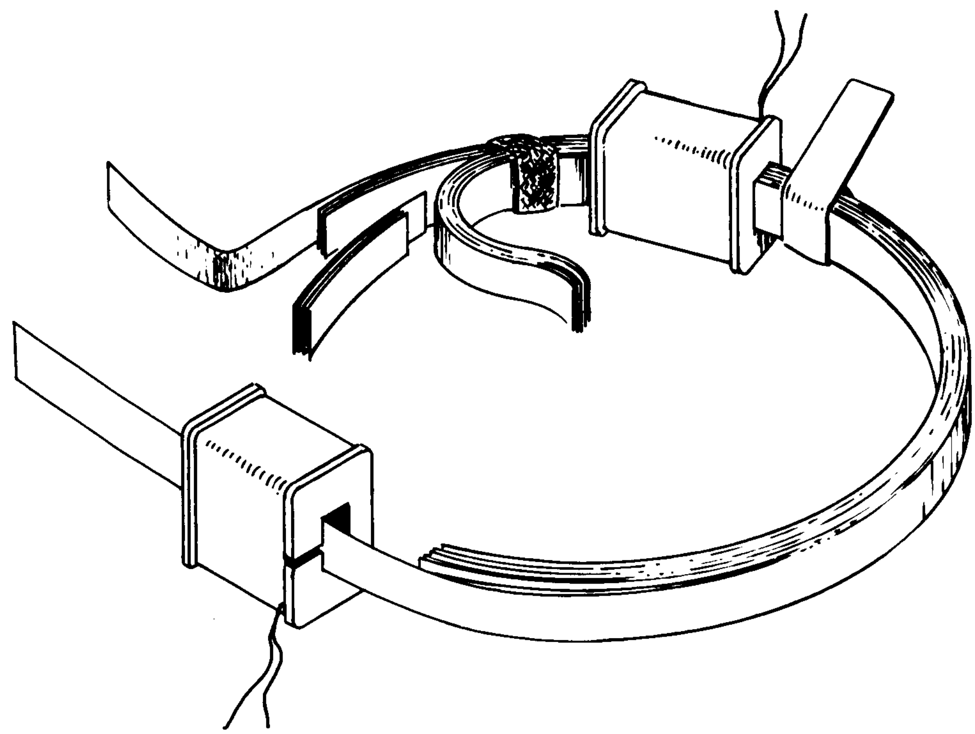


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FIG. E2 PRELIMINARY MAGNET ASSEMBLY DETAILS

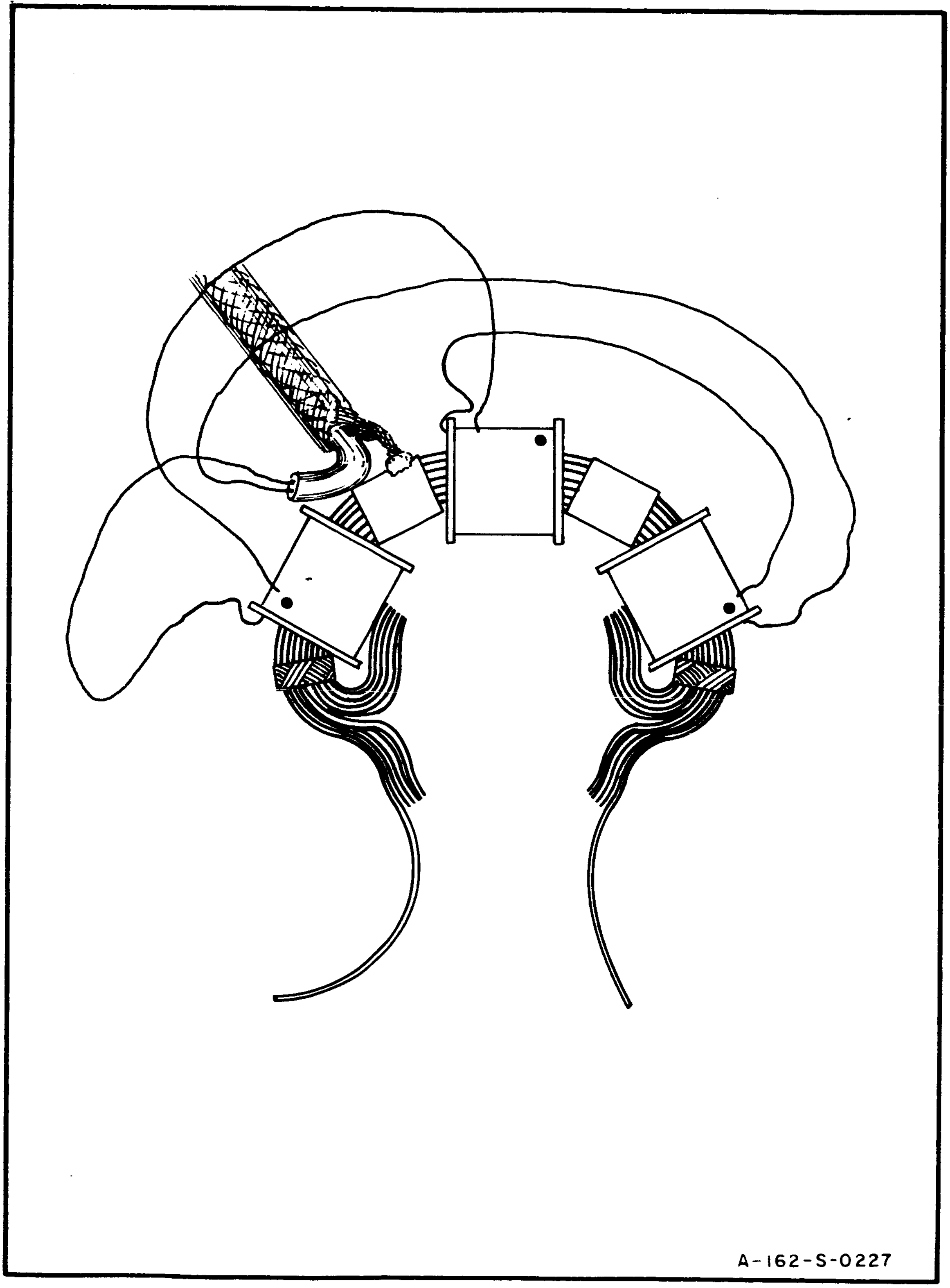


FIG. E3 MAGNET ASSEMBLY DETAILS

portant,) retained its insulating qualities despite the very high internal temperatures generated in the small bobbin.

A red dot was used to show the end of each bobbin where the winding starts. This permits proper assembly of the coils on the magnet core.

The original probes employed a Teflon coated (TFE) multi-conductor cable purchased intact. These cables contained pin-holes and were not sufficiently flexible. Moreover, the shield was not of sufficiently close weave and did not provide adequate shielding. Since non-toxic cables having satisfactory mechanical and electrical properties were not then available, a program of cable construction was undertaken.

Two types of shielded cable are necessary: signal cable consisting of three #32 stranded wires in a double (silicone) rubber jacket and magnet excitation cable constructed similarly but employing two #28 stranded wires. The larger size wire is necessary because of the high magnet current.

Silicone rubber is an excellent material for wire jacket construction for two reasons: (1) Dow Corning adhesive RTV 731 adheres to it very well, and this adhesive makes a good mechanical bond to the epoxy embedment of the probe, (2) Silicone rubber undergoes a remarkable expansion upon being soaked in toluene, and this greatly facilitates the process of drawing the tubing over the completed cable assemblies to form a jacket. This rubber returns to its original flexible condition upon evaporation of the toluene.

Two alternatives to silicone rubber tubing were investigated. These were polyurethane and Teflon. Polyurethane did not bond well either to epoxy directly or RTV adhesive. Moreover, liquid expanders left the polyurethane very brittle and weak. Teflon tubing was unsatisfactory for the following reason: it must be etched, of course, before any appreciable adhesion will take place, but the etched surface does not adhere very well to the parent or unetched material. The etched joints were found to be highly unreliable.

The signal cable is constructed as follows:

1. Cut 3 wires 24 in. long from Teflon (FEP, pin-hole free) wire 7 stranded #32 (W. L. Gore, Newark, Del.).

2. Completely immerse each wire in Teflon etch bottle (Chemplast Inc., Newark, N.J.). This permits color code paints to stick.

3. Gently twist the 3 wires to form a cable.

4. Solder a "fish" wire to one end of the 3 wire cable. This permits pulling sleeving, shielding, etc., over the cable while one end is fast to a bench vise.

5. Expand the .023 in. ID X .015 wall silicone rubber tube (Ronthor Reiss Corp.,) in toluene for about 15 minutes. "Fish" the expanded tube over the 3 wire cable. Allow to dry.

6. Remove the shield from #1200 wire (Alpha Wire Co.,) and fish the shield over the silicone tube of Step 5. The silicone tube is necessary to prevent short-circuits between shield and signal wires. Work the shield down tightly.

7. Expand the outer silicone tube, .125 X .030 wall, in toluene and fish it over the shield.

8. To obtain additional strain relief where the cable is secured rigidly at both ends, add 2 in. long pieces of .125 OD silicone tubing, over the outer tube in Step 7, near each end of the cable.

The magnet current cable is constructed in a similar manner as follows:

1. Cut 2 wires #28 stranded vinyl covered wire type B-100° Alpha 1851 MIL W-16878D and twist.
2. Pull shield from Alpha #1200 wire directly over the twisted pair.
3. Pull outer silicone tube .125 OD over shield.
4. Add 2 in. pieces of tubing for strain relief.
5. Fish the twisted pair through the sidewall of the shield to form a pigtail at the probe end.

Preassembling the platinum electrodes in an epoxy tube enables precise alignment of the electrodes and permits a check of final probe assembly before cementing magnet in place. The procedure is as follows:

An unfilled epoxy rod (Hypol Corp., #CPI-4264) is machined to provide magnet grooves, electrode wire grooves and lumen of desired diameter. The tube length should be at least three (3) times the lumen diameter so that there will be sufficient liquid level during the alignment of the magnet on the tube. (With too short a tube length the currents inside the tube are affected by variation in liquid level which in turn affect the magnet position for minimum induced spike voltage.)

The electrodes were made from 1/16 platinum wire because it was available but the wire drawing operation could be saved if .016 diam. is purchased directly. Melt .040 in. diam. balls on the end of .016 in platinum wire and cut to 3/8 in. stem lengths (See Fig. E4a). Flatten the ball end to the double spherical shape with the cold heading die made as follows: Hammer a 3 in. finishing nail over polished steel balls until a recess forms in the nail head. Die #1 (Fig. E4b) uses a 1/32 diam. ball, one-half depth. Die #2 (Fig. E4c) uses a 1/16 diam. ball and Die #3 (Fig. E4d) uses a 3/32 diam. ball. The cold heading operation is performed with the wire inserted in a close-fitting hole.

The finished platinum electrode is inserted into small holes in the tube and bedded down in epoxy cement (Hysol 1-C).

The signal cable is attached to an insulated (Bakelite) rod to avoid lead breakage during probe assembly. The rod is cemented into a pre-drilled hole at a position which permits the cable to lie between coil bobbins when assembled as shown in Fig. E5a.

The magnet core is obtained from commercial Deltamax toroidal cores (Arnold Eng. Co., core #3T-5515-D4) opened up and ultrasonically washed in carbon tetrachloride. The 1/8 in. wide spiral core is cut to 3-1/2 in. lengths with a scissors. Thirteen (13) strips are stacked up and inserted into the 3 magnet bobbins, one at a time.

The winding "start" wire is marked on the lead wire and bobbin itself. This permits two bobbins to be polarized the same way while the third bobbin is polarized oppositely, see Fig. E3. The magnet lead-in wires are now symmetrically displaced about the lumen so that the capacitively coupled spike voltages will tend to neutralize one another.

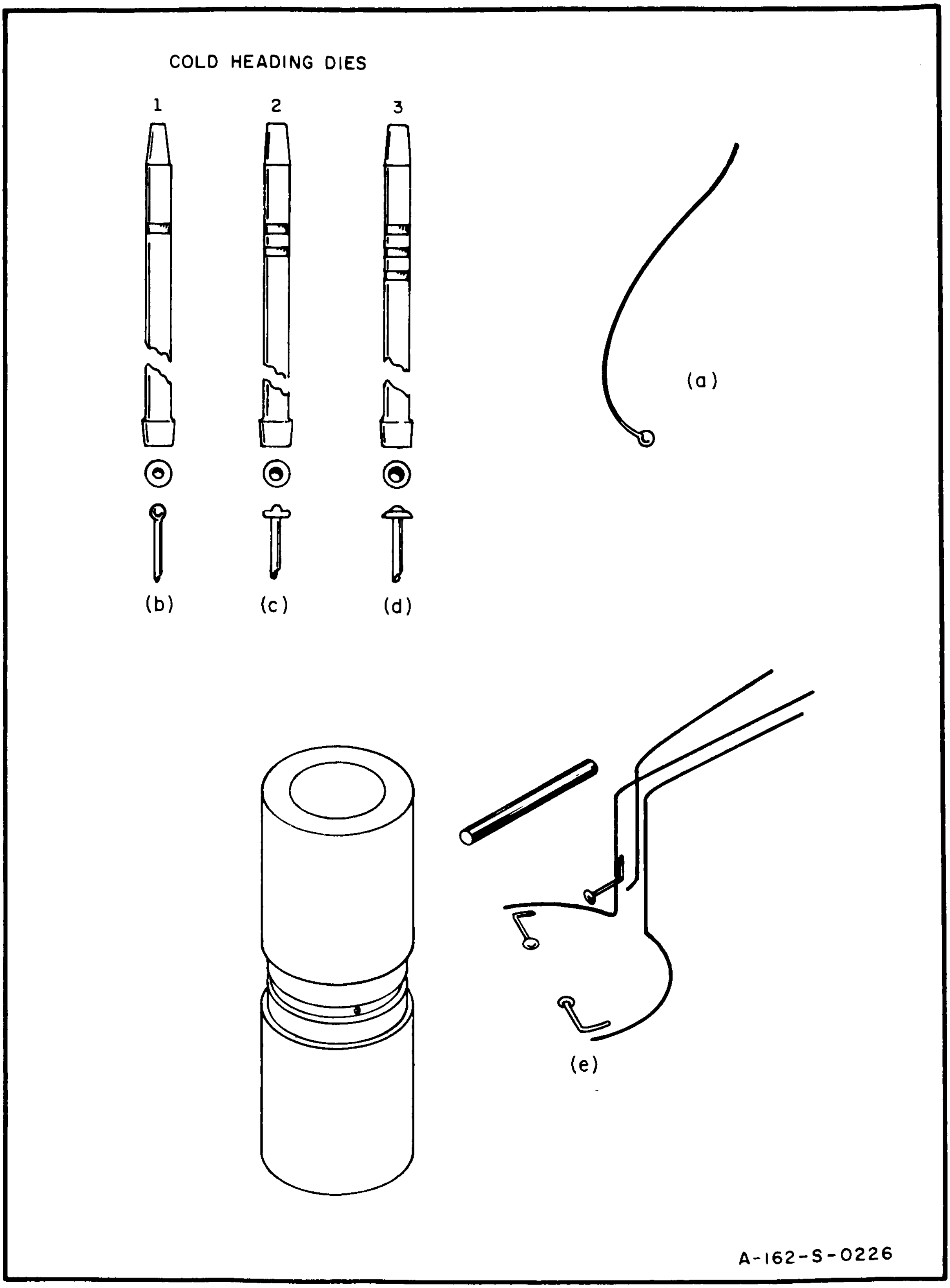


FIG. E4 ELECTRODE ASSEMBLY

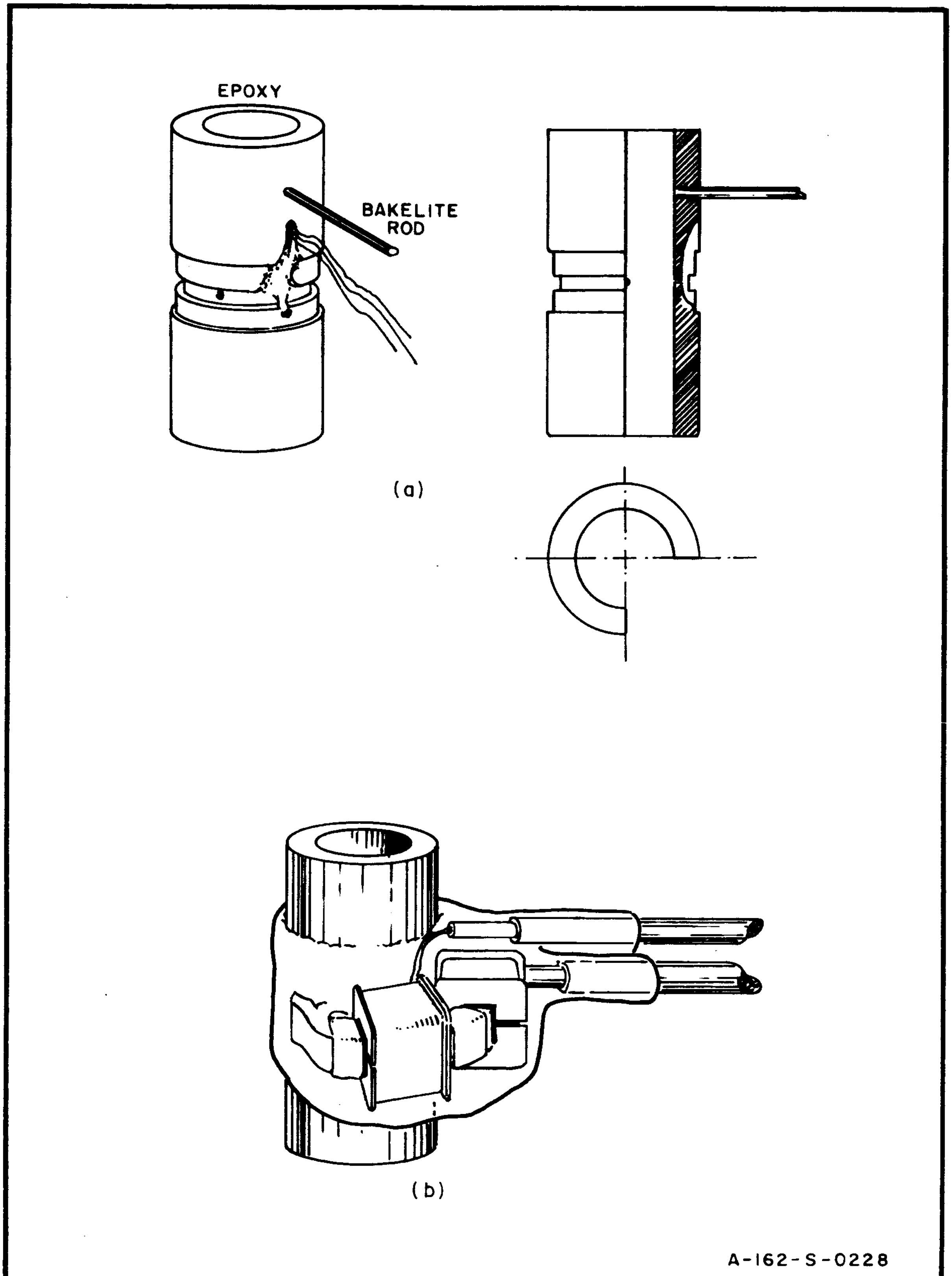


FIG. E5 FINAL PROBE ASSEMBLY DETAILS

Four turns of Deltamax from a 1/4 in. wide tape (Arnold Eng. Co.,#3T-5502-D4) are wrapped between coils 1 and 2, also between 2 and 3.

As explained earlier, this additional core area ensures maximum core permeability where non-saturation is desired.

Six (6) layers of Deltamax (1/8" wide) are inserted into each pole near the outer layers and laced down tightly. This also increases the permeability in the pole face area.

The "rough" assembly may now be wired together and checked for; (a) inductance at zero dc current; (b) inductance at 0.5 amp dc; (c) magnetic field pattern around the magnet. To check the field pattern, place a glass plate (Petrie Dish) over the magnet and sprinkle iron (cast iron) filings while gently tapping the plate. Mistakes in coil phasing are easily discerned by examining the field pattern.

The rod end may now be trimmed.

The electrode assembly must have the platinum electrode cleaned in HCl and platinized before being attached to the magnet. The lower end of the tube should be plugged with a shallow plastic disc so that liquids will be retained for the final operations.

Pour platinizing solution into the tube and connect the electrodes (both signal leads in parallel) to the terminals of the platinizing kit. (Industrial Instruments, Cedar Grove, N. J., #PK-1a, Platinizing solution # PL-1.) The circuit contains a 4.5 volt battery source, a reversing switch and a meter. There is nothing critical about the current, but for the electrode size described, 25 ma is sufficient. Reverse the current whenever gas bubbles start to form on the electrodes (every few seconds). In 15 seconds a black coating will cover the platinum surface. If the coating is spotty, clean the surface again with an abrasive, wash and replatinize. Wash the electrode assembly thoroughly in clean water and fill with saline immediately. If the electrodes are left to dry in air for any length of time, noise voltages may be very evident and replatinizing may be necessary.

With the magnet assembly held in the electrode assembly grooves, Figs. E5 and E6 square wave excitation current should be applied. A saline solution is used to fill the tube. This simulates blood sufficiently well for calibration purposes.

An oscilloscope, connected to the output of a pre-amplifier, should be used to observe the electrode signals when no flow signal is present.

By adjusting the position of the magnet axis relative to the tube axis, the spike voltage can be minimized. For a good probe, the spike voltage can be made equal to or smaller than the maximum average flow signal (about 5-15 microvolts p-p). A 12.0 mm lumen probe has a 3 liter per minute average "full scale flow."

When the proper orientation of the magnet with respect to the electrode tube is obtained the spikes will have minimum amplitude and there will be a space between the outer electrode and one pole piece for the slot that enables the insertion of a blood vessel. The proper orientation is shown in Fig. E6. Epoxy cement is added in several places to tack the assembly together. If the spike voltage has increased appreciably due to distortion or slippage of parts during epoxy curing time a trimming operation can be performed. Small pieces of Deltamax, 1/16 X 1/8 in. can be laid adjacent to the pole (on the outside of the tube). These act to change

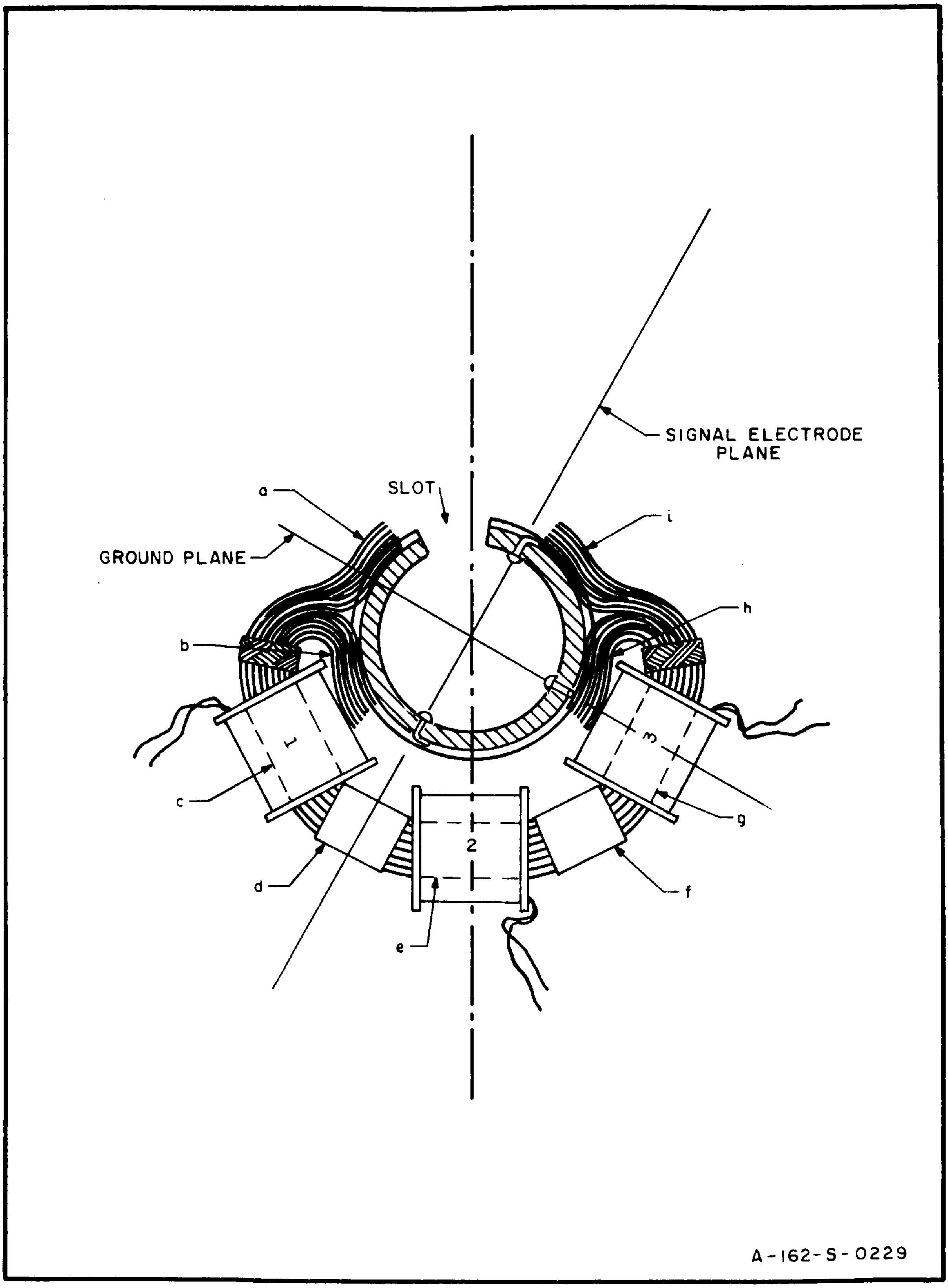
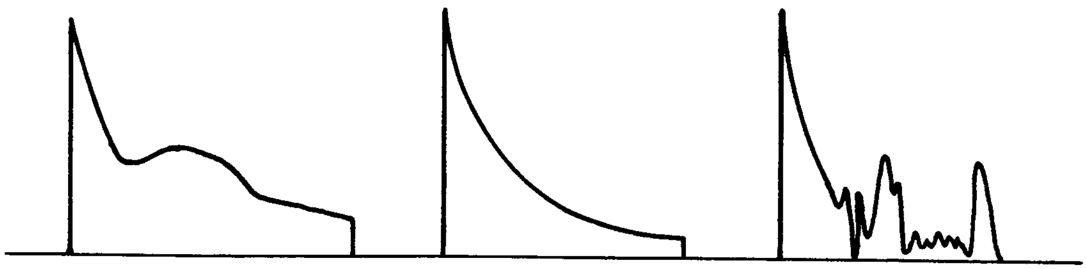


FIG. E6 ELECTRODE AND PROBE ORIENTATION DRAWING the axis of the magnetic flux. The most effective place for the trimming pieces is on the side near the ground electrode. Additional epoxy cement is then added to hold the trimming pieces in place. Several days of checking, trimming and baking in an oven may be required to stabilize the assembly so that the spike voltage remains tolerable.

The platinizing process described above produces surfaces which exhibit the least amount of electrical noise of all those tested to date. But the electrodes so treated must be stored in saline. A platinized surface stored in air usually becomes useless, producing output waveforms like those shown below.



Artifacts and noise obtained from a defective electrode.

A finished probe may be calibrated by passing a saline solution through it at the maximum flow rate for which the probe is designed. (See the table on p. 92.) Having set the first thumbwheel on the Flowmeter front panel, to the position corresponding to this rate the indicated flow rate may be set to within 0.1 per cent of this value by means of the three remaining thumbwheels. (These are part of an attenuator described on p. 80.) The number corresponding to the final settings of the wheels should then be stamped on the probe body. Under continuous maximum rated flow conditions the voltage at the INSTANTANEOUS and AVERAGE flow output jacks will be -1.000 and +10.00 VDC, respectively.