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# TECHNICAL ADVISEMENT MEMORANDUM NO. 171-1

# A SURVEY OF SPACEBORNE COMPUTERS

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# TECHNICAL ADVISEMENT MEMORANDUM NO. 171-1

# A SURVEY OF SPACEBORNE COMPUTERS

## 1. Introduction

The purpose of this memorandum is to present the results of a preliminary survey of a set of digital computers generally applicable to the Airborne Evaluation Equipment problem. No attempt was made to draw any conclusions from the data or to select one or more machines over the others. The primary use to be made of these data is the conceptual design of alternate AEE hardware systems.

The machines were characterized by numerous parameters, including:

1. Main memory characteristics
2. Scratch pad memory characteristics
3. Arithmetic unit characteristics
4. Addressing structure
5. Input/output organization
6. Interrupt system
7. Physical characteristics
8. Operating and environmental characteristics

In addition to the fairly standard parameters listed above, others have been introduced that should make the selection more meaningful in terms of the computer's impact on the overall system or should make comparisons between machines more objective. The added parameters are as follows:

1. Availability of acceptable peripheral devices
2. Compatibility with ground-based computer
3. Maturity and availability of hardware
4. Performance measure

It should be understood that this discussion in no way limits the consideration of alternate test system philosophies. The test system may be mechanized with a single centralized computer or with a number of machines distributed among the various vehicle stages. Furthermore, the fact that this document discusses only general-purpose machines should not be taken to imply that special-purpose mechanizations would not be acceptable.

This initial look at the Airborne/Spaceborne computer market indicated that there was a wide variety and large number of candidate machines available. This evaluation has been restricted to those computers that weigh 100 pounds or less and utilize 300 watts or less due to the restraints of the space environment. However, even these numbers are considered to be in excess of what are felt to be reasonable design goals, and were chosen so as to prevent us from ignoring highly desirable machines with marginal physical characteristics.

## 2. Evaluation Parameters

Before presenting the data on the machines, it would be well to discuss some of the evaluation parameters, so as to provide the reader with a better understanding of their meaning. In addition, a short discussion of input/output organization will clarify some of the nomenclature used on the data sheets.

### a. Performance Measure

In order to determine whether or not a given machine can perform a specified function or to compare one machine with another, it is necessary to have an unbiased measure of machine performance. Performance is generally considered to be a function of the speed with which a machine can perform a given task and, as such, is greatly dependent on the task selected.

To eliminate problems involved in task selection and to make an evaluation of machine speed more meaningful than a simple comparison of add times and multiply times, it was decided to evaluate machine performance based on the relative frequency of instruction use for typical checkout problems.

For this purpose, the Eason-Lane mix, developed at the Douglas Aircraft Company, is used. This mix is a variation of the standard Gibson mix and is oriented toward automatic checkout problems. This mix is shown at the top of the following page.

| | Operation | Relative Frequency |
|---|---|---|
| (1) | Load, Add, Subtract (indexed) | 0.45 |
| (2) | Store (indirect) | 0.11 |
| (3) | Multiply | 0.02 |
| (4) | Divide | 0.01 |
| (5) | Branch | 0.12 |
| (6) | Logical | 0.19 |
| (7) | Shift (6 bits) | 0.10 |

The "rated speed" of any machine, with respect to the problems of automatic checkout, is determined using the several operation times weighted by their relative frequencies.

b. Compatibility

A significant requirement in the selection of any spaceborne computer is the availability of a ground-based machine with a compatible instruction set to be used for support purposes. Manufacturers will normally indicate one or more machines that are directly compatible, having either the same instruction repertoire or a subset that will satisfy the requirement. Alternatively, manufacturers may choose to provide software for such machines as the IBM 7094 or CDC 3600 to functionally simulate the spaceborne computer. The completeness of each simulation package must be considered carefully to ensure that the simulation software will operate under control of existing support computer executive and monitor systems, and that the necessary programming debugging aids are provided. These compatibility factors are noted.

c. Input/Output Organization

A number of classifying I/O features are included for each machine profile. Most spaceborne machine I/O organizations are tailored to specific applications. It is not uncommon, therefore, to find machines in this class with multistructured I/O centers for processing serial, discrete, or parallel digital data. The I/O interface may even provide for the exchange of analog signals. Most manufacturers will offer a machine interface custom-designed to the user's application.

An attempt has been made in this study to ignore these "special I/O fixtures" and to examine the I/O design in terms of basic data path organization and word length. Most of the I/O data word lengths correspond to the C.P.U. word length; however, some machines provide for half-word and character communication modes. Only one manufacturer in this survey included parity in the I/O data channel as a standard feature; however, most offer it as an optional feature. The I/O control organization is delineated in each machine profile by including the definition of I/O data path and location of I/O control word(s). To reduce hardware, some machines will utilize the arithmetic unit (i.e., accumulator or instruction register) to perform I/O control, while other, more elaborate machines will provide special registers to hold the current storage address and block length count information. Another useful I/O feature is the ability to access memory by specifying the data address from an external source (e.g., ESA and ESI as used in UNIVAC machines). This feature provides for very efficient data exchange in certain applications. The maximum data block length that can be directly accessed with one set of I/O control words may vary from a single word to the entire memory.

A flexible approach for controlling a continuous series of data transmissions involves the concept of data chaining. Data chaining provides for accessing a number of contiguous or noncontiguous memory buffer regions without program intervention. The ability to chain data, and the extent thereof, is indicated in each profile.

In the survey, consideration is given to the number of available interrupt levels and the organization of the interrupt system. No attempt is made to define the individual machine interrupt reaction times or overheads. However, such characteristics as hardware "nesting" of interrupts, the ability to "lock out" interrupts programmably, and the ability to perform dynamic priority reallocation have been indicated in each machine profile.

## 3. Computer Data Sheets

The following pages contain data sheets for all computers evaluated to date and a summary chart of all major characteristics. The computer survey is not yet complete as there are a few machines on which manufacturer's data have not yet been received.

Computer: IBM-4π (EP)

a) MAIN MEMORY:

word length: 32 Bits + 4 parity
cycle time: 2.5 μ sec.
capacity: 165 K words
parity check: yes
protection: software memory protect
type: core

b) SCRATCH PAD MEMORY:

| | |
|---|---|
| word length: | none |
| cycle time: | none |
| capacity: | none |
| parity: | none |
| type: | none |

c) ARITHMETIC FEATURES:

data representation: binary, 2s comp.
serial/parallel: parallel
no. of registers(G.P.): 16 hardware
number of inst: 129 (78 basic)
instruction word: 32 bits
op. code field: 8 bits
address field: 24 bits

| | Inter-register |
|---|---|
| add time: 5.04 μ sec. | 1.66 μ sec. |
| multiply time: 10.08 μ sec. | 8.75 μ sec. |

d) ADDRESSING:

index registers: 16 G.P. hardware
indirect: no
effective address: All memory can be directly addressed relative to base registers
access to general loc: direct, indexed, branch and link

e) INPUT/OUTPUT:

channels: 3 including mux, selector, and direct
data length: 8 bit
parity: memory-channel buffer
basic I/0 data path: NA
word rate: mux. mode: 33K bytes/sec.; burst mode: 160K bytes/sec.
I/0 control word loc.: I/0 channel hardware
max. block length: 64,000 bytes
chaining: automatic chain of variable field lengths

interrupt levels: 16
nesting: yes
dynamic priority assignment: yes

f) PHYSICAL CHARACTERISTICS:

| | 8K MEM | 16K MEM | 32K MEM |
|---|---|---|---|
| weight: | 52 lbs | 63 lbs | 85 lbs |
| volume: | .84 cu. ft. | 1.09 cu. ft. | 1.60 cu. ft |
| power: | 300 watts | 380 watts | 540 watts |

implementation: I.C. (T.T.L)

g) OPERATING CHARACTERISTICS:

MTBF: 5000 hrs (for lab. environment)
temp: )
vibration: ) MIL-E-5400

h) PERIPHERAL DEVICES:

bulk storage: Drum*
CRT: -
typewriter: -
others: Mag. tape unit

i) COMPATIBILITY:

Directly compatible upward on all IBM 360 models (from model 40)

j) EQUIPMENT MATURITY:

flight proven hardware
availability: early 1967

k) OTHER FEATURES:

1) micro program - is alterable

L) SOFTWARE:

Assembler
Service routines
Compiler

*DRUM SPECS.

Storage: $10^6$ bits
Speed: 12000 RPM
Wt: 2.5 lbs.
Volume: 40 cu. in.
Power: 20 watts

Computer: IBM - 4π (CP)

a) MAIN MEMORY:

word length: 16 bits (32 bit optional)
cycle time: 2.5 μ sec.
capacity: 32K words
parity check: yes
protection: software memory protect
type: core

b) SCRATCH PAD MEMORY:

word length: none
cycle time: none
capacity: none
parity: none
type: none

c) ARITHMETIC FEATURES:

data representation: binary, 2s comp.
serial/parallel: parallel
no. of registers (G.P): up to 8

| | 360 set | 1800 set |
|---|---|---|
| no. of inst: 129 | (51 basic) | 31 |
| instruction word: | 32 bits | 32 bits |
| op. code field: | 8 bits | 5 bits |
| address field: | 16 bits | 16 bits |
| add time: | 8.50 μ sec. | 5 μ sec. |
| multiply time: | 41.5 μ sec. | 12 μ sec. |

d) ADDRESSING:

index registers: 8 located in memory
indirect: no
effective address: All memory can be addressed relative to base registers
access to general loc.: direct, indexed, branch and link

e) INPUT/OUTPUT:

channels: 2 including mux and direct
data length: 8 bit
parity: yes
basic I/O data path: memory-channel buffer
word rate: mux mode: 33K bytes/sec; burst mode 160 K bytes/sec
I/O control word loc: I/O channel hardware
max. block length: 64000 bytes
chaining: yes - variable field lengths

interrupt levels: 8
nesting: yes
dynamic priority assignment: yes

f) PHYSICAL CHARACTERISTICS:

8K mem
weight: 37 lbs.
volume: .8 cu. ft.
power: 250 watts
implementation: IC. (TTL)

g) OPERATING CHARACTERISTICS:

MTBF: 3000 hrs.
temp.: } MIL-E-5400
vibration: }

h) PERIPHERAL (SPACEBORNE) DEVICES:

bulk storage: Drum*
CRT: - NA
typewriter: - NA
others: Mag. tape

i) COMPATIBILITY:

1800 set option: Directly compatible IBM 1800 simulator available for 7090-94
360 set option: Directly compatible upward IBM 360-40

j) EQUIPMENT MATURITY:

flight proven hardware
available early 1967

k) OTHER FEATURES:

1. Optional instruction set.

L) SOFTWARE:

Assemblers
Service Programs
Compilers
Simulator (for 1800 opt.)

* DRUM: $16^6$ bits capacity
12000 RPM
2.5 lbs.
40 cu. in.
20 watts

Computer: AUTONETICS-D26C

a) MAIN MEMORY:

word length: 30 Bits
cycle time: 6 μ Sec.
capacity: 8-32 K Words
parity check: None
protection: Power Protection
type: Core

b) SCRATCH PAD MEMORY:

word length: 30 Bits
cycle time: 1 μSec.
capacity: 256 Words
parity: None
type: Core

c) ARITHMETIC FEATURES:

data representation: Binary, 2C
serial/parallel: Parallel
number of registers (G.P): - NA
number of inst: 87
instruction word: 30 Bits
op. code field: 7 Bits
address field: 14 Bits
add time:* 6-12 μ Sec.
multiply time: 33-45 μSec.

d) ADDRESSING:

index registers: 1 Hardware, 6 MEM (scratch pad)
indirect: No
effective address: Direct
access to general loc.: Direct, Index, Return Jump

e) INPUT/OUTPUT:

channels: ** One input, one output
data length: Character of word
parity: No
basic I/0 data path: MEM - I/0 Channel
word rate: 13,800 words/sec or 33,000 CHAR/Sec.
I/0 control word loc: Scratch pad memory
max. block length: 32K
chaining: No

interrupt levels: 8
nesting: no
dynamic priority assignment: No, Programmed ENABLE/DISABLE

f) PHYSICAL CHARACTERISTICS:

| | 8 K Memory | 32K Memory |
|---|---|---|
| weight: | 47 lbs. | 68 lbs |
| volume: | .65 cu. ft. | .85 cu. ft. |
| power: | 175 watts | 220 watts |

implementation: I.C.

g) OPERATING CHARACTERISTICS:

MTBF: 15,600 hrs.
temp.: -40 °C to + 65 °C
vibration: 20g RMS at 10 - 20 KCPS

h) PERIPHERAL DEVICES:

bulk storage: Disk available
CRT: - NA
typewriter: - NA
others: - NA

i) COMPATIBILITY

A simulator program for the IBM 7094 permits use of this machine to check-out D-26C Prog.

j) EQUIPMENT MATURITY

Flight tested in North American T-39 airplane

k) OTHER FEATURES:

1) Real time clock
2) ESA
3) Three special purpose I/0 processo

L) SOFTWARE:

1) Simulator (IBM 7094)
2) Assembler (IBM 7094 fap)
3) Compiler
4) Utility

* Add time dependent on location of oper and in main and scratch pad memory

** Three separate I/0 processors provide for parallel, analog, or discrete data exchange

Computer: AUTONETIC D26J

a) MAIN MEMORY:

word length: 12 or 16 Bit (Optional)
cycle time: 6 $\mu$ Sec.
capacity: 1K - 16K words
parity check: none
protection: Transient
type: Core

b) SCRATCH PAD MEMORY:

word length: none
cycle time: none
capacity: none
parity: none
type: none

c) ARITHMETIC FEATURES:

data representation: Binary, 2's complement
serial/parallel: Parallel
number of registers (G. P.): 1
number of inst: 27
instruction word: 12 or 16 Bit (Optional)
op. code field: 5 Bits
address field: 7 or 9 Bits (Option.)
add time: 12 $\mu$ Sec.
multiply time: 42 $\mu$ Sec at 12 Bits
54 $\mu$ Sec at 16 Bits

d) ADDRESSING:

index registers: None
indirect: None
effective address: relative to bank register address
access to general loc.: direct, return jump.

e) INPUT/OUTPUT:

channels: * single bilateral
data length: 12 or 16 Bit (optional)
parity: none
basic I/O data path: Memory-arithmetic unit - I/O channel
word rate: 13,800 words/sec. max serial processor, 138,000 word/sec parallel - processor (optional mechanization)

I/O control word loc.: instruction register
max. block length: 1 word
chaining: none

interrupt levels: One, designed into I/O hardware
nesting: none
dynamic priority assignment: none

f) PHYSICAL CHARACTERISTICS: (includes P.S. and MEM)

weight: 20 lbs
volume: .21 cu. ft.
power: 62 watts
implementation: Integrated CKT (DTL)

g) OPERATING CHARACTERISTICS:

MTBF: 18,000 hrs.
temp.: -40 °C. to + 65° C.
vibration: 20g RMS 10-2000 CPS.

h) PERIPHERAL DEVICES:

bulk storage: Disk storage (1096-12K words) 5MS avg. access time
CRT: NA
typewriter: - NA
others: - NA

i) COMPATIBILITY:

Software simulation pkg. available to enable checkout of programs on the IBM 7094 or CDC 3600.

j) EQUIPMENT MATURITY:

Flight tested at Holloman AFB on F106 and C130.

k) OTHER FEATURES:

NA

L) SOFTWARE:

simulator package

* I/O is tailored to need; the basic unit contains A-D, D-A and other signal conditioning hardware to provide exchange of discrete and analog data

Computer: NORTHROP NDC-1051

a) MAIN MEMORY:

word length: 24 Bits
cycle time: 2 $\mu$ Sec.
capacity: 2-8K words
parity check: No
protection: Yes - power transient
type: Core

b) SCRATCH PAD MEMORY:

word length: none
cycle time: none
capacity: none
parity: none
type: none

c) ARITHMETIC FEATURES:

data representation: Binary 2's comp.
serial/parallel: Parallel
number of registers (G. P.): 1
number of inst: 39
instruction word: 24 Bits
op. code field: 6 Bits
address field: 12 Bits
add time: 8 $\mu$ sec.
multiply time: 72 $\mu$ Sec.

d) ADDRESSING:

index registers: 7 located in memory
indirect: yes
effective address: Direct to 4K words indexed
access to general loc: extend to additional 4K by bank select command; all addressing relative to roll arrow; return jump.

e) INPUT/OUTPUT:

Channels: One buffered I/0 controlled ext. or by program
data length: 24 bits
parity: None - can be added opt.
basic I/0 data path: memory-arith unit - I /0 channel
word rate: 250 K words max.
I/0 control word loc. : accumulator
max. block length: one word
chaining: none

Interrupt levels: none with basic machine, can be added optionally
Nesting: none
Dynamic priority assignment: none

f) PHYSICAL CHARACTERISTICS: (8K memory)

weight: 28.6 lbs.
volume: .5 cu. ft.
power: 140 watts
implementation: integrated CKT.

g) OPERATING CHARACTERISTICS

MTBF: 8500 hrs.
temp.: ) MIL-E-5400G
vibration: )

h) PERIPHERAL DEVICES:

bulk storage: Disk memory ($7.5 \times 10^8$ Bits)
CRT: - NA
typewriter: - NA
others: - NA

i) COMPATIBILITY:

Not compatible with any machine, no simulater written

j) EQUIPMENT MATURITY:

Two prototypes developed - to be tested on inertial platform in-house

k) OTHER FEATURES:

--

L) SOFTWARE

--

Computer: HONEYWELL - ALERT

a) MAIN MEMORY:

word length: 24 Bits
cycle time: 1 $\mu$ Sec. Read, 4 $\mu$ Sec. Write
capacity: 4-32K words
parity check: none
protection: power failureprotect
type: Micro Biax or Core D. R. O.

b) SCRATCH PAD MEMORY:

word length: none
cycle time: none
capacity: none
parity: none
type: none

c) ARITHMETIC FEATURES:

data representation: Binary
serial/parallel: Parallel
number of registers (G. P.): 1
number of inst: 64
instruction word: 24 bits
op. code field: 6 Bits
address field: 15 Bits
add time: 2.0 $\mu$ sec.
multiply time: 12.0 $\mu$ Sec.

d) ADDRESSING:

index registers: Six hardware
indirect: yes, multi-level
effective address: Direct to 32K words
access to general loc.: Direct, indirect, indexed

e) INPUT/OUTPUT:

Channels: One direct channel, up to three buffered channels
Data Length: 6 or 24 Bits-Buffered channel, discretes - direct channel
Parity: none
Basic I/O data path: memory- I/O buffer register
Word rate: Buffered: 166K words/sec.; Direct: 70 K words/sec.
I/O control word loc.: Buffered: I/O channel register
max: block length: 512 words
chaining: No. - but can automatically repeat block

Interrupt levels: 8 external, expandable to 24 levels
Nesting: Yes.
Dynamic priority assignment: yes

f) PHYSICAL CHARACTERISTICS:

| | (8K MEM) | (16K MEM) |
|---|---|---|
| weight: | 60 lbs | 86 lbs. |
| volume: | 1.21 cu. ft. | 1.57 cu. ft. |
| power: | 194 watts | 274 watts |
| implementation: | integrated CKTS-TTL. | |

g) OPERATING CHARACTERISTICS:

MTBF: 10,000 hrs.
temp.: -53 °C. to + 85 °C.
vibration: ± 10g at 70-500 CPS.

h) PERIPHERAL DEVICES:

bulk storage: Tape unit
CRT: - NA
typewriter: - NA
others: - NA

i) COMPATIBILITY:

Honeywell 800

j) EQUIPMENT MATURITY:

Qualification testing

k) OTHER FEATURES:

1. Character or word addressing
2. Self test fixtures

L) SOFTWARE

H-800 simulator
Assembly Prog (SHAP-8)

Computer: CONTROL DATA - 5400-8

a) MAIN MEMORY:

word length: 24 bits
cycle time: 3.0 μ sec.
capacity: 32,256 words
parity check: no
protection: Yes - power transient
type: core

b) SCRATCH PAD MEMORY:

word length: 24 bits
cycle time: 2.5 μsec.
capacity: 2048 words
parity: no
type: core

c) ARITHMETIC FEATURES:

data representation: Binary, 2 s complement
serial/parallel: parallel
number of registers (G. P.): 2
number of inst: 64
instruction words: 24 bits
op. code field: 6 bits
address field: 15 bits
add time: 6 μ sec.
multiply time: 18.0 μ sec. (12 bits)
30.0 μ sec. (24 bits)

d) ADDRESSING:

index registers: 4 Hardware
indirect: Yes
effective address: Direct to 32K words
access to general loc.: index, direct, indirect

e) INPUT/OUTPUT

channels: one ext controlled I/0 channel, one prog. controlled I/0 channel
data length: 24 bits
parity: none
basic I/0 data path: Ext. controlled: Memory- I/0; prog. controlled: memory→S→X→I/0;
Data → X → Adder → AC C → Memory
word rate: 333 kc. Ext. Controlled; progr. controlled: 83 kc
I/0 control word loc.: Ext. controlled: by ext. device; prog control: NA
max. block length: 512
chaining: no

interrupt levels: 3- type 1; 16 type 3(ext.)
nesting: yes
dynamic priority assignment: no - has mask register to disable interrupt

f) PHYSICAL CHARACTERISTICS:

| | 16K | 8K |
|---|---|---|
| weight: | 70 lbs. | 46 lbs. |

volume: .851 cu. ft.
power: 230 watts
implementaton: integrated ckts.

g) OPERATING CHARACTERISTICS:

MTBF: 4750 hrs.
temp.: NA
vibration: NA

h) PERIPHERAL DEVICES:

bulk storage: none
CRT: none
typewriter: none
others: none

i) COMPATIBILITY:

CDC 1604, CDC 3600 Simulation software can assemble program on these machines

j) EQUIPMENT MATURITY:

components flight tested

k) OTHER FEATURES:

1) Program "look-ahead"
2) Real Time Clock
3) Ext. I/0 controlled addressing

L) SOFTWARE:

See: 5400 Profile

Computer: CDC 5400

a) MAIN MEMORY: (Instructions)

word length: 24 Bits
cycle time: 2.5 μ sec.
capacity: 32K words
parity check: no
protection: yes - power transient
type: thin film NDRO

b) SCRATCH PAD MEMORY: (Variables)

word length: 24 bits
cycle time: 2.5 μ sec.
capacity: 4K words
parity: no
type: core DRO

c) ARITHMETIC FEATURES:

data representation: binary, 2C
serial/parallel: parallel
number of registers (G.P): 2
number of inst. 70
instruction word: 24 bits
op. code field: 6 bits
address field: 15 bits
add time: 2.5 - 3.1 μ sec.
multiply time: 15.0 μ sec. at 12 bits
24.0 μ sec. at 24 bits

d) ADDRESSING:

index registers: 4 hardware
indirect: yes
effective address: direct to 32K
access to general loc.: indexed, direct, indirect

e) INPUT/OUTPUT

channels: 3 (external, prog, and special controlled)
data length: 24 bits
parity: none
basic I/0 data path: Programmed: Input: Data → X → Adder → Acc → Mem
Output: memory OCU → S → X → Data
Ext: Memory - I/0 channel
word rate: Prog: 100K words/sec; Ext: 400 K words/sec.; special: 100 K words/sec
I/0 control word loc: Prog.: memory, ext: via ext device
max. block length: 512
chaining: no

interrupt levels: 16 external
nesting: yes
dynamic priority assignment: no - prog enable/disable of interrupts only

f) PHYSICAL CHARACTERISTICS:

| | 16K | 8K |
|---|---|---|
| weight: | 45 lbs | |
| volume: | 1.1 cu. ft. | .55 cu. ft. |
| power: | 190 watts | |
| implementation: | integrated DTL | |

g) OPERATING CHARACTERISTICS

MTBF: 4750 hrs.
temp: ) MIL-E-5400
vibration: )

h) PERIPHERAL DEVICES:

bulk storage: No airborne peripherals
CRT: No airborne peripherals
typewriter: No airborne peripherals
other: No airborne peripherals

i) COMPATIBILITY:

Simulator software permits program assembly in either CDC 1604 or 3600

j) EQUIPMENT MATURITY:

Components flight tested

k) OTHER FEATURES:

1) Real time clock
2) Look ahead
3) Externally specified addressing

L) SOFTWARE:

1) Assembly System
2) Simulator
3) Utility
4) Debugging aids

Computer: CDC-5360

a) MAIN MEMORY:

word length: 24 Bits
cycle time: 6 μ Sec.
capacity: 8K - 32K
parity check: No
protection: Yes - Power Transient
type: Core

b) SCRATCH PAD MEMORY:

word length: None
cycle time: None
capacity: None
parity: None
type: None

c) ARITHMETIC FEATURES:

data representation: Binary, 2s Complement
serial/parallel: Parallel
no. of registers (G.P.) : 2
number of inst: 31
instruction word: 24 Bits
op. code field: 5 Bits
address field: 15 Bits
add time: 12 μ Sec.
multiply time: 90 μ Sec.

d) ADDRESSING:

index registers: 28 located in core
indirect: yes
effective address: directly addressable to 32 K.
access to general loc.: Direct, indexed, Indirect

e) INPUT/OUTPUT

channels: 2-24 Bit parallel I/O channels; 2-8 Bit parallel I/O channels; 2-serial input, (1 serial); also: 24 discrete inputs (8 are output channel interrupts)

data length: 24 Bit, 8 Bit, serial bus
parity: None
basic I/O data path: memory ↔ accumulator ↔ I/O channel
word rate: 18,300 words/sec, 83,500 words/sec (short), 167,600 bits/sec. serial
I/O control word loc.: arithmetic unit
max. block length: 1
chaining: no

interrupt levels: 8
nesting: no
dynamic priority assignment: No

f) PHYSICAL CHARACTERISTICS:

8 K Mem.
weight: 35 lbs.
volume: .6 cu. ft.
power: 125 Watts
implementation: Integrated CKT.

g) OPERATING CHARACTERISTICS

MTBF: 2840 hrs.
temp.: ) MIL-E-5400
vibration: )

h) PERIPHERAL DEVICES:

bulk storage: No airborne peripherals
CRT: No airborne peripherals
typewriter: No airborne peripherals
others: No airborne peripherals

i) COMPATIBILITY:

Assembly language (MICAP) operated on CDC 1604, CDC 3600 prepares object code for 5360. via simulation package.

j) EQUIPMENT MATURITY:

Fire control calculations for Hughes PHOENIX air-air missile

k) OTHER FEATURES:

Optional: external specified address

L) SOFTWARE

Assembly program
utility
diagnostic
simulation

Computer: HUGHES HCM-206

a) MAIN MEMORY:

word length: 32 Bits
cycle time: 2 μSec.
capacity: 8-32K
parity check: Opt.
protection: Power transient
type: Core

b) SCRATCH PAD MEMORY: (Optional)

word length: Part of main mem.
cycle time: can be wired to
capacity: operate scratchpad
parity:
type:

c) ARITHMETIC FEATURES:

data representation: Binary, 2C
serial/parallel: Parallel
number of registers (G.P.): 8-Hardware
number of inst: 64
instruction word: 16 and 32 Bits
op. code field: 6 Bits
address field: 16 Bits
add time: 2 μSec.
multiply time: 9 μSec at 16 Bits
15 μSec at 32 Bits

d) ADDRESSING:

index registers: * 8 hardware
indirect: yes
effective address: Direct to 32 K words
access to genera. loc: Direct
Indirect
Indexed
Ret. Jump.

e) INPUT/OUTPUT

channels: Two (one to each indep. mem. bank)
data length: 32 Bits
parity: No
basic I/0 data path: Mem-I/0 channel
word rate: 500 K words/sec/mem. bank
I/0 control word loc.: I/0 channel hardware
max. block length: 32K.
chaining: no

interrupt levels: 32
nesting: yes
dynamic priority assignment: Yes

f) PHYSICAL CHARACTERISTICS:

8K Mem.
weight: 20 lbs.
volume: .375 cu. ft.
power: 250 watts
implementation: I.C. (DTL)

g) OPERATING CHARACTERISTICS:

MTBF: 6,400 hrs.
temp.: -54°C to +85°C
vibration: 10 cps.RMS at 1KC. BW.

h) PERIPHERAL DEVICES:

bulk storage: Drum (See NCM 205profile
CRT: NA
typewriter:
others:

i) COMPATIBILITY:

Simulator for IBM 7094

j) EQUIPMENT MATURITY:

Prototype in development phase

k) OTHER FEATURES:

1) floating point hardware
2) Scratch pad option
3) Memory banks, independent access

L) SOFTWARE: (Available 2 67)

1) Simulator
2) Assembler
3) Compiler
4) Monitor
5) Library
6) Diagnostics

*Index registers are 32 bits including both address and countdown fields.

Computer: HUGHES NCM-205

a) MAIN MEMORY:

word length: 18 Bits
cycle time: 2 μ sec.
capacity: 2-8K
parity check: no
protection: Power transient
type: Core DRO

b) SCRATCH PAD MEMORY: (optional)

word length: Part of main memory
cycle time: can be wired to operate
capacity: scratchpad.
parity:
type:

c) ARITHMETIC FEATURES:

data representation: Binary, 2C
serial/parallel: Parallel
number of registers (G. P): - NA
number of inst: 42
instruction word: 18 Bits
op code field: 5 Bits
address field: 10 bits
add time: 4 μ Sec.
multiply time: 24 μ Sec.

d) ADDRESSING:

index registers: 3 Hardware
indirect: yes
effective address: Direct 1K Bank and relative to base add reg.
access to general loc: Direct, Indirect, Indexed, Ret. Jump.

e) INPUT/OUTPUT:

Channels: One bilateral
data length: 18 Bits
parity: No
basic I/0 data path: M.em to I/0 channel
word rate: 500K words/sec.
I/0 control word loc.: I/0 chan. hardware
max. block length: 8 K.
chaining: no.

Interrupt levels: One
Nesting: No
Dynamic priority assignment: No.

f) PHYSICAL CHARACTERISTICS:

| | 8K memory |
|---|---|
| weight: | 16 lbs |
| volume: | .2 cu. ft. |
| power: | 110 watts |
| implementation: | I. C. (ITL) |

g) OPERATING CHARACTERISTICS:

MTBF: 15,000 hrs.
Temp: -54 °C to +85 °C
Vibration: 10 g's RMS at 1000 CPS BW

h) PERIPHERAL DEVICES:

bulk storage: Drum*
CRT: - NA
typewriter: - NA
others: - NA

i) COMPATIBILITY:

With simulator compatible with IBM 7094. Another simulator to be available for GE 600 series

j) EQUIPMENT MATURITY:

Prototype in evaluation phase

k) OTHER FEATURES:

1) Scratch pad option

L) SOFTWARE: (To be ready 8/66)

1) Assembler
2) Simulator
3) Diagnostics
4) Library

* DRUM:

| | |
|---|---|
| Capacity: | $6.08 \times 10^5$ Bits |
| Access: | 6 MS. Aver. Access |
| Wt. | 7.5 lbs. |
| Power: | 75 watts |
| Volume: | .138 cu. ft. |

Computer: UNIVAC 1824C

a) MAIN MEMORY:

word length: 48 bits
cycle time: 4 μ sec.
capacity: 3K-18K words (i.e. 16 bit words)
parity check: no
protection: software power surge protect
type: thin film-NDRO

b) SCRATCH PAD MEMORY:

word length: 24 bits
cycle time: 4 μ sec
capacity: 256 words
parity: no
type: core-DRO

c) ARITHMETIC FEATURES:

data representation: Binary, 2s complement
serial/parallel: parallel
no. of registers (G.P): 1
no. of inst: 45
instruction word: 16 bits
op. code field: 5 bits
address field: 8 bits
add time: 8 μ sec.
multiply time: 64 μ sec.

d) ADDRESSING:

index registers: 3 registers located in thin film memory
indirect: no
effective address: relative to bank address register
access to general loc.: direct, indexed, return jump

e) INPUT/OUTPUT

channels: 2 buffered I/O (actual config. tailored to requirement)
data length: 24 bits
parity: no
basic I/O data path: memory-I/O chan. or acc. - I/O channel
word rate: Direct: 120,000 words/sec; indirect: 82,000 word/sec.
I/O control word loc.: accumulator
max. block length: 1
chaining: no

interrupt levels: 2
nesting: no
dynamic priority assignment: no

f) PHYSICAL CHARACTERISTICS:

max memory config. (18K)
weight: 55 lbs.
volume: .67 cu. ft.
power: 95 watts
implementation: integrated ckt, DTL

g) OPERATING CHARACTERISTICS:

MTBF: 10,000 hrs.
temp.: } MIL.STD-810
vibration: } FS - 151A
USAF-BSD 62-87

h) PERIPHERAL DEVICES:

bulk storage: mag. tape
CRT: NA
typewriter: NA
others: NA

i) COMPATIBILITY:

Compatible with UNIVAC 1206, 490 and 1230 with interpreter simulator software package

j) EQUIPMENT MATURITY:

Airforce Guidance Computer
Titan III SABRE

k) OTHER FEATURES:

1. ESI
2. Real time clock
3. I/O custom to requirements

L) SOFTWARE:

Assemblers (1824 and 1206)
interpreter for 1206
(service library)

Computer: IBM - LVDC

a) MAIN MEMORY:

word length: 26 bits
cycle time: 2 μ sec.
capacity: 4-32K words
parity check: yes
protection: parity only
type: core

b) SCRATCH PAD MEMORY:

word length: none
cycle time: none
capacity: none
parity: none
type: none

c) ARITHMETIC FEATURES:

data representation: binary, 2s comp.
serial/parallel: serial
no. of registers (G.P): 1
no. of inst. 18
instruction word: 13 bits
op. code field: 4 bits
address field: 9 bits
add time: 82 μ sec.
multiply time: 328 μ sec.
separate add/sub and mul/div arith. units

d) ADDRESSING:

index registers: none
indirect: none
effective address: 1) relative to sector* address. 2) direct to a 256 word sector register
access to general loc.: direct, hop

*Sector: 256 words

e) INPUT/OUTPUT:

channels: one
data length: serial bus only
parity: no
basic I/O data path: via accumulator
word rate: 12,000 words/sec (156,000 bits/sec.)
I/O control word loc.: instruction register
max. block length: single word
chaining: no

interrupt levels: one -
nesting: no
dynamic priority assignment: no

f) PHYSICAL CHARACTERISTICS:

32K memory (w. o. power supply
weight: 78.5 lbs.
volume: 2.2 cu. ft.
power: 142 watts
implementation: integrated CKT and delay lines

g) OPERATING CHARACTERISTICS:

MTBF: 25,000 hrs.
temp: } MIL-E-5400
vibration: }

h) PERIPHERAL DEVICES:

bulk storage: Drum**
CRT: - NA
typewriter: - NA
others: mag. tape unit (GEMINI)

i) COMPATIBILITY:

compatible with IBM 7090--7094 with simulator package

j) EQUIPMENT MATURITY:

used in SATURN vehicle for navigation.

k) OTHER FEATURES:

separate mul/div - add/sub arith. unit

L) SOFTWARE:

assembler

DRUM**: $10^6$ bits storage
12,000 RPM
2.5 lbs.
40 cu. in.
20 watts

Computer: LITTON L-306

a) MAIN MEMORY:

word length: 32 bits
cycle time: 1.8 μ sec.
capacity: * 131 K words
parity check: no
protection: power failure
type: core

b) SCRATCH PAD MEMORY:

word length: none
cycle time:
capacity:
parity
type:

c) ARITHMETIC FEATURES:

data representation: Binary, 2C
serial/parallel: parallel
no. of registers: 8 G.P. (memory)
no. of inst: 63
instruction word: 32 bits
op. code field: 6 bits
address field: 16 bits
add time: 1.8 μ sec.
multiply time: 8.1 μ sec.

d) ADDRESSING:

index registers: 8 X64 prog. levels (memory)
indirect: yes
effective address: Direct to 32K words relative to bank add reg. to 131K
access to general loc.: Direct, Indirect, Indexed, Ret. jump

e) INPUT/OUTPUT:

channels: 8 I/O exchange units
data length: 32 bits or 8 bit char.
parity: no
basic I/O data path: Mem. -I/O exchange channel
word rate: 278 K words/sec. or 556K words/sec burst mode
I/O control word loc.: memory
max. block length: 4K words or 4K characters (8 bit)
chaining: no

interrupt levels: 64
nesting: yes
dynamic priority assignment: No. program interrupt enable/disable only (activation)

f) PHYSICAL CHARACTERISTICS:

| | 8K memory |
|---|---|
| weight: | 46 lbs. |
| volume: | .36 cu. ft. |
| power: | 140 watts |
| implementation: | I.C. (TTL) |

g) OPERATING CHARACTERISTICS:

MTBF: > 2300 hrs.
temp.: -55°C to +125°C.
vibration: NA

h) PERIPHERAL DEVICES:

bulk storage: No peripherals
CRT:
typewriter:
others:

i) COMPATIBILITY:

interpretive simulator permits assembly on IBM 7094

j) EQUIPMENT MATURITY:

development phase

k) OTHER FEATURES:

1) multiprocessing capability
2) look ahead

L) SOFTWARE:

1) Simulator (IBM 7094-94)
2) Assembler
3) Diagnostics
4) Service routines
5) Function subroutines

Note: The L-304 and L-305 are similar to L-306 with exception denoted:

| | Add Time | Multiply | Vol. | Wt. | Power |
|---|---|---|---|---|---|
| L-304 | 6.3 μ sec. | 19.8-34 μ sec. | .28 cu. ft. | 38 lbs. | 100 W. |
| L-305 | 3.6 μ sec. | 9.9-17 μ sec. | .31 cu. ft. | 40 lbs. | 120 W. |

* 4K modules at 1.6 μ sec. cycle time optional

Computer: LITTON L-3060

a) MAIN MEMORY:

word length: 32 bits
cycle time: 1.8 μ sec.
capacity: * 8-131K words
parity check: none
protection: power failure
type: core

b) SCRATCH PAD MEMORY:

word length: None
cycle time:
capacity:
parity:
type:

c) ARITHMETIC FEATURES:

data representation: Binary, 2c
serial/parallel: parallel
no. of registers (G.P): 16 (memory)
number of inst: 500 inst and variations (64 basic)
instruction word: 16 or 32 bits
op. code field: 6 bits
address field: 16 bits
add time: 1.8 μ sec.
multiply time: 4.5 - 8.1 μ sec.

d) ADDRESSING:

index registers: 7 G.P. (memory)
indirect: yes
effective address: direct to 32K words
relative to bank
add. reg. to 131K
access to general loc.: Direct, indirect
indexed, return jump

e) INPUT/OUTPUT:

channels: up to 8 I/0 exchange units
data length: 32 bits or 8 bit char.
parity: no
basic I/0 data path: memory-I/0 exchange
word rate: 278 K burst mode
I/0 control word loc.: memory
max. block length: 4K words or 4K char.
chaining: no

interrupt levels: 64
nesting: Yes
dynamic priority assignment: No - program enable/disable

f) PHYSICAL CHARACTERISTICS:

8K Mem.
weight: 50 lbs.
volume: .38 cu. ft.
power: 150 watts
implementation: IC. (TTL)

g) OPERATING CHARACTERISTICS:

MTBF: > 2100 hrs.
temp.: -55°C to + 125°C.
vibration: NA

h) PERIPHERAL DEVICES:

bulk storage: no peripherals
CRT:
typewriter:
others:

i) COMPATIBILITY:

interpretive simulator permits assembly on IBM 7094

j) EQUIPMENT MATURITY:

development phase

k) OTHER FEATURES:

1) multi processor capability

L) SOFTWARE:

1) Simulator
2) Assembler
3) Diagnostics
4) Service routines
5) Function subroutines

* 4 K modules at 1.6 μ sec Available Optionally

Note: L-3040 and L-3050 are similar to L-3060 with exceptions noted:

| | Add | Mult | Wt. | Vol. | Power |
|---|---|---|---|---|---|
| L-3040 | 6.3 μ sec. | 12.6-21.5 μ sec. | 38# | .28 cu. ft. | 110 W. |
| L-3050 | 3.6 μ sec. | 6.3 - 9.9 μ sec. | 44# | .33 cu. ft. | 130 W. |

Computer: TRW MARCO-4418

a) MAIN MEMORY:

word length: 18 bits
cycle time: 5 μ sec.
capacity: 2-8 K words
parity check: no
protection: no
type: core

b) SCRATCH PAD MEMORY:

Optional
word length: trade off with main
cycle time: memory to 4K.
capacity:
parity:
type:

c) ARITHMETIC FEATURES:

data representation: binary
serial/parallel: parallel
no. of registers(G. P): NA
no. of inst: 27
instruction word: 18 bits
op. code field: 5 bits
address field: 12 bits
add time: 10 μ sec.
multiply time: 70 μ sec.

d) ADDRESSING:

index registers: one hardware
indirect: no
effective address: Direct address to 4K
relative bank register to 8K
access to general loc: index, direct

e) INPUT/OUTPUT:

channels: One * basic bilateral
data length: 18 bits
parity: no
basic I/0 data path: via accumulator
word rate: 33,000 words/sec.
I/0 control word loc.: arithmetic unit
max. block length: one word
chaining: no

interrupt levels: one line
nesting: none
dynamic priority assignment: none

* I/0 includes interface to handle:
Discretes
Serial binary
Analog
Pulse data

f) PHYSICAL CHARACTERISTICS:

| | 8K mem. |
|---|---|
| weight: | 32.5 lbs. |
| volume: | .56 cu. ft. |
| power: | 75 watts |

implementation: integrated ckt. (DTL)

g) OPERATING CHARACTERISTICS:

MTBF: 20,000 hrs.
temp.: } to NASA spec.
vibration: }

h) PERIPHERAL DEVICES:

bulk storage: - NA
CRT: - NA
typewriter: - NA
others: -Leach mag. tape

i) COMPATIBILITY:

Simulated on 7094 and GE 635

j) EQUIPMENT MATURITY:

Used in NASA LEM (Lunar exclusion module)

k) OTHER FEATURES:

NA

L) SOFTWARE:

1) assembly program
2) simulator interpretive
3) diagnostics
4) service library

Computer: UNIVAC 1830-A

a) MAIN MEMORY:

word length: 36 bits
cycle time: 2 μ sec (has overlapped mem.)
capacity: 32K up to 131K words
parity check: none
protection: software-power surge
type: core

b) SCRATCH PAD MEMORY: (Optional)

| | |
|---|---|
| word length: | None with basic unit |
| cycle time: | None with basic unit |
| capacity: | None with basic unit |
| parity: | None with basic unit |
| type: | None with basic unit |

c) ARITHMETIC FEATURES:

data representation: Binary one's complement
serial/parallel: Parallel
no. of G.P registers: 1
no. of inst: 62
instruction word: 30 bits
op. code field: 6 bits
address field: 15 bits
add time: * 2 μ sec. (assumes overlap)
multiply * time: 18 μ sec. (assumes overlap)

d) ADDRESSING:

index registers: 7 hardware
indirect: limited to indirect jump
effective address: direct, indexed
access to general loc.: indexed, direct, indirect return jump, bank relative if 232K memory

e) INPUT/OUTPUT:

channels: 16 I/0 channels
data length: 30 bits
parity: none
basic I/0 data path: memory - I/0 channel
word rate: 167,000 words/sec
I/0 control word loc.: core
max. block length: 32K words
chaining: no

interrupt levels: 81
nesting: none
dynamic priority assignment: no

* add 2 μ sec. if overlapped memory is not utilized, (i.e. where instruction and operand are in different banks)

f) PHYSICAL CHARACTERISTICS:

| | 32K |
|---|---|
| weight: | 190 lbs. |
| volume: | 3 cu. ft. |
| power: | 567 Watts |
| implementation: | integrated ckts. |

g) OPERATING CHARACTERISTICS:

MTBF: 4500 hrs.
temp: } MIL-E-5400
vibration: }

h) PERIPHERAL DEVICES:

bulk storage: No spaceborne periph.
CRT: "
typewriter: "
others: "

i) COMPATIBILITY:

directly compatible with UNIVAC 1230

j) EQUIPMENT MATURITY:

equipment in development phase

k) OTHER FEATURES:

1. ESI or/and ESA

L) SOFTWARE:

Assembler (AS-1)
Compiler (CS-1
Utility
Diagnostics
Mathematical

| MACHINE | MAIN MEMORY | | | |
|---|---|---|---|---|
| | Word Size | Cycle Time (μ sec) | Capacity $10^3$ words | Overlap Banks |
| AUTONETIC D26C | 30 | 6 | 32 | |
| AUTONETIC D26J | 12 or 16 | 6 | 16 | |
| CDC 5360 | 24 | 6 | 32 | |
| CDC 5400 | 24 | 2.5 | 32 | |
| CDC 5400-8 | 24 | 3.0 | 32 | |
| HONEYWELL-ALERT | 24 | 5.0 | 32 | |
| HUGHES HCM205 | 18 | 2.0 | 8 | |
| HUGHES HCM206 | 32 | 2.0 | 32 | |
| IBM 4π - CP | 16 | 2.5 | 32 | |
| IBM 4π - EP | 32 | 2.5 | 165 | |
| LITTON L-304 | 32 | 1.8 | 131 | |
| LITTON L-305 | 32 | 1.8 | 131 | Yes |
| LITTON L-306 | 32 | 1.8 | 131 | |
| LITTON L-3040 | 32 | 1.8 | 131 | |
| LITTON L-3050 | 32 | 1.8 | 131 | |
| LITTON L-3060 | 32 | 1.8 | 131 | |
| NORTHROP NDC-1051 | 24 | 2.0 | 8 | |
| TRW 4418 | 18 | 5.0 | 8 | |
| UNIVAC 1824-C | 48 | 4.0 | 6 | |
| UNIVAC 1830-A | 30 | 2.0 | 131 | Yes |
| UNIVAC 1818 | 18 | 20 | 32 | |
| IBM LVDC | 26 | 2.0 | 32 | |

| SCRATCH PAD | ARITHMETIC FEATURES | | | | | ADDRES |
|---|---|---|---|---|---|---|
| | Par/ Ser. | Instr. Set | Add Time (μ sec) | Mul Time (μ sec) | Rated Speed (μ sec) | Index Registers |
| 256 words | P | 87 | 6-12 | 33-45 | 15.4 | 1H |
| None | P | 27 | 12 | 42-54 | 18.3 | None |
| None | P | 31 | 12 | 90 | 18.9 | 28 M |
| 4k words | P | 70 | 2.5-3.1 | 15-24 | 6.0 | 4 H |
| 2 k words | P | 64 | 6.0 | 18-30 | 7.0 | 4 H |
| None | P | 64 | 2.0 | 12.0 | 4.0 | 6 H |
| Opt. | P | 92 | 4.0 | 24 | 5.2 | 3 H<br>8 H |
| Opt. | P | 64 | 2 | 9-15 | N/A | 8 H |
| None | P | 51(b)<br>31(e) | 8.5(b)<br>5.0(e) | 12 (b)<br>42 (e) | N/A | 8 M |
| None | P | 78 | 1.66(r)<br>5.0 (m) | 8.7 (r)<br>12.0 (m) | 2.6 | 16 H |
| None | P | 63 | 6.3 | 19.8-34 | 7.8 | 512 M |
| None | P | 63 | 3.6 | 10-17 | 4.6 | 8 H and 512 M |
| None | P | 63 | 1.8 | 8.1 | 2.8 | 3 H and 512 M |
| None | P | 63 | 6.3 | 12.6-21.5 | 7.0 | 1024 M |
| None | P | 63 | 3.6 | 6.3-9.9 | 4.0 | 7 H and 1024 M |
| None | P | 63 | 1.8 | 4.5- 8.1 | 2.4 | 7 H and 1024 M |
| None | P | 39 | 8.0 | 72 | 11.1 | 7 M |
| Opt. | P | 27 | 10 | 70 | 17.0 | 1 H |
| 1 k words | P | 47 | 8 | 64 | 14.5 | 7 M |
| Opt. | P | 62 | 2 | 18 | 3.9 | 7 M |
| 32 k words | P | 32 | 4-6 | 24.5 | N/A | 3 H |
| None | S | 18 | 82 | 328 | 190.1 | None |

| SSING CAPABILITIES | | | INPUT/OUTPUT | | | PHYSICAL (12 k MEMORY) | | | M |
|---|---|---|---|---|---|---|---|---|---|
| Indirect | Reference | Page Size | Chan. No. (parallel) | Speed $10^3$ WPS | Inter-rupts | Weight (lbs) | Vol. (cu. ft.) | Power (watts) | |
| No | Direct | -- | 1 | 13.8 | 8 | 47 | .65 | 175 | |
| No | Relative to Bar | 128 or 512 | 1 | 13.8 | 1 | 20 | .21 | 62 | |
| Yes | Direct to 32 k | -- | 2 | 18.3 | 8 | 35 | .60 | 125 | |
| Yes | Direct | -- | 3 | 100 | 16 | 39 | 1.0 | 155 | |
| Yes | Direct | -- | 2 | 333 ext. 82 prog. | 16 | 58 | .80 | 190 | |
| Yes | Direct | -- | 4 | 166 | 8-24 | 60 | 1.21 | 194 | |
| Yes | Direct to 1 k Relative to Bar | 1 k | 1 | 500 | 1 | 16 | .2 | 110 | |
| Yes | Direct | -- | 2 | N/A | 32 | 20 | .375 | 250 | |
| No | Relative to Bar | -- | 2 | 165 aux. 80 burst | 8 | 37 | .8 | 250 | |
| No | Relative to Bar | -- | 3 | 165 mux 80 burst | 16 | 52 | .84 | 300 | |
| Yes | Direct to 32 k Relative to Bar >32 | -- | 8 | 278 mux 556 burst | 64 | 38 | .28 | 100 | |
| Yes | ↓ | -- | 8 | ↓ | 64 | 40 | .31 | 120 | |
| Yes | | -- | 8 | | 64 | 46 | .36 | 140 | |
| Yes | | -- | 8 | | 64 | 38 | .28 | 110 | |
| Yes | | -- | 8 | | 64 | 44 | .33 | 130 | |
| Yes | | | 8 | | 64 | 50 | .38 | 150 | |
| Yes | Relative to Bar | 4 k | 1 | 250 | None | 29 | .50 | 140 | |
| No | Relative to Bar | 4 k | 1 | 33 | 1 | 33 | .56 | 75 | |
| No | Relative to Bar | 256 | 2 | 82 120 | 2 | 55 | .67 | 95 | |
| No | Direct to 32 k Relative to Bar >32 | -- | 8 | 135 | 81 | 87 | 1.4 | 250 | |
| No | Relative to Bar | 512 | 1 | ? | None | 55 | 1.2 | 268 | |
| No | Direct 256 words Relative Bar | 256 | Serial Bus | 12 | 1 | 78.5 | 2.2 | 142 | |

| RELIABILITY MTBF (hrs) (Manuf. Est.) | COMPATIBILITY | SOFTWARE | AVAILABILITY | OTHER |
|---|---|---|---|---|
| 15.6 k | Simulated on IBM 2094 | S, A, C, U | Flight tested | Rt. clock; |
| 18.0 k | Simulated on IBM 7094 or CDC 3600 | S | Flight tested | |
| 2.8 k | Sim. on CDC 1604 or 3600 | S, A, U, D | Used in Phoenix missile | Opt. ESA |
| 4.7 k | Sim. on CDC 1604 or 3600 | S, A, U | Flight tested | Rt. clock; |
| 4.7 k | Sim. on CDC 1604, 3600 | S, A, U | Prototype | Rt. clock; |
| 10 k | Sim. on Honeywell 800 | S, A | Qualification testing | Character |
| 15 k | Sim. IBM 7094 | S, A, D, L | Prototype eval. | |
| 6.4 k | Sim. IBM 7094 | S, A, C, D, U, L | Developmental | Flt. pt. ha banks |
| 3.0 k | Direct on 360-40 up Direct 1800 or Sim.360 | S, A C, U | Hardware tested | Opt. inst. |
| 5.0 k | Direct IBM 360-40 up | S, A, C | Developmental early 1967 | Alterable |
| >2.3 k | Sim. IBM 7094 | S, A, D, U, L | Developmental | Multiproce |
| >2.3 k | | | | |
| >2.3 k | | | | |
| >2.1 k | | | | |
| >2.1 k | | | | |
| >2.1 k | | | | |
| 8.5 k | None | None | Prototype tested | |
| 20.0 k | Sim. IBM 7094 G. E. 635 | S, A, D, L | Used in LEM | |
| 10.0 k | Sim. UNIVAC 1230, 1206, 490 | S, A, L | Used for Titan III evidance | Rt. clock; |
| 4.5 k | Direct UNIVAC 1230 | S, A, D, U, L | Equip. in development | Rt. clock; |
| 1.5 k | None | None | New. avail: 6/67 | Rt. clock |
| 25.0 k | Sim. IBM 7090-94 | A | Used in Saturn vehicle | Separate a processin |

R FEATURES

ESA

ESA; look ahead

ESA; look ahead

or word addressing

ırdware; ind. mem.

set

inst. set

ssing capability

and look ahead

ESI

ESI; ESA

dd-mux
g

## LEGEND

| Under ARITHMETIC FEATURES | Under ADDRESSING CAPABILITIES |
|---|---|
| (b) 360 Inst. set | H = Hardware implement |
| (c) 1800 Inst. set | M = Memory implement |
| (e) Add from register | P = Parallel |
| (m) Add from memory | S = Serial |
| N/A Data not available | |
| Bar = Base address register | |

| Under SOFTWARE | Under OTHER FEATURES |
|---|---|
| S = Simulator | ESA = Ext. specified address |
| A = Assembler | |
| C = Compiler | ESI = Ext. specified index |
| D = Diagnostic | |
| L = Library | |
| U = Utility | |