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PROCESS TECHNIQUES STUDY OF INTEGRATED CIRCUITS

Quarterly Report No. 3

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INTRODUCTION

Experimental activities have evolved, as previously anticipated, along specific lines resulting from surveys performed earlier in the program. These lines of endeavor have been selected largely on the basis of two criteria: immediacy, and lack of understanding of mechanism or of control of process origin. In the consideration of immediacy, particular attention was given to the unique reliability requirements of NASA missions. The functional sensitivity of an integrated circuit to condensable package ambients in a space environment is an example of this type of problem. The investigation of package ambient compositions by mass spectrometry and gas chromatography was undertaken to discover correlations with abnormal integrated circuit function. Low temperature reverse bias leakage associated with traces of moisture has been observed with mesa transistors, and investigation is being continued with planar devices.

A second area of investigation considers the effects of tool damage on silicon, utilizing x-ray diffraction and etching procedures. Little consideration has been given to the long range effects of such damage particularly under varying stress, and even the short range effects have been assessed primarily in terms of manufacturing reject ratios.

A third newly introduced investigation explores the process origins of dielectric anomalies in passivation oxide with the objective of eliminating such defects by improved oxide growth techniques. A substantial contribution to this investigation is being made by test methods recently developed at Autonetics for revealing dielectric defects at any stage of wafer processing. The dielectric integrity requirements of the oxide in MOS gates are particularly severe and require careful process control. Thus far it has been shown that adjustment of gate oxide thickness by etching procedures increases the density of dielectric defects. Post oxidation treatments of such areas reduce but do

not eliminate the problem. Present evidence indicates that a significant proportion of dielectric defects is located at abrupt thickness transitions (steps) in the oxide. The structural discontinuities associated with such defects offer far less resistance to electrical discharge than sound oxide and are capable therefore of acting as loci for metallization to substrate shorts. Breakdown in sound silicon dioxide occurs at fields approaching 10^{-1} V/Å, but in air discharge occurs at approximately 10^{-4} V/Å. MOS gate voltage parameters seldom exceed 10^{-2} V/Å which is well within the dielectric capability of sound oxide but in considerable excess of that of gaseous insulation at ordinary pressures. Thus, shorting may occur regardless of whether the overlying metallization has penetrated a crack or pinhole in the oxide.

The behavior of ionic impurities in otherwise sound oxide was originally recognized as a key problem in planar technology, as discussed in the initial program proposal. The investigation of this problem by radiochemical and isotopic techniques is being continued along previously established lines.

ACCOMPLISHMENTS

Item 1

A. Tool Damage Effects

Initial investigations utilizing etching procedures on scribed and separated silicon dice (10 ohm cm p-type) revealed no significant residual crystal damage. In subsequent experiments, scribe marks were made on unoxidized silicon wafers which consisted of grooves about 10 microns wide with contiguous observable damage extending to a maximum width of about 50 microns. The width of the mark after etching ranged from 55 to 105 microns with a depth of about 20 microns. Smoothness of etched contours suggested that the specimen was overetched, and the experiment will be repeated.

B. Gas Ambient Effects

Mass spectrometry and gas chromatography have been employed to determine the gas contents in the ambient of semiconductor device packages (transistors and integrated circuits). A significant proportion of abnormal ambients has been observed, but their correlation with

failure mechanisms and process control problems has been achieved only in a few instances. Substantial additional effort is required to firmly establish the effects, or lack thereof, of gas ambients on device function.

Special techniques have been developed to analyze the gas in small devices without destruction of the device electrical parameters. Therefore, electrical characteristics could be monitored before, during, and after the gas was evacuated so that electrical changes could be correlated with removal of the ambients.

A failure mode concerned with excessive I_{CBO} leakage at subzero temperature in pnp mesa transistors was investigated using both mass spectrometry and gas chromatography. Initial mass spectrometric analysis of five electrically good devices and five low temperature failures indicated no significant differences in gas content. The major constituent in all devices was nitrogen with traces of argon, carbon dioxide, and methane. (No water was detected.) Gas chromatography was used for moisture analysis only. Using a column adsorbent of Carbowax 400 supported on Teflon, this procedure is sensitive to approximately 3×10^{-7} grams H_2O. All four of the low temperature failures analyzed showed detectable moisture content between 0.025 and 0.24 weight percent. Five out of six electrically good devices showed no detectable moisture. The lower limit of detection was estimated at 0.01 to 0.06 weight percent for the gas chromatographic techniques currently in use. It is therefore postulated that the low temperature failures are related to the condensation of moisture on the device surfaces below the dew point of the package gas. It is possible that the water mobilizes ionizable surface contamination which may then migrate in surface potential gradients and cause anomalous leakage currents.

Analysis of the data was made to determine the origin of the noted moisture. Since oxygen was detected in only one device out of ten subjected to mass spectrometry, the possibility of in-leakage of air (containing moisture) is small. Therefore, it is believed that processing prior to or during the package lidding step allowed introduction of the moisture. Possible sources are poor control of dry box ambients or improper bakeout of the transistor can before packaging.

The information obtained from this study will be of value in further device ambient studies. Since many surface failure mechanisms are related to ion transport, it is important that device moisture content be determined. Previous gas ambient investigations of integrated circuits by mass spectrometric technique failed to indicate the presence of water largely because of the extensive internal surface area available for condensation. Gas chromatography, on the other hand, utilizes the adsorptive characteristics of water in its detection and is not subject to this limitation.

C. Instrumentation and Processing Survey

The nonuniformity of wafer doping referenced in the Seventh Monthly Report has been found to be relatively common. Process variations aimed at decreasing this effect have not been generally adopted because other variables less amenable to control cause equal or greater resistivity perturbations. Some causes of nonuniform doping are considered to be variability of purity and structural perfection of bulk silicon, changing amounts of dopant absorbed and emitted by furnace tube walls, and variation in furnace temperature. Calculations of heat treansfer in a diffusion tube furnace, however, indicated that complete heating of carrier gas takes place in the first four inches of the tube so that convection currents generated in the hot zone are not significant, and smoothing of gas flow by baffles may not appreciably improve uniformity of diffusion.

Additional error also is introduced in resistivity measurement. Methods which may become superior to the four point probe technique include microwave absorption[1], infrared attenuated total reflectance (ATR)[2], and variation of resistance with temperature on epitaxial structures[3]. The first method is limited to surface resistivities of <1 ohm-cm for 10 mil penetration to <0.0001 ohm-cm for 0.1 mil penetration. It also gives average volume resistivity up to 60 ohm-cm. The sampled area is about 0.2 in^2. Infrared ATR requires a very flat 0.04 in. by 0.25 in. sample. It is accurate to only about 20 percent but may be amenable to refinement. The third method involves transconductance measurement of epitaxial layers on lower resistivity substrates of the same conductivity type. It is empirically based on the high temperature value at which resistance again drops to that of

room temperature. To date, the four point probe method, or modifications thereof, remains the most generally applicable nondestructive means of measuring resistivity, and the ASTM is presently comparing results on identical samples by different laboratories.

Additional compilation of instrumental capabilities and sensitivities includes the following: Improvement of the resolution of the electron microscope to 2.8 Å (theoretical present best is 2 Å) at the University of Chicago[4] and investigation of defects of less than 100 Å diameter in silicon[5], improvement of the resolution of the scanning electron microscope to 0.05 micron at Berkeley[6] and 0.008 micron at Argonne[7], mass spectroscopy by ion bombardment of areas about 13 mils square[8], gas chromatographic analysis of gases in one milligram of deposited tantalum film using xenon light flash to evaporate the sample[9], radiography to a resolution of 0.1 to 0.2 micron[10], thermal plotting by use of low melting point paints[11], and use of the Kelvin probe on areas as small as 25 microns across[12].

Current process technique innovations that may become subjects of future reliability investigation are: the use of silicon nitride for passivation layers and possibly encapsulation as developed by Sperry-Rand Corp.[13], and RF sputtering as a method for depositing passivation layers of silicon oxide and other insulators[14].

Item 2

A. Oxide Radiotracer Experiments

Previously counted tritium-active oxidized wafers were re-analyzed after 550 hours (23 days) exposure to a humid laboratory environment. The average hydrogen concentration in the oxide layers, as determined by the tritium beta activity, remained unchanged indicating negligible exchange of the tritium with ambient moisture. The corresponding data are presented in Table I.

Table I. Tritium Exchange With Humid Environment

Period	Sample	Net CPM, Total	Total H Atoms per cm^3	Average
Initial	1 (2)	345.4	3.6×10^{16}	2.7×10^{16}
	2 (3)	225.2	2.3×10^{16}	
	3 (4)	199.1	2.1×10^{16}	
After 550 hrs. Humid Exposure	1	354.6	3.7×10^{16}	2.7×10^{16}
	2	270.1	2.8×10^{16}	
	3	142.7	1.5×10^{16}	

Samples 1, 2, and 3 in this table correspond to Samples 2, 3, and 4 previously reported in the Second Quarterly Report, November 10, 1965.

The results given in Table I cannot be considered conclusive proof that the trapped tritium does not exchange with ambient moisture at room temperature because the process may be diffusion limited within the silicon dioxide. It will be recalled (Second Quarterly Report) that the oxidation run was terminated by a >1 hour bake in a tritium-free stream of nitrogen. This treatment may have depleted the outer SiO_2 surface in tritium. The spread in observed beta activities may have been due to a redistribution of tritium within the bulk of the SiO_2 prior to its possible exchange with the atmosphere. Subsequent beta counts should resolve this question.

Additional wafers prepared in the tritium run (October 7, 1965) are being submitted for beta activity analysis. These specimens will be metallized for subsequent tritium electromigration experiments.

Neutron activation analysis for sodium was carried out on the oxides of the samples listed in Table I. The composite sample, and a standard, were irradiated $\frac{1}{2}$ hour at 250 KW in a Mark I TRIGA reactor. The thermal neutron flux was 1.8×10^{12} n cm^{-2} sec^{-1}. The oxides were stripped from the wafers after irradiation (to isolate them from activities within the silicon wafers) and the combined solution concentrated by evaporation. The concentrate was counted overnight in a NaI well detector coupled to a multichannel pulse-height analyzer. The irradiated sodium standard was counted in identical geometry. The 2.75 Mev photopeak of Na^{24} was used for analysis because of the comparative freedom from interference by other residual activities (e.g., Si^{31}) present in the concentrate. Other peaks attributable to Au^{198}, Cu^{64}, and Mn^{56} also were observed.

The analysis revealed a sodium concentration of 1.1×10^{18} atoms/cm^3 oxide which is significantly higher than the hydrogen content. It also is slightly higher than that obtained on the wafers of the first tritium run (7.6×10^{17} atoms/cm^3) where no hydrogen chloride pretreatment of the equipment was used. Although this evidence suggests that the hydrogen chloride treatment was ineffective, the possibility of chance contamination by sodium during the period between the tritium run and

neutron irradiation cannot be completely ignored. This interval was 13 days for the first set of specimens and 26 for the second. The bulk of the sodium, however, probably deposits on (and into) the silicon dioxide layer during the cooling down period at the termination of oxidation.

A technique for incremental oxide removal using "buffered" HF has been standardized for use in determining the tritium distribution in the dielectric layers.

B. Isotopically Labeled Inversion Study

Previous investigations performed at Autonetics[15] have demonstrated that the recovery of a device from surface inversion can be described in terms of the activation energy for migration of charged species (ions) on the surface and in the oxide. Initial results had indicated some Minuteman II transistors to have time-temperature dependent I_{CBO} recoveries with activation energies between 0.6 and 0.7 ev which approximates those derived from independent determinations of hydrogen migration in the oxide.

An objective of the present program is to utilize this approach in establishing whether hydrogen ions play a role in inversions of steam-oxide passivated devices. Specifically, the experiment involves a comparison of the inversion recovery kinetics of two sets of devices, one fabricated by normal steam oxidation procedure, the other identical to the first except that pure D_2O is substituted for H_2O in the initial oxide growth. It is recognized, of course, that succeeding processing steps may serve to deplete the initially present deuterium or cause its exchange with ambient hydrogen. It also is conceivable that the difference between the recovery activation energies associated with the two groups will be insufficient to exceed the experimental precision. Consequently, a positive correlation between isotopic treatment and recovery activation energy will constitute positive evidence for the participation of hydrogen ions in inversion, but the absence of such a correlation should not be considered evidence to the contrary.

Fabrication of the required devices was requested from an external supplier. These consisted of 30 small signal transistors of a type employed in Minuteman II electronics, half of which were processed with

deuterium.

All 30 of the transistors were electrically good as-received. Their response to inversion stress, however, was variable. Consequently, they were subjected to initial inversion stress of 200C at -40 V_{CB} for various lengths of time in order to classify them in terms of usefulness for recovery experiments. In order to be useful, the device was required to show a leakage above 1 x 10^{-9} amps (with presently available instrumentation) when subjected to the inversion stress and to have a region where I_{CBO} is independent of voltage. This would indicate surface leakage as distinguished from bulk leakage.

A summary of the device characterization is shown in Table II. Electrically good devices are those which showed less than 1 x 10^{-9} amps leakage at -60 V_{CB} after stress.

Table II. Stress Response Distribution

Group	Device Characteristics	Number
I	Electrically Good	13
II	Ambiguous or not Useful	9
III	Suitable Inversion	8

The collector-base characteristics of devices initially showing ambiguous response are plotted in Figure 1 and of originally invertible devices in Figure 2. Subsequent testing revealed that invertible devices F-1 and E-10 (Figure 2) were too unstable to yield reliable recovery data, while device D-1 (Figure 1) proved sufficiently stable for study, yielding a net of eight suitable devices. Onset of collector-base leakage in this group, as shown in Figures 1 and 2, extended over a wide range of threshold voltages.

Inversion recovery kinetics of all eight devices were studied. The devices were subjected to 200C at -40 V_{CB} for a one hour period, then removed from the oven and quenched to room temperature using compressed air while still under electrical bias. The room temperature I_{CBO} was then measured at 5 volt intervals to 60 V_{CB}. The devices were then reheated, without electrical bias, at lower temperatures for specific time periods. After each storage period, the devices were removed from the oven, immediately quenched in air, and electrically tested. The

Fig 1 AMBIGUOUS CB CHARACTERISTICS

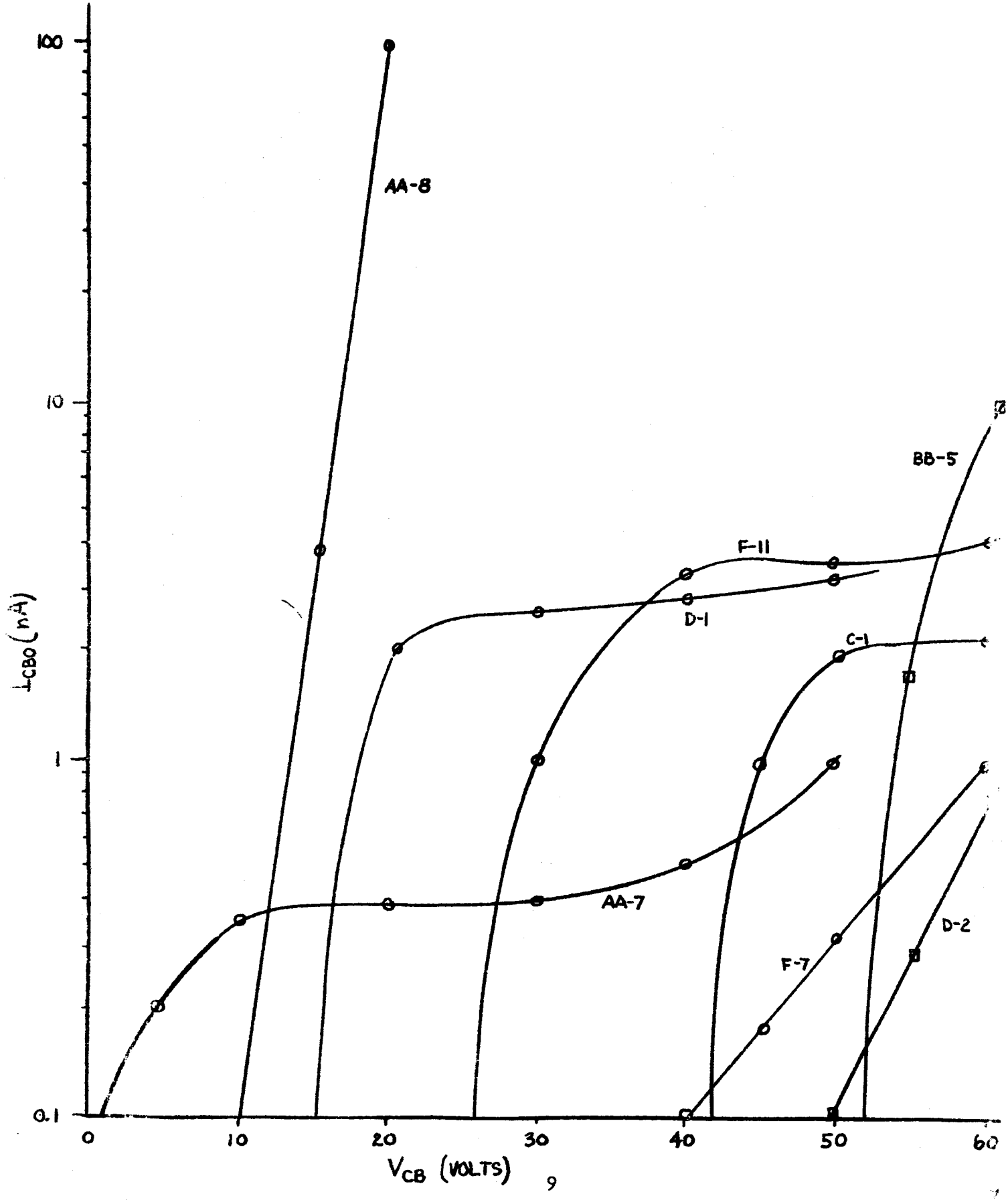
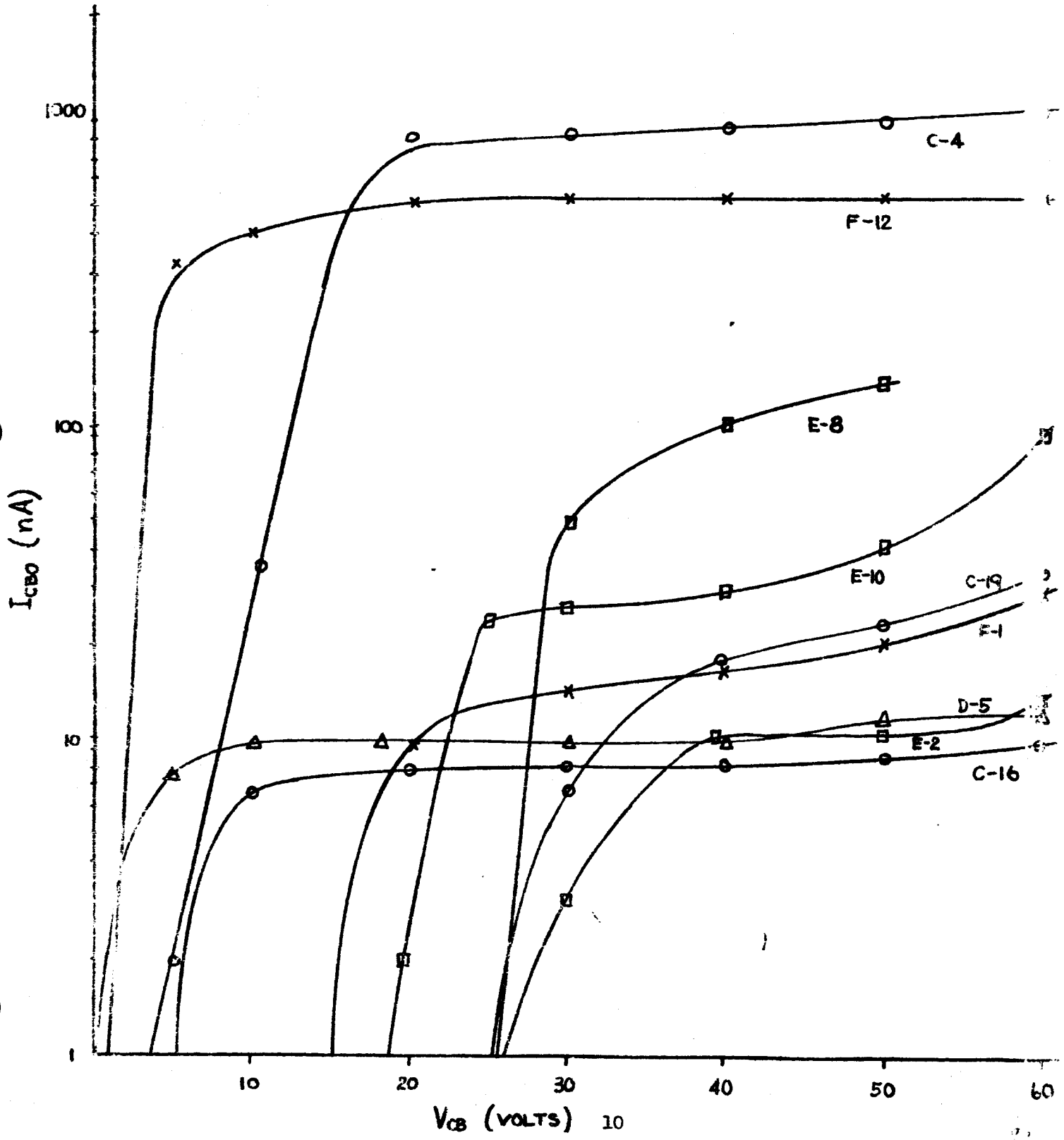


Fig. 2 SUITABLE INVERSIONS



procedure was repeated by re-inverting the transistors at 200C under bias and observing the time dependence of I_{CBO} recovery at additional selected baking temperatures. For example, the behavior of device F-12 after being inverted (upper curve) and then stored for various time intervals at 130C is shown in Figure 3. Note that above 10 volts, the I_{CBO} decreases normally with storage at 130C. However, below 10 volts, the initial storage (4 minutes) results in a relatively large decrease in I_{CBO} (from 340 to 80 na at 5 volts). However, succeeding recovery treatment results in an increase in the low voltage I_{CBO}. This behavior may indicate the transient appearance of a bulk leakage component in the electrical characteristic.

Following reference (15), I_{CBO} recoveries were normalized with respect to maximum (inverted) values (I'_{CBO}) to obtain correlative, constant temperature time dependences:

$$I_{CBO}/I'_{CBO} = 1 - (Dt)^{\frac{1}{2}}/\Delta r_{max} \qquad (1)$$

where D is the diffusion rate constant, t, the zero-bias constant-temperature storage interval, and Δr_{max}, the radius of maximum junction spreading associated with inversion. From linear plots of I_{CBO}/I'_{CBO} vs $t^{\frac{1}{2}}$ at several temperatures (derived from recovery sequences analogous to that of Figure 3), a convenient constant recovery ratio (e.g., 0.5) was selected. Since the associated diffusion process is thermally activated, the recovery times corresponding to the constant I_{CBO}/I'_{CBO} may be plotted against reciprocal absolute temperature and the thermal activation energy obtained from the resulting slope.

Activation energy plots of the eight devices are given in Figure 4. The recovery activation energies computed from these curves are presented in Table III where they are ranked in ascending order and correlated with the isotopic composition of the steam used in growing the initial oxide.

Fig. 3

RECOVERY OF TRANSISTOR F-12 AFTER BAKE AT 130 C

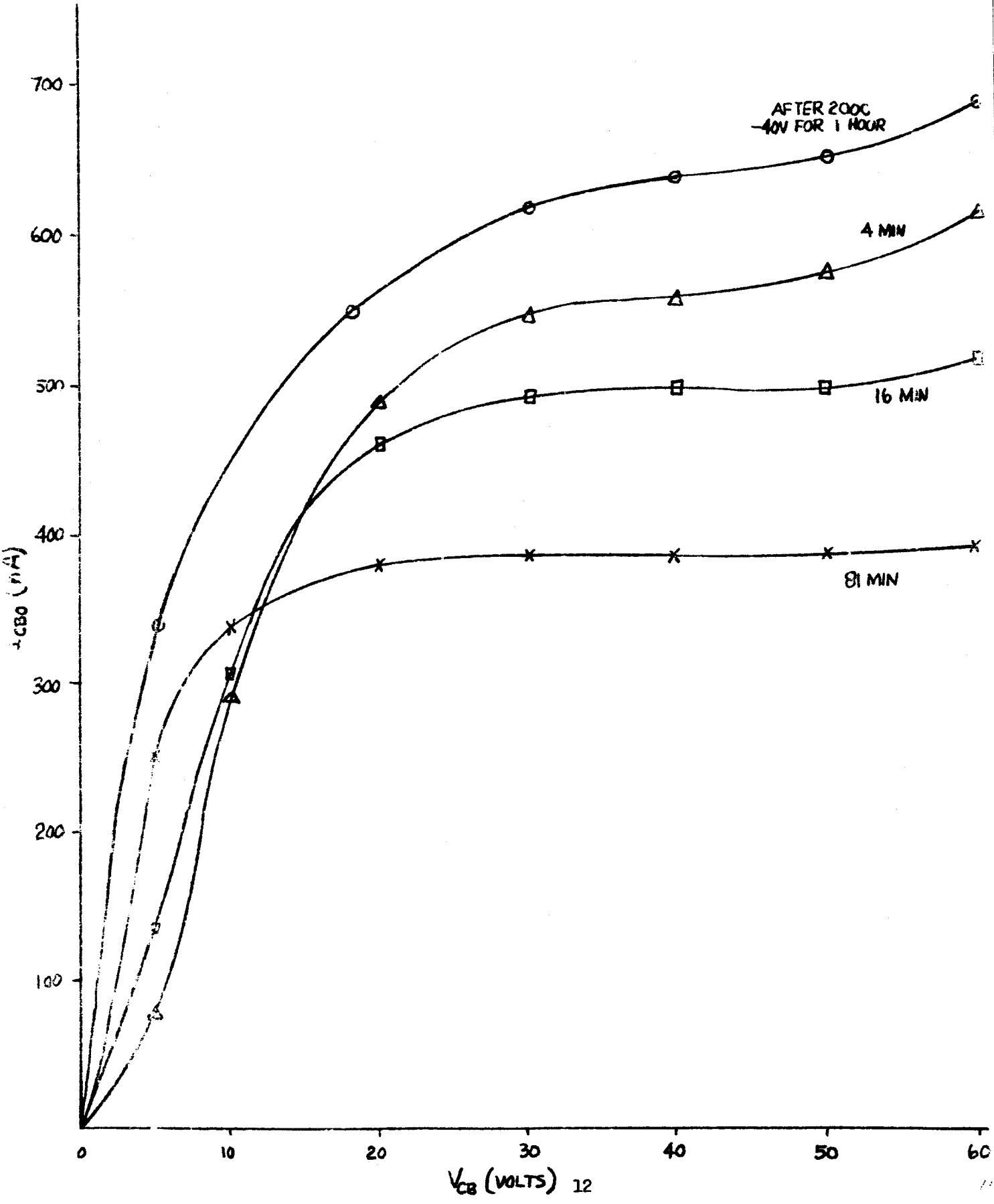


FIGURE 4
INVERSION RECOVERY

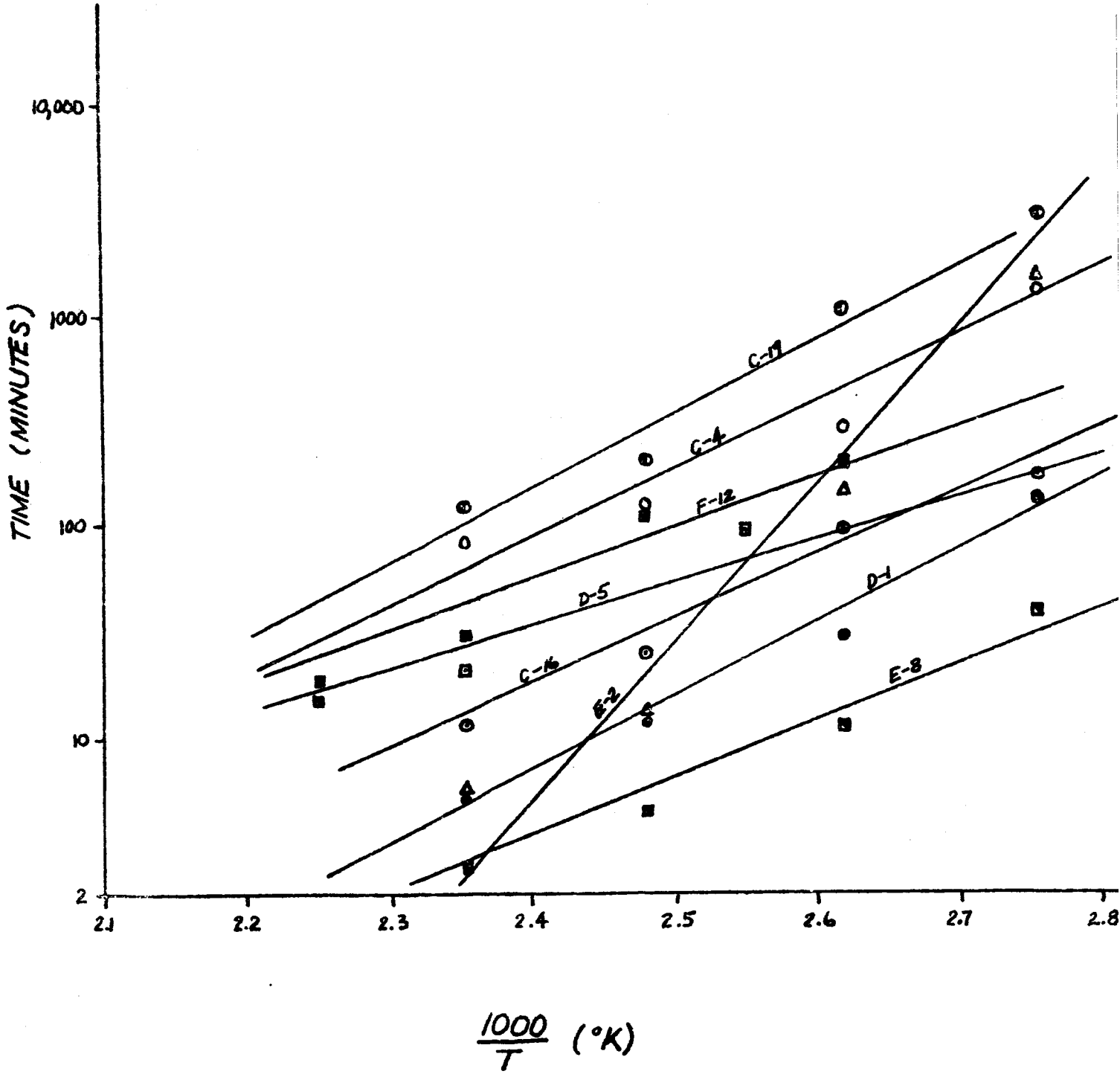


Table III. Inversion Recovery Activation Energies of Selected Small Signal Transistors

Sample Designation	E (Thermal) of Recovery (e.v.)	Group	Steam Used
D-5	0.46		H_2O
F-12	0.54	A	H_2O
E-8	0.56		D_2O
C-4	0.68		D_2O
C-19	0.70	B	D_2O
C-16	0.74		D_2O
D-1	0.74		H_2O
E-2	1.29	C	D_2O

The energy levels appear to fall into three distinct groups designated A, B, and C. Group A is seen to be dominated by normal steam treated devices and Group B, as expected, by deuterated specimens. The recovery activation energy of Group C (Device E-2, 1.29 e.v.) is uncharacteristic of the entire sample and suggests the presence of sodium as a contaminant. Excluding E-2, the average activation energy associated with the normal steam treated devices is 0.58 $\pm$ .08 e.v., and the deuterated devices, 0.67 $\pm$ .06 e.v. The spread in these results does not permit definite conclusions to be drawn at this time, especially in view of the uncertainties in some of the recovery data thus far taken. This is particularly true of device E-8 which did not yield sufficiently flat current leakage plateaus for accurate recovery rate determinations. The indicated trend, however, warrants a more precise investigation of these specimens.

C. Incidence of Dielectric Defects: Processing Contributions

The objective of this investigation is to vary the individual process steps in order to generate information on the optimum process compatible with device requirements which will provide an oxide with a high percentage of its area free from pores or regions of anomalously low dielectric breakdown.

The program is based on a technique for the detection of oxide dielectric defects designated the "Electric Probe Test" (to differentiate it from other detection methods). It consists of scanning a wafer immersed in methyl alcohol with a metal probe ~1 mm above the wafer at a

positive potential of 10-100 volts, and with the wafer resting on a negative plate. The hole or defect is indicated by bubbles (probably due to decomposition of the alcohol) and by the collection of insoluble metallic salts if certain metals are used for the probe. Other detection methods will be described as they are introduced into the program.

The initial experiments were made on oxides grown on high resistivity n-type substrates and on oxides grown over boron-doped regions during the diffusion of boron into the n-type substrate. The virgin oxides on the n-type substrate were grown to a thickness of 1.2μ, the first 0.3μ being grown in steam and the remainder in dry O_2 (in accordance with the particular process specifications under study). The defect density was measured on the initial oxide and after successive removal of approximately 0.2μ layers by etching in a buffered HF solution. The defect density in the oxide layer, as a function of oxide thickness for wafers treated in this manner, was obtained. Figure 5 is the result obtained on a single wafer in an initial test of the technique while Figure 6 represents measurements on two wafers oxidized together and lightly pattern-etched, followed by etching and probing in the same manner. The effect of partial regrowth of oxide on wafer 2 is also shown in Figure 6. Both figures show a rapid increase in the number of defects as the oxide thickness is reduced by etching.

The oxides over the p-doped regions were grown at temperatures of 1050C and 1100C in dry O_2. At 1050C, layers of 850, 1300, 1600, and 3000 Å were obtained, and at 1100C layers of 1100, 1500, 2000, and 3500 Å were obtained. The oxides were probed after growth, and the defect density in these oxide layers for the two different growth temperatures are shown in Figure 7. Most of the defects observed in the oxides over 1300 Å thick were concentrated near the edges of the wafer so that the central regions of the wafers were quite free from defects.

Comparison of Figures 5, 6, and 7 indicates that oxides grown up to a specified thickness have substantially fewer defects than those grown to greater thicknesses and etched back to the specified thickness. This is in agreement with the findings of a previous internal oxide

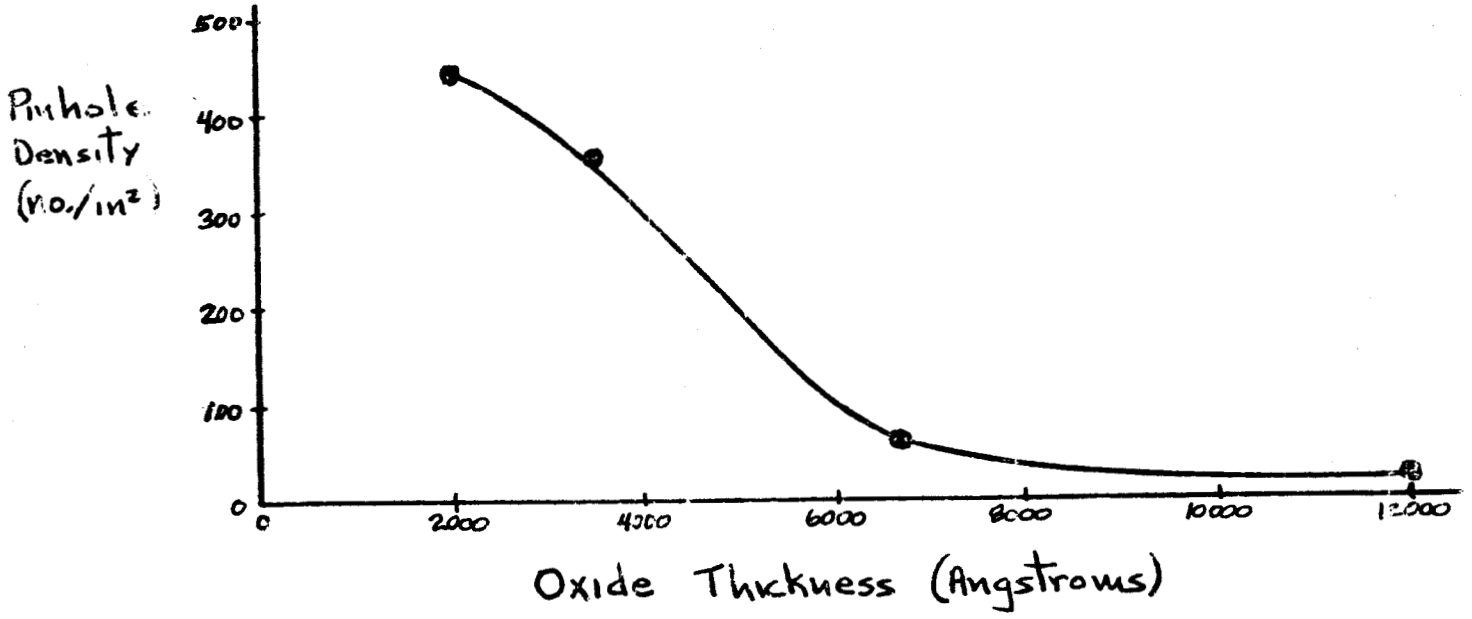


Figure 5. Etch Back Of Initial Oxide

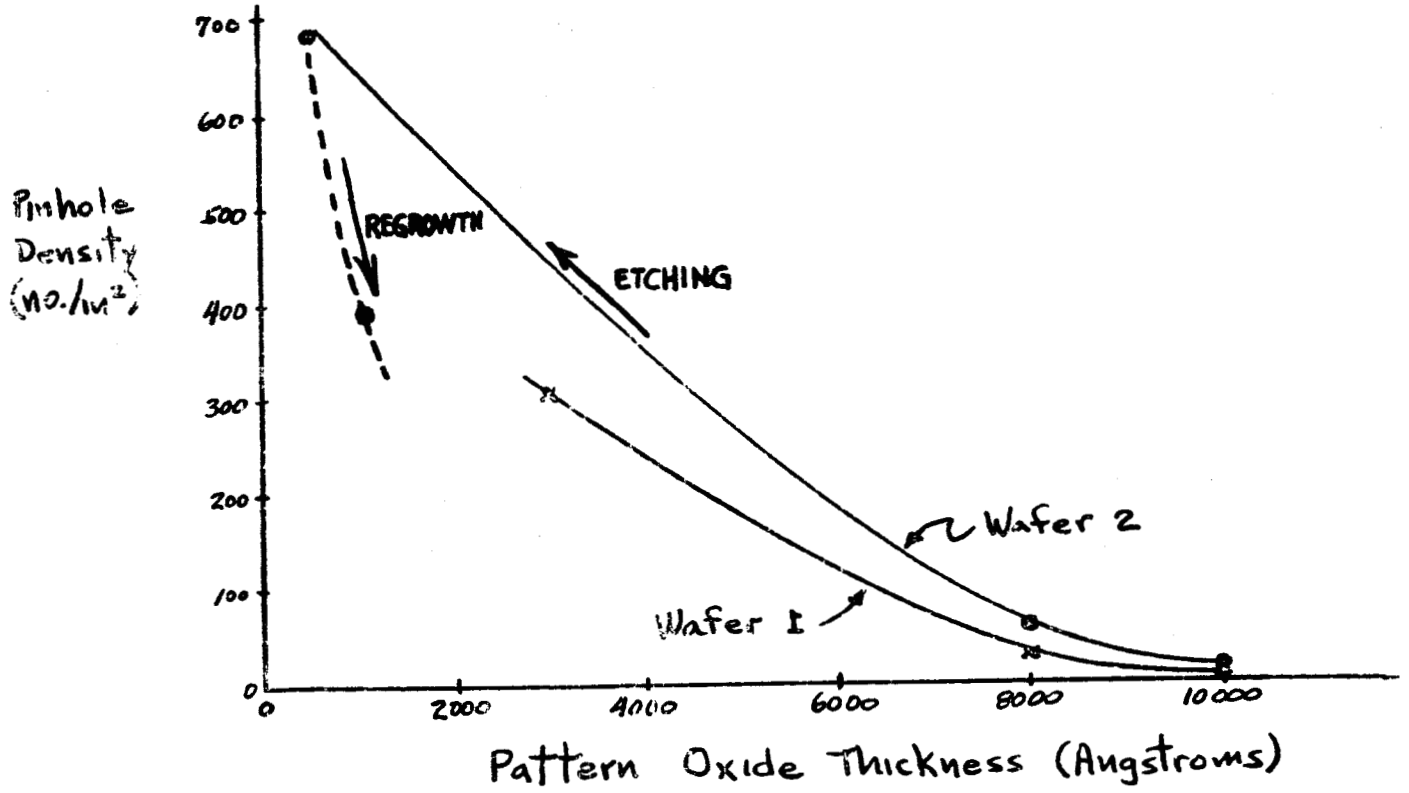


Figure 6. Etch Back On Two Wafers

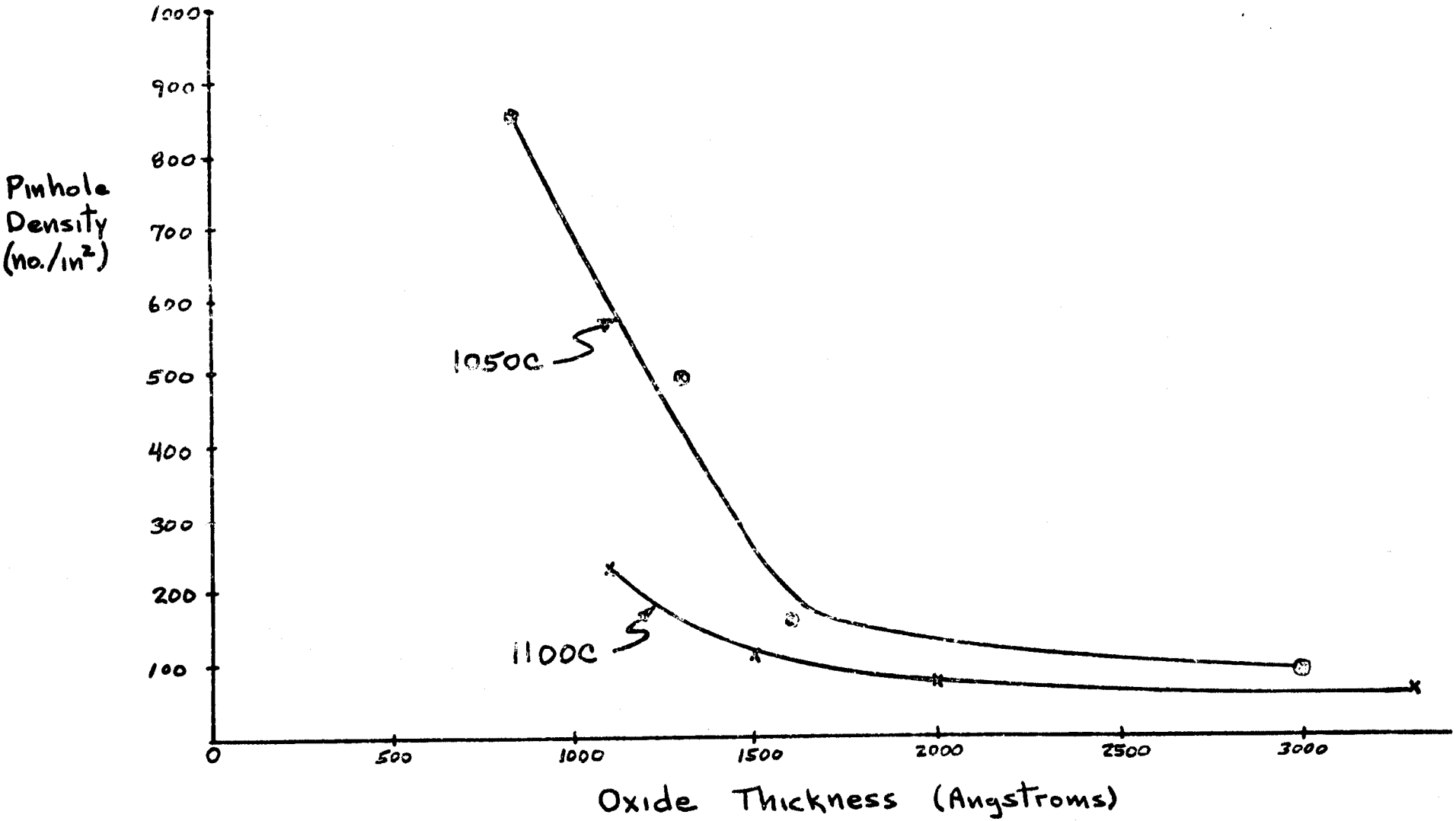


Figure 7. Eight Unetched Wafers

evaluation program at Autonetics[16] and recent work at Bell Labs[17]. Caution should be exercised, however, in drawing conclusions from these preliminary results since the oxides in one case were grown over high resistivity n-material, and in the other were grown over highly doped p-regions where the growth rate is more rapid.

Since etch-thinning of oxide layers is important to some MOS device fabrication procedures, it appeared desirable to learn whether dielectric defects in such layers could be repaired by a brief reoxidation step. A regrowth experiment was performed on wafer No. 2 (Figure 6) which increased the thickness to 1200 Å (from 500 Å) and decreased the defect density to 390 in^{-2}. This density is considerably below the etch-back defect density curve shown for this wafer but is still not acceptable for device use. The improvement introduced by this step therefore appears to be useful only when the initial defect density is low.

Additional confirmation of this effect was obtained on a wafer containing 36 MOS circuits employing about 800 gates each. All of the circuits were electrical short failures. Regrowth of approximately 500 Å additional oxide on the wafer yielded the defect distribution given in Table IV.

Table IV. Defect Distribution in Regrown Oxide on an MOS Device Wafer

Region	Approximate Oxide Thickness (Å)	Number of Defects	Approximate Effective Device Area (%)
Gate Regions	2000	31	5
Diffused Regions	2000	350	45
Remaining Initial Oxide	12,000	10	50

The evidence indicates defect densities are approximately the same in both the diffused and gate regions, and considerably greater than in the thick oxide regions. A significant proportion (about 30%) of the defects were observed at steps in the oxide profile, suggesting a structural damage contribution due to mechanical stress relief in the oxide at these locations. Other remedial procedures are being sought.

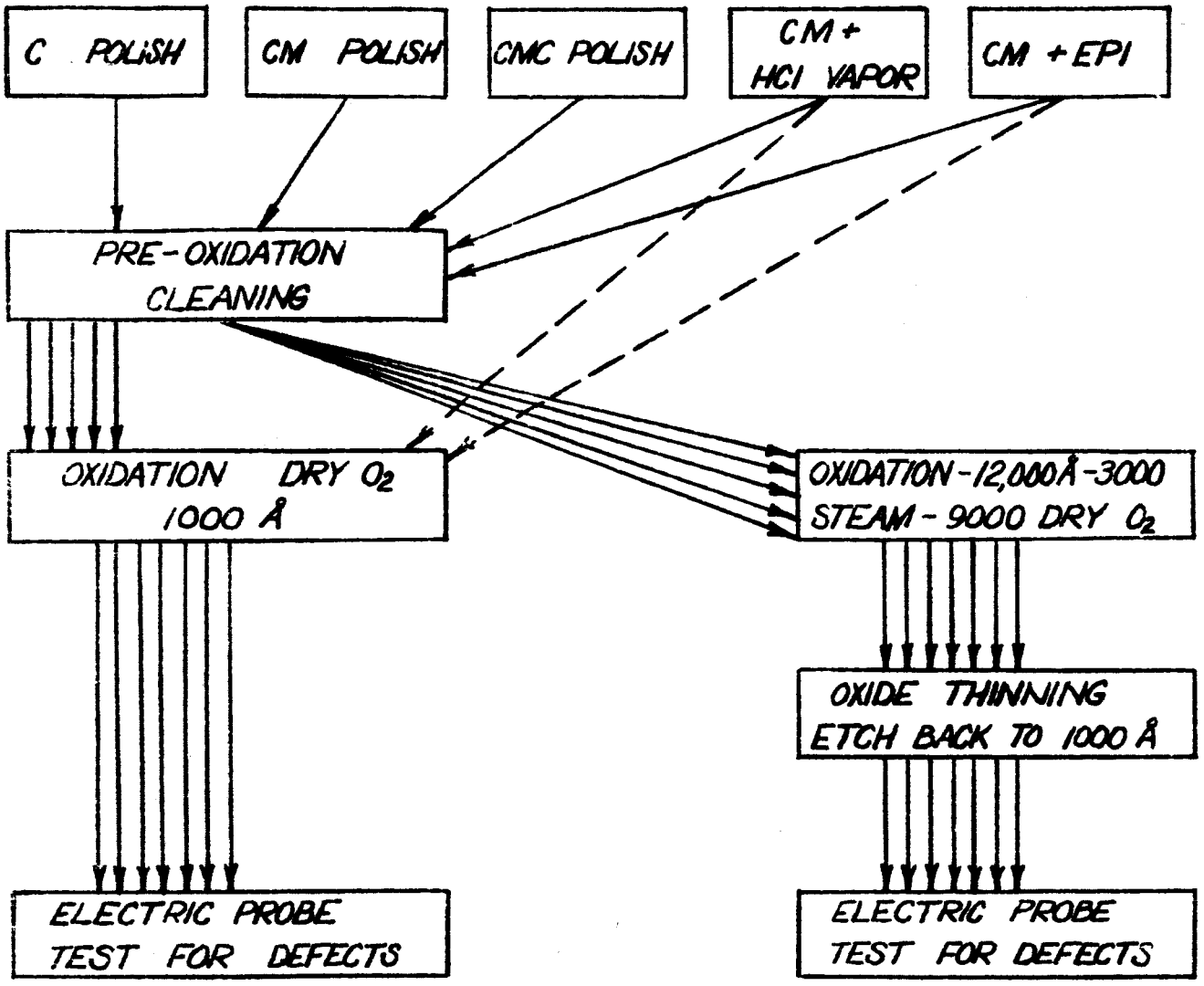
The investigation of the effects of process variables on the occurrence of dielectric defects is being directed initially toward silicon wafer surface preparations, and a comparison of the relative effects of etch back and regrowth techniques. A flow chart for this investigation is presented in Figure 8.

D. Incidence of Dielectric Defects: Contaminant Contributions

One possible source of oxide defects or pinholes is particulate contamination on the silicon wafer before oxidation or during diffusion and re-oxidation steps. An experiment to test this hypothesis was devised in which silicon wafers would be deliberately contaminated prior to oxidation. Two methods of contamination were attempted: (1) exposure to room ambient dust for various periods and (2) evaporation of suspensions of 0.3μ alumina in water containing varying numbers of particles per unit volume.

For Method (1), exposures to room air for 10 minutes, 100 minutes, and 1000 minutes were used. Method (2) employed suspensions containing 400, 4000, and 40,000 particles/ml. One ml of each was evaporated on wafers at approximately 4 cm^2 area to give 100, 1000, and 10,000 particles/cm^2. One wafer was prepared with one ml of deionized water evaporated on it. The evaporation of suspended particles proved to be unsatisfactory because the silicon is hydrophobic, and the resulting evaporation produced a nonuniform distribution of particles (spotting and streaking). When oxidized, many oxide defects were visible along these stain lines which, of course, contained a far greater concentration of particles than was intended.

The defect count on the air exposed wafers gave counts of 20, 20, and 28 defects/cm^2 for the 10, 100, and 1000 minute exposure, respectively. A control wafer that had been cleaned in deionized water, drained, and dried with warm air gave a count of 20 defects/cm^2. A dust count for 1000 minutes in the room during a similar period gave a particle count of 300-400/cm^2 which is fairly low for such an area. Thus, it is apparent that the contamination caused by room exposure is barely sufficient to produce an oxide imperfection level above that intrinsic to this oxidation process.



LEGEND:

C - CHEMICAL POLISH
CM - CHEMICAL + MECHANICAL POLISH
CMC - CHEMICAL + MECHANICAL + CHEMICAL POLISH
CM+HCl - CM FOLLOWED BY HCl VAPOR POLISH
CM+EPI - CM FOLLOWED BY EPITAXIAL DEPOSITION

FIG. 8 DIELECTRIC DEFECTS vs. PROCESS TECHNIQUES TEST SCHEDULE

A wafer passivation experiment using contaminated water (tap water) has been carried out with the expectation that spray carry-over would introduce particulate contamination (alkali and alkaline earth salts) into the growing oxide. Electric probe data have not yet been obtained on these specimens.

PROPOSED PLAN FOR FOLLOWING QUARTER

Gas ambient effects on the function of planar silicon devices and integrated circuits will be continued with emphasis on condensable polar molecules (e.g., H_2O, CO_2).

Investigation of silicon imperfections and tool damage by the Schwuttke modification[18] of the Lang x-ray method and by etching techniques will be continued.

Previously prepared tritiated wafers will be beta assayed, metallized, and examined for tritium electromigration under stress conditions that normally produce inversion in planar devices.

Particle localization of sodium in oxide layers will be sought by neutron activation and correlation of dielectric defect densities with extracted (etched) Na^{24} activities.

Inversion recovery kinetics of deuterated devices will be investigated in greater detail.

Investigation of process contributions to dielectric defects in oxide layers will proceed according to the schedule given in Figure 8. Study of the effects of deliberate contamination also will be continued.

COMPLETION INFORMATION

Approximate physical completion:	65%
Approximate expenditures:	63%

ACTION REQUIRED BY NASA

None

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REFERENCES

(1) G. L. Allerton and J. R. Seifert, Western Electric Engineer, 5, 43, July 1961.

(2) T. G. R. Rawlins, J. Electrochem. Soc., 111, 810 (1964).

(3) J. R. Biard and S. B. Watelski, J. Electrochem. Soc., 109, 705 (1962).

(4) Scientific Research, 1, No. 1, p. 3 (1966).

(5) J. W. Faust in the 4th Annual Symposium on the Physics of Failure in Electronics, Chicago, 1965.

(6) Consolidated Quarterly Progress Report No. 15, ERL, University of California, Berkeley, p. VI-6.

(7) Scientific Research, 1, No. 1, p. 5 (1966).

(8) GCA Corp., Bedford, Mass., Product Data Sheet No. 113B.

(9) Chemical and Engineering News, January 31, 1966, p. 31.

(10) V. E. Cosslett, Reports on Progress in Physics, XVIII, p. 385 (1965).

(11) D. W. Howarth in the 4th Annual Symposium on the Physics of Failure in Electronics, Chicago, 1965.

(12) W. Schroen and W. W. Hooper, Failure Mechanisms in Silicon Semiconductors, pp. 129-142, AD 615312.

(13) Chemical and Engineering News, January 10, 1966, p. 35.

(14) P. D. Davidse and L. I. Maissel, 3rd Int. Vacuum Congress, Stuttgart, 1965; Circuits Manufacturing, Sept.-Oct. 1965, p. 14; J. D. Hall, Research and Development, October 1965, p. 116.

(15) Proceedings of the Second Physics of Failure Colloquium, Autonetics, June 4, 1965; J. E. Forrester, R. E. Harris, J. E. Meinhard, and R. L. Nolder, "Imperfections and Impurities in Silicon Associated with Device Failure Mechanisms," Physics of Failure in Electronics, 4th Annual Symposium, Chicago, November 1965.

(16) Autonetics Internal Report T5-2257/3111, December 8, 1965.

(17) A. D. Lopez, J. Electrochem. Soc., 113, 89 (1966)

(18) AD 608335, AFCRL-64-542, TR 64-302.15, G. H. Schwuttke, "X-ray Diffraction Microscopy of Imperfections in Semiconductor Crystals."