INTERIM REPORT

FOR

SRD FREQUENCY MULTIPLIERS

CONTRACT NO. NAS 8 20257

RYAN

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CONTENTS

LIST OF ILLUSTRATIONS

1.0 INTRODUCTION

Ryan Electronic and Space Systems, a facility of the Ryan Aeronautical Co., is presently investigating the applications of Step Recovery Diodes (SRD's). The program is supported by the Marshall Space Flight Center, Huntsville, Alabama under Contract NAS 8-20257. The contract has recently been amended to include the study of other circuits utilizing the SRD. Since the contract extension will postpone the issuance of a final report for approximately one year, this interim report is submitted to summarize the work done to date on step recovery diode frequency multipliers.

1.1 PROGRAM OBJECTIVES

The principal objective of the initial phase of the investigation was the development of the necessary circuitry to use the fast current switching capabilities of step recovery diodes for frequency multiplication. Particular interest lay in multiplying in one stage from the VHF band (100 to 200 mc) to S-band (2200 mc) with ultimate application in the area of space communication. Areas of specific task assignment were:

a. Study of the problems of using more than one diode in parallel or push-pull to increase power handling capability.

b. Study of the problems of matching the widely varying input impedance of the multiplier to a fixed impedance of the driving source.

c. Measurement of the effects of temperature and the development of a temperature compensating circuits.

d. Measurement of phase modulation characteristics.

e. Measurement of AM noise characteristics.

f. Development of an S-band prototype multiplier.

Overriding all of the above tasks was the need to develop a theory of operation for the SRD frequency multiplier. The existence of such a theory would make possible the systematic design of circuits having specific characteristics and making the best use of commercially available step recovery diodes.

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1.2 HISTORY OF PROGRAM

Ryan had been active in the study and application of SRD's for approximately one year prior to the start of Contract NAS 8-20257. During this time, a number of X-band frequency multipliers had been built and a start made on understanding the operation of the several types of circuits. It was apparent very early that the conventional analysis, which had evolved for design of varactor frequency multipliers, was not adequate when applied to the SRD. Varactor theory could not account for the high efficiencies which were attainable without the use of idler circuits.

A most useful experimental tool in the study of SRD frequency multipliers is the low frequency model. This is nothing more than a scaled up model of the circuit under study. By operating in the frequency range from 20 to 500 mc, the circuit geometry is large enough so that the circuit can be instrumented by sampling probes and the various events taking place can be observed on a high speed oscilloscope. A typical low frequency model is shown in Figure 1.

Prior to starting the work on Contract NAS 8-20257, Ryan used the low frequency modeling techniques to study the so-called series type of SRD frequency multiplier and had developed a working theory of its operation.

Work on the contract was started in August 1965, and the first task was to extend the series circuit to push-pull multipliers using multiple diodes.

Concurrently, a study of the second class of multipliers, the shunt type, was undertaken. This work proved very fruitful and led eventually to a mathematical analysis of the shunt multiplier.

Because the step recovery diode is both time-wise and piece-wise nonlinear, designing the input matching network has been larger an empirical process. Since early multipliers demonstrated severe hysteresis problems, a mathematical and experimental study of the input matching problem was then carried out.

In order to obtain cross correlation between the low frequency model work and a microwave multiplier, a series of S-band (220 mc to 2200 mc) units were built and tested. These models provided data on phase modulation characteristics, temperature effects, and also provided a vehicle for evaluating various types of diodes.

In addition to the S-band multipliers, it was necessary to build one X-band multiplier to take advantage of available AM noise measuring equipment. These tests have not been completed and therefore will not be reported here.

1.3 OUTLINE OF REPORT

This report will not follow the chronological sequence of the program. Because the shunt type of circuit is more easily described, and because its mathematical analysis has been carried further, that circuit is considered first. Later paragraphs will describe this circuit and its operation, develop the analysis using the intermediate step of the SRD impulse generator, and finally present experimental data.

Next, the report will discuss the series type of SRD multiplier circuit. The series circuit has a major advantage over the shunt type in that it is mechanically more simple. This fact becomes increasingly important as the output frequency is pushed up to X-band and beyond. The operation of the series circuit is understood in a qualitative sense, but a complete mathematical analysis has been frustrated by the arithmetic complexity. Ryan is currently attempting to devise a computer analysis which will relieve this situation. However, many of the results of the analysis of the shunt circuit can be applied to the series circuit, even though there is not a physical one-to-one correspondence.

Having discussed the frequency multiplier itself, the report will then discuss the problem of devising an input matching network.

Finally, the results of phase modulation tests factors affecting efficiency, effects of temperature, and the problems and potentialities of multiple diode circuits are considered.

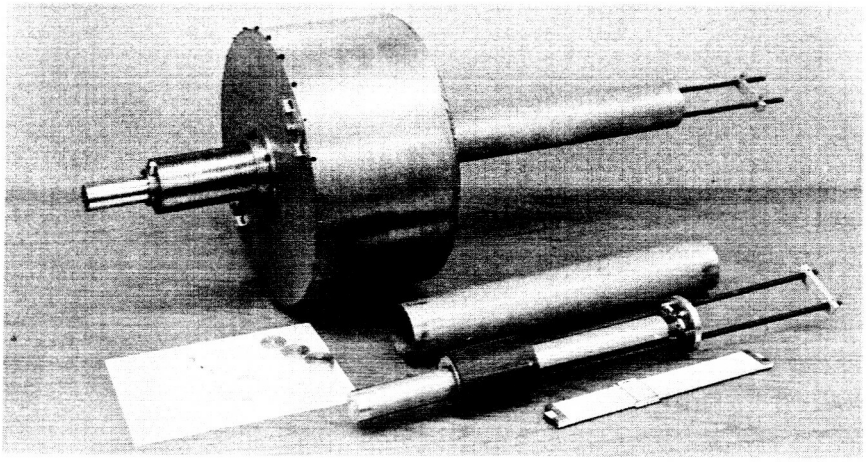

Figure 1 SRD Frequency Multiplier

2.0 SHUNT SRD FREQUENCY MULTIPLIERS

2.1 STEP RECOVERY DIODE CHARACTERISTICS

Before considering frequency multiplier circuits, the properties of step recovery diodes will be reviewed. There are perhaps three separate mechanisms by which a semiconductor diode can produce frequency multiplication. These are the non-linear capacitance of the junction when back-biased, the non-linear capacitance due to charge storage when forward biased, and the current step during transition from forward to reverse bias. The first and second are the mechanisms utilized in the varactor mutiplier. The third is the dominating mechanism in the high order SRD frequency multiplier. The stipulation of a high order multiplier is important because at multiplication factors of five and below the variable capacitance due to charge storage very probably effects the operation of the SRD multiplier. This report will consider only the high order SRD multiplier wherein the diode functions as a switch.

If voltage is applied to a semiconductor diode in the forward direction, charge in the form of minority carriers is stored in the region of the junction. In this condition, the diode has low impedance, ideally a fraction of an ohm. If the voltage is suddenly reversed, the diode will continue to conduct while the stored change is being swept out. When the charge is depleted, the diode suddenly becomes high impedance. An SRD is simply a diode whose parameters have been optimized to make the transaction form stored charge conduction to zero current take place very rapidly, typically in a few hundred picoseconds.

Basically, the SRD acts as a very fast switch. However, the switching speed is not zero and the finite time required to interrupt must be considered in the design of high frequency multiplier. There are several other characteristics of SRD, which must also be considered. First of these is the junction capacitance. In the non-conducting state, the SRD, rather than being a perfect open circuit, appears as a small capacitance. Diode manufacturers have reduced this capacitance to a few picofarads or less, but this parameter is the second factor which determines the maximum output frequency of an SRD multiplier.

A third limiting parameter is the finite resistance of the diode. The driving current passing through this resistance results in a power loss, which reduces efficiency and generates heat which must be removed from the circuit. Diode resistance is also a parameter which diode manufactures try to reduce to a minimum.

Finally, a portion of the stored charge is lost by recombination. This results in a dc current flowing in the circuit and also represents a power loss, since the amount of charge lost is proportional to the time the charge is stored. The recombination rate sets a lower limit on the frequency at which the multiplier can be driven. Recombination rate is usually specified by the inverse parameter, i.e., carrier life time.

The ideal step recovery diode would have minimum transition time, minimum junction capacitance, minimum series resistance, maximum lifetime, and maximum heat dissipation. Unfortunately, these characteristics are never available in a single SRD.

2.2 DESCRIPTION OF SHUNT SRD MULTIPLIER

Figure 2 is a schematic diagram of the shunt-type SRD frequency multiplier. The circuit is driven at a frequency, f_1. The limitations placed upon f_1 will be discussed in a later section of this memorandum. However, f_1 typically will be in the range from 50 to 1000 mc. In general, an impedance matching network will be required at the input.

The input signal alternately drives the SRD into forward and reverse conduction. During each negative half cycle, the diode "snaps", i.e., the diode transfers suddenly to the high impedance condition, as the charge stored during the positive half cycle is depleted. The time of the occurrence of the snap can be varied by adding dc bias to the driving signal.

When the SRD snaps, it interrupts the current flowing in the section of transmission line labeled Pulse Line (Figure 2). This creates a voltage pulse at point A of magnitude:

$$V_p = I_o Z_o \qquad (1)$$

and duration:

$$\tau = 2\frac{\ell}{v} \qquad (2)$$

Where:

Z_o is the characteristic impedance of the line

I_o the interrupted current

ℓ the length of the line

v the velocity of propagation in the line.

The choke is usually a quarter-wave section of low impedance line and appears as a short to the pulse, but as a shunt capacitance to the driving signal.

The frequency multiplier is completed by coupling a high-Q resonator to the pulse line. The resonator is tuned to a multiple of the input frequency and receives an impulse for each cycle of the driving signal. It acts as a flywheel supplying energy to the output load between impulses. It appears that best efficiency would be obtained if the length of the pulse line were adjusted to give a pulse length equal to one-half cycle of the output frequency.

Frequency multiplication as high as 30 is practical. The upper limit of output frequency is set by the characteristics of the diodes themselves. The lower limit upon drive frequency is set by the lifetime of the minority carriers. As the lifetime becomes an appreciable part of the period of the driving signal, more and more of the stored charges will be lost, due to recombination. The upper limit on output frequency is set by two factors. These are the transition or snap time of the diode, and the RC time constant formed by the impedance of the pulse line and the junction capacitance of the diode. Both of these factors tend to round off the pulse and degrade the efficiency.

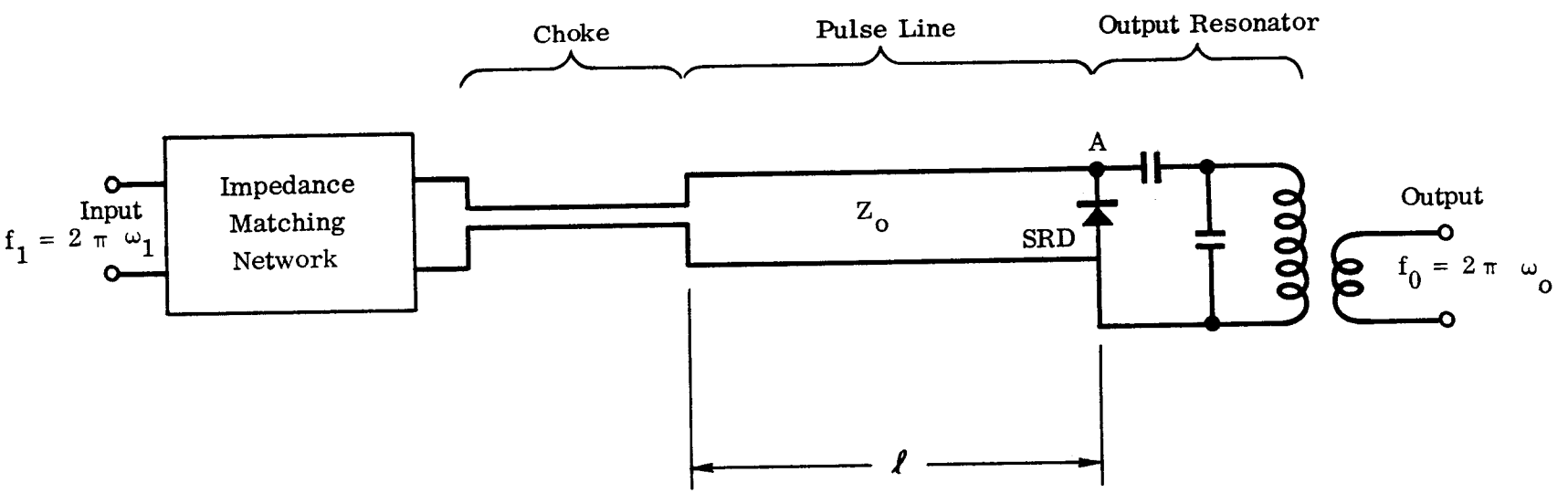

Figure 2 Schematic Diagram of Shunt SRD Multiplier

2.3 ANALYSIS OF SHUNT MULTIPLIER

The method of analysis to be followed in the succeeding sections of this report is very similar to that used by S. M. Krakauer of HP Associates*, which, in turn, follows the traditional analysis of radar pulse modulator.

First, consider the pulse line, assuming that the SRD is a perfect switch and that the load is a pure resistance. The effect of finite diode capacitance will be discussed.

The input impedance at the choke as seen by the driving signal will be derived. From this, a power output versus power input relationship will be determined.

Since this portion of the multiplier is an impulse generator, which is an interesting and useful circuit in itself, a model was built and tested. Experimental results are in good agreement with theory.

The analysis will then be extended to the frequency multiplier by replacing the resistive load with a resonant tank. This analysis results in a somewhat idealized picture, since all losses are not considered.

The next step then is to perturb the idealized solution by adding the losses due to the diode series resistance, the losses in the circuit, and the effects of recombination current due to a finite minority carrier lifetime.

Finally, having derived an input impedance to the multiplier, the restrictions placed upon the input matching circuit can be determined.

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*Bimonthly Report No. 5, Contract DA 59-186-AMC-98 (D) for United States Army Material Command

2.3.1 Analysis of Impulse Generator

2.3.1.1 Pulse Line

Consider the circuit shown in Figure 3. It consists of length, ℓ, of transmission line of impedance Z_o. The line is shorted at one end and shunted at the other by an SRD, which is represented as a switch in parallel with a capacitance, C_j, and a resistive load, R_L. Assume as the initial condition that the switch is closed, and a current, I_o, is flowing in the line as shown. The voltage and current distribution in the line is shown in Figure 3b.

When the switch opens, the current at point A drops to a value given by:

$$I = I_o \frac{Z_o}{Z_o + R_L} \tag{3}$$

and a voltage appears at A given by:

$$V = \left(I_o - I_o \frac{Z_o}{Z_o + R_L} \right) Z_o = I_o \left(\frac{R_L Z_o}{Z_o + R_L} \right) \tag{4}$$

If the shunt capacitance C_j were zero, the voltage would rise to the above value instantaneously. The presence of the capacitance slows the rise time with an RC time constant equal to:

$$T = \frac{Z_o R_c}{Z_o + R_L} C_j \tag{5}$$

In the following discussion, assume the aforementioned time constant as small. Actually in the case of microwave frequency multipliers, the existence of a finite pulse rise time is one of the factors which limits the upper frequency of operation.

After the switch opens, the voltage and current steps propagate down the transmission line; are reflected by the shorted end, and return to the load end. Figures 3c through 3e show the voltage and current distribution at various times after the switch opens.

Assume that the switch closes when the voltage step reaches the right end of the line. Note in the example shown in Figure 3, the SRD (represented by the switch) would indeed become conducting at time, $t = 2\ell/v$, if R_L is greater than Z_o, since the current through it would then be in the forward direction.

Several consequences of the sequence shown in Figure 3 can be listed:

1. A voltage pulse of magnitude

$$V_p = I_o \left(\frac{R_L Z_o}{Z_o + R_L} \right) \tag{6}$$

and duration

$$\tau = \frac{2\ell}{v} \tag{7}$$

has been applied to the load resistor, R_L.

2. The current in the line, which was I_o before the operation, is equal to

$$I_1 = I_o - 2 \left[I_o - I_o \left(\frac{Z_o}{R_L + Z_o} \right) \right] \tag{8}$$

$$I_1 = I_o \left(\frac{Z_o - R_L}{Z_o + R_L} \right) \tag{9}$$

3. The effect of the capacitance, C_j, is to round the leading and trailing edges of the voltage pulse.

2.3.1.2 Pulse Line and Driving Circuit

The previous discussion considered the pulse line without indicating how the initial current I_o was created. Next, consider the circuit shown in Figure 4. The short at the left end of the pulse line is replaced by a choke which appears as a short to the pulse.

Let the circuit be driven by both dc voltage, V, and a sinusoidal voltage, $E \sin(\omega_1 t + \Theta)$. Of interest is only the case where the period of the

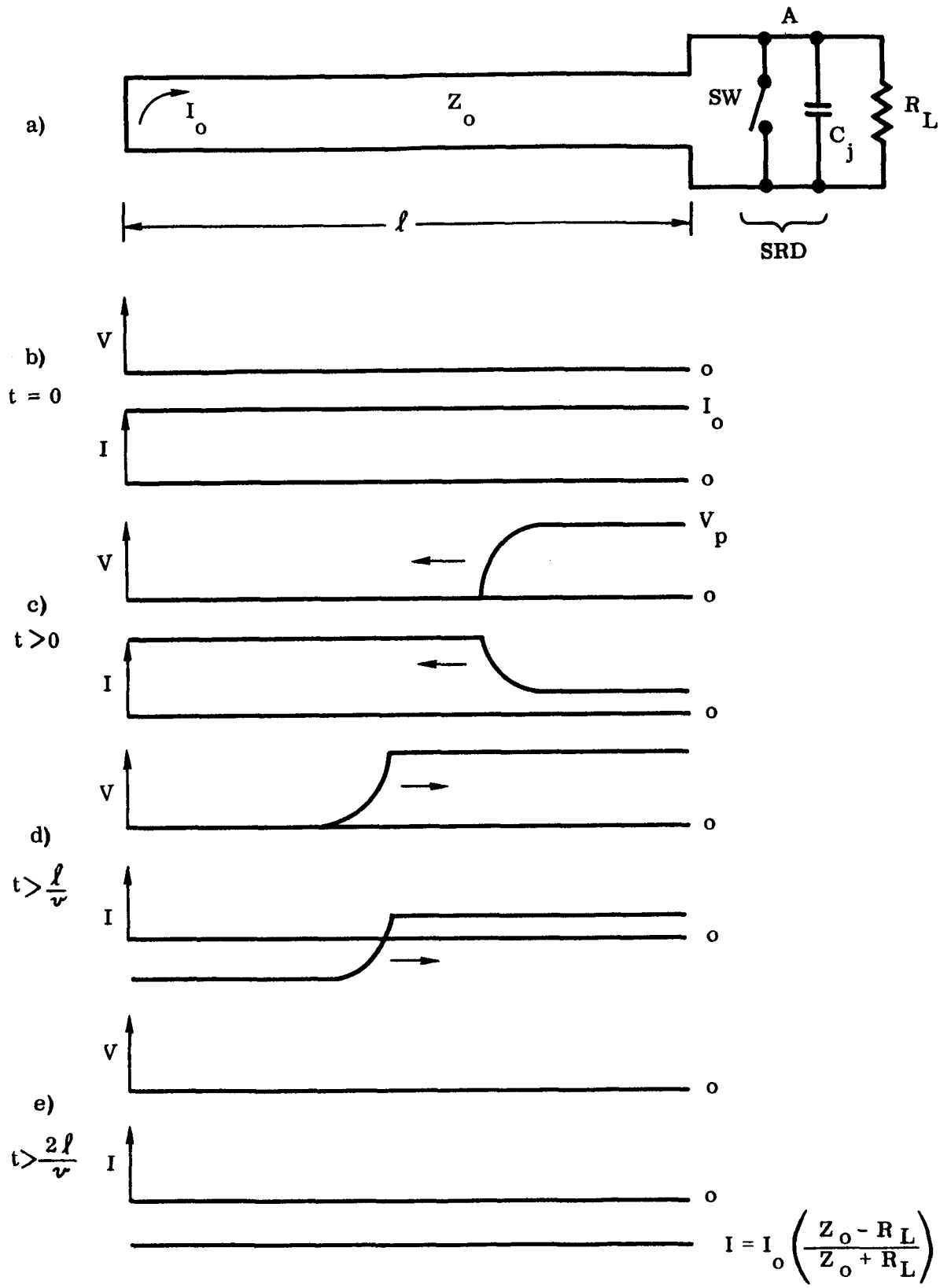


Figure 3 Schematic Diagram Pulse Line

driving signal is very much longer than duration of the output pulse. With this restriction, the choke appears as a capacitance C_c, and the pulse line itself as an inductance L, to the driving signal. The inductance can be related to pulse line impedance and length as:

$$L = Z_o \ell \sqrt{\mu\epsilon} = Z_o \frac{\ell}{v} = Z_o \frac{\tau}{2} \tag{10}$$

Where μ and ϵ are the permeability and dielectric constant of the dielectric of the pulse line.

Consider the current flowing into the pulse line, (thereby excluding the current into capacitance, C_c, which will be added later) and determine the conditions which must be met to have the diode snap once, and only once, per cycle at the driving signal. Take as t = o the time when the diode starts to conduct. Then:

$$E \sin(\omega_1 t + \Theta) + V = L\frac{di}{dt} \tag{11}$$

$$i = \frac{V}{L} t + D - \frac{E}{\omega_1 L} \cos(\omega_1 t + \Theta) \tag{12}$$

At t = 0

$$i = I_1 = I_o \frac{Z_o - R_L}{Z_o + R_L} \tag{13}$$

Therefore, the constant of integration, D, can be evaluated:

$$D = I_o \frac{Z_o - R_L}{Z_o + R_L} + \frac{E}{\omega_1 L} \cos\Theta \tag{14}$$

and the instantaneous current becomes:

$$i = \frac{V}{L} t + I_o \left[\frac{Z_o - R_L}{Z_o + R_L}\right] + \frac{E}{\omega_1 L} \cos\Theta - \frac{E}{\omega_1 L} \cos(\omega_1 t + \Theta) \tag{15}$$

At $t = \frac{2\pi}{\omega_1} - \tau$, that is, just before the diode snaps again, the current equals I_o, making the approximation that $\tau \ll \frac{2\pi}{\omega_1}$, then:

$$i = I_o = 2\pi \frac{V}{\omega_1 L} \left[\frac{Z_o + R_L}{2 R_L} \right] \tag{16}$$

A second condition must be met if the SRD is to snap once, and only once, per cycle. The charge stored during forward current must be depleted during reverse current. Assuming the minority lifetime is long compared to the time of one cycle, we can write:

$$\int_0^{\frac{2\pi}{\omega_1}} i \, dt = 0 \tag{17}$$

Substituting Eq. (15) and performing the integration:

$$\frac{V}{2L} \left[\frac{2\pi}{\omega_1} \right] + I_o \left[\frac{Z_o - R_L}{Z_o + R_L} \right] + \frac{E}{\omega_1 L} \cos \Theta = 0 \tag{18}$$

Substituting for I_o, we obtain a relationship between E, cos Θ, and V which must be satisfied, that is:

$$E \cos \Theta = - \frac{\pi V Z_o}{R_L} \tag{19}$$

If:

$$|E| > \frac{\pi V Z_o}{R_L}, \tag{20}$$

the conditions for one snap per cycle are met. As E is increased beyond the critical value, Θ varies to satisfy the relationship of equation (19).

Several rather unexpected conclusions can be drawn from the foregoing analysis. These are:

1. The magnitude of I_o and therefore the magnitude of the output pulse is a function only of the dc bias voltage, and not of the ac driving voltage.

2. The ac driving voltage must be above a threshold value for proper operation. Increasing the drive voltage beyond this point serves only to change the phase relationship between the occurrence of the pulse and the driving signal.

2.3.1.3 Calculation of Input Impedance

Having determined the instantaneous current into the pulse line, we can now determine the impedance which it presents to the driving signal. Substituting the value for E cos Θ from Eq. (19) into Eq. (15), we arrive at an instantaneous current:

$$i = \frac{V}{\omega_1 L}(\omega_1 t - \pi) - \frac{E}{\omega_1 L}\cos(\omega_1 t + \theta) \qquad (21)$$

The average or dc current is zero, since this was one condition for stable operation (see Eq. (17).)

The second term of Eq. (20) is obviously the current due to the driving voltage, E sin ($\omega_1 t + \theta$), through an inductance, L.

The first term of Eq. (21) can be expanded in a Fourier series of ω_1 and the in-phase and quadrature components (relative to the driving voltage, E sin ($\omega_1 t + \theta$) can be calculated to be:

$$i\Big|_{\text{in phase}} = -\frac{2V\cos\theta}{\omega_1 L}\sin(\omega_1 t + \theta) \qquad (22)$$

$$i\Big|_{\text{quadrature}} = \frac{2V\sin\theta}{\omega_1 L}\cos(\omega_1 t + \theta) \qquad (23)$$

Therefore, the input to the pulse line appears as three parallel impedances at the driving frequency. These are:

1. Inductance, $X_L = j\omega_1 L$ (24)

2. Equivalent Resistance:

$$R_\omega = -\frac{\omega_1 L E}{2V \cos\theta} = \frac{E^2}{V^2}\left[\frac{R_L \omega_1 L}{2 \pi Z_o}\right] \tag{25}$$

3. Equivalent Reactance:

$$X_\omega = j\omega_1 L \frac{E}{2V \sin\theta} = j\omega_1 L \frac{E}{2V\sqrt{1 - \frac{V^2}{E^2}\left[\frac{\pi Z_o}{R_L}\right]^2}} \tag{26}$$

To the above must be added the shunt capacitance of the choke, C_c. The complete equivalent input circuit is shown in Figure 5.

Note that with the diode polarity which we have chosen, θ will be equal to π when E is set at its threshold value. At this point:

$$R_\omega = \frac{\pi Z_o \omega_1 L}{2 R_L} \tag{27}$$

$$X_\omega = \infty$$

And, assuming the value of C_c is chosen to tune out L, the input is purely resistive.

2.3.1.4 Input-Output Power Relationship

It is interesting to calculate the overall conversion efficiency using the equivalent impedances developed in the previous section.

The input power drawn from the bias supply is zero since the dc current is zero.

The input power drawn from the driving signal is:

$$P_{in} = \frac{E^2}{2 R_\omega} \tag{28}$$

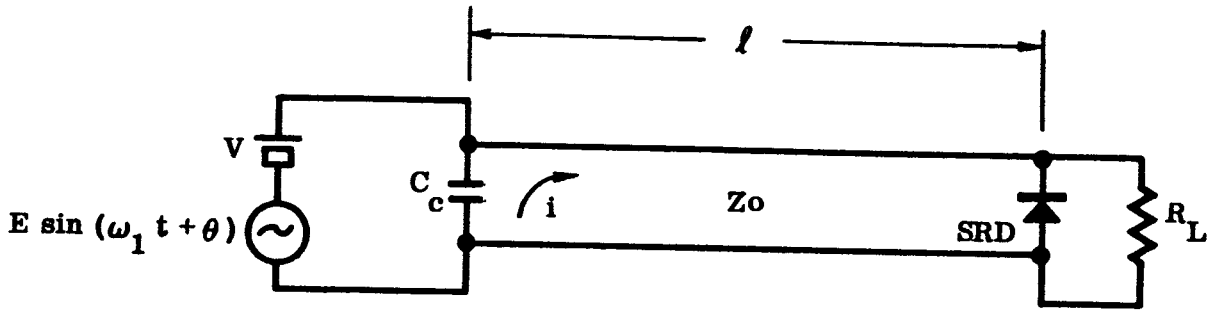
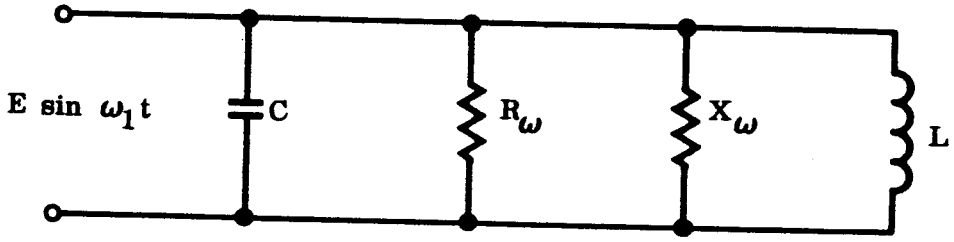


Figure 4 Schematic Diagram SRD Impulse Generator



$$R = \frac{E^2}{V^2} \frac{R_L \omega_1 L}{2 \pi Z_o}$$

$$X_\omega = j \omega_1 L \frac{E}{2V \sqrt{1 - \left(\frac{V}{E}\right)^2 \left(\frac{\pi Z_o}{R_L}\right)^2}}$$

Figure 5 Equivalent Input Circuit of Impulse Generator

The factor of 1/2 must be added, since we have chosen E as a peak voltage:

$$P_{in} = \frac{1}{2} V^2 \frac{2\pi Z_o}{R_L \omega_1 L} \tag{29}$$

setting $L = Z_o \tau/2$ then,

$$P_{in} = V^2 \frac{2\pi}{\omega_1 R_L \tau} \tag{30}$$

The average power output can be calculated from the peak power multiplied by the duty cycle:

$$P_{out} = \frac{V_p^2 \tau}{R_L \left[\frac{2\pi}{\omega_1}\right]} \tag{31}$$

$$P_{out} = I_o^2 \left[\frac{R_L Z_o}{Z_o + R_L}\right]^2 \frac{1}{R_L} \left[\frac{\tau}{\frac{2\pi}{\omega_1}}\right] \tag{32}$$

Substituting Eq. (16), then

$$P_{out} = V^2 \frac{2\pi}{\omega_1 R_L \tau} \tag{33}$$

Thus, the impulse generator is 100 percent efficient, as indeed it should be, since we have not yet postulated any losses.

2.3.1.5 Experimental Data

Before proceeding to the analysis of the SRD frequency multiplier, it would be interesting to compare some actual test data with the results

predicted by theory. An experimental impulse generator was built with the following characteristics:

Input frequency	-	40 mc
Pulse line impedance	-	50 ohms
Pulse line length	-	9.5 in.
Load resistance	-	60 ohms
Choke capacitance	-	230 to 290 pf variable

The calculated pulse length is 1.6 nanoseconds, and this is exactly the measured value.

The curves of Figure 6 summarize the data taken at a fixed bias of 1 volt as the drive voltage was varied from 1.2 to 15 volts. The calculated values are indicated in the figure. It should be remembered that 0.7 volts must be added to the applied bias to account for the contact potential of the diode.

There is excellent agreement between the calculated pulse magnitude and experimental results. The comparison between the theoretical and measured input impedance is not as good, particularly at higher values of drive voltage. This discrepancy probably is due to the fact that the SRD used in the multiplier (hpa 0242) has a minority lifetime of approximately 100-200 nanoseconds, which cannot be considered infinitely larger than the period of the driving signal (25 nanoseconds). Thus, the recombination current is not zero. The power required to cause the recombination current to flow against the bias voltage must come from the driving voltage, and can be represented by a second resistive load in parallel with R_ω. This will be discussed further in Paragraph 2.3.3.5.

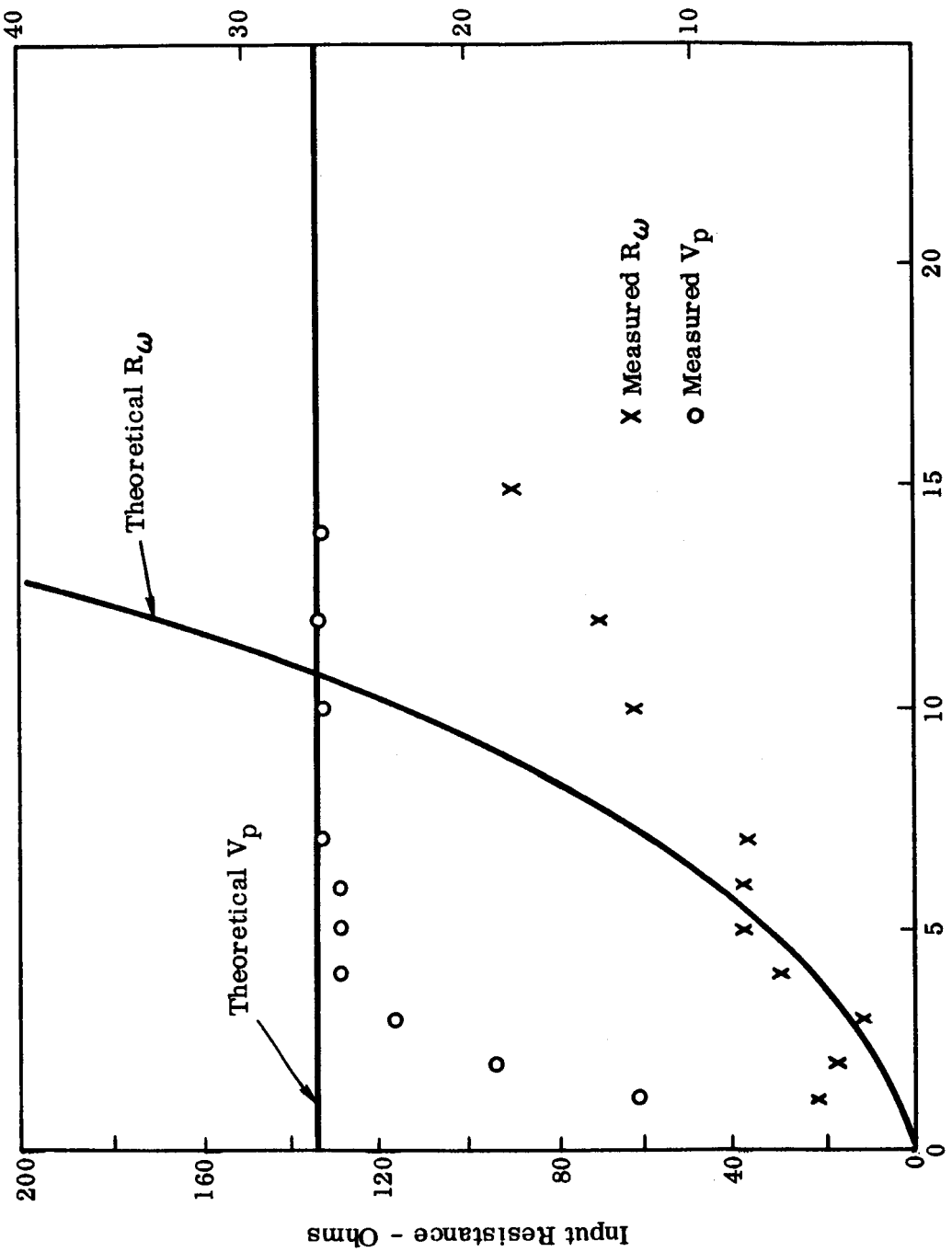


Figure 6 Pulse Amplitude and Input Resistance Versus Drive Voltage

2.3.2 Extension of Theory to Frequency Multiplication

The extension of the theory developed for the impulse generator to the SRD frequency multiplier involves replacing the load resistor, R_L, by a resonant circuit and determining what must be added and how to modify the impulse analysis.

2.3.2.1 Resonant Circuit Model

The first step in the multiplier analysis is to develop a model of the output resonator as it is seen by the pulse line, when the diode is nonconducting during the period immediately after the snap. The model must also be valid for the much longer period between snaps when the diode is conducting, and the resonator is isolated from the pulse line.

A number of different resonant tanks have been utilized for SRD multipliers. The circuit shown in Figure 7a can be used for this analysis with little loss in generality. The assumptions implied in this circuit are:

1. The frequency of the resonant circuit is not appreciably changed by the impedances connected to the input.

2. The losses within the resonator are negligible compared to the external losses and the power delivered to the load.

3. The voltage, e, is sinusoidal with constant amplitude over the period of interest, which is 10 to 20 cycles of ω_o.

These conditions amount to saying that the unloaded Q of the resonator is very high and that the input and output coupling coefficients are small.

The inclusion of the phase angle, γ, is required since we have already taken t = 0 as the time when the diode snaps.

Let $\omega_o = N \omega_1$. (34)

Here, N is an integer and is the multiplication factor of the multiplier.

The circuit of Figure 7a can be modified to Figure 7b without changing its essential characteristics. The resistor R_o now represents the cw power transferred to the load by:

$$P_o = \frac{e^2}{2 R_o} \tag{35}$$

2.3.2.2 Pulse Line Equilibrium Conditions

In the analysis of the impulse generator, we determined that the output waveform was a square pulse of length τ. Let the length of the pulse line be chosen so that:

$$\tau = \frac{\pi}{\omega_o} \tag{36}$$

or, in other words, the pulse line is made a quarter wave length of the output frequency. We shall be interested in the half cycle immediately following the diode snap. During this period, the equivalent circuit of the pulse line and output resonator is as shown in Figure 8. During this time, the pulse line appears as a pure resistance of value Z_o.

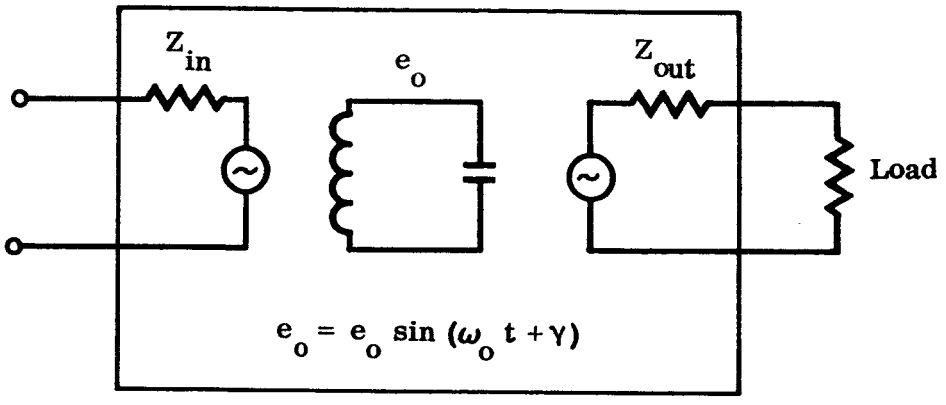
We must now make a limiting assumption that the input impedance of the resonator is also resistive. In all probability, Z_{in} will certainly not be purely resistive to all of the frequency components making up the square pulse and, as will be discussed later, there may be some advantages in making Z_{in} reactive to shape the output of the pulse line. However, in order not to unduly complicate the analysis, let Z_{in} be a pure resistance.

With this restriction, the instantaneous current during the time, t, after the snap is:

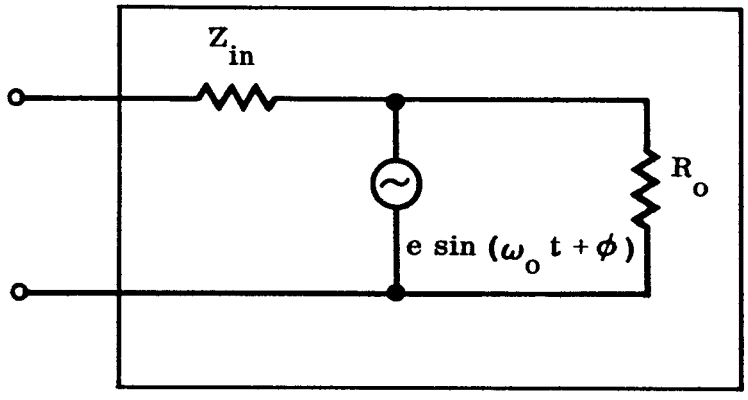
$$i = \frac{I_o Z_o - e \sin(\omega_o t + \phi)}{Z_o + Z_{in}} \tag{37}$$

Where Z_{in} and ϕ are defined in Figure 7b.

In order to find the equilibrium conditions for the pulse line, it is necessary to determine the average current in the line immediately after the SRD resumes conduction. The time which the current flows is just equal



(a)



(b)

Figure 7 Model of Output Circuit

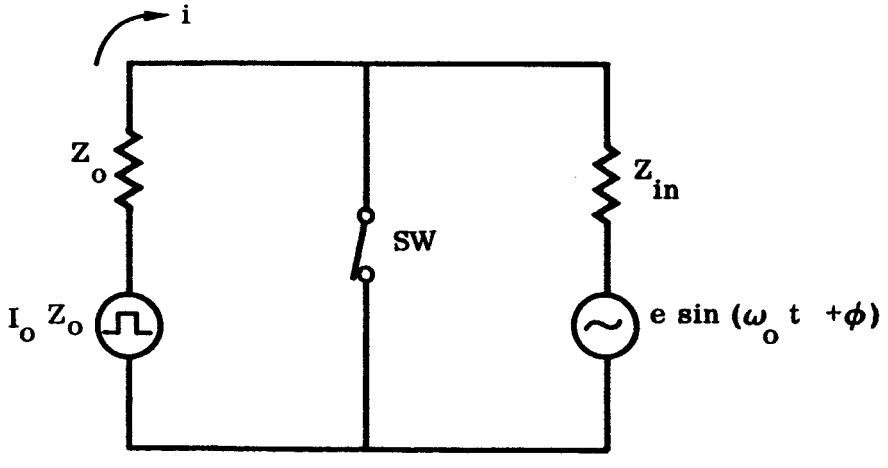


Figure 8 Equivalent Circuit-Pulse Line and Resonator

to the time required for the leading edge to travel down the line, be reflected from the choke, and travel back to the diode. The average current is:

$$i_{ave} = \frac{\omega_o}{\pi} \int_0^{\frac{\pi}{\omega_o}} \frac{I_o Z_o - e \sin(\omega_o t + \phi)}{Z_o + Z_{in}} dt \tag{38}$$

$$i_{ave} = I_o \frac{Z_o}{Z_o + Z_{in}} - \frac{Z e \cos\phi}{\pi(Z_o + Z_{in})} \tag{39}$$

The current in the pulse line after the snap, per Eq. (8), is:

$$I_1 = I_o - 2(I_o - i_{ave}) \tag{40}$$

$$I_1 = \left[\frac{Z_o - Z_{in}}{Z_o + Z_{in}}\right] I_o - \frac{4 e \cos\phi}{\pi(Z_o + Z_{in})} \tag{41}$$

If we let e go to zero, Eq. (41) becomes identical to Eq. (9) with R_L replaced by Z_{in}.

Define an effective load resistance, R_L', in accordance with Eq. (9). Then:

$$R_L' = Z_o \frac{I_o - I_1}{I_o + I_1} \tag{42}$$

$$R_L' = Z_o \frac{I_o Z_{in} + \frac{2 e \cos\phi}{\pi}}{I_o Z_o - \frac{2 e \cos\phi}{\pi}} \tag{43}$$

But from the impulse generator analysis, we found for equilibrium, Eq. (16),

$$I_o = \frac{V\pi}{\omega_1 L}\left[\frac{Z_o + R_L'}{R_L'}\right] \tag{44}$$

Or:

$$R_L' = \frac{Z_o \frac{\pi V}{\omega_1 L}}{I_o - \frac{\pi V}{\omega_1 L}} \tag{45}$$

Substituting Eq. (45) into Eq. (43) we can solve for the equilibrium values of I_o:

$$I_o^2 Z_{in} + I_o \left[\frac{2 e \cos \phi}{\pi} - \frac{\pi V}{\omega_1 L} (Z_o + Z_{in}) \right] = 0 \tag{46}$$

Or:

$$I_o = 0 \tag{47}$$

And

$$I_o = \frac{\pi V}{\omega_1 L} \left[\frac{Z_o + Z_{in}}{Z_o} \right] - \frac{2 e \cos \phi}{\pi Z_{in}} \tag{48}$$

Again, if we let e = 0, we obtain the same equation for I_o as derived for the impulse generator:

Substituting Eq. (48) into Eq. (43) results in:

$$R_L' = Z_{in} \frac{\frac{\pi V}{\omega_1 L}}{\frac{\pi V}{\omega_1 L} - \frac{2 e \cos \phi}{\pi Z_o}} \tag{49}$$

Letting e = 0, we find the effective load resistance is Z_{in} as expected. As e cos ϕ becomes larger, R_L' increases, finally becoming infinite when:

$$e \cos \phi = \frac{\pi^2 V Z_o}{2 \omega_1 L} = \frac{\omega_o}{\omega_1} \pi V \tag{50}$$

At this point, the sinusoidal voltage of the resonant tank is greater than the voltage generated by the pulse line, and no energy can be transferred from the line to the tank.

The input resistance, R_ω, is from Eq. (25),

$$R_\omega = \frac{E^2}{V^2}\left[\frac{\omega_1 L}{2 Z_o}\right] R_L \tag{51}$$

$$R_\omega = \frac{E^2}{V^2}\left[\frac{Z_{in}}{2 Z_o}\right] \frac{\pi V}{\frac{\pi V}{\omega_1 L} - \frac{2 e \cos\phi}{\pi Z_o}} \tag{52}$$

Thus, the impedance presented to the driving source is low at turn-on and and increases as the signal level builds up in the output tank.

2.3.2.3 Input-Output Power Relationship

Consider now the input-output power relationship of the multiplier, assuming a fixed drive voltage E, the bias voltage V, and the signal level $e \cos\phi$. The input power is:

$$P_{in} = \frac{E^2}{2 R_\omega} \tag{53}$$

$$P_{in} = 2\frac{V}{Z_{in}}\left[\left[\frac{\omega_o}{\omega_1}\right] V - \frac{e \cos\phi}{\pi}\right] \tag{54}$$

The power into the resonant tank is

$$P_o = \frac{\omega_1}{2\pi}\int_0^{\frac{\pi}{\omega_o}} i\, e_1\, dt \tag{55}$$

$$= \frac{\omega_1}{2\pi}\int_0^{\frac{\pi}{\omega_o}} (i^2 Z_{in} + e\, i)\, dt \tag{56}$$

Substituting the value of instantaneous current given by Eq. (37) and performing the integration:

$$P_{out} = \left(\frac{\omega_1}{\omega_o}\right) \frac{Z_o}{(Z_o + Z_{in})^2} \left[\frac{Z_o Z_{in}}{2} I^2 + \frac{Z_o - Z_{in}}{\pi} I e \cos\phi - \frac{e^2}{4}\right] \quad (57)$$

Substituting for I_o from Eq. (48):

$$P_{out} = 2 \frac{V}{Z_{in}} \left[\left(\frac{\omega_o}{\omega_1}\right) V - \frac{e \cos\phi}{\pi}\right] + \left(\frac{\omega_1}{\omega_o}\right) \frac{Z_o}{(Z_o + Z_{in})^2} \left[\frac{2 e^2 \cos^2\phi}{\pi^2} - \frac{e^2}{4}\right] \quad (58)$$

$$P_{out} = P_{in} + \left(\frac{\omega_1}{\omega_o}\right) \frac{Z_o}{(Z_o + Z_{in})^2} \left[\frac{2 e^2 \cos^2\phi}{\pi^2} - \frac{e^2}{4}\right] \quad (59)$$

An interesting question is what is the physical significance of the second term of Eq. (59), which is always negative? It appears that it represents a power loss in a system in which no mechanism for power loss has been incorporated.

As mentioned earlier, the spatial distribution of voltage and current in the pulse line is not uniform at the conclusion of the snap. We calculated the average value to determine the equilibrium conditions. However, the energy represented by the ac components will be lost since, after the diode starts to conduct again, these currents will eventually damp out. The energy lost per snap is:

$$E_{ac} = \int_o^e \frac{1}{2} (i_{ac})^2 \mathscr{L} dx + \int_o^e \frac{1}{2} (V_{ac})^2 \mathscr{C} dx \quad (60)$$

Where $\mathscr{L}$ and $\mathscr{C}$ are the inductance and capacitance per unit length of the line. And:

$$i_{ac} = \frac{e}{Z_o + Z_{in}} \left[\sin\left(\frac{\pi X}{2\ell} + \phi\right) + \sin\left(\frac{\pi X}{2\ell} - \phi\right)\right] - \frac{4e}{\pi(Z_o + Z_{in})} \cos\phi \tag{61}$$

$$V_{ac} = e\left(\frac{Z_o}{Z_o + Z_{in}}\right)\left[\sin\left(\frac{\pi X}{2\ell} + \phi\right) - \sin\left(\frac{\pi X}{2\ell} - \phi\right)\right] \tag{62}$$

Or:

$$i_{ac} = \frac{e}{Z_o + Z_{in}} \left[2 \sin\left(\frac{\pi X}{2\ell}\right) - \frac{4}{\pi} \right] \cos\phi \tag{63}$$

$$V_{ac} = 2e\left(\frac{Z_o}{Z_o + Z_{in}}\right) \cos\left(\frac{\pi X}{2\ell}\right) \sin\phi \tag{64}$$

Integrating and noting that for the length of line chosen:

$$\mathscr{C} = \frac{\pi}{2\omega_o \ell Z_o} \tag{65}$$

$$\mathscr{L} = \frac{\pi Z_o}{2\omega_o \ell} \tag{66}$$

$$E_{ac} = \frac{\pi e^2}{2\omega_o} \frac{Z_o}{(Z_o + Z_{in})^2} - \frac{4}{\pi}\left[\frac{e^2 \cos^2\phi}{\omega_o}\right]\frac{Z_o}{(Z_o + Z_{in})^2} \tag{67}$$

The power lost is:

$$P_{ac} = \frac{\omega_1}{2\pi} E_{ac} \tag{68}$$

$$P_{ac} = \left(\frac{\omega_1}{\omega_o}\right) \frac{Z_o}{(Z_o + Z_{in})^2} \left[\frac{e^2}{4} - \frac{2\,e^2 \cos^2 \phi}{\pi^2}\right] \tag{69}$$

Or substituting in (59) we find:

$$P_{out} = P_{in} - P_{ac} \tag{70}$$

While we have not yet incorporated a resistive loss, the analysis shows that some of the input power is converted into a form which is not useful and is thereby lost.

As might be expected, even with our simplifying assumptions, the analysis of the SRD multiplier is somewhat more complicated than that of the impulse generator. It might be well to consider some of the simplifying assumptions and how a more rigorous attack would modify the results.

First, we assumed that the pulse line was a quarter wave long at the output frequency. From the Fourier analysis of a square pulse, one would expect that increasing the pulse length beyond this value would have a detrimental effect on efficiency. Shortening the pulse length would perhaps improve efficiency. It would certainly lessen the dependance of the several performance parameters on the phase angle, ϕ, and reduce the power lost to higher order modes in the pulse line. However, before shortening the pulse line, one must consider the effect of diode capacitance.

In the analysis of the impulse generator, we discussed the effect of diode capacitance and found that the chief result was to round off the output pulse. As the pulse length is shortened, the distortion of the pulse due to diode capacitance will become a more important factor. It then becomes an engineering compromise to consider available diodes, their power handling capability in relation to their capacitance, and to determine the optimum pulse line length and pulse line impedance.

We assumed also that the resonator input impedance, Z_{in}, was resistive. This allowed us to solve for the current after the snap without resorting to a complex Fourier analysis which would have obscured the results of analysis. It should be possible to devise input circuits which incorporate reactive elements, and which are more efficient than the pure resistance just considered. The effect of adding the reactive component would be to shape the pulse applied to the resonator and perhaps, to minimize the energy lost due to ac components left on the pulse line.

Finally, we assumed the frequency and voltage of the tank were both constant. This will not be the case of a practical resonator and the result can generally be predicted to be the degradation of the spectral purity of the output signal.

2.3.2.4 Summary of Lossless Multiplier Analysis

Before going on to consider the various losses and their effect upon multiplier performance, it might be well to recapitulate the results of the analysis of the lossless multipliers:

1. The effective load resistance seen by the pulse line is:

$$R_L' = Z_{in} \frac{\frac{\pi V}{\omega_1 L}}{\frac{\pi V}{\omega_1 L} - \frac{2 e \cos \phi}{\pi Z_o}} \tag{71}$$

Or:

$$R_L = Z_{in} \frac{\left(\frac{\omega_o}{\omega_1}\right) V}{\left(\frac{\omega_o}{\omega_1}\right) V - \frac{e \cos \phi}{\pi}} \tag{72}$$

2. The input impedance presented to the driving signal at ω_1 is:

$$R_\omega = \frac{E^2}{V} \frac{Z_{in}}{4} \frac{\pi}{\left(\frac{\omega_o}{\omega_1}\right) V - \frac{e \cos \phi}{\pi}} \tag{73}$$

3. The input power is:

$$P_{in} = 2 \frac{V}{Z_{in}} \left[\left(\frac{\omega_o}{\omega_1}\right) V - \frac{e \cos \phi}{\pi} \right] \tag{74}$$

4. Even though the multiplier is considered lossless, a portion of the power is lost to higher order modes. This power is:

$$P_{ac} = \left(\frac{\omega_1}{\omega_o}\right) \frac{Z_o}{(Z_o + Z_{in})^2} \left[\frac{e^2}{4} - \frac{2\,e^2 \cos^2 \phi}{\pi^2}\right] \tag{75}$$

5. And the output power is:

$$P_o = P_{in} - P_{ac} \tag{76}$$

2.3.3 Multiplier With Losses

An actual SRD frequency multiplier will inevitably incorporate a number of different mechanisms for power loss which will not only affect its overall efficiency, but will also modify the expressions for impedance, equilibrium condition, etc., developed in the previous section. In this section, we shall consider each loss mechanism separately and determine how the analysis must be modified to account for it. In general, we shall find that we can divide the several losses into two classes; those associated with the resonant tank and those related to the driving current. The effect of the former is to reduce efficiency. The latter not only reduces efficiency but also modifies the input impedance of the multiplier, and thereby complicates the input matching problem.

2.3.3.1 Resonator Losses

Since the output resonator is a linear passive circuit, its losses can be considered by adding a resistance, R_R, in parallel to R_o. Thus:

$$P_r = \frac{e^2}{2\,R_R} \tag{77}$$

Obviously, it is desirable to minimize resonator losses by making the ununloaded Q as high as possible. Note that resonator losses are directly proportional to the power levels in the tank and can be accounted for by calculating or measuring a resonator efficiency factor.

2.3.3.2 Diode RF Losses

In addition to the circuit losses, power will be lost from the output resonator due to the finite resistance of the SRD. Referring to Figure 6, during the time the diode is conducting, the current in the input circuit is:

$$i = \frac{e \sin (\omega_o t + \phi)}{Z_{in} + Z_d} \tag{78}$$

where Z_d is the impedance of the diode.

The power lost is:

$$P_d = \frac{N - 1/2}{N} \frac{e^2}{2 (Z_{in} + Z_d)^2} R_d \tag{79}$$

which, if N is 10 or more and $Z_d << Z_{in}$, becomes:

$$P_d = \frac{e^2}{2(Z_{in})^2} R_d \tag{80}$$

The diode losses are also proportional to e^2 or the power level.

2.3.3.3 Losses due to Higher Order Modes

In Paragraph 5.3, we determined that some energy would go into the generation of higher order modes in the pulse line. Since this energy is not recovered, it represents a power loss equal to:

$$P_{ac} = \left(\frac{\omega_1}{\omega_o}\right) \frac{Z_o}{(Z_o + Z_{in})^2} e^2 \left[\frac{1}{4} - \frac{2 \cos^2 \phi}{\pi^2}\right] \tag{81}$$

This loss is also directly proportional to e^2 or power level. It can be made minimum by tuning so that $\cos \phi = 1$.

2.3.3.4 Input Current Diode Losses

The current in the diode due to the driving signal is given by Eq. (21) and is:

$$i = \frac{V}{L} t - \frac{V \pi}{\omega_1 L} - \frac{E}{\omega_1 L} \cos (\omega_1 t + \theta) \tag{82}$$

The power lost in the input circuit due to the various resistances is then:

$$P_L = \frac{\omega_1}{2\pi} \int_0^{\frac{2\pi}{\omega_1}} i^2 R \, dt \tag{83}$$

However, in most practical circuits, the SRD will be the major resistive element; thus, integrating and substituting R_d for R:

$$P_L = \frac{R_d}{(\omega_1 L)^2} \left[\frac{1}{3} \pi^2 V^2 + \frac{E^2}{2} - 2 V E \sin \theta \right] \tag{84}$$

In most cases, the last of three terms within the bracket can be neglected, resulting in:

$$P_L = \frac{E^2}{\frac{E^2}{V^2} \frac{3(\omega_1 L)^2}{\pi^2 R_d}} + \frac{E^2}{2 \frac{(\omega_1 L)^2}{R_d}} \tag{85}$$

Thus, the diode loss can be represented by two resistors in parallel with the input, one having a characteristic similar to the multiplier input resistance, R_ω defined by Eq. (25), and the other being a fixed resistor of value:

$$R_{dL}\Big|_{\text{fixed}} = 2 \frac{(\omega_1 L)^2}{R_d} \tag{86}$$

Comparing the variable resistor:

$$R_{dL}\Big|_{\text{variable}} = \frac{E^2}{V^2} \frac{3(\omega_1 L)^3}{\pi^2 R_d} \tag{87}$$

$$= \frac{E^2}{V^2} \omega L \frac{3}{2} \left[\frac{\omega_1}{\omega_o} \right] \frac{Z_o}{\pi R_d} \tag{88}$$

to the input resistor:

$$R_\omega = \frac{E^2}{V^2} \left[\frac{R_L \omega_1 L}{2 Z_o} \right] \tag{89}$$

we find that when typical values are inserted, $R_{dL}\big|_{variable}$ is perhaps an order of magnitude larger than R_{ω}.

2.3.3.5 Recombination Current Losses

The last seat of lost power is the recombination current which flows against the bias voltage. The instantaneous recombination current is:

$$i_r = \frac{1}{T_o} q(t) \tag{90}$$

where T_o is the carrier lifetime and $q(t)$ is the stored charge. Since:

$$q(t) = \int_o^t i\, dt \tag{91}$$

$$q(t) = \frac{V}{L}\,\frac{t^2}{2} - \frac{V\pi}{\omega_1 L}\,t - \frac{E}{\left(\omega_1\right)^2 L}\sin(\omega_1 t + \theta) + \frac{E}{\left(\omega_1\right)^2 L}\sin\theta \tag{92}$$

The average recombination current is then:

$$i_{ave} = \frac{\omega_1}{2\pi}\,\frac{1}{T_o}\int_o^{\frac{2\pi}{\omega_1}} q(t)\, dt \tag{93}$$

$$i_{ave} = \frac{V}{T_o}\left(\frac{\omega_o}{\omega_1}\right)\frac{2}{Z_o\,\omega_1}\left[\frac{\pi}{3} + \frac{Z_o}{R_L}\tan\theta\right] \tag{94}$$

And the power lost is:

$$P_i = \frac{V^2}{T_o}\left(\frac{\omega_o}{\omega_1}\right)\frac{2}{\omega_1 Z_o}\left[\frac{\pi}{3} + \frac{Z_o}{R_L}\tan\theta\right] \tag{95}$$

The power lost is proportional to the power level. This loss also increases with angle θ. Therefore the multiplier should be operated with drive level close to threshold value.

2.3.3.6 Summary of Losses

By way of summary, adding the three resonator losses (resonator I^2 R losses, diode rf losses, and higher order mode losses) has the effect of reducing the efficiency of the multiplier without changing its operating characteristics. Adding the input I^2 R losses and the effects of recombination current also reduces the efficiency and does so by adding shunt resistance across the input. The added resistance is non-linear with input voltage. If the multiplier is not overdriven, i.e., the angle θ is kept small, the loss resistances have the same voltage characteristic as the input resistance of the multiplier in that:

$$R_{input} = K\frac{E^2}{V^2} \tag{96}$$

The result is that the multiplier draws constant power from the driving source, regardless of driving level.

2.4 EXPERIMENTAL DATA - SHUNT MULTIPLIER

In order to illustrate the theory developed in the previous section, sample data from the test of one low frequency model will be presented. The multiplier in question is shown in schematic form in Figure 9. Pertinent data are:

Input Frequency	-	50 mc
Input Power	-	600 mw
Output Frequency	-	500 mc
Output Power	-	63 mw
Multiplication	-	X-10
Diode Type	-	hpa 0114

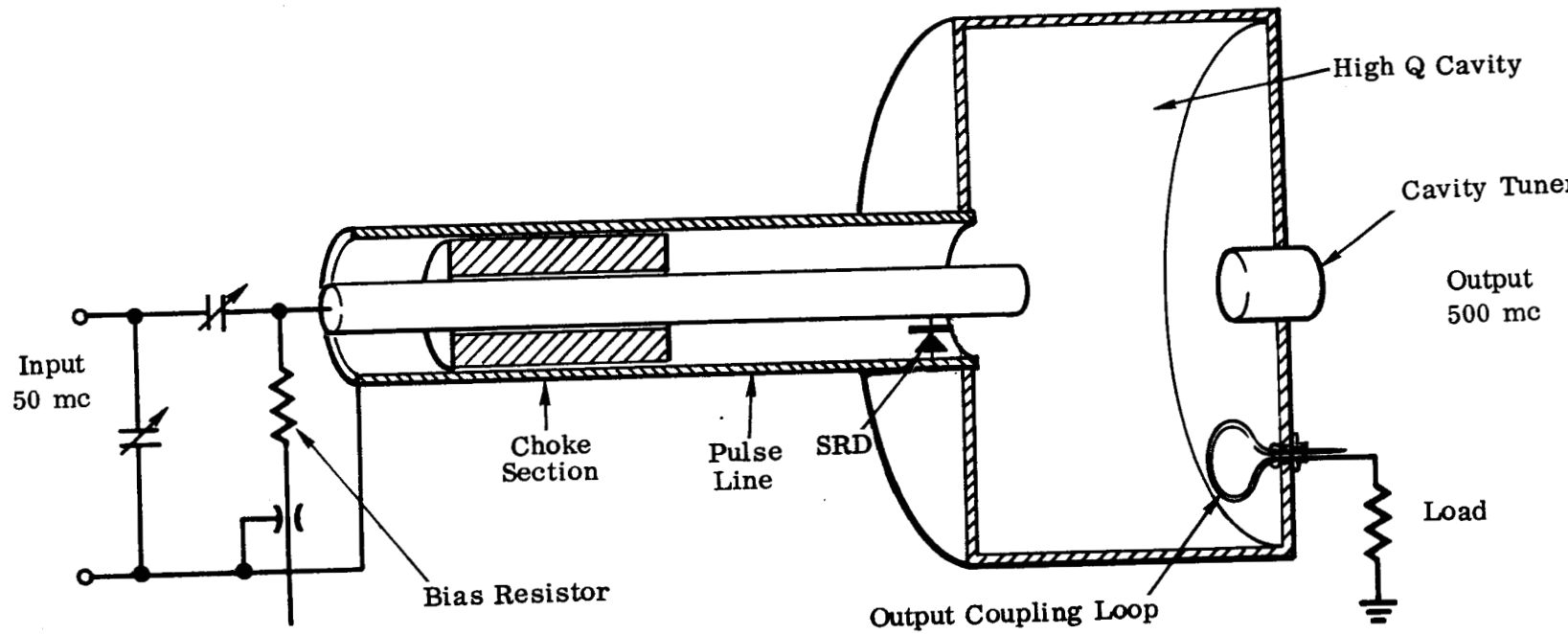


Figure 9 Schematic Diagram - 50 to 500 mc Multiplier

Referring to Figure 9, the input matching circuit is a pi with the shunt legs being a variable capacitance and the capacitance of the input choke of the multiplier and the series leg being a variable capacitance and the inductance of a length of coaxial line. DC bias is applied to the diode via a 50 ohm resistor. The sending impedance at the input to the multiplier proper, i.e., at the input choke, is estimated to be 15 ohms when the matching network is tuned for maximum power output.

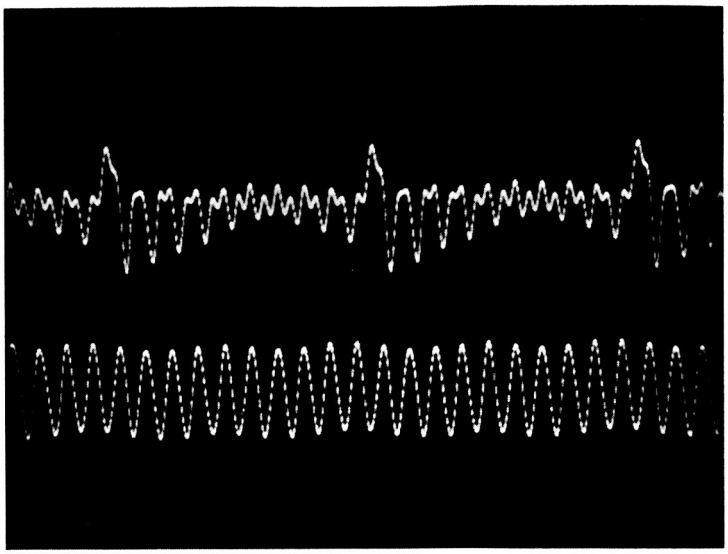
The pulse line consists of a length of coaxial line of 50 ohms impedance. In these particular tests, its length was set at 0.3 wavelength, that is, slightly longer then the quarter wavelength used in the analysis. The pulse line is coupled to the high Q TM_{010} cavity by extending it slightly into the region of maximum electric field of the cavity. Output is taken from the cavity by a loop coupling to a 50 ohm load.

This particular example was chosen because it illustrates both the theory, and how the low frequency model can provide a physical picture that extends beyond the analysis.

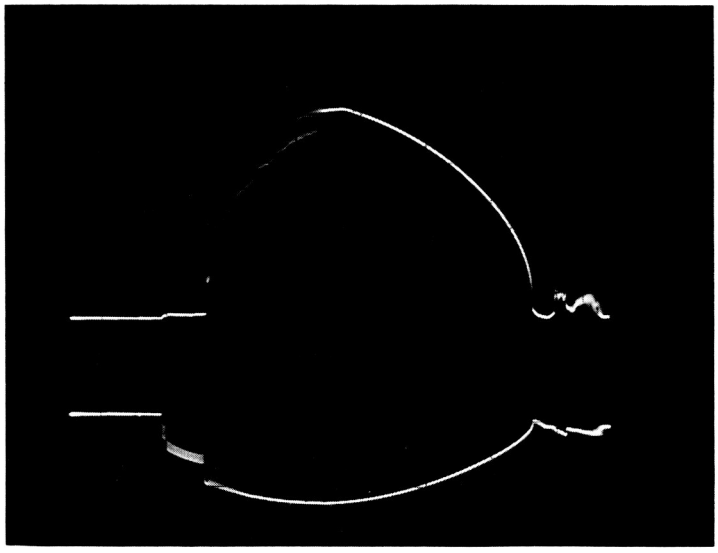
The bottom trace of Figure 10a is the 500 mc signal from the high Q cavity as seen by a sampling oscilloscope. A small amount of 50 mc amplitude modulation is detectable. The top trace is the voltage seen by a probe inserted in the pulse line near the SRD. The pulse occurring when the diode snaps is quite apparent. In addition a X-9 (450 mc) signal can be seen since the line is longer than a quarter wavelength for X-10. One can also see a signal of approximately 1000 mc. The hpa 0114 diode is sufficiently fast to excite the higher harmonics and the pulse line, when shorted by the diode, acts as a half-wave resonator at approximately 1000 mc.

The traces of Figure 10b were obtained by sweeping the bias voltage, while keeping the 50 mc drive to the multiplier constant. Increasing negative bias is toward the left. The top trace is power output as seen by a crystal detector on the output of the cavity. As the bias increases (going toward the left), the power increases and reaches a maximum. Shortly beyond the maximum, the signal breaks up into noise. This corresponds to the point where the fixed 50 mc drive is less than the threshold value required by the increasing bias voltage. Increasing the bias voltage finally reduces the power to zero.

The bottom trace is the power reflected from the input matching network as seen by a directional coupler and crystal detector in the 50 mc input line. The bottom of the trace corresponds to zero reflected power. Best match occurs at the point of maximum power output since this was the criterion in tuning the input circuit.



(a) Output Signals, Fixed Bias



(b) Output Power and Reflected Power Versus Bias

Figure 10 Oscilloscope Traces

3.0 SERIES SRD FREQUENCY MULTIPLIER

The second generic type of SRD frequency multiplier has been called the series circuit. It has several advantages over the shunt circuit just described. Chief of these is that the required geometry is mechanically less complex, a fact that becomes particularly important at very high output frequencies where the structure is small.

3.1 DESCRIPTION SERIES CIRCUIT

Figure 11 shows the series multiplier in schematic form. The input matching network and choke section are similar to those described for the shunt circuit. The distinguishing feature of the series circuit is that the resonator and pulse line are combined. The resonator consists of a length, ℓ, of transmission line of impedance, Z_o. The line is shorted at the right end and shunted by the low impedance choke at the left. The length is made a half wavelength at the output frequency, ω_o.

The SRD is placed a distance $K\ell$ from one end of the line. Typical construction would be to make the line coaxial with the diode in series with the center conductor.

Output power can be taken from the resonator in a number of ways. Typical is the use of a small loop at the shorted end as shown in Figure 11.

3.2 OPERATION AND ANALYSIS OF SERIES CIRCUIT

Operation of the series multiplier is best described by considering a special case. Take $K = 1/3$ so that one section of the line is twice the length of the other. Assume a current, I_o, flowing in the line due to the driving signal. And further assume that $\omega_o \gg \omega_1$ so that the current, I_o, can be considered to be uniform throughout the line.

Let the diode snap at $t = 0$ and consider the voltage and current distribution in the line as a function of time thereafter. The current and voltage sequences are shown in Figure 12.

At $t = 0$, the current is I_o and the voltage is zero throughout the line. When the diode snaps, the current at that point goes to zero. This negatively going current step, accompanied by the corresponding voltage steps, propagates in both directions. The step traveling to the right is reflected by the shorted end of the line and returns to the diode in time equal to:

$$t = \frac{2}{3}\left(\frac{2\pi}{\omega_o}\right) \qquad (97)$$

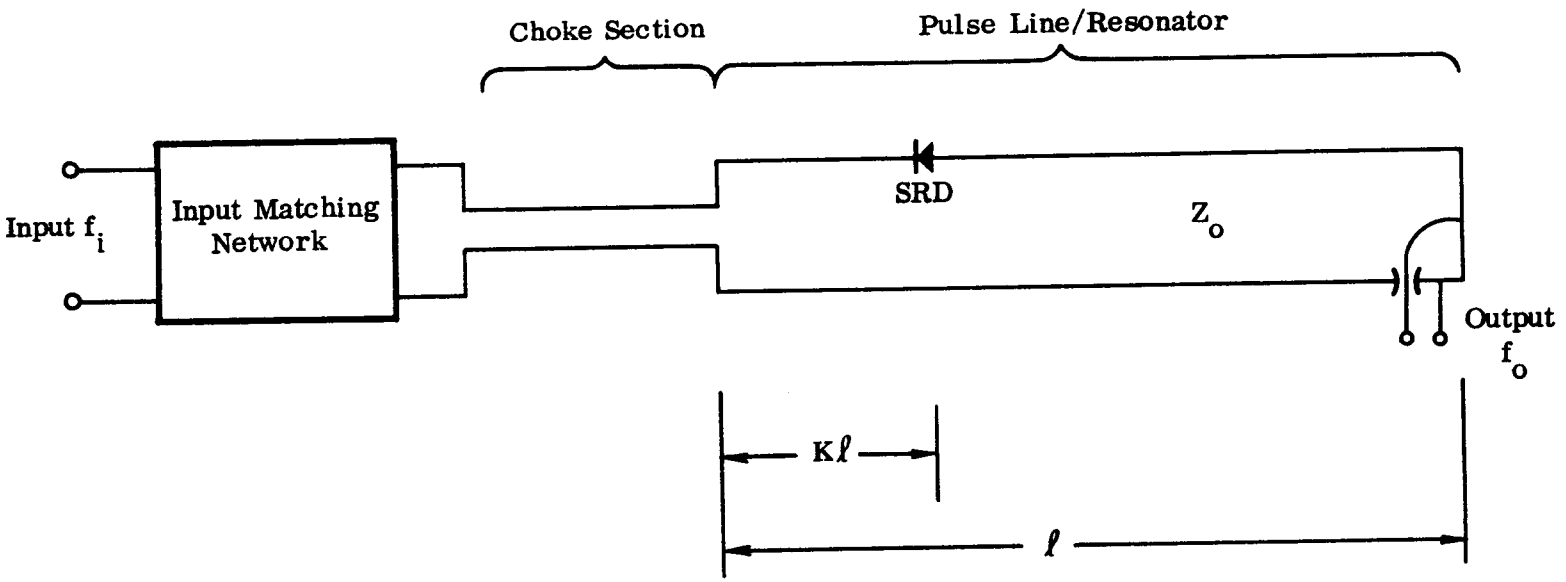


Figure 11 Schematic Diagram, Series SRD Multiplier

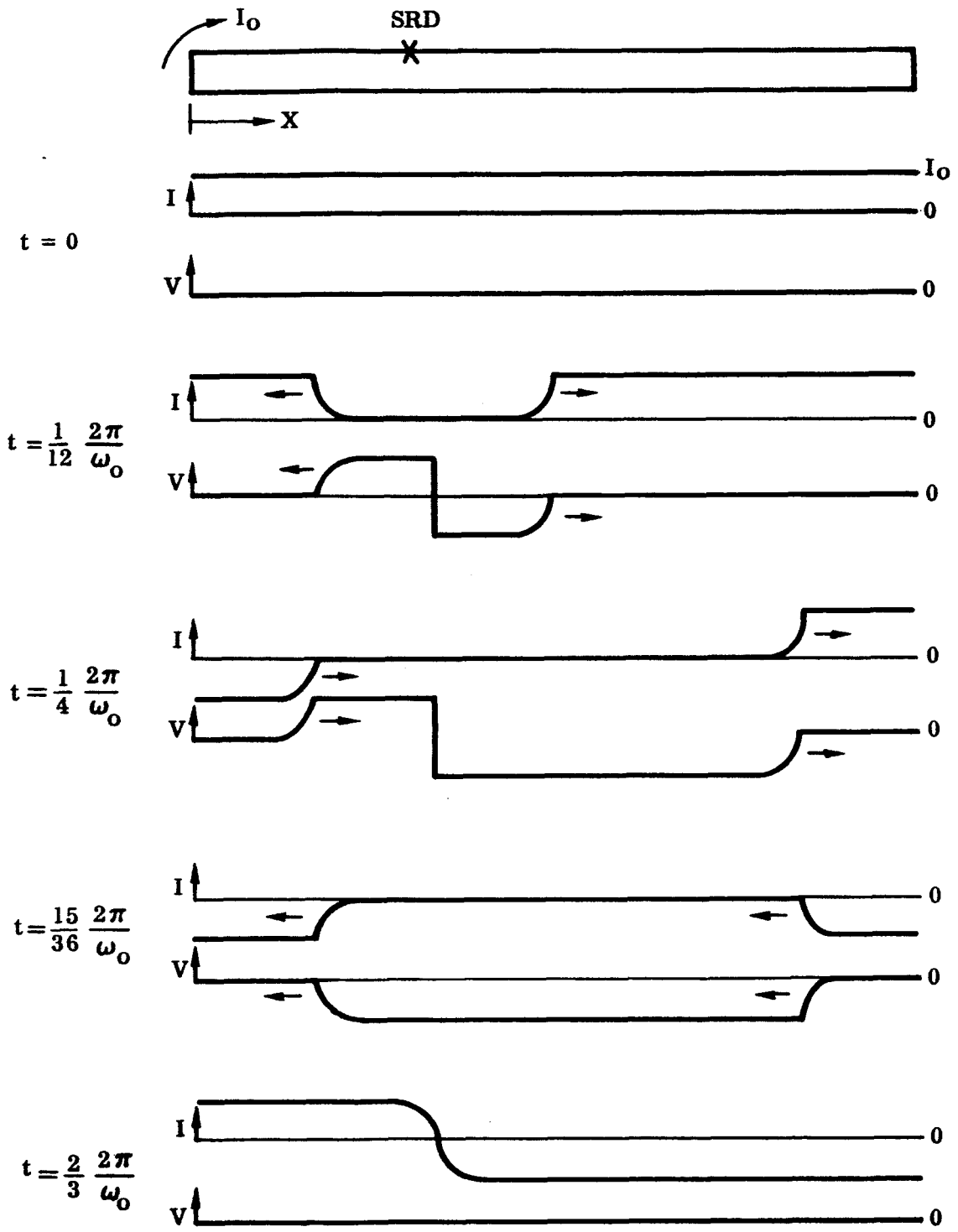


Figure 12 Voltage and Current Waveforms, Series Multiplier

During this same time, the step traveling to the left has been reflected by the choke, return to the diode and been reflected by the open circuit, returned to the choke and been reflected a second time, and returned to the diode again. At this point, the voltage across the diode is of the correct polarity to put the diode into forward conduction.

Thus, after the sequence described in Figure 12, the line is returned to its original condition, except that the current distribution which had been uniform, now approximates the distribution for half-wave resonance at the output frequency, ω_o, which is:

$$i = I_{\omega_o} \cos \frac{x}{\ell} \pi \tag{98}$$

By expanding the current distribution into its Fourier components, the average current in the line after the snap and the energy transferred each snap can be calculated. The current at ω_o is :

$$I_{\omega_o} = \frac{\pi}{2\ell} \int_0^{\frac{\ell}{3}} I_o \cos \frac{x}{\ell} \pi \, dx + \int_{\frac{\ell}{3}}^{\ell} (-I_o) \cos \frac{\lambda}{\ell} \pi dx \tag{99}$$

$$I_{\omega_o} = I_o \sin \frac{\pi}{3} \tag{100}$$

The energy transferred per snap is then -

$$E_{net} = \int_0^{\ell} \frac{1}{2} \mathscr{L} \, i^2 \, dx \tag{101}$$

Where $\mathscr{L}$ is the inductance per unit length of the line. Substituting the $\mathscr{L}$ from Eq. 66 and for i from Eq. 98 -

$$E_{net} = \frac{1}{2} \frac{\pi Z_o}{\omega_o} I_o^2 \sin^2 (\tfrac{\pi}{3}) \int_0^{\ell} \cos^2 \frac{x}{\ell} \pi dx \tag{102}$$

$$E_{net} = \frac{1}{4} \frac{\pi}{\omega_o} Z_o I_o^2 \sin^2 \left[\frac{\pi}{3}\right] \tag{103}$$

We can find an effective load impedance, R'_L, by noting that:

$$I_1 = -\frac{1}{3} I_o \tag{104}$$

Therefore, from Eq. 42,

$$R'_L = Z_o \frac{I_o - I_1}{I_o + I_1} = 2 Z_o \tag{105}$$

And the multiplier input impedance is:

$$R_\omega = \frac{E^2}{V^2} = \left[\frac{\omega_1}{\omega_o}\right] Z_o \tag{106}$$

Finally, as was done in the analysis of the impulse generator, we can calculate the output and input power as follows:

$$P_{out} = \frac{\omega_1}{2\pi} E_{net} = \frac{1}{8}\left[\frac{\omega_1}{\omega_o}\right] Z_o I_o^2 \sin^2\left[\frac{\pi}{3}\right] \tag{107}$$

Substituting equation (16) for I_o and (105) for R_L,

$$P_{out} = \frac{9}{32}\left[\frac{\omega_o}{\omega_1}\right] \frac{V^2}{Z_o} \sin^2\left[\frac{\pi}{3}\right] \tag{108}$$

The input power is:

$$P_{in} = \frac{E^2}{2 R_\omega} = \frac{1}{2}\left[\frac{\omega_o}{\omega_1}\right] \frac{V^2}{Z_o} \tag{109}$$

Finally,

$$P_{out} = \frac{9}{16} P_{in} \sin^2\left[\frac{\pi}{3}\right] = .42 P_{in} \tag{110}$$

The missing power goes into the production of higher order modes within the line.

3.3 LIMITATIONS ON ANALYSIS

The preceding is about as far as the analysis of the series circuit can be carried without being overwhelmed by mathematical complexity. The limitations on the above analysis are most restricting. We assumed that there was no signal at the output frequency in the resonator when the diode snaps. This is equivalent to saying that the rundown between snaps is complete, which is impractical operation, since the output signal would be 100% amplitude modulated.

The next step in the attack would be to assume some residual rf signal in the resonator and determine a new current distribution after snap. This would have to be done for all possible phase angles and levels of the residual signal. From these data, the stable operating level of the multiplier could be determined for the particular operating conditions chosen.

It would then be necessary to repeat the calculation assuming a different position of the diode. From all of these calculations, presumably the optimum operating conditions could be determined.

During the course of the program, a start was made toward programming the above series of calculations for solution by computer. The preliminary results appeared promising, and the work should be continued. However, at this time, the task was abandoned in favor of building and testing a series of experimental models.

4.0 INPUT MATCHING CIRCUIT

Perhaps the most difficult task in designing an SRD frequency multiplier is devising a satisfactory matching network between the variable input impedance of the multiplier and the fixed impedance of the driving signal source. The analysis indicates that, neglecting losses, the input impedance varies in such a way as to always accept constant power from the source. If one considers losses, additional non-linear resistance must be added in parallel with the calculated lossless impedance.

In addition to the unusual characteristics of the input impedance, one must also consider the fact that the current is rich in harmonics other than the output frequency. If care is not exercised in designing the input circuit, one or more of these harmonics may be supported by an unexpected resonance. The result can be loss of power, modulation, or hysteresis. Similarly the bias circuit can sometimes be a source of trouble.

4.1 MATCHING THE LOSSLESS MULTIPLIER

In Paragraph 5.2, the input impedance for small signals of the lossless frequency multiplier was determined to be:

$$R_\omega = \frac{E^2}{V^2} \frac{Z_{in}}{2 Z_o} \frac{V}{\frac{\pi V}{\omega_1 L} - \frac{2 e \cos \phi}{\pi Z_o}} \tag{111}$$

Assume that the output tank is tuned so that $\phi = 0$. Substituting for L and rewriting:

$$R_\omega = \frac{\pi}{4}\left(\frac{\omega_1}{\omega_o}\right) Z_{in} \frac{E^2}{V^2} \frac{1}{1 - \frac{1}{\pi}\left(\frac{\omega_1}{\omega_o}\right)\frac{e}{V}} \tag{112}$$

$$R_\omega = A \frac{E^2}{V^2} \frac{1}{1 - B\frac{e}{V}} \tag{113}$$

where A and B are constants which depend upon the fixed circuit parameters.

The equivalent circuit of the input interface is shown in Figure 13. E_{in} is the peak open circuit generator voltage and R_g is the generator impedance, which is assumed to be resistive:

$$E_{in} = \left(1 + \frac{R_g}{R_\omega}\right) E \tag{114}$$

$$E_{in} = E + \frac{1}{E} \frac{R_g V^2}{A} \left(1 - B\frac{e}{V}\right) \tag{115}$$

$$E = \frac{E_{in} \pm \sqrt{E_{in}^2 - 4 \frac{R_g V^2}{A} \left(1 - B\frac{e}{V}\right)}}{2} \tag{116}$$

Consider first the case when $e = 0$, that is, when the multiplier is first turned on. Curves of E versus E_{in} are shown in Figure14 for three values of $\frac{R_g V^2}{A}$.

If $\frac{R_g V^2}{A}$ is large, curve (a), and the drive is fixed at $E_{in} = (E_{in})_o$, the multiplier does not have an operating point. Experimentally, it is found that the multiplier does function, but the output is noisy and no phase coherence exists.

If $\frac{R_g V^2}{A}$ is reduced to curve (b) the multiplier will have two operating points, X and Y; however, point Y is unstable since a small increase in the value of E causes an increase in R_ω which causes a further increase in E.

Decreasing $\frac{R_g V^2}{A}$ further causes the operating point to move up to X'.

Now consider the case where $\frac{V^2 R_g}{A}$ is held constant and the voltage, e, is allowed to build up. Curves for E versus E_{in} are shown in Figure 15. Increasing values of e are represented by curves a, b, and c. Note that

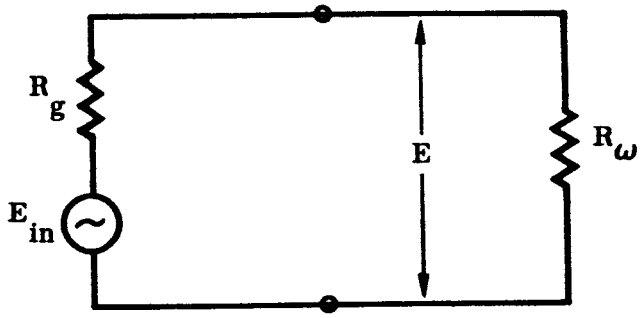


Figure 13 Input Interface Circuit

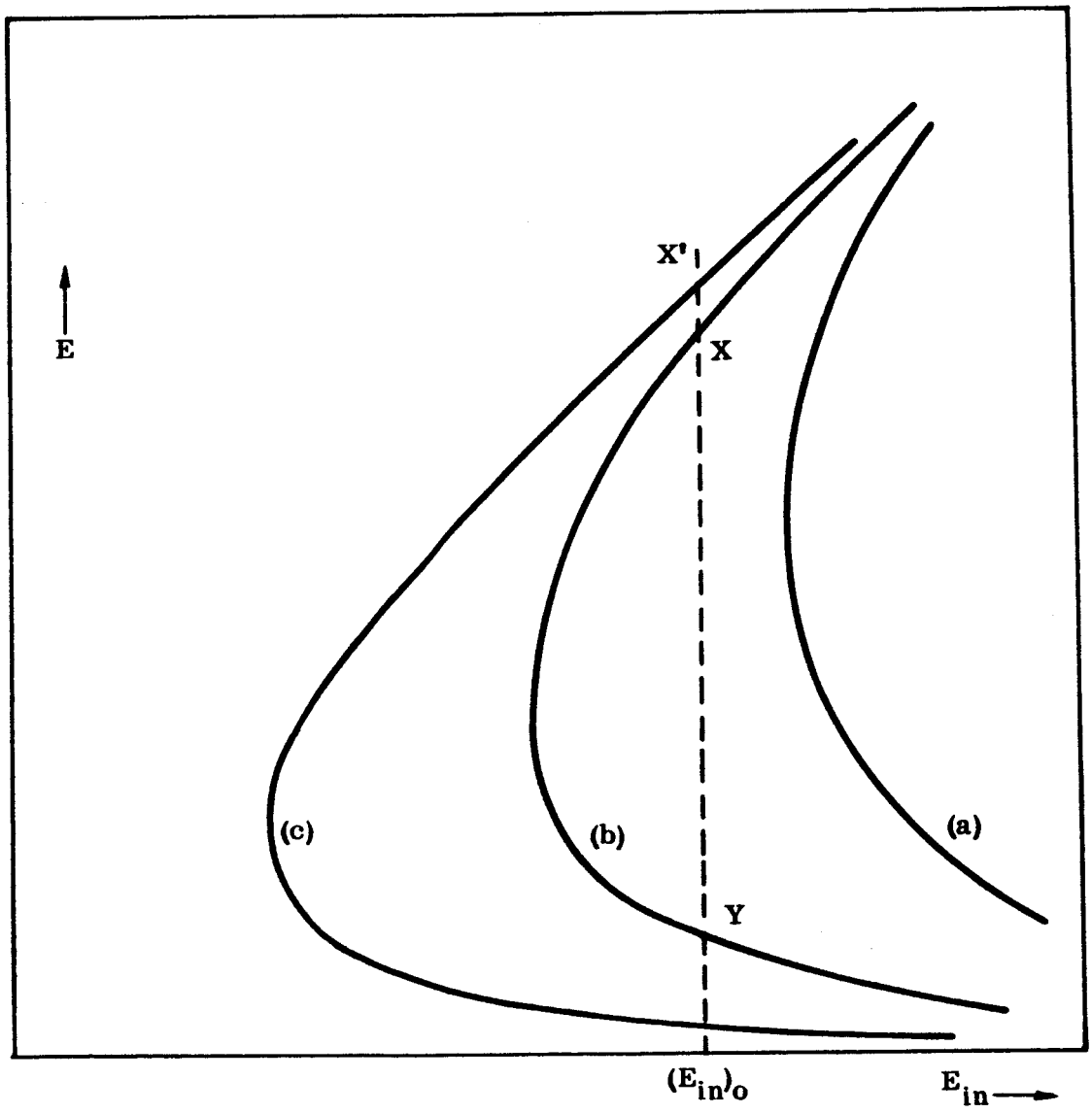


Figure 14 Input Voltage Versus Generator Voltage
(Zero Output)

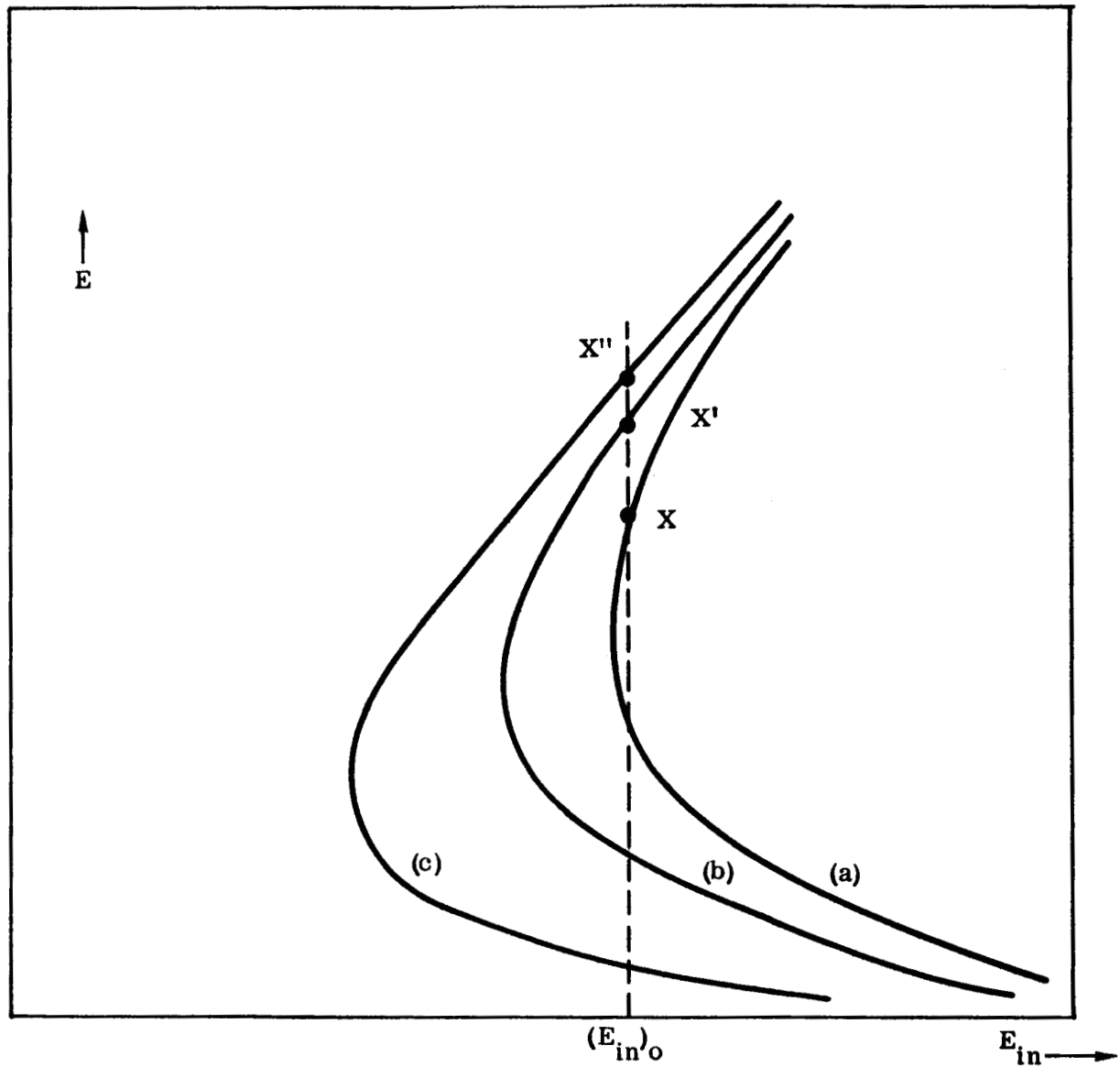


Figure 15 Input Voltage Versus Generator Voltage

each of these curves represents a constant power input. The operating point moves from X to X' to X'' as the voltage in the resonator builds up.

Constant level operation is reached when the output power, which is proportional to e^2, equals the input power multiplied by the system efficiency. That is:

$$\sigma e^2 = \eta \frac{V^2}{A} \left(1 - B\frac{e}{V}\right) \tag{117}$$

where σ is constant at proportionality and η is the efficiency. Equation (117) can be solved for e and is found to be:

$$e = K V \tag{118}$$

where K is a function at the circuit parameters of the multiplier but not of R_g. The power output at the stable operating point is:

$$P_{out} = \eta \frac{V^2}{A} (1 - BK) \tag{119}$$

Since the power output is proportional to V^2, one might be tempted to increase V until the operating curve is tangent to the line of constant E_{in}.

This would indeed result in maximum power output once the multiplier was operating, but the curve corresponding to the same circuit parameters with zero resonator voltage would lie to the right of the $E_{in} = (E_{in})_o$ line and the multiplier would not start.

Differentiating Eq. (115) with respect to E and setting to zero yields the value of E at the knee of the curve:

$$\frac{\partial E_{in}}{\partial E} = 0 = 1 - \frac{1}{E^2} \cdot \frac{R_g V^2}{A} \left(1 - B\frac{e}{V}\right) \tag{120}$$

$$E^2 = V^2 \frac{R_g}{A} \left(1 - B\frac{e}{V}\right) \tag{121}$$

$$R_\omega = A \frac{E^2}{V^2} \frac{1}{1 - B\frac{e}{V}} = R_g \tag{122}$$

That is, the multiplier input impedance is matched to the generator impedance at the knee of the curve. Since the multiplier will never be operated at this point, it follows that normal operation is with the input mismatched and that the mismatch is such that the input of the multiplier is a higher impedance than the generator.

4.2 MULTIPLIER WITH LOSSES AND INPUT REACTANCE

In Paragraph 2.3.3.6 the analysis indicated that recombination current losses and diode I^2R losses could be represented by non-linear resistors placed in parallel with the equivalent lossless input resistor, R_ω. Furthermore, it was found that these added resistances could be approximated by two parallel resistors, one being purely ohmic and the other having a characteristic similar to R_ω, that is:

$$R = K\frac{E^2}{V^2} \tag{123}$$

The analysis of Paragraph 4.1 will not be extended to consider the added resistors, except to point out that the form of the curves of Figures 14 and 15 is not greatly altered. A family of curves of E versus E_{in} considering losses is sketched in Figure 16. It can be seen that the matching problem is qualitatively the same.

A somewhat more serious perturbation is encountered if the multiplier is operated in such a manner that the reactive portion of the input impedance cannot be neglected. The input reactance is given by Equation (26), and

$$X_\omega = j\,\omega_1 L\,\frac{E}{2V\sqrt{1-\frac{V^2}{E^2}\left(\frac{\pi Z_o}{R_L}\right)^2}} \tag{124}$$

Consider first the problem of changing input reactance due to the signal level building up in the output tank. At the start of operation $R_L = Z_{in}$, and the drive level will normally be set so that:

$$E \approx E_{Thresh} = \frac{\pi V Z_o}{R_L} \tag{125}$$

Under these circumstances, X_ω is very large.

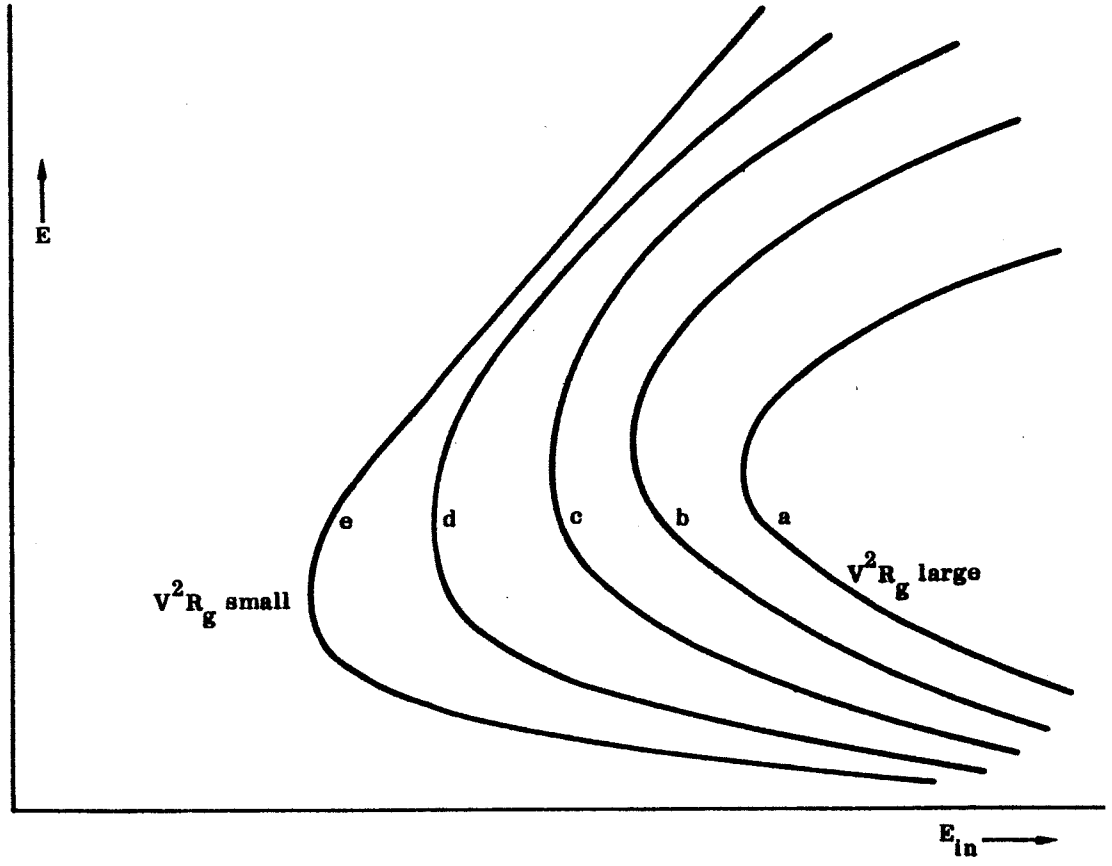


Figure 16 Drive Voltage Versus Generator Voltage Multiplier with Losses

As the signal level builds up, R_L increases in magnitude. The maxium value, by Equation (45), approaches infinity. Therefore the minimum value of X_ω is:

$$X_\omega \Big|_{\text{min}} = j\ \omega_1\ L \frac{E}{2V} \tag{126}$$

Since the magnitude of E will typically be ten times greater than V,

$$X \Big|_{\text{min}} \approx 5\ (j\ \omega_1\ L) \tag{127}$$

This reactance is in parallel with a fixed reactance of:

$$X \Big|_{\text{fixed}} = j\ \omega\ L \tag{128}$$

which is due to the inductance of the pulse line. As a result, the detuning due to the variable reactance as the signal builds up will not be a serious problem, unless the input circuit has an unusually high Q.

On the other hand, there are applications where the bias voltage, V, is varied over a wide range; for example, to obtain wide phase deviations. In this case, the variations in X_ω can seriously detune the input matching network, and it is often necessary to add a fixed resistance across the input to swamp the reactive components to obtain smooth operation.

5.0 SPECIAL TESTS AND CIRCUITS

In the course of the program carried out on NAS 8-20257, a number of specialized areas were explored. These will be discussed briefly in the following paragraphs.

5.1 PHASE MODULATION TESTS

One of the more useful characteristics of the SRD multiplier is the ease with which it can be phase modulated. Equation (19) relates the time of the snap to the phase of the driving signal. That is,

$$E \cos \theta = \frac{-\pi V Z_o}{R_L} \tag{129}$$

The phase change of the output signal is

$$\theta' = N\theta = \frac{\omega_o}{\omega_1} \theta \tag{130}$$

where N is the multiplier multiplication factor.

Therefore,

$$\theta' = \frac{\omega_o}{\omega_1} \cos^{-1} \left[\frac{\pi Z_o}{R_L} \frac{V}{E} \right] \tag{131}$$

Substituting for R_L and E from (49) and (116),

$$\theta' = \frac{\omega_o}{\omega_1} \cos^{-1} \left\{ \frac{2\pi \frac{Z_o}{Z_{in}} V \left| 1 - \frac{1}{\pi} \left(\frac{\omega_1}{\omega_o} \right) \frac{e}{V} \right|}{E_{in} + \sqrt{E_{in}^2 - \frac{16}{\pi} \left(\frac{\omega_o}{\omega_1} \right) \frac{R_g}{Z_{in}} V^2 \left| 1 - \frac{1}{\pi} \left(\frac{\omega_1}{\omega_o} \right) \frac{e}{V} \right|}} \right\} \tag{132}$$

The above expression is not too useful in its present form; however, assuming the approximation of equation (118) is valid over the range of values of V of interest, equation (132) can be reduced to:

$$\theta' = N \cos^{-1}\left[\frac{GV}{E_{in} + \sqrt{E_{in}^2 - HV^2}}\right] \qquad (133)$$

where G and H are constants which depend only on circuit parameters. Equation (133) has the general form shown in Figure 17 and can be differentiated to find the modulation coefficient at any operating point. The analysis will not be carried out further, but one of the problems in applying Equation (133) to a practical SRD multiplier should be pointed out. In our analysis of the matching problem, we have assumed that the reactive portion of the input impedance, given by Equation (26) was tuned out. In practice, this is possible if the operating point is not shifted over too wide a range of the driving voltage E_{in} and the bias voltage, V. If wide variations in phase are required, as when the multiplier is used to drive a phased array antenna, the variation in the reactive portion of the input impedance probably becomes the dominating factor in determining the multiplier performance.

The curve of Figure 18 shows the variation in phase of the output signal as a function of bias voltage for an S-band series type multiplier. Pertinent data are as follows:

Input Frequency	-	220 mc
Input Power	-	1000 mw
Output Frequency	-	2200 mc
Output Power	-	160 mw (center of band)
Power Variation Over Mode	-	2 db
Diode Type	-	hpa 0242

The phase is measured by driving two identical multipliers from a common source. The bias voltage of one is held fixed and it serves as a phase reference at 2200 mc. The phase of the second is compared to the reference, using a slotted line as an interferometer. Accuracy of the system is better than ±1°.

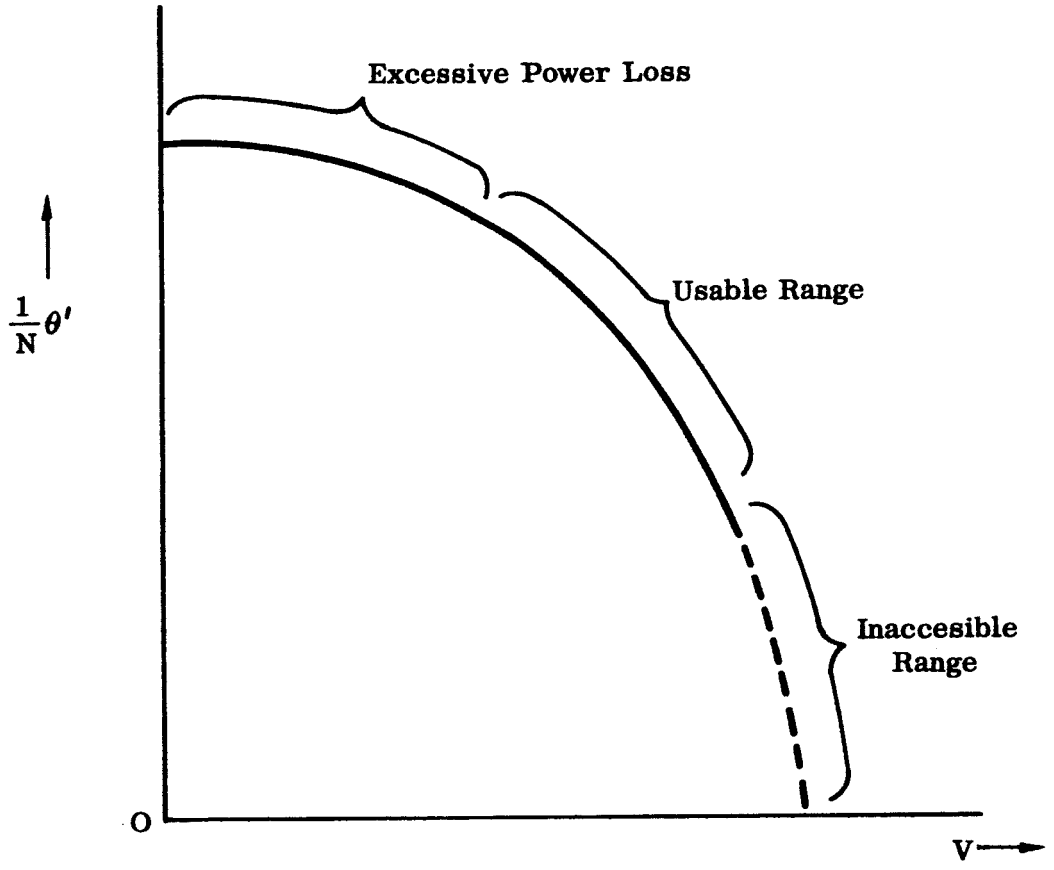


Figure 17 Output Phase Versus Bias Voltage

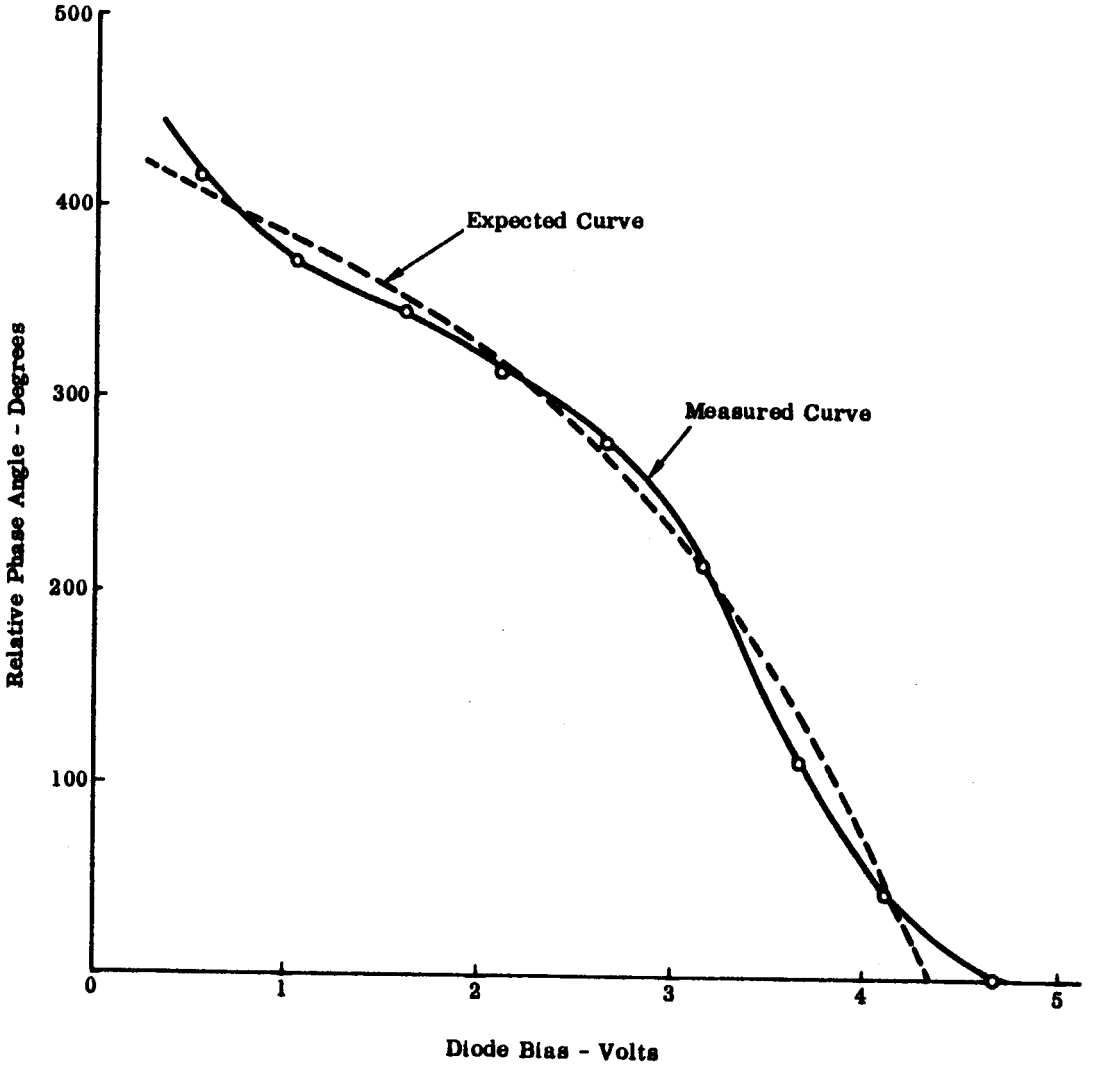


Figure 18 Phase Shift Versus Diode Bias

The curve of Figure 18 shows the general form of the predicted curve of Figure 17; however, there appears to be a periodic variation superimposed on the gross curve. The cause of this phenomenom has not yet been determined.

5.2 AMPLITUDE MODULATION - SELF-BIAS OPERATION

The analysis of the multiplier indicates that the output power is independent of the driving voltage as long as the latter is greater than a threshold valve set by the bias voltage. This fact is confirmed by the experimental data presented in Figure 19, which shows curves of output power versus power input for the same S-band multiplier described in Paragraph 5.1. Curves for three values of bias voltage, V_1 are presented.

The constant output power would seemingly preclude using the SRD multiplier in an amplitude modulation system, however, one can take advantage of the recombination current to self-bias the diode. With proper choice of self-biasing resistor and fixed bias, one can achieve a reasonable linear relationship between input and output power.

The average recombination current is given by Equation (94),

$$i_{ave} = \frac{V}{T_o} \frac{\omega_o}{\omega_1} \frac{2}{Z_o \omega_1} \left[\frac{\pi}{3} + \frac{Z_o}{R_L} \tan\theta \right] \tag{134}$$

The diode bias is the sum of the self-bias, fixed bias, and internal contact potential,

$$V = R_b i_{ave} + V_F + V_C \tag{135}$$

Setting $V_f = -V_c$ and substituting Equation (135) into Equation (134),

$$1 = \frac{R_b}{T_o} \left(\frac{\omega_o}{\omega_1} \right) \frac{2}{Z_o \omega_1} \left[\frac{\pi}{3} + \frac{Z_o}{R_L} \tan\theta \right] \tag{136}$$

or

$$\tan\theta = \frac{R_L}{Z_o} \left[\frac{T_o}{R_b} \left(\frac{\omega_1}{\omega_o} \right) \frac{Z_o \omega_1}{2} - \frac{\pi}{3} \right] \tag{137}$$

With the proper choice of R_b, θ will be small and, assuming R_L is constant, θ will not change with varying drive voltage. Thus, the bias voltage increases with increasing drive voltage. As a consequence, the input impedance, R_ω, is constant and the output power proportional to the input power.

The curves of Figure 20 show output power and reflected power (from the input mismatch) as a function of input power for the S-band multiplier with a self-biasing resistor of 372 ohms. Since the ratio of reflected to incident power stays constant, the input impedance is constant.

5.3 TEMPERATURE EFFECTS

Exhaustive temperature tests were not performed on the SRD multiplier during the course of this program. Sufficient tests were performed however to indicate that no major problem exists in this area. The two diode parameters which directly effect multiplier performance, the transition time and the minority carrier lifetime, are very slow functions of temperature. Thus, it would be expected that multiplier operation would be reasonably constant with temperature, even if no measures were taken to compensate the device. This is borne out by test on the S-band multiplier whose output power varied less than 10% as the temperature was varied over the range from -50° to +100°C.

The principal effect of temperature variation is to shift the bias point which, unless counteracted, will shift the phase of the output signal. The curve of Figure 21 shows the phase shift of the output as a function at multiplier temperature. The effect is dependent upon the bias point chosen, but for a fixed bias point, the change is reasonably linear with temperature.

The investigation of temperature effects was not pursed further, since the multiplier appears amenable to temperature compensation, using the usual techniques. A much more difficult design task will probably be compensating the circuit providing the drive signal to the multiplier.

5.4 MULTIPLE DIODE CIRCUITS

One of the present limitations on SRD multiplier output power is set by the thermal properites of the diodes themselves. Diode manufacturers are attempting to increase the allowable input power by reducing the diode resistance and improving diode package to get rid of heat more efficiently.

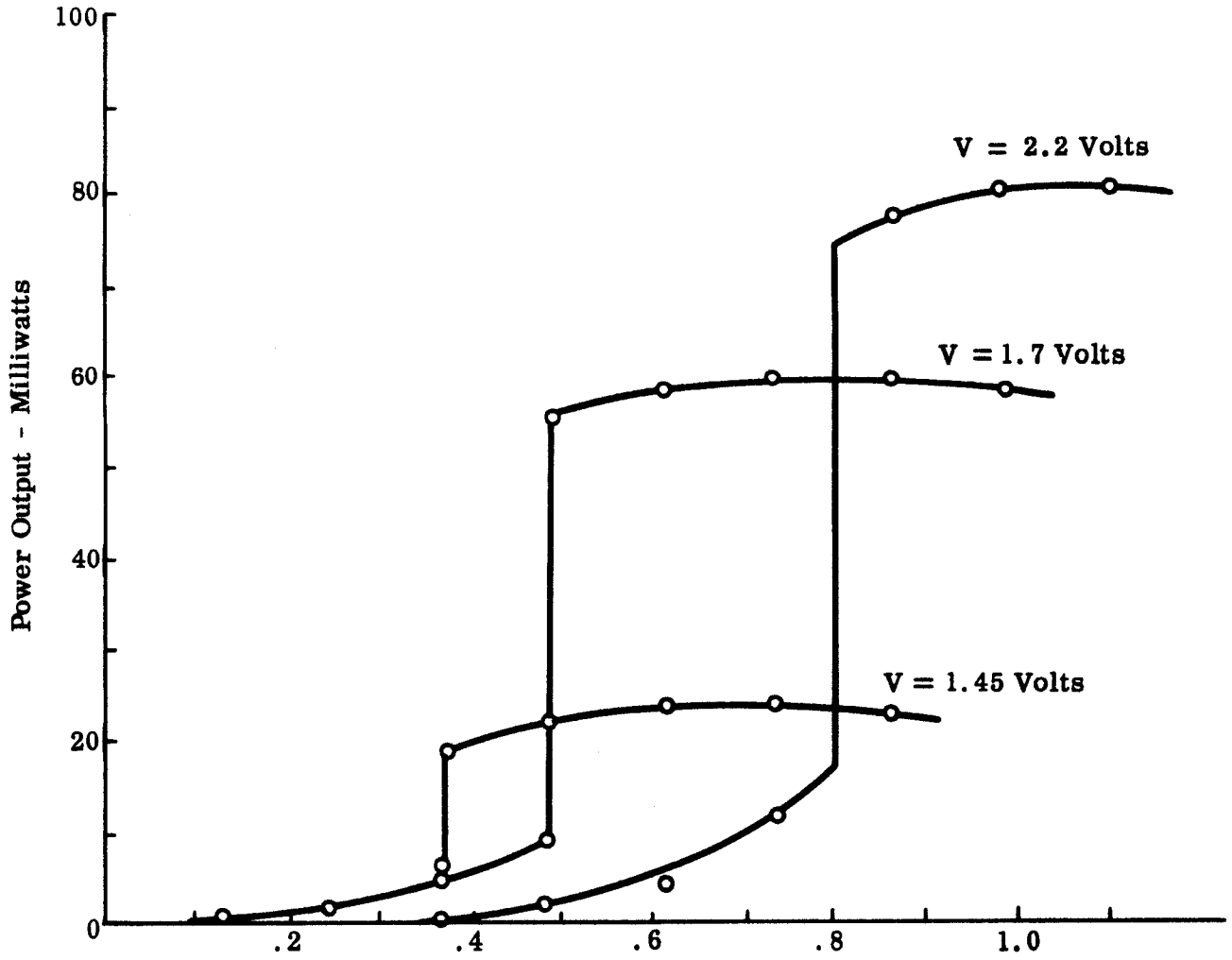


Figure 19 Power Output Versus Power Input S-Band Multiplier with Fixed Bias

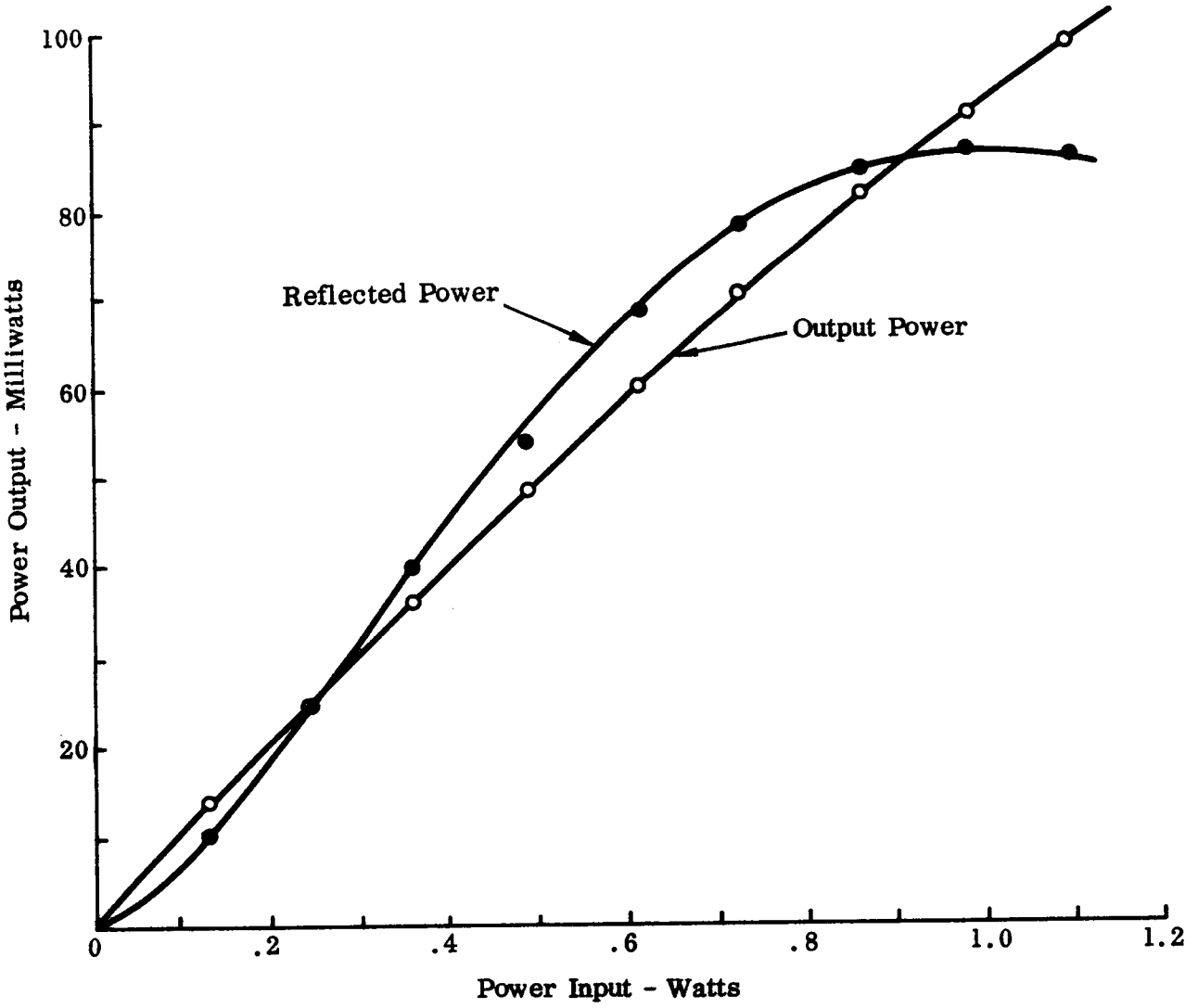


Figure 20 Power Output Versus Power Input S-Band Multiplier with Self Bias

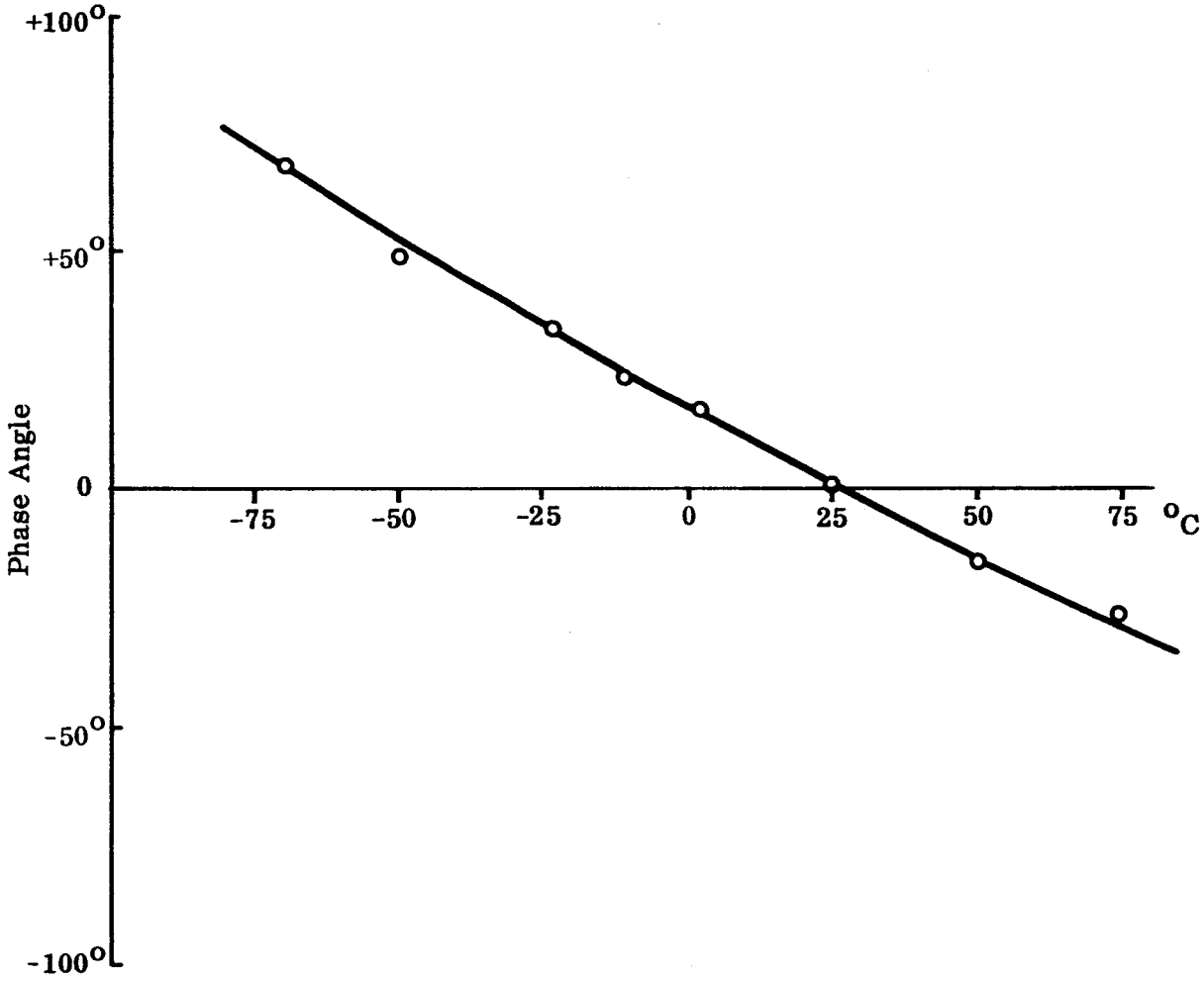


Figure 21 Phase Shift Versus Temperature

An obvious way to increase the allowable input power and thereby increase the output is to use more than one diode in the circuit. The problems of using multiple diodes was explored as an early task of this program, and it was found that such circuits are entirely feasible, provided certain rules were observed.

In the case of the shunt circuit, the rules are quite simple. Each diode must have its own pulse line and its own bias circuit. Attempting to parallel two diodes in a common circuit simply results in one or the other of them carrying the entire load. By operating each in a separate pulse line, each operates independently of the other and, indeed, no special care is required in matching the characteristics of the diodes. The output of the pulse lines are coupled to a common high Q cavity from which the multiplier output is taken. Enough signal is fed back from the cavity to keep each diode synchronized.

Separate bias circuits are required to allow each diode to be set at its optimum power point, and to provide gross phase adjustment to synchonize the individual snap points to the common output signal.

In practice, it was found easier to provide a separate input matching network for each diode although in theory this should not be required.

Multiple diode series type multipliers are more complex since the pulse line is combined with the resonator. No satisfactory arrangement was found except to parallel complete multipliers and combine the outputs in a common output resonator.

A two diode push-pull series multiplier was built and tested. It had approximately the same efficiency as a single diode multiplier and could be safely operated at twice the power level.

There appears to be no reason why more than two diodes could not be used and the power handling capability increased proportionately. Such a circuit would become very complex and difficult to package and operate.

6.0 CONCLUSIONS

Although great progress has been made in the past year in the application of step recovery diodes, the SRD multiplier is still in early stages of its evolution. As might be expected, the program carried out so far on Contract NAS 8-20257 has brought to light as many questions as it has resolved. The design of SRD multipliers is less of an empirical process, but the designer can expect to be surprised occasionally.

6.1 CHOICE OF CIRCUIT TYPE

Two types of circuits have been considered in this report. The choice between the shunt and series type depends largely upon the application. The shunt circuit is easier to handle because the various parameters can be identified with physical circuit elements. The shunt circuit may also have an advantage in that the diode can be cooled more efficiently. On the other hand, the series circuit is mechanically less complex, making it more easily adapted to high frequency multipliers.

This report has concentrated on what have been called the shunt and series circuits. It is recognized that the distinction between the two is somewhat artificial, and that other circuits can be devised which will take advantage of the fast switching characteristics of the SRD to transfer energy from one circuit to another.

6.2 NEEDED DIODE IMPROVEMENTS

Many semiconductor manufacturers have entered the step recovery diode field and presumably all are working toward reducing the transition time, reducing junction capacitance, and reducing series resistance of their product. These are obvious areas where diode improvement will result in immediate improvement in multiplier performance.

From the circuit designers' point of view, an equally important area for improvement is diode packaging. Smaller physical size is needed to enable the devices to be used above X-band. Conversely, better thermal properties are needed to reach higher powers. Since these two requirements are not generally compatible, the final answer to the packaging problem may lie in integrating the diode and its immediate circuitry.

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6.3 FURTHER CIRCUIT DEVELOPMENT

The primary need now is a backlog of engineering experience in using the SRD. Such a backlog can be built up best by using the device in specific circuits and solving the specific problems which appear. However, further general study and circuit development would be profitable in several areas. One such area is the development of transitorized driving circuits with particular study of the problems of matching an SRD multiplier to a class C power amplifier. A second is a study of the problems associated with packaging in integrated circuits.

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