June 1967 Brief 67-10176

NASA TECH BRIEF

Thermal and Bias Cycling Stabilizes Planar Silicon Devices

The problem:

To reduce the inversion tendencies of planar silicon devices.

The solution:

Extend the time of the terminal burn-in or baking step carried out in the processing of the device (e.g., a planar transistor) and cyclically bias the collector-base junction of the device during the burn-in period. Alternate application and removal of reverse bias discharges and purges those ions which give rise to the problem of inversion and long-term drift during operation of these devices. For MOS field effect transistors, this processing step will reduce the surface-state density of inversion-causing ions and result in more stable threshold voltages.

Note:

Inquiries concerning this invention may be directed to:

Technology Utilization Officer
Electronics Research Center
575 Technology Square
Cambridge, Massachusetts 02139
Reference: B67-10176

Patent status:

Inquiries about obtaining rights for the commercial use of this invention may be made to NASA, Code GP, Washington, D.C. 20546.

Source: J. E. Meinhard and R. E. Harris
of North American Aviation, Inc.
under contract to
Electronics Research Center
(ERC-48)

Category 01