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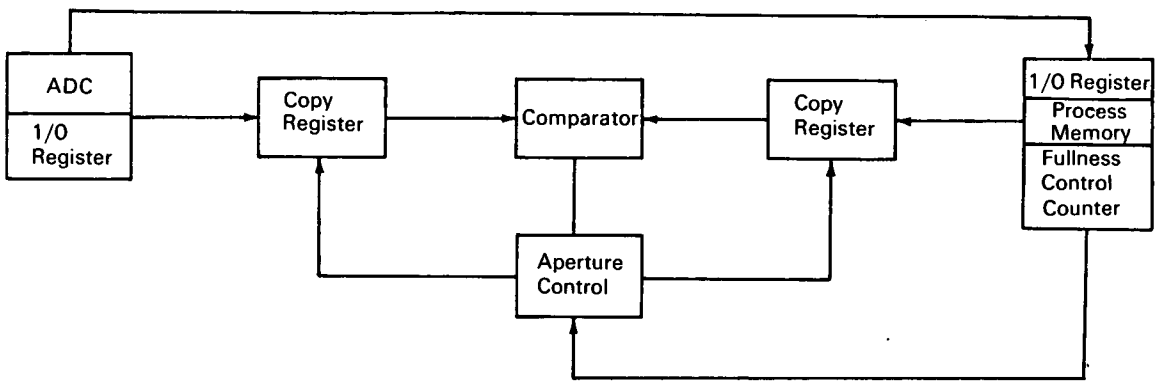
A Conceptual, Parallel Operating Data Compression Processor



The problem:

Ever increasing bit rates in telemetry communication have caused prior art processors to become more and more bulky and complex due to their serial operation at relatively low speed.

The solution:

A novel data compressor processor concept wherein the system is, at the same time, a zero-order processor, a floating aperture, a variable aperture, and a binary integer aperture with a decoded buffer fullness counter directly constituting the aperture.

How it's done:

Two samples, one of which is the present sample (data point) assumed to be available in parallel at the analog-to-digital converter (ADC) input-output (I/O) register, the other being the last accepted sample (of the same channel that is presently being sampled) that is assumed to be available in parallel at the process memory (PM) I/O register, are to be compared as to relative magnitude. The amount of the aperture is then added to the smaller and the two samples are again compared using the same relative magnitude comparator. If the outcome of the second comparison is the same as that of the first, the difference between the two samples is equal to or greater than the amount of the aperture, indicating that the sample is accepted. Each of the two I/O registers is followed by a copy register so that the original value may be recovered if the outcome of the comparison between the altered and unaltered sample is inconclusive. These copy registers are connected as unidirectional binary counters with entries at each bit. Connected between the copy registers is a comparator with a single output that is pulsed only when the ADC sample is greater than the PM sample. The output from the comparator at time t_1 controls the adding of the aperture to either copy register. Because the aperture control is a binary integer, its addition to either copy register is simply a one term entry to the specific register at the proper position. The copy registers are connected as binary counters with regular forward carries. After the aperture has been added to either copy register, the output from the comparator at time t_2 will control the transfer of the number in the ADC I/O register to the PM I/O register.

(continued overleaf)

A fixed-aperture processor so described may be modified to provide an exponentially variable aperture that would be a function of the process memory fullness. This requires a shift-right, shift-left shift register containing all zeroes except one "1" at any time. These shift-right, shift-left pulses derive from the process memory fullness level markers. The position of the "1" indicates the aperture size 1, 2, 4, 8, 16, 32, etc.

Note:

This development is in conceptual stage only, and as of date of publication of this Tech Brief, neither a model nor prototype has been constructed.

Patent status:

No patent action is contemplated by NASA.

Source: Tage O. Anderson
Jet Propulsion Laboratory
(NPO-10068)