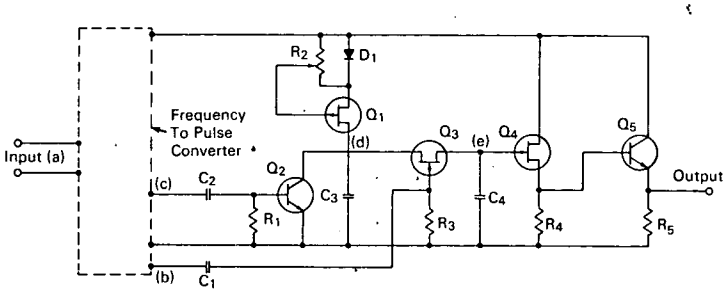
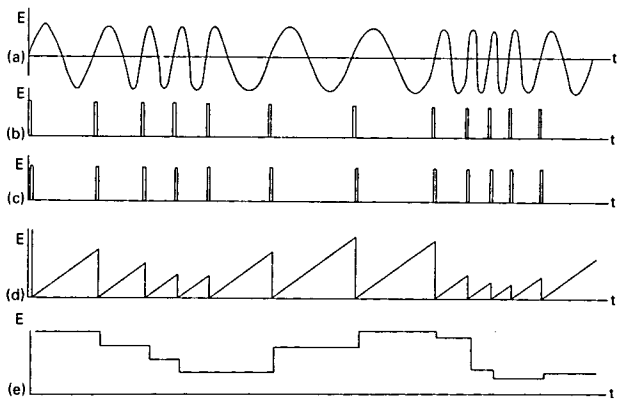
NASA TECH BRIEF

Fast-Response Frequency-to-Analog Converter





WAVEFORMS AT DESIGNATED POINTS ON CIRCUIT DIAGRAM

The problem:

To design a frequency-to-analog converter having a fast response time (equal to the period of the input signal) and a low ripple (no higher than 1 percent of reading).

The solution:

The circuit employs a frequency-to-pulse converter which provides two pulse trains, both at the same frequency as that of the input signal, but with a 10 microsecond difference between the trains. The pulses should have a duration of 5 to 10 microseconds and an amplitude of approximately 5 volts.

Pulse train (c) is coupled to transistor Q_2 through capacitor C_2. Capacitor C_3 is charged by the constant current network consisting of R_2, D_1, and Q_1. Potentiometer R_2 adjusts the charging current, and diode D_1 biases the FET (field effect transistor) Q_1. As transistor Q_2 is turned on by pulse train (c), capacitor C_3 discharges to zero potential. Between pulses, this capacitor is charged at constant current, resulting in a sawtooth waveform at (d) having a peak voltage that

(continued overleaf)

is proportional to the period of the input frequency.

Pulse train (b) (which leads pulse train (c) by 10 microseconds) is coupled through C_1 to Q_3, a unipolar FET. A low-resistance path (approximately 600 ohms) is provided between C_3 and C_4 when Q_3 is turned "on" by pulse train (b). During the "off" time of Q_3, the resistance is approximately 150 megohms. Therefore, the potential difference between C_3 and C_4 will fall to zero when Q_3 is turned "on". Capacitor C_4 has a much smaller capacitance than C_3 to minimize any loading effect of C_4 on C_3 and also to reduce the time for potential equalization to less than 1 microsecond.

Transistor Q_3 is turned "on" at approximately the peak of a sawtooth, thereby charging C_4 to the peak sawtooth potential. The dc level (e) on C_4 is directly coupled to Q_4, an FET with an input impedance of approximately 10,000 megohms. Q_4 is placed in a source follower configuration for low output impedance. The output of Q_4 is in turn coupled into a common emitter configuration for even a lower output impedance (approximately 200 ohms).

The dc output voltage (maximum 20 volts at 1 cps) of the converter is inversely proportional to the input frequency. Its upper frequency limit is 5000 cps, with an output of approximately 5 millivolts. A dc voltage monitor can be coupled to the output and calibrated to read in cps.

Notes:

1. The frequency-to-pulse converter (shown as a dashed block) is of standard design.
2. This frequency-to-analog converter can be used to record small response changes in electrical output transducers. It can also be used as a low-frequency modulation detector.
3. Inquiries concerning this invention may be directed to:

   Technology Utilization Officer
   Marshall Space Flight Center
   Huntsville, Alabama 35812
   Reference: B67-10257

Patent status:

Inquiries about obtaining rights for the commercial use of this invention may be made to NASA, Code GP, Washington, D.C. 20546.

Source: Frank S. Hagihara
of North American Aviation, Inc.
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