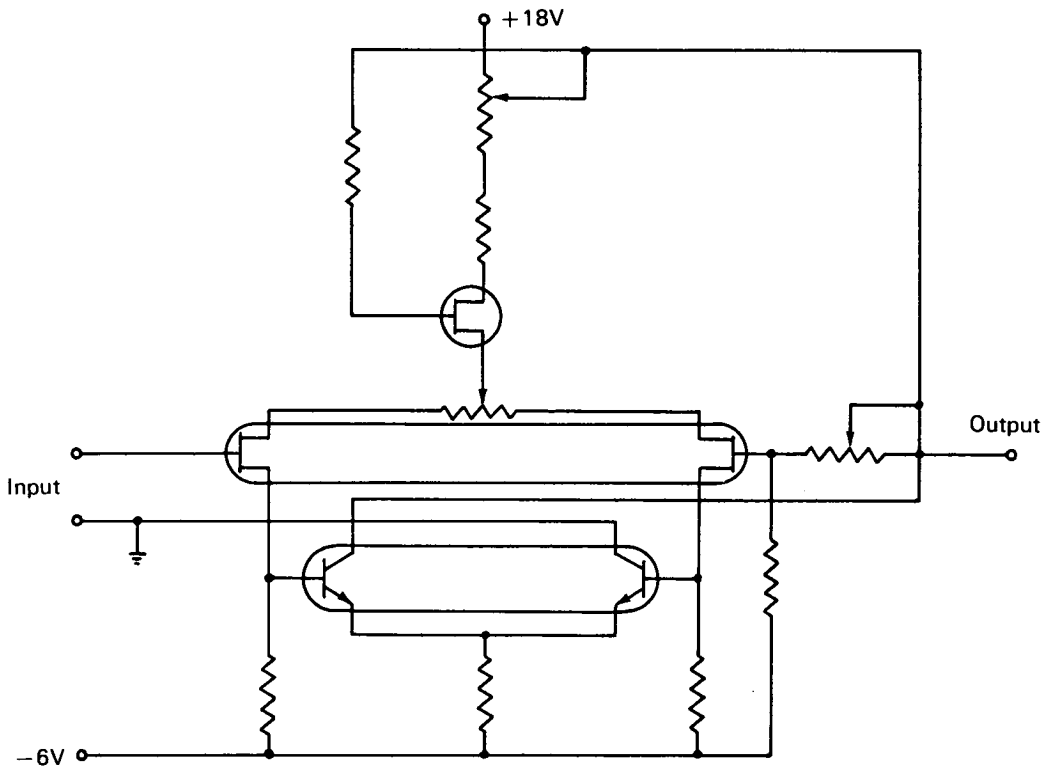
NASA TECH BRIEF

Field Effect Transistors Improve Buffer Amplifier



The problem:

To achieve a buffer amplifier with an input current of 0.1 microamp maximum at −20°C, it is necessary to use a Darlington connection at the input differential stage to the amplifier. Such an arrangement causes collector current to be so low that serious degradation in the gain-bandwidth product of the transistors results in poor performance of the buffer amplifier. Therefore, a basic tradeoff must be made between input current and bandwidth for any stable dc amplifier using bipolar transistors.

The solution:

A unity gain buffer amplifier with a field effect transistor (FET) differential input stage that responds much faster than bipolar transistors when operated at low current levels. The circuit illustrated uses a dual FET in a unity gain buffer amplifier having extremely high input impedence, low bias current requirements, and wide bandwidth. Input bias current is less than 10^{-8} amps maximum and bandwidth exceeds 2 mc while measured offset stability is −4mv at −20°C and +5mv at 85°C.

(continued overleaf)

Notes:

1. Adequate gain stability will be realized with this circuit only through use of a very stable constant current source.
2. Inquiries concerning this innovation may be directed to:

   Technology Utilization Officer
   Marshall Space Flight Center
   Huntsville, Alabama 35812
   Reference: B67-10334

Patent status:

No patent action is contemplated by NASA.

Source: Dynatronics, Inc.
under contract to
Marshall Space Flight Center
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