NASA TECH BRIEF

Analog Buffer Isolates High Impedance Source from Low Impedance Load

The problem:

Although there are many buffer amplifier circuits available commercially, a requirement has arisen that they do not satisfy. The requirement is for near complete isolation of a high impedance source from a low impedance load with temperature stability, linearity, and gain parameters not generally available in state-of-the-art circuitry.

The solution:

An analog buffer amplifier that essentially isolates source from load through an impedance ratio of approximately 200 million to one.

How it's done:

The problem of current gain (approximately 1%/°C) for small values of Ic is handled by having the Ic of the input stage held to a low level (approximately 450 nanoamps). The current is also held constant by the constant current source. The relative error introduced by current gain changes in this circuit is very small. The most significant source of error is the Delta Vbe/Delta T of the input stage transistor which is specified at 10 microvolts/°C differential voltage for the pair. This voltage is not compensated for and the differential voltage appears at the output as error. The high input impedance requirements of the buffer circuit, when used as an amplifier in the filter system, dictated the use of cascaded input stage transistors. With this configuration, the theoretical and actual input impedance is approximately 40 megohms. Resistor changes increase this value to approximately 80 megohms. The final configuration of the buffer circuit has been breadboarded, and bench and environmental tests conducted. Drift checks were made during three test runs. For each test run all active elements in the circuit were replaced with a new set. Each set of active elements was then tested three times at 50°F and 100°F. The mean average drift for nine tests with three sets of active elements was ±100 microvolts with the greatest recorded error being 200 microvolts. The testing was conducted in this manner to reduce the possibility of having a set of active elements that favored each other in producing a low drift characteristic. The output impedance was measured and found to be less than 0.2 ohm.

The linearity tests on the circuit were conducted in the same manner as the drift tests. That is, the active elements were changed for each test run and then several tests were conducted on each set of elements. The worst linearity deviation was 208 microvolts while the average for all tests was 131 microvolts; well within design specifications.

Notes:

1. This buffer amplifier exhibited the following characteristics:
   a. Temperature stability for 45°C change from ambient—0.004%
   b. Linearity from 0.0 to 5.0 volts—0.005%
   c. Gain—0.9984
2. Inquiries concerning this invention may be directed to:
   Technology Utilization Officer
   Marshall Space Flight Center
   Huntsville, Alabama 35812
   Reference: B67-10544

Patent status:

Inquiries about obtaining rights for the commercial use of this invention may be made to NASA, Code GP, Washington, D.C. 20546.

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Category 01