NASA TECH BRIEF

Improved Digital TV Encoding and Decoding System

An analog-to-digital coder and digital-to-analog decoder system has been designed to handle wide-band TV signals. The system incorporates solid state plug-in modular units which are mounted in standard 19-inch racks. By means of simple switch selection, the system may be operated in a VSD (Variable Slope Delta Modulation) mode or in the conventional one-bit DM (Delta Modulation) mode. When operated in its primary, VSD, mode, the system employs 4 encoding increments, with relative step sizes of ± 1, ± 2, ± 4, and ± 8. When operated as a conventional one-bit DM system, any one of the 4 increments may be selected. The system is capable of operating at a sampling rate of 30 MHz, which represents an advance over the prior state-of-the-art for VSD coders and decoders.

The input signal (a standard 1-volt peak-to-peak composite video) and the inverted predicted (quantized video) value are summed, resulting in a difference signal which is quantized in time and amplitude to form a polarity bit. When operated as a one-bit DM system, this polarity bit results in either a positive or negative pulse of current into the integrator which forms a new predicted value. The predicted value therefore represents a quantized version of the video signal. The polarity bit is transmitted to the decoder which is used to form an identical predicted value or quantized video signal. When operated in the VSD mode, pulses of ± 1, ± 2, ± 4, and ± 8 are used as determined by digital processing according to the present and past values of the polarity bit. The following algorithm describes VSD operation. On the third consecutive "same" polarity bit, increase the step size. Continue to increase the step size for a subsequent "same" polarity bit until the maximum step size is reached. When a polarity reversal occurs reduce the step size. For subsequent reversals, continue to reduce the step size until the smallest step size is reached. The technique employed to use the system as a conventional delta modulator is to lock up the reversing feedback shift register in the digital processor at a particular state. Thus a particular step size is always called for, its polarity determined by the polarity bit.

Notes:

1. A separate printed circuit plug-in test card is used to introduce either of two test patterns into the system. These test patterns are used for system setup, alignment, and troubleshooting.
2. Inquiries concerning this system may be directed to:

   Technology Utilization Officer
   Manned Spacecraft Center
   Houston, Texas 77058
   Reference: B67-10562

Patent status:

Inquiries about obtaining rights for the commercial use of this invention may be made to NASA, Code GP, Washington, D.C. 20546.

Source: A. R. Deutermann
of Philco-Ford Corporation
under contract to
Manned Spacecraft Center
(MSC-11147)

Category 01