DESIGN, DEVELOPMENT AND FABRICATION OF PROTOTYPE SEMICONDUCTOR AMPLIFIERS

Final Report
(17 March 1965 to 16 March 1966)

Contract NAS8-11861

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NASA

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FOREWORD

This work was performed at the Research Laboratories of Westinghouse Electric Corporation, Pittsburgh, Pennsylvania, for George C. Marshall Space Flight Center, National Aeronautics and Space Administration under Contract NAS8-11861.

The reported research was conducted from 17 March 1965 to 16 March 1966.

The Principal Investigator was Dr. Hung-Chi Chang, Manager, Compounds and Surfaces, Power Devices Research and Development, Westinghouse Research Laboratories.

The areas of research for this program and the professional personnel involved are listed below:

Amplifier Circuit Design	P. F. Pittman
Device and Process Design	H. C. Chang N. P. Formigoni J. S. Roberts
Crystal Growth	D. L. Barrett
Epitaxy	R. B. Campbell C. H. Lee
Crystal Evaluation	R. B. Campbell
Aluminum Diffusion	J. S. Roberts
Device Fabrication	N. P. Formigoni J. S. Roberts
Device Evaluation	N. P. Formigoni J. S. Roberts

Many other technical personnel of the Westinghouse Research Laboratories have participated in this program for consultation and professional services.

This final report was prepared and edited by H. C. Chang with the assistance of R. B. Campbell.

SUMMARY

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This report covers the results of the investigation in the fabrication of a high temperature silicon carbide (SiC) integrated circuit using the junction-gate type field-effect transistor (FET) as an active component. The modern photoresist masked-diffusion technique was utilized providing precise control in making the planar device configuration. Aluminum diffusion in SiC requires temperatures from 1800°C to 2100°C. At these temperatures only SiC itself proved effective as a diffusion mask. The self-masked diffusion process consists of the following steps: (1) growth of SiO_2 on the SiC, (2) photoresist etching of the SiO_2 to expose areas of designed pattern for chlorine etching, (3) chlorine etching of the SiC through the openings of the SiO_2 mask, (4) aluminum diffusion, the unetched SiC acted as a diffusion mask, and (5) removal of the SiC self-mask to obtain a planar structure.

Device fabrication techniques of high precision necessary for the self-masked diffusion process have been further investigated. A SiC platelet with an area of about 6 mm x 6 mm can be lapped with a parallelism precision of $\pm$ 1μ and a thickness precision of $\pm$ 7μ at a thickness of 52μ. Smooth chlorine etch surfaces have been obtained with less than 1μ texture at etch depths up to 20μ. A surface concentration of aluminum greater than 10^{18} cm^{-3} has been attained in SiC during diffusion and junction depths up to 38μ have been diffused with a precision of $\pm$ 1μ. In addition to its use as a chlorine-etch mask, the SiO_2 formation can be used for accurate junction delineation, face identification and removal of damaged material after mechanical polishing.

With the achievement of such precise techniques, a complete microelectronic process has been developed for the fabrication of SiC monolithic planar devices. The fabrication of FET from crystals of medium quality for the purpose of process evaluation has already yielded two transistors out of twenty possible devices from three crystals. These results have shown that this process is adequate for the fabrication of FET, resistors, and thus amplifiers containing FET and resistors.

Author

Table of Contents

LIST OF TABLES

LIST OF FIGURES

1. INTRODUCTION

Active and passive electronic components capable of operating at temperatures of 500°C and above are needed for the construction of power conditioning, control, and telemetric systems in space vehicles. These components must be of light weight, small size, low power consumption, high reliability and long life. In certain applications, these components must also be capable of withstanding a high energy, high density nuclear radiation flux.

Most such systems presently being used are based on silicon devices and are designed to operate at temperatures below 250°C and integrated neutron fluxes lower than 10^{14} evt. For space applications, these components must have adequate cooling and shielding from thermal and nuclear radiation. The penalty involved in the increase of size and weight of the electronic systems is severe.

There exist two approaches to the solution of this problem: high temperature ceramic tubes and wide-band-gap semiconductor devices. The first approach has its inherent drawbacks since ceramic tubes are bulky and usually have large power losses, slow speed, low reliability and short life in comparison with semiconductor devices. It is expected, however, that for very high power systems ceramic tubes may be favorable because of their high voltage capability. The second approach holds great promise, particularly for control systems and power conditioning systems of the medium power range. For low-power instrumentation and

telemetric systems, the second approach becomes unique since it can utilize the very important concept of integrated circuits. The development of wide-band-gap semiconductor integrated circuits can avoid the need for high temperature passive components, most of which are not available.

Hexagonal silicon carbide has a relatively wide energy band-gap (about 3.0 eV for 6H polytype SiC, compared with 1.1 eV for silicon). It can be made either n-type or p-type and is quite stable at elevated temperatures. The Westinghouse Research Laboratories has pursued a broad program of research in SiC technology, including crystal growth,[1-7] device fabrication,[6-23] investigation of basic properties,[24-43] and study of radiation effects.[15-17] The high temperature operating capability of SiC devices has been established. Devices developed at this laboratory include 500°C power rectifiers with 150 V peak reverse voltage and current ratings up to about 10A,[6] nuclear particle detectors operable up to 700°C,[15-17] and ultraviolet detectors showing responses of 1-100 mV near 2850 Å at 530°C.[20,21] Silicon carbide active devices have been shown feasible. A unipolar field-effect transistor of the junction-gate type has been demonstrated exhibiting a power gain at 500°C.[13,14]

The response of silicon carbide to nuclear irradiation has not been extensively studied. However, wide band-gap semiconductors, such as silicon carbide, should have a higher tolerance to nuclear radiation than silicon for two reasons: (1) a higher concentration of doping impurities can be used, and (2) appreciable thermal annealing

occurs at the operating temperature. Preliminary data on SiC nuclear particle detectors[15] have shown that annealing at temperatures up to 800°C for periods of one hour can restore over 70% of the initial collection efficiency and counting rate of the detector which had been irradiated with 2 Mev protons to the equivalent dosage of 10^{16} nvt. Recent data have also indicated that a SiC unipolar field-effect transistor of the junction-gate type should be operated up to an integrated neutron flux greater than 10^{16} nvt at 500°C.[18] It was revealed recently that the irradiation-produced defects which control carrier recombination appear quite different from the defects which control electrical conductivity.[17] The former anneal hardly at all and the latter anneal almost completely below 500°C. Based on this information, a SiC unipolar device should have a higher radiation resistance than a SiC bipolar device, operated at high temperatures since the operation of a unipolar device involves no carrier recombination mechanism.

The present program was initiated on the basis of the technological background discussed above, with the objective of demonstrating the feasibility of a high temperature SiC integrated circuit. The work has included the following areas:

1) Device Design - Design of the device structures and fabrication processes of a prototype SiC integrated amplifier, based on the use of a junction-gate type unipolar transistor as the active component, and taking into consideration the properties of the available SiC materials and probable fabrication technology.

2) Crystal Growth - Preparation and evaluation of high-purity hexagonal SiC platelets employing the state-of-the-art sublimation-growth

techniques.

3) Junction Formation - Studies of diffusion and epitaxy methods so that the junction profile required for the amplifier can be prepared.

4) Device Fabrication - Investigations of basic fabrication techniques--including mechanical shaping, thermal oxidation, chlorine etching, contacting, and device assembly--and development of processing procedures for the fabrication of a prototype SiC amplifier.

5) Device Evaluation - Measurements of the characteristics of the active and passive SiC components as well as the integrated circuit.

2. DEVICE AND PROCESS DESIGN

2.1 Circuit Design

Circuit design is an intermediate step which establishes the parameters required for the component design and the design of a realizable integrated structure having the required properties.

The electrical specifications for the designed amplifier are listed, as follows:

a) DC voltage gain: minimum of 10

b) Frequency response: 1 Mc or higher

c) Power supply: + 24 volts dc

d) Power output: 10 mW or higher

These specifications generally suggest a circuit containing at least one power amplifying device. The minimum gain required is sufficiently low that it should be satisfied by a well designed circuit containing a single active device. At the present state of development, the feasibility of such an amplifier should be demonstrated with a simple circuit which presents the minimum foreseeable difficulty in its fabrication. Such a circuit is shown in Figure 2.1 in which the single active device used is a junction-gate type unipolar transistor, and the only passive devices used are three resistors. Because of the exploratory nature of the work, efforts have been directed toward the design and fabrication of this simple circuit and corresponding integrated structure which satisfies the performance specification.

Classical circuit analysis shows that if separate components are connected together to form the circuit of Figure 2.1, an equivalent

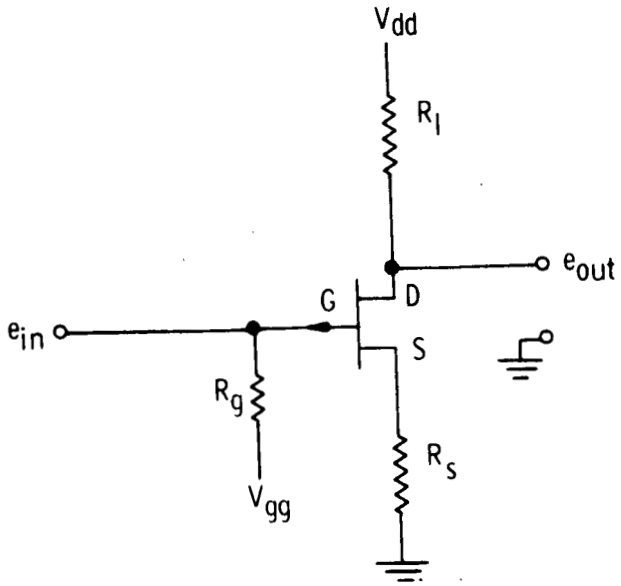


Figure 2.1 - Schematic diagram of an amplifier circuit

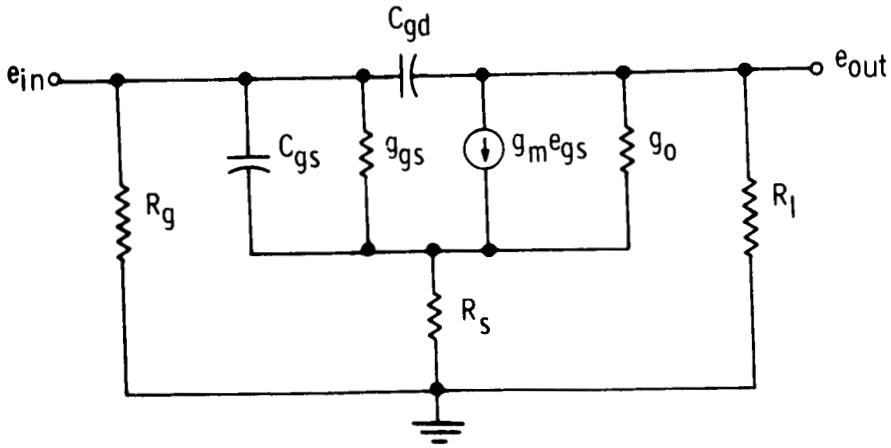


Figure 2.2 - Equivalent ac circuit for Figure 2.1

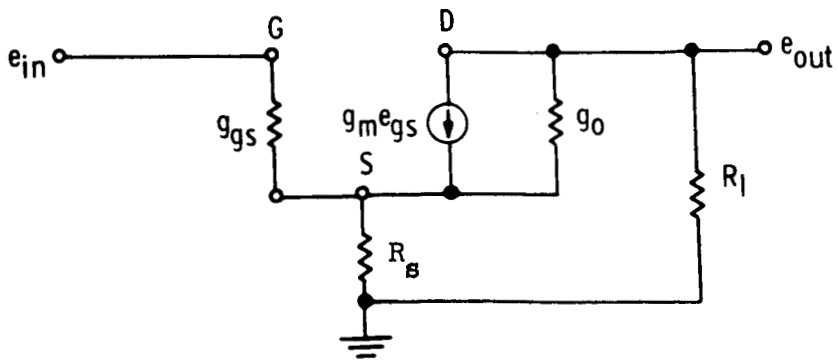


Figure 2.3-Midband approximate ac equivalent of Figure 2.1

circuit from which ac performance can be predicted is as shown in Figure 2.2. Furthermore, if certain reasonable assumptions are made concerning secondary effects, an even simpler equivalent circuit from which ac performance may be predicted at midband is shown in Figure 2.3.

Assuming that

$$R_g \gg R_\ell, \qquad g_m \gg g_o,$$

$$\omega C_{gs} \ll g_{gs}, \qquad g_o R_\ell \ll 1,$$

$$\omega C_{gd} \ll g_{gs}, \qquad g_m R_s \gg 1,$$

the ac voltage gain (A_v) of this equivalent circuit is:

$$A_v \cong R_\ell / R_s.$$

The mathematical derivation of this relation is given as Appendix A.

2.2 Transistor Design

The junction-gate type unipolar field-effect transistor can be regarded as a solid-state triode containing a semiconducting current path (instead of vacuum or gaseous), the conductivity of which is modulated by applying a transverse electric field. A structure suitable for analysis and design is shown in Figure 2.4. The device shown consists of a wafer of n-type semiconductor (in this case, SiC) with ohmic contacts at each end, and two p-type regions at the center of opposing faces. The ohmic contacts are called the "source" and "drain" and the p-type regions are called the "gates". The conducting layer between the gates is called the "channel".

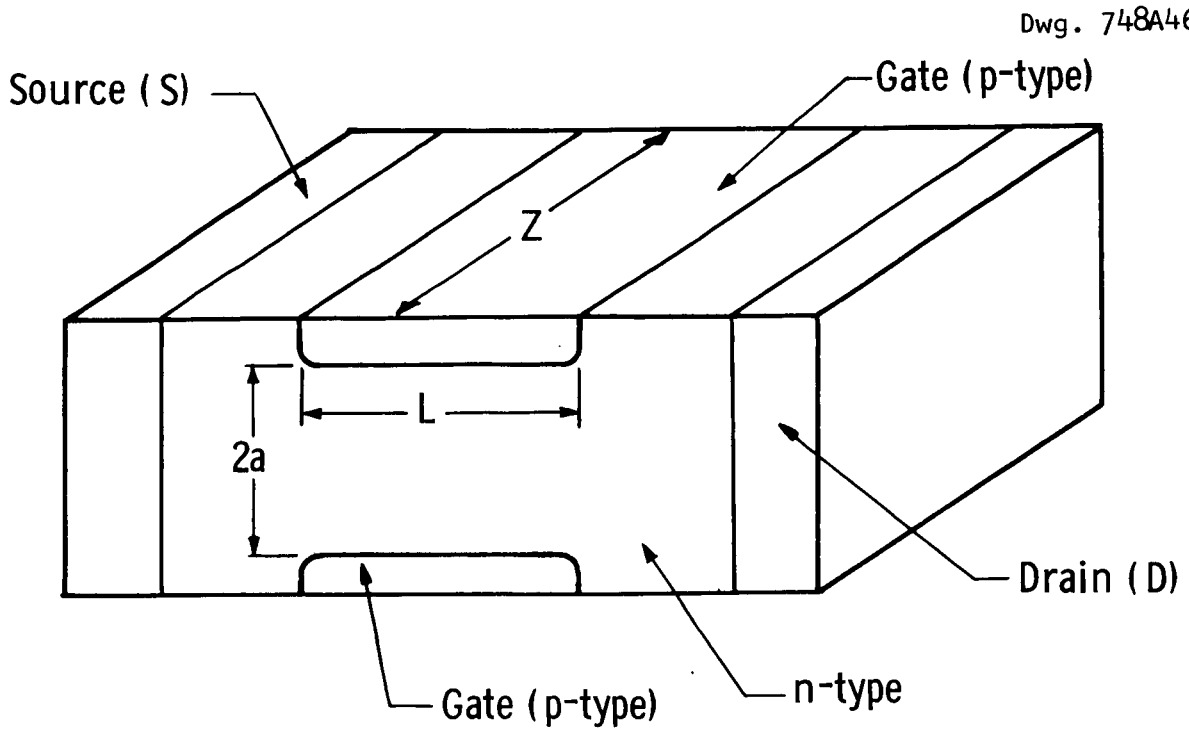


Fig. 2.4(A) – Schematic for describing the theory of its operation

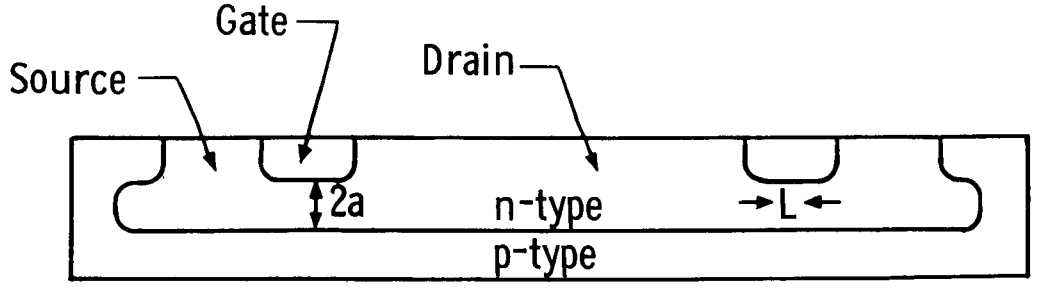


Fig. 2.4(B) – Section view of an actual device

Fig. 2.4 – Junction-gate type unipolar transistor

The theory of the unipolar transistor has been developed in detail by Shockley,[44] and Dacey and Ross[45] assuming that the gates are abrupt junctions. The equations derived from the theory are reproduced here. The structural parameters to be determined are the channel thickness, 2a; length, L; and width, Z. These are obtained in terms of the material properties and the desired operating voltages and currents. The following notations and units will be used.

N_o = ionized donor concentration of the channel material (cm^{-3})

σ = channel conductivity ($ohm^{-1}\ cm^{-1}$)

μ = electron mobility of the channel material ($cm^2\ volt^{-1}\ sec^{-1}$)

K = dielectric constant of SiC ($\cong 9 \times 10^{-13}$ farads cm^{-1})

q = electronic charge = 1.6×10^{-19} coulombs

W_o = pinch-off voltage (volt)

I_o = drain current at pinch-off for $V_G = 0$

V_G = gate voltage (volt)

V_D = drain voltage (volt)

I_D = drain current (amperes)

f_{max} = maximum operating frequency (cycles per sec)

P_{DO} = maximum power density ($watts/cm^2$)

P_o = maximum device power (watts)

The channel thickness, 2a, is given by:

$$2a = 2(2KW_o/qN_o)^{1/2} = 6.7 \times 10^3 (W_o/N_o)^{1/2} \text{ cm} \qquad (2.2.1)$$

This relationship is shown graphically in Figure 2.5. For a channel material of $N_o = 10^{15}$ cm^{-3}, along with a pinch-off voltage of 25 volts, a channel thickness of 10 microns is obtained. The channel thickness will be only about one micron for a channel material of $N_o = 10^{17}$ cm^{-3} with the same pinch-off voltage.

The ranges of donor concentrations and channel thickness in Figure 2.5 are within the capability of the present methods of crystal growth and junction formation.

The remaining dimensions of the device, the channel length, L; and width, Z; can be determined from Equations (2.2.2), (2.2.3), (2.2.4), and (2.2.5).

$$I_o = 2\sigma W_o aZ/3L \tag{2.2.2}$$

$$P_{DO} = 2\sigma W_o^2 aZ/3L^2 \tag{2.2.3}$$

$$P_o = I_o W_o = P_{DO} LZ \tag{2.2.4}$$

$$f_{max} = (\sigma/4\pi K)(a/L)^2 \tag{2.2.5}$$

These equations are inter-related and therefore can be used in several ways depending on limiting parameters and the parameter to be optimized. The limiting parameters involve the channel dimension and crystal quality. For instance, the tolerance of the gate contact area dictates the channel length to be no less than 50 microns. These parameters are listed as follows:

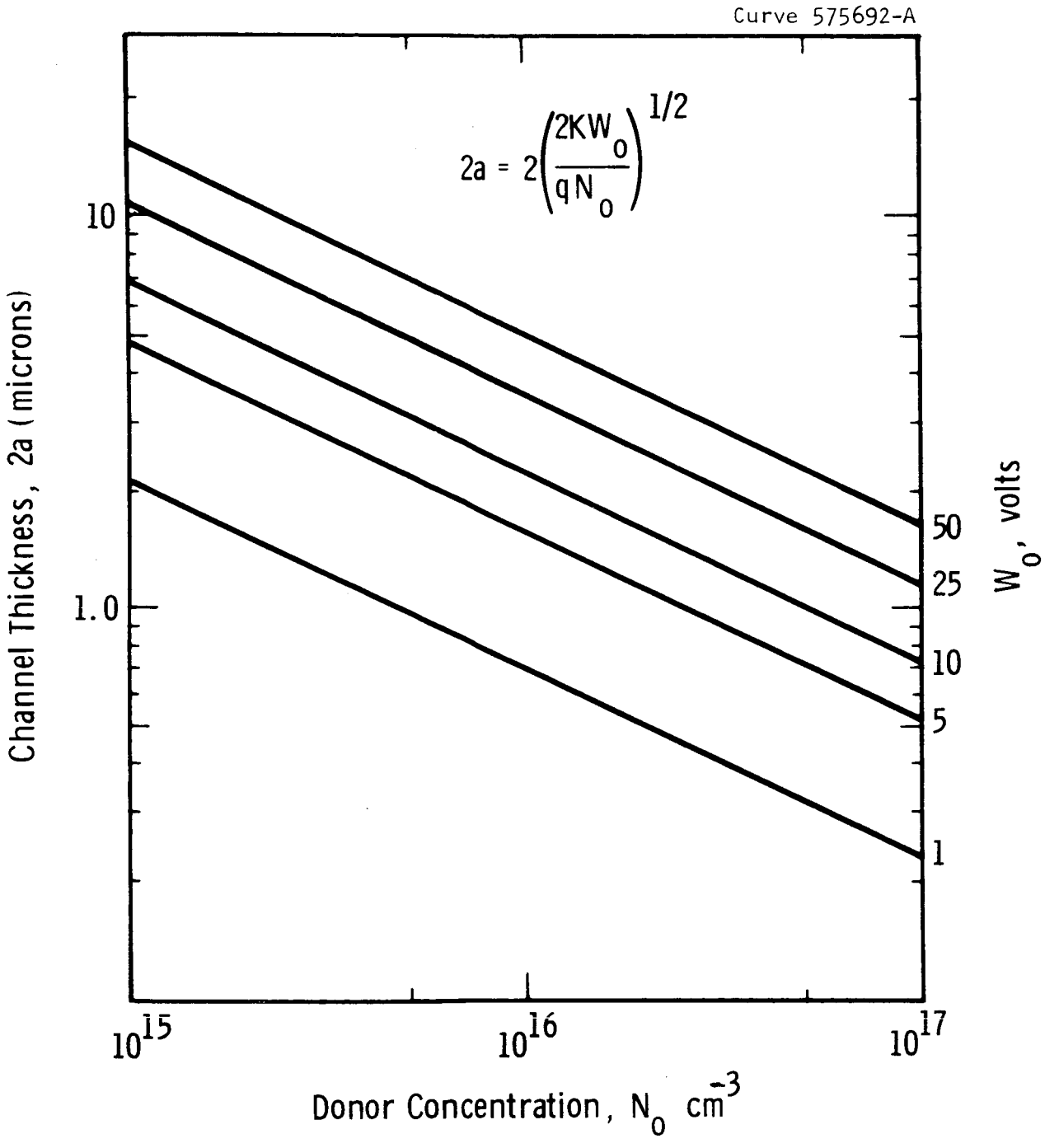


Figure 2.5 - Channel thickness as a function of donor concentration and pinch-off voltage, for the abrupt gate junction case

$L \geq 50$ microns

$2a \geq 2$ microns

$N_o \geq 10^{16}$ cm^{-3} at 500°C

$\mu \leq 40$ cm^2 volt^{-1} sec^{-1} at 500°C

Based on these parameters, the device design data can be calculated and these data are listed in Table 2.1.

Table 2.1 Design Data for SiC Unipolar Transistor

Donor Concentration of the Channel Material, N_o	$\geq 10^{16}$ cm^{-3}
Electron Mobility of the Channel Material at 500°C, μ	≤ 40 cm^2 volt^{-1} sec^{-1}
Channel or gate Length, L	≥ 50 microns
Channel or gate Width, Z	2 mm
Channel thickness, 2a	3 microns
Pinch-off voltage, W_o	20 V
Maximum drain current, I_o	5 mA
Maximum Power Density, P_{DO}	100 W cm^{-2}
Maximum Device Power, P	100 mW
Cut-off frequency, f_{max}	5 Mc sec^{-1}

It should be pointed out that the data presented above were based on the donor concentration and electron mobility of the channel

material of a fabricated device, and cannot be used for designing the device dimension and characteristics based on the starting crystal properties, without taking into consideration the fabrication process. At the present state of development, the aluminum-diffused junction in SiC is always graded, and the diffusion tail beyond the junction would compensate the channel region appreciably. Thus, a channel with a lower effective donor concentration than the starting crystal can be achieved. In other words, the compensated channel would allow a larger channel thickness with the use of starting materials having a higher donor concentration. This is advantageous since high purity SiC crystals presently grown have net donor concentrations around 10^{17} cm^{-3} with which the channel thickness would become very small.

A quantitative graded junction theory has been derived[18] assuming that the acceptor distribution consists of two exponential and symmetrical distributions extending into the crystal from opposite parallel faces. The two distributions form two gate junctions and the two diffusion tails overlap to produce the total acceptor concentration. This theory is more complex mathematically than the abrupt junction theory. The calculation was made through a Burroughs B5500 computer at the Research Laboratories. Detailed data are available in the reference report.

At the present state of SiC diffusion technology, the use of this quantitative graded junction theory is hardly needed. As will be described later, the diffusions into opposite parallel faces of the

crystal are usually not symmetrical, and during the fabrication process several diffusions are performed under differing conditions. The control of the device structure requires step-by-step evaluations. The processing parameters are dependent rather on experimental data and cannot be represented by such a quantitative theory.

Based on the diffusion data the junction depth and the net donor concentration in the channel region can be determined. The simpler abrupt junction-gate theory would provide sufficient information of the required channel dimension and transistor characteristics for controlling the processing parameters.

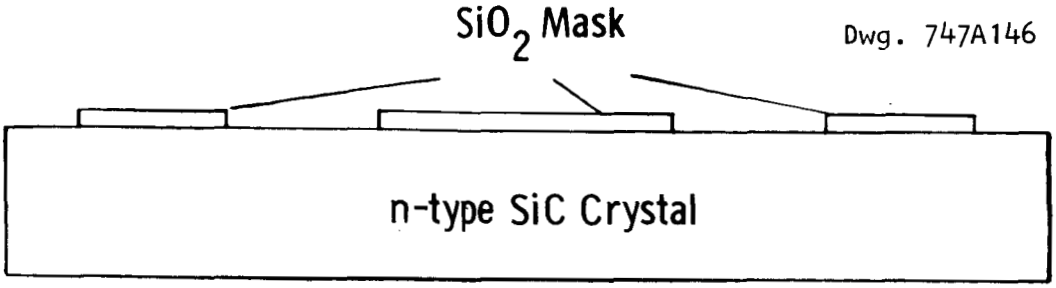
The design data clearly indicate the need for precise dimensional control in making the transistor. This requirement led to a fabrication plan based on the modern photoresist diffusion mask approach employed for silicon planar devices and integrated circuits.

Aluminum diffusion in SiC requires temperatures from 1800°C to 2100°C. At these temperatures, only SiC itself proved effective as a diffusion mask. The self-masked diffusion process developed in this laboratory[18] is illustrated in Figure 2.6 and consists of the following steps:

1) Growth of SiO_2 over the entire carbon-face surface of the SiC crystal by the conventional steam oxidation technique,

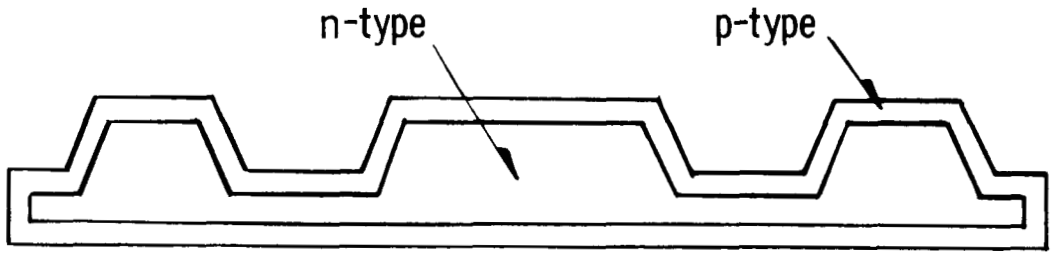
2) Photoresist etching of the oxide layer to expose areas for chlorine etching of the SiC,

3) Chlorine etching of the SiC through the openings of the SiO_2 mask,

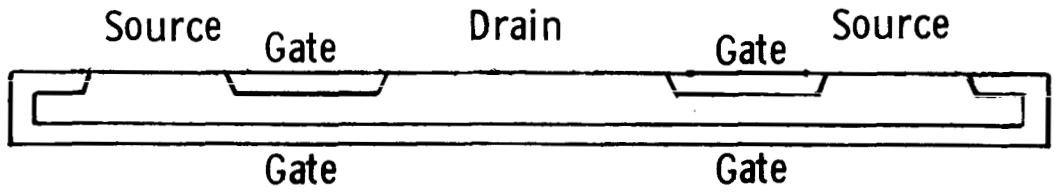


(a) Section view, oxide mask after photoresist etch

(b) Following Cl_2-O_2 etch and removal of oxide



(c) Following diffusion of p-type impurity



(d) "Self-mask" removed leaving finished structure

Figure 2.6 – Schematic representation of method for making SiC unipolar transistor by "self-masked" diffusion

4) Aluminum diffusion,

5) Removal of the SiC self-mask to obtain a planar structure.

This "self-masked" diffusion process is a key technology which contributes to the success of achieving precise control of the device structure. The basic processes are discussed in detail in Sections 3 and 4.

2.3 Resistors Design

The simple amplifier circuit involves three resistors of different values, designated as R_g, R_ℓ and R_s, as shown in Figure 2.3. According to the design data listed in Table 2.1, the maximum power dissipation of the transistor $\doteq$ 100 mW, maximum drain current $\doteq$ 5 mA, and voltage gain = 10, i.e. $R_\ell = 10\ R_s$.

In order to find R_s we assume that 20 mW of the total 100 mW power be dissipated in the R_ℓ and R_s resistors, then R_s should have a value of 80 ohms approximately, and accordingly, R_ℓ = 800 ohms and R_g = 8000 ohms. The actual value of R_s may vary from 80 ohms to 800 ohms depending on the selected values of the maximum drain current and power dissipation. In any way, the resistors will involve three orders of magnitude variations. In order to achieve such large variations, a parallel layout of the crystal areas for the lowest value resistor and a series layout for the highest resistor value, with intermediate layout for the value in between have been considered in Figure 2.7(A); however improvements will be made, if necessary, in order to minimize parasitic capacitances. In the first approach to the resistors design the n-type crystal itself will be adopted as resistors material. The

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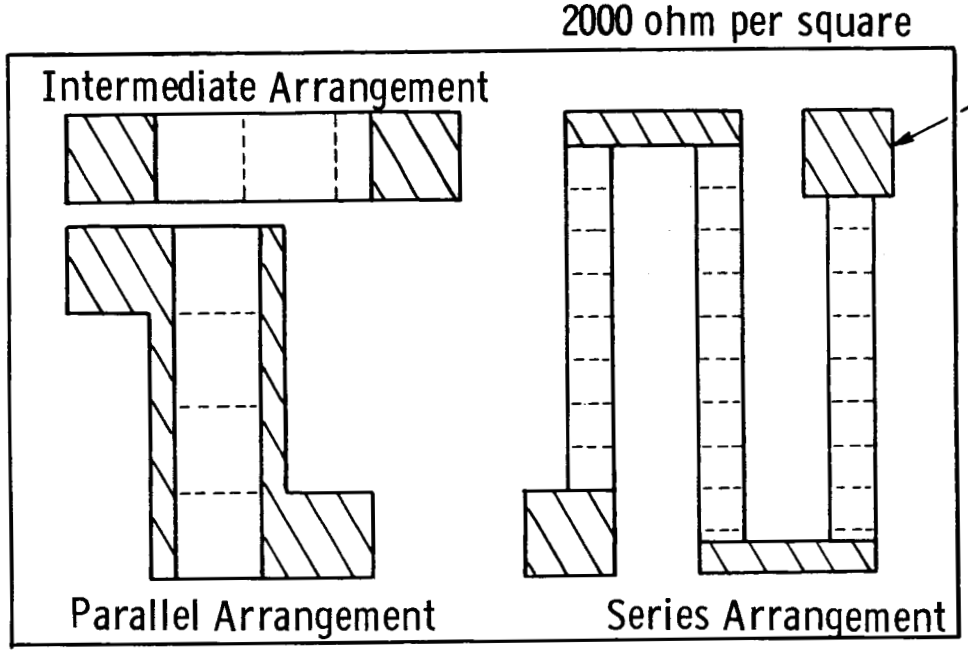
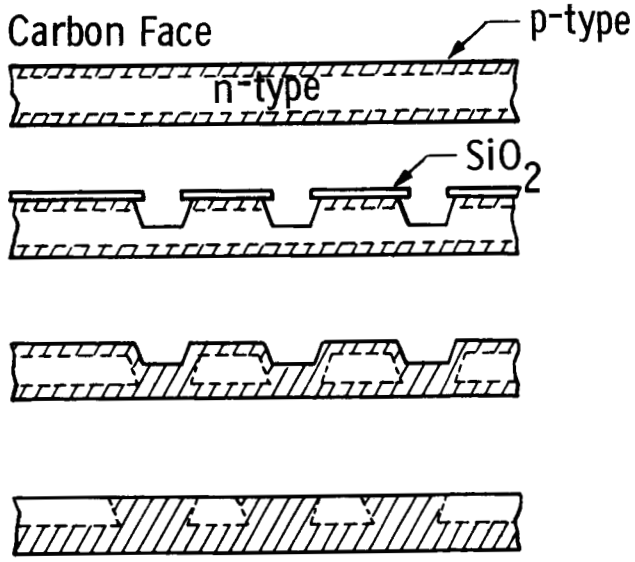


(A)



(B)

Acceptors diffused in both sides of parallel polished SiC crystal

SiO_2 masked, photoengraved, selectively chlorine etched as per resistors pattern

Acceptors diffused in order to isolate resistors

Planar polishing, passivation, metalization of terminals

Fig. 2.7—Resistors network design

(A) schematic layout of array of resistors for the SiC integrated amplifier

(B) outline of process for obtaining compatible, bulk, N-type resistors in SiC planar functional blocks

justification of this approach rests mainly in the fact that the electrical properties of the high purity crystal are comparatively well characterized in a large temperature interval. As accurate data on the resistivity of p-type materials are available, the same design can be applied to the p-type material.

The relatively large temperature coefficient of resistivity of SiC should be considered as an important design parameter. The temperature variations of bulk resistivity of high purity, n-type silicon carbide crystals are accurately measured in a relatively routine fashion in this laboratory. A typical set of conductivity data for high purity n-type crystal is given in Table 2.2

Table 2.2 Variation of Bulk Electric Conductivity with Temperature in High Purity, N-Type SiC Crystals

Temperature (^{o}K)			
resistivity (ohm-cm)	0.680	4.350	10.600
conductivity (ohm^{-1} cm^{-1})	1.470	0.230	0.094

The change in resistivity is indeed a large one, compared to the tolerances normally accepted for electronic components. However, the actual variation of resistance of the resistors may be reduced because of the heating in the resistor as well as at the junction.

One of the possible processes for fabricating a monolythic array of dc isolated resistors is illustrated in Figure 2.7(B). This process is again based on the "self-masked" diffusion technique. The

crystal is lapped plane parallel like in the transistor process, and given a deep background acceptor diffusion. Following diffusion depth evaluation the crystal is oxidized, photoresist masked and chlorine etched over the isolation area regions. Later on, acceptors are diffused again in the crystal so that the entire isolation area is converted to p-type conductivity.

The chlorine etch should be deeper in the crystal than the junction boundary over the n-type material, after the second acceptor diffusion. When subsequently the upper part of the crystal is removed by parallel lapping-polishing no residual p-type material will be left on top of the n-type regions which will be isolated from each other by converted p-type crystal.

Like in the case of the transistor, a nearly planar structure will be available for processing according to planar techniques. Electrical terminals will be photoengraved on the resistor with a process identical to the one for the transistor.

3. BASIC TECHNIQUES

3.1 Introduction

The major techniques involved in the development of a SiC amplifier are crystal growth, mechanical processing, junction formation, oxidation, chlorine etching, alloying and encapsulation.

The sublimation-growth method has been extensively investigated and has successfully produced SiC crystals of device quality. Several other methods of producing large SiC crystals have been investigated in various laboratories. None of these methods has resulted in hexagonal SiC crystals of a quality even close to that grown by the sublimation method.

Recent improvements made in the growth process have resulted in further reduction of the total impurity concentration.[7] Pure n-type crystals have been produced with a net donor concentration of about 10^{17} cm^{-3} and electron mobilities up to 500 cm^2 $volt^{-1}$ sec^{-1} at room temperature. Crystals having lower donor or acceptor concentrations are largely due to compensation and actually not of high purity.

The crystals used for device fabrication have nominal values of ionized donor concentration of 1-3 x 10^{17} cm^{-3} and electron mobilities of about 300 cm^2 $volt^{-1}$ sec^{-1} at 25°C and 40 cm^2 $volt^{-1}$ sec^{-1} at 500°C.

During the early stages of the program it was planned to use epitaxial growth techniques to form one or more of the junctions. However, an all diffused junction structure was adopted for the final design for the following reasons:

1) Suitable p-type epitaxial layers could not be grown by the thermal reduction technique. It was not possible to grow aluminum-doped epitaxial layers, and although boron-doped layers were prepared, there is insufficient information concerning boron as a dopant.

2) Epitaxial layers of the highest quality could be grown only on the "silicon" face of the SiC crystal. The layers grown on the "carbon" face were generally of poorer quality. Most of the fabrication procedures to be described later require processing of the "carbon" face.

3) The epitaxial junctions at the present state-of-the-art are inferior to the diffused junctions.

4) The epitaxial growth technique was not as reproducible as the diffusion process.

Crystal growth was not an integral part of this program, and the work was supported mainly by the Air Force Avionics Laboratory under contracts AF 33(615)-2363 and AF 33(615)-1440. The epitaxial growth study was also supported jointly with the Air Force.

A comparatively detailed description of the growth of SiC crystals by the sublimation method, the epitaxial growth of SiC by the thermal reduction technique and the electrical and optical characterization of the crystals and epitaxial layers is given, respectively, in Appendix B, C and D. The basic device fabrication techniques are described in the following sections.

3.2 Mechanical Processing

Silicon carbide platelets as obtained from the growth furnace vary in size and thickness. For device use, these platelets should be cut, if necessary, and lapped to a specific dimension with a very small tolerance. Since silicon carbide has a hardness of about 9.5 on a diamond scale of 10, the mechanical processing is always carried out with boron carbide grit from No. 280 to No. 1000 and finally polished with 5 to 1/4 micron diamond paste.

For this program, it is required to lap an area of about 6 mm x 6 mm with a parallelism tolerance of $\pm$ 7μ at a thickness of 52μ. In order to achieve this precision, a special lapping jig, designed and fabricated in these laboratories, was used. This jig is shown in Figures 3.1 and 3.2. Figure 3.1 is the mounting jig which allows the crystal to be positioned flat and parallel to the plane of the lapping surface. If desired, several crystals can be mounted at one time. Since a thickness precision of $\pm$ 7μ is needed, precision shims are inserted between the lapping fixture and the weight so that the lapping automatically stops at the proper thickness. (See Figure 3.2) For the lapping of the upper surface to obtain a planar device, the crystal is examined during the operation and the lapping stopped when all the source drain and gate surfaces are exposed and planar.

A second method has been utilized to lap down to the upper gate region. This process, which removes only a few microns, is especially difficult since sufficient material must be removed to permit metallization and contacting, yet preserve the integrity of the individual devices.

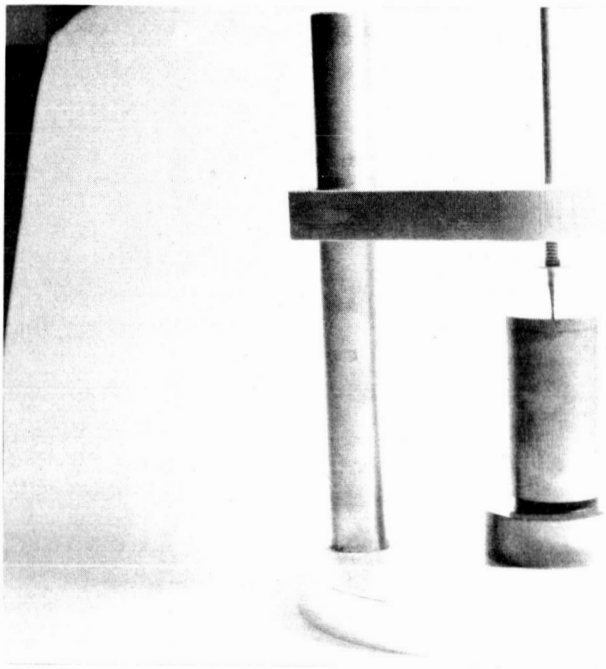


Figure 3.1 Parallel Lapping Jig with Mounting Fixture

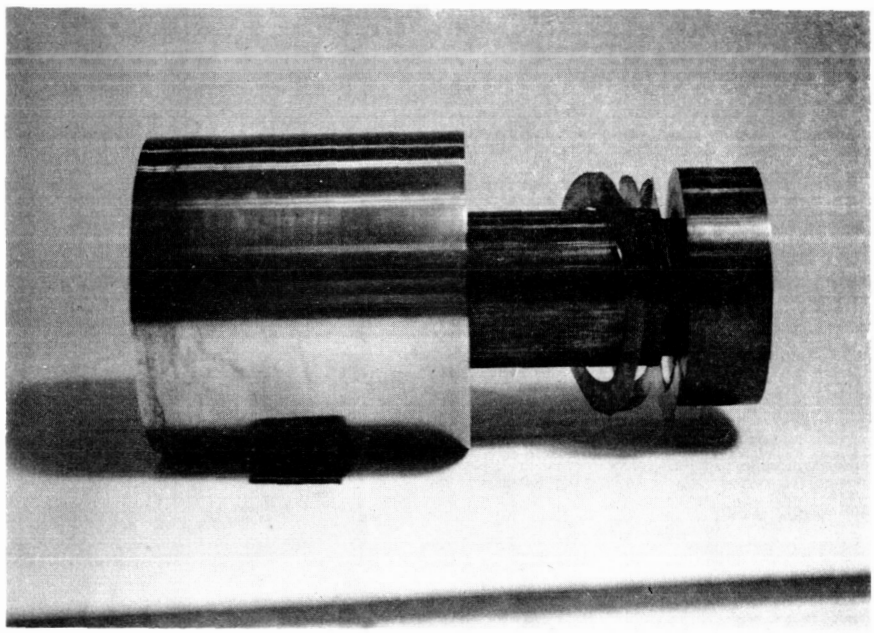


Figure 3.2 Parallel Lapping Jigs with Precision Shims

This has been accomplished by mounting the crystal (parallel) with the bottom on a plate glass and lapping the upper surface (gate region) by hand using a glass slide. A small amount of slurry (800 mesh boron carbide) is put on the crystal and the glass slide carefully moved back and forth over the device area. If the glass slide is pressed tightly to the crystal, the device configuration is visible and depth of lapping together with the planarity can be continuously checked.

During many of the fabrication procedures, the device crystal is less than 40 microns thick, therefore extreme care must be taken in handling to prevent breakage. It has been found most feasible to use vacuum tweezers for this purpose. Crystals less than 25 microns thick have been handled in this manner (e.g., diffused, lapped, photoresisted, contacted, etc.) without undue strain.

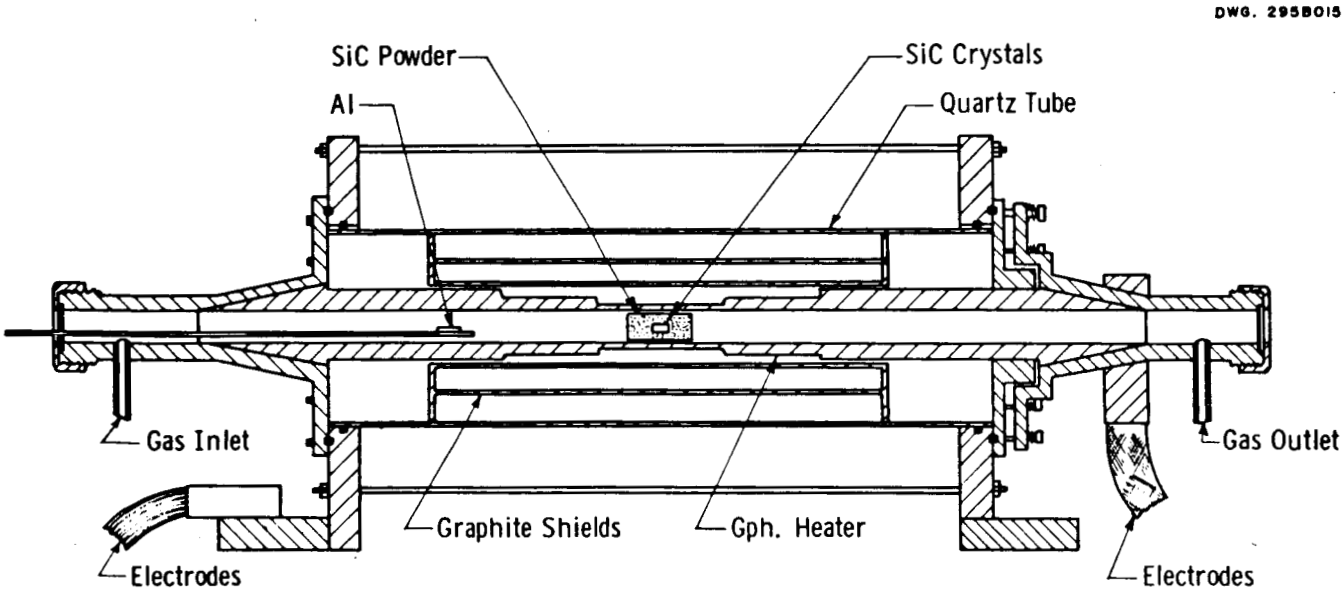


Figure 3.3 High Temperature Vacuum Tight Diffusion Furnace

3.3 Aluminum Diffusion

The aluminum diffusion process is of first importance in the fabrication of the field effect transistor and the associated resistors. A large effort [in part supported by contracts AF 33(615)-1440 and AT(301)-3405][18,19] was therefore expended to achieve a process sufficiently reproducible for a) precision control of the junction depth, and b) control of the diffusant concentration. Both conditions are necessary for the formation of the small channel thickness.

There are four basic requirements for any diffusion process.

1) An ambient condition for the crystals such that the surfaces of the crystals are maintained,

2) A diffusant in a proper thermodynamic form such that diffusion can take place,

3) Proper temperature such that diffusion proceeds at a significant rate,

4) A "clean" ambient such that diffusion of unwanted impurities does not take place.

Aluminum diffusion in SiC was first achieved in 1958 by H. C. Chang and L. F. Wallace.[12] The furnace used is shown schematically in Figure 3.3. It is of the open tube-carrier gas type. The water cooled electrodes are separated by a quartz cylinder which also acts as a vacuum envelope. The heater was a graphite cylinder, thinned at the center to provide a uniform hot region.

SiC has a significant vapor pressure at the temperature required for aluminum diffusion (1800 to 2000°C), and therefore the crystals must be diffused in a cavity surrounded by Si and C vapor species to minimize sublimation. To reduce transport of SiC inside the cavity the temperature gradient in the diffusion cavity must be very small.

The diffusant source used was 99.999% aluminum contained in a high purity boron nitride crucible which had been boiled in methanol to remove the boron oxide binder. The loaded crucible was placed upstream in the gas flow system from the SiC crystals to be diffused. The temperature of the diffusant source was usually between 1450°C and 1650°C and was not considered critical by Chang and Wallace. The carrier gas was argon containing 5% by volume of hydrogen, however, pure argon gas was used at various times in the course of the experiments. Before being used for diffusion the furnace is degassed at high temperature to remove volatile impurities inside the furnace.

The crystals are prepared for diffusion using the following cleaning procedure:

1) Trichloroethylene ultrasonic degrease - 1 minute
2) Mixed Acids - ultrasonic - 1 minute (50% deionized H_2O, 25% HCl and 25% HNO_3
3) Deionized H_2O rinse
4) HF ultrasonic - 1 minute
5) Deionized H_2O rinse
6) Acetone rinse

The crystals were stored in clean bottles until used for diffusion.

After loading, the furnace is evacuated to about 5×10^{-5} torr and the temperature raised to 1200°C. The furnace is then backfilled with the Ar-H_2 gas and a gas flow of 760 cc/minute for 15 minutes. The temperature is then raised to the diffusion temperature (1850°C - 2000°C) with the gas flow reduced to 350 cc/minute. The maximum operating temperature of the furnace is about 2100°C.

The development work in this program concerning diffusion may be divided into the following areas:

1) Attainment of a sufficiently high surface concentration (N_s) that base crystals having carrier concentration near 10^{17} cm^{-3} at 25°C could be diffused to reasonable depths (up to 38 microns) in reasonable time (up to 40 hours),

2) Purification of the system so that the diffusion ambient is clean and the aluminum vapor is not lost by reaction with contaminants,

3) Changes in the geometry of the crystal holder so that the surfaces of the crystal remain stable,

4) Refinements of the techniques for delineating the diffused junction.

These areas will be discussed in turn.

The net donor concentration of most of the crystals used for device fabrication is near 5×10^{17} cm^{-3}. Therefore a surface concentration of aluminum significantly higher than 5×10^{17} cm^{-3} is needed. Curves[52] plotted from a computer solution of the diffusion equation (assuming a complementary error function and the D_o and activation energy determined by Chang and Wallace[12]) are shown in Figures

3.4 a and b for 2000°C and indicate that a surface concentration near 10^{18} cm^{-3} is required for reasonable diffusion times and temperatures.

When this program was initiated, the results of Chang and Wallace[12] could not be reproduced. In some cases, junctions could not be delineated, and when junctions were obtained, the results could not be repeated. The diffused junctions which were obtained at diffusion temperatures of 2000°C had a calculated surface concentration of about 2×10^{17} acceptors/cm^3 which is much lower than that obtained previously. Surface concentrations of this magnitude are insufficient since the background concentration of the starting crystals is near 10^{17} donors cm^{-3}.

Evaluation of a diffusion run was based mainly on the junction depth obtained for a given time and temperature and background concentration (N_B) in the crystal. N_s was determined from these data using the activation energy and diffusion constant of Chang et al, and assuming a complementary error function profile. N_B for the diffused crystals was inferred from Hall and resistivity measurements on crystals from the same run.

A number of experiments arrived at increasing the surface concentration were carried out but a significant increase (up to 3×10^{18} cm^{-3}) was achieved only when the furnace was saturated with aluminum and all contaminants were removed from the furnace. The saturation was accomplished by evaporating a relatively large quantity of aluminum ($\sim$ 8-10 gms) inside the furnace. This aluminum apparently reacted with the graphite heater and graphite shields forming aluminum

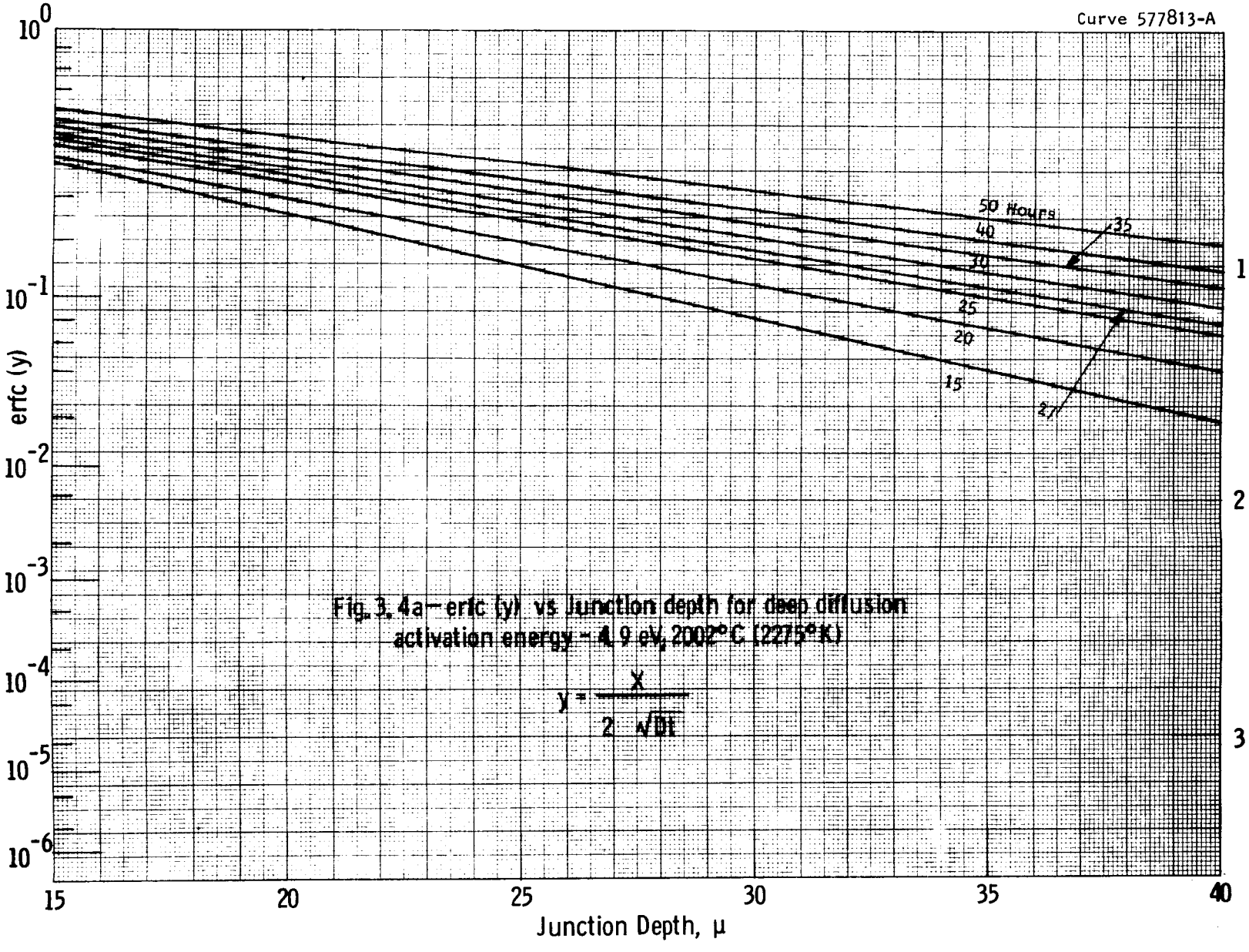
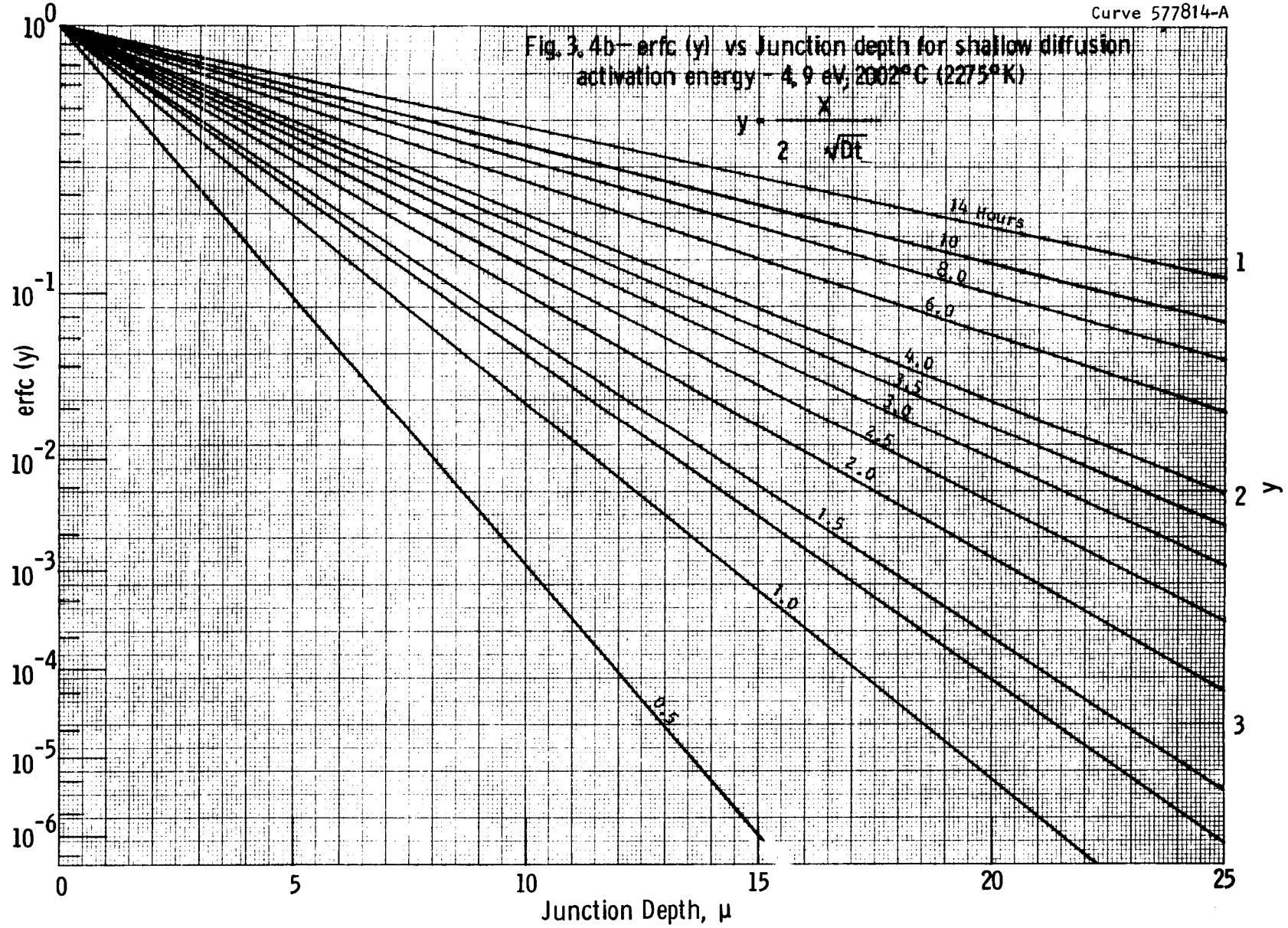


Fig. 3.4a – erfc (y) vs Junction depth for deep diffusion activation energy – 4.9 eV, 2002°C (2275°K)

$$y = \frac{x}{2\sqrt{Dt}}$$


Curve 577814-A
Fig. 3.4b – erfc (y) vs Junction depth for shallow diffusion
activation energy – 4.9 eV; 2002°C (2275°K)
$y = \frac{X}{2\sqrt{Dt}}$
14 Hours
10
8.0
6.0
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
erfc (y)
10^{0}
10^{-1}
10^{-2}
10^{-3}
10^{-4}
10^{-5}
10^{-6}
0
5
10
15
20
25
Junction Depth, μ
1
2
3
y

carbides. It is assumed that during the diffusion experiments aluminum vapor from the decomposing carbides as well as aluminum vapor from the diffusant source were available for diffusion.

During early diffusion experiments, some difficulty was experienced with contamination of the source.

Either of two types of results were observed: 1) the aluminum source was covered with various compounds of Al, B, N_2, C and O_2 after diffusion and there was a weight gain of the source material with little or no diffusion being observed, or 2) a significant weight loss of the aluminum source was observed (10 to 20 mg/hr), but the surface concentration was very low ($\sim 2 \times 10^{17}$ acceptors-cm^{-3}). The latter was generally obtained with high flow rates of gas (> 1/2 liter/min). Also in the latter case, a "cottony froth" deposited in the diffusion tube downstream from the crystal boat at a temperature of about 1400°C. X-ray analysis of this deposit showed that it was a complex of aluminum carbide and aluminum oxide.

In view of the significant weight loss of the source and the abundant deposition of the complex, it was hypothesized that the aluminum was in this complex form in the vapor phase and was unavailable for diffusion. One obvious solution would be to eliminate O_2 from the system. The furnace is usually run at a slight positive pressure of ambient gas making entry of O_2 or H_2O from the outside ambient unlikely, nevertheless, leaks were eliminated from the system which improved the vacuum to 2×10^{-6} torr (nearly 2 orders of magnitude improvement) before backfilling with pure argon.

The gas flow system utilized a dry ice-acetone cold trap for H_2O removal with a rather complicated valving system. The bottled gas available today is, in general, of higher purity (< 5 ppm O_2, 2 ppm H_2O) than that used in the original diffusion work of Chang and Wallace.[12] In order to eliminate a large amount of plumbing from the input gas system, diffusion was attempted using a direct flow of high purity argon as the ambient gas (i.e., no trap and a single valve with flow monitored at the furnace exit). The complex was still formed; however, a slight improvement in surface concentration was observed and the source aluminum had a metallic appearance.

5% H_2 was then added to the Ar gas (original process) to determine if it might prevent the complex from forming. The result was that the complex disappeared completely (in diffusions up to 6 hours) with a small amount of deposition in a 24 hour run. The surface concentration was also increased to about 2×10^{18} cm^{-3}.

To improve the surface stability of the crystals during the diffusion process, the geometry of the crystal holder was modified. In place of the graphite and SiC grain geometry shown in Figure 3.3, a solid, porous cylinder of SiC (taken from a sublimation growth charge) was used. The sublimation growth charge was machined into the form of a solid cylinder approximately 1-1/2" long and 1" in diameter (the I.D. of the diffusion tube is approximately 1-1/8" in diameter). A 1/2" diameter hole was then bored perpendicular to the axis of the SiC cylinder about 3/4" from one end. The crystals were mounted in the hole with aquadag such that the large area faces of the crystal, faced

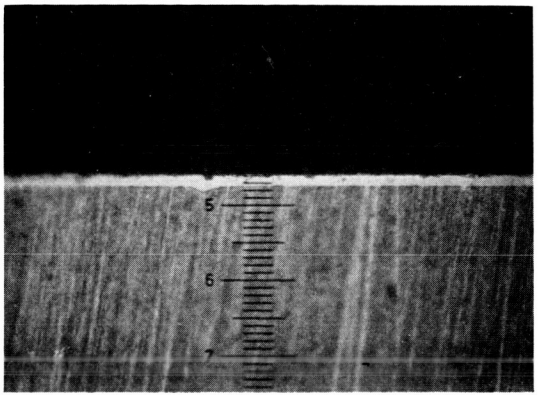
the hot graphite heater (i.e., the plane of the platelet is parallel to the axis of the cylinder). Diffusion for 10 hours at 1950°C under these conditions resulted in no detectable change in surfaces.

The surfaces were checked by diamond scribing and breaking off a piece of the crystal before diffusion. The diffused and undiffused pieces were fitted together after the diffusion and compared under a high power microscope (450X). (The sensitivity of this method is about 1 micron.)

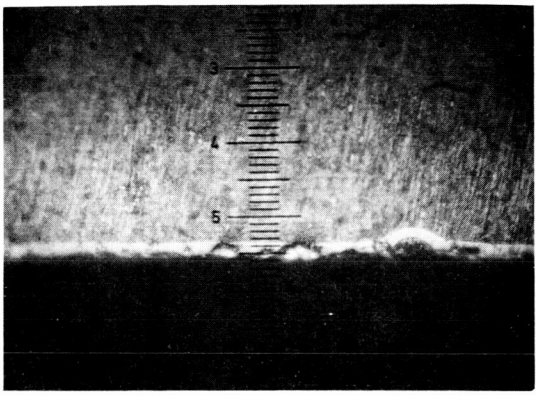
Figure 3.5 shows a diffused, delineated junction in an SiC crystal. The diffusion front is quite uniform, and the surfaces of the crystals are essentially unchanged from their pre-diffusion state.

The diffused junctions are generally delineated by electrolytically etching in a HF-alcohol mixture. The standard etching solution is 0.3 cc 49% HF to 50 cc alcohol although the relative concentrations are adjusted according to the resistivity of the crystal to achieve efficient etching. The crystals shown in Figure 3.5 were etched in this manner.

The second delineation technique utilizes the difference in oxidation rates of p-type and n-type material. This method is described in Section 3.4.



(a) (Upper)



(b) (Lower)

Figure 3.5 Aluminum diffused junctions on upper (a) and lower (b) surfaces of SiC crystal

3.4 Oxidation

Silicon dioxide can be grown on SiC by a method similar to the one used for the growth of SiO_2 on silicon crystals. Oxidation takes place at 900° to 1200°C in a carrier gas such as argon or oxygen saturated with water vapor at 100°C.[18,22] The oxide is found to grow at a significantly different rate on the carbon face of the SiC surface as compared to the growth rate on the silicon face, the growth rate being approximately 6 to 7 times faster on the carbon face. In addition the growth rate of the oxide on the carbon face of the SiC surface is significantly slower than that on silicon crystals, but appears to obey the same square law found for the growth rate on silicon.

In order to have better control of the various processes in which the SiO_2 layer is used in the fabrication of the unipolar transistor, a number of experiments on the growth of SiO_2 on the carbon face of SiC were performed, as well as the etching rate of this oxide in the buffered HF etch routinely used in the photoresist process. The data from these experiments are given in Table 3.1.

The thickness of the oxide was determined by interference fringe counts using a sodium light and taking 1900 Å per fringe. The fringe counts were calibrated using a silicon wafer oxidized at the same time. The error introduced by the phase of the zero order fringe resulting from the difference in the indices of refraction of Si and SiC was neglected, and the index of refraction of oxide grown on SiC was assumed to be the same as that grown on silicon.

Table 3.1

GROWTH OF SiO_2 ON CARBON FACE OF SiC AT 1173°C
AND ETCHING RATE OF SiO_2 WITH BUFFERED HF SOLUTION AT 25°C

Run No.	Oxidation Time (hours)	Carrier Gas Flow = 120 cc/min	Thickness (Å)	Etching Rate of SiO_2 in Buffered HF (Å/min)
2	11.25	Ar	17,000	980
4	15.0	Ar	20,900	860
5	11.0	O_2	17,050	875
6	1.7	Ar	5,400	830

The oxidation of SiC follows the same parabolic law of the oxidation of Si, viz:

$$\log d = \log K + \frac{1}{2} \log t$$

where d = thickness in Å

t = time in hours

and K (a constant) was found to be 3900 Å for SiC as compared to 6900 Å for Si. This was determined at 1173°C.

Using a standard buffered HF solution (7 parts NH_4F to 1 part 49% HF) as an etchant, the average etching rates of the SiO_2 on SiC or Si were found to be essentially the same, about 870 Å/min at 25°C. No significant difference was found in the etching rate of oxides grown using argon or oxygen as the carrier gas.

The SiO_2 layer is utilized in several ways in the fabrication of the transistor.

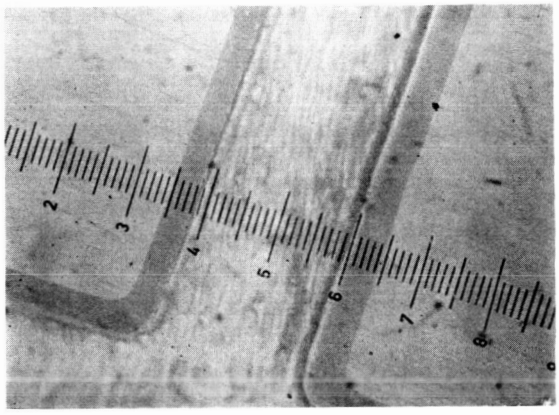
1) As a mask for the chlorine etch in preferentially etching SiC to create the self-diffusion mask for formation of the upper gate and source and drain regions (see Fig. 2.6),

2) As a positive means of identifying the polarity of the SiC crystal surface, i.e., the C or Si face for processing,

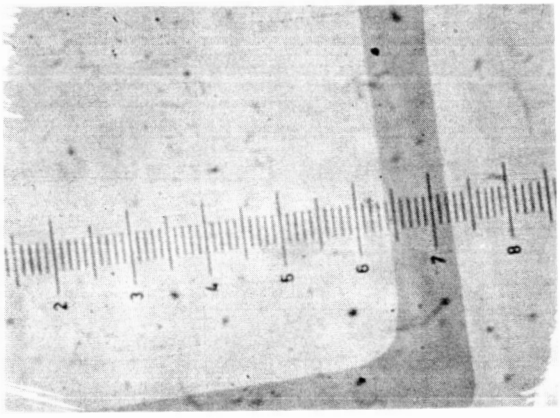
3) Contact confinement in the contact alloying process,

4) As a means of delineating p-type regions from n-type regions on a crystal. (See Figure 3.6)

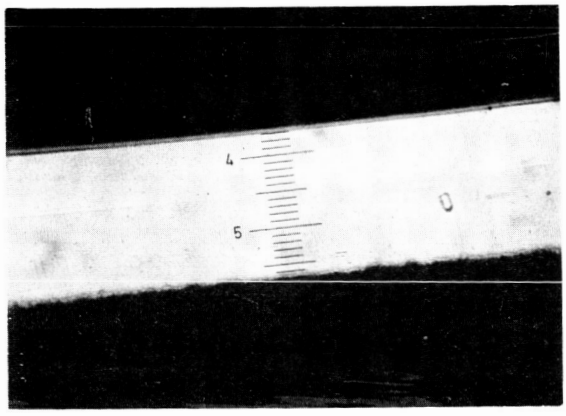
The last one is an important and new contribution to SiC technology. It has been found that the oxide grows at a different rate on



480X view of the isolation region of a FET after polishing to planarity. The difference in color of the oxide delineates the depth of the second aluminum diffusion.



480X detail of gate region after reduction to planarity. The difference in color of the oxide offers an easy delineation method.



360X cross section of a crystal after first aluminum diffusion. Notice difference in color of the n and p areas and thick oxide layer on carbon face of the crystal.

Figure 3.6 Oxide delineation of p-n junctions

p and n-type regions on a single crystal of SiC leading to a different coloration of these regions as a result of the interferences of thin films. That the difference in coloration is a result of at least a difference in the oxide thickness has been shown by long oxidation of surface with both p and n regions and a delineation of these regions after the removal of the oxide.

This difference in oxidation has also been used in the delineation of junctions after edge polishing a crystal to determine the junction depth after aluminum diffusion. It has been noted that the oxidation coloration is different on the edge of the crystal from that on the carbon face of the same crystal indicating that the oxidation rate is anisotropic in crystallographic direction in addition to the anisotropy of the two faces. The delineation is clear and has been checked and found to be in agreement with the junction delineation observed on the electrolytic etch. It has also been noted that the time of oxidation required for edge delineation ($\sim 1175^{\circ}C$) is considerably longer (minimum of 90 minutes for rather poor delineation) than that required for delineation on the carbon face (30 minutes gives a very clear delineation) indicating that the difference in oxidation rates on p-type from n-type is probably considerably greater in the C-direction than perpendicular to the C-direction.

The clear delineation of the gate region from the source and drain regions on the carbon face give a means of positive identification for photoresist mask alignment in the contact process. In addition, it clearly shows when a gate region is incomplete as a result of non parallel lapping in removal of the SiC self-diffusion mask, and also indicates the

failure mode of that device thereby saving time of further processing this device.

It has also been found that SiO_2 is useful in confining the alloy when alloying contacts onto the crystal. For this reason, the contacts are deposited through a window in the oxide to prevent spreading of the contact and consequent shorting of the planar junctions during alloying.

3.5 Chlorine Etching

It was shown previously that chlorine will etch SiC surfaces at elevated temperatures.[22] During an allied program[18] this method was developed and the etching rate determined as a function of temperature. In the present program further improvements were made and this technique is now a controllable fabrication procedure.

The experimental apparatus now used for the etching is shown in Figures 3.7 and 3.8. The silicon carbide crystal to be etched is placed on the quartz boat sample holder which is fused to a hollow quartz rod containing the monitoring thermocouple. The control thermocouple, mounted near the heater, keeps the temperature fluctuations of the furnace to within 1% of the operating temperature. In operation the quartz rod-sample boat assembly is inserted into the reaction chamber with the sample in place. The reaction tube is flushed with argon with the specimen at room temperature and the etching mixture introduced. The furnace is then rolled on the tracks until the specimen is in the uniform temperature zone of the furnace. This zone has been determined to be about two inches long. When the etching has proceeded for the required time, the furnace is rolled back to the idling position and the crystal is allowed to cool to room temperature before being removed from the reaction chamber. There is very little thermal inertia in this system, thus the etching time can be controlled quite accurately.

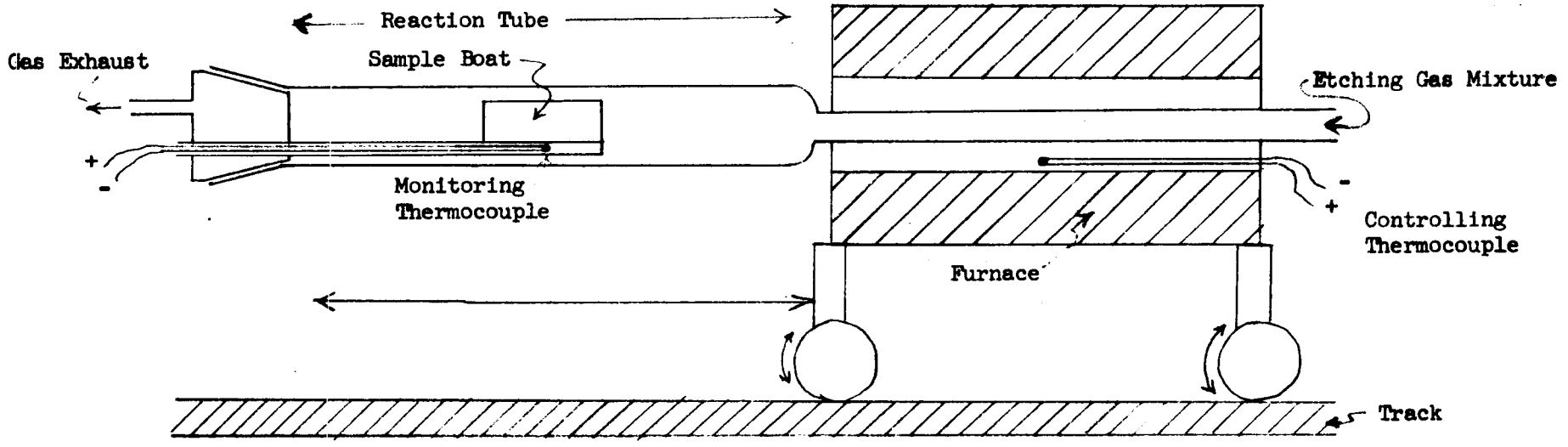


Figure 3.7 Schematic of chlorine etching apparatus

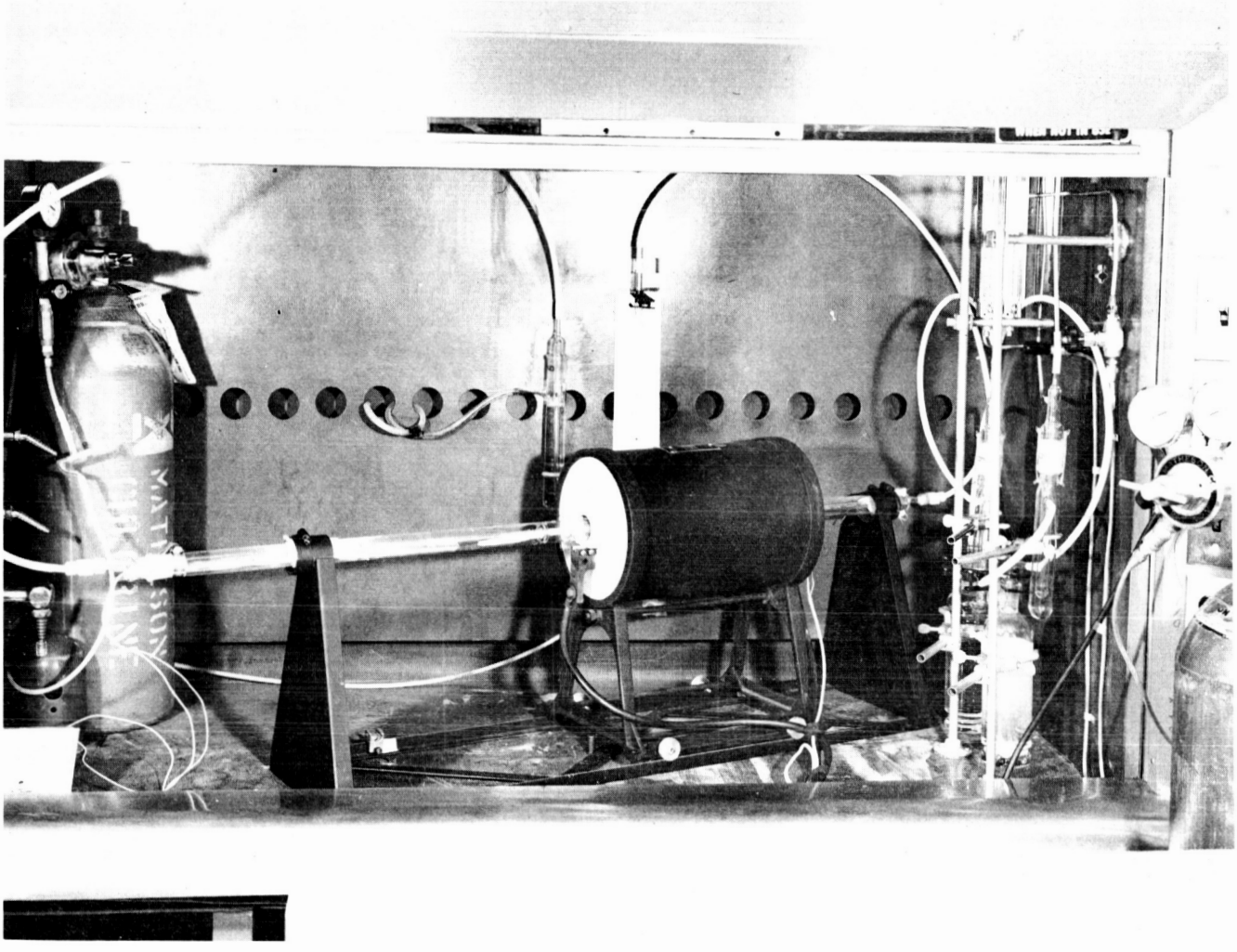


Figure 3.8 Photograph of chlorine etching apparatus

Three flowmeters are used for monitoring the flow of Cl_2, O_2 and Ar, with a flow rate range up to 500 cc/min. The cross-sectional area of the reaction tube is 6-7 cm^2, therefore, the linear velocity can be varied from zero to one cm/sec which is within laminar flow condition.

The following etching reaction occurs in the reaction tube:

$$SiC + 2Cl_2 \rightleftharpoons SiCl_4 + C$$

To remove the carbon from the surface, oxygen is added to the etching reaction to form CO and CO_2.

An idea of the etching rates obtainable with this method are shown in Figure 3.9. This curve (determined earlier) indicates the etch rate can be varied two orders of magnitude over a 300 degree temperature range. By varying the oxygen content from 15% by volume to 85% by volume, the etching rate can be increased by a factor of two. In fact it was not possible to determine a maximum etch rate (as a function of the Cl_2, O_2 mixture) as the etching rate increase monotonically with the O_2 concentration. However, when the O_2 concentration exceeds 50% by volume, large amounts of SiO_2 are formed, leading to rough, irregular etch surfaces. Similarly the concentration of O_2 cannot be drastically reduced in that 1) the pure chlorine etch leaves a pseudo-lattice of carbon on the surface, and 2) the undercutting of the mask pattern becomes more pronounced with a high chlorine concentration. It has been found most feasible to control the etch rate by mixing varying amounts of argon with the etchants.

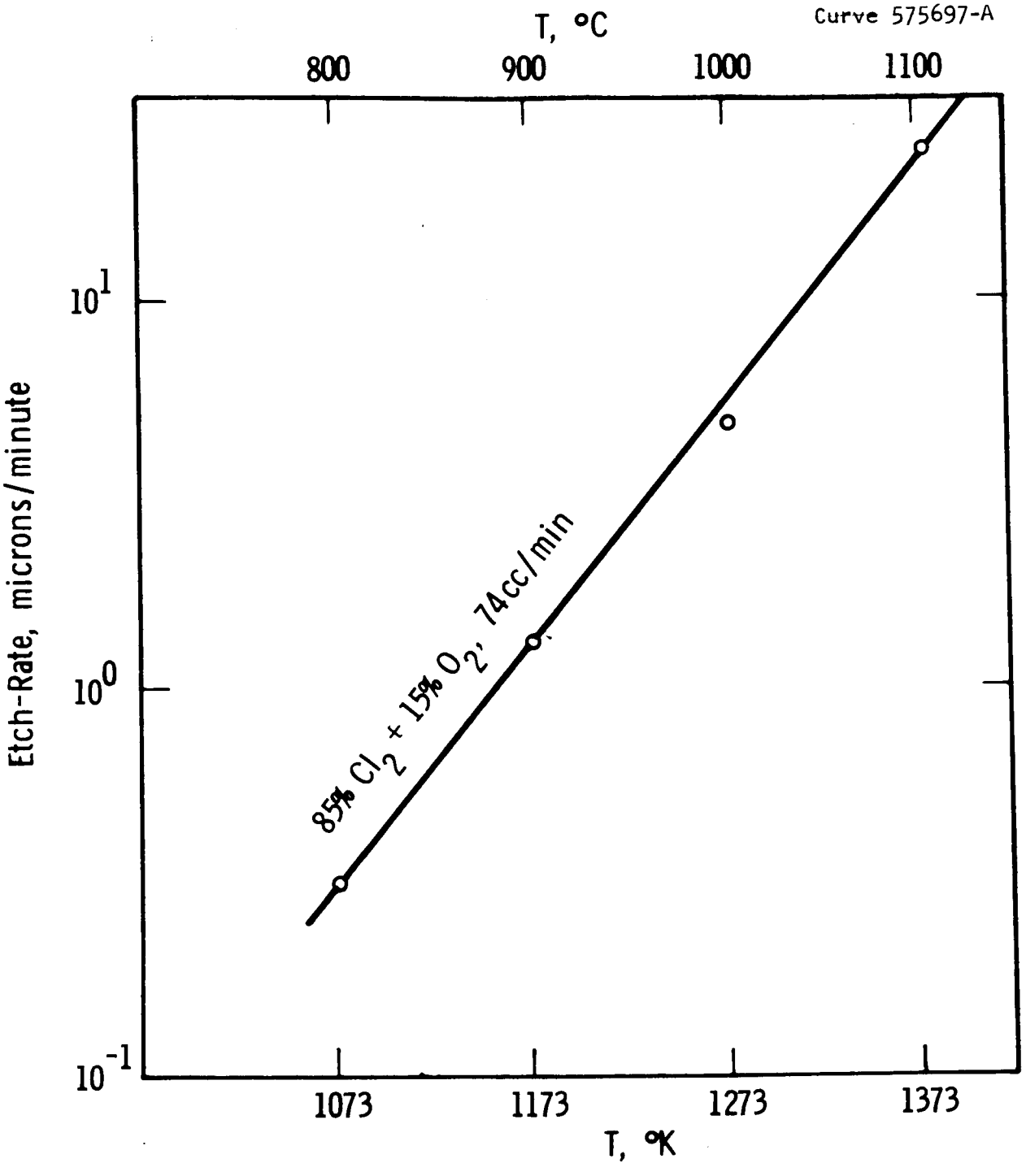


Figure 3.9 — Chlorine etch rates

The argon retards the etching rate without negative side-effects. The optimum concentration was found to be:

45 cc/min Cl_2

120 cc/min Ar

10 cc/min O_2

This composition gives an etching rate of 0.25 $\pm$ 0.02 microns per minute at 900°C, and is sufficiently fast that excessive times are not required for the etching.

These etching rates were determined on the carbon face of the crystal. The etching rate on the silicon face is at least an order of magnitude less.

A problem that occurred during this work was a surface roughness produced by the etching and the formation of amorphous silicon on certain areas of the crystal. These amorphous layers would inhibit further etching. Figure 3.10 shows a rough cobblestone appearance on the surface produced by etching. Such structure would probably not prevent a device from operating, but it would certainly degrade the properties since an uneven diffusion front would result. Both effects, (the surface roughness and the amorphous silica) disappeared when two further improvements were made. First, the gases were dried (using H_2SO_4 for the Cl_2) before they entered the reactor. Water vapor contamination in the gases would lead to the formation of SiO_2. The SiO_2 would then deposit on the surface and prevent etching in those areas.

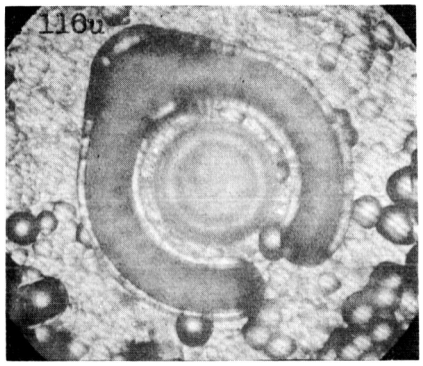


Figure 3.10 Rough chlorine etched surface

It was also found necessary to etch the crystal in a buffered HF solution (7 parts NH_4F + 1 part 49% HF) just before the chlorine etching. This treatment removed any small pieces of oxide left from the photo-resist procedure, etc., which apparently were the major cause of the cobblestone effect.

With these improvements, the process is now quite controllable and extremely smooth etch surfaces are obtained. Figure 3.11 is an example of a chlorine etched surface only a very slight texture ($< \mu$) is noted on this surface. Such deviations are permissible in the transistor fabrication process.

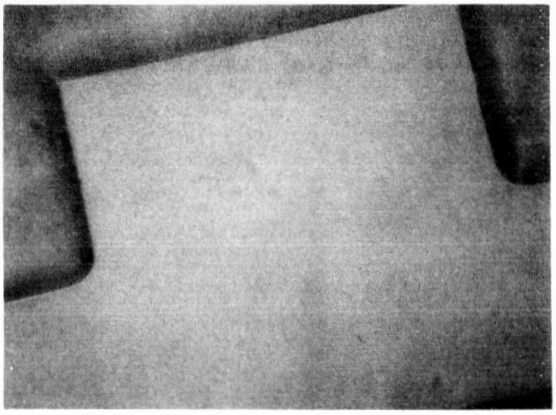


Figure 3.11 Chlorine etched surface showing little texture (560X)

3.6 Alloying and Mounting

The size of unipolar transistor as presently designed is 32.5 mils x 38.75 mils. The contact areas are correspondingly small, for example, the upper gate contact dimensions are 60 x 60 microns. It is possible (although difficult) to alloy a small contact to this area, (see Fig. 3.12) however, to achieve optimum operation of the transistor, the entire length of the gate (corresponding to the channel width) must be contacted. The gate width (or channel length) is approximately 20 microns, and to alloy contacts along the entire length using alloy preforms would not be feasible. Therefore the photoresist process is also being used for contacting.

Gold-tantalum alloys[7,18] are used as the contacting materials, and a set of photoresist contact and rejection masks (described in Section 4.1) were prepared.

The rejection mask process is necessary since there is no convenient etchant for tantalum. Concentrated HF will remove the tantalum but this also attacks the SiO_2. Therefore an evaporated film of aluminum is deposited over the crystal. Subsequently, when it is desired to remove a portion of the gold-tantalum films, etching in hot NaOH solution will dissolve the aluminum and thus remove the gold-tantalum by floating it away. This process is difficult, in that if the aluminum film is too thick the etching will effect the gold-tantalum on the contact area while if it is too thin it will not completely strip the gold-tantalum film.

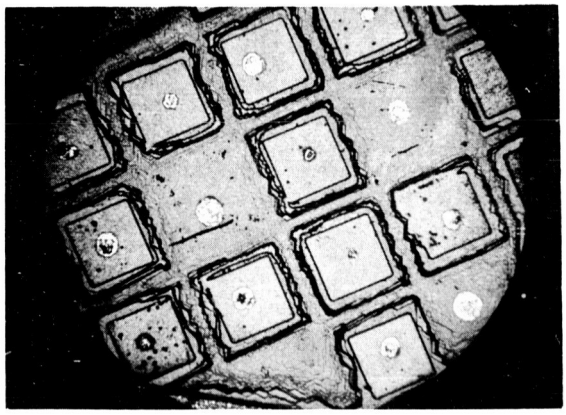


Figure 3.12 Circular Au-Ta alloyed contacts on square areas of 16 mils x 16 mils

It was found most feasible to prepare the alloy films by sputtering since the evaporation of tantalum is difficult to control. The sputtering apparatus is shown in Figure 3.13. An important feature is the multiple cathode assembly where up to four different materials can be sputtered without entering the system. External fixturing makes it possible to rotate the individual cathodes in position over the specimen.

In early work a film of tantalum was sputtered over the surface (500 Å thick) followed by a layer of gold (4000 Å thick). However during the alloying, the gold had a tendency to ball up and continuous contacts were not formed. This undesirable situation is illustrated in Figure 3.14. However, by sputtering five alternate layers of gold and tantalum followed by sintering to homogenize the alloy, the alloying was much more satisfactory. Figure 3.15 shows contacts prepared this way. Although there is still some balling up of the gold, the contact is continuous and has low contact resistances. With further development, this technique would undoubtedly lead to flat, uniform contact regions.

Since the device is quite fragile, it must be alloyed to a solid tab before probe testing. A tungsten tab, previously sputtered with Au, and three alumina parts, also gold sputtered on each end, are used for this purpose. The crystal and the posts are placed on the tungsten disk and alloyed at about 1225°C. At the same time, the photoresisted contacts are alloyed into the device.

Thermocompression bonded gold leads (1 mil diameter) from the contact areas to the posts complete the assembly for testing. A completed device is shown in Figure 3.16.

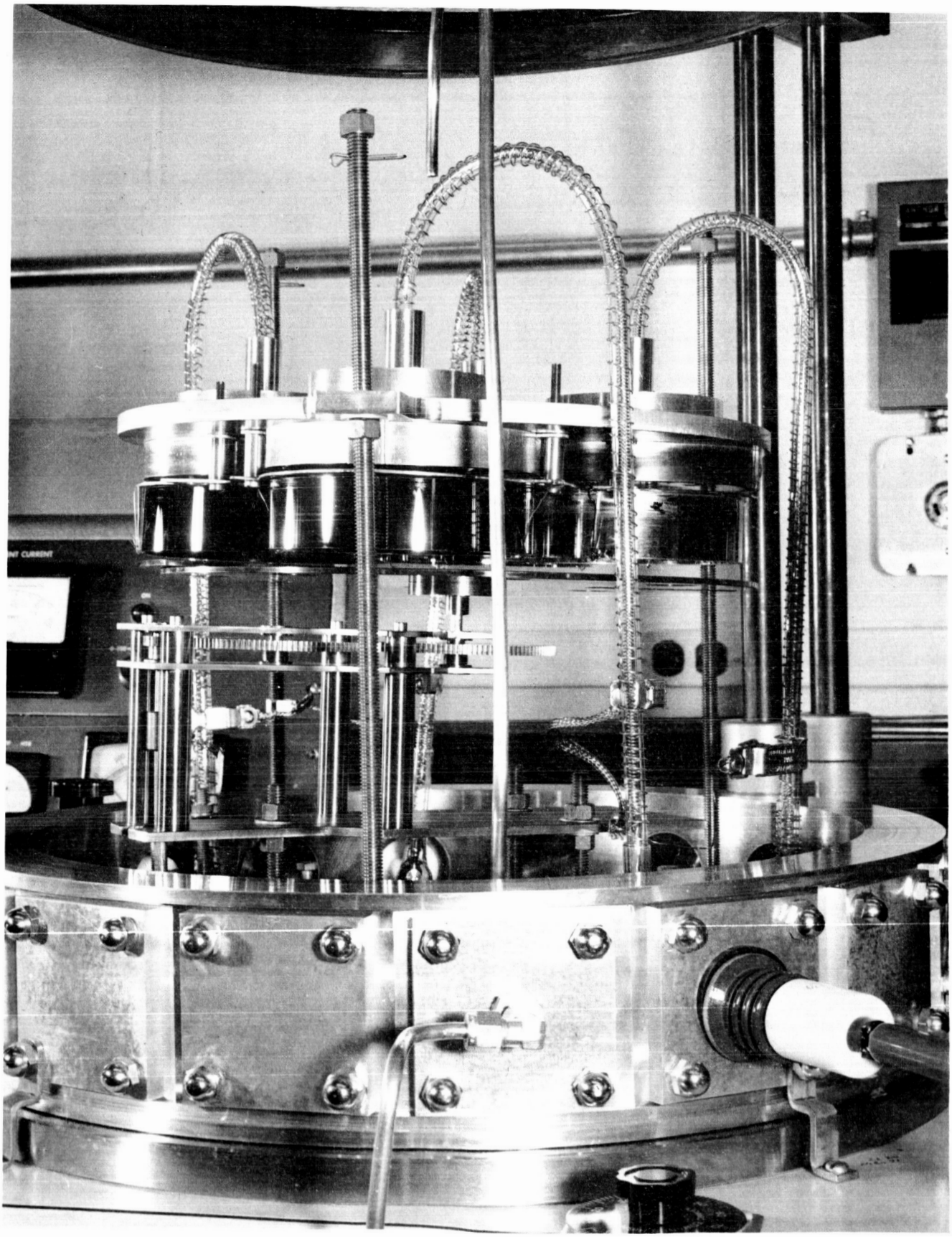


Figure 3.13 Sputtering Apparatus with Multiple Cathodes

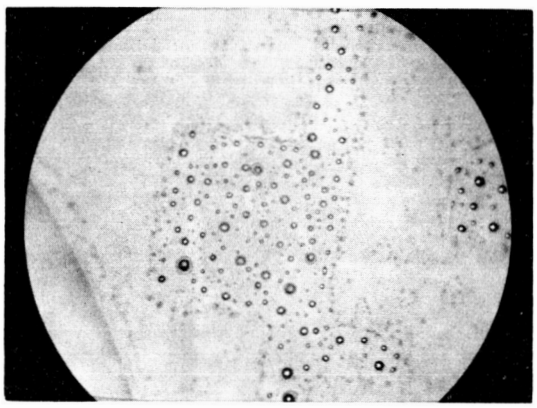


Figure 3.14 Gold-Tantalum Alloy -- Note "balling" of Au

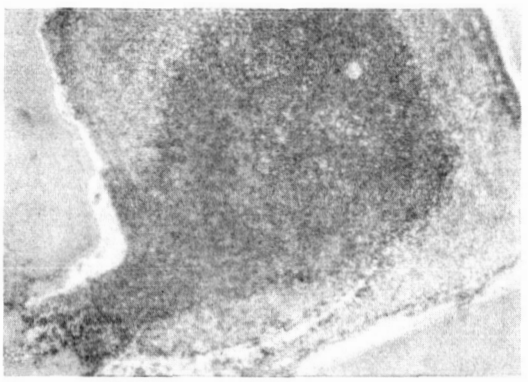


Figure 3.15 More uniform alloying using layered Au Ta alloy (450X)

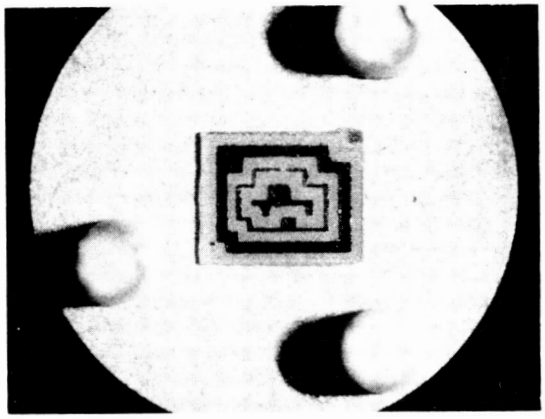


Figure 3.16 Completed Device (27X)

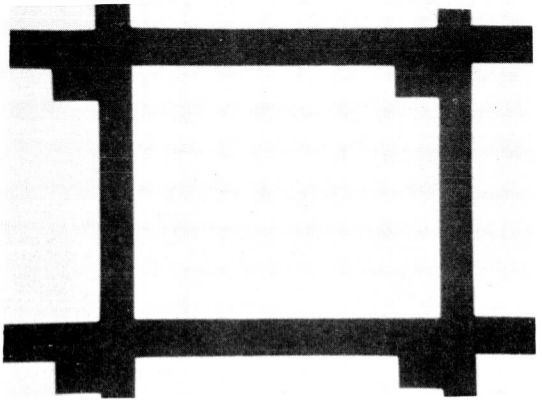
4. DEVICE FABRICATION

4.1 Mask Design

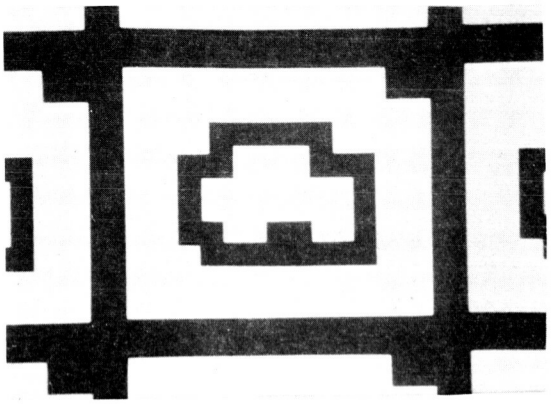
The photoresist masks used for the amplifier components have undergone refinement during the program. The initial masks were designed to test fabrication procedures and process feasibility.[18] The main features of these early masks were large contact areas for both channel terminals and gate. However, no isolation between devices was attempted.

After the fabrication procedures (described in Section 3) had been tested new masks were designed which kept the proven mechanical features of the old masks, but which provided isolation.

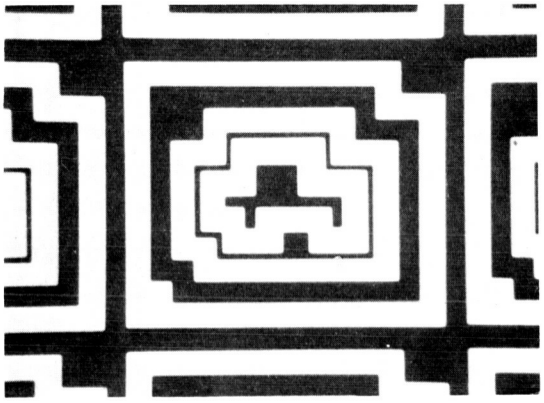
Figure 4.1 shows the set of photoresist masks (Series 110) used in the fabrication of the field effect transistor. Mask 110/1 (110 = serial number; 1 = sequential number) provides an etch pattern in the oxide for chlorine etching of the isolation grooves. Mask 110/2 provides an etch pattern in the oxide for the gate region. During chlorine etching of the gate, the isolation grooves are etched deeper. Mask 110/3 provides an etch pattern in the oxide for electrical contacting to the SiC. The aluminum rejection mask is also etched along the same areas. Mask 110/4 is used in conjunction with 110/3 to expose the alignment pattern around the device. If this is not done, there is danger of shorting the lower gate to the source. Mask 110/5 is designed to allow a metal etch procedure for making contacts before developing the mask rejection process. The smallest division of the



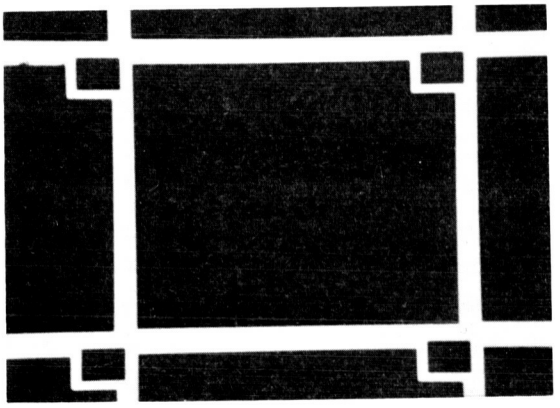
Mask No. 110/1



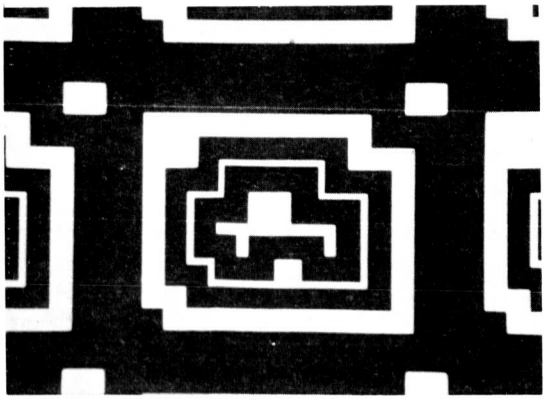
Mask No. 110/2



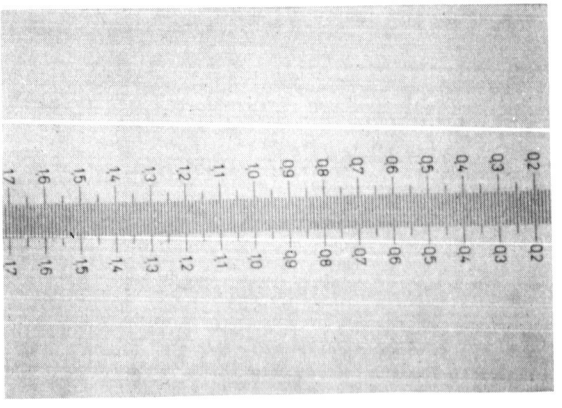
Mask No. 110/3



Mask No. 110/4



Mask No. 110/4



Micrometer Scale

Figure 4.1 Set of Photoresist Masks to Fabricate Field-Effect Transistor

scale of the masks shown in Figure 4.1 is 0.01 mm (or 10 microns).

Figure 4.2 is a composite drawing of the mask system. Individual masks for any one processing step can be derived from such a composite drawing.

The device has a basic rectangular shape providing sufficient contact areas and at the same time still maintaining an almost uniform dimension between source, drain and gate. This design also makes maximum use of crystal area. Considerations reflecting the special SiC device technology have dictated the minimum distance between electrodes. While the dimension of the device may not be optimum from the theoretical point of view, the large device area, however, is good for power dissipation.

These masks were used in the processing of a number of crystals and were shown to be quite satisfactory.

It was necessary to modify the mask slightly when it was determined that the side etch effect in SiC (i.e. undercutting of the oxide mask during Cl_2 etching) was negligibly small. The top area of the etched SiC region is therefore not much greater than the oxide opening area. Because of the etching shape factor, the bottom area of the etched SiC region is smaller than originally designed.

The etching shape factor is due to the fact that the width of the etched trough decreases uniformly as the etching proceeds in depth. The shape factor for SiC has been determined and can be expressed as follows:

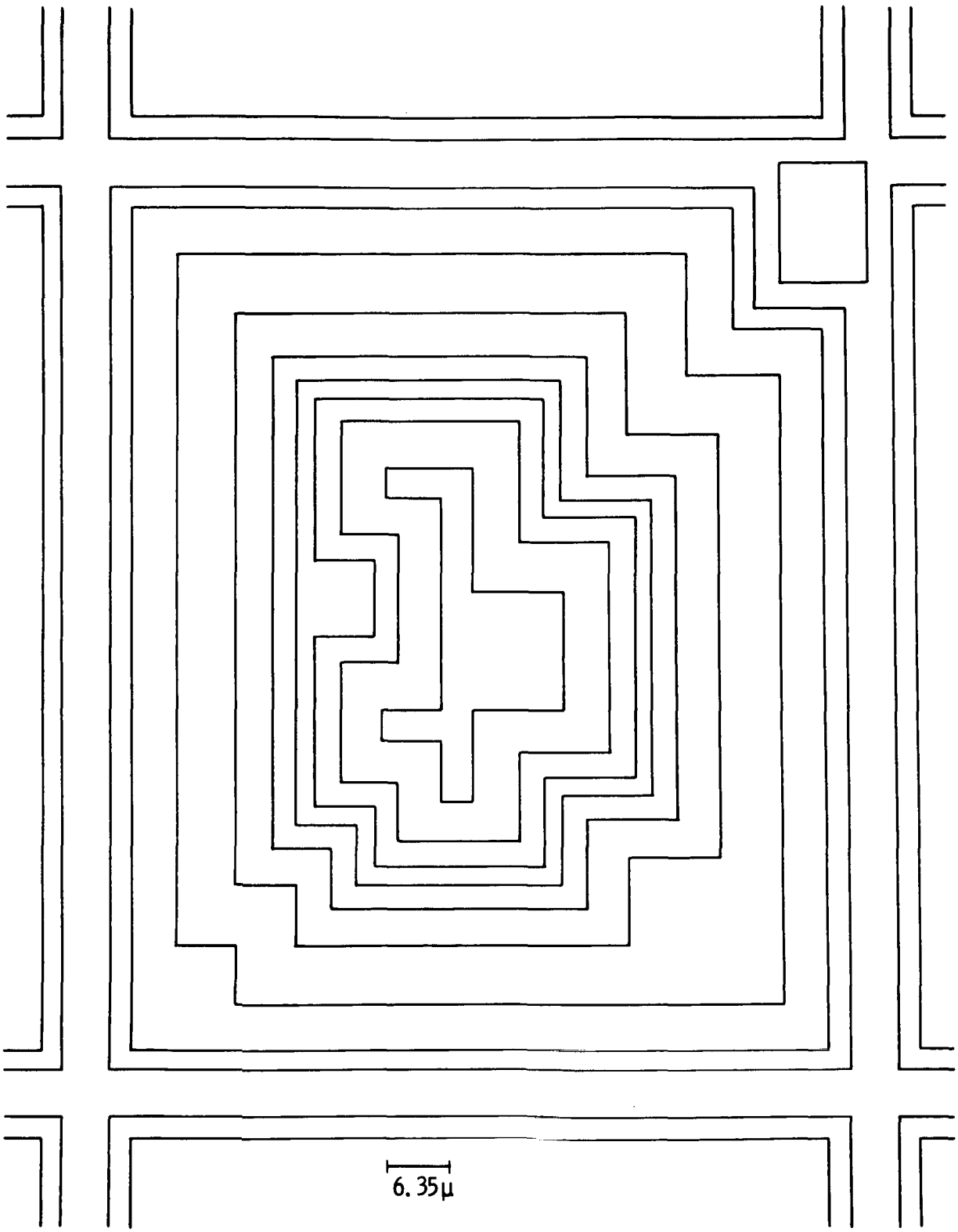


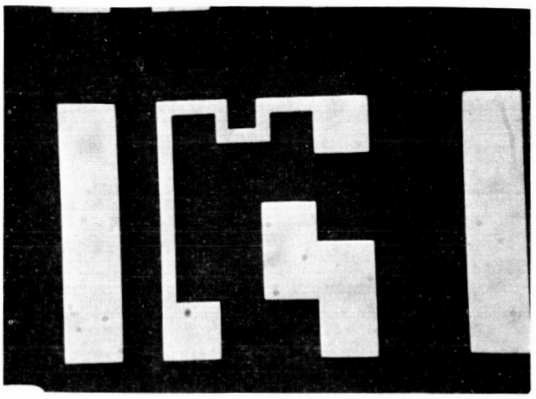
Fig. 4.2—Series 110 composite mask for field effect transistor

$$\begin{bmatrix}\text{Width of the etched}\\ \text{trough at the top}\end{bmatrix} = \begin{bmatrix}\text{Width of the etched}\\ \text{trough at the bottom}\end{bmatrix} + 2 \begin{bmatrix}\text{Depth of the}\\ \text{etched trough}\end{bmatrix} \times \text{Cot } 55^{\circ}$$

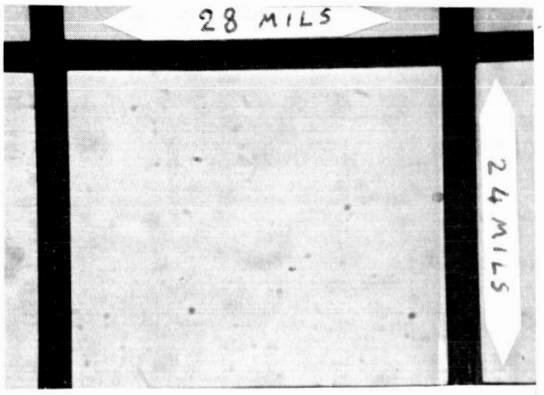
The width at the bottom of the etched trough controls the gate area of the transistor and dictates a limiting size of the metallic contact area. As a result of this investigation, the photoresist-etch mask has been redesigned (serial no. 110) to replace the first one (serial no. 90). The new mask will provide a gate length at the contact surface of approximately 60μ for the expected range of etching depth and diffusion depth.

The length of the gate contact is 19μ. This will allow about 0.9 mil of tolerance in alignment on each side of the contact. This alignment is achieved by aligning on the isolation grooves remaining in the crystal after the lap to planarity of the device region. This critical alignment can be checked before alloying with the assistance of the delineation of the gate region by the oxide coloration described in the last section.

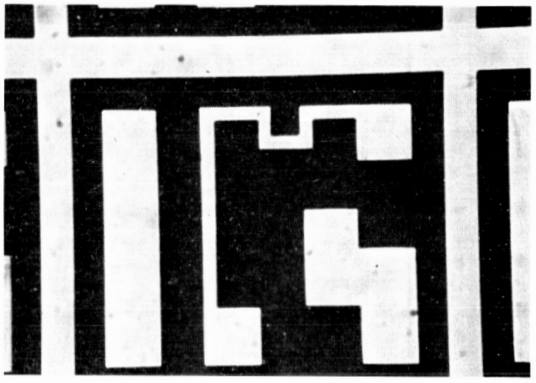
The set of photoresist masks necessary to fabricate the network of resistors for the amplifier circuit is presented in Figure 4.3. Mask dimensions can be evaluated by using the micrometer scale, where the smallest division is equal to 10 microns. Mask 102/1 is used to remove the second SiO_2 layer on a pattern (black area) complementary to the resistors network pattern (white areas). Mask 102/2 is used to remove the second SiO_2 layer over the dice boundary area. Mask 102/3 is used for removing the second SiO_2 layer on an area (black) complementary to



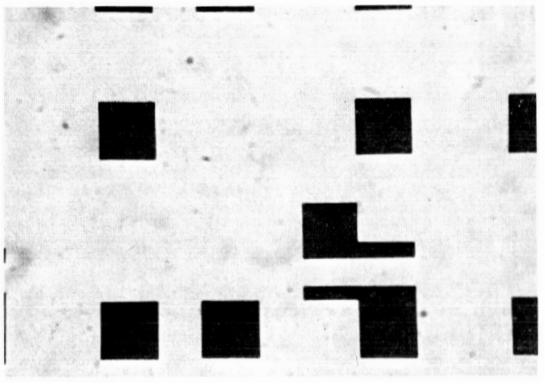
Mask No. 102/1



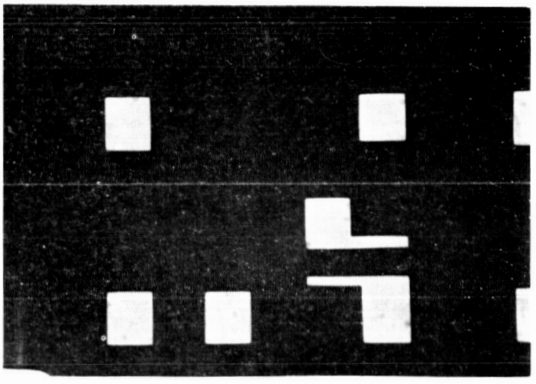
Mask No. 102/2



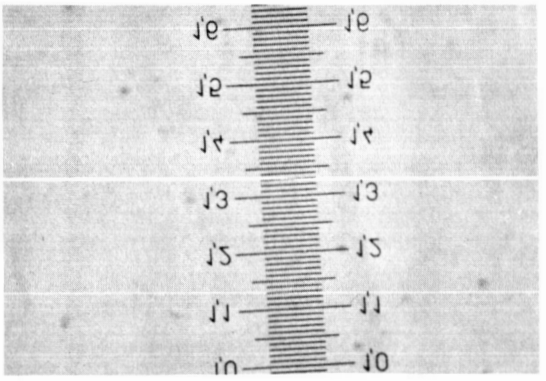
Mask No. 102/3



Mask No. 102/4



Mask No. 102/5



Micrometer Scale

Figure 4.3 Set of photoresist masks to fabricate monolithic array of resistors for integrated SiC amplifier

the resistor area (white); and is applied after first chlorine etch along the dice boundary. Mask 102/4 is used after second chlorine etch, acceptor diffusion, removal of masking SiC crystal by lapping and reoxidation. It serves the purpose of opening windows in the SiO_2 to apply contacts to the resistors terminals. Mask 102/5 is used after vacuum deposition of the Au-Ta films for electrical contacts and serves the purpose of selectively removing such metal films for contact delineation.

The network consists of three resistors whose length/width ratios (commonly referred as number of "squares") are respectively 0.25, 2.5 and 25. Assuming that for a suitable choice of parameters the sheet resistivity of the resistor material will be 1.6 ± 0.4 KΩ/square for the small cross section resistor and 2 ± 0.4 KΩ/square for the large cross section resistors, the three resistors will respectively measure 0.5, 5 and 40 KΩ. Resistors of other values can be obtained by varying the sheet resistivity of the material or the dimensions of the marks.

The technique adopted here to integrate the resistors network into a single crystal SiC block, will yield three n-type resistor regions resting in a single crystal matrix of converted p-type material. If properly biased, the resistors will be isolated with each other and from the p-type substrate.

It should be noted, that due to applicable experience the resistor network and the transistor were fabricated on separate chips. However the process proposed for making either component are fully compatible and nearly identical. Thus the amplifier can be fully integrated and fabricated on a single chip.

4.2 Processing Procedures

The procedure through which a given crystal progresses to the more final transistor structure was continuously being improved as more experience was gained on the various fabrication techniques.

The process in use at the end of the program is given in Table 4.1. A discussion of the various procedures for the transistor and resistor follows the table.

Table 4.1 Device Processing Procedures

1	Crystal Selection
2	Lap to 8 mils thick
3	Chlorine Etch (initial)
4	Acceptor Diffusion (No. 1)
5	Diffusion Evaluation (No. 1)
6	Lap and Polish Carbon Face
7	Cross-section Device Crystal
8	Oxidation
9	Strip SiO_2
10	Oxidation
11	Photoresist and etch SiO_2
12	Examine SiO_2 for poor Photoresist
13	HF Etch of SiO_2
14	Chlorine Etch (No. 1)
15	Photoresist and etch SiO_2
16	Chlorine etch (No. 2)
17	Depth evaluation
18	Acceptor Diffusion (No. 2)
19	Diffusion evaluation (No. 2)
20	Acceptor Diffusion (No. 3)
21	Diffusion Evaluation (No. 3)
22	Lap and polish to planarity
23	Oxidation
24	Photoresist and Etch SiO_2 from Contact Areas
25	Evaporate Al and reject mask photoresist
26	Sputter alternating layers of Au and Ta (total 5000 Å)
27	Reject mask etch
28	Sinter
29	Dicing
30	Tungsten Tab Preparation
31	Mounting and Alloying

1. As stated the crystals are selected on the basis of size, purity, electrical properties and perfection. This data is obtained as described in Appendix B. (Unless specifically mentioned, the purpose of the step is the same for the resistors as for the transistors.)

2. The process requires that all starting crystals be nearly the same thickness. In addition, by lapping to 8 mils, more uniform sections of the large, intergrown crystals are obtained.

3. This initial chlorine etch is to identify the polarity of the crystal, i.e., the silicon or carbon face. This etch is for 15 min at 1025°C.

4. In this first diffusion the lower gate is formed. A diffusion depth of ~30 microns is aimed for which requires a diffusion time of 35-40 hours at 2000°C.

5. The diffusion depth is evaluated by edge lapping a control crystal included in the run and delineating the junction by oxidation or electrolytic etching. This depth is then a guide for Step No. 7.

6. As described previously, the techniques of chlorine etching and oxidation proceed at a reasonable rate only on the carbon face of the crystal. Therefore the process steps which require either of these two techniques must be carried out on the carbon face. In this step, then, the carbon face is prepared for subsequent operations. Since the next diffusion step (Step 18) must be controlled to $\pm$ 1 micron, the crystal is reduced in thickness so that the second diffusion can be shallow and therefore more controllable. Material is removed from the carbon face until the total thickness of the crystal is 25 $\pm$ 7 microns

greater than the first diffusion depth, or about 55 microns.

7. At this point, the crystals to be used for the device are polished on two edges and examined microscopically. This assures that the lapping has been planar and provides diffusion data on the crystal for the 2nd diffusion.

8. The crystal is oxidized for 16 hours at 1175°C to form a 2-3 micron SiO_2 layer. This is a surface preparation step found necessary to obtain a uniform SiO_2 layer in Step No. 10.

9. The SiO_2 layer is completely removed in HF, and the crystal carefully cleaned in alcohol and water.

10. The cleaned crystal is oxidized for 2 hours at 1175°C. This forms about 5000-6000 Å layer of SiO_2 upon which the first photoresist pattern is made.

11. The crystal is photoresisted through a mask (No. 110/1 or 102/1) and the isolation grooves are opened by developing the photoresist and removing the SiO_2 at the grooves with HF etching.

These isolation grooves are important for the following reasons:

(a) They bring the lower gate to the upper surface, thus preventing shorting of the lower gate by subsequent alloying procedures.

(b) They isolate the devices in a single crystal (necessary if the devices are to be tested before dicing).

(c) They permit contacting the lower gate on the upper surface if it is not possible to contact the mounting tab.

(d) If needed, they permit alignment of the photoresist mask after lapping to planarity (Step No. 22).

(e) They should permit easier dicing.

12. The entire crystal is examined microscopically to make sure that the photoresist does not contain pinholes, etc.

13. The crystal is etched in a buffered HF solution for 45 seconds. This step is done just prior to step No. 14 and gives a uniformly clean surface for the chlorine etching.

14. The photoresisted crystal is then chlorine etched to etch in the isolation grooves. An etch depth near six microns is aimed for and an etch rate on the specific crystal is determined from the actual etch depth. An etch temperature of 900-910°C is used. For the resistors, this operation provides a scribing line.

15. Using Mask No. 110/2 (or 102/3) the crystal is photoresisted to delineate the upper gate geometry, and etched in buffered HF to remove the SiO_2 from the upper gate region.

16. The crystal is again etched in chlorine etch in the upper gate geometry. An etch depth of 3-4 microns $\pm$ 0.5 micron is obtained using the etch rate obtained in Step 14. The isolation grooves are also etched deeper during this step. In the resistors, this etches the isolation grooves.

17. The depth of the chlorine etching in Step No. 16 must be evaluated quite accurately. The diffusion in Step 18 (and Step 20, if needed) determines the final channel thickness, and the diffusion

parameters are chosen from the measurements in this step. The etch depth is determined by alternately focusing the microscope on the surface of the crystal and on the bottom of the gate region, and then determining the depth from the calibrated rack. This is done on perhaps 40-60 positions over the gate region, and a histogram is prepared from these readings. The depth is determined from the histogram. At this point, also, the depth of the isolation grooves is determined.

18. Using the etch depth determined in Step No. 17, a second acceptor diffusion is performed. Time and temperature are chosen to give a channel width of 1-2 microns.

19. The diffusion depth (and therefore the channel width) is evaluated by edge lapping the device crystal and delineating the junction by oxidation.

20. Based on the results of Step No. 19, a third diffusion may be necessary to further reduce the channel width.

21. Self explanatory.

22. The crystal is lapped to planarity; the lapping stopped at the upper gate level. This exposes the source and drain contact and resistor contact; generally >8 microns will be removed in this procedure.

23. The device crystal is oxidized (30 minutes at 1175°C) to form a 2000-3000 Å SiO_2 layer. This is used for gate location and alignment of the metallization photoresist masks.

24. The crystal is photoresisted using Mask 110/3 or 102/4 and 110/4, and contact windows are opened by buffered HF etching.

25. Since no convenient etch is available for tantalum, a rejection mask technique must be used. Therefore the entire surface is coated with an evaporated Al film, about 15000 Å (1.5μ) thick. The reject mask is now photoresisted (Mask 110/5 or 102/5) onto this Al film and again the contact windows opened by etching in NaOH.

26. Alternate layers of Ta (100 Å thick) and Au (900 Å thick) are sputtered onto the device crystal.

27. The rejection mask is now etched in a saturated solution of NaOH in H_2O for 1 minute at 100°C. This removes the Au-Ta alloy from the device except at the contact areas. The device crystal is then cleaned by an H_2O spray.

28. The alloy is sintered for 15 min at 900°C. This procedure is intended to increase the homogeneity of the alloy. As a result a more continuous contact is formed.

29. The components on the crystal are separated by dicing.

30. A tungsten tab is coated with an evaporated Au film.

31. Three cylindrical alumina posts (gold coated on each end) and the device are placed on the tungsten tab and alloyed (in vacuo) at 1600°C. Thermocompressed gold wires (1 mil in diameter) from the device to the posts complete the fabrication.

To facilitate following the procedure, the crystal and transistor device structure are sketched at various stages of the process

and shown in Figures 4.4 to 4.10.

Figure 4.11 shows a crystal which has been processed through Step 23. The devices are all well defined. This is a small crystal which contains only three devices. Figure 4.12 (a,b) show the top and edge of a device in a crystal which is ready for Step 22. Figure 4.13 is an enlarged edge view of the same crystal. The channel is clearly visible and is about six microns in this device.

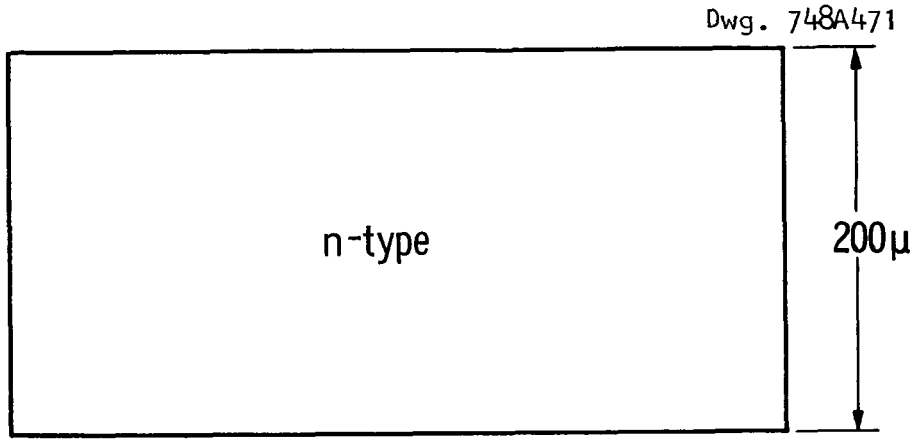


Fig. 4.4—Step 2

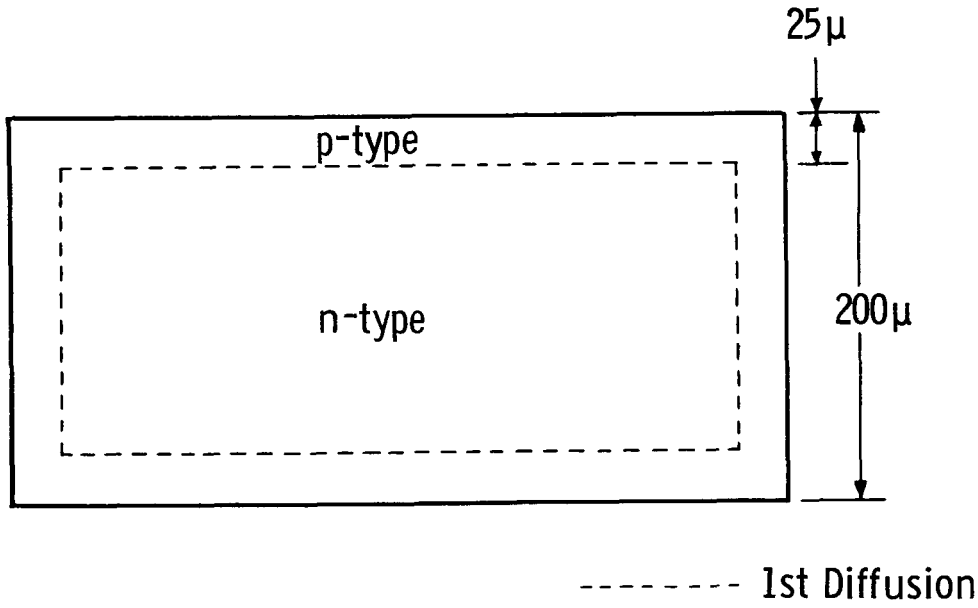


Fig. 4.5—Step 4

Dwg. 748A472

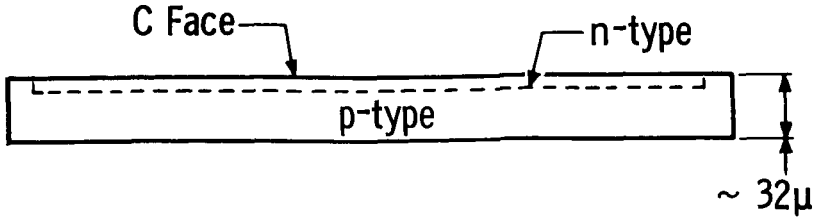


Fig. 4.6—Step 6

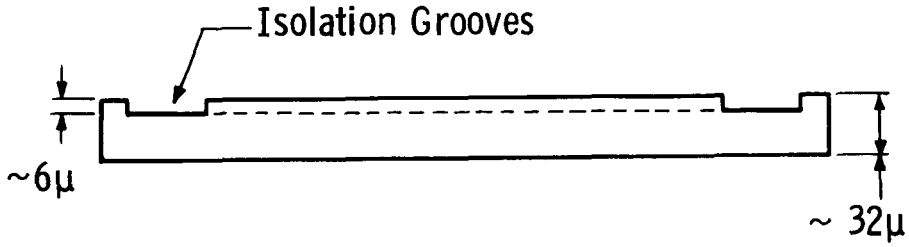


Fig. 4.7—Step 14

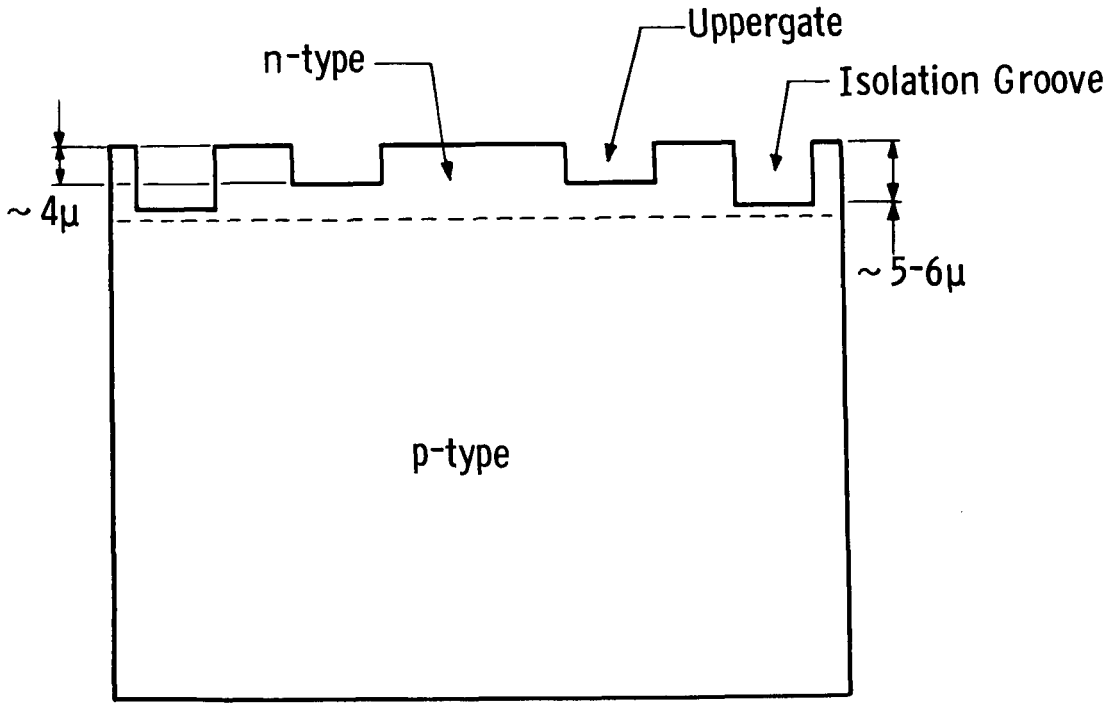


Fig. 4.8—Step 16

Scale expanded 10X from previous figures

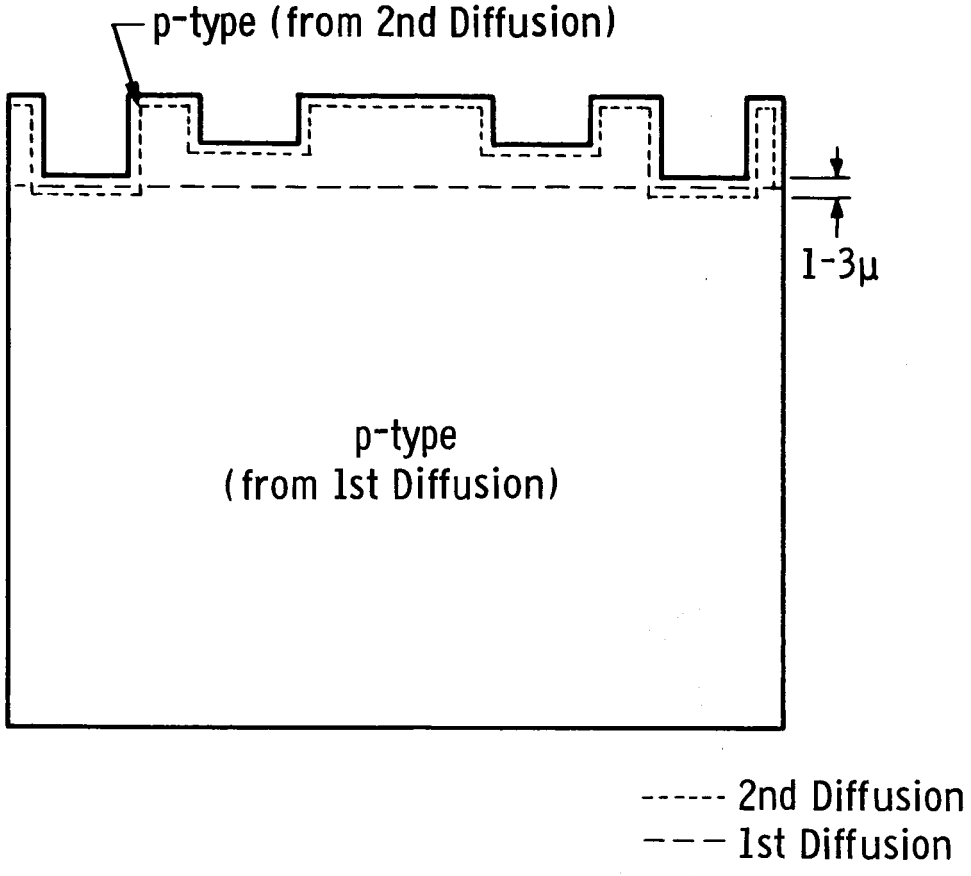


Fig. 4.9—Step 18

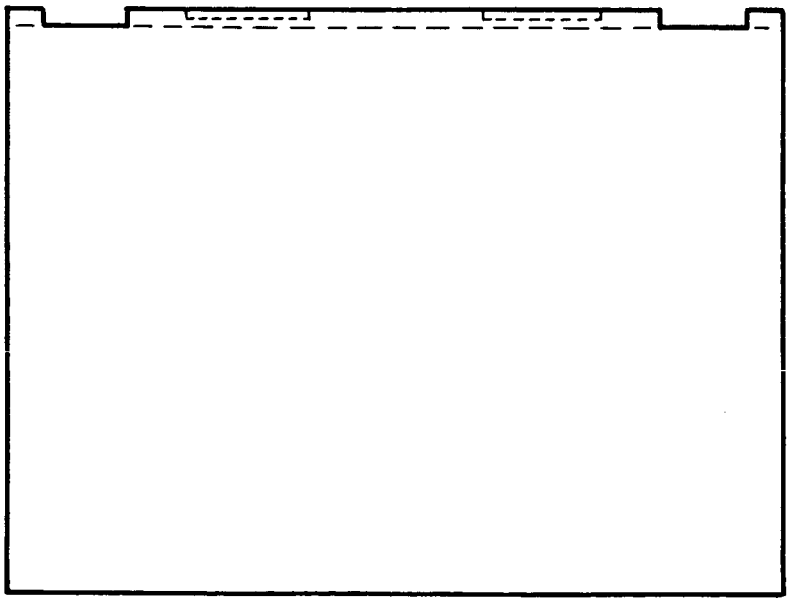


Fig. 4.10—Step 22

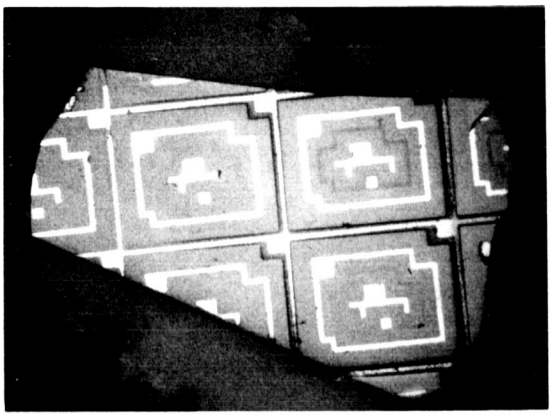
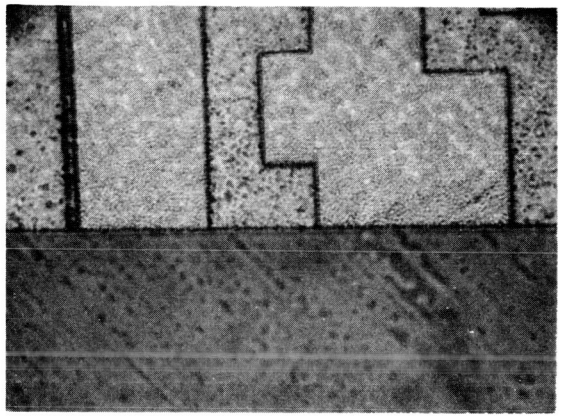
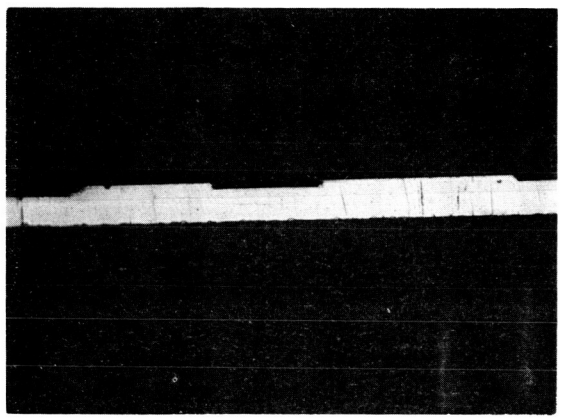


Figure 4.11 Crystal D-80-16 - Finished Device Structure (25X)



(a)



(b)

Figure 4.12 Crystal D-80-20 - Top View (a) and Edge View (b) Showing Device (137X)

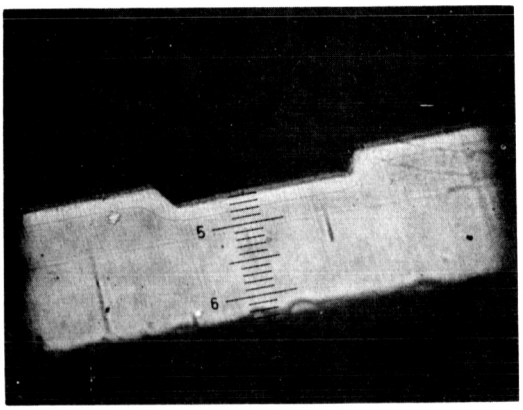


Figure 4.13 Crystal D-80-20 - Edge View
Note Diffusion Fronts (480X)

5. DEVICE EVALUATION

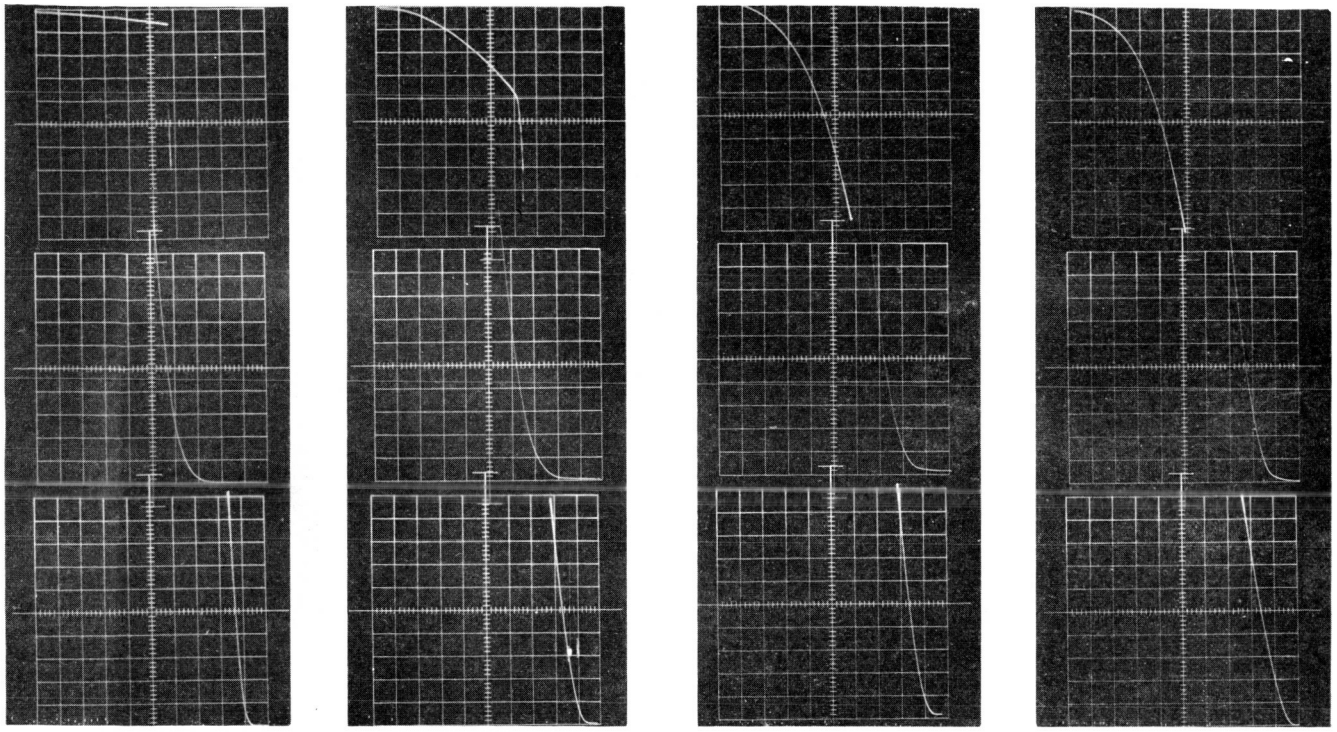
The fabrication procedures designed for SiC monolithic functional blocks have been tested first on the unipolar field-effect transistors (FET). This test is now almost finalized. Improvements in the process of metallization of electrical terminals, dice bonding, and lead attachment are still needed.

At present there are several crystals in different steps of processing, but only the first three have been completed. These three crystals, D75-34, D80-20 and D80-22 do not represent the best choice of material nor the best combination of processing techniques; yet two out of the total 25 units on these crystals exhibit transistor characteristics at room temperature as well as at 500°C. Several of the gates on the 25 FET structures exhibit very good rectifying junction characteristics. The evaluation methods, detailed data and analysis will be presented as follows.

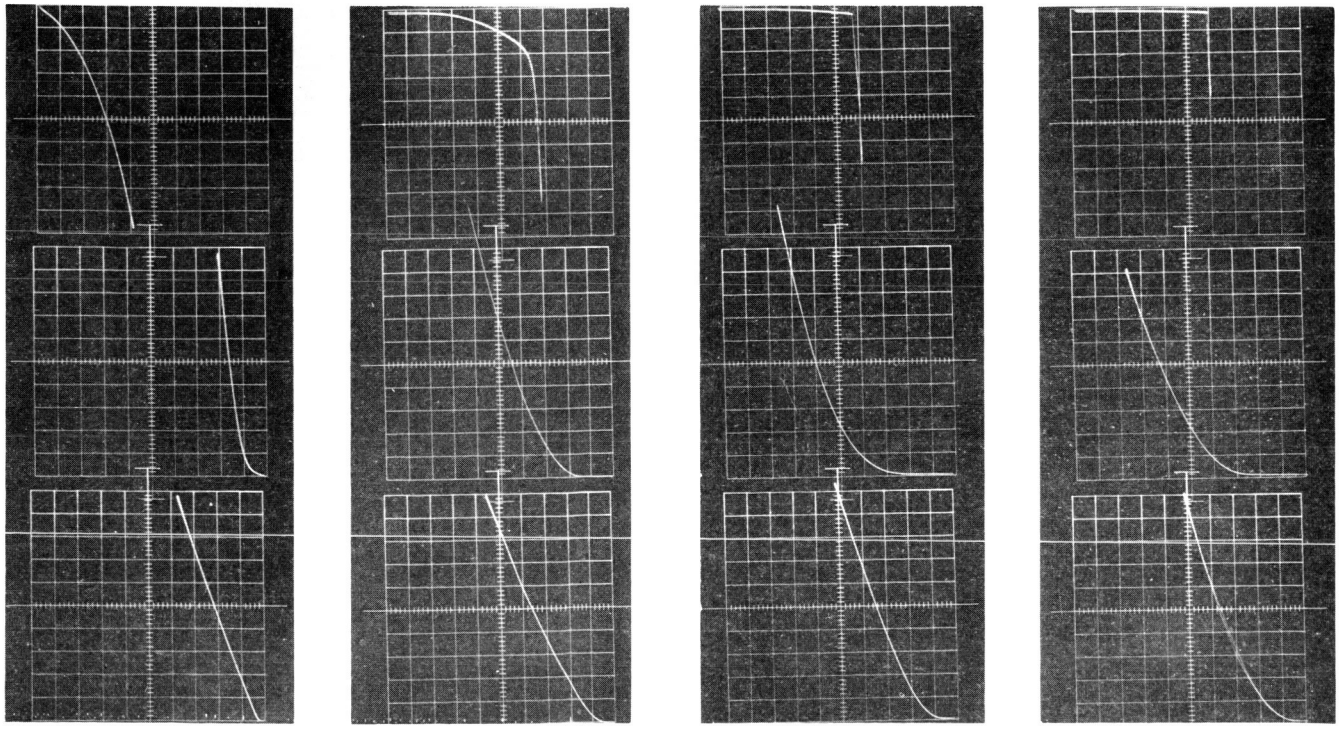
Preliminary electrical evaluation of the completed FET structures was done, using a Tektronix 575 Transistor Curve Tracer. The large gate voltages required by SiC FET devices presented somewhat of a problem because the stepped voltage source of the curve tracer designed for silicon devices has an insufficient range. The problem was partly overcome by grounding the stepped current source through a 1 KΩ resistor, thereby obtaining up to 10V in steps of about 1V. For larger gate voltages, an external dc voltage source can be used. In order to obtain the electrical characteristics of these devices as a function of temperature, the transistor was heated gradually from

room temperature up to 520°C and then cooled to room temperature again. As the temperature of the unit was increasing and decreasing several pictures of the family of the FET drain characteristics and of the selected diode characteristics were obtained from the curve tracer. As mentioned above, the contact wiring technique still needs some improvements, therefore all of the electrical measurements were taken with probes connecting the contacts instead of regular bonded wires as planned. All measurements were made with a continuous flow of argon over the units.

Figures 5.1 through 5.4 illustrate the behavior of some electrical characteristics of selected SiC devices as a function of temperature. Figures 5.1 and 5.2 show the reverse and forward characteristics of an upper gate and a lower gate biased with respect to the source electrode. Figure 5.1-a displays the reverse characteristics of the diode. It is interesting to notice that the abrupt breakdown voltage of this junction does not decrease with increasing temperature, although the "leakage" component of the reverse current is increased by a factor of three for a 100°C increase in temperature. The slope of the forward characteristic in Fig. 5.1-c, after the heating cycle, shows a change from before heating indicating an increased contact resistance. Figure 5.3 shows the family of characteristics of one of the FET's as a function of temperature. The maximum transconductance of the device, approximately 90μ mhos/mA, decreases as a function of the gate voltage. The saturation strain resistance measures approximately 150 KΩ. The characteristic with $V_g = 0$ does not show saturation because the drain voltage V_d is still smaller than the pinch-off voltage V_p.

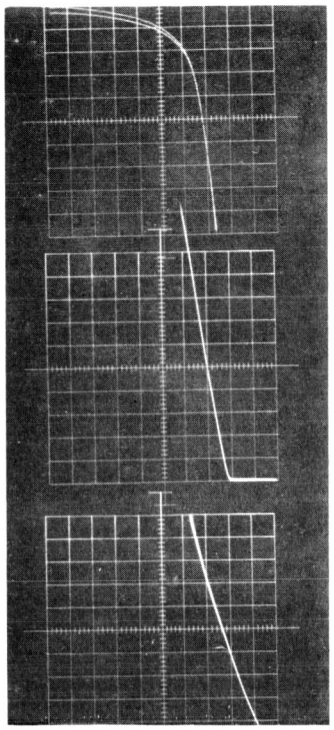


25°C 100-120°C 200-220°C 300-320°C

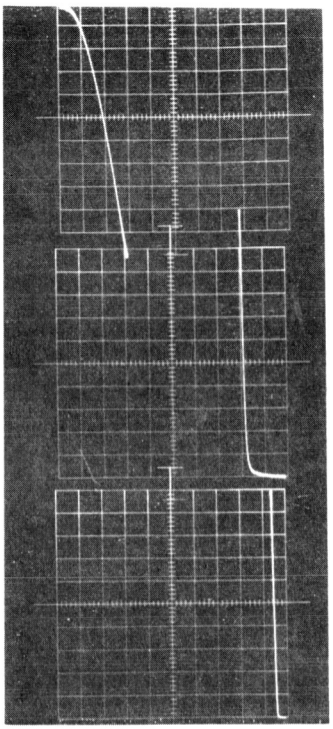


500-520°C 220-200°C 60-55°C 25°C

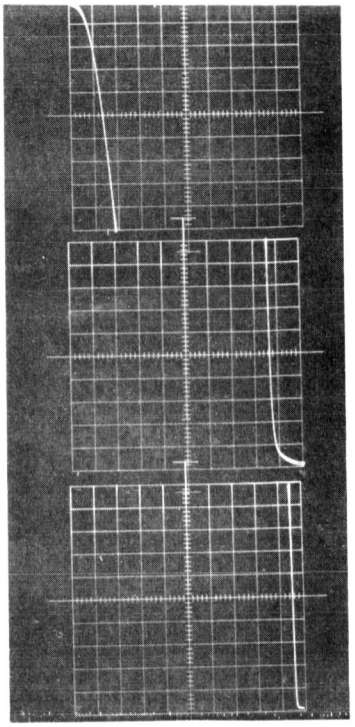
Figure 5.1 Device D-80-20 No. 8; Upper Gate to Source Diode Characteristics at the Indicated Temperatures
a-reverse, 20V/div horizontal, 0.1 mA/div vertical;
b-forward, 1V/div horizontal, 0.1 mA/div vertical;
c-forward, 5V/div horizontal, 2 mA/div vertical.



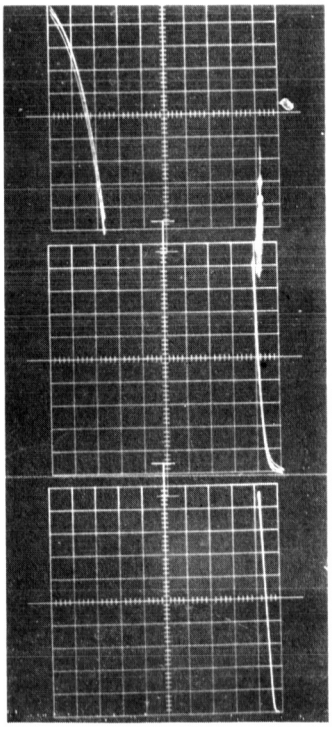
25°C



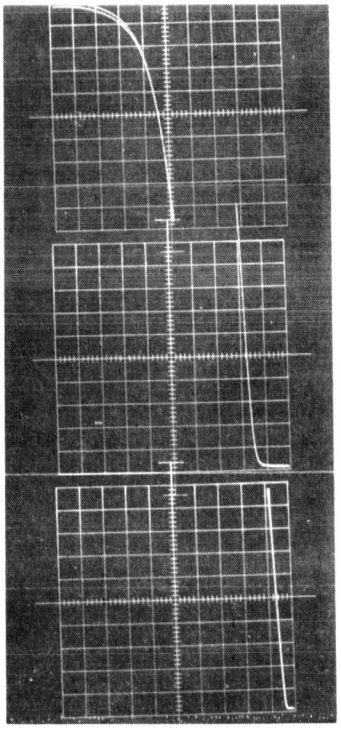
190°C



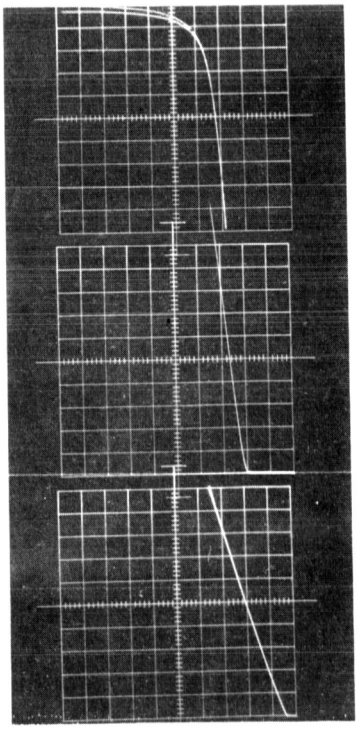
300-320°C



500-520°C

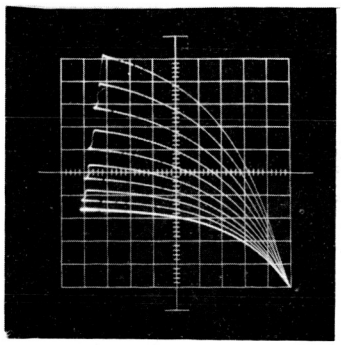


320-280°C

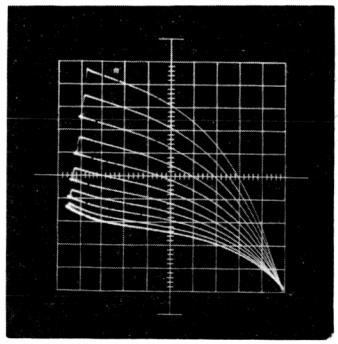


25°C

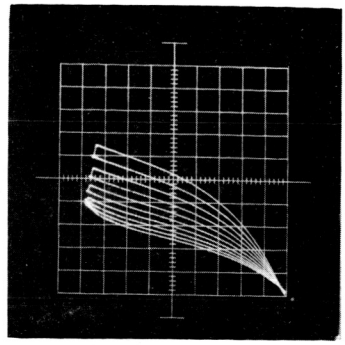
Figure 5.2 Device D-80-20 No. 3; Lower Gate to Source Diode Characteristics at the Indicated Temperatures
a-reverse, 20V/div horizontal, 0.1 mA/div vertical;
b-forward, 1V/div horizontal, 0.1 mA/div vertical;
c-forward, 5V/div horizontal, 2 mA/div vertical.



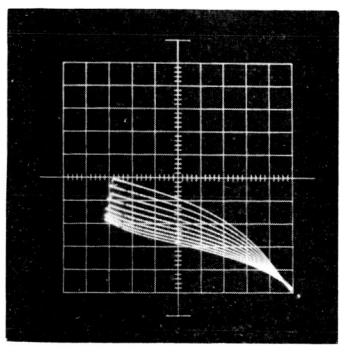
25°C
1.35-.9V/Step



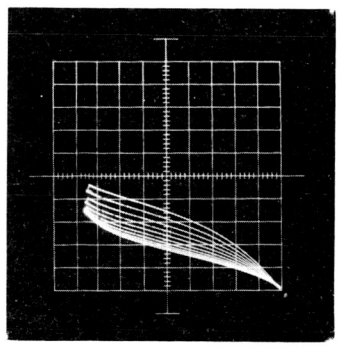
110°C
1.2-.8V/Step



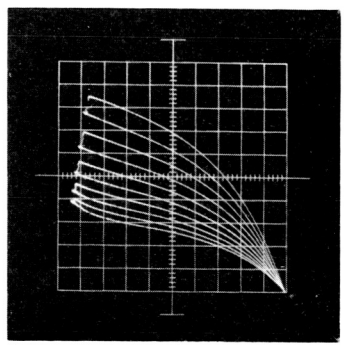
290°C
1-.7V/Step



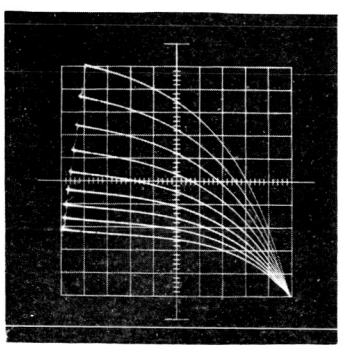
400°C
.95-.7V/Step



500°C
1.2-.8V/Step

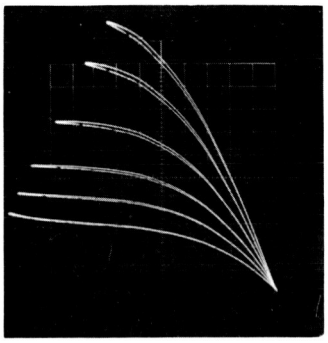


200°C
1.4-1.0V/Step

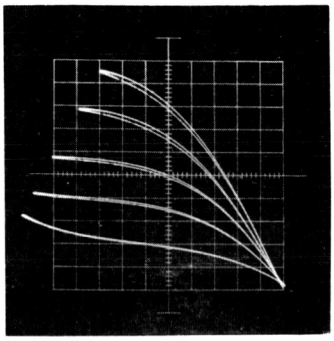


25°C
1.4-1.2V/Step

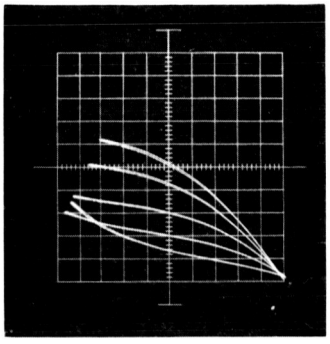
Figure 5.3 Device D-80-22 No. 3; Families of Drain Characteristics of Field-Effect Transistor at the Indicated Temperatures and Gate Drive Conditions. All Families with Upper Gate Shorted to Source and Lower Gate Driven Only. 5V/div horizontal, 0.5 mA/div vertical.



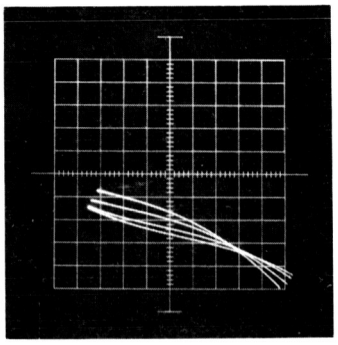
25°C
10V/Step



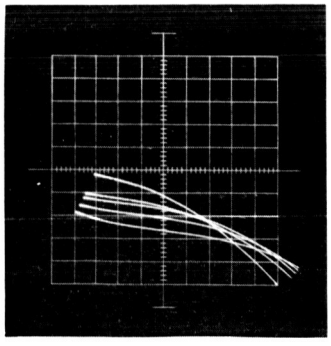
100-40°C
10V/Step



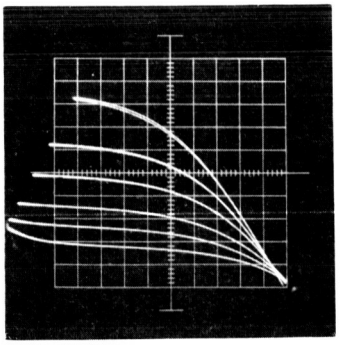
300-330°C
10V/Step



500°C
10V/Step



320°C
10V/Step



25°C
10V/Step

Figure 5.4 Device D-80-22 No. 9; Families of Drain Characteristics of Field-Effect Transistor at the Indicated Temperatures and Gate Drive Conditions. All Families with Upper Gate Shorted to Source and Lower Gate Driven Only. 10V/div horizontal, 5 mA/div vertical.

The most evident consequence of the temperature increase is the decrease in drain current while the transconductance does not decrease very much. The slope of the drain characteristic is also increased with temperature. The same qualitative considerations apply also to the set of characteristics in Figure 5.4. On this device, however, the drain resistance is only approximately 20 KΩ and the maximum transconductance at $V_g = 0$ is about 30μ mhos/mA.

The set of two terminals electrical characteristics listed in Table 5.1 was obtained with the following conditions. The drain terminal was biased positive with respect to a grounded source, while both gates were driven with negative voltage. "Lower gate" and "upper gate" were measured by biasing the respective junctions in forward and reverse with respect to the source common to drain. D75-34 crystal exhibits poor characteristics in every device, with just one exception, the upper gate of D75-34 No. 5. Such a poor yield is in character with the abundance of "bands" and "inclusions" in this crystal.

Crystal D80-20 shows a number of very good diode junctions, but not one device in this crystal shows pinch-off phenomenon. Crystal D80-22 has two devices exhibiting FET characteristics but only two very good diode junctions. The surface of this crystal was not as well finished mechanically and not quite as deeply oxidized as the surface of D80-20. It is possible then that the surface of D80-22 was not sufficiently polished and the mechanical damage was not completely removed by oxidation.

Table 5.1 SURVEY OF SOURCE-DRAIN, LOWER GATE, UPPER GATE CHARACTERISTICS ON FET'S

Crystal D75-34

Unit No.	4	5	6	7	8	9	10	11
Source Drain	V*	V	V	V	V	V	V	V
Upper Gate	V	Good	V	V	V	V	V	V
Lower Gate	V	V	V	V	V	V	V	V

Crystal D80-20

Unit No.	2	3	4	5	6	7	8	9	10
Source Drain	V	V	V	V	V	V	V	V	V
Upper Gate	V	Good	Good	Good	V	V	Good	V	V
Lower Gate	V	Good	Good	V	V	V	V	V	V

Crystal D80-22

Unit No.	2	3	4	5	7	8	9	12
Source Drain	V	Good	V	V	V	V	Good	V
Upper Gate	V	V	V	V	Good	Good	V	V
Lower Gate	V	V	V	V	V	V	V	V

* "V" indicates poor characteristics

Table 5.2 lists R_o values of three crystals. A comparison of R_o values measured over D80-20 and D80-22 seems to indicate that the channel thickness obtained in D80-22 was too large.

The main result achieved during this program, besides the limited number of devices made so far, seems to be the development of a microelectronic process which has been proven to be adequate for the fabrication of field-effect transistors, array of resistors and eventually integrated amplifiers in SiC. The extrapolation involved in our statement rests on the inferences obtainable from the results already on hand. For instance, if the junction properties frequently found in D80-20 crystal were coupled with the channel conductance found in crystal D80-22, much better FET's would be available.

The techniques used in this process, such as mechanical lapping-polishing, chlorine etching, oxidation, aluminum diffusion, Ta-Au contacts metallization are now under sufficient control to achieve reproducibility of results. Considering the device performance demonstrated so far, it indicates that the high purity SiC material used in this project has transport properties which are adequate to implement the expected electronic functions.

Table 5.2 VALUES OF THE UNMODULATED CHANNEL RESISTANCE, R_o ON FET'S

Crystal D75-34

Unit No.	4	5	6	7	8	9	10	11
$R_o(\Omega)$	110	500	300	500	400	300	100	200

Crystal D80-20

Unit No.	2	3	4	5	6	7	8	9	10
$R_o(\Omega)$	4	162	220	42	35	31	50	--	--

Crystal D80-22

Unit No.	2	3	4	5	7	8	9	12
$R_o(\Omega)$	320	3,100	--	800	400	1,300	500	800

6. CONCLUSIONS

Electronic systems capable of operating at temperature of 500°C and above are needed in space vehicles. For low-power instrumentation, control and telemetric applications, the development of high temperature integrated circuits from wide-band-gap semiconductors, such as SiC, becomes a necessity. Such solid-state systems will meet the requirements of light weight, small size, low power consumption, high reliability and long life.

The feasibility of a high temperature SiC integrated circuit was technologically demonstrated during the program period. Principal fabrication processes for SiC monolithic functional blocks have been established. These processes are comparable with the modern silicon integrated circuit technology. A junction-gate type unipolar field-effect transistor was designed and fabricated. The same fabrication procedure can be used for the resistors. Thus, a SiC amplifier can be constructed using the field-effect transistor as an active component.

The conclusions of this investigation can be summarized as follows:

1) Pure n-type SiC crystals having an excess donor concentration of about 10^{17} cm^{-3} and electron mobilities of about 300 cm^2 $volt^{-1}$ sec^{-1} at 25°C and about 40 $cm^2 volt^{-1}$ sec^{-1} at 500°C have been routinely prepared by the sublimation-growth technique. The quality of these crystals is adequate for device fabrication. Further

reduction of the donor concentration is desirable but difficult.

2) The diffusion of impurities in silicon carbide requires temperature near 2000°C. No effective diffusion mask exists at these temperatures, therefore silicon carbide, itself, was used as a mask. The self-masking technique developed permitted the precise fabrication of complicated device geometries. The following sections discuss the separate operations in this self-masking procedure.

2.1) Silicon dioxide has been grown on silicon carbide by heating the crystals at 900°C to 1200°C in a carrier gas saturated with water vapor. The oxidation rate was found to have the parabolic behavior as the steam oxidation of silicon.

In addition to its use in the self-masking process the oxidation technique has also been invaluable for the following:

1) delineation of junctions by virtue of selective oxidation on p-type and n-type material,

2) identification of polarity of SiC crystal, again by selective oxidation of carbon and silicon faces, and 3) removal of damaged material after mechanical processing.

2.2) The photoresist process, routinely used in silicon device technology has been adapted for the fabrication of

the silicon carbide junction gate field-effect transistor.

2.3) The etching of silicon carbide using a chlorine-oxygen-argon gas mixture at elevated temperatures has been developed into a controllable fabrication process. Smooth etch surfaces have been obtained with less than one micron texture at etch depths up to twenty microns.

2.4) A surface concentration of aluminum greater than 10^{18} cm^{-3} has been attained in SiC during diffusion and junction depths up to 38 microns have been diffused with close control ($\sim$ 1μ) of the junction depth. The geometry of the sample holder was improved so that surface decomposition is no longer a serious problem.

3) Through the use of sputtered layers of gold and tantalum and photoresist technique, ohmic alloyed contacts have been made to the source drain and gate regions of the transistor. In the gate region, contacts 20 microns wide by 2000 microns long have been prepared with a larger area for lead bonding.

4) Based on the successful development of the foregoing techniques utilized for the junction gate, field-effect transistor, the fabrication of a resistor network on the same silicon carbide chip should be realizable.

5) Junction gate type, unipolar field-effect transistors have been fabricated and characterized.

7. RECOMMENDATIONS

The development of high temperature integrated circuits should be considered as an integral part of our space research program because of the unique and vital function of these circuits involved in low-power instrumentation, control and telemetric systems. The high temperature operating capability of silicon carbide devices has been established. A sophisticated process for the fabrication of silicon carbide integrated circuits has been developed. An expanded effort is needed to fabricate such solid-state systems with designed characteristics.

It is recommended that further development be made in the following areas:

1) A study of preparing high purity n-type as well as p-type SiC crystals be made for device research.
2) Diffusion of aluminum, boron, nitrogen and phosphorus and arsenic be investigated with increase of surface concentration and surface stability being emphasized.
3) Epitaxial growth is still potentially the best technique for junction formation and should be further studied.
4) The self-masked diffusion process including oxidation and chlorine etching techniques be further studied to improve the precision and reproducibility of the process.
5) The alloying technique be further investigated to increase the uniformity and precision of the contact configuration.
6) The mounting and encapsulation processes be developed.

APPENDIX A

MATHEMATICAL TREATMENT OF THE AMPLIFIER CIRCUIT SHOWN IN FIGURE 2.3

Referring to the ac equivalent circuit shown in Figure 2.3 and assuming that $R_g \gg R_1$, $\omega C_{gs} \ll g_{gs}$, $\omega C_{gd} \ll g_{gs}$, we obtain

$$g_m e_{gs} = e_{ds}\left(g_o + \frac{1}{R_s + R_1}\right) \tag{1}$$

$$e_{out} = \frac{R_1}{R_s + R_1} e_{ds} \tag{2}$$

$$g_m e_{gs} = \frac{R_s + R_1}{R_1}\left(g_o + \frac{1}{R_s + R_1}\right) e_{out} \tag{3}$$

$$= \left(\frac{R_s + R_1}{R_1} g_o + \frac{1}{R_1}\right) e_{out}$$

$$e_{in} = e_{gs} + \frac{R_s}{R_1} e_{out} \tag{4}$$

$$e_{gs} = e_{in} - \frac{R_s}{R_1} e_{out} \tag{5}$$

Then

$$g_m\left(e_{in} - \frac{R_s}{R_1} e_{out}\right) = \left(\frac{R_s + R_1}{R_1} g_o + \frac{1}{R_1}\right) e_{out} \tag{6}$$

$$g_m e_{in} - \frac{R_s g_m}{R_1} e_{out} = \left(\frac{R_s + R_1}{R_1} g_o + \frac{1}{R_1}\right) e_{out} \tag{7}$$

$$\frac{e_{out}}{e_{in}} = \frac{g_m}{\frac{R_s g_m}{R_1} + \frac{R_s + R_1}{R_1} g_o + \frac{1}{R_1}}$$

$$= \frac{g_m R_1}{R_s g_m + (R_s + R_1) g_o + 1} \tag{8}$$

If $g_m \gg g_o$ and $g_o R_l \ll 1$, then

$$\frac{e_{out}}{e_{in}} = A_v \cong \frac{g_m R_l}{1 + R_s g_m} \tag{9}$$

If $g_m R_s \gg 1$, then

$$A_v \cong \frac{R_l}{R_s} \tag{10}$$

APPENDIX B

SUBLIMATION GROWTH OF SiC PLATELETS

Single crystal SiC platelets used for this program were prepared by a closed cavity sublimation technique similar to that described by Lely.[46] The general arrangement for sublimation growth is shown in Fig. A.1, where a charge after sublimation is sectioned through the cavity with grown crystals. The cavity was artificially formed within a mass of SiC grain by a thin graphite tube, 5-7 mils thick, closed at both ends by thicker graphite disks.[3] This graphite tube was sufficiently permeable to allow SiC vapor to pass through so that nucleation and crystal growth could occur on the inner surface, but at the same time was not so permeable as to permit excessive nucleation, which would result in crystal intergrowth. The grain charge and cavity were contained within a graphite crucible positioned within a cylindrical graphite resistance heater. At temperatures near 2600°C the rate of sublimation (under one atmosphere pressure of argon) was sufficient to obtain crystal growth in the cavity. As the outer portion of the charge adjacent to the heater sublimed, vapor was transported towards the cooler cavity region. Crystals grew as hexagonal platelets which were oriented horizontally presenting a surface for radiation to the cavity ends to dissipate heat of condensation. Crystals were found to nucleate during a period of high initial supersaturation as the growth temperature was approached.

Figure A.1 SiC Charge with Growth Crystals

In Figure A.1, lines of recrystallized material can be observed along the directions of vapor transport, and the results of many experiments suggest that the thermal configuration may be evaluated by supposing the isotherms to be normal to these recrystallized "flow lines".

Due to the high temperature used in sublimation growth, and to the relatively porous charge, many materials less refractory than SiC are removed from the charge by fractional sublimation and gaseous diffusion.[2] However the residual concentrations of impurities which substitute in the lattice as electrically active centers are more significant. A reduction in these impurity concentrations was the object of much of the work in this program. In SiC acceptors are aluminum and boron, and donors are nitrogen and phosphorus.[46,47] A reduction in the nitrogen impurity concentration is difficult since the furnace contained a quantity of powdered carbon thermal insulation, on which nitrogen (admitted each time the furnace was opened to the atmosphere) was adsorbed. For this reason even the purest crystals were n-type, with nitrogen as the dominant donor impurity.

The materials used in preparing the charge, and samples of the residual charge after sublimation were analyzed by emission spectrograph and the results are shown in Table A.1. Commercial "green grain" SiC may be purchased and used as the sublimation source, but its use results in the growth of excessively impure crystals. For this reason, pure silicon needles (prepared by a zinc reduction process and obtained from the Allegheny Electronic Chemicals Corp.) were mixed with high purity carbon to prepare the growth charge. The carbon used for the reaction was either AGOT graphite powder (obtained from

TABLE A.1

EMISSION SPECTROCHEMICAL ANALYSIS (PPM)

Typical Analysis

	Al	B	Fe	V	Ti	Mg	Cu	Zn
SiC "Green Grain"(1)	10-20	-	10-20	10-20	5-10	-	-	-
Si Allegheny Fines(2)	-	-	-	-	-	-	1	20
C "AGOT" Graphite(3)	-	-	3	13	-	-	6	-
C "Thermax"(4)	-	-	10	-	-	2	1	-
C Degassed "Thermax"	-	-	-	-	-	-	-	-
SiC Residual Charge	-	-	-	-	-	-	-	-
Minimum detectable limit of the method used	5	5	5	10	10	.5	1	10

(-) Indicates element not detected

Other metals were looked for but were not detected

(1) Obtained from the Carborundum Corp.

(2) Obtained from Allegheny Electronic Chemicals Corp.

(3) Obtained from the National Carbon Co.

(4) Obtained from the R. T. Vanderbilt Co.

National Carbon Co.), or baked and degassed THERMAX carbon powder (obtained from T. T. Vanderbilt Co.). Analysis of the residual charge after sublimation shows that the impurity concentrations were below the minimum detection limit of the spectrographic technique used, even when significant concentrations of zinc were found present in the initial silicon. Mass spectrographic analysis of pure crystals was made using a double focusing spectrographic having a resolution of 500:1. From this analysis chromium was found to be present at a level of about 5 ppm. Chromium has not been observed to be an electrically active impurity in SiC, but the experiments were not conclusive. In one sample phosphorus was also found at a level of 1 ppm, and although its presence has not been explained, its occurrence is evidently unusual and probably not significant. The nitrogen concentration was not determined by mass spectrometry due to interference by the mass peak of doubly ionized silicon from the SiC matrix.

The sublimation furnace was constructed in a manner similar to those reported by Lely[46] and Chang and Kroko[9] and is based on a split cylindrical graphite resistance heater design by Kroll.[48] The furnace was insulated with several graphite shields and a small volume of fine carbon powder, all located within a water-cooled vacuum chamber. Prior to positioning the charge within the heater, all the graphite elements and insulation were baked by heating the furnace to near 2700°C, as measured on the outer surface of the graphite heater. The outer most graphite insulation reached a temperature of ~1000° during the bake-out. After several hours the temperature was reduced to 2000° and the furnace pumped to less than 10^{-6} torr

to increase the removal rate of volatiles. After bake-out the sublimation growth was made in two steps. The first consisted of vacuum degassing for considerable time, typically 48 hours, at a temperature varying from 1300 to 2200°C. This degassing reduced the volume of adsorbed gases and volatile impurities in the charge. At first, the degassing temperature was kept below the melting point of silicon to prevent reaction of the silicon and carbon mixture until the gas pressure level in the furnace, and particularly that of nitrogen, was reduced. The major portion of the degassing was done at a heater temperature of 2000°C, however degassing at 2200°C for an additional 4-6 hours resulted in increased crystal purity. The extended degassing time and the high degassing temperature, along with attention to the prevention of contamination are presumably the reasons for the marked improvement in crystal purity. After degassing, pressures of less than 10^{-6} torr were routinely obtained at 1900°C, however a more useful measure of the furnace condition prior to growth was the degassing rate. This rate was measured as the rate of increase in gas volume after the pumping system was valved off from the furnace. An increase in volume of 100 micron-liters was used as a standard measurement to avoid any non-linear effects in the pressure-time relationship. The degassing rate was primarily a measure of the degassing of the internal parts within the furnace, for leakage into the furnace was below the level of detection with a helium mass spectrometer.

The second step in the program, crystal growth, was carried out only when the degassing rate was reduced to below 200 micron-liters per hour at 1900°C. Since the furnace volume was near 200 liters, this

rate corresponds to a rate of increase in pressure of 1 micron per hour. The sublimation growth was made in an ambient of pure argon gas having a nitrogen concentration of less than 5 ppm (the detection limit of ordinary mass spectrometry fornitrogen). The lines connecting the argon supply tank to the furnace were pumped prior to admission of the gas. Growth runs were made at a temperature of 2600°C for a period of 12-20 hours. Larger crystals were grown by first preparing high purity grain SiC by reacting pure Si and C, crushing this grain under an inert atmosphere and constructing from this denser grain a second charge of higher density. The added mass of SiC allowed longer growth times to be used, resulting in increased crystal size. A few colorless transparent crystals, measuring 5-7 mm across the platelet face, are shown in Figure A.2. The crystals grown were primarily of the 6H polytype, however, pure and mixed crystals of the 4H and 15R polytypes were also observed.

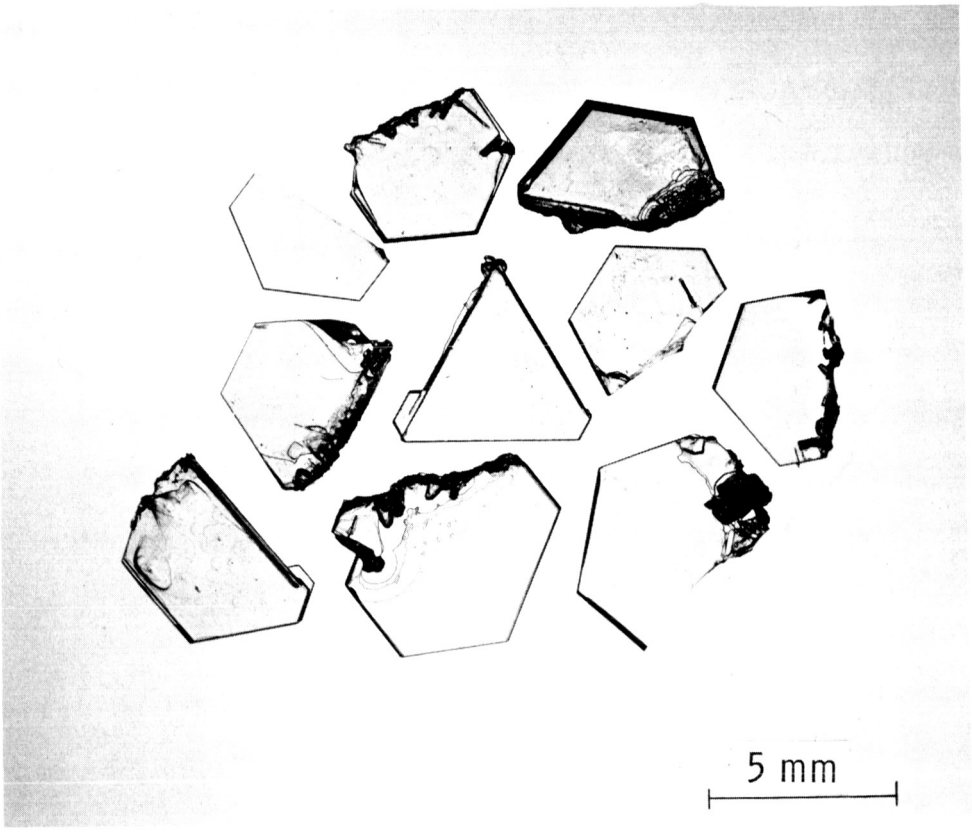


Figure A.2 High Purity Sublimation Grown SiC Crystals

APPENDIX C

EPITAXIAL GROWTH OF SiC BY THERMAL REDUCTION

The feasibility of using the thermal reduction of mixtures of carbon and silicon tetrachlorides with hydrogen for the isoepitaxial growth of silicon carbide, in a manner similar to the epitaxial growth of silicon by the hydrogen reduction of silicon tetrachloride, has been reported.[4] The epitaxial growth of silicon carbide, however, poses the complicating problem in that it exists in cubic and hexagonal phases with the latter possessing a variety of polytypes. It was found in the early work[4] that either phase could be deposited on the basal planes of hexagonal silicon carbide substrates, depending on experimental conditions. Furthermore, the cubic phase was grown at substrate temperatures (brightness) of 1660°-1775°C, and the hexagonal phase was grown on mechanically polished substrates at brightness temperatures higher than 1725°C.

In the work on this program the epitaxial growth of silicon carbide on the basal planes of hexagonal silicon carbide substrates by the thermal reduction technique has been further studied with the aim of preparing homogeneously doped layers. To achieve this, new experimental techniques were devised to prepare epitaxial silicon carbide layers with structural perfection similar to that of the substrate. Doping techniques were also developed to control the conductivity type and carrier concentration of the epitaxial layer. It is established in the epitaxial silicon technology that the structural perfection of the

epitaxial layer prepared under proper conditions of substrate temperature and growth rate is determined predominately by the purity of the growth apparatus and reactants, and the surface condition of the substrate. Contaminants from the growth apparatus and foreign impurities on the substrate surface are the principal causes of imperfections in the epitaxial layer. Because of the temperatures required for the epitaxial growth of hexagonal silicon carbide, the purity of the growth apparatus is more difficult to maintain than in the silicon process. For example, the rf susceptor for the support and heating of silicon carbide substrates must be stable and inert toward silicon carbide and the reactants under the conditions used in the growth process. The choice of susceptor material is therefore limited. Refractory metals react with silicon carbide at high temperatures, and graphite and refractory carbides, including silicon carbide, react with hydrogen to form hydrocarbons. Refractory silicides were found to be more stable under conditions used for the epitaxial growth of silicon carbide. Tantalum silicide-coated tantalum was used as the susceptor in this work with satisfactory results.

The substrate surface should be free from foreign impurities and mechanical damage. The usual etching and cleaning operations are not entirely satisfactory, and it is advantageous that the substrate surface be chemically etched with a gaseous reagent in the reaction tube immediately prior to the growth process. The in situ etching of substrates has been shown to be useful for producing epitaxial silicon layers of good perfection.[49] Chlorine-oxygen mixtures[22] or hydrogen[23] can be used as etchants. The hydrogen etch provides a clean and microscopically smooth surface and is particularly convenient to use in this process.

Electronic grade silicon tetrachloride and carbon tetrachloride were used for the epitaxial growth of silicon carbide. They were introduced into the reaction tube by using a measured amount of hydrogen as a carrier gas. The hydrogen was purified by diffusion through a palladium-silver alloy. Since nitrogen is electrically active in silicon carbide, the silicon and carbon tetrachlorides were thoroughly outgassed to remove dissolved air and the growth system was made gas-tight to minimize any undesirable doping.

Hexagonal silicon carbide platelets with main faces of (0001) orientation grown by the sublimation technique[1,7,18,19] were used as substrates for the epitaxial growth process. They were selected on the basis of optical examination and were etched in a molten 1:3 sodium peroxide-sodium hydroxide mixture to determine the polarity of faces.[50]* The face of the substrates with the desired polarity was then successively lapped with boron carbide and polished with diamond paste. The substrates were subsequently cleaned ultrasonically in hydrofluoric acid and water.

The growth experiments were carried out in a gas flow system, using a horizontal, water cooled quartz tube of 2.5 cm I.D. with gas inlet and exhaust tubes. The silicon carbide substrates were supported on a tantalum silicide-coated tantalum susceptor in the reaction tube, and the susceptor heated externally by an rf generator. Prior to the growth process, the substrates were etched with hydrogen at 1650°-1700°C**

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* The (0001) and (000$\bar{1}$) faces of hexagonal silicon carbide exhibit different etching behaviors toward molten sodium peroxide. One face remains smooth and the other becomes rough in appearance. The former has been shown in a recent work to be the silicon face. (7)

** All temperatures reported here were brightness temperatures measured with a micro-optical pyrometer. These temperatures are about 100°C lower than the true temperature because of the emissivity correction of silicon carbide and the reflection loss at the wall of the reaction tube.

to remove about 10 microns of silicon carbide from the substrate.

During the growth process, the substrates were maintained at 1700°-1715°C. The flow rate of hydrogen was 2.5 ℓ/min, and the concentration of silicon and carbon tetrachlorides in the reactant mixture was 0.04-0.1%. Under these conditions, the linear velocity of the reactant over the substrate surface in our apparatus at room temperature was about 12 cm/sec, and this high linear velocity was essential to provide a uniform flux of the reactant over the substrates.

The structural perfection of deposited silicon carbide layers was evaluated principally by chemical etching technique and optical microscopy. Imperfections in these layers were readily revealed by etching the specimen with a 3:1 NaOH-Na_2O_2 mixture at 700°C for 5-15 sec.

Under proper conditions of cleanliness, the structural perfection of epitaxial silicon carbide layers is affected by the substrate temperature, growth rate, imperfections in substrates, etc. Using a given hydrogen flow rate at a given substrate temperature, the growth rate of silicon carbide depends on the concentrations of silicon and carbon tetrachlorides in the reactant mixture. In this work, equal concentrations of carbon and silicon tetrachlorides were used. Table A.2 summarizes the growth rate of silicon carbide layers on the silicon face of the substrate as a function of the reactant composition; the substrate temperature was 1700°C and the hydrogen flow rate was 2.5 ℓ/min. (The growth rate was found to be approximately 50% greater on the carbon face of the substrate.) The observed growth rate is the net result of

the deposition of silicon carbide by thermal reduction and the etching of silicon carbide by hydrogen. Since the etch rate of silicon carbide by hydrogen is considerable at the temperature used for the deposition process, approximately 2μ/min, the composition of the reactant mixture

Table A.2

GROWTH RATE OF EPITAXIAL SILICON CARBIDE LAYERS AS A FUNCTION OF REACTANT COMPOSITION

(Brightness Temperature of Substrate = 1700°C, H_2 Flow Rate = 2.5 ℓ/min)

Mol % of CCl_4 and $SiCl_4$	Growth Rate, μ/min
0.055	etching
0.060	0.4
0.075	0.7
0.090	polycrystalline growth

becomes very critical. Under a given set of growth conditions, there exists a definite reactant composition at which no net deposition of silicon carbide occurs, and any deviation from this composition results in the etching of the substrate or the deposition of silicon carbide. As indicated in Table A.2, the silicon carbide substrates were found to be etched when the concentration of carbon and silicon tetrachlorides was 0.055% or less. As the concentration of the tetrachlorides was gradually increased, the growth rate of silicon carbide increased rapidly. However, at tetrachloride concentrations of 0.08% or higher, the grown layer had large areas of apparently polycrystalline material.

Chemical etching and optical microscope examinations indicated that epitaxial layers grown at rates of about 0.5 microns/min were similar to the substrate in structural perfection and that defects in the grown layer were usually propagated from the substrate. An example is given in Figure A.3 where a noted defect in a grown layer is correlated, after the removal of this layer, with defects in the substrate. The apparent unevenness of the substrate surface was due to the higher etch rate in the defect areas.

The epitaxial growth of hexagonal silicon carbide layers of good structural perfection was achieved only over a limited temperature range. Using a reactant mixture containing 0.06-0.065% of carbon and silicon tetrachlorides, the grown layer was of cubic phase at temperatures below 1700°C. These layers were characterized by high concentrations of linear etch figures at 60° or 120° to each other (Figure A.4), and these etch figures are presumably stacking fault traces. Hexagonal silicon carbide layers were grown from 1700° to 1730°C, and no growth occurred at high temperatures due to the increased etching rate of silicon carbide by hydrogen. Even when the concentrations of carbon and silicon tetrachlorides in the reactant mixture were increased by a factor of four, no growth was observed at substrate temperatures above 1750°C.

The electrical properties of epitaxial silicon carbide layers obtained by the thermal reduction technique without intentional doping are determined predominately by impurities in the reactant mixture and in the growth apparatus. When these impurity effects are known, controlled addition of dopants into the reactant can yield epitaxial layers

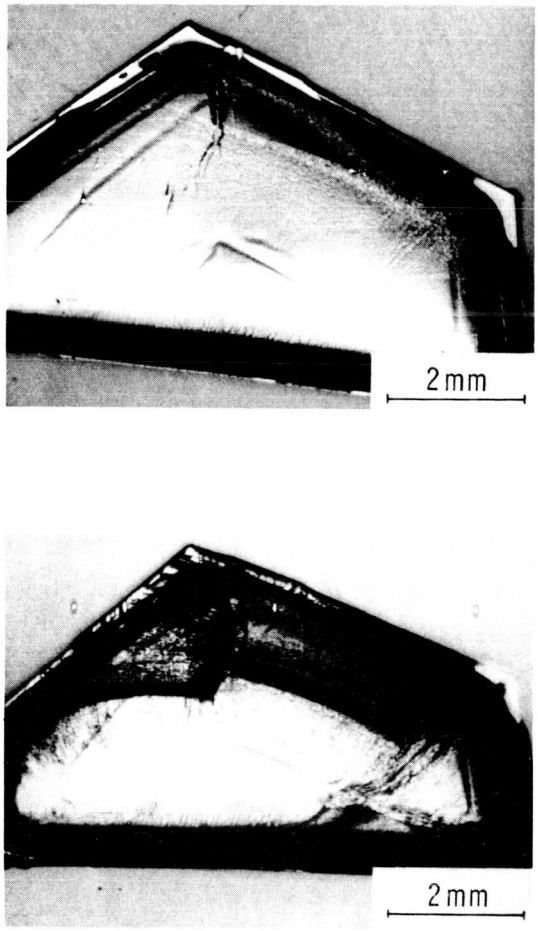


Figure A.3 As-grown surface of an epitaxial silicon carbide layer showing structural defects (upper photograph). These defects were correlated with those in the substrate after the removal of the epitaxial layer (lower photograph).

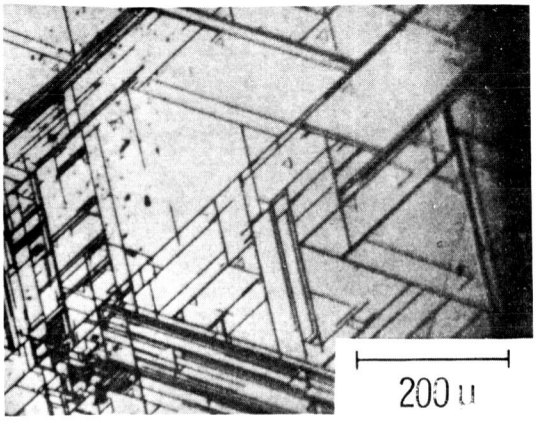


Figure A.4 Linear etch figures associated with stacking faults in a cubic silicon carbide layer deposited on a hexagonal substrate.

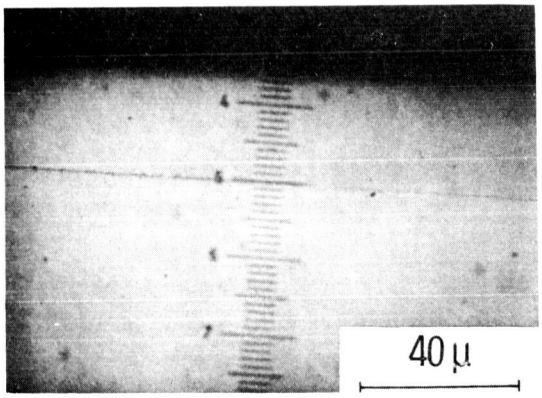


Figure A.5 An epitaxial p-n junction in silicon carbide delineated by electrolytic etching of a vertically cross-sectioned surface.

of desired conductivity type and carrier concentrations. Junction structures can be prepared accordingly by programming the type and concentration of the dopant during the growth process.

Rectifying junctions were made by depositing either n-type epitaxial layers on p-type substrates or vice versa. Figure A.5 shows a p-n junction delineated by electrolytic etching of a vertically cross-sectioned surface. These epitaxial junctions generally exhibited a low forward voltage (1.5 - 2.5 V at 1-5A) with a reverse capability of 50 V at 500°C.

A number of experiments were carried out, aimed at preparing epitaxial junctions with a higher reverse capability, but none of these were successful.

During most of the processing steps described earlier, the device crystal is between 25-35 microns thick. Such thin specimens may be handled but the possibility of breakage is high. Therefore, attempts were made to grow layers of polycrystalline SiC on a SiC substrate. These layers would then act as a mechanical support, simplifying the processing.

This type of layer was produced using dimethyldichlorosilane $\{(CH_3)_2SiCl_2\}$. In the presence of hydrogen this compound is reduced forming the silicon and carbon vapor species. These experiments were carried out in the experimental apparatus used for the thermal reduction epitaxy except that a single saturator filled with $(CH_3)_2SiCl_2$ served as a source of both Si and C. This saturator was maintained at 25°C during the run where the vapor pressure is about 100 torr.

Growth times of 20-60 minutes were used with growth temperatures between 1200°C and 1650°C. Best results were obtained using temperatures of 1400-1450°C. At 1550 and 1650°C, a loosely adherent, yellow powder layer was formed. In one experiment at 1650°C, a 1 mil polycrystalline layer was also grown under the powdery layer. At temperatures below 1350°C the layers were blackish and carbon rich, having no mechanical stability.

Near 1400°C, however, the layers adhered tightly to the substrate. They were mainly composed of elongated rods, more or less randomly packed on the surface. Figure A.6 shows such a layer at 200X. In several cases, the layer surface appeared to have a higher degree of order, and hexagonal platelets were noted. This is shown in Figure A.7.

The growth rate obtained in these experiments was about 20 times that of the normal thermal reduction technique, i.e. about 20 mils/hour. The layer was n-type although no dopant was added to the growth system. The conductivity is presumably due to inadvertant nitrogen doping.

Several crystals were cross-sectioned to reveal the interface between the polycrystalline layer and the substrate. Figure A.8 shows such a layer grown in 1 hour at 1390°C. Figure A.8a shows the layer-substrate as polished. After a short chlorine etch the interface is delineated and the layer shows a polycrystalline nature as seen in Figure A.8b. An enlarged view is shown in Figure A.8c. The bonding between the layer and the substrate was quite good, and the layer

Figure A.6 Polycrystalline SiC Deposit
200X

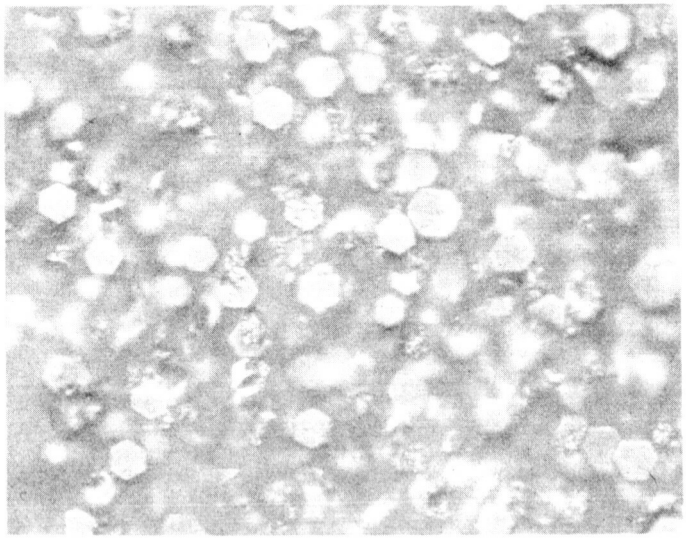
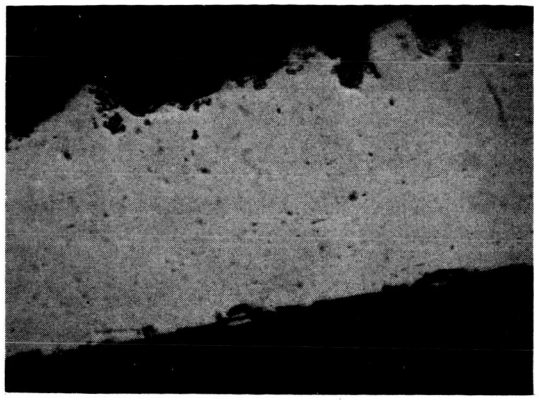
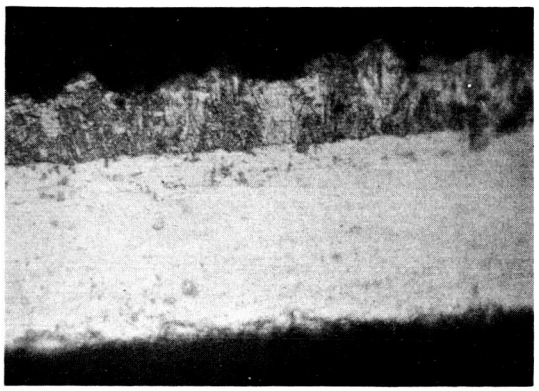


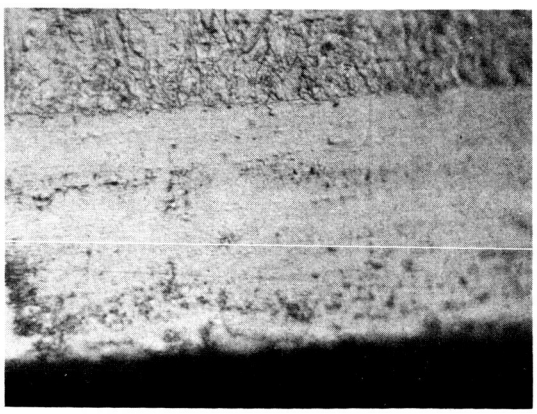
Figure A.7 SiC Layer Prepared Using $(CH_3)_2SiCl_2$ (500X)



(2a) Polycrystal surface on the top (100X)



(2b) Chlorine-etch delineated polycrystal layer on a single crystal substrate (100X) The top darker portion is polycrystal layer.



(2c) Enlarged view of Figure (2b) (225X)

Figure A.8 Cross-sectional views of polycrystalline SiC layer

possessed adequate mechanical properties, but the surface was generally sufficiently irregular that a lapping operation would be needed. (A flat surface is needed so that the other processing steps can be carried out.) Experiments designed to grow layers having uniform surfaces were not successful and this approach was not followed due to a lack of time.

APPENDIX D

EVALUATION OF SUBLIMATION-GROWN CRYSTALS AND EPITAXIAL LAYERS OF SiC

The crystals grown by the sublimation technique were n-type with donor (N_d) and acceptor (N_a) concentrations unmeasurable by ordinary and mass spectroscopy. Therefore an indirect determination of the active impurity concentration was necessary.

The excess donor concentration (N_d-N_a) and the electron mobility were measured between 78^o and 900^oK by Hall and resistivity methods. The Hall mobility is sensitive to the total number of active impurities ($N_d + N_a$), but was also thought to be sensitive to unidentified impurities as well as structural defects. For this reason some other method other than mobility measurement was desired in estimating the acceptor concentration (N_a).

An alternate method of determining trace concentrations of the acceptor impurity, aluminum, is based on the contribution of the aluminum-nitrogen pair to the photoluminescence of crystals excited by ultraviolet light at 4^oK. Patrick, Choyke and Hamilton[38] have made detailed evaluations of the exciton spectra in several SiC polytypes. Although the aluminum concentration could not be determined quantitatively, due to the complex nature of the exciton spectra from the aluminum-nitrogen pairs, the relative intensities were compared on a crystal to crystal basis and these were in turn compared with the Hall mobilities measured on the same crystals. In all crystals compared, a

decrease in the relative intensity of the pair spectra, and hence a decrease in the aluminum concentration, corresponded to an increase in the Hall mobility. Thus to a good approximation, the evaluation of crystal purity may be based on the Hall mobility above, for it is apparent that the mobility is primarily sensitive to trace concentrations of acceptor impurities and as the total number of donor impurities. The Hall mobility is evidently relatively independent of other trace impurities and the structural defects in these crystals.

Resistivity and Hall measurements were made using the van der Pauw technique.[51] Disks of 55 to 250 mils diameter were cut by cavitron from individual crystals. Small 10 mil diameter ohmic contacts were made using gold-tantalum solder on low resistivity samples. Gold leads were bonded directly to the gold-tantalum contacts, and with an antimony doped gold solder to the silicon contact. The contact diameter was small, so that the inter-contact distance to contact diameter ratio was at least 10, minimizing sensitivity to the correction factor in the van der Pauw calculation. The contacted samples were attached to an alumina plate, and the assembly inserted in a fixture which provided external contacts. This fixture was positioned within a furnace for high temperature measurements, and within a small heater immersed in liquid nitrogen for low temperature measurements, so the temperature could be adjusted by equilibration between the heat supplied and the liquid nitrogen.

Laminar layers parallel to the platelet face, such as those shown in Figure A-9, were often observed in SiC. These layers were frequently associated with a polytype change or a twin boundary. A

common example is a "double sided" crystal, 6H on one side and 15R on the other face. Since the sample thickness must be known for the resistivity calculation, the effect of such multilayered structures on the measurements was determined. The presence of layers was found to effect the measurements, so all crystals were checked by microscopy and transmission Laue methods for barriers before measurements were made. When extraneous layers were found present, they were removed by lapping before making the measurements.

Figure A-10 shows the excess donor concentration $(N_a - N_d)$ for 5 growth preparations of differing purity. Curve 1 was obtained using an impure, high resistivity sample known to be compensated with aluminum. The remaining samples were pure crystals having room temperature resistivities ranging from 0.09 to 1 ohm-cm. The carrier concentration from impurities within the highly compensated sample 1 increases rapidly with temperature, while the pure crystal samples tend to saturate at donor concentrations up to 3×10^{17} per cm^3. Intrinsic conduction was not observed at the highest temperatures measured ($\sim 900^{\circ}K$).

The Hall mobilities calculated for this series of crystals are plotted in Figure A-11. The mobilities compared at any one temperature increase in the series as the excess donor concentration increases, with the exception of sample 2 which exhibits the highest mobility and the lowest concentration in the series. Those samples in which the mobility increases as the excess donor concentration increases are likely compensated, recalling that the aluminum-nitrogen pair spectra

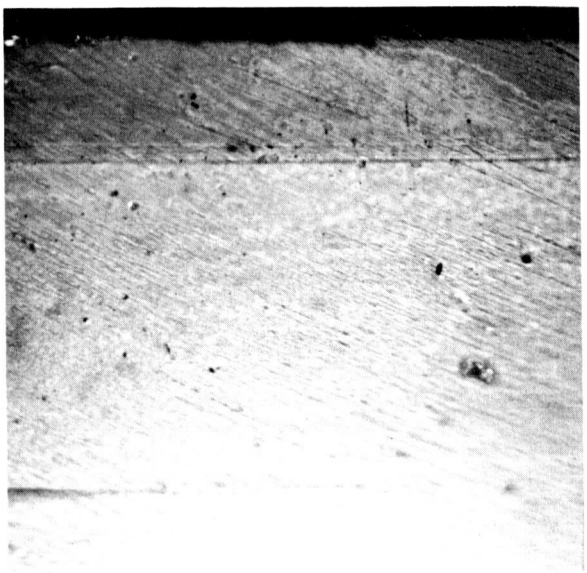


Figure A.9 Laminar Layers in SiC Crystal

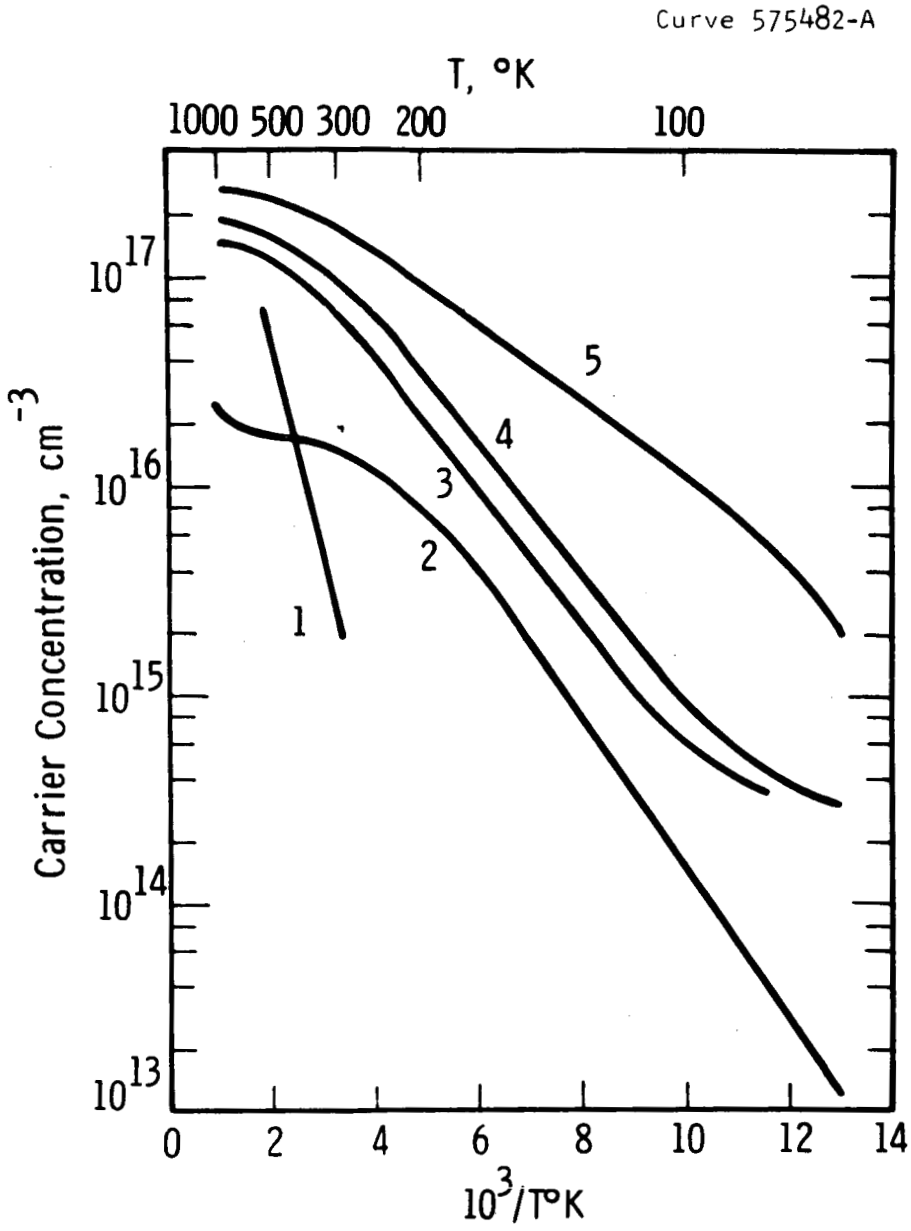


Figure A.10 - Carrier concentration as a function of temperature

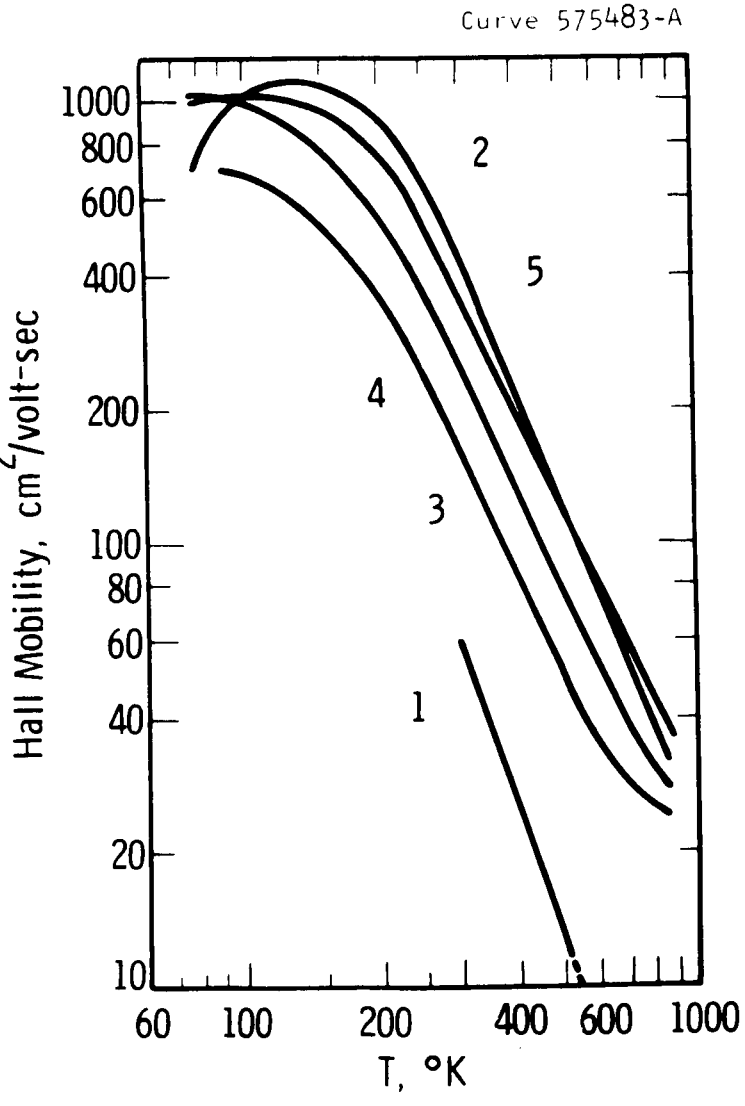


Figure A.11 - Hall mobility as a function of temperature

was roughly correlated with the mobility. The total impurity concentration ($N_d + N_a$) must be decreasing by a reduction in (N_a), while ($N_d - N_a$) is increasing. The characteristics of sample 2 on the other hand may be explained as a reduction in both (N_d) and (N_a), where the nitrogen donor concentration and the compensating acceptor concentration are lower than the other crystals of the series. The mobility value at room temperature for this sample was 462 cm^2/volt-sec, reaching a peak of 1225 cm^2/volt-sec at 130°K. Crystals such as sample 2 were used for fabrication of all-diffused unipolar transistor.

Epitaxial silicon carbide layers grown by the thermal reduction technique without intentional doping were n-type, with representative room temperature resistivity of 0.07 ohm-cm, mobility of 290 cm^2/V-sec, and carrier concentration of 3×10^{17} cm^{-3}. It is believed that these carriers were due to residual nitrogen in the reactants and in the apparatus.

When dopants were introduced into the reactant mixture under conditions yielding epitaxial silicon carbide layers of good perfection, the growth rate was found to increase more than 50%, with degradation in the quality of the layer. To obtain doped layers of good perfection, the concentrations of carbon and silicon tetrachlorides in the reactant were reduced to 0.04% to achieve a growth rate of 0.5 microns/min. The electrical properties of several representative doped layers, measured at room temperature, are summarized in Table A-3. The phosphorus doped layers showed a significantly higher mobility than similarly doped nitrogen or arsenic doped layers.

Table A-3

ELECTRICAL PROPERTIES OF DOPED SILICON CARBIDE

Layers Measured at Room Temperature

Flow Rate of Dopant, mol/min.		Resistivity, ohm-cm	Mobility, $cm^2/V\text{-}sec$	Carrier Concn., cm^{-3}
N_2	6×10^{-3}	0.053	48	2.8×10^{18}
N_2	2×10^{-4}	0.023	52	6.0×10^{18}
PH_3	0.5×10^{-6}	0.07	155	5.6×10^{17}
PH_3	2.2×10^{-6}	0.02	109	2.6×10^{18}
AsH_3	0.5×10^{-6}	0.32	37	5×10^{17}
B_2H_6	2.2×10^{-5}	90.4	2	4×10^{16}

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