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STUDY FOR A FLIGHT FAILURE WARNING AND ANALYSIS PCM SYSTEM

FINAL REPORT

15 November 1965

AUTONETICS
A DIVISION OF NORTH AMERICAN AVIATION, INC.

Approved by

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I. INTRODUCTION

This is the final report of a study conducted by the Autonetics Division of North American Aviation for the NASA Flight Research Center, Edwards, California.

The purpose of the study was to determine the feasibility of mechanizing a flight failure warning system. NASA visualized an airborne digital computer and a PCM data system functioning together to provide failure warning data to a pilots display panel. NASA also intended that the combined computer/PCM system be capable of gathering flight test data for analysis by ground based personnel.

The study has concluded that the NASA failure warning concept is both feasible and practical. Consequently, Autonetics devised the AWARE system (Automatic Warning and Recording Equipment) to illustrate the feasibility of mechanizing such a system.

The AWARE computer/PCM System monitors flight safety parameters and warns the pilot if any operating limit is exceeded. The pilots panel identifies the overlimit parameter and indicates the actual value along with the upper and lower operating limits.

The AWARE system also warns the pilot of any dangerous trends so that he can anticipate overlimit operation and take appropriate preventive action.

In addition, the pilot can select any parameter for display by momentarily depressing the "SCAN" switch and then depressing the "HOLD" switch when the desired parameter appears. Subsequently, the selected parameter will remain on the display and be periodically updated until the pilot selects another parameter or until the computer issues a failure warning. Once the pilot acknowledges a failure warning he can override that particular warning by mementarily depressing the "INHIBIT" switch. The inhibited parameter can be reselected at anytime.

The mechanication of the AWARE system takes full advantage of current advanced integrated circuits and thin film technology. The system uses the same type of integrated circuits and multilayer boards that were developed by Autonetics for the highly reliable Minuteman D37 computer.

The primary purpose of this system is to aid the pilot by warning him of potentially dangerous conditions. Once this warning function is performed, the system serves as a source of additional data for analysis by the pilot and the flight engineer. In this way, the AWARE system takes full advantage of sophisticated electronic data processing without loosing the advantages of human reasoning and human judgment which is absolutely necessary when evaluating flight performance of manned vehicles.

II. SUMMARY

The Autonetics AWARE system fulfills the flight failure warning requirements specified in the NASA Statement of Work NAS4-882. Significant features of the AWARE system include:

A. FAILURE WARNING CAPABILITY

Up to 256 parameters are monitored and compared to normal operating limits. If any parameter exceeds its normal operating range an appropriate failure warning is displayed on the pilots panel and an audio pulse is injected into his headset.

B. DATA RECORDING CAPABILITY

Up to 256 measurements can be recorded in PCM format on an airborne tape recorder or the data can be relayed via a PCM telemetry transmitter to ground based recorders.

C. LIMIT CALCULATION

Operating limits may be loaded directly into the computer memory or the computer can calculate the appropriate limits based upon flight conditions and programmed instructions.

D. DANGEROUS TREND DETECTION

The AWARE system can detect and warn the pilot if any parameter approaches an operating limit at an excessive rate so that the pilot can take preventive action.

E. PILOT OPTIONS

The pilot can call-up any measurement for display in alpha numeric terms and in engineering units.

The pilot can introduce new limits into the computer or he can inhibit any measurement at will.

F. PCM FLEXIBILITY

The AWARE PCM system is extremely flexible. This flexibility is made possible by including a core storage memory in the PCM system itself. The multiplexer program, word format and frame synchronization codes can be stored in the PCM core memory. Thus, many of the traditional PCM hardware modifications can now be accomplished by software change, namely, a PCM program tape can be loaded into the PCM core memory.

In addition, an adjustable PCM output buffer allows the PCM system to supply narrow bandwidth data to on-board tape recorders while supplying wide bandwidth data to the computer. In this way, the AWARE system can help conserve the on-board tape supply by operating at narrow bandwidth and low tape recorder speed during static conditions. Conversely, the PCM system can operate at wide bandwidth, high tape speeds during dynamic test conditions.

G. AWARE ADAPTABILITY

The AWARE telemetry system communicates with the airborne computer through an asynchronous buffer unit which allows the telemetry system and the computer to operate at different clock frequencies. Therefore, the AWARE PCM system could be used to expand the input/output capacity of airborne digital computers already in use.

Another application of the entire AWARE system, including computer, is in the data compression field. Many sensors can be monitored at high sampling rates and the computer can be programmed to eliminate redundant samples. In some cases data bandwidth can be reduced significantly.

III. CONCLUSIONS AND RECOMMENDATIONS

The AWARE system was specifically devised to fulfill the failure warning requirements of the subject NASA contract. Since the essential functional building blocks are readily available, it is recommended that an experimental or prototype AWARE system should be assembled to further demonstrate the feasibility of mechanizing such a system.

IV. AWARE SYSTEM DESCRIPTION

The AWARE system consists of a digital computer, a PCM data system, a display panel, and a tape recorder or radio transmitter. A simplified block diagram is shown in Fig. 1.

A. COMPUTER

The digital computer selected for this system is the Autonetics D26J microminature digital computer. The D26J is ideally suited for the AWARE system since it is a reliable general purpose computer with a random access memory and parallel word transfer capability. The core memory is expandable to over 16,000 words if required.

The D26J integrated circuits and multilayer boards (Fig. 2) have proven reliability since they are identical to those used in the highly reliable Minuteman D37 computer. In addition, the D26J has successfully completed flight tests at Holloman Air Force Base. Additional detailed description of the D26J is contained in later sections of this report.

B. AWARE DISPLAY

1. Data Call-Up

The pilot may request any measurement for display by depressing the appropriate system "SCAN" switch on the display panel (Fig. 3). When the desired parameter appears on the display, the pilot depresses the "HOLD" switch. This selected parameter, along with it's upper and lower limits, will remain on the display and be continually updated until the pilot selects another parameter or until the computer issues a warning alarm pertaining to the system being monitored. Even then, the pilot can override the warning by depressing the "INHIBIT" switch and then select the original parameter again.

2. Confidence Tests and System Self Test

The validity of any sudden warning of impending failure will naturally be questioned by most flight test pilots. Therefore, methods of verifying dangerous conditions must be available to the pilot.

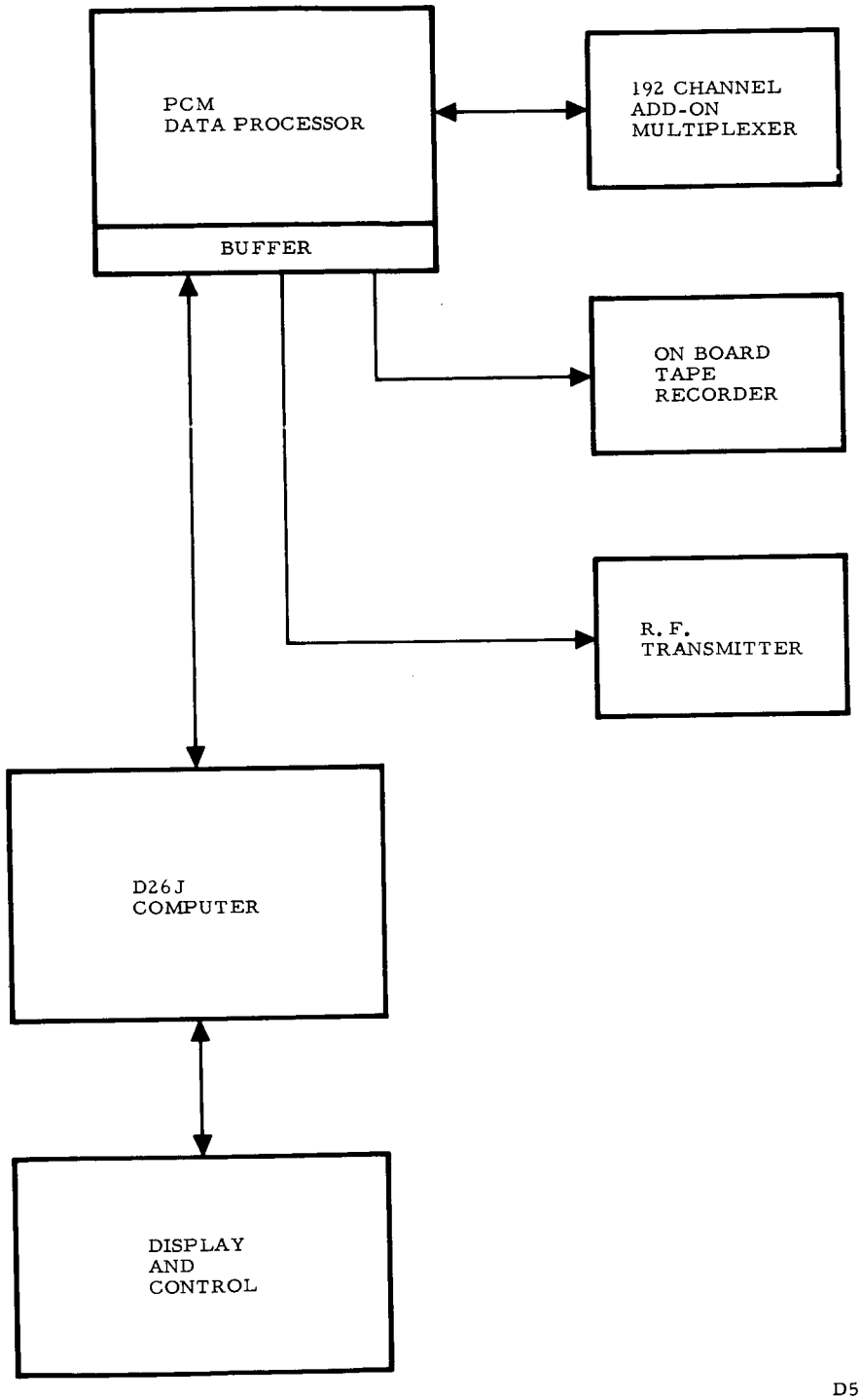

Fig. 1. AWARE System

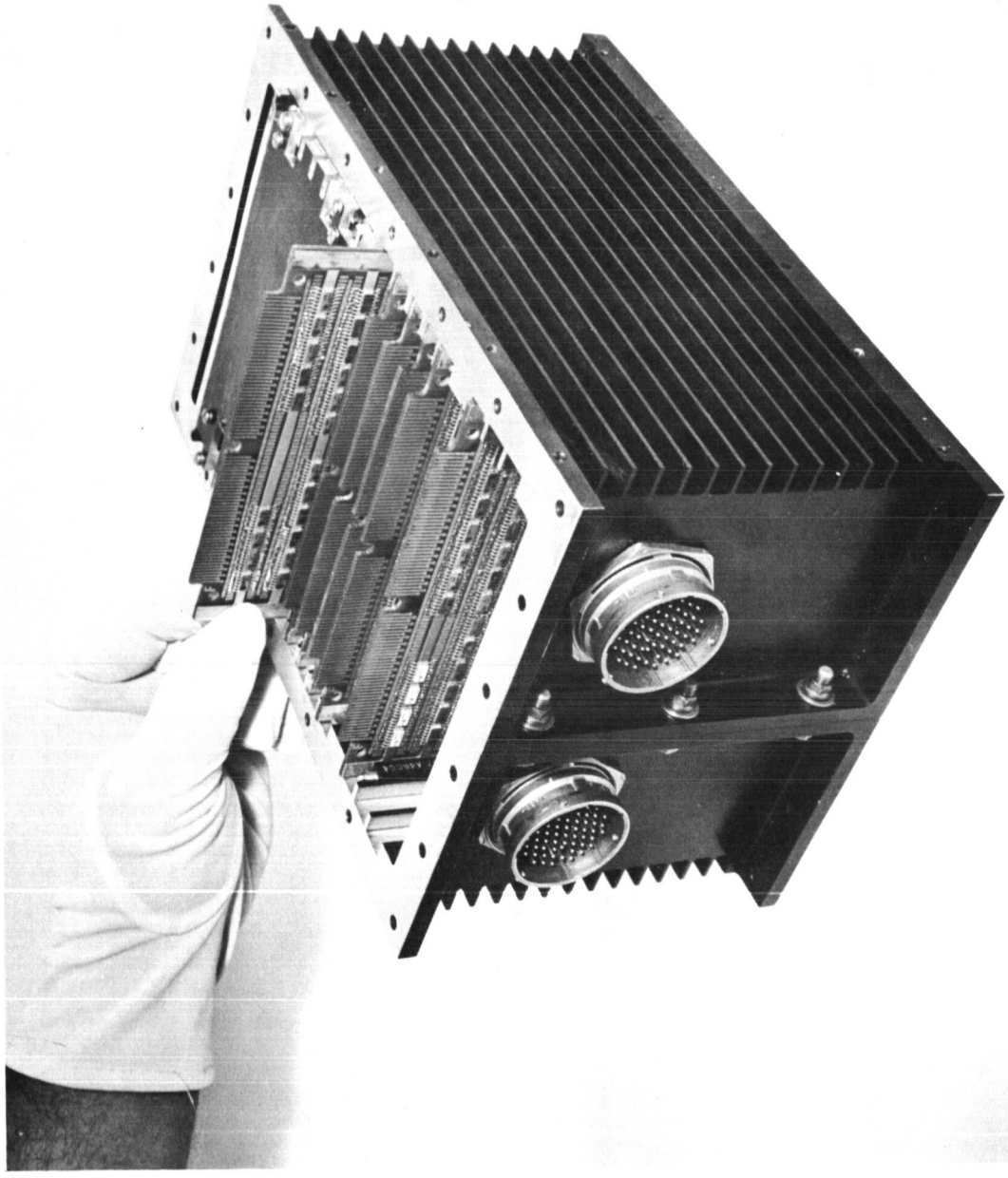

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Fig. 2. D26J Integrated Circuits and Multilayer Boards

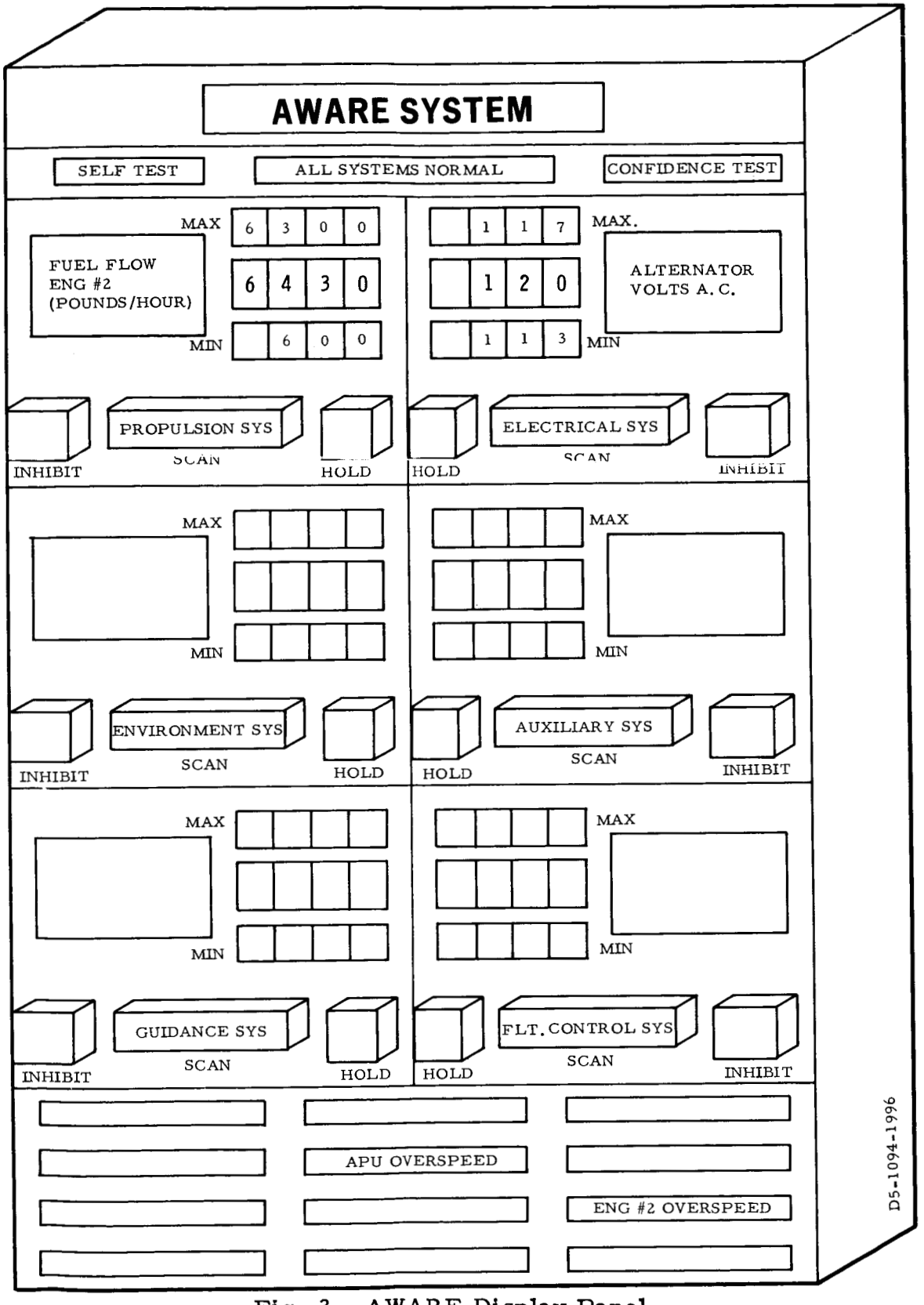

Fig. 3. AWARE Display Panel

The AWARE system allows the pilot to verify proper system operation by three different means. (1) The computer completes a self test of the entire AWARE system once each frame and illuminates a green "SELF TEST" light continuously if all the self test criteria are fulfilled. (2) A green "ALL SYSTEMS NORMAL" light is illuminated when there are no measurements exceeding their respective operating limits and (3) the pilot can initiate a special system test by depressing a "CONFIDENCE TEST" switch which in turn illuminates a green "CONFIDENCE TEST" light.

C. AWARE CONTROL PANEL

The AWARE control panel (Fig. 4), in conjunction with the display, allows the operator to induce a simulated input into any channel of the AWARE system. Actually, the simulated input is routed through one single multiplexer gate, through the A/D converter and then into the computer. However, the computer analyzes the input signal as though it were the actual channel being requested by the pilots panel. The simulated input is converted to engineering units and displayed on the panel as an actual measurement.

This simulated input capability can be used in two ways. First, it allows the pilot to check the AWARE system, by simulating abnormally high or low measurements to ascertain that the warning system will actually generate a warning if an out of limits condition ever existed. Secondly, it allows the operator to insert the simulated value into the computer as a new fixed limit.

This control panel could be installed in the aircraft accessible to the pilot or it could be part of the ground test console whichever the customer desired.

D. PCM SYSTEM

The AWARE PCM Data Processor system shown in Fig. 5 is capable of performing the usual PCM functions of multiplexing and encoding analog information but it also includes some special features which make it particularly useful in the AWARE system.

These special features include:

1. A core storage memory is a part of the basic PCM system.

2. An internal 64 channel multiplexer is included plus a 192 channel add-on multiplexer (Fig. 6).

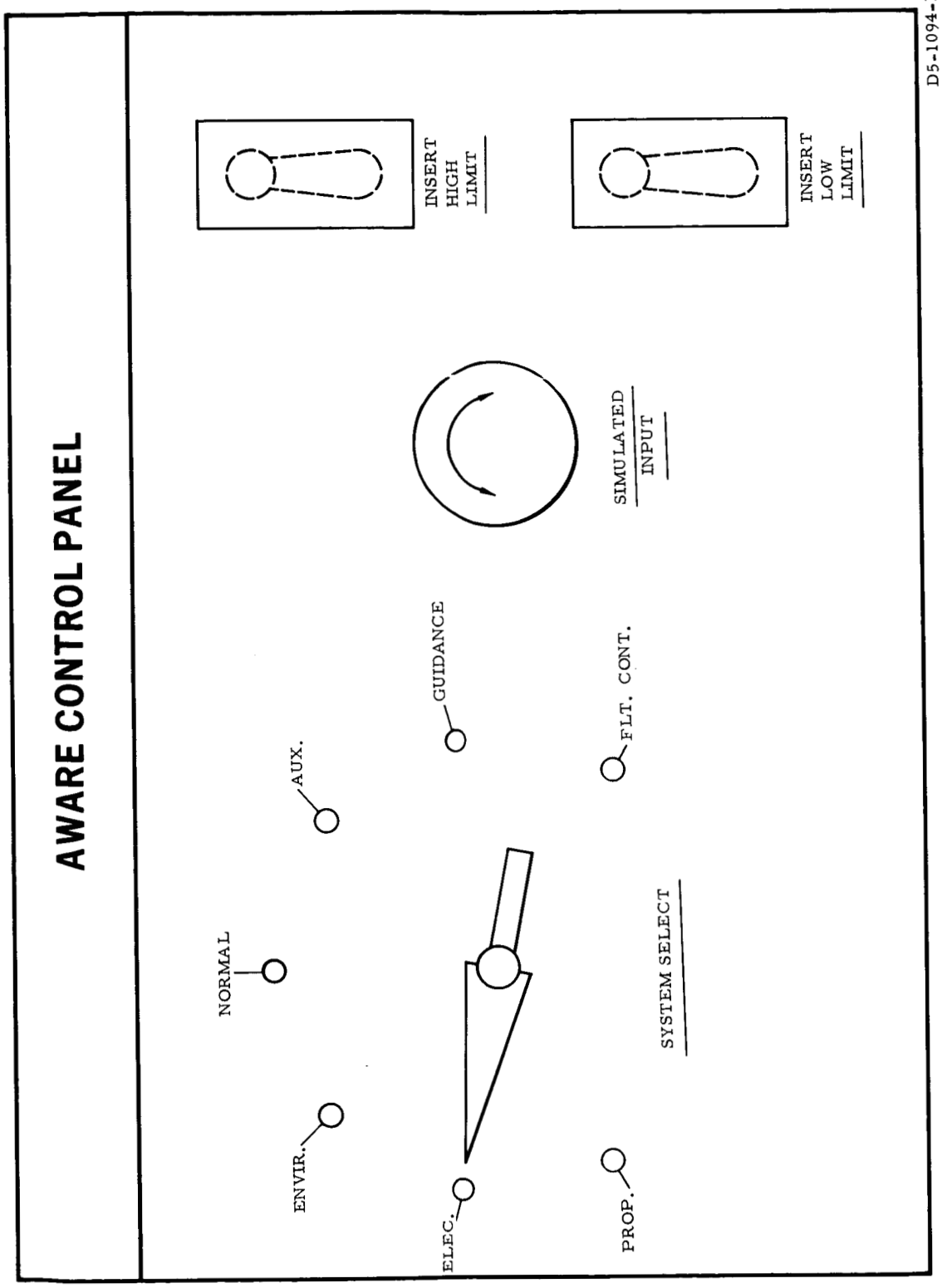

Fig. 4. AWARE Control Panel

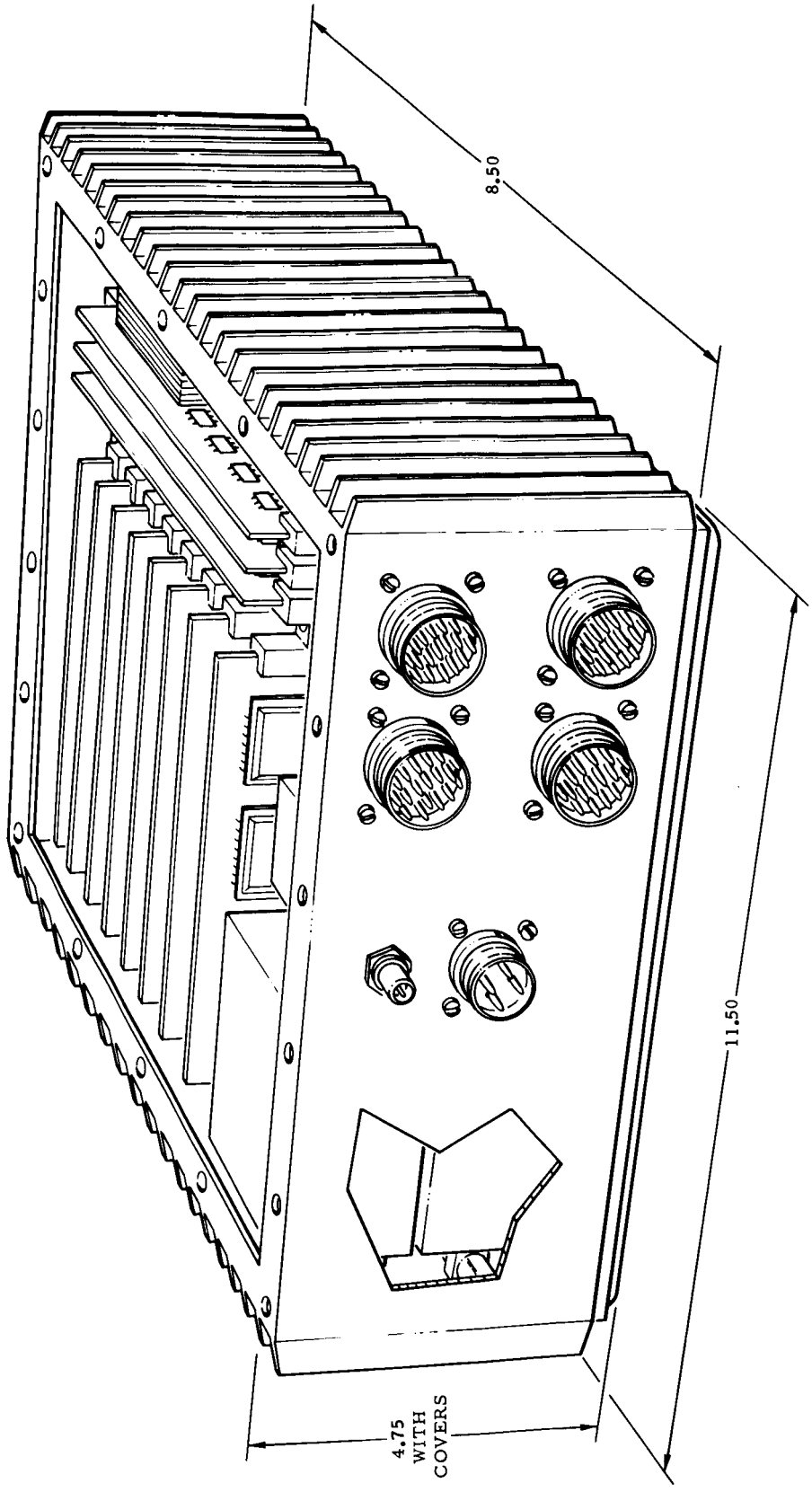

Fig. 5. PCM Data Processor

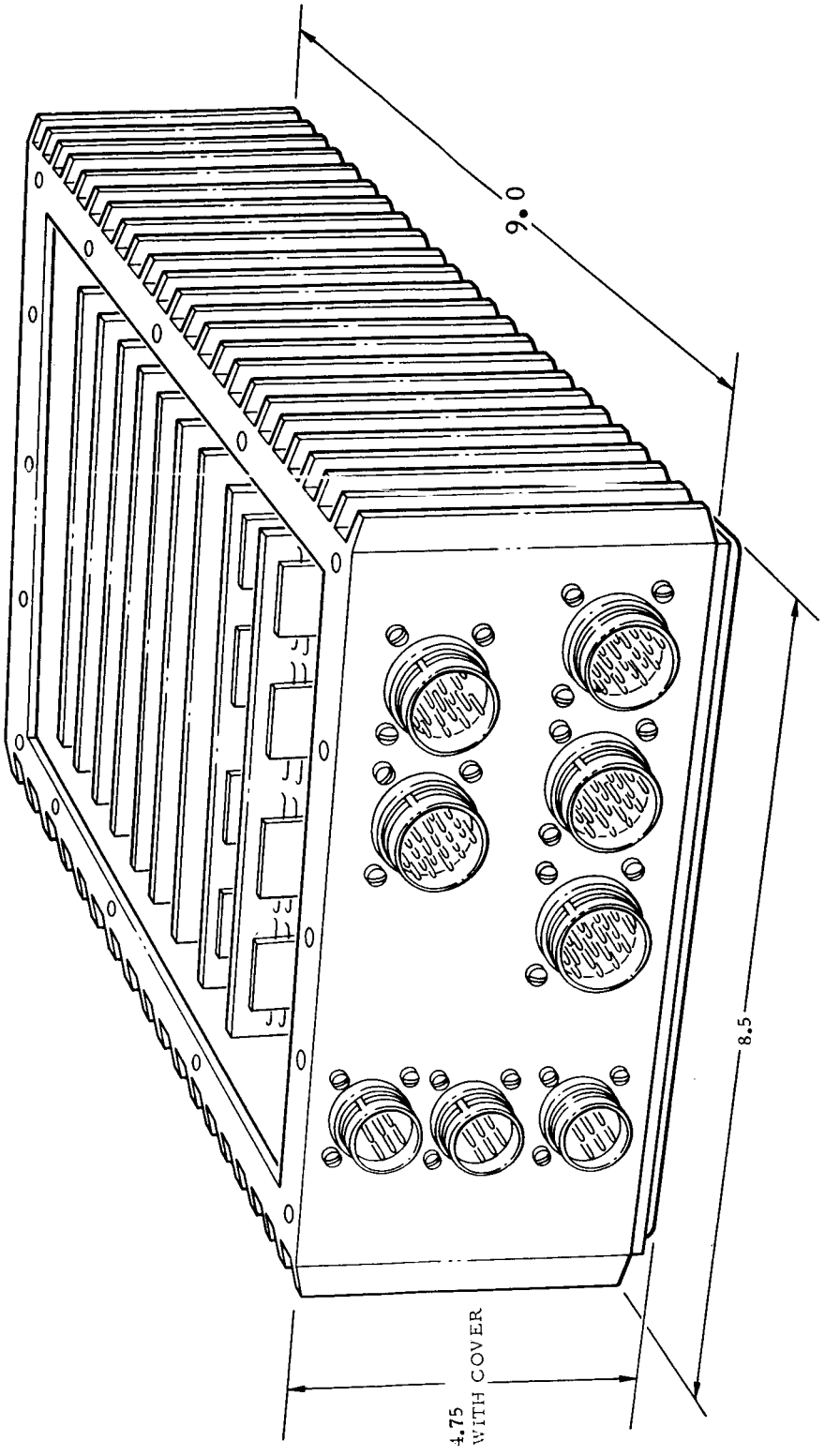

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Fig. 6. Add-On Multiplexer (192-Channel)

3. Both multiplexers are capable of low and high level multiplexing.

4. The multiplexer program is stored in the core memory to designate sampling rate and signal level (low or high level switching).

5. The telemetry output format is controlled by the program loaded into the core memory.

6. A buffer section is included which allows the PCM system to operate asynchronously with various computers.

7. The buffer section also provides for telemetry data bandwidth control by varying the telemetry buffer output frequency. The AWARE PCM telemetry is shown in Fig. 7.

8. The multiplexer gates can be selected either by core storage sequencing or by computer initiated data requests.

E. GROUND CHECKOUT OF THE AWARE SYSTEM

Analog stimulation signals and digital sequencing commands are provided to the system from a test set consisting of an incremental tape recorder, a digital to analog converter and a digital comparator (Fig. 8). In essence, the test set performs an automated end-to-end test of the AWARE system exclusive of the display panel which, of course, must be monitored visually. The analog stimulation signal is routed through one gate of the multiplexer and the digital parameter identification signal is routed into the computer input register once each frame upon command from the computer. Subsequently, the AWARE system processes the stimulation signal as if it were a "call up" from the on board display. Thus, the on board and test set displays are driven to the parameter commanded by the tape reader and the analog voltage supplied is encoded and displayed as an actual measured value in engineering units after processing by the computer. The analog voltage from the test set is programmed so that first it is within limits, next its value exceeds the high limit, and finally, it's value is below the low limit. This, in turn, gives the expected normal, high warning, and low warning indications on both the on board and test set displays. Simultaneously, the system provides a unique computer word back to the telemetry along with digital data equivalent to the original analog voltage supplied by the test set. This, in turn, requires that the telemetry recognize the unique computer word, thus

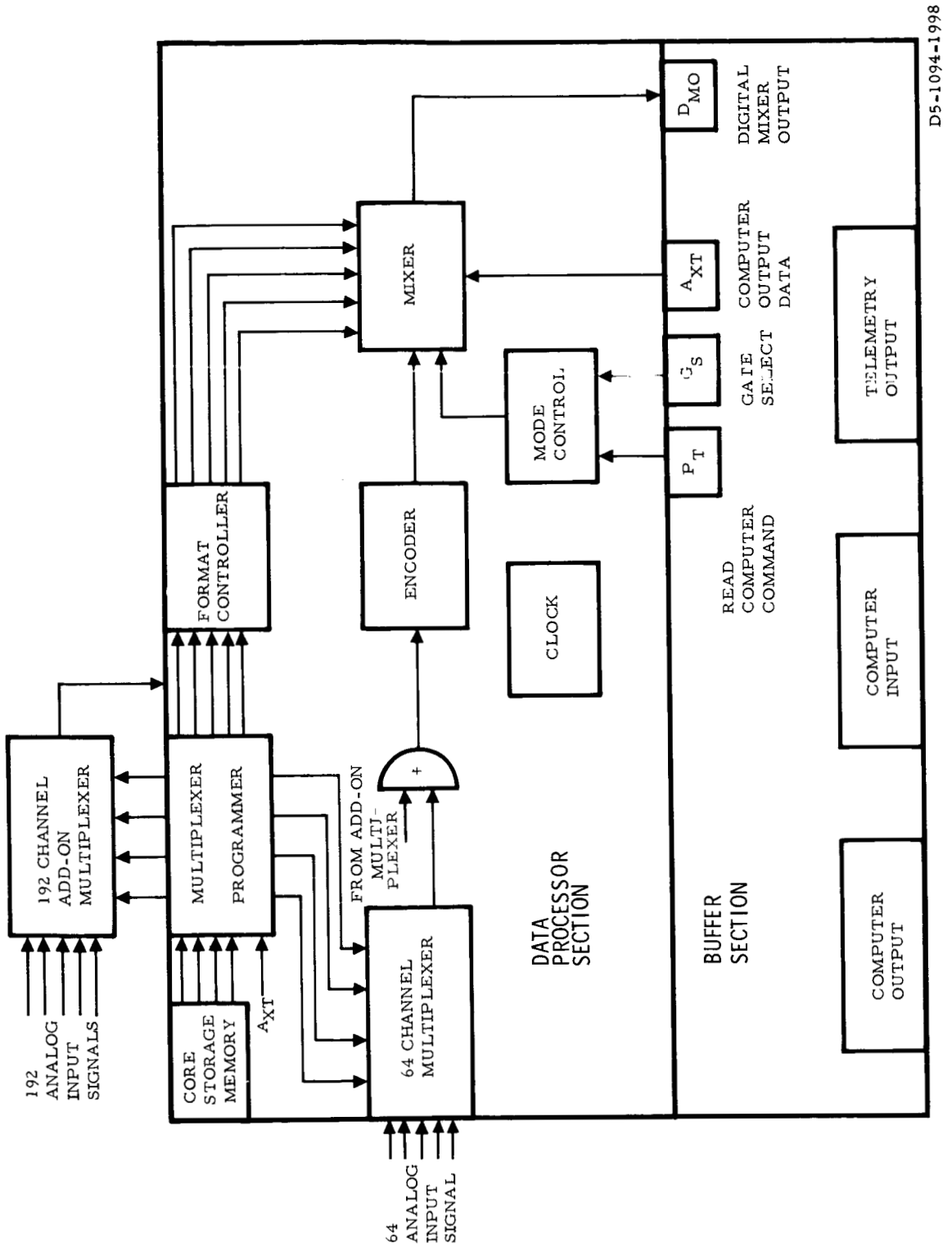


Fig. 7. AWARE PCM Telemeter

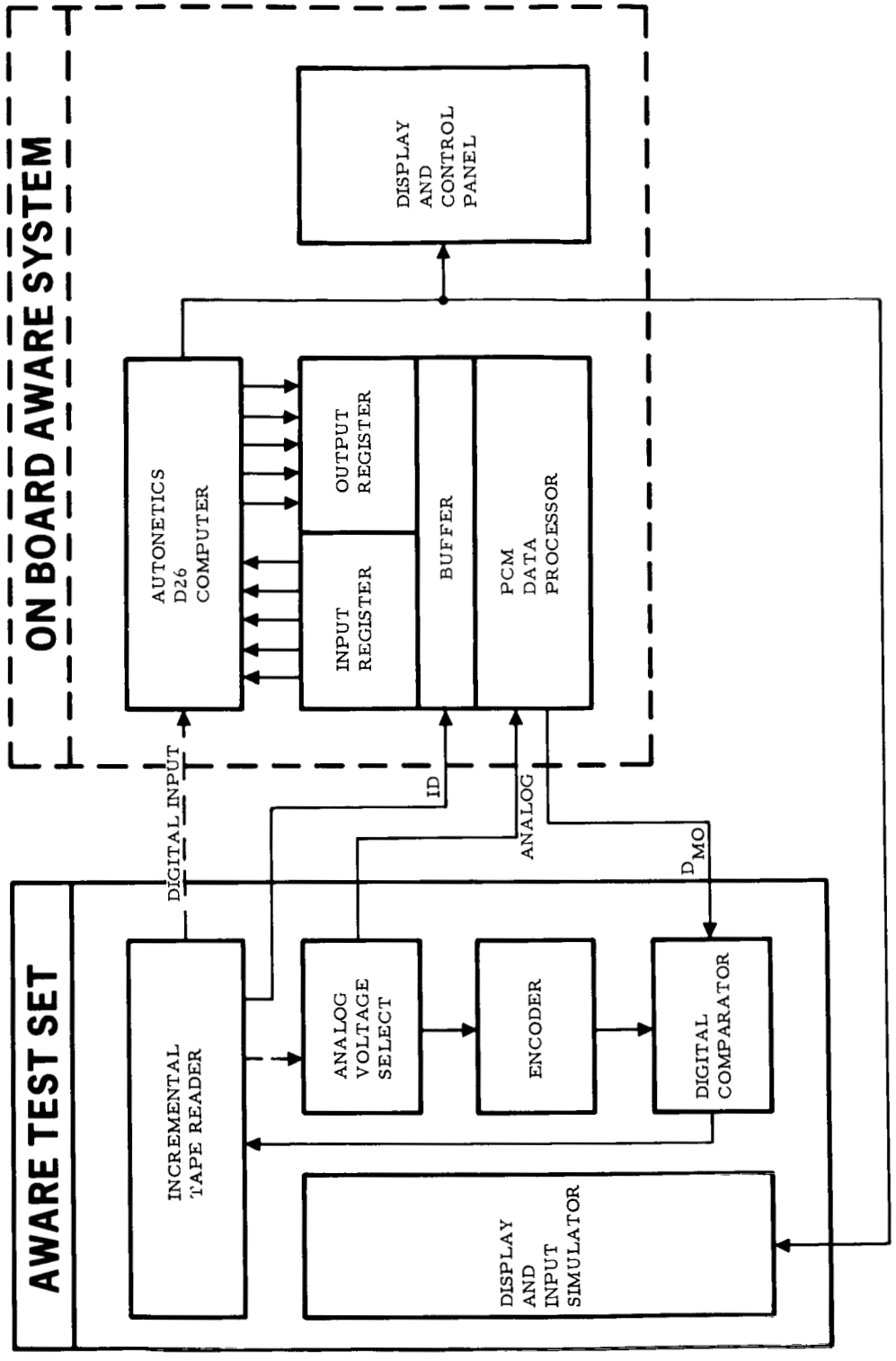


Fig. 8. AWARE System/Test Set Interface

commanding transmittal out to the test set. At this point, the digital comparator compares transmitted telemetry data with encoded test set input data and thus checks the telemetry link. If the comparison is proper, the incremental tape reader is stimulated to the next parameter. This process is repeated until all parameters are checked unless comparisons indicate a malfunction. In this case the test set commands a halt, indicating which channel of data is erroneous and appropriate maintenance procedures can be initiated such as using computer diagnostic tapes to isolate the malfunction to the faulty module.

V. GENERAL DISCUSSION

The primary goal of this study was to provide a practical method of warning the flight test pilot of potentially dangerous conditions so that he might take preventive or corrective measures he considers necessary. A secondary goal was to provide ground based flight test engineers with adequate quantitative data for effective flight performance analysis.

A. COMPUTER CONSIDERATIONS

The ideal flight failure warning system, from a computer utilization viewpoint, would use the PCM telemetry as a synchronized input/output device with random access and parallel word transfer capability. Such a system could possibly be mechanized. In this configuration the computer could issue a data selection command at any time and the telemetry would respond instantaneously with the encoded value of the requested analog measurement. The computer could then analyze the requested measurement to determine if it was within normal operating range. If the data did not exceed normal limits then the computer could command another measurement immediately. If the normal limits are exceeded, then a warning message could be relayed to the pilots panel and the telemetry system could be commanded to record or transmit similar warning data. If all measurements remain within normal operating range then no data would be displayed on the pilots panel and no data could be flagged to telemetry.

Although this system might be acceptable for many applications it probably would not be completely adequate for use in most flight test aircraft because it doesn't provide adequate test data for flight performance analysis purposes.

B. PCM TELEMETRY CONSIDERATIONS

The on-board computer can be an extremely valuable aid to the pilot and to the flight test engineer. However, one of the primary missions of flight test aircraft is to gather quantitative flight test data to evaluate aircraft performance characteristics. Also, when an unexpected malfunction occurs, accurate quantitative data must be available for analysis. This analysis is necessary to determine what action is necessary to prevent failure recurrence. Consequently, there are definite test data requirements for nearly all flight test aircraft.

The ideal flight failure warning system (from a PCM telemetry utilization viewpoint) would use the PCM telemetry system as a sequential input/output device with serial data transfer to the computer and recorders or transmitter. The PCM data bandwidth would be narrow to be compatible with low frequency tape recorders and narrow bandwidth transmitters.

Although this PCM centered failure warning system could be easily mechanized, it would not be acceptable because of the severe computer programming limitations it imposes. The computer must accept the data whenever the PCM system supplies it and, since PCM data samples must be sequential with uniform spacing between samples, the computer program would be extremely inflexible.

C. SYSTEM CONSIDERATIONS

It is clear that an effective failure analysis system must incude a computer with parallel word transfer and random access memory. Likewise, the PCM system must be capable of sequentially sampling test data at a uniform rate and symmetical sampling pattern.

Therefore, it appears that the best method of mechanizing a combined computer/PCM system must involve an unusual time sharing arrangement. Normally, a computer must perform several functions and it is common practice to time share a computer with several input/output devices. However, in this case, the telemetry must perform two functions. It must act as a computer input/output device and it must feed sequential uniformly spaced samples of test data to telemetry tape recorders or telemetry transmitters. In essence then, the PCM system must be time shared between its computer input/output functions and its conventional telemetry functions.

Fortunately, telemetry multiplexers and encoders are capable of high speed operation so that it is practical to time share them. For example, it is feasible to operate a basic PCM system at 300 kilopulses per sec and by time sharing, supply 150 kilopulse data to the computer and 150 kilopulse data to the telemetry recorder. Of course, it is necessary to include buffer registers in the PCM package to allow for this time sharing operation. These buffers require little space though, since they can be mechanized with microminiature integrated circuits.

Consequently, it is feasible to mechanize a failure warning system using an airborne digital computer and a PCM system and still retain the operational capabilities of both pieces of equipment. The Autonetics AWARE system (Automatic Warning and Recording Equipment) is an example of such a system.

D. AWARE COMPUTER PROGRAMMING CONSIDERATIONS

While it was not within the scope of the study to develop and write a digital computer program to accomplish the Early Warning Task, it was necessary to develop a general program philosophy in order to arrive at reasonable estimates for storage and timing requirements. The information presented in the following paragraphs of this section describe the program in general terms and list the basis for the associated memory and timing estimates.

1. D26J Functional Description

The following information describes the programming and program execution characteristics of the D26J computer.

Type: General Purpose. Internally stored

Clock Rate: 500 kilopulses/sec

Time Unit: 2 usec

Memory Type: Random Access Core

Memory Sizes: 1024, 4096, 8192, 16, 384 words

Memory System: Binary with two's complement negative values.

Instruction Word Length: 16 bits

Data Word Length: 15 bits plus sign

Input-Output: as required by customer with respect to the number and types of external communication required. The minimum requirement for the failure warning task is one full word of input and one full word of output.

Address Modification: Accomplished in 512 word blocks by means of a program controllable bank register.

Instruction List: See Table 1

Instruction Execution Times: See Table 1

2. Memory and Time Estimates for Individual Functions

The following data was developed using the D26J 2 usec time unit.

Function	Memory Required (Words)	Time (ms)
Execution Section	1470	49.340
Constants Block	500	- - -
MACH from Pressure Measurements	90	2.240

Function	Memory Required (Words)	Time (ms)
Flare Computer Computations	2500	200.000
True Airspeed	145	1.686
Angle of Attack and Side Slip	190	3.940
Atmospheric Density	25	0.330
Actual Versus Planned Profile	2050	0.380

3. Program Purposes

The primary purpose of the digital computer program is to periodically read values for a predetermined number of vehicle environmental and state parameters, compute values which are functions of one or more of the input values, test the computed values against pre-set limits by one of three methods and, if the test is failed, generate and output sufficient data to identify the failed parameter or system, and display the limits used in the test, the value which failed the test, the type of engineering units in which the data is displayed and turn on an alarm light/signal device.

The three limit test methods are: (1) direct comparison of the converted input value with high and low limits, (2) comparison of the rate of change of the converted input value with high and low limits and, (3) comparison of a proportional rate of change of the converted input value to high and low limits.

A secondary purpose of the program is to accept manually controlled parameter identifications and instructions to: (1) compel the generation and display of outputs similar to the above, (2) inhibit the display even when a test is failed, (3) sequence through a set of parameters at a preset rate, generating and emitting the required data, (4) read and process a synthetic value as if it were the actual input value and (5) change one of the limits used in the test to an indicated value.

Other purposes of the program are to perform as many computations other than the above as time and computer storage space will allow.

Table 1. D26J Instruction List

MNEMONIC	$Code_8$	Bits 2 1	Name	Execution Time (us)
ADD	34		Add	12
AND	66	0 1	Logical AND	12
DIV	70		Divide	108
DPAD	74		Double Precision Add	18
DPLD	76		Double Precision Load	18
DPST	72		Double Precision Store	18
DPSU	64		Double Precision Subtract	18
HPR	04		Halt and Proceed	6
LDB	10		Load Bank Register	6
LDL	36		Load L	12
LDU	26		Load U	12
MPY	60		Multiply	54
RIL	30	0	Read Input to L	12
RIU	30	1	Read Input to U	12
SAL	50		Shift A Left n Bits	6 + 2 n
SAR	40		Shift A Right n Bits	6 + 2 n
SLR	44		Shift L Right n Bits	6 + 2 n
SφL	00		Set Output Lines	6
SSS	62		Store Spread Sign	18
STB	42		Store Bank Register	12
STL	32		Store L	12
STU	22		Store U	12
SUB	24		Subtract	12
TML	02		Transfer on Minus L	6
TMU	16		Transfer on Minus U	6
TRA	56		Indirect Transfer	12
TRB	06		Transfer in Bank	6
TSR	52		Indirect Transfer and Return	18
TZL	12		Transfer if ZERO L	6
WφL	20	0	Write Output from L	12
WφU	20	1	Write Output from U	12
XUL	66	1 0	Exchange U&L	18

4. Definitive Assumptions

The following assumptions were used to define program requirements in addition to those imposed by the stated purposes of the program:

a. Computer Configuration

1. Random access storage

2. Single address command structure

3. Fixed execution times for all instructions

4. At least one full word of input

5. At least one full word of output

b. Program Flexibility

Except for those functions which require a solution to unique analytical expressions or which are non-limit testing computations the program will have the following capabilities (as allowed by the available storage) without requiring any changes to the main program or subroutines:

1. Input any number of data values in any order.

2. Generate and test any number of computer values at individually assigned rates.

3. Accept information from and generate output data for any number of display devices of various types.

4. Modification of the program after being loaded will allow the substitution, deletion, or limit and scaling constant changes for any input or output parameter without disturbing the main program functions or timing.

c. Input Format

All input data for all parameters will be conditioned to have a magnitude between fixed limits and will be binary integers.

d. Output Formats

All output data will consist of one of the following:

1. Parameter Identification - at least 16 six-bit binary code alphameric characters.

2. Limits and Values - four 4-bit binary code decimal characters.

3. Telemetry Data - a parameter identification code plus the input value in conditioned units in one word.

4. Display Device Controls - a full word with specific portions having control over unique device functions.

5. Manually Generated Commands - a full word with specific portions allocated to unique instructions and parameter identifications.

5. Program Structure

a. Discussion

The following, which consists of a description of a program structure or memory allocation scheme, was developed for the purposes of estimating memory and timing requirements for a program which would satisfy the conditions imposed by the program purposes stated in Par. 3 and the assumptions listed in Par. 4 The inclusion of this program in the report does not imply that it is the only method of satisfying the imposed conditions. It is, however, a reasonable and sufficient method of meeting the conditions. The memory and timing requirements which were computed for it are not grossly different from those which would be computed for any other programming scheme which satisfies the conditions.

All of the main parts of the program and its subroutines were partially or completely coded using the instructions for a computer satisfying the requirements stated in Exhibit A of Contract NAS4-883 and the assumed conditions stated in Par. 4.a. (Autonetics D26J). The memory and timing data were obtained by analyzing the coded information and by estimating minor linkage and control functions. All timing information is in terms of computer clock rate (bit rate).

The basic program structure consists of an Execution Section which contains all of the executable sequences (except for those parameters which require a unique solution) and the remainder of the memory contains all of the input/output dependent constants in modular blocks and the unique program sequences.

b. Execution Section

This section accomplishes all of the normal computations, limit testing, control and input-output functions of the program. Its size is independent of the number of parameters being processed either for input or output. It is in the form of a program loop which repeats at a fixed, predictable rate dependent on the number of Constants Blocks being processed. The Execution Section is described in functional form in Fig. 9. The number of words of storage for each function is shown and the time required to process each modular block of constants is noted.

c. Constants Block

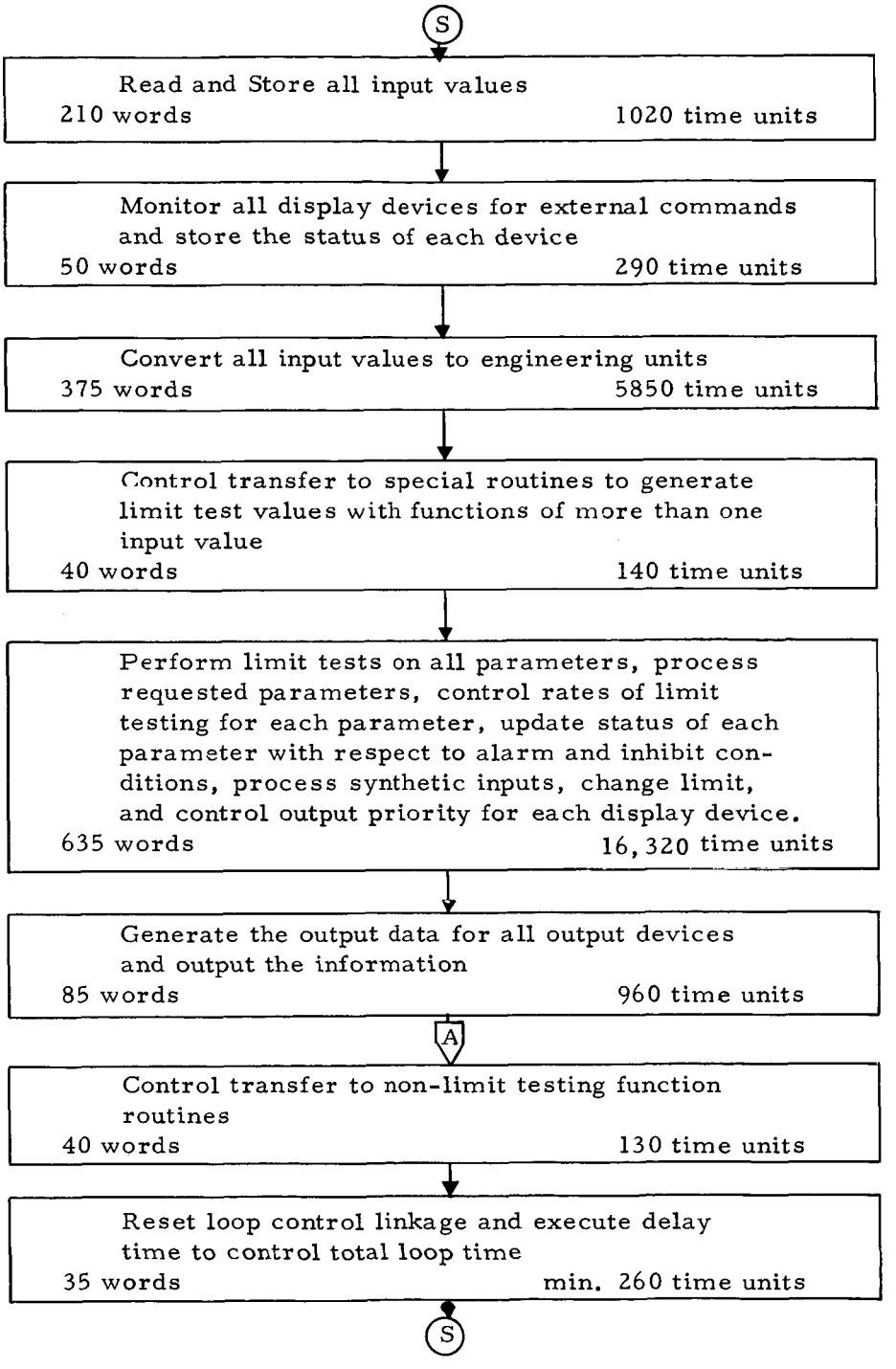
Each Constants Block contains the definition, status and numerical constant words for 16 input parameters, 16 output parameters, 4 display devices, 2 special limit test function controls and 2 special non-limit test function controls. These ratios were determined by (1) analyzing the types and number of input and output parameters, the display device capabilities and the special function requirements and, (2) making the program have the capability of operating in systems of various sizes as determined by the number of input and output parameters required. A format for a Constants Block is shown in Fig. 10 with memory word requirements.

d. Program Dependent System Size Capabilities

The following information indicates the range of system sizes which can be accommodated by the varying number of Constants Blocks in the memory. The Execution Section will process up to 16 constants blocks without a programmed change.

1. 16 to 256 input and output parameters in increments of 16 parameters.

2. 4 to 64 display devices in increments of 4 devices. Each device can have from 1 to 32 parameters assigned to it for display and control.



Total memory required = 1470 words
Total time required = 24,670 time units

Fig. 9. Program Execution Section Diagram

Linear Interpolation tables for converting input values to engineering units (10 words/input parameter x 16 parameters = 160 words)
Raw Input Data Storage
(1 word/parameter x 16 paramters = 16 words)
Converted Input Data Storage (1 word/parameter x 16 paramters = 16 words)
Output parameter constants storage two limits and one constant (3 words/parameter x 16 parameters = 48 words)
Output parameter control, Identification and Status Storage (8/parameter x 16 parameters = 128 words)
Alphameric Identification and Descriptive Storage (5 words/parameter x 16 parameters = 80 words)
Display Device Control, Identification and Status Storage (6 words/device x 4 devices = 24 words)
Special Limit Test Function Transfer Controls (4 per function x 2 functions = 8 words)
Special Non Limit Test Function Transfer Controls (4 per function x 2 functions = 8 words)

Total memory required = 488 words

Fig. 10. Constants Block Memory Allocation

3. 2 to 32 special limit test function routines in increments of 2 routines.

4. 2 to 32 special non-limit test function routines in increments of 2 routines.

e. Memory Time Estimates versus System Size

The following information shown in Fig. 11 represents minimum requirements in that no special functions have been included. The memory and time requirements for special functions are dependent on the complexity of the individual functions and the memory and time requirements would be in addition to the indicated minimum requirements.

f. Special Limit Test Functions Memory and Time Estimates

The following functions are presented to indicate the types of computations which could be performed using one or more input parameters for the purpose of testing the computed result against stored limits. The estimates were predicated on having particular noted types of input data available and the complexity of the analytical expression for generating the required parameter value.

1. MACH from Pressure Measurements

Given: a. p_d, dynamic pressure (lb/ft^2)

b. p_s, static pressure (lb/ft^2)

c. $$MACH = \sqrt{5}\sqrt{\left(\frac{p_s}{p_d + p_s}\right)^{.286} - 1}$$

Memory required = 90 words

Time required = 1120 time units

2. Flare Computer Equations

Memory required = 2500 words

Time required = 100,000 time units

Note: The above was derived from information contained in EM-0363-113 prepared by Autonetics for Contract NAS2-1201.

Number of Constants Blocks	Number of Input/Output Parameters	Number of Display Devices	Number of Special Limit Test Functions	Number of Other Functions	Memory Words Required	Time (1000 units)
1	16	4	2	2	2000	25
2	32	8	4	4	2500	50
3	48	12	6	6	3000	75
4	64	16	8	8	3500	100
5	80	20	10	10	4000	125
6	96	24	12	12	4500	150
7	112	28	14	14	5000	175
8	128	32	16	16	5500	200
9	144	36	18	18	6000	225
10	160	40	20	20	6500	250
11	176	44	22	22	7000	275
12	192	48	24	24	7500	300
13	208	52	26	26	8000	325
14	224	56	28	28	8500	350
15	240	60	30	30	9000	375
16	256	64	32	32	9500	400

Fig. 11. Memory and Time Estimates versus System Size

3. True Airspeed

Given: a. V_i, indicated airspeed

b. A, altitude

c. a 50 point table of density versus altitude

d. Va, actual airspeed = $\left(\frac{p_o}{p_a}\right)^{1/2} V_i$

where p_o = standard air density

p_a = density of altitude A

Memory required - 145 words

Time required = 843 time units

4. Angle of Attack and Side Slip

Given: a. Vehicle orientation: heading, inclination and roll

b. Vehicle Velocity Vector: dx, dy and dz in a known inertial reference system.

Memory required = 190 words

Time required = 1970 time units

g. Special Non-Limit Test Functions Memory and Time Estimates

The following functions are presented to indicate the types of computation which could be performed for purposes other than warning analysis.

1. Atmospheric Density

Given: a. p_s, static pressure (lb/ft^2)

b. T, Temperature in F

c. R, gas constant

d. p, atmospheric density = $\frac{p_s}{(T+540)R}$

Memory required ≈ 25

Time required = 330 time units

2. Actual Versus Planned Profile Computations

Given: a. a 1000 point table of time versus planned profile, (A_i)

b. actual heighth value in a known inertial reference system, (a)

c. at any time (t) output the planned heighth (A_t), the actual heighth (a) and the error, $\Delta a = A_t - a$

Memory required ≈ 2050 words

Time required = 190 time units

h. Change Capabilities

The descriptions of the methods of changing the program are presented in three classes; (1) changes prior to program loading, (2) changes while the computer is connected to the ground control panel and (3) changes immediately prior to or during the mission.

1. Changes prior to loading - all changes for this category require changes in the loading tape, either the generation of a new program tape or portions of the program tape.

2. Changes while the computer is connected to the ground control panels - Any input or output parameter can be deleted, modified or substituted by manually entering a constant or constants into known locations in the appropriate Constants Block. Any special function can be deleted or modified by entering a constant or constants into known locations in the appropriate Constants Block. It is possible to substitute a new special function sequence for an existing one either manually or by a special tape, however, for all but very simple functions, this technique is impractical.

3. Changes immediately prior to or during the mission - No parameters may be added or substituted at this time. Parameters can be inhibited to prevent display, if they are assigned to a manually controllable display panel.

6. Timing and Functional Capability Versus Memory Size

The functional configurations described in this section are presented to demonstrate the types of applications which can be installed in the system and the flexibility of functional formats that can be accomplished without changing the main program. The total time indicated for each case represents the minimum cycle or iteration time interval for the configuration. This time interval can be increased to any desired value by storing an appropriate value in a constant location which is used by a Loop Control Delay Timer.

The numbers of input parameters, output parameters special functions and display devices for each of the configurations are specifically for the configuration and do not represent the limits for the associated memory size. The total possible number of each of these items which can be controlled is a function of the number of Constants Blocks in the configuration. Each Constants Block can control 16 input parameters, 16 output parameters, 4 display devices, 2 special limit test functions and 2 special non limit test functions.

a. Capability with a 4096 Word Memory

1. Typical Configuration

64 input parameters, 64 output parameters, 3 special limit test functions, 1 special non limit test function and up to 16 display devices

Function	Memory Words	Time (ms)
Control 4 constants blocks at 49.340 ms/block	3470	197.4
Angle of Attack and Sideslip	190	3.9
MACH from Pressure Measurements	90	22
True Airspeed	145	1.7
Atmospheric	25	0.3
Unused Words	176	- - -
Totals	4096	205.5

2. Configuration with no Special Functions

80 Input Parameters, 80 Output Parameters and control of up to 20 Display Devices

Function	Memory Words	Time (ms)
Control 5 Constants/Blocks at 49.340 ms/Block	3970	246.7
Unused Words	126	- - -
Totals	4096	246.7

b. Capability with an 8192 Word Memory

1. Typical Configuration

128 input parameters, 128 output parameters, 4 special limit test functions, 1 non-limit test function and control of up to 32 display devices

Function	Memory Words	Time (ms)
Control 8 Constants Blocks at 49.340 ms/Block	5470	394.7
MACH from Pressure Measurements	90	2.2
True Airspeed	145	1.7
Angle of Attack and Sideslip	190	3.9
Atmospheric Density	25	0.3
Actual Versus Planned Mission Profile	2050	0.4
Unused Words	222	- - -
Totals	8192	403.2

2. Configuration with Flare Computer Computations

128 input parameters, 128 output parameters, 1 special limit test function, flare computer computations and control of up to 32 display devices

Function	Memory Words	Time (ms)
Control 8 Constants Block at 49.340 ms/Block	5470	394.7
Flare Computer Computations	2500	200.0
Angle of Attack and Side Slip	190	3.9
Unused Words	32	- - -
Totals	8192	598.6

3. Configuration with No Special Functions

The following configuration will allow 208 input parameters, 208 output parameters and control of 52 display devices.

Function	Memory Words	Time (ms)
Control 13 Constants Blocks at 49.340 ms/Block	7970	661.4
Unused Words	222	
Totals	8192	661.4

VI. AWARE PCM DETAILED DESCRIPTION

A. PCM CIRCUIT DESIGN

A conservative design approach was taken on the application of microcircuit technology. Proven analytical techniques were used to determine the optimum method of mechanizing each circuit function. The result of these analyses indicate that a combination of hybrid thin film circuits, discrete components, and integrated circuits would provide a minimum sized package.

The physical description is as follows:

1. Basic PCM Data Processor

The physical characteristics are:

Size	8-1/2 x 11-1/2 x 4-3/4 in.
Weight	17 lb
Power	58 w at 28 vdc
Cooling	None required between 50 and 85 F ambient air

2. Add-On 128-Channel Multiplexer

The physical characteristics are:

Size	8-1/2 x 8-1/2 x 4-3/4 in.
Weight	12 lb
Power	26 w at 28 vdc
Cooling	None required between 50 and 85 F ambient air

The Basic PCM System and the Add-On 192-Channel Multiplexer are packaged as shown in Fig. 5 and 6. The packages are made from cast aluminum. The packaging design incorporates in its design provisions for RFI integrity. In addition, the packaging design will have thermal characteristics which will allow continuous operation of the units in an ambient environment between 50 and 85 F.

1. ADC Operation

During the telemeter analog and analog frame sync words, the ADC converts multiplexed analog voltage samples into a digital representation. For the telemeter analog word, the digital representation is serially stored in an 8-flip-flop encoding register. Each bit of this stored digital information is telemetered to the ground station one bit time after it is generated.

The philosophy in the design of the ADC is to generate and present to a comparator an analog voltage which converges toward the level of the analog input signal with each successive bit time. The generated analog voltage is obtained by a resistive ladder network which is controlled by the 8-flip-flop encoding register. The encoding process may be called one of "successive approximation." The analog equivalent of the binary register is successively compared with the input signal until agreement (within the accuracy of the comparator) occurs. During telemeter analog words, the analog data is encoded to 8 bits, accurate to the least significant bit (20 mv). During word 0, the analog data is encoded to 9 bits which is accurate to 10 mv. During the encoding of a telemeter analog word, the serial readout of the flip-flop encoding register is feasible because the flip-flops are required to contribute to the ladder network in a sequential order. In order to readout at the first bit time of a telemeter analog word, encoding must commence during the last bit time of the previous word which may be either a telemeter analog word, computer word, or analog frame sync word.

2. Drift Correction - Encoding During the Analog Frame Sync Word

During segment "A", word 0 of each analog frame sync word, the ADC is calibrated to a precision ground level. The ground level is programmed from the multiplexer to the input of the ADC and encoding of this signal follows a process similar to that explained in the previous discussion. However, in the encoding of the precision

ground level, an additional flip-flop is added to the 8-flip-flop encoding register and the ADC is increased to 9-bit resolution. Since an additional flip-flop has been added to the encoding register, the encoding process must be prolonged for one extra bit time as compared to encoding during an analog word. After the ground signal has been encoded, the three least significant flip-flops of the encoding register are copied by three drift correction flip-flops. The drift correction flip-flops then remain frozen throughout an analog frame until the ADC is calibrated again at the next word 0.

3. Basic Multiplexer

The basic multiplexer is a precision high-speed, 64-channel analog multiplexer providing random channel selection, high common mode rejection, programmable gain selection, and sample-and-hold capability. The basic multiplexer will be an integral part of the basic PCM Digital Data Processor and will operate separately or in conjunction with the Add-on 192-channel multiplexer.

The multiplexer will be capable of multiplexing 0 to 50 mv and 0 to 5 v analog signals and providing a gain of 100 or unity, respectively, as programmed by the DDP. The overall accuracy of the multiplexer subsystem including the sample and hold circuit will be 0.5 percent of full scale for the 0 to 5 v channels and 0.6 percent of full scale for the 0 to 50 mv scales. The input impedance to the multiplexer will be greater than 500 k for the closed condition of the multiplexer switch, and greater than 1 megohm for the open condition of the multiplexer switch. The feedback current to the data source for a 0 to 50 mv channel will not exceed 300 nanoamperes and for the 0 to 5 v channels will not exceed 1 microampere. Under command of the DDP, the multiplexer will select the analog input channel and provide a 0 to 5 v PAM output to the ADC at a data rate of 25,600 words per second.

The multiplexer unit shall be capable of rejecting dc common mode potentials over the range of a minus 10 to a plus 10 v with a common mode rejection ratio of 5000:1 on 5 v channels, and 20,000:1 on 50 mv channels.

The multiplexer unit shall be capable of rejecting ac common mode potentials of 200 mv. The 5-v channel ac common mode rejection ratio is 5000:1 at dc decreasing linearly with increasing frequency to 2000:1 at 10 kc. The 50 mv channel ac common mode rejection ratio

is 20,000:1 at dc decreasing linearly with increasing frequency to 2000:1 at 10 kc. The multiplexer will provide this common mode rejection capability for data source impedances of up to 1000 ohms resistive or 5000 ohms shunted by 0.5 uf to 150 uf. To aid achievement of this common mode rejection capability, the multiplexer will contain its own dc-to-dc converter power supplies.

A block diagram of the basic multiplexer is shown in Fig. 12. The operation of the multiplexer is explained in the following paragraphs, with the aid of the timing and sequencing diagram, Fig. 13.

4. Programming and Configuration Control

The loading of the multiplexer program into the DDP multiplexer programmer is accomplished from the ground test equipment utilizing a conventional tape reader and associated loading electronics. The mechanisms associated with transferring the information from the program punched tape into the core memory is basic memory loading technology. The configuration control, and programming of the multiplexer program tapes will be discussed to illustrate the programming flexibility attainable while still maintaining strict configuration control of the multiplexer programs.

The task of programming may either be accomplished by a computer or manually. In either case the basic considerations of the number of channels available, required sampling rates, and maximum total number of samples per second must be observed.

Upon obtaining the desired program the programming information is transferred to punched tape. The tape may be punched and verified by a computer. Configuration control of the punched tape may be maintained similar to Instrumentation Control Drawings, or Airborne Computer programming tapes.

5. Multiplexer Timing

The timing as it relates to the multiplexer, for one 27-bit data word, will be discussed to provide details on the sequencing. At the leading edge of bit time T_1, all multiplexer gates will be disabled by the Data Strobe Signal. The six channel select lines and two multiplexer select lines for the next channel to be selected will be true from the DDP during the multiplexer select data-on-time as shown in Fig. 13, and will be clocked into the multiplexer register on the

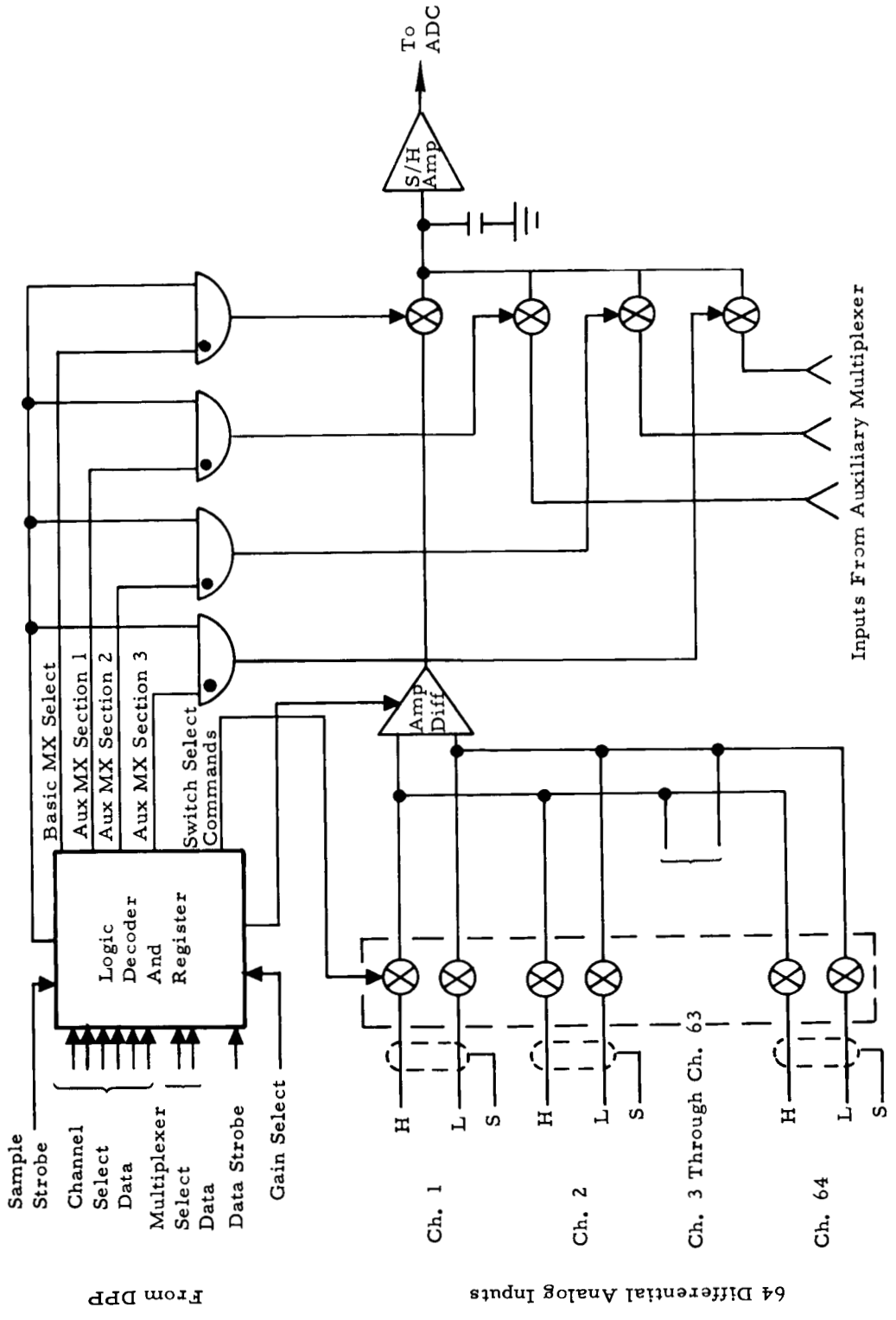


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Fig. 12. Basic Analog Multiplexer

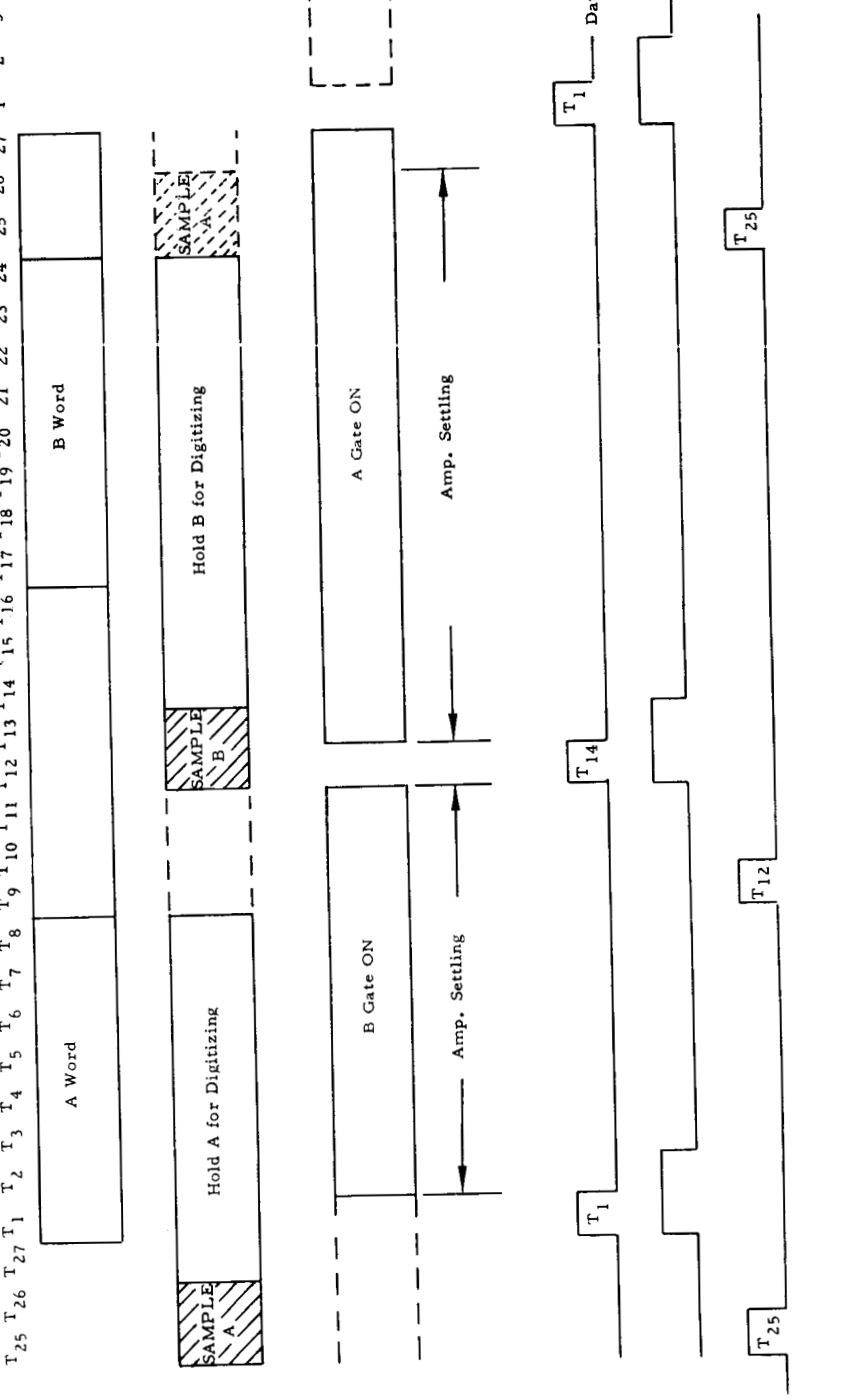


Fig. 13. Multiplexer Timing and Sequencing Diagram

lagging edge of the Data Strobe. The multiplexer differential amplifier will settle out in the "B" gate on-time, and will be sampled by the sample-and-hold during bit times 12 and 13 for approximately 5 usec. The "B" word will be digitized during bit time T_{16} through T_{23}. The The Data Strobe will disable the multiplexer switches on the leading edge of T_{14} and clock in the "A" gate select information on the lagging edge of T_{14}. The multiplexer differential amplifier will settle out during the subsequent 12-bit times and will be sampled by the sample-and-hold circuit starting on the leading edge of T_{25} for approximately 5 usec. The "A" word will be digitized during bit times T_{27} through T_7 (T_8 during word 0) of the subsequent word. This sequence will be repeated for each data word.

The basic multiplexer will consist of the following four functional blocks:

1. Logic decoder and register
2. 64-channel differential input solid state switching circuit
3. A precision wideband differential amplifier
4. A high speed sample-and-hold circuit

a. Logic Decoder and Register

The Logic Decoder interfaces with the DDP (Multiplexer Programmer) and decodes the programmer signals for sequencing the multiplexer system. The control lines from the DDP consist of 11 signals. These signals are:

1. Six channel select signals: providing random selection of any one of the 64 analog input channels.
2. Two multiplexer select signals: providing selection of either the basic or one of the inputs from the three 64-channel groups of the add-on multiplexer.
3. One gain select signal: providing the appropriate gain selection for a 0 - 50 mv or 0 to 5 v channel.

4. One data strobe signal to disable the analog switches during the decoder register transition period.

5. One sample strobe signal to control the sample-and-hold circuit.

The Logic Decoder is transformer coupled to the DDP control lines and floating to provide necessary isolation for common mode rejection requirements.

b. Differential Input Switching Circuit

The switching circuits will be constructed using hybrid thin film techniques employing discrete field-effect transistors (FET's) as the switching elements for the differential input channels. The hybrid thin film circuits will be enclosed in metal cans to provide electrostatic shielding of the low level input signals.

The discrete FET's were selected in preference to the integrated FET switches because they are field-proven to provide highest performance, reliability, versatility and ease of fault location.

The field-effect transistor is ideally suited for switching applications caused by the following desirable characteristics:

1. Low "ON" offset voltage

2. Low "OFF" leakage current

3. High "OFF" resistance

The basic limitations of the FET as a switching element is the variation in resistance of the ON condition and the capacitance to the gate circuit. With a differential amplifier input impedance of 500 k ohms or greater, the loading error of the two gates in each circuit will be less than 0.12 percent. The actual error will be considerably less than this figure, since the amplifier will initially be fabricated to offset the nominal FET switch resistive loading error, thereby reducing the error to the variation in the resistance of the FET's, rather than their absolute resistances. The actual error should be less than 0.04 percent. By using isolated power supplies in conjunction with the FET switches, the gate capacitance effect can be reduced considerably, so that the error contribution, including common mode current, will fall well within the acceptable value.

A representative schematic diagram of a differential switch using the FET switch element is shown in Fig. 14. When the control signal is true, the FET Q_1 will appear as a low resistance, thereby applying a positive voltage to the gate load of Q_2 and Q_3. Field-effect transistors Q_2 and Q_3, which make up one differential input signal channel switch, will then turn on, thereby closing the double pole single throw switch.

c. Differential Amplifier

The multiplexer differential amplifier provides the isolation and amplification of the multiplexed analog signals. Because of the important role the amplifier plays in the multiplexer subsystem a detailed discussion of the design considerations are presented in Appendix B. A summary of the capability provided by the amplifier is given in Table 2.

Table 2. Summary of Amplifier Capability

Voltage Gain:	Program selected steps of 1 and 100	
Input Impedance:	Greater than 500 k shunted by the transistor input capacity	
Output Voltage:	0 to +5 v nominal	
Settling Time:	In 30 usec to within 0.05 percent of final value	
Common Mode Rejection:		
DC Common Mode:	Common Mode Potential ±10 v	
	Source Impedance:	1000 ohms or less resistive
		10 to 5000 ohms resistive, shunted by 0.5 to 150 uf
	Rejection Ratio:	20,000:1 for 50 mv channels
		5,000:1 for 5 v channels

Table 2. (Cont)

AC Common Mode:	Common Mode Potential	200 mvac
	Source Impedance:	As defined under dc Common Mode Source Impedance
	Rejection Ratio:	20,000:1 at dc decreasing linearly with frequency to 2000:1 at 10 kc for 50 mv channels
		5000:1 at dc decreasing linearly with frequency to 2000:1 at 10 kc for 5 channels

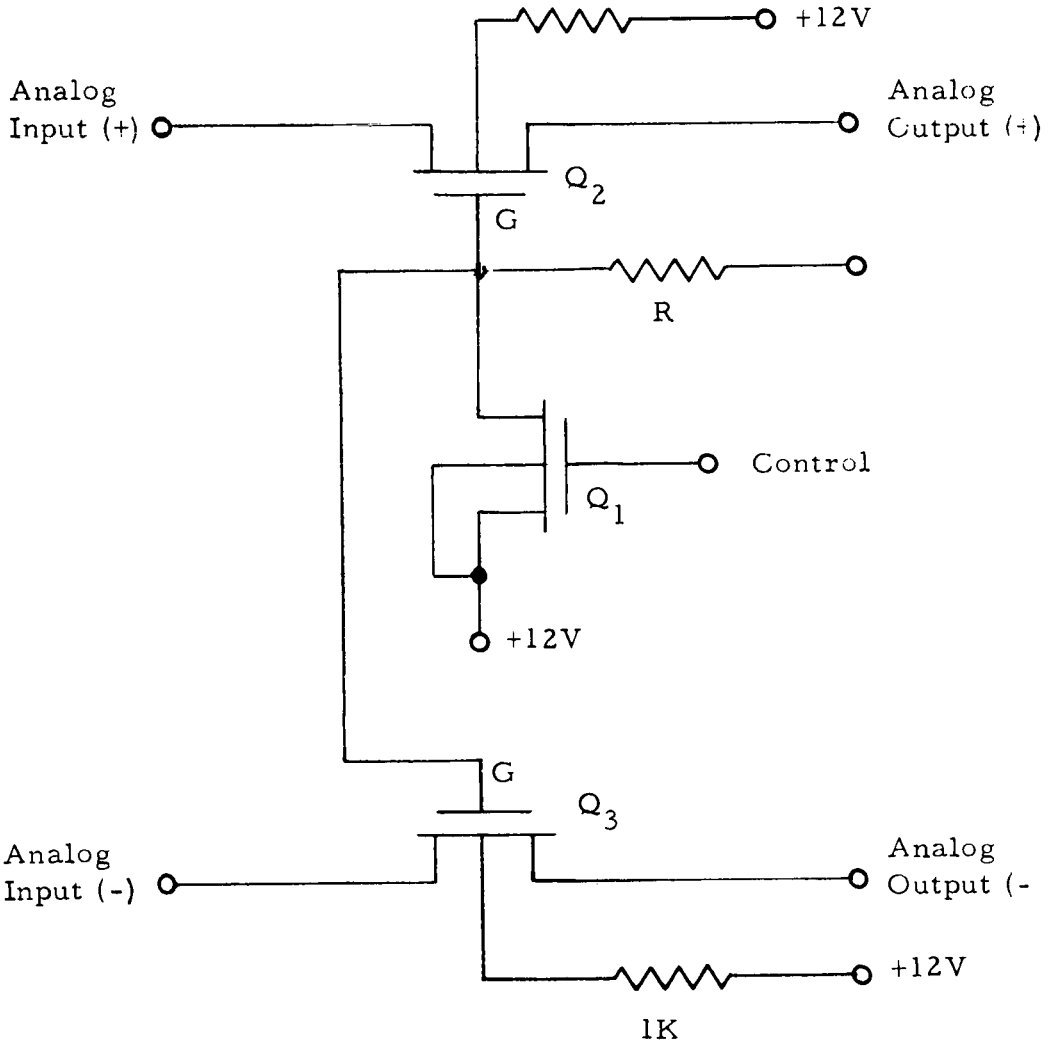
The programmable gain capability allows the use of a single differential amplifier. The voltage gain to be applied is selected by the DDP independently for each of the 64 channels.

d. Sample and Hold Circuit

The sample and hold circuit will be a hybrid thin film circuit using uncased transistors and diodes. The following requirements will be met by the sample and hold circuits:

SAMPLE TIME	Maximum of 5 usec occurring during the final 5 usec of amplifier settle time
HOLD TIME	Minimum of 11 bit times (2.89 usec/bit)
ACCURACY	Better than 0.15 percent of full scale
DATA SELECTION	Multiplexes the four differential amplifier outputs from the basic and add-on multiplexers

The sample and hold circuit provides the capability for accurately measuring at finite points in time the varying dc outputs from the differential amplifier(s). It provides a constant, (held), output to the ADC during the digitizing process and allows the differential amplifier(s) to settle on the next data sample.



R, can be either a discrete resistor,
thin film resistor,
or a properly biased FET.

Fig. 14. Double Pole, Single Throw FET Switch

6. Add-On 192 Channel Multiplexer

The Add-On Multiplexer unit will be very similar to the Basic Multiplexer unit, with the exception of size. It will provide the capability for multiplexing 192 different channels and its differential amplifier outputs will be multiplexed into the Basic Multiplexer Sample-and-Hold circuit under DDP control. The circuit boards from the Add-On Multiplexer and the Basic Multiplexer will be interchangeable.

A block diagram of the add-on multiplexer is shown in Fig. 15. As can be seen by comparing the basic multiplexer shown in Fig. 12 with Fig. 15, the Add-On Multiplexer consists of three 64-channel multiplexer sections identical to the Basic Multiplexer with the exception of the Sample and Hold circuit.

7. Packaging

a. PCM Data Processor Packaging and Thermal Characteristics

(1) Physical Description.

(a) Packaging. The PCM Data Processor is packaged in a cast aluminum chassis having the required structural and thermal characteristics in addition to its primary function of containing the electronics and power supplies. The two power supply modules are mounted adjacent to the power input connector.

In order to achieve the best thermal characteristics with the restriction that no additional cooling outside of the compartment ambient is available, heat dissipating fins have been made an integral part of the chassis. Aluminum was chosen because of its high thermal conductivity in addition to other desirable physical properties. To achieve maximum heat transfer, the electronics boards are fastened to support structures with captive screws torqued down to effect a thermal interface of the board with the chassis. Analysis and tests have shown this method to be thermally efficient, and reduces the machining required when using board guide slots and other mechanical retainers.

Radio frequency interference integrity is maintained through the use of an RFI seal between the chassis and covers. The power input is protected by the use of an RFI filter integral with the input power connector. The unit, in addition to the RFI seal, has an environmental seal protecting the electronics against dust and moisture.

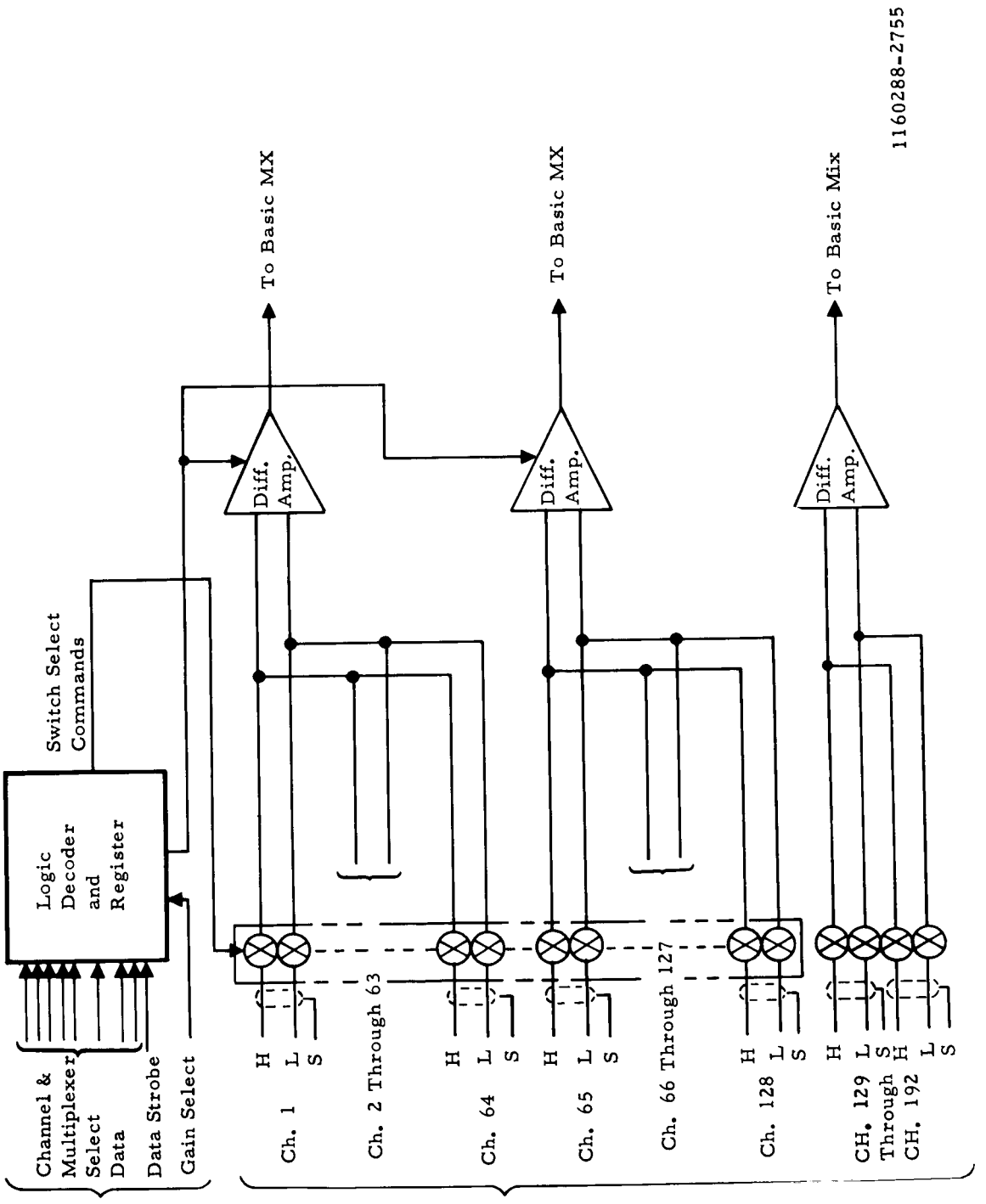


Fig. 15. Add-On Analog Multiplexer

Interconnection of the electronics is effected through a single multilayer interconnect board (MIB) utilizing pin and socket connectors. The concept of design and construction have been perfected on the Minuteman II D37 Computer and utilizes the same connectors and fabrication techniques. Interconnections within the power supply section are effected by conventional point-to-point wire harness techniques.

(b) Thermal Considerations. The thermal design of this unit is similar to the method used in the D37C computer except that this unit makes use of free convection and radiation to remove heat from the package while the D37C computer is water cooled.

Heat generated within the unit is conducted along heat conducting strips on the module boards, through a controlled thermal joint and into the chassis. Once the heat has entered the chassis it is distributed uniformly throughout the chassis and is removed from the unit via free convection and radiation. To facilitate heat transfer from the unit, the ends are finned with 1/8 in. thick, 0.5 in. high fins. Radiation heat transfer is enhanced by providing the unit with a high emissivity (dull black) surface finish. The chassis material will have a minimum thermal conductivity of

$$92 \ \frac{\text{BTU Ft}}{\text{Hr Ft}^2\text{F}}$$

b. Add-On Multiplexer Packaging

The add-on multiplexer will be packaged in an 8.5 x 8.5 x 4.75 in. cast aluminum chassis. The weight of the complete unit will be less than 12 lb. The chassis will provide necessary structural and thermal characteristics in addition to containing the circuit electronics.

To provide circuit card interchangeability and system uniformity, the add-on multiplexer chassis will be very similar to the basic PCM system chassis. The basic structure, thermal, and RFI characteristics will consequently be similar to those previously discussed, and will not be discussed here.

B. D26 DETAILED DESCRIPTION

Small size, low power consumption and reliable operation are prime requirements in airborne and space-system computers. To meet these objectives, Autonetics developed the D26J family of micro-miniature digital computers.

D26J logic design features parallel word transfer and computation, integrated circuits, coincident-current core memory, and advanced multilayer board construction.

D26J random access core memory can be expanded from 1024, twelve-bit words to 16,384, sixteen-bit words. Random access memory and parallel processing mean rapid computing speeds typified by a 12 usec add time and a 54 usec multiply time.

1. Operational Characteristics

D26J has the speed necessary to perform the computations required in a real time control system. Speeds shown in Table 3 include access times for both data and instructions; the speeds are for a 16-bit version of the D26J.

Table 3. Typical Operation Times

Add	16 bits	12 usec
Add	32 bits	18 usec
Multiply	16 bits	54 usec
	32 bits	270 usec
Divide	16 bits	108 usec

D26J has double precision add, subtract, and store capability. It can be programmed for double precision multiplication and division. Double precision makes more effective use of memory because instructions and many words can be stored in the 16 (or 12) bit word length. A 16 (or 12) bit word allows faster arithmetic operations than a longer word. But double precision allows more accuracy where it is needed.

2. Physical Characteristics

A D26J is composed of a general purpose section, an input/output section and a memory. The general purpose (GP) section contains an arithmetic unit and control unit. This GP section is the same for any D26J. The input/output section and memory are tailored to user needs.

The D26J can vary in size, weight and power depending on I/O, memory size and word length. Table 4 lists the general characteristics of the D26J family.

Table 4. Characteristics of the D26J

General	
Type	Stored-program, general purpose computer with single-address logic
Data Processing	Parallel
Clock Rate	500 kilopulses/sec
Memory	
Type	Random-access core
Capacity	1024, 4096, 8192, or 16,384 words with 6 usec cycle time
Arithmetic	
Number System	Binary with negative numbers represented in two's complement form
Word Length	
Instruction	The 16-bit computer word has 5 bits for the operation code and 9 bits for operand address. The remaining 2 bits are spares and can be used as I/O instructions. The 12-bit computer word has 5 bits for the operation code and 7 bits for operand address.

Table 4. (Cont)

Data	Single-precision, 12 bits including sign for the 12-bit machine. Sixteen bits including sign for the 16-bit machine.
Double-Precision	Twenty three bits including sign for the 12-bit machine; 31 bits including sign for the 16-bit machine. The second sign bit is not used in double-precision.

3. Environmental Characteristics

The D26J case is hermetically sealed to protect it from humidity, sand, dust, and salt spray.

The computer will operate without malfunction under the following environmental conditions in all axes:

45 g sustained acceleration

100 g shock 11 ms

100 g (rms) vibration 10-2000 cps

It will operate in ambient magnetic fields up to 10 gauss and will operate in an ambient pressure environment from deep space (approaching zero psia) to pressures up to 45 psia without permanent degradations.

4. Input/Output Characteristics

A computer must be flexible if it is to communicate with other subsystems. Some subsystems use incremental information; for example, from accelerometers, fuel flow meters, and raw data from Doppler navigation systems. Flight control and CRT displays are d-c voltage devices while angle and attitude sensors for inertial navigation platform gimbals, star trackers, and radar antennas operate on shaft position information. The D26J communicates in all these forms.

The D26J input/output section is tailored to meet system needs and can be expanded, if necessary, with only a minor redesign.

5. Packaging

The chassis is a sealed unit that protects the D26J from contamination and ensures that the inherent reliability is protected. The sealed package consists of a cast housing with pressure and RFI sealing gaskets for the top and bottom covers.

Inside the case, the modules are installed in heat transfer grooves and held in mechanical and thermal contact by wedge-type module locks. They are electrically mated to a master interconnect board through a high density, microminiature pin and socket connector. One master interconnect board replaces the conventional wire harness. This increases reliability and maintains the size and weight improvements of integrated circuits over standard circuits. All electrical connections between modules are made with the master interconnect board.

6. Integrated Circuit Construction

Integrated circuits and multilayer boards used in the D26J are the same types used in the Minuteman D37 computer. Integrated circuits are mounted on multilayer boards. These boards, or modules, plug into the master interconnect board. This construction improves reliability; reduces size, weight and power; and simplifies maintenance.

7. Cooling

Integrated circuits are cooled by bonding them to heat-conducting strips on the multilayer circuit boards. Heat generated by the integrated circuits is conducted through these strips to the computer case.

A coolant (liquid or gas) removes heat by flowing through heat dissipators on the computer case. This method of cooling permits simple, sealed case, no compatibility problems, small size and light weight.

8. Special Features

a. Predictable Program Times

Every instruction has a predictable program time instead of an execution time which is a function of the operand value. This is an important asset in a real time control computation which depends upon

a fixed iteration rate. Where instruction times can vary, the programmer must allow maximum execution time to all instructions. The D26J requires no such waste of program time.

b. Power Transient Protection

If supply voltages or environmental conditions exceed operating limits, the computer completes an existing memory cycle and turns off but retains all information in memory. Power resumption sends the program to a unique memory location. A subroutine in this location analyzes the state of the computation at the time of power loss and resumes computation at the correct point in the program.

c. External Interrupt

An external signal causes the following sequence:

1. Completion of present instruction
2. Execution of interrupt subroutine
3. Resumption of normal program at point where it was interrupted

9. D26J Organization

The 26J is organized into three major sections:

1. The input/output section (I/O) which provides the communication link between the computer and the outside world.
2. The general purpose section (GP) which performs the arithmetic and control function
3. The memory section which provides the program and temporary storage for the GP

a. Input/Output

All signals to and from the computational center pass through the input/output. Design of the I/O depends on what signals need processing and how many of these signals there are.

Some accelerometers and fuel flow devices have incremental outputs. Flight control systems and cathode ray tubes use dc communication. Inertial navigation platform gimbals, attitude sensors, star trackers and radar antennas have shaft position input and output. The D26J can communicate in any of these forms.

A partial list of other input/output signals encountered in aerospace systems includes; analog (ac and dc), shaft (angle encoding and shaft positioning), digital (ternary incremental and binary incremental), discrete, whole word serial, synchro and clock. The D26J handles all these signals.

The D26J's modular construction permits tailoring the I/O to specific system needs. This is done by adding modules as required. An input/output module is a circuit board with enough space on it for 182 integrated circuits. Enough integrated circuits are put on the board to process the input/output signals. If more capacity is needed, more boards are added.

Using integrated circuits and multilayer boards as building blocks, the I/O section is designed for the intended task. The computer's logical design permits a variety of configurations in the I/O section.

Two D26J configurations are shown in Table 5 to illustrate its adaptability to system needs. The table shows how size, weight and power depend on input/output, memory size and word length. The two configurations are for illustration only and do not represent the complete capability of the D26J family.

b. General Purpose Section

The general purpose (GP) section of the computer operates in a parallel mode under control of an internally stored program in conjunction with a coincident-current core memory.

(1) General Purpose Section Operation

(a) Word Format. The computer instruction word format consists of the function code (bits 12-16), the lower portion of the operand address (bits 1-9), and bits 10 and 11 which are used only in conjunction with input/output operations. The upper portion of the operand address is stored in an external register. Four of the basic function codes use bits 1 and/or 2 to bring the total number of instructions to 32.

Table 5. Typical D26J Configurations

1. D26J

(Minimal)

Memory	-	1024 words x 12-bit word		
Inputs	-	12 Discretes	Outputs -	12 Discretes
		3 Resolver		3 Incremental
		1 Incremental		1 Whole Word
		1 Whole Word		

Physical Characteristics (computer not including power supply)

Weight	-	13 lb
Volume	-	0.216 cu ft
Power	-	50.0 w

2. D26J

(Expanded)

Memory	-	16,384 words x 16-bit word		
Inputs	-	16 Discretes	Outputs -	16 Discretes
		4 Resolver		4 Incremental Ternary
		4 Incremental		4 Incremental Binary
		1 Whole Word		1 Whole Word
		32 Shaft Encoder		32 Shaft Positioning
		16 Voltage		15 Voltage

Physical Characteristics (computer not including power supply)

Weights	-	20 lb
Volume	-	0.33 cu ft
Power	-	90 w

(b) Operand Bank Register. Temporary storage for the upper portion of the operand address is provided by the "operand bank register" (5 flip-flops in the control section). The contents of the "operand bank register" can be stored in bank "0." This register can be loaded from any memory location. These actions are generated by the "store bank register" and "load bank register" instructions, respectively.

(c) Instruction Sequencing. The computer has a 14-bit program address register/counter which automatically provides sequencing of instructions as in other conventional single address machines. A "transfer of control" instruction is executed by specifying in the operand address a memory cell that contains a 14-bit branch address which is extracted from memory and placed in the program register. Exceptions to this are the "transfer in bank" and conditional jump instructions. Here, the action causes the least significant nine bits of the instruction (if the condition is met) to be placed in the least significant nine bits of the program address register. The upper 5-bits of the program address register will not be changed except when the least significant 9-bits are all one's. In this event, the most significant 5-bits are incremented by one count.

A single adder is used for all arithmetic operations. A common address register C is used for both instructions and operands. A common memory data buffer register N is used for intermediate storage in transferring both instruction words and operand words to and from memory. The U and L registers respectively comprise the upper and lower halves of the accumulator. The specific half of the accumulator (U or L) is logically selected for addition, interchanging U and L, logical product of U and L, or transferring L or U, to N as required by the instruction. An instruction execution proceeds as follows: After a control signal initiates a memory cycle, the "instruction fetch" mode is generated. The instruction word is read into N and simultaneously the program address register/counter is incremented to provide the address for the next instruction. The function code is transferred to the F register; the operand address is transferred to the C register if the instruction requires an operand from memory. Otherwise, the contents of the program address counter/register is transferred to C in preparation for the next instruction selection.

(d) Single-Precision Operation. Single-precision (16-bit) arithmetic operations are executed using the L register as the accumulator. The operand is read into the N register from memory. The L and N registers are switched into the adder during addition. For subtraction, the complement of the N register is used and a carry is inserted into the least significant stage. The sum or difference is gated into L. For the load operation L or U is cleared to zero and then the contents of N are added to zero resulting in the desired information transfer.

(e) Double-Precision Operation. For double-precision (sign plus 30* bit) addition or subtraction, the least significant half of the operand is first read into N from memory. The operation is similar to single precision, as described above, except that the sign position is made zero. Then the most significant half of the operand is obtained from memory by placing a one in the least-significant stage of the C register. It is assumed that the programmer has specified an even operand address, that is, the least significant half of the double-precision operand will be in an even location and the most significant in the next one higher. The addition or subtraction is again performed; this time accumulating the sum or difference in the U register. The carry, having been stored from the previous operation, is introduced into the least-significant stage. For double-precision load the above applies, except that both U and L are cleared to zero before being added.

(f) Multiply and Divide. In the multiply instruction, the 16-bit operand and the sign plus 30-bit product appears in U and L. The multiplier is decoded two bits at a time. For divide, the double-length dividend in U and L is divided by a 16-bit operand, the quotient being collected in L and the remainder in U.

(g) Transfer and Store Return. In the "transfer and store return" instruction, the address of the next instruction (stored in the program address register) is first stored at a fixed location in bank "0." The branch address is acquired by selecting the word from the address specified in the instruction.

(h) Shift. The right shift causes the sign to be extended and the left shift causes zeroes to be inserted into the least-significant stage.

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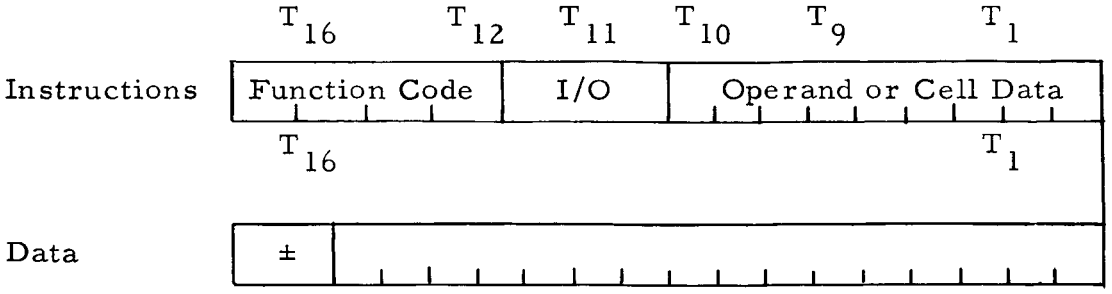
*The second sign bit is not used in double-precision operation.

(2) Command Descriptions. Following are the command descriptions.

(a) Cell and Address Structure. A word in memory consists of 16 (or 12) binary digits and is referred to as a cell. A cell may contain either an instruction, a prestored constant, or a computation result. All cells are addressable and may be modified by the program.

The address of a cell consists of the number of the bank which contains that cell, followed by the cell number, written b, c. The banks are numbered from 0 to 20 (octal) and the cells within each bank from 0 to 777 (octal).

Instructions and data are stored in the following formats:



Note that bits T_1 through T_9 of an instruction contain only the cell number of the operand. For all instructions that require a complete operand address, the contents of the bank register will denote the bank number of the operand.

The interpretation of bits T_1 through T_9 for various instructions is as follows:

1. ADD, SUB, MPY, DIV, DPAD, DPSU, LDU, LDL, STU, STL, DPST, DPLD, STB, SSS. T_1 through T_9 contain the cell number, c, of the operand. In the case of double-precision commands, c must be even.

2. SAL, SAR, SLR. T_1 through T_5 contain the number of bits the register is to be shifted.

3. TRA, TSR. T_1 through T_9 contain the cell number, c, from which the address of the next instruction will be taken.

4. TRB, TML, TZL, TMU. T_1 through T_9 contain the cell number, c, from which the next instruction will be taken if the transfer condition is met.

5. LDB. T_1 through T_5 contain the bank number to be stored in B.

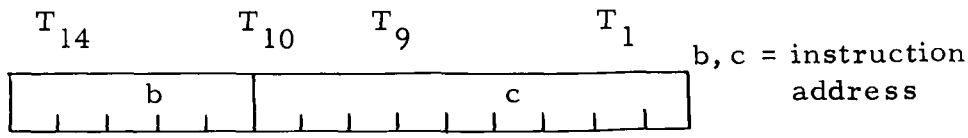
(b) Programming Registers. The following registers are referred to in the command operation descriptions. None of the registers may be addressed directly.

1. Accumulator Register - A (32 bits). The A register consist of two separate registers, the U and L, which are used for arithmetic and data transfer operations.

2. Bank Register - E (5 bits). The bank register contains the number of the memory bank, b, from which operands may be accessed. The contents of E can be changed only by a Load Bank command.

3. Function Register - F (5 bits). The function register holds the binary operation code of the current instruction. It may not be accessed by any instruction.

4. Instruction-Address Register - D (14 bits). The D register contains the address of the next instruction to be executed. Except in the case of transfer instructions, the contents of D are boosted by one during the fetch cycle of the current instruction address.



(c) Instructions. All instructions are listed in Table 6, and indicated by name, mnemonic code, execution time and operation code.

10. Coincident-Current Core Memory

The D26J has a coincident-current, random access core memory for program and data storage. High speed ferrite cores with a wide temperature range are used. These high speed cores eliminate the need for special, temperature compensating circuits, thus reducing the power requirements.

Table 6. D26J Command List

Octal Code	L.S. Rate 21	Mnemonic	Time Usec	Name
00	XX	SOL	6	Set output lines
02	XX	TML	6	Transfer on minus
04	XX	HPR	6	Halt and proceed
06	XX	TRB	6	Transfer in bank
10	XX	LDB	6	Load bank register
12	XX	TZL	6	Transfer in zero L
14	-	-	-	Not used
16	XX	TMU	6	Transfer on minus U
20	X0	WOL	12	Write output from L
20	X1	WOU	12	Write output from U
22	XX	STU	12	Store U
24	XX	SUB	12	Subtract
26	XX	LDU	12	Load U
30	X0	RIL	12	Read input to L
30	X1	RIU	12	Read input to U
32	XX	STL	12	Store L
34	XX	ADD	12	Add
36	XX	LDL	12	Load L
40	XX	SAR	6 + 2n	Shift A right n bits
42	XX	STB	12	Store bank register
44	XX	SLR	6 + 2n	Shift L right n bits
46	-	-	-	Not used
50	XX	SAL	6 + 2n	Shift A left n bits
52	XX	TSR	18	Indirect transfer and store return
54	-	-	-	Not used
56	XX	TRA	12	Indirect transfer
60	XX	MPY	54	Multiply
62	XX	SSS	18	Store and spread sign
64	XX	DPSU	18	Double-precision subtract
66	01	AND	12	Logical "AND"
66	10	XUL	18	Exchange U and L
70	XX	DIV	108	Divide
72	XX	DPST	18	Double-precision store
74	XX	DPAD	18	Double-precision add
76	XX	DPLD	18	Double-precision load

A word is selected from memory by using a diode-decoding matrix. Because both ends of the memory drive line are switched, the component count in the switching network has been reduced by a factor of approximately 5. The memory array output is routed to sense amplifiers that are used to drive an output register.

1. Address Timing. The address timing gates a new address into the address register.

2. Read Timing. The read timing synchronizes the closing of the switches that allow the read currents to pass through the array.

3. Strobe. The strobe is used by the sense amplifier to sample the contents of the memory during read time. It prevents noise from triggering the amplifier during write time.

4. Inhibit Timing. The inhibit timing times the inhibit driver pulses.

5. Write Timing. The write timing synchronizes the closing of the switches that control the write current.

Selection of a word consists of the following steps: The address register is set to provide for 1 out of 3 outputs. This requires two levels of logic because a low-gain NAND gate is used to drive two high-gate NAND gates. The output of the high-gain NAND gates drives a read or write current driver.

The output of the memory array is sensed by the sense amplifiers. The sense amplifiers drive an output register which consists of flip-flops. These flip-flops retain the information for the remainder of the time after read time, and are used to feed back the information through external gating into the inhibit driver. New information is gated from an external register for rewriting during the interval of time between the read and write pulses.

11. Cooling

Autonetics studied different methods of cooling the D26J. Studies were made of direct air cooling (coolant flow over components), direct liquid cooling (dielectric coolant flow over components), indirect cooling (liquid or gas), thermoelectric cooling, and vaporizing cooling.

Indirect cooling was selected. In this method the coolant (liquid or gas) does not flow over the components. It flows through heat dissipators located in the side of the computer. This method gives a simple sealed case, no compatibility problems, the smallest physical size and the lightest weight.

Heat generated by the components is transferred to heat sinks on the modules, to the case, into the dissipators, and then into the airstream. Indirect cooling offers the following advantages:

1. Contaminated air can be used for cooling (the air may contain dust, and moisture).

2. Housing can be easily sealed.

3. Gas in contact with components can be dry air, nitrogen, etc.

4. Computer package size and weight are reduced.

5. Electrical interfaces among the circuit boards, master interconnection board, and other subassembles are simplified.

The dissipators are dip-brazed aluminum structures with high fin density. This type of dissipator provides a large heat transfer area and a low pressure drop. The dissipators are attached to the computer and power supply housing with a high thermal-conducting cement. The thermal resistance across this junction is very low.

The detailed heat flow path for the computer is as follows: The heat generated in the junction of the component flows to the component case by conduction, across the cement that fastens the component to the board, and into the heat conduction rail on the circuit board. The heat then flows down the rail, across the junction between the board and case, and into the case. The module retainer provides firm contact between the module and the chassis to prevent a high temperature rise in this area. From the case, it passes into the dissipators and then into the airstream. Although there are many parallel paths for the heat to follow, all the other paths have such high thermal resistances that the rails carry most of the heat. The memory housing also acts as a heat path.

12. Power Supply and Power-Control System

The D26J has a variety of circuits (integrated and discrete) that require continuously regulated power for proper operation. The power supply regulates the input power and provides the proper voltage levels to the computer.

The power supply operates from a d-c source formed by rectifying 3-phase, 400-cps power conforming to MIL-STD-704, Category B. The supply maintains normal in-tolerance operation for the high-voltage transients as specified in MIL-STD-704. For low-voltage source transients below 21 v, the supply does not maintain regulation. Computer operation during these conditions is controlled by a special power control system that protects the stored program.

a. Description of Power Supply

The power supply block diagram is shown in Fig. 16, The d-c input voltage is chopped into a 20 kcps square wave so that the voltage can be preregulated with magnetic-amplifier preregulators and transformed to the correct positive and negative levels. Power ground is isolated from the computer signal ground. The chopping rate of 20 kcps was selected for optimum power dissipation in the switching transistors, magnetic-component sizes and filter requirements.

The square wave is passed through an isolation transformer to the magnetic-amplifier preregulators. The mag-amp preregulators regulate current to the loads by detecting the voltage across the loads and changing the current to maintain correct output voltage. Mag-amp regulation only is used on the four secondary levels sensed by the controllers.

The preregulated power is transformed to the proper voltage levels. These levels are then rectified by full-wave, center-tapped rectifier circuit, and filtered with CLC Pi section filters. For levels that are subject to transient loads and require faster frequency response, class "A" series voltage regulators are used. Overcurrent-protection circuits are used to protect the series regulators.

A separate dc-to-dc inverter is used to supply power for the power-control circuits since these circuits are required to maintain control before the main-power inverter is turned on and after it is turned off. A series regulator is used to preregulate the input voltage to the power-control inverter.

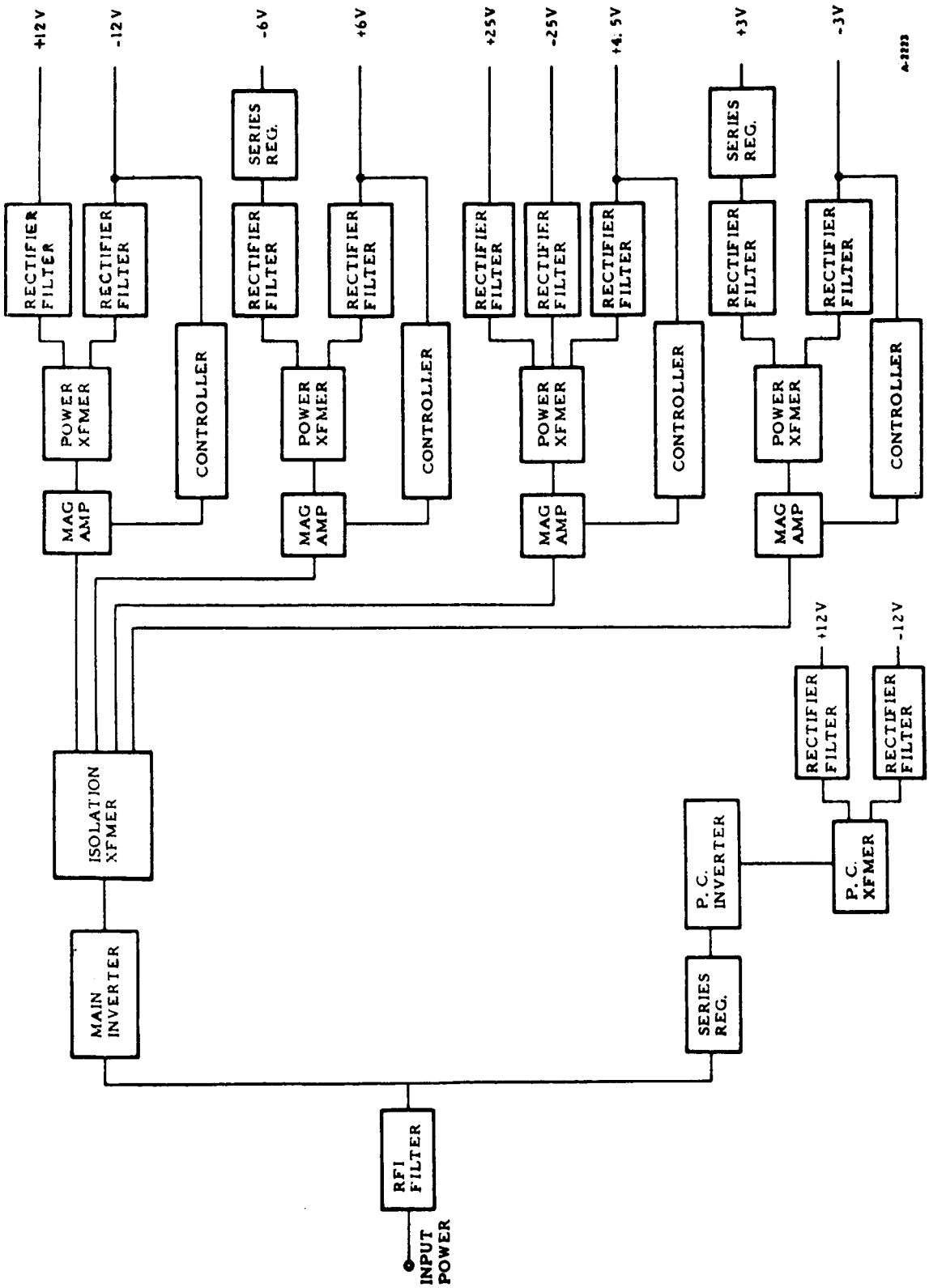


Fig. 16. D26J Power Supply

b. Power-Control System

The power-control system controls application and removal of power to the computer; permits optimum computer performance if the power to and/or from the power supplies is out of tolerance; and protects the computer and supplies from a high-temperature condition.

Power-control system functions are described by Table 7. Sequence of turn-on and off are to insure that stored-memory information is not destroyed.

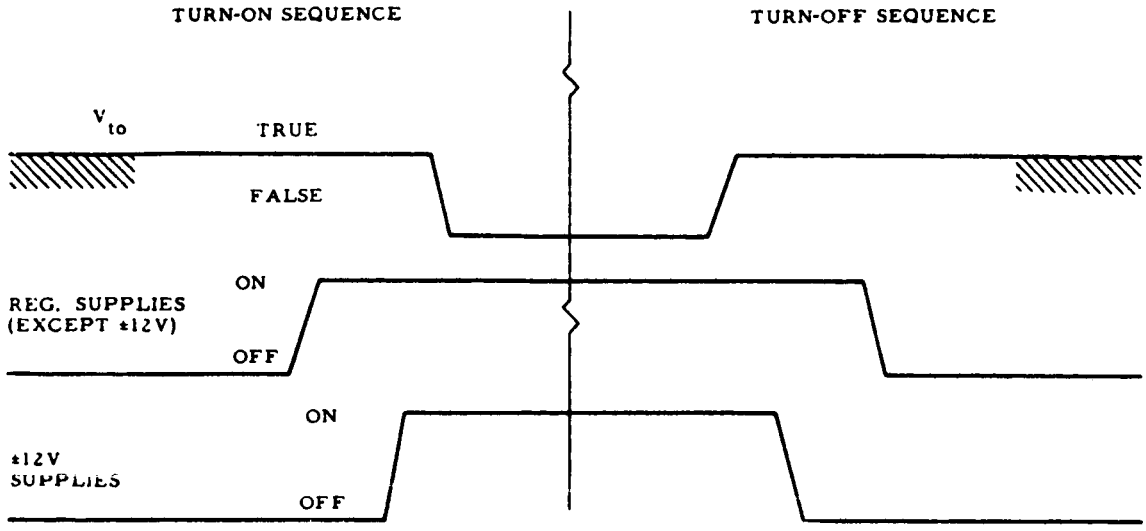
Table 7. Power Control Functions

Sensing Element Location	Condition	Generate V_{to}	Turn Off ±12 v	Turn Off Other Supplies
Primary Power Line	Low Primary Voltage	Yes	Yes	Yes
All Secondary Levels Except ±12 v	Low Secondary Voltage	Yes	Yes	No
Memory and Power Supply Case	High Temperature	Yes	Yes	Yes

Figure 17 illustrates the timing sequences of the occurrence of secondary power turn-on and off and the occurrence of V_{to}, the logic control signal to the computer.

A low primary-voltage condition is defined as 21.5 ± 0.5 vdc. Low secondary voltage is any of the regulated voltages (except the ±12 v) departing from -6 percent ±3 percent. The signal V_{to} is generated if the temperature, sensed by either of the high-temperature thermistors, exceeds +6 C ± 2.5 C. The turn-on sequence is initiated if the temperature drops from 2 to 3 C below the value at which V_{to} is generated.

Once a turn-off cycle is initiated by a V_{to} signal, the entire turn-off and turn-on sequence must be completed.



NOTE SHADED PORTION ON V_{to} INDICATES A "DON'T CARE" TIME, THE REQUIREMENTS BEING THAT V_{to} BE TRUE AT THE TIME THE SUPPLIES TURN ON, AND REMAIN TRUE UNTIL THE SUPPLIES ARE OFF.

Fig. 17. Timing Sequence

One high-temperature thermistor, with its associated bridge and preamplifier, is located inside the memory package. The outputs of this preamplifier are routed to the power supply and power-control package where all other circuits for the power-control system are located.

The signal, V_{to} to the computer, has a positive true state indicating an out-of-tolerance voltage or temperature condition. The signal is negative to indicate an in-tolerance condition.

The circuits can operate with a package-case temperature of 10 C higher and 5 C lower than the power-supply circuits. The circuits are operating and in control before the secondary levels are applied at power turn-on and after the levels are applied at power turn-off.

Figure 18 is the D26J power control block diagram.

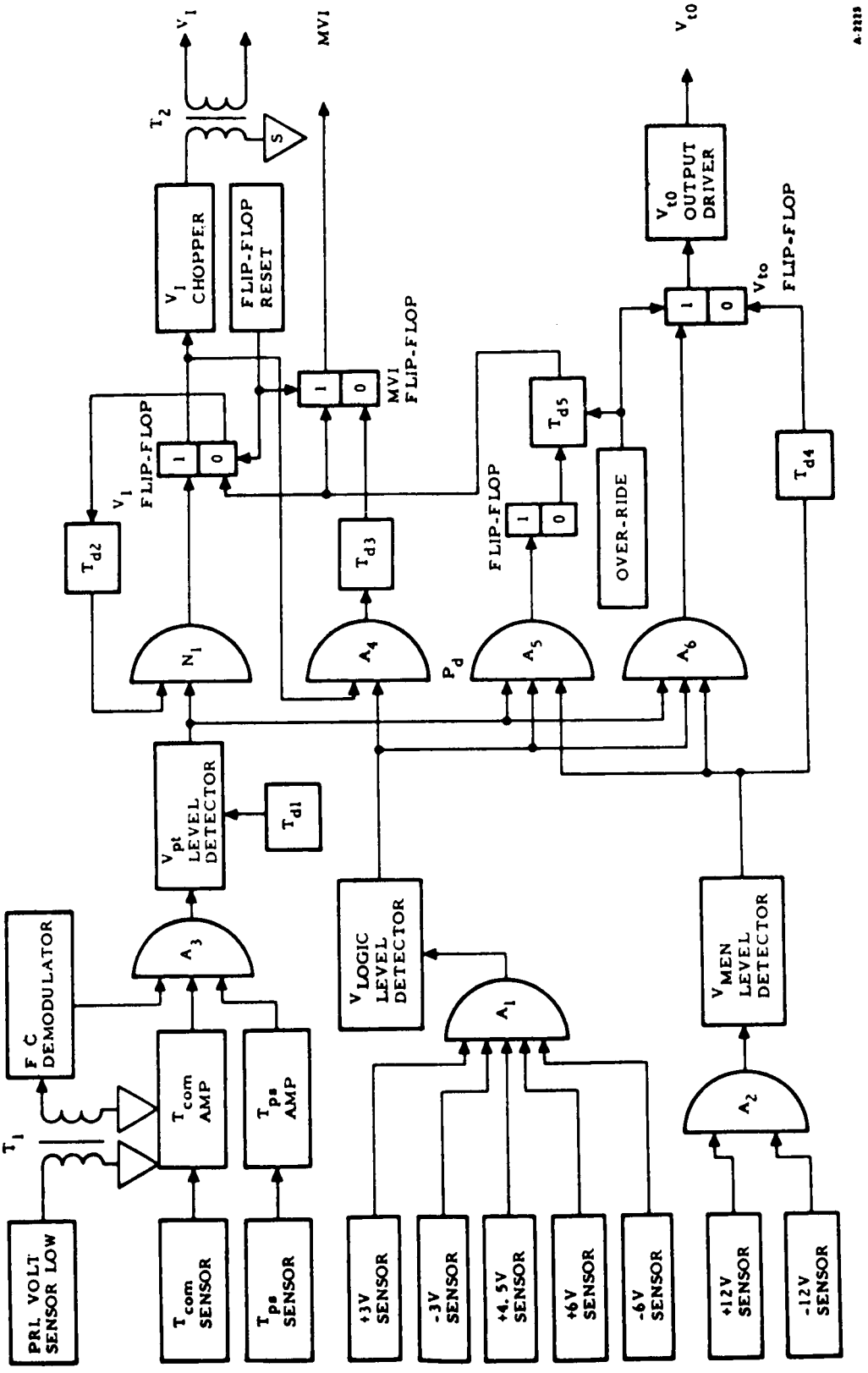


Fig. 18. Block Diagram D26J Power Control

13. Test Equipment

Test equipment for the D26J consists of three suitcase-mounted portable packages (photoelectric tape reader, control panel, and input/output tester). This equipment controls computer operation during tests of the computer in the system and is used to isolate malfunctions to the module level.

Operation of the computer test equipment is semi-automatic. Technicians must set up the equipment for an automatic, programmed sequence of tests. The tape reader and control panel allow new flight programs or diagnostic test tapes to be loaded into the computer memory. By using the input/output tester in conjunction with the control panel and tape reader, it is possible, via diagnostic test tapes, to isolate malfunctions to the computer (or peripheral device) while the computer is in the system.

a. Tape Reader

The tape reader can read 200 characters/sec of 8-channel, 1-in. punched tape under remote control. It can rewind at 600 characters/sec.

The tape reader has a built-in power supply and requires 3-phase, 110/208-v, 60 cps primary power. Eight data outputs are provided plus a timing signal derived from the sprocket hole. Only two inputs (start and stop) are required for control.

b. Control Panel

The control panel is used as a control, input/output, and indicating device for the D26J. Display switches and trouble indicators permit the operator to monitor or manually alter computer data or commands and thus aid in monitoring computer operation or in locating a malfunctioning module.

The panel is divided into the following groups of control and indicators: (1) power control, (2) manual operate, (3) trouble indicator, and (4) readout. The manual operate section contains the controls and indicators necessary to fill the computer manually from the thumb-wheel keyboard, to control filling from the tape reader and to control the starting location in a program. Numeric display units indicate the contents of manually-selected register or memory locations in the computer under program control. Checkout programs

are written to display certain numbers if the test sequences are properly carried out. If the computer does not function correctly, the manually-selected display aids in diagnosing the trouble.

The control panel is used in conjunction with the tape reader as a memory-fill device for loading flight programs into the computer.

c. Input/Output Tester

The input/output tester semi-automatically tests all data input and output lines of the computer. Inputs to the test panel are the data output lines of the computer. Test panel outputs drive the data input lines of the computer. The test panel has logic to generate a set of computer input signals in response to any legitimate combination of computer output signals. The tester also can switch computer analog voltage outputs back into computer analog voltage inputs. During an input/output test, the computer produces a particular output configuration under program control. This set of signals is fed into the tester which, in turn, generates a set of computer input signals. The resulting input configuration is compared with stored, predetermined values. If error exists, the results of the comparison aid in diagnosing the trouble.

VII. ALTERNATE AWARE SYSTEM

The basic AWARE system was devised using the Autonetics D26J general purpose digital computer because it is ideally suited to fulfill the NASA requirements for a microminiature general purpose computer and because of the inherent advantages of using a random access expandable memory and parallel word transfer. However, an alternate system was also considered using the Minuteman D37 microminiature computer. The D37 computer is a serial machine using a rotating disk memory. Unfortunately, memory expansion would not be easily accomplished if expansion becomes necessary but the D37 can be programmed to perform the AWARE functions if the straight limit comparisons are performed externally in a controller/comparator unit. This concept uses a portion of the PCM telemetry core memory to store straight limit values. Some of the multiplexer programming flexibility could be sacrificed or the core memory could be easily expanded to include limit storage capacity. The Alternate AWARE system schematic is shown in Fig. 19.

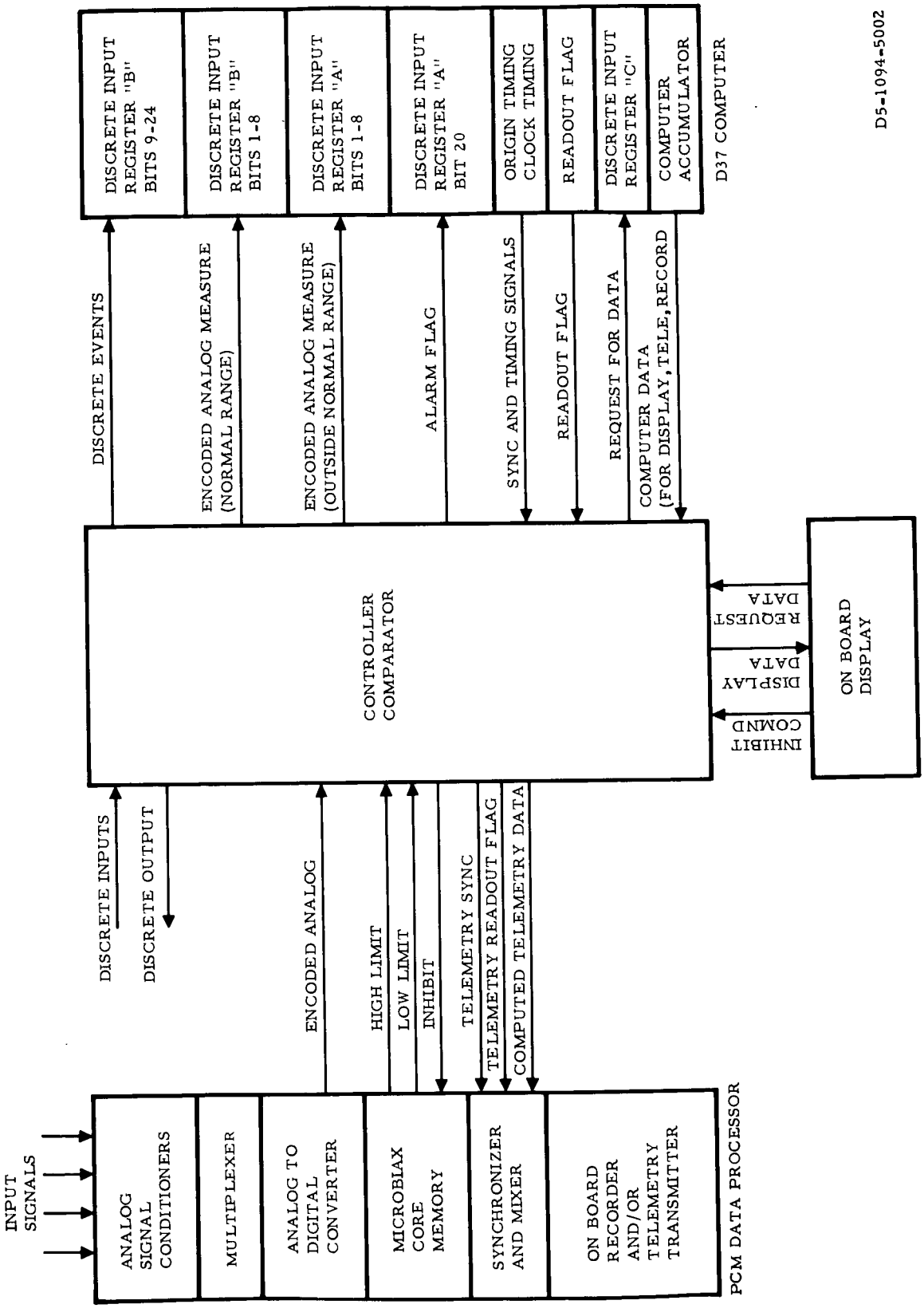


Fig. 19. Alternate AWARE System