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W. T. Homiller

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Submitted by: 

John S. Nisbet, Associate Professor of Electrical Engineering, Project Supervisor

Approved by: 

A. H. Waynick, Director, Ionosphere Research Laboratory

The Pennsylvania State University

College of Engineering

Department of Electrical Engineering

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ABSTRACT

An analysis of a d.c. feedback picoammeter is presented. The circuit uses an insulated gate field-effect transistor input as a solution to the limitations associated with the electrometer vacuum tubes which are presently used. The factors which affect frequency response, open loop voltage gain, and temperature dependence are determined, and methods are found for increasing response speed and for minimizing drift. Based on the above, a practical circuit is designed and evaluated experimentally.

Author

CHAPTER I

INTRODUCTION

1.1 Small Current Measurement

Devices for very small current measurement find wide application in rocket and satellite experiments employing transducers such as ion chambers, photomultiplier tubes, proportional counters, and ionization gauges. The output of these devices falls into the range of 10^{-7} to 10^{-14} amperes and requires considerable amplification to operate the input of a telemetry system. The two basic types of current or voltage amplifiers most suited are the D.C. electrometer amplifier, and the capacitor modulated A.C. amplifier. With respect to the latter, semiconductor and mechanical modulators do not possess the stability or low noise figure required. In addition, the vibrating reed capacitor modulator is frequently impractical because of its large size, its power requirements, and complexity of the circuits required. The D.C. electrometer amplifier, consequently, is usually the most attractive choice for rocket-born applications.

1.2 Origin and General Description of the Problem

The basic feedback electrometer, as first described by Peichowitch and Zaalberg VanZelst (1952) is well known and consists of a high negative gain D.C. amplifier with a shunt feedback resistance, R_f, connected between output and input terminals. If the amplifier input current is small compared to the current to be measured, and the voltage gain large compared

to unity, then the output voltage is given by

$$E_o \approx -I_{in}R_f$$

Until recently, electrometer vacuum tubes were the only devices suitable for use in the amplifier input circuit. Since they are directly heated, it is difficult to obtain the usual low drift advantages of a differential configuration, and they are also microphonic. An insulated gate transistor input stage appears to be the solution of these drawbacks. In addition, insulated gate transistors yield higher ultimate sensitivity and lower power requirements, and promise lower noise levels and temperature drift.

1.3 Specific Statement of the Problem

1.31 To analyze the voltage gain of a D.C. electrometer amplifier using an insulated gate field-effect transistor balanced input stage, followed also by balanced conventional transistor stages.

1.32 To analyze the temperature dependence of the circuit.

1.33 To analyze the response speed of the system, used with feedback.

1.34 To design a circuit to give good performance with respect to low drift, reasonable response speed, and adequately high open loop voltage gain, and stable closed loop operation.

1.35 To evaluate the overall performance by comparing measured and calculated values, and by comparing with the performance of presently used electrometers, in the case of quantities not easily calculated.

CHAPTER II

VOLTAGE GAIN ANALYSIS

Description of the Circuit

2.1 The general form of the feedback electrometer is shown in Figure 1. The differential input configuration is necessary for low drift operation. The balanced second stage allows a high impedance connection to the FET's to minimize the effects of second stage drift on the input stage while still allowing a fairly high gain. The third stage provides the additional gain necessary for accurate, stable operation. Its balanced form minimizes any additional drift which may be contributed by this stage, although in less critical applications an unbalanced stage may be satisfactory. The emitter-follower stage provides low output impedance and reduces the effects of reactive loads on stability and response time.

The open loop voltage gain is determined for the circuit as shown in Figure 2, without feedback and with a signal source inserted.

The simplified Giacoletto hybrid-pi circuit model as shown in Figure 3b is used as a circuit equivalent for the junction transistors. The parameters are directly related to the D.C. bias currents and are well suited to the following analysis. A similar simplified model, shown in Figure 3a, is used for the insulated gate field effect transistors, and is described in Appendix A.1.

2.2 Voltage Gain of the Field-Effect Differential Input Circuit

The following voltage gain quantities are defined for the FET input stage:

$$A_{va} = \frac{E_{da}}{E_{ia}} \tag{1}$$

$$A_{vb} = \frac{E_{db}}{E_{ib}} \tag{2}$$

$$A_{vab} = \frac{E_{da} - E_{db}}{E_{ia}} \tag{3}$$

From 3a, summing currents at the drain nodes

$$\frac{E_{da}}{R'_{DA}} + \frac{E_{da} - E_s}{r_{da}} + g_{ma}E_a = 0 \tag{4}$$

and

$$\frac{E_{db}}{R'_{DB}} + \frac{E_{db} - E_s}{r_{db}} + g_{mb}E_b = 0 \tag{5}$$

where

$$E_b = -E_s \tag{6}$$

$$E_a = E_{in} - E_s \tag{7}$$

solving for E_{da} and E_{db}

$$E_{da} = \left[\frac{E_s(1+r_{da}g_{ma}) - E_{in}r_{da}g_{ma})}{r_{da} + R'_{DA}}\right] R'_{DA} \tag{8}$$

$$E_{db} = \frac{E_s(1+r_{db}g_{mb})R'_{DB}}{r_{db} + R'_{DB}} \tag{9}$$

At the source node,

$$\frac{E_s}{R_s} + \frac{E_s - E_{db}}{r_{db}} + g_{mb}E_b + \frac{E_s - E_{da}}{r_{da}} + g_{ma}E_a = 0 \tag{10}$$

solving for E_s,

$$E_s = \frac{\dfrac{g_{ma}r_{da}E_{in}}{r_{da}+R'_{DA}}}{\dfrac{1}{R_s} + \dfrac{1+g_{ma}r_{da}}{r_{da}+R'_{DA}} + \dfrac{1+g_{mb}r_{db}}{r_{db}+R'_{DB}}} \tag{11}$$

and if $R_s > \dfrac{r_{da}+R'_{DA}}{1+g_{ma}r_{da}} + \dfrac{r_{db}+R'_{DB}}{1+g_{mb}r_{db}}$ (12)

then

$$E_s \approx \frac{g_{ma}r_{da}E_{in}}{1 + g_{ma}r_{da} + \dfrac{r_{da}+R'_{DA}}{r_{db}+R'_{DB}}(1 + g_{mb}r_{db})} \tag{13}$$

Substituting equation (13) into (8) and (1),

$$A_{va} \approx \frac{-g_{ma}r_{da}R'_{DA}}{r_{da} + R'_{DA} + \dfrac{1+r_{da}g_{ma}}{1+r_{db}g_{mb}}(r_{db} + R'_{DB})} \tag{14}$$

Substituting equation (13) into (9) and (2),

$$A_{vb} \approx \frac{g_{ma}r_{da}R'_{DB}}{r_{da} + R'_{DA} + \dfrac{1+r_{da}g_{ma}}{1+r_{db}g_{mb}}(r_{db} + R'_{DB})} \tag{15}$$

Substituting (14) and (15) into (3),

$$A_{vab} \approx \frac{-2g_{ma}r_{da}(R'_{DA} + R'_{DB})}{r_{da} + R'_{DA} + \dfrac{1+r_{da}g_{ma}}{1+r_{db}g_{mb}}(r_{db} + R'_{DB})} \tag{16}$$

2.3 Voltage Gain of the Second Differential Stage

For the differential second stage the following gain quantities are defined:

$$A_{v1} = \frac{E_{c1}}{E_{da} - E_{db}} \tag{17}$$

$$A_{v2} = \frac{E_{c2}}{E_{da} - E_{db}} \tag{18}$$

$$A_{v12} = \frac{E_{c1} - E_{c2}}{E_{da} - E_{db}} = A_{v1} - A_{v2} \tag{19}$$

From Figure 3b,

$$E_{c1} = -g_{m1} V_{b'e1} R'_{C1} = -g_{m1} I_{b1} r_{b'e1} R'_{C1} \tag{20}$$

$$E_{c2} = -g_{m2} V_{b'e2} R'_{C2} = -g_{m2} I_{b2} r_{b'e2} R'_{C2} \tag{21}$$

Summing voltage drops around the base-emitter loops,

$$E_{da} = I_{b2} R_{E1}(1 + g_{m2} r_{b'e2}) + I_{b1}\left[r_{bb'1} + r_{b'e1} + R_{E1}(1+g_{m1} v_{b'e1})\right] \tag{22}$$

$$E_{db} = I_{b2}\left[r_{bb'2} + r_{b'e2} + R_{E1}(1+g_{m2} r_{b'e2})\right] + I_{b1} R_{E1}(1+g_{m1} r_{b'e1}) \tag{23}$$

Solving for I_{b2},

$$I_{b2} = \frac{-E_{da} + E_{db}\left[1 + \dfrac{r_{bb'1} + r_{b'e1}}{(1+g_{m1} r_{b'e1}) R_{E_1}}\right]}{r_{b'2} + r_{b'e2} + (r_{bb'e1}) \dfrac{1 + g_{m2} r_{b'e2} + \dfrac{1}{R_{E1}}(r_{bb'2} + r_{b'e2})}{1 + g_{m1} r_{b'e1}}} \tag{24}$$

and, if $R_{E1} >> \dfrac{r_{bb'1} + r_{b'e}}{1 + g_{m1} r_{b'e1}}$ and $\dfrac{r_{bb'2} + r_{b'e2}}{1 + g_{m2} r_{b'e2}}$ (25)

$$I_{b2} \approx \frac{-E_{da} + E_{db}}{r_{bb'2} + r_{b'e2} + \frac{1 + g_{m2} r_{b'e2}}{1 + g_{m1} r_{b'e1}} (r_{bb'1} + r_{b'e1})} \tag{26}$$

similarly,

$$I_{b1} \approx \frac{E_{da} - E_{db}}{r_{bb'1} + r_{b'e1} + \frac{1 + g_{m1} r_{b'e1}}{1 + g_{m2} r_{b'e2}} (r_{bb'2} + r_{b'e2})} \tag{27}$$

Substituting equation (27) into (20) and (17),

$$A_{v1} \approx \frac{-g_{m1} r_{b'e1} R'_{C1}}{r_{bb'1} + r_{b'e1} + \frac{1 + g_{m1} r_{b'e1}}{1 + g_{m2} r_{b'e2}} (r_{bb'2} + r_{b'e2})} \tag{28}$$

Substituting equation (26) into (21) and (18),

$$A_{v2} \approx \frac{g_{m2} r_{b'e2} R'_{C2}}{r_{bb'2} + r_{b'e2} + \frac{1 + g_{m2} r_{b'e2}}{1 + g_{m1} r_{b'e1}} (r_{bb'1} + r_{b'e1})} \tag{29}$$

Finally, substituting (28) and (29) into (19),

$$A_{v12} \approx - \left[\frac{g_{m1} r_{b'e1} R'_{C1}}{r_{bb'1} + r_{b'e1} + \frac{1 + g_{m1} r_{b'e1}}{1 + g_{m2} v_{b'e2}} (r_{bb'2} + r_{b'e2})} + \frac{g_{m2} r_{b'e2} R'_{C2}}{r_{bb'2} + r_{b'e2} + \frac{1 + g_{m2} r_{b'e2}}{1 + g_{m1} r_{b'e1}} (r_{bb'1} + r_{b'e1})} \right] \tag{30}$$

2.4 Voltage Gain of the Differential Third Stage

For the differential third stage, the voltage gain is defined as

$$A_{v3} = \frac{E_{c3}}{E_{c1} - E_{c2}} \tag{31}$$

From Figure 4a,

$$E_{c3} = -g_{m3}V_{b'e3}R'_{C3}$$

$$= -g_{m3}I_{b3}r_{b'e3}R'_{C3} \qquad (32)$$

Summing voltage drops around the base-emitter loops, as in part 2.3,

$$E_{c1} = I_{b4}R_{E2}(1+g_{m4}r_{b'e4}) + I_{b3}\left[r_{bb'3}+r_{b'e3}+R_{E2}(1+g_{m3}r_{b'e3})\right] \qquad (33)$$

$$E_{c2} = I_{b4}\left[r_{bb'4}+r_{b'e4}+R_{E2}(1+g_{m4}r_{b'e4})\right] + I_{b3}R_{E2}(1+g_{m3}r_{b'e3}) \qquad (34)$$

Solving for I_{b3},

$$I_{b3} = \frac{-E_{c2} + E_{c1}\left[1 + \frac{r_{bb'4} + r_{b'e4}}{(1 + g_{m4}r_{b'e4})R_{E2}}\right]}{r_{bb'3}+r_{b'e3}+(r_{bb'4}+r_{b'e4})\frac{1+g_{m3}r_{b'e3}+\frac{1}{R_{E2}}(r_{bb'3}+r_{b'e3})}{1 + g_{m4}r_{b'e4}}} \qquad (35)$$

As before,

$$\text{If } R_{E2} >> \frac{r_{bb'4} + r_{b'e4}}{1 + g_{m4}r_{b'e4}} \quad \text{and} \quad \frac{r_{bb'3} + r_{b'e3}}{1 + g_{m3}r_{b'e3}} \qquad (36)$$

$$I_{b3} \approx \frac{E_{c1} - E_{c2}}{r_{bb'3} + r_{b'e3} + \frac{1 + g_{m3}r_{b'e3}}{1 + g_{m4}r_{b'e4}}(r_{bb'4}+r_{b'e4})} \qquad (37)$$

Substituting (37) into (32) and (31)

$$A_{v3} \approx \frac{-g_{m3}r_{b'e3}R'_{C3}}{r_{bb'3} + r_{b'e3} + \frac{1 + g_{m3}r_{b'e3}}{1 + g_{m4}r_{b'e4}}(r_{bb'4}+r_{b'e4})} \qquad (38)$$

2.5 Voltage Gain of the Common-Collector Output Stage

The voltage gain of the common-collector stage may be defined as

$$A_{v4} = \frac{E_o}{E_{c3}} \qquad (39)$$

From Figure 4b,

$$E_o = R_L(I_{b5}+g_{m5}V_{b'e5}) = R_L I_{b5}(1+g_{m5}r_{b'e5}) \tag{40}$$

$$E_{c3} = I_{b5}(r_{bb'5}+r_{b'e5}) + E_o$$

$$= I_{b5}\left[r_{bb'5}+r_{b'e5}+R_L(1+g_{m5}r_{b'e5})\right] \tag{41}$$

Substituting (41) and (40) into (39),

$$A_{v4} = \frac{R_L(1+g_{m5}r_{b'e5})}{r_{bb'5} + r_{b'e5} + R_L(1+g_{m5}r_{b'e5})} \tag{42}$$

2.6 Open-Loop Voltage Gain

The total voltage gain is defined in Figure 2 as

$$A_v = \frac{E_o}{E_{ia}} \tag{43}$$

From equations (3), (19), (31), and (39),

$$A_v = A_{vAB}A_{v12}A_{v3}A_{v4} \tag{44}$$

$$A_v \approx \left[\frac{-2g_{ma}r_{da}(R'_{DA} + R'_{DB})}{r_{da} + R'_{DA} + \frac{1 + r_{da}g_{ma}}{1 + r_{db}g_{MB}}(r_{da}+R'_{DB})}\right]$$

$$\left[\frac{-g_{m1}r_{b'e1}R'_{C1}}{r_{bb'1} + r_{b'e1} + \frac{1 + g_{m2}r_{b'e2}}{1 + g_{m1}r_{b'e1}}(r_{bb'1}+r_{b'e1})}\right.$$

$$\left.\frac{-g_{m2}r_{b'e2}R_{C'2}}{r_{bb'2} + r_{b'e1} + \frac{1 + g_{m2}r_{b'e2}}{1 + g_{m1}r_{b'e1}}(r_{bb'1}+r_{b'e1})}\right]$$

$$\left[\frac{-g_{m3}r_{b'e3}R'_{C3}}{r_{bb'3}+r_{b'e3}+\frac{1+g_{m3}r_{b'e3}}{1+g_{m4}r_{b'e4}}(r_{bb'4}+r_{b'e4})}\right]\left[\frac{R_L(1+g_{m5}r_{b'e5})}{r_{bb'5}+r_{b'e5}+R_L(1+g_{m5}r_{b'e5})}\right] \tag{45}$$

Since, for all of the junction transistors:

$$r_{b'e}=\frac{kT}{qI_B},\ g_m=\frac{\beta}{r_{b'e}},\ 1+g_m r_{b'e}=1+\beta \tag{46}$$

For the field effect transistors:

$$g_m=\sqrt{2\beta_{ab}I_{ab}} \tag{47}$$

$$\text{Where } \beta_{AB}=\frac{\epsilon_{ox}\mu_o W}{L\,T_{ox}}=\frac{C_{ox}\mu_o}{L^2} \text{ as defined} \tag{48}$$

by Hofstein and Heiman (1963).

$$\frac{1}{R'_{DA}}=\frac{1}{R_{DA}}+\frac{1}{r_{b1}+\frac{kT}{qI_{B1}}} \tag{49}$$

$$\frac{1}{R'_{DB}}=\frac{1}{R_{DB}}+\frac{1}{r_{b2}+\frac{kT}{qI_{B2}}} \tag{50}$$

$$\frac{1}{R'_{C1}}=\frac{1}{R_{C1}}+\frac{1}{r_{b3}+\frac{kT}{qI_{B3}}} \tag{51}$$

$$\frac{1}{R'_{C2}}=\frac{1}{R_{C2}}+\frac{1}{r_{b4}+\frac{kT}{qI_{B4}}} \tag{52}$$

$$\frac{1}{R'_{C3}}=\frac{1}{R_{C3}}+\frac{1}{r_{b5}+\frac{kT}{qI_{B5}}+R_L(1+\beta_5)} \tag{53}$$

The individual stage gains may now be written

$$A_{vab} \approx \frac{-2\mu_a}{r_{da} + \frac{R_{DA}(\frac{kT}{qI_{B1}} + r_{bb'1})}{R_{DA} + \frac{kT}{qI_{B1}} + r_{bb'1}} + \frac{1+\mu_a}{1+\mu_b}\left[r_{db} + \frac{R_{DB}(\frac{kT}{qI_{B2}} + r_{bb'2})}{R_{DB} + \frac{kT}{qI_{B2}} + r_{bb'2}}\right]} \times \left[\frac{R_{DA}(\frac{kT}{qI_{B1}} + r_{bb'1})}{R_{DA} + \frac{kT}{qI_{B1}} + r_{bb'1}} + \frac{R_{DB}(\frac{kT}{qI_{B2}} + r_{bb'2})}{R_{DB} + \frac{kT}{qI_{B2}} + r_{bb'2}}\right] \tag{54}$$

$$A_{v12} \approx \frac{\frac{-\beta_1 R_{C1}(\frac{kT}{qI_{B3}} + r_{bb'3})}{R_{C1} + \frac{kT}{qI_{B3}} + r_{bb'3}}}{r_{bb'1} + \frac{kT}{qI_{B1}} + \frac{1+\beta_2}{1+\beta_1}(r_{bb'2} + \frac{kT}{qI_{B2}})}$$

$$\frac{\frac{-\beta_2 R_{C2}(\frac{kT}{qI_{B4}} + r_{bb'4})}{R_{C2} + \frac{kT}{qI_{B4}} + r_{bb'4}}}{r_{bb'2} + \frac{kT}{qI_{B2}} + \frac{1+\beta_2}{1+\beta_1}(r_{bb'1} + \frac{kT}{qI_{B1}})} \tag{55}$$

$$A_{v34} \approx \frac{-\beta_3 R_{C3}(r_{b5} + \frac{kT}{qI_{B5}} + R_L(\beta_5+1)}{r_{bb'3} + \frac{kT}{qI_{B3}} + \frac{1+\beta_3}{1+\beta_4}(r_{bb'4} + \frac{kT}{qI_{B4}})\ R_{C3} + r_{bb'5} + \frac{kT}{qI_{B5}} + R_L(\beta_5+1)} \tag{56}$$

$$A_{v5} \approx \frac{R_L(1+\beta_5)}{r_{bb'5} + \frac{kT}{qI_{B5}} + R_L(1+\beta_5)} \tag{57}$$

Several valid assumptions may be made to simplify the gain expressions:

$$\frac{kT}{qI_{B1}} >> r_{bb'1} \qquad \frac{kT}{qI_{B2}} >> r_{bb'2} \tag{58}$$

$$R_L(\beta_5+1) >> r_{bb'5} + \frac{kT}{qI_{B5}} \tag{59}$$

$$R_{C3} << R_L(1+\beta_5) \tag{60}$$

Of particular interest is the case of equal drain and emitter currents in the balanced pairs, since this condition minimizes drift in the differential configuration. This is particularly important in the input and second stages, and for this reason balanced currents will be assumed. In addition, it will be assumed that the transistor pairs are selected for similar Beta's, and that symmetrical resistor values are used.

With the above approximations, the gain expressions reduce to:

$$A_{vab} \approx \left[\frac{-2\mu_a}{r_{da} + r_{db} + \frac{2R_{DA}\frac{kT}{qI_{B1}}}{R_{DA} + \frac{kT}{qI_{B1}}}}\right] \left[\frac{2R_{DA}\frac{kT}{qI_{B1}}}{R_{DA} + \frac{kT}{qI_{B1}}}\right] \tag{61}$$

$$A_{v12} \approx \frac{\frac{-2\beta_1 R_{C1}(\frac{kT}{qI_{B3}} + r_{bb'3})}{R_{C1} + \frac{kT}{qI_{B3}} + r_{bb'3}}}{2\frac{kT}{qI_{B1}}} \tag{62}$$

$$A_{v34} \approx \frac{-\beta_3 R_{C3}}{r_{bb'3} + r_{bb'4} + 2\frac{kT}{qI_{B3}}} \tag{63}$$

$$A_{v5} \approx 1$$

Provided, $I_{DA} \approx I_{DB}$ $\beta_A \approx \beta_B$

$$I_{E1} \approx I_{E2} \qquad \beta_1 \approx \beta_2$$

$$I_{E3} \approx I_{E4} \qquad \beta_3 \approx \beta_4$$

and

$$R_{DA} = R_{DB}, \quad R_{C1} = R_{C2}, \quad R_{C3} = R_{C4} \tag{64}$$

From Figure 2,

$$I_{C1} \approx I_{B3} + \frac{(I_{C3}+I_{C4})R_{E2} + V_{BE3}}{R_{C1}} \tag{65}$$

$$I_{D1} \approx I_{B1} + \frac{(I_{C1}+I_{C2})R_{E1} + V_{BE1}}{R_{D1}} \tag{66}$$

$$I_{C3} \approx V_1/R_3 \tag{67}$$

Substituting equations (65), (66), (67) into equations (61), (62), and (63),

$$A_{vaB} \approx \frac{-2\left\{2\beta_A\left[\frac{V_{BE1}}{R_{DA}} + \left(\frac{V_1}{R_3}\left(\frac{1}{\beta_3} + \frac{2R_{E2}}{RC_1}\right) + \frac{V_{BE3}}{R_{C1}}\right)\left(\frac{1}{\beta_1} + \frac{2R_{E1}}{R_{DA}}\right)\right]\right\}^{1/2}}{\frac{1}{r_{da}} + \frac{1}{R_{DA}} + \frac{q}{\beta_1 kT}\left(\frac{V_1}{R_3}\left[\frac{1}{\beta_3} + \frac{2R_{E2}}{R_{C1}}\right] + \frac{V_{BE2}}{R_{C1}}\right)} \tag{68}$$

$$A_{v12} \approx -\left[\frac{\frac{V_1}{R_{C3}}\frac{R_{C1}}{\beta_3} + 2R_{E2} + V_{BE3}}{\frac{R_{C1}V_1}{R_{C3}\beta_3} + \frac{kT}{q}}\right] \tag{69}$$

$$A_{v34} \approx \frac{-qV_1}{2kT} \tag{70}$$

neglecting $r_{bb'3}$ and $r_{bb'4}$.

The complete gain expression as a function of D.C. quantities only is

$$A_v \approx \frac{-2\left\{2\beta_A\left[\frac{\bar{V}_{BE1}}{R_{DA}} + \left[\frac{\bar{V}_1}{R_3}\left(\frac{1}{\beta_2} + \frac{2R_{E2}}{R_{C1}}\right) + \frac{V_{BE3}}{R_{C1}}\right]\left(\frac{1}{\beta_1} + \frac{2R_{E1}}{R_{DA}}\right)\right]\right\}^{1/2}}{\left[\frac{1}{r_{da}} + \frac{2}{R_{DA}} + \frac{2q}{\beta_1 kT}\left(\frac{V_1}{R_3}\left[\frac{1}{\beta_3} + \frac{2R_{E2}}{R_{C1}}\right] + \frac{V_{BE3}}{R_{C1}}\right)\right]}$$

$$\frac{\left[\frac{\bar{V}_1}{R_3}\left(\frac{R_{C1}}{\beta_3} + 2R_{E2}\right) + V_{BE3}\right]}{\left[\frac{R_{C1}V_1}{R_{C3}\beta_3} + \frac{kT}{q}\right]\frac{2kT}{qV_1}} \qquad (71)$$

2.7 Output Impedance

From Figure 1, if $R_{in} >> R_F$, and if

R'_o = output impedance without feedback, then

$$I_o \approx \frac{E_o + A_v E_o}{R'_o} \qquad (72)$$

and

$$\frac{E_o}{I_o} = R_o \approx \frac{R'_o}{1+A_v} \qquad (73)$$

For the common-collector stage without external feedback, the output impedance is given by

$$R'_o = \frac{R_{C3}}{(1+\beta_5)} \qquad (74)$$

Consequently, for any $R_F << R_{in}$, the output impedance is decreased by the magnitude of the total gain A_v:

$$R_o \approx \frac{R_{C3}}{(1+\beta_5)A_v} \qquad (75)$$

2.8 Input Impedance

From Figure 1,

$$I_{in} = \frac{V_{in} - V_o}{R_f} + \frac{V_{in}}{R_G} \tag{76}$$

$$V_o = -A_v(V_{in})$$

$$I_{in} = V_{in} \frac{A_v + 1}{R_f} + \frac{1}{R_G} \tag{77}$$

and if $R_G >> R_f$

$$\frac{V_{in}}{I_{in}} = R_{in} = \frac{R_f}{A_v + 1} \tag{78}$$

That is, the effective value of the measuring resistor is reduced by the voltage gain.

CHAPTER III

DRIFT RATE ANALYSIS

The output voltage level of the feedback electrometer is a function of the temperature and the bias conditions of the transistors. It is generally useful to express this dependance, known as drift, as the equivalent correction voltage at the input required to restore the output voltage level to zero. The drift rate referred to the input is the rate of change of the input drift voltage with respect to temperature.

It is well known that in multistage feedback amplifier circuits, the total noise and drift are contributed primarily by the first stage and, to a lesser degree, the second stage.

In the following analysis the effect of the contributions from the first three stages will be accounted for, while the fourth or common collector stage is neglected.

3.1 Drift-Rate Derivation

Figure 6 illustrates the amplifier with the hypothetical input voltage generator, V_{in} whose magnitude is that input voltage which exactly cancels the total output drift due to variations in transistor parameters. Therefore, $E_o = 0$ and is constant.

Adding voltage drops around the gate-source legs of T_A and T_B in Figure 2,

$$V_{IN} = V_{GS_A} - V_{GS_B} - V_{GB} \tag{79}$$

Since the effective gate-source voltage,

$$V_{EFF_{GS}} = V_{GS} - V_T \tag{80}$$

$$V_{IN} = V_{TA} - V_{TB} + V_{GSA_{EFF}} - V_{GSB_{EFF}} \tag{81}$$

$$I_D = \frac{\beta}{2} V_{EFF}^2 \tag{82}$$

$$V_{IN} = V_{TA} - V_{TB} + \left(\frac{2I_{DA}}{\beta_A}\right)^{1/2} - \left(\frac{2I_{DB}}{\beta_B}\right)^{1/2} \tag{83}$$

$$\frac{\partial V_{IN}}{\partial T} = \frac{\partial V_{TA}}{\partial T} - \frac{\partial V_{TB}}{\partial T} + \left(\frac{2I_{DA}}{\beta_A}\right)^{1/2} \left(\frac{1}{\beta_A} \frac{\partial I_{DA}}{\partial T} - \frac{I_{DA}}{\beta_A^2} \frac{\partial B_A}{\partial T}\right)$$

$$- \left(\frac{2I_{DB}}{\beta_B}\right)^{1/2} \left(\frac{1\partial}{\beta_B} \frac{I_{DB}}{\partial T} - \frac{I_{DB}}{\beta_B} \frac{\partial \beta_B}{\partial T}\right) \tag{84}$$

$$I_{DA} = I_{B1} + \frac{(I_{E1}+I_{E2})\, R_{E1} + V_{BE1}}{R_{DA}} \tag{85}$$

$$\frac{\partial I_{DA}}{\partial T} = \frac{I_{C1}}{\beta_1^2} \frac{\partial \beta_1}{\partial T} + \frac{1}{\beta_1} \frac{\partial I_{C1}}{\partial T} + \frac{1}{R_{DA}} \left[\frac{\partial V_{BE1}}{\partial T} + \frac{\partial V_{BE1}}{\partial I_{B1}}\right.$$

$$\left.\left(\frac{1}{\beta_1} \frac{\partial I_{C1}}{\partial T} - \frac{I_{C1}}{\beta_1^2} \frac{\partial \beta_1}{\partial T}\right)\right] + \frac{R_{E1}}{R_{DA}} \left(\frac{\partial I_{E1}}{\partial T} + \frac{\partial I_{E2}}{\partial T}\right) \tag{86}$$

Similarly

$$\frac{\partial I_{DB}}{\partial T} = -\frac{I_{C2}}{\beta_2^2} \frac{\partial \beta_2}{\partial T} + \frac{1}{\beta_2} \frac{\partial I_{C3}}{\partial T} + \frac{1}{R_{DB}} \left[\frac{\partial V_{BE2}}{\partial T} + \right.$$

$$\left. + \frac{\partial V_{BE2}}{\partial I_{B2}} \left(\frac{1}{\beta_2} \frac{\partial I_{C2}}{\partial T} - \frac{I_{C2}}{\beta_2^2} \frac{\partial \beta_2}{\partial T}\right)\right] + \frac{R_{E1}}{R_{DB}} \left(\frac{\partial I_{E1}}{\partial T} + \frac{\partial I_{E2}}{\partial T}\right) \tag{87}$$

$$I_{E1} = \frac{\beta_1 + 1}{\beta_1} I_{C1} \tag{88}$$

$$I_{E2} = \frac{\beta_2 + 1}{\beta_1} I_{C2} \tag{89}$$

$$\frac{\partial I_{E1}}{\partial T} = \left[\frac{\partial I_{C1}}{\partial T} - \frac{I_{C1}}{\beta_1(\beta_1+1)} \frac{\partial \beta_1}{\partial T}\right] \frac{\beta_1 + 1}{\beta_1} \tag{90}$$

$$\frac{\partial I_{E2}}{\partial T} = \left[\frac{\partial I_{C2}}{\partial T} - \frac{I_{C2}}{\beta_2(\beta_2+1)} \frac{2\beta_2}{\partial T}\right] \frac{\beta_2 + 1}{\beta_2} \tag{91}$$

$$I_{C1} = I_{B1} + \frac{(I_{E3} + I_{E4})R_{E2} + V_{BE3}}{R_{C1}} \tag{92}$$

$$\frac{\partial I_{C1}}{\partial T} = \frac{1}{\beta_3}\left[\frac{\partial I_{C3}}{\partial T} - \frac{I_{C3}}{\beta_3} \frac{\partial \beta_3}{\partial T}\right] + \frac{1}{R_{C1}}\left[\frac{\partial V_{BE3}}{\partial T} + \frac{I_{C3}}{\beta_3^2} \frac{\partial \beta_3}{\partial T} + R_{E2}\left(\frac{\partial I_{C3}}{\partial T} + \frac{\partial I_{C4}}{\partial T}\right)\right] \tag{93}$$

Similarly,

$$\frac{\partial I_{C2}}{\partial T} = \frac{1}{\beta_4}\left[\frac{\partial I_{C4}}{\partial T} - \frac{I_{C4}}{\beta_4} \frac{\partial \beta_4}{\partial T}\right] + \frac{1}{R_{C2}}\left[\frac{\partial V_{BE4}}{\partial T} + \frac{I_{C4}}{\beta_4^2} \frac{\partial \beta_4}{\partial T} + R_{E2}\left(\frac{\partial I_{C3}}{\partial T} + \frac{\partial I_{C4}}{\partial T}\right)\right] \tag{94}$$

Since the drift effects of the output stage are negligible, and E_o is constant, then V_{C3} is also constant and

$$\frac{\partial I_{C3}}{\partial T} = 0 \tag{95}$$

While this is not true of I_{C4} and V_{C4}, a more reasonable assumption concerning I_{C3} is that

$$I_{E34} = I_{E3} + I_{E4} \approx \text{Constant} \tag{96}$$

$$I_{E34} = I_{B3}(\beta_3+1) + I_{B4}(\beta_4+1) \tag{97}$$

assuming low leakage silicon transistors for which I_{co} is negligible.

$$0 = \frac{\partial I_{B3}}{\partial T}(\beta_3+1) + \frac{I_{C3}}{\beta_3}\frac{\partial \beta_3}{\partial T} + \frac{\partial I_{B4}}{\partial T}(\beta_4+1) + \frac{I_{C4}}{\beta_4}\frac{\partial \beta_4}{\partial T} \qquad (98)$$

Solving for $\frac{\partial I_{C4}}{\partial T}$,

$$\frac{\partial I_{C4}}{\partial T} = \frac{-\beta_4}{\beta_4+1}\left[(\beta_3+1)\frac{\partial I_{B3}}{\partial T} + \frac{I_{C3}}{\beta_3}\frac{\partial \beta_3}{\partial T}\right] + \frac{I_{C4}}{\beta_4}\frac{\partial \beta_4}{\partial T}\left[1 - \frac{\beta_4}{\beta_4+1}\right] \qquad (99)$$

Substituting equations (86), (87), (90), (91), (93), (94), (95), and (99) into equation (84), and rewriting (84) as

$$\frac{\partial V_{in}}{\partial T} = \frac{\partial V_{TA}}{\partial T} - \frac{\partial V_{TB}}{\partial T} + \frac{1}{g_{ma}}\left(\frac{\partial I_{DA}}{\partial T} - \frac{I_{DA}}{\beta_A}\frac{\partial \beta_A}{\partial T}\right) - \frac{1}{g_{mb}}\left(\frac{\partial I_{DB}}{\partial T} - \frac{I_{DB}}{\beta_B}\frac{\partial \beta_B}{\partial T}\right)$$

and solving for the drift,

$$\frac{\partial V_{in}}{\partial T} \approx \frac{\partial V_{TA}}{\partial T} - \frac{\partial V_{TB}}{\partial T} + \frac{1}{g_{ma}}\left\{\left[\frac{1}{\beta_1 R_{C1}}\left(\frac{\partial V_{BE3}}{\partial T} - \frac{kT}{q\,\beta_3}\frac{\partial \beta_3}{\partial T}\right)\right.\right.$$

$$\left(1 + \frac{R_{E1}}{R_{DA}}(\beta_1+1)\right) - \frac{I_{C3}}{\beta_1\beta_3^{\,2}}\frac{\partial \beta_3}{\partial T}\left(1 - \frac{1}{\beta_4+1} + \frac{R_{E1}}{R_{DA}}(\beta_1+1)\right)\frac{I_{C1}}{\beta_1^{\,2}}\frac{\partial \beta_1}{\partial T}$$

$$\left(1 + \frac{R_{E1}}{R_{DA}}\right) + \frac{1}{R_{DA}}\left[\frac{\partial V_{BE1}}{\partial T} + \frac{kT}{qI_{B1}}\left[\frac{I_{C3}}{\beta_1\beta_3}\frac{\partial \beta_3}{\partial T} + \frac{1}{R_{C1}}\left(\frac{\partial V_{BE3}}{\partial T} - \frac{kT}{q\beta_3}\frac{\partial \beta_3}{\partial T}\right)\right.\right.$$

$$\left.\left. - \frac{I_{C1}}{\beta_1^{\,2}}\frac{\partial \beta_1}{\partial T}\right]\right] + \frac{R_{E1}}{R_{DA}}\frac{(\beta_2+1)}{\beta_2 R_{C2}}\left[\frac{\partial V_{BE4}}{\partial T} - \frac{kT}{q\beta_4}\frac{\partial \beta_4}{\partial T}\right] - \frac{R_{E1}}{R_{DA}}\frac{I_{C4}}{\beta_4(\beta_4+1)}$$

$$\left.\left.\frac{\partial \beta_4}{\beta_2\partial T} - \frac{R_{E1}}{R_{DA}}\frac{I_{C2}}{\beta_2^{\,2}}\frac{\partial \beta_2}{\partial T}\right] - \frac{I_{DA}}{\beta_A}\frac{\partial \beta_A}{\partial T}\right\} - \frac{1}{g_{mb}}\left\{\left[\frac{1}{\beta_2 R_{C2}}\left(\frac{\partial V_{BE4}}{\partial T} - \frac{kT}{q\beta_4}\frac{\partial \beta_4}{\partial T}\right)\right.\right.$$

$$\left(1+\frac{R_{E1}}{R_{DA}}(\beta_2+1)\right)-\frac{I_{C4}}{\beta_2\beta_4(\beta_4+1)}\frac{\partial\beta_4}{\partial T}\left(1+\frac{R_{E1}}{R_{DB}}(\beta_2+1)\right)-\frac{I_{C2}}{\beta_2^{\,2}}\frac{\partial\beta_2}{\partial T}$$

$$\left(1+\frac{R_{E1}}{R_{DB}}\right)+\frac{R_{E1}(\beta_1+1)}{R_{C1}\beta_1 R_{DB}}\left[\frac{\partial V_{BE3}}{\partial T}-\frac{kT}{q\beta_3}\frac{\partial\beta_3}{\partial T}\right]+\frac{I_{C3}}{\beta_3^{\,2}}\frac{\partial\beta_3}{\partial T}\frac{1}{\beta_2(\beta_4+1)}$$

$$\left[1-\frac{R_{E1}}{R_{DB}}\frac{(\beta_1+1)(\beta_4+1)\beta_2}{\beta_1}-(\beta_2+1)\right]-\frac{R_{E1}}{R_{DB}}\frac{I_{C1}}{\beta_1^{\,2}}\frac{\partial\beta_1}{\partial T}+\frac{1}{R_{DB}}$$

$$\left[\frac{\partial V_{BE2}}{\partial T}+\frac{kT}{qI_{B2}}\left[\frac{I_{C4}}{\beta_2\beta_4}\frac{\partial\beta_4}{\partial T}+\frac{1}{R_{C2}}\left(\frac{\partial V_{BE4}}{\partial T}-\frac{kT}{q\beta_4}\frac{\partial\beta_4}{\partial T}\right)-\frac{I_{C2}}{\beta_1^{\,2}}\frac{\partial\beta_1}{\partial T}\right]\right]$$

$$-\frac{I_{DB}}{\beta_B}\frac{\partial\beta_B}{\partial T}\Bigg\} \qquad \text{where } g_m=\sqrt{2\beta I_D} \tag{100}$$

Equation (100) is the complete drift-rate expression. Although not always valid, the following assumptions help to clarify the nature of the significant drift terms:

$$\beta_1 \approx \beta_2 >> 1$$

$$\beta_3 \approx \beta_4 >> 1$$

$$R_{DA}=R_{DB} \qquad R_{C1}=R_{C2} \qquad R_{C3}=R_{C4}$$

If balanced currents in the differential pairs are also assumed as in Chapter 2,

$$\frac{\partial V_{IN}}{\partial T}\approx\frac{\partial V_{TA}}{\partial T}-\frac{\partial V_{TB}}{\partial T}+I_{DA}\left(\frac{1}{g_{mb}\beta_B}\frac{\partial\beta_B}{\partial T}-\frac{1}{g_{ma}\beta_A}\frac{\partial\beta_A}{\partial T}\right)$$

$$+\frac{\partial\beta_3}{\partial T}\frac{1}{\beta_1\beta_3}\left[\frac{I_{C3}}{\beta_3}\left[\beta_1\frac{R_{E1}}{R_{DA}}\left(\frac{1}{g_{mb}}-\frac{1}{g_{ma}}\right)-\frac{1}{g_{ma}}\right]+\frac{kT}{qR_{C1}}\right.$$

$$\left.\left[\frac{\beta_1 R_{E1}}{R_{DB}g_{mb}}+\frac{R_{C1}I_{C3}}{R_{DA}I_{B1}g_{ma}}\right]\right]+\frac{\partial\beta_4}{\partial T}\frac{1}{\beta_2\beta_4}\left[\frac{I_{C4}}{\beta_4}\left[\beta_1\frac{R_{E1}}{R_{DA}}\left(\frac{-1}{g_{mb}}+\frac{1}{g_{ma}}\right)\right.\right.$$

$$\left.\left.+\frac{1}{g_{ma}}\right]+\frac{kT}{qR_{C2}}\left[\frac{\beta_2 R_{E1}}{R_{DA}g_{ma}}+\frac{R_{C2}I_{C4}}{R_{DB}I_{B2}g_{mb}}\right]\right]+\frac{1}{R_{DA}}\left[\frac{1}{g_{ma}}\right.$$

$$\left.\frac{\partial V_{BE1}}{\partial T}\left(\frac{1}{g_{mb}}\frac{\partial V_{BE2}}{\partial T}\right)\right]+\frac{\partial\beta_1}{\partial T}\frac{I_{C1}}{\beta_1^{\,2}}\left[-\frac{1}{g_{ma}}+\frac{R_{E1}}{R_{DA}}\left(\frac{1}{g_{mb}}-\frac{1}{g_{ma}}\right)\right]$$

$$\frac{\partial\beta_2}{\partial T}\frac{I_{C1}}{\beta_1^{\,2}}\left[\frac{1}{g_{mb}}+\frac{R_{E1}}{R_{DA}}\left(\frac{1}{g_{mb}}-\frac{1}{g_{ma}}\right)\right]$$

$$+\frac{\partial V_{BE4}}{\partial T}\frac{1}{R_{C2}}\left[-\frac{1}{g_{mb}\beta_2}+\frac{R_{E1}}{R_{DA}}\left(\frac{1}{g_{ma}}-\frac{1}{g_{mb}}\right)-\frac{kT}{qI_{B2}R_{DB}g_{mb}}\right]$$

$$+\frac{\partial V_{BE3}}{\partial T}\frac{1}{R_{C1}}\left[+\frac{1}{g_{mb}\beta_1}+\frac{R_{E1}}{R_{DA}}\left(\frac{1}{g_{ma}}-\frac{1}{g_{mb}}\right)+\frac{kT}{qI_{B1}R_{DA}g_{ma}}\right] \tag{101}$$

3.2 Methods of Minimizing Drift-Rate

Equation (101) is the total drift-rate referred to the input. The importance of matching the input transistors, T_A and T_B, with respect to V_T temperature coefficients, β temperature coefficients, and magnitude of β or g_m is apparent. The recurring $(\frac{1}{g_{ma}} - \frac{1}{g_{mb}})$ term shows that drift contributed by differences in β and V_{BE} temperature coefficients is minimized

when $g_{ma} = g_{mb}$. Terms not containing $\frac{1}{g_{ma}} - \frac{1}{g_{mb}}$ are functions of β'^{s} and quiescent current level, illustrating the effect of balanced currents in minimizing drift.

In a particular case, $T_1 + T_2$ and $T_3 + T_4$ need not be selected as carefully as $T_A + T_B$ since contributions due to these stages are reduced by the gain of the preceding stage(s).

CHAPTER IV

ANALYSIS OF RESPONSE SPEED

4.1 Uncompensated Response

The basic circuit for response time analysis is shown in Figure 5a. Although it will be assumed that the amplifier gain $-A_v$, is real over the bandwidth of interest, it is useful to examine the relative importance of the dominant poles in the amplifier response. Referring to Figure 2, the "corner frequencies" associated with the drain circuits of T_A and T_B and with the collector circuits of $T_1 - T_2$ and $T_3 - T_4$ are given by

$$\omega p_{AB} = \frac{\frac{2R_{DA}r_{da}}{R_{DA}+r_{da}} + \frac{2kT}{qI_{B1}}}{C_{b'1}\frac{kT}{qI_{B1}}\frac{R_{DA}r_{da}}{R_{DA}+r_{da}}}$$

$$\omega p12 = \frac{2R_{C1} + \frac{2kT}{qI_{B3}}}{C_{b'3}\frac{kT}{qI_{B3}}R_{C1}} \tag{102}$$

$$\omega p34 = \frac{R_{C3} + R_L(1+\beta_5)}{C_{b'5}\frac{kT}{qI_{B5}}(R_{C3}+R_L)}$$

where

$$C_{b'1} = C_{b'e1} + C_{b'c1}\left(1 + \beta_1 \frac{qI_{B1}}{kT} R_{C1}\right)$$

$$C_{b'3} = C_{b'e3} + C_{b'c3}\left(1 + \beta_3 \frac{qI_{B3}}{kT} R_{C3}\right)$$

$$C_{b'5} \quad C_{b'e5} \tag{103}$$

$$C_{b'e} = C_{TE} + C_d = C_{TE} + \frac{W^2 qI_E}{2DkT}$$

Using (103), the corner frequencies are given by

$$\omega_{pAB} = \frac{\frac{2R_{DA}r_{da}}{R_{DA}+r_{da}} + \frac{2kT}{qI_{B1}}}{\left[C_{TE'} + \frac{W_1^2}{2D_1}\frac{qI_{E3}}{kT} + C_{b'c1}\left(1+\beta_1\frac{qI_{B1}}{kT}R_{C1}\right)\right]\frac{kT}{qI_{B1}}\frac{R_{DA}r_{da}}{R_{DA}r_{da}}}$$

$$\omega_{p12} = \frac{2R_{C1} + \frac{2kT}{qI_{B3}}}{\left[C_{TE3} + \frac{W_3^2}{2D_3}\frac{qI_{E3}}{kT} + C_{b'C3}\left(1+\beta_3\frac{qI_{B3}}{kT}R_{C3}\right)\right]\frac{kT}{qI_{B3}}R_{C1}}$$

$$\omega_{p34} = \frac{R_{C3} + R_L(1+\beta_5)}{\left(C_{TE5} + \frac{W_5^2}{2D_5}\frac{qI_{E5}}{kT}\right)(R_{C3}+R_L)\left(\frac{kT}{qI_{B5}}\right)} \tag{104}$$

Since the total phase shift becomes large as frequency increases, it is clear that there is a possibility of instability for very high loop gain. The corner frequencies will be evaluated in Chapter 6 to check the system stability and the validity of the negative real gain assumption. While this assumption may be valid with field-effect transistors as input devices, it is not necessarily justified for circuits employing electrometer vacuum tubes, which require very large plate resistors with the resulting relatively low corner frequency. For the purpose of later

analysis, a network, whose transfer function is B, is included in the feedback loop. The equivalent circuit, then, is as shown in Figure 5b. Solving for the input current,

$$I_{in} = E_{in}pC_{in} + (e_{in}-BE_o)\left(\frac{1-pC_fR_f}{R_f}\right) \tag{105}$$

where p = differential operator.

Rearranging,

$$I_{in} = -E_o\left[\frac{pC_{in}}{A_v} + \frac{1 + pC_FR_F}{A_vR_F} + \frac{B(1+pC_FR_F)}{R_F}\right] \tag{106}$$

If the circuit is excited by a current square wave equal to $i_{in}u(t)$, the solution of equation (101) is

$$E_o = \frac{-I_{in}R_FA_v}{1 + BA_v}\left[1 - e^{\frac{-t}{R_F\left(\frac{e_{in}}{1 + BA_v} + C_F\right)}}\right] \tag{107}$$

The time constant of this response is

$$T = R_F\left[\frac{C_{in}}{1 + BA_v} + C_F\right] \tag{108}$$

It can be seen that the time constant formed by the input capacitance and the feedback resistance, R_FC_{in}, is reduced by the loop gain or feedback factor, BA_v. In general, the effect of any capacitance across the input is reduced by the loop gain. On the other hand, R_FC_F, the time constant formed by the feedback resistor and its associated parallel capacitance is not affected, and thus determines the minimum time constant possible with a given R_F.

4.2 Compensated Response

With C_F equal to at least 1 pf. and R_F equal to 10^{12} ohms, a minimum response time of at least one second results. This minimum time would be prohibitively slow in many rocket applications, so that in high-speed work, the $R_F C_F$ time constant limitation must be overcome. To this end, let the network represented by the box "B" in Figure 5a be of the form shown in Figure 5c. The transfer function of this network is

$$B = \frac{1}{1 + pR_B C_B} \tag{109}$$

If this transfer function is now substituted for B in equation (106), and $C_F R_F$ adjusted so that $C_B R_B = C_F R_F$, then the third term on the right hand side of (101) is simply $\frac{1}{R_F}$.

$$C_{in} = - E_o \left[\frac{pC_{in}}{A_v} + \frac{1 + pC_F R_F}{A_v R_F} + \frac{1}{R_F} \right] \tag{110}$$

If the response to a current step $I_{in}\, u(t)$ is now obtained, the result is,

$$e_o = \frac{-i_{in} R_F A_v}{1 + A_v} \left[1 - e^{\frac{-t}{R_1 (C_F + C_{in})(A_v + 1)}} \right] \tag{111}$$

whose time constant is

$$T_{comp} = \frac{R_F (C_{in} + C_F)}{A_v + 1} \tag{112}$$

In other words, if the above lead and lag networks are equal, the principal time constants associated with the circuit are decreased by the loop gain.

In practice, a 10^{11} or 10^{12} ohm resistor has a stray capacitance distributed all along its resistance element and can resemble a delay line in performance. As such, it is impossible to perfectly compensate the circuit. Although this consideration, plus that of signal to noise ratio limits the attainable response speed, a significant improvement may be obtained through the method discussed above.

CHAPTER V

CIRCUIT DESIGN

5.1 Design Considerations

The D.C. operating point of the FET input pair is chosen at $I_D = 250\mu$ ampere since this is the "zero drift" bias point, as defined in Appendix A, for the GME 2N3608 MOS FET. This type is chosen for its comparative low cost, high transconductance, and input terminal current $< 10^{-14}$ ampere.

It is desirable that I_{B1}, the quiescent current in the second stage pair, be very small to allow high first stage gain. Conversely, decreasing the value of I_{B1} results in lowered second stage gain with the result that third stage temperature effects may become important. Terms in the drift rate expression (101) of the form $\frac{kT}{qI_B}$ are also increased with decreasing I_B. A value of 10^{-6} amperes is chosen as a reasonable compromise between the drift and first and second stage gain considerations. Although the amplifier bandwidth is also a function of this bias point, other considerations limit upper frequency response more severely than the transistors themselves, and this consideration may be disregarded.

5.2 Circuit Value Design

The serviceability of the 2N 1711 (NPN) and 2N 1132 (PNP) silicon transistors is well known, and these types are used. The transistors maintain reasonable β values at 10^{-6} ampere base currents and have values of I_{CO} less than 10^{-9} amperes at 25^{o}C.

The 2N3608 has an average β value of 5×10^{-4} amp./volt^2 or g_m = 500 micromhos at I_D = 250 microamperes. The average threshold voltage value, V_T, is about -5 volts.

The design conditions are:

$$I_{B1,2} = 10^{-6} \text{ ampere}$$

$$I_{DA,B} = 250 \times 10^{-6} \text{ ampere} \qquad (113)$$

$$V_2 = 12 \text{ volts}, \quad V_1 = -9 \text{ volts}$$

Typical values of β for the junction transistors are, 2N1711: $\beta \approx 100$; 2N1132: $\beta \approx 50$; at $I_B = 10^{-6}$ amperes.

From Figure 2,

$$I_{DA} = \frac{V_2 - (V_{SGA})}{2R_S}$$

$$I_{DA} = \frac{V_2 - (V_{TA} + \frac{2I_{DA}}{\beta_A})}{2R_S} \qquad (114)$$

or

$$R_s = \frac{12 - (5+1)}{5 \times 10^{-4}} = 12 \text{ k ohms, choose 12k.}$$

similarly,

$$I_{B1} = \frac{V_{B1} - V_1 - V_{BE1}}{2\beta_1 R_{E1}} \qquad (115)$$

To assure FET operation in the "saturation" region, V_{DG} should not be less than zero. Letting $V_{DGA} = 0$ or $V_{DA} = V_{B1} = 0$ (since $V_{GA} \approx 0$) allows the largest possible value of R_{DA} for a given V_2, and also allows the maximum first stage gain. With $V_{B1} = 0$ in (115)

$$R_{E1} = 42 \text{ k ohms, choose 47 k.}$$

Also

$$V_{DA} \approx V_1 - I_{DA} R_{DA} = 0 \tag{116}$$

$$R_{DA} \approx \frac{V_1}{I_{DA}} = 36 \text{ k ohms, choose 33 k.}$$

The quiescent value of V_{C1} will be approximately equal to the maximum positive value of the output voltage, E_o. The maximum negative value of E_o will approach V_1, so for symmetrical output voltage range, let $V_{C1} = 7.5$ volts.

$$V_{C1} \approx V_2 - \beta_1 I_{B1} R_{C1} \tag{117}$$

if $I_{C1} >> I_{B3}$,

then

$$R_{C1} = \frac{12 - 7.5}{100 \times 10^{-6}} = 45 \text{ k ohms, choose 47 k.}$$

If the second stage gain is very small, drift contributed by the third stage may not be negligible. On the other hand, very high gain is unnecessary and may make the circuit more difficult to stabilize with respect to high frequency oscillations. Compromising, let $A_{V12} = 20$. From equation (69),

$$A_{V12} = 20 \approx \frac{I_{C3}\left(\frac{R_{C1}}{B_3} + 2R_{E2}\right)}{\frac{I_{C3} R_{C1}}{\beta_3}} \tag{118}$$

or

$$A_{V12} = 20 \approx \frac{1 + 2\beta_3 R_{E2}}{R_{C1}}$$

and

$$R_{E2} \approx 8.9 \text{ k ohms, choose } 8.2 \text{ k.}$$

As in (115)

$$I_{CE} = \frac{V_2 - V_{B3} - V_{BE3}}{2R_{E2}} \tag{119}$$

$$= 235 \times 10^{-6} \text{ amperes.}$$

In order that $E_O = 0$ when $E_{IN} = 0$, it is necessary that the quiescent value of V_{C3} be equal to V_{BE5}.

$$V_{C3} = V_{BE5} \simeq 0.6 \approx V_1 + I_{C3}R_{C3}, \tag{120}$$

and

$$R_{C3} = \frac{9 + 0.6}{235 \times 10^{-6}} = 40.9 \text{ k ohm, choose } 39 \text{ k.}$$

Ordinarily, R_L would be chosen with consideration for the magnitude of the d.c. current drained from the output terminal by the external load. Aside from this consideration, R_L need only be chosen such that

$$R_L > \frac{R_{C3}}{1 + \beta_5} = \frac{39 \times 10^3}{100 + 1} \approx 390 \text{ ohms} \tag{121}$$

A value of $R_L = 10$ k gives

$$I_{E5} \approx \frac{V_1 - V_{BE5}}{R_L} = \frac{8.4}{10^4} = 0.84 \times 10^{-3} \text{ ampere} \tag{122}$$

which results in a total supply current of about 2×10^{-3} amperes, or a total power requirement less than 40 milliwatts.

Since negligible current flows into the gate terminal of T_B from the "zero adjust" divider R_1, R_2 and R_3, R_1 and R_3 may

be made large enough to dissipate negligible power but must still provide adequate voltage range for V_{GB} adjustment. If R_4 is small compared to R_2,

$$V_{GB\ max} \approx V_2 \frac{R_4}{R_1}$$

$$V_{GB\ min} \approx V_1 \frac{R_4}{R_3} \qquad (123)$$

Values of R_1 = 120 k, R_2 = 50 k, R_3 = 150 k, and R_4 = 15 k satisfy the above requirements and give V_{GB} range of about + 1.5 to -1.5 volts, which will accommodate a large range of threshold voltage and transconductance mismatch.

With C_F, the effective capacitance in parallel with R_F, equal to approximately 1 picofarad, $R_F C_F \approx 1$ sec. for $R_F = 10^{12}$ ohms. It is convenient to make the time constant of the compensating network, $C_B R_B$, variable, as $R_F C_F$ is difficult to predict exactly. Making R_B variable and equal to 10 megohms, and C_B = 0.2mfd., allows $C_B R_B$ to take on any value up to 2 seconds.

In order to improve the stability margin, a capacitance, C_1, is added across the first stage drains to restrict the open-loop frequency response. A small resistance is added to prevent the phase shift from becoming equal to 90^o, and stability is maintained for a wide range of input capacitance values.

A value of 10 mfd. for C_1 provides a corner frequency in the open loop response at about 2 cps.

The complete circuit, with component values, is shown in Figure 8. The collector resistor R_{C4} is omitted, as its value does not materially affect gain or temperature dependence.

CHAPTER VI

EVALUATION OF PERFORMANCE

6.1 Voltage Gain

The open loop voltage gain may be determined from equations (68), (69), and (70). For the transistors used, the measured small signal parameters at $I_{B12} = 10^{-6}$ amperes, $I_{B3} = 5 \times 10^{-6}$ amperes, and $I_{DA} = 250 \times 10^{-6}$ amperes are $\beta_1 = 115$, $\beta_2 = 121$, $\beta_3 = 63$, $\beta_4 = 51$, $\beta_A = \beta_B = 5 \times 10^{-4}$, $r_{da} = r_{db} = 10^5$ ohms. Assuming V_{BE1} and $V_{BE3} = 0.6$ volts,

From (68)

$$A_{VAB} \approx \frac{-2\left\{2x5x10^{-4}\left[\frac{0.6}{3.3x10^4}+\left(\frac{9}{3.9x10^4}\left[\frac{1}{51}+\frac{2x8.2}{47}\right]+\frac{0.6}{4.7x10^4}\right)\right.\right.}{\frac{1}{10^5}+\frac{1}{3.3x10^4}+\frac{40}{115}\left(\frac{9}{3.9x10^4}\left[\frac{1}{51}+\frac{2x8.2}{47}\right]\right.}$$

$$\left.\left.\left.\left(\frac{1}{115}+\frac{2x47}{33}\right)\right]\right\}^{1/2}}{\left.+\frac{0.6}{4.7x10^4}\right)} = -13.75 \qquad (124)$$

From (69)

$$A_{V12} \approx -\left[\frac{\frac{9}{3.9x10^4}\left(\frac{4.7x10^4}{51}+2x8.2x10^3\right)+0.6}{\frac{47 \times 19}{39 \times 51}+0.25}\right] = -19.12 \qquad (125)$$

and from (70)

$$A_{V34} = \frac{-40 \times 9}{2} = -180 \qquad (126)$$

$$A_{V\ total} = -13.75 \times 19.12 \times 180 = -47,341.$$

Calculated and measured values of gain are tabulated in

Table 1. The errors in the gain values may be attributed to the resistor tolerances (10 percent) and the fact that the currents in the differential stages are not perfectly balanced, as assumed.

6.2 Temperature Dependence

It is clear from equation (101) that the total drift rate is essentially a function of transistor matching, but it is valuable to determine more quantitively the degree to which the total drift depends upon matching of the input transistors, T_A and T_B. To this end, a simplified expression may be developed by making the following assumptions:

a. Third stage drift effects are negligible.

b. Second stage transistors are reasonably well matched.

For the sake of calculation, assume that the ratios of V_{BE1} to V_{BE2} and β_1 to β_2, and the ratios of their respective drift rates are equal to 0.8, and that the larger of each pair is chosen for the worst possible case.

Typical drift rates are $\frac{\partial V_{BE}}{\partial T} = -2.5 \times 10^{-3}$ v/°C, $\frac{\partial \beta}{\partial T} = .01\ \beta$/°C for silicon junction transistors, and $\frac{\partial V_T}{\partial T} = -1.5 \times 10^{-3}$ volts/°C, $\frac{\partial \beta}{\partial T} = -.0033\ \beta$/°C for the silicon mos field effect transistors. Applying the above assumptions to equation (101)

$$\frac{\partial V_{in}}{\partial T} \quad -1.5 \times 10^{-3}\,(1-n) + 1.5 \times 10^{-3}\,(1-m) + 9 \times 10^{-6} \qquad (127)$$

where $$n = \frac{\partial V_{TA}/\partial T}{\partial V_{TB}/\partial T} \quad \text{and} \quad m = \frac{\partial \beta_A/\partial T}{\partial \beta_B/\partial T}$$

if the input transistors are chosen for equal drift.

The reason for biasing the fet's at the so called "zero drift" operating point is now clear: Even if the transistors are not matched, the V_T and β drift terms will tend to cancel if the degrees of mismatch in $\frac{\partial V_T}{\partial T}$ and $\frac{\partial \beta}{\partial T}$ are nearly equal. On the other hand, if m = 1, the V_T values must differ by less than 5 per cent for a total drift less than 100 $\mu V/^{o}C$.

The total drift was measured for four pairs of input transistors, with the first pair selected for the best match in V_T and g_m, the last pair for greatest mismatch, and the remaining two at random. These results indicate that with careful selection of the input transistors, drift rates on the order of 20-30 $\mu V/^{o}C$ may be obtained. In the most critical applications, the first and second stage pairs may be replaced with matched integrated transistor pairs for better temperature tracking. The measured results are listed in Table 1 and compared with typical values for presently used electrometers. In Figure 6 input error voltage is plotted as a function of temperature for the four F.E.T. pairs described above.

6.3 Initial Drift

The M.O.S. input transistors, (as well as electrometer vacuum tubes) have initial drift when supply voltage is applied after long (hours) interruption. Typical initial drift curves are shown in Figure 7, where it can be seen that initial effects are negligible after about 3 hours.

6.4 Long Term Stability

The long term stability, based on 48 hour measurement

periods initiated after initial drift effects had become small, average about ± 1 percent of full scale per week.

6.5 Response Speed

To measure the amplifier rise time for a current step input, the "injection capacitor" method described by Praglin and Nichols(1960) was used. In this method, a triangular voltage waveform is applied through a small capacitance, C_2, to the amplifier input. Solving for the amplifier response as in Chapter 4, but including the injecting capacitor C_2,

$$e_o = \frac{-aR_F C_2 A_v}{1 + A_v} \left[1 - \exp\left(\frac{-t}{R_1 \frac{C_2 + C_{in}}{1 + A_v} C_F} \right) \right] \qquad (128)$$

where a is the slope of the ramp input.

The response time constant is

$$T = R_F \left[\frac{C_2 + C_{in}}{A_v + 1} + C_F \right] \qquad (129)$$

If C_2 is smaller than C_{in} and C_F, the error in rise time caused by the presence of C_2 is entirely negligible. Using this method, the uncompensated rise time was found to be 0.22 seconds for $R_F = 10^{12}$ ohms. This implies a time constant $R_F C_F$ of 0.1 seconds. To match this time constant compensating network values of $R_B = 2.2 \times 10^6$ ohms, and $C_B = 0.05 \times 10^{-6}$ farads were selected. Varying R_B confirmed that this was the most effective value for $R_B C_B$, and with this compensation the rise time was decreased to 0.009 seconds.

The poles ω_{PAB}, ω_{P12} and $\omega_{P\omega4}$ in the amplifier gain may now be found from equations (104). For the transistors used,

2N1711: $C_{TE_{1,5}} = 50 \times 10^{-12}$ f.

$C_{b'c_{1,5}} = 18 \times 10^{-12}$ f.

$\frac{W^2}{2D_{1,5}} = 2.3 \times 10^{-9}$ sec. at 25°C (130)

2N1132: $CTE_3 = 60 \times 10^{-12}$ f.

$C_{b'c3} = 35 \times 10^{-12}$ f.

$\frac{W^2}{2D_3} = 6 \times 10^{-9}$ sec. at 25°C (131)

Substituting these values, the circuit values calculated in Chapter 5, and the measured parameters, into equations (103),

$C_{b'1} = 50\text{x}10^{-12} + 2.3\text{x}10^{-9} \times 40 \times 10^{-4} + 18\text{x}10^{-12}\ (1+10^2\text{x}40\text{x}10^{-6}$ $\text{x}33\text{x}10^3) \approx 2.16 \times 10^{-9}$ f. (132)

$C_{b'3} = 60\text{x}10^{-12} + 6\text{x}10^{-9} \times 40 \times 2.35 \times 10^{-4} + 35 \times 10^{-12}$ $(1+50\text{x}40\text{x}5\text{x}10^{-6}\text{x}39\text{x}10^3) = 13.6 \times 10^{-9}$ f. (133)

$C_{b'3} = 50 \times 15^{-12} + 2.3\text{x}10^{-9} \times 40 \times 8.4 \times 10^{-4}$ $= 1.27 \times 10^{-10}$ f. (134)

The corner frequencies, from equations (104) are

$$\omega_{PAB} = \frac{44 \times 10^3 + 50 \times 10^3}{2.16 \times 10^{-9} \times 2\omega \times 10^3 \times 22 \times 10^3} = 77.6\text{x}10^3 \frac{\text{rad.}}{\text{sec.}} \quad (135)$$

$$\omega_{P12} = \frac{94 \times 10^3 + 10^4}{13.6 \times 10^{-9} \times 5 \times 10^3 \times 47 \times 10^3} = 32.6\text{x}10^3 \frac{\text{rad.}}{\text{sec.}} \quad (136)$$

$$\omega_{P34} = \frac{39 \times 10^3 + 10^4 \times 10^2}{1.27 \times 10^{-10} \times 3 \times 10^3 (39\text{x}10^3 + 10^4)} = 53.6\text{x}10^6 \frac{\text{rad.}}{\text{sec.}} \quad (137)$$

6.6 Sensitivity

The smallest measurable current value is approximately 2×10^{-14} amperes. With compensation, the noise level is increased with the bandwidth and the sensitivity is limited to about 5×10^{-14} amperes.

6.7 Power Supply Voltage Sensitivity

For both positive and negative supply voltages, the change in output voltage per unit change in supply voltage was measured at 15 millivolts/volt, at $V_1 = -9$, and $V_2 = +12$. This means that extremely well regulated supply voltages are unnecessary and regulation of a few percent will be adequate.

6.8 Supply Voltage Range

The output voltage may be "zeroed" and satisfactory performance obtained for the following ranges of supply voltage"

Negative supply voltage range: -5.5 to -13.5 volts

Positive supply voltage range: +6 to +19 volts

6.9 Allowable Input Capacitance

For feedback resistance in the range of 10^8 to 10^{12} ohms, the circuit was stable for input capacitances less than 5000 pf.

6.10 Performance Summary

Table 1

Quantity	Measured Value	Calculated Value	Typical Value Existing Systems
Voltage Gain		error	
A_{vAB}	-14.1	-13.75 (2.5%)	
A_{v12}	-17.9	-19.12 (6.8%)	
A_{v34}	-176	-180 (2.3%)	
A_v total	44,500	47,340	10^3 to 10^5
Temperature Drift	30-300μV/°C		
Response Speed			
(Rise Time, Rf = 10^{12} sc)			
Uncompensated	0.22 sec (1.5Hz)	1Hz	
Compensated	0.009 sec (37Hz)		30-50Hz
Initial Drift			
After 15 min.	22mV/hr		
After 1 hr.	3.6mV/hr		
After 4 hrs.	<1mV/hr		
Long Term Stability,			
After 5 hr. "warmup"	1.5% of full scale per week		1-2%/wk.

Quantity	Measured Value	Calculated Value	Typical Value Existing Systems
Max. Sensitivity	5×10^{-14} amp.		10^{-12} amp.
Power Supply Sensitivity	15mV/volt		
Supply Voltage Range			
Neg.	-5.5 to 13.5		
Pos.	+6 to +18		
Input Capacitance Allowed	0-5000 pf.		

CHAPTER VII

SUMMARY AND CONCLUSIONS

7.1 Voltage Gain

The voltage gain expression was determined and evaluated under limitations put on the supply voltage and the operating point. First stage gain was maximized, and second stage gain was chosen equal to 20 to reduce the effect of third stage drift, while keeping the total gain at a manageable level. Third stage gain was found to be equal to $\frac{qV_1}{2kT'}$ where V_1 is the negative supply voltage, if the output load (emitter) resistor is of moderate size. While a maximum total gain of about 50,000 resulted from the above, if the differential stages are not perfectly balanced, as is inevitable, the total gain will be somewhat less. Deliberate mismatching reduced the gain to approximately 8000. Calculated and measured values of gain compared satisfactorily with errors, falling well within the tolerance of the components used. Errors in the calculated stage gains A_{vAB}, A_{v12}, and A_{v34} were 2.5 percent, -6.8 percent, and 2.3 percent, respectively.

7.2 Temperature Drift

The total temperature drift rate voltage, referred to the input, was determined. It was found that for balanced currents and symmetrical resistance values, the total drift rate was essentially a function of the matching of transistor β's, V_{BE}'s, and V_T's and their drift rates. The predominant contribution to the total drift rate arises as a result of transistor

mismatch in the first stage with respect to V_T, β, and the β drift rates. The second and third stage contributions are of a similar nature, but are reduced by functions dependant upon the first stage gain, and the product of the first and second stage gains, respectively. As a result, while third stage contributions are virtually negligible, and second stage effects small, fairly careful first stage transistor matching is required for small drift. With such selection, drifts on the order of 20-30 x 10^{-6} volts/^{o}C are possible, using silicon enhancement mode p-channel MOS input transistors, and modern double-diffused silicon planar transistors in succeeding stages.

7.3 Response Speed

The response to a current step input was obtained and showed that the effect of any input capacitance is reduced by the voltage gain, while the effect of any parallel capacitance associated with the feedback resistor is undiminished by the gain. Consequently, if no large external input capacitor is added, the amplifier rise time is that of the feedback resistor in parallel with its associated capacitance. With feedback resistors greater than 10^{11} ohms, the response becomes prohibitively slow. To improve the response speed, a simple compensating network is described which decreased rise time by a factor of about 20, for a 10^{12} ohm feedback resistor. Measured rise times were 0.22 seconds without compensation, and 0.009 seconds with compensation.

7.4 D.C. Stability

All insulated-gate type transistors (as well as electrometer vacuum tubes, to a lesser degree) suffer initial drift when power is applied after long interruption. The resulting output drift requires several hours operation before maximum sensitivity can be approached. Typical initial drift rates are 4 millivolts/hour after one hour, 1.5 millivolts/hour after 3 hours, and entirely negligible after 5 hours, although the magnitude of initial drift, like the temperature drift, is dependent upon the matching of the input transistors.

The long term drift was found to average about $\pm$ 1% of full scale per week, after a four-hour warmup. The sensitivity of the output voltage to changes in supply voltage was 15 millivolts/volt for both negative and positive supplies, measured at + 12 and - 9 volt supply voltage. This means that highly regulated supply voltages are not necessary, and simple zener diode regulation will be adequate in most cases.

7.5 Power Supply Requirements

Satisfactory operation may be obtained for a wide range of supply voltages. The negative supply voltage may have any value from -5.5 to -13.5 volt, the positive supply any value from +6 to +18 volts. Power requirements depend upon the current level required in the output emitter resistor to accommodate the external load.

In general, power required will be less than 100 milliwatts and could be as small as 25 milliwatts.

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APPENDIX A

A.1 Insulated - Gate Field-Effect Transistor Drain Characteristics

When operated in the saturation or pinch-off region, defined by $V_d \geq V_g - V_p$ where V_p is the pinch-off voltage, the drain characteristics are given by

$$I_{ds} = \frac{\beta}{2}(V_g - V_T)^2$$

where

$$\beta = \frac{C_{ox}\mu_o}{L^2} = \frac{E_{ox}\mu_o W}{LT_{ox}}$$

and C_{ox} = oxide capacitance per unit area.

μ_o = carrier mobility

L = channel length

W = channel width

T_{ox} = oxide thickness

E_{ox} = oxide permitivity

Differentiating with respect to V_g,

$$\frac{\partial I_{ds}}{\partial V_g} = g_m = \beta (V_g - V_T)$$

or

$$g_m = 2\beta I_{ds}$$

A.2 Temperature Dependence of β and V_T

The drift rates associated with the quantities β and V_p are

$$\frac{\partial \beta}{\partial T} = -\frac{.0033\beta}{^oC}$$

and

$$\frac{\partial V_T}{\partial T} = - 1.5 \times 10^{-3} \ \frac{\text{volts}}{^oC}$$

These effects tend to oppose each other in the drain characteristic equation, and it can be shown that for a given device there is an operating point at which these effects cancel. This condition occurs when

$$I_D = 0.41\beta$$

and represents the operating point at which the gate voltage required to maintain a given value of drain current is independent of temperature.

A.3 Insulated-Gate Transistor

Small-Signal Low Frequency Circuit Model

An approximate small-signal circuit model for the insulated gate field-effect transistor opearated in the pinch-off region is shown in Figure 3a. A description of the parameters is as follows:

R_G - Gate resistance; Results from a silicon oxide or nitride layer which insulates the gate electrode from the "channel". The value is constant and ranges from 10^{10} to 10^{15} ohms.

C_{GS} - Gate-to-source (or input) capacitance; comprised mainly of the interlead and intercontact capacitances, internal gate-to-source capacitance and the active gate-to-channel distributed capacitance, C_{GC}. In saturation, C_{GC} is constant and equal to $2/3\ A_{GC}C_{ox}$, where A_{GC} is the effective gate area. Typically, C_{GC} = 1.5 picofarad for a unit with

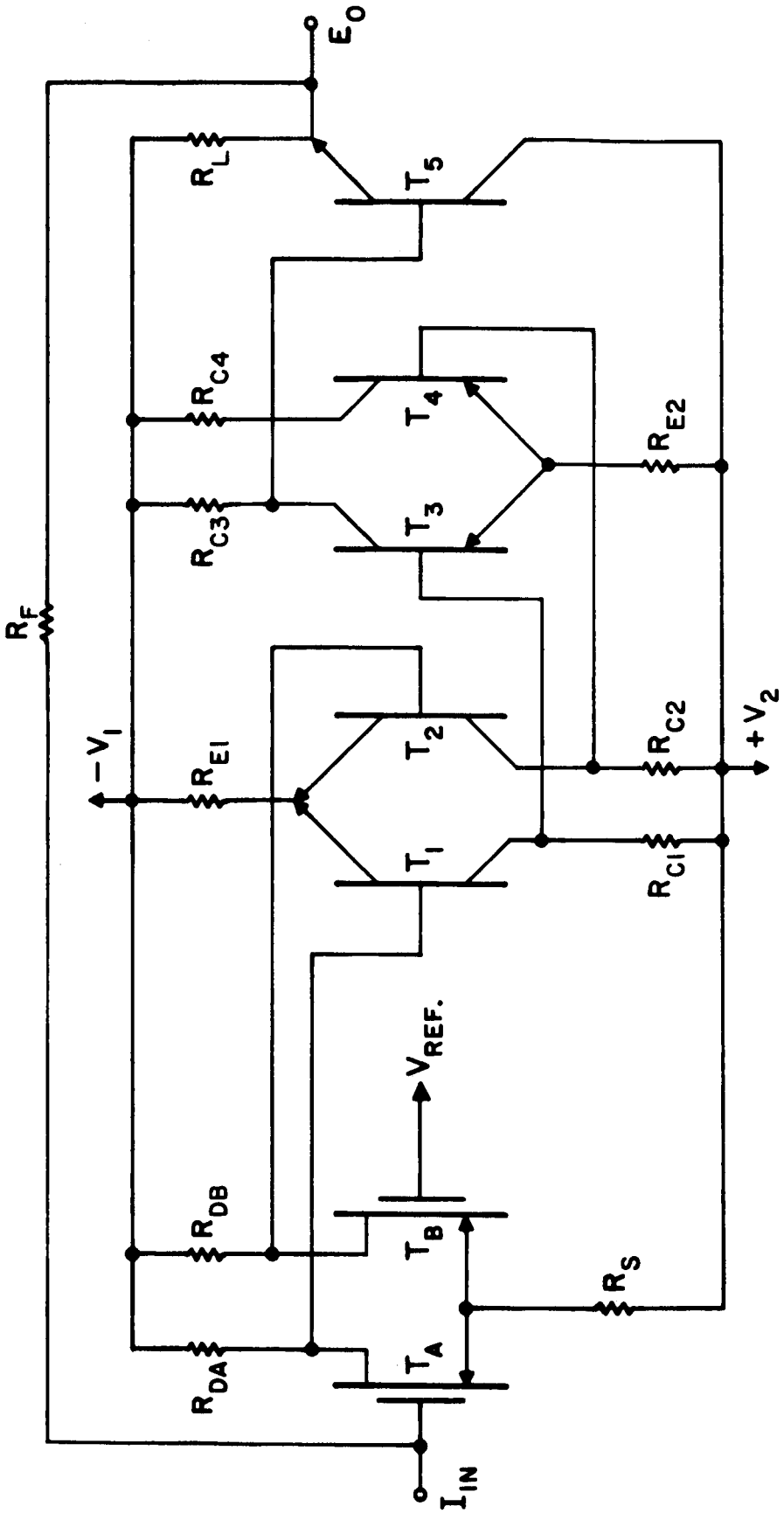
g_m = 1500 μ mhos.

C_{GD} - Drain to gate capacitance; the value of C_{GD} is constant and typically .5 to 2 picofarad.

C_{DS} - Drain to source capacitance; the total of the drain-source interlead and intercontact capacitances, and typically about 0.5 to 1.5 picofarad.

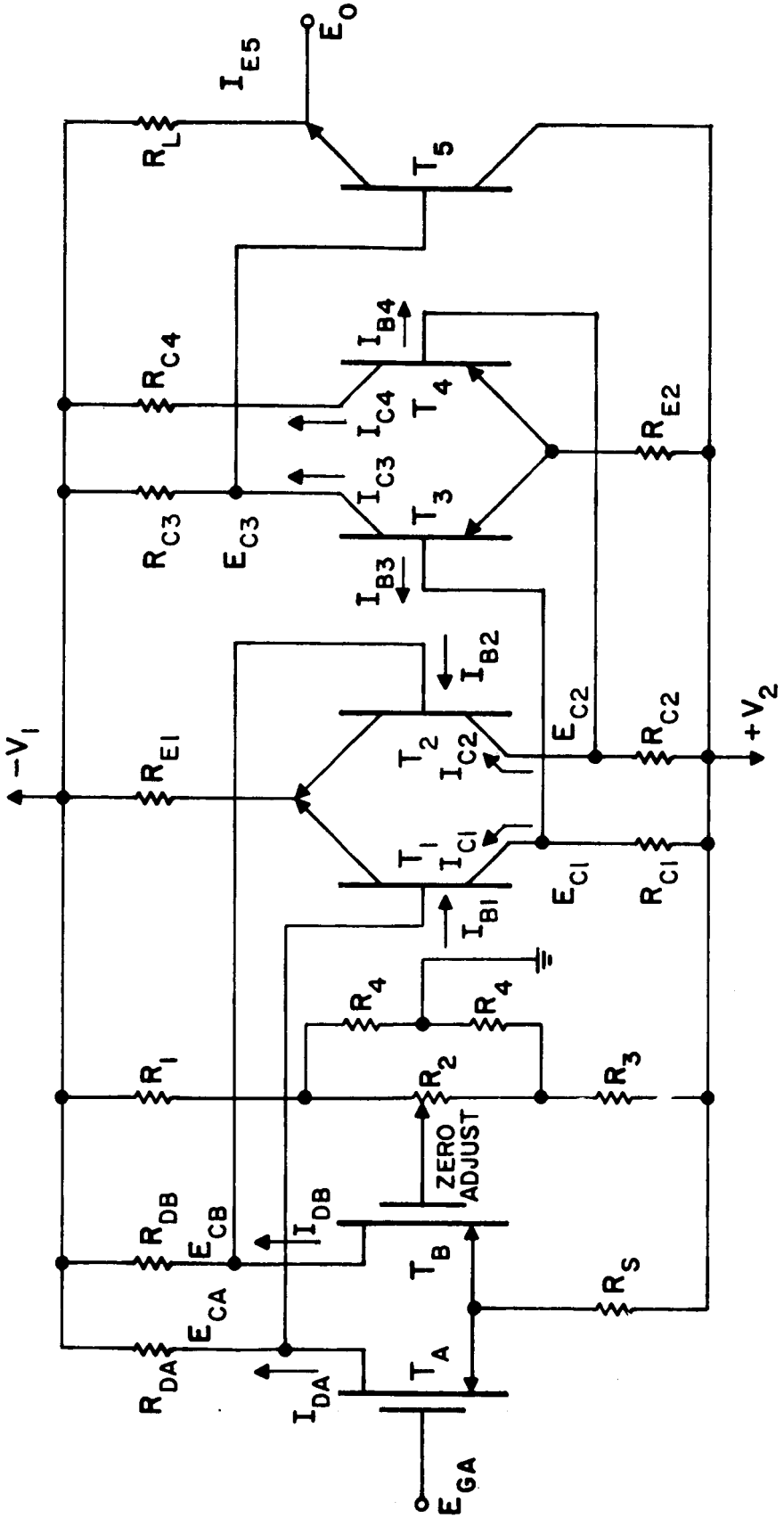
g_m - Forward transfer conductance; the partial derivative of drain current with respect to gate (to-source) voltage. $g_m = 2\beta I_{drain}$.

r_d - Dynamic drain resistance; the drain resistance is inversely proportional to drain current and is typically equal to 40 k ohms at I_D = 1 milliampere.



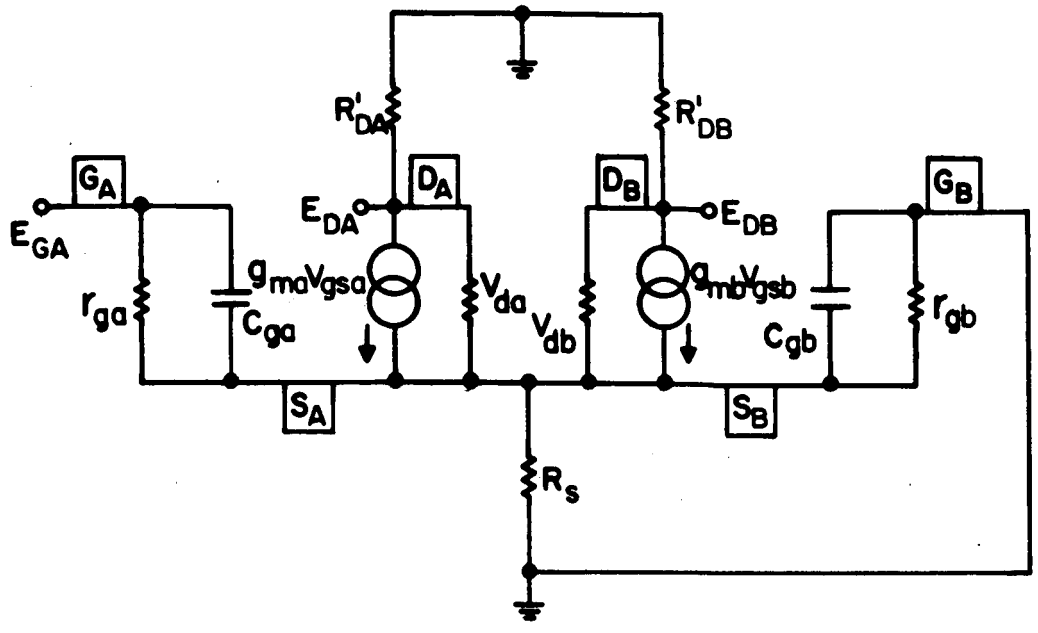
FEEDBACK PICOAMMETER, SCHEMATIC DIAGRAM

FIGURE I

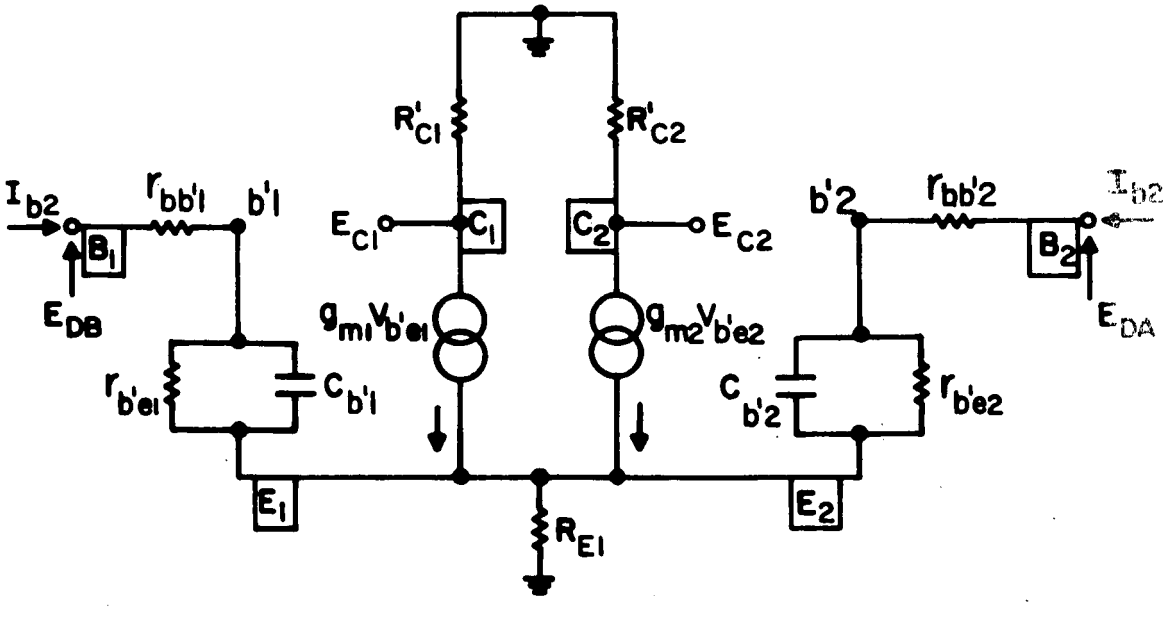


SCHEMATIC DIAGRAM FOR OPEN LOOP GAIN

FIGURE 2



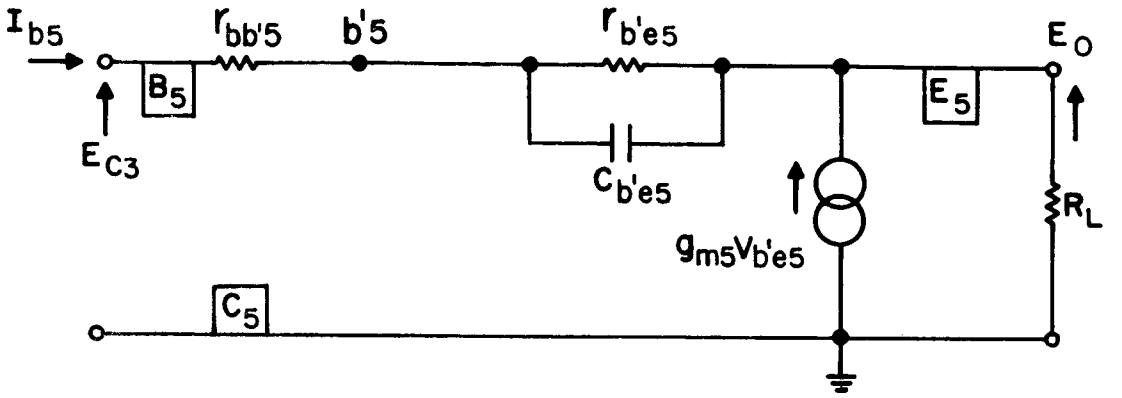
a. MOSFET INPUT STAGE



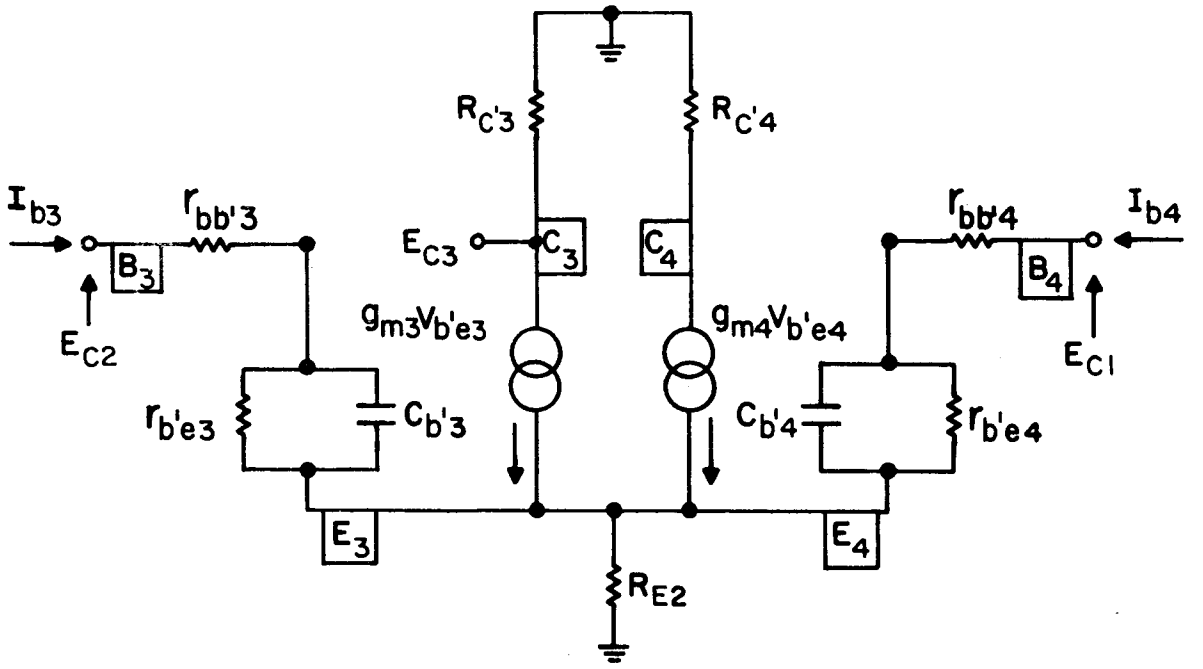
b. SECOND STAGE

SIMPLIFIED CIRCUIT MODELS

FIGURE 3



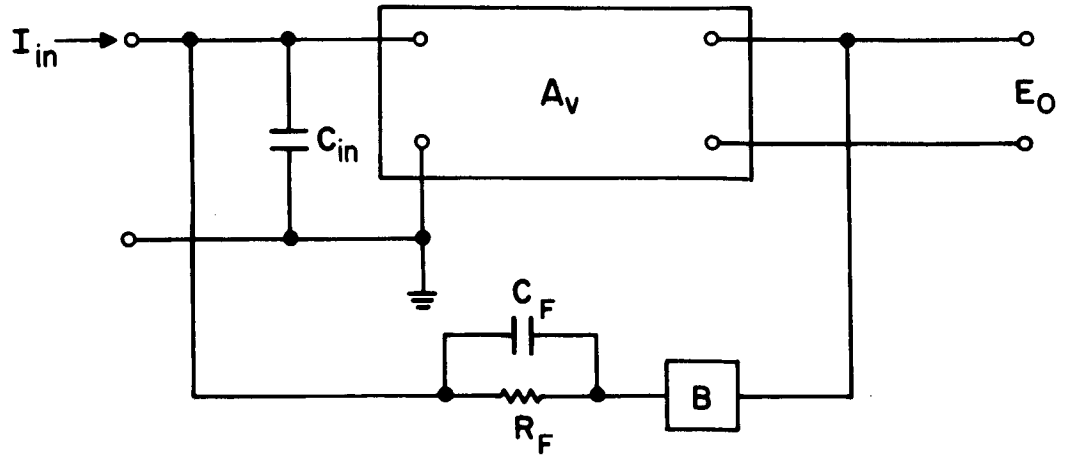
b. COMMON-COLLECTOR OUTPUT STAGE



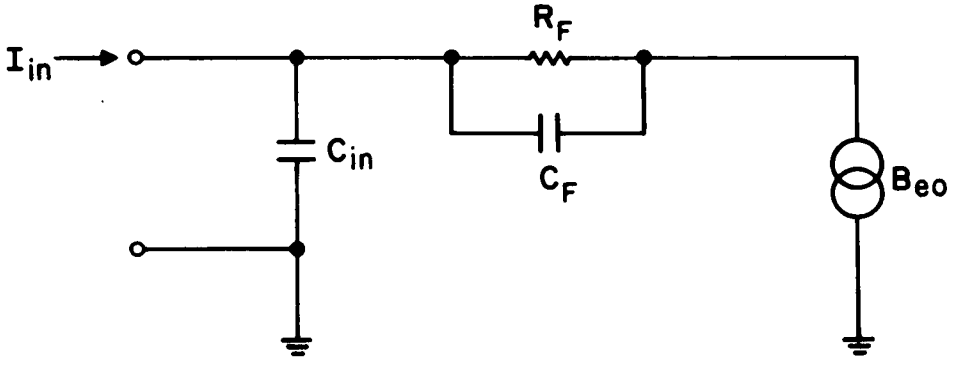
a. THIRD STAGE

SIMPLIFIED CIRCUIT MODELS

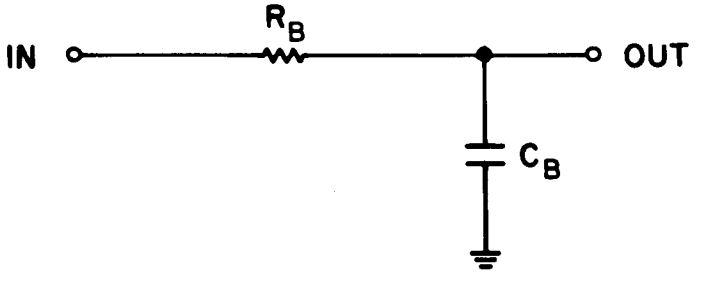
FIGURE 4



a. FEEDBACK PICOAMMETER WITH FEEDBACK CORRECTING NETWORK



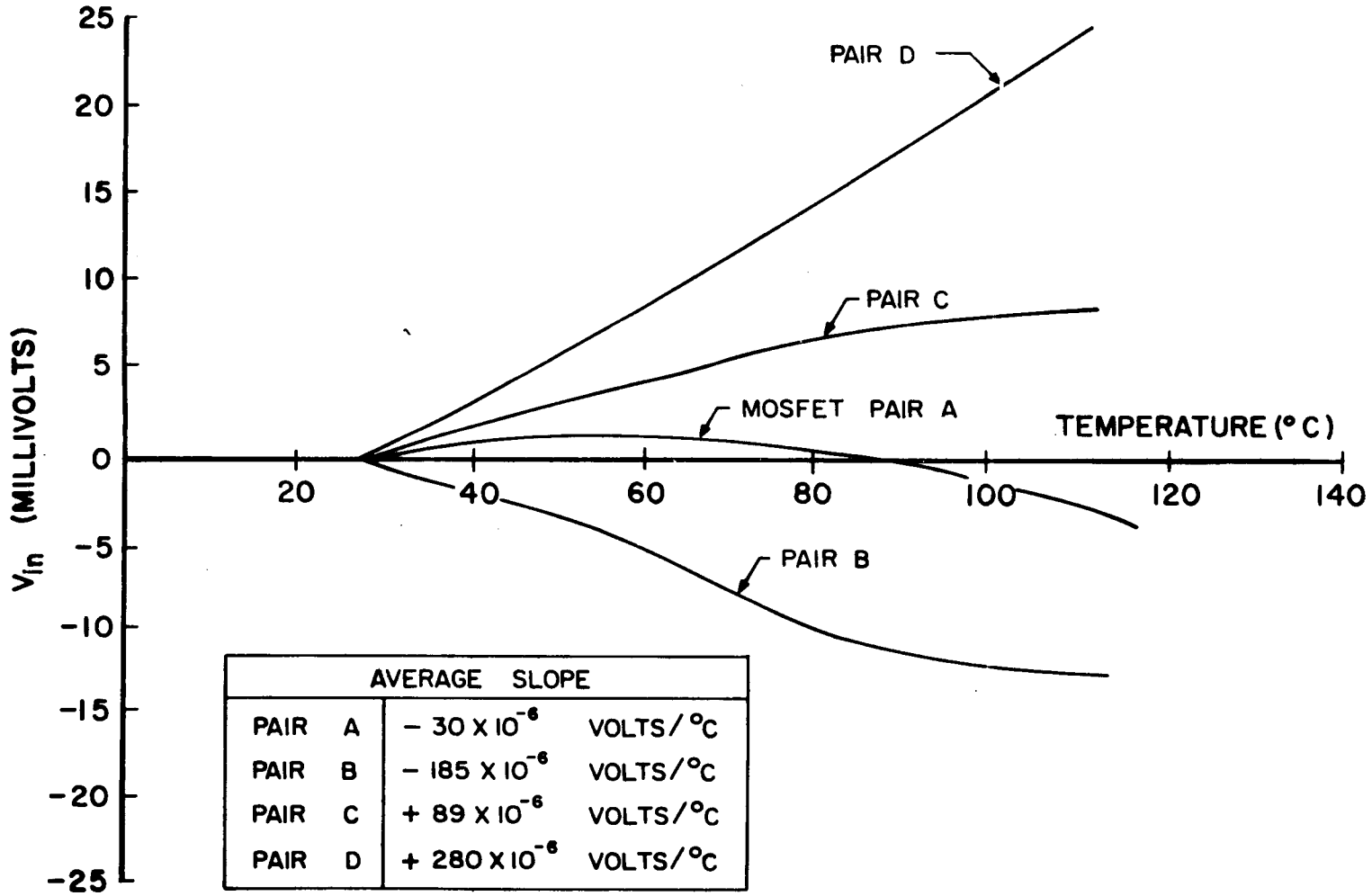
b. EQUIVALENT CIRCUIT OF FIG. 5a



c. FORM OF CORRECTING NETWORK IN FEEDBACK LOOP

CIRCUITS FOR RESPONSE SPEED ANALYSIS

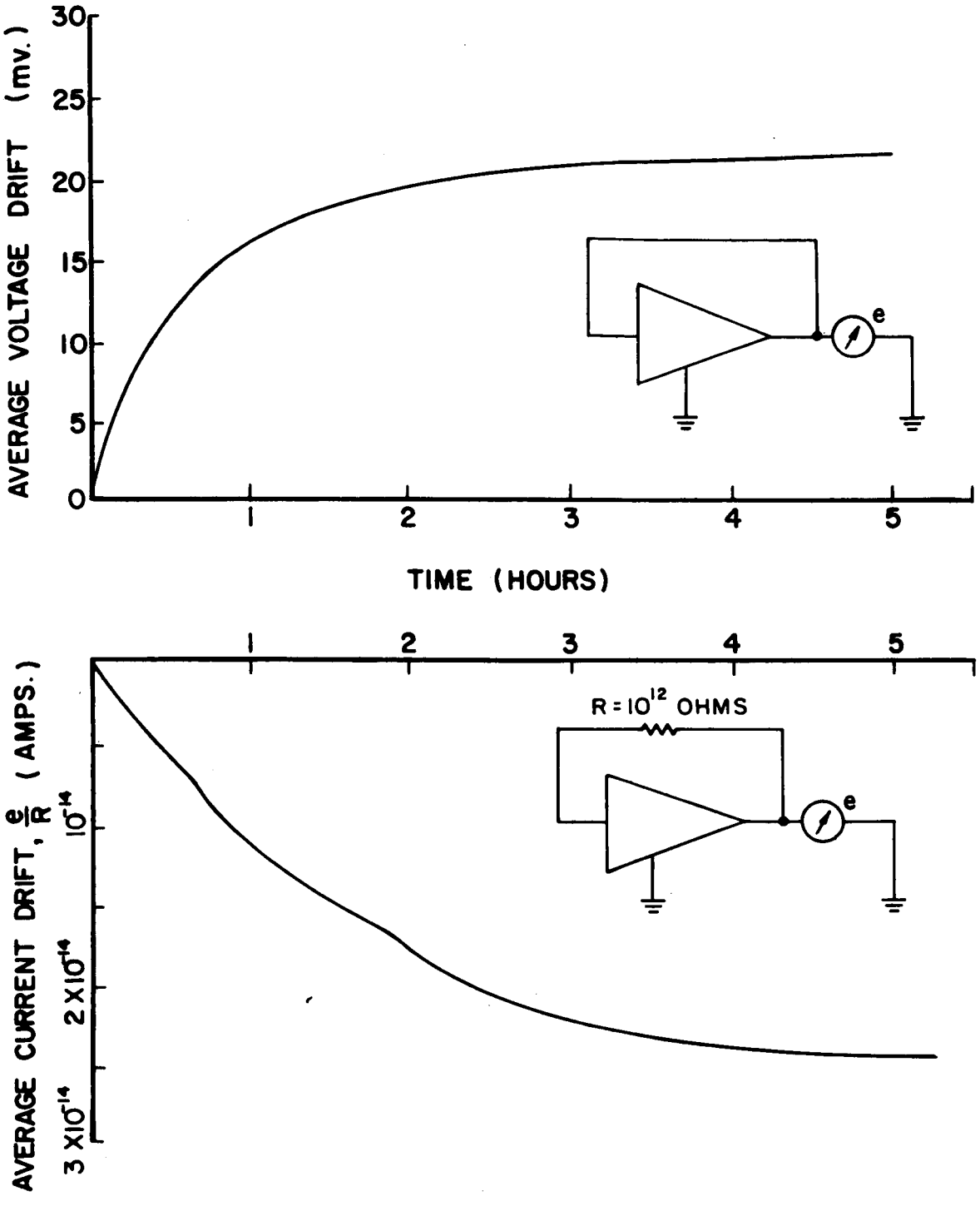
FIGURE 5



AVERAGE SLOPE		
PAIR A	-30×10^{-6}	VOLTS/°C
PAIR B	-185×10^{-6}	VOLTS/°C
PAIR C	$+89 \times 10^{-6}$	VOLTS/°C
PAIR D	$+280 \times 10^{-6}$	VOLTS/°C

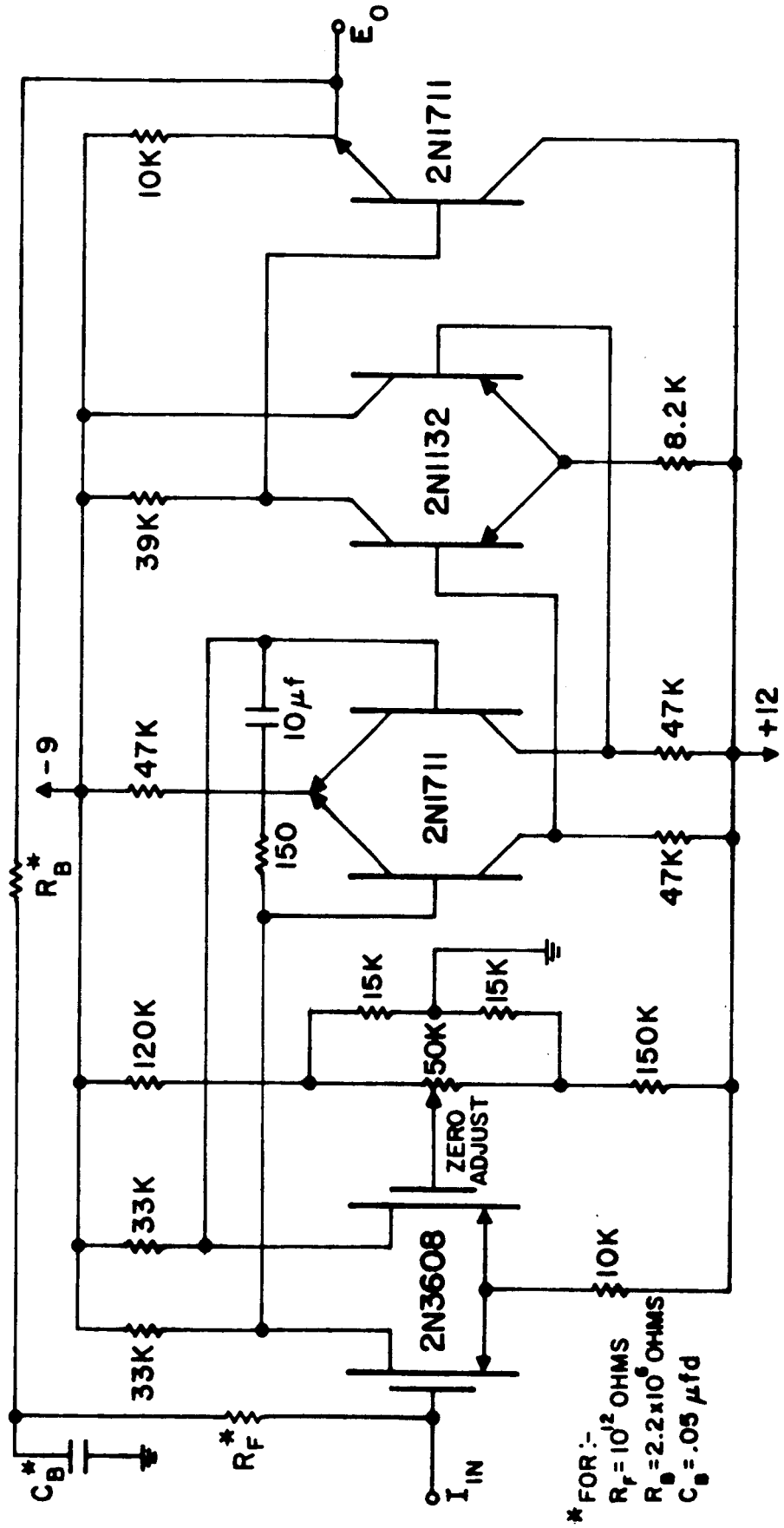
MEASURED DRIFT VS TEMPERATURE

FIGURE 6



TYPICAL INITIAL DRIFT CURVES
(MEASURED)

FIGURE 7



COMPLETE CIRCUIT WITH COMPONENT VALUES

FIGURE 8