JET PROPULSION LABORATORY

POWER SUPPLY SYNCHRONIZER

CONTRACT NO. 950237

FINAL REPORT

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Submitted by:

Westinghouse Electric Corporation
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Contract Objectives

The objective of this program was to demonstrate the feasibility and develop the technology to fabricate entire subsystems on a minimum number of chips and in a single package. The subsystem chosen as the vehicle in this development was the power supply synchonizer. Inputs to this system are 38.4 kc square wave, 3 to 5 volts peak to peak and capable of switching 3 milliamperes, or optionally 4.8 kc square wave 3 to 5 volts peak to peak and again capable of switching 3 milliamperes. Outputs are 2.4 kc square wave, 5.5 volt peak to peak, capable of switching 10 milliamperes, three phases of a three phase four-hundred cycle square wave capable of switching 50 volt peak to peak signal to an 8.2 k load from a 52 volt power supply.

Logic Design

The above described function can be performed by the logic shown in Figure 1. It consists of five stages of direct coupled binary counters each of which contain 6 diode transistor nand gates. Three phase four-hundred cycle square wave is generated by the 13 gate array shown, which is driven by 1200 cycle complimentary square wave outputs from the binary section of the system. Three complimentary output switching circuits are used to obtain the necessary high voltage swings. Circuit diagram of the high voltage PNP section is shown in Figure 2.

Low Level Logic

The original approach to fabricating the low level logic was to use Westinghouse dual nand gates which were a standard product fabricated at the Newbury Park facility. This would insure a continuing supply of material for the program. However due to the complexity of the circuit cross under tubs had to be incorporated in the pattern to insure adequate interconnect flexibility. These cross under tubs consist of high concentration N type impurity diffused into the epitaxial layer at the same time as the emitter. The fabrication and use of such cross under tubs was the subject of intensive study at this point in the program. All tests, however were done on relatively simple systems. The method of fabricating integrated circuits at this time was by a tripled diffused process. A cross section of such a device is shown in Figure 3. The basic layout of the standard dual nand gate required, for a system of this complexity, that aluminum interconnect lines of 1/2 mil width would be required to affect an interconnection of the entire circuit. This imposed several severe limitations and restrictions on the fabrication of the circuit: 1) although mask quality and photo lithographic processing technology was adequate to resolve lines of these dimensions it would have seriously affected yield to try to accomplish this over any large area; 2) an excessive voltage drop existed over long interconnections of 1/2 mil width, for these reasons it was decided to affect a complete redesign from the low level logic portion all of which was done on a single chip. The original design utilizing 1/2 mil interconnect lines is shown in Figure 2. The new design utilizing no interconnections less than 1 mil is shown in Figure 3. At this point in time a double diffused epitaxially grown silicon process for device fabrication was developed at Westinghouse.

Detailed yield studies clearly demonstrated the superiority of the new approach and since yield is the all important consideration in large area devices, the decision was made to convert from triple diffused to diffused epitaxial devices for this program. A cross section of a device fabricated by this process is shown in Figure 2, details of the process are given in the Appendix. After the final redesign in the development of the diffused epitaxy process considerable runs were made and tested. Single gate yield at this time was approximately 80%. Failures of the device were largely of a random nature. The original diffused epi process required a double epitaxial layer. This approach used a high concentration low resistivity sublayer and high resistivity top layer to obtain adequate breakdown. The sublayer was necessary to reduce the collector series resistance to provide low saturation voltage. Following this the boron isolation diffusion was performed, and severe difficulties were encountered in attaining adequate isolation through the high concentration lower epi yield was extremely low using this process. An improved process consisted of selectively depositing arsenic in the substrate material only under collector regions, subsequently low concentration epi was grown and isolation affected from the top of the epi layer. No isolation was required through a region of high concentration. Figure 4 is a cross section from a device fabricated by such a technique. On the Failure Analysis performed on many many devices unfortunately a systematic failure became evident. This was in the cross under tubs used to achieve cross overs in the interconnect pattern; although many tests of smaller devices have been made utilizing one or two diffused cross unders, the weakness of such a system did not become apparent until it was applied to a system of extreme complexity. 129 cross under tubs in all were required to affect interconnection.

Two major failure modes existed; one was failure to make ohmic contact through the opening in the silicon dioxide passivating layer and the second was alloy shorting through the oxide of the interconnect to the silicon. The overall single gate yield at this point, due to the above described failure modes and no non-systematic failure modes occurring in the individual devices was approximately 80%. This yield was much too low to attempt to build a system of this complexity and hope for any reasonable usable yield. In order to achieve a device yield at die sort of 5%, an individual gate yield of 94% would have to be realized.. It was therefore deemed unfeasible to build a system of this complexity at that time by non-redundant techniques. Another major contributing factor to the low yield was the extremely large junction area required for the cross under tubs. At this time Westinghouse proposed a continuance of effort on the basis of using multilayer metal interconnects to fabricate the low level logic section of the device. Three possible ways exist to effect large area interconnect: 1) jumper wires can be used between different sections of the device. This leads however to an extremely complex bonding scheme with extremely low reliability due to shorting of the jumper wires and the large number of gold to aluminum bonds required; 2) to use diffused cross under tubs of low resistivity N type silicon insulated by a thermal oxide from the aluminum interconnects passing over it; 3) to use conventional aluminum first interconnect over thermal oxide, followed by a dielectric material applied by one of several ways ie; a position of the aluminum reactive sputtering, of sputtering thermal evaporation, electron beam evaporation.

In the first phase of the program, Westinghouse elected to use approach number two because of the previously mentioned low reliability and complication of fabricating approach number one, and because at that time it was felt that the technology required to develop approach number three was beyond the scope of the program. Also considerable data existed on the use of cross under tubs in much less complex systems. At the end of phase one of the program, Westinghouse proposed an extension of effort to fabricate the sub system using approach number three. A major inovation in this extension of effort, phase two, was to incorporate redundancy on a component level to overcome the yield problem mentioned earlier. The first approach was to provide two components for every component required in the circuit after first metalization the wafer was 100% tested at the component level and very carefully mapped.

Rather than provide a unique interconnect mask for every device, since it was understood in advance that many devices would be processed, a scheme in which only a contact opening mask need be altered was devised. This contact opening mask was first made in a dark field version at ten times final size, it gives access to every component on the wafer.

After component selection testing has been complete and the good components selected, those components not needed are painted out on the contact selection mask. The mask is then applied to the oxide and a standard interconnect mask which gives access to all components is applied over it. During the interval between the submission of the proposal and the initiation of work yield rose

to a level at which Westinghouse felt at the level of redundancy to be reduced from three to two. In other words, for every two devices required on the wafer, three were provided. The layout was as shown in Figure . This scheme requires that two masks be altered, one the contact selection mask and two, the second interconnection masks, in that interconnect common to two devices must be opened at one point.

Accordingly, a complete redesign of the low level logic was undertaken to accommodate the redundancy approach.

At this time a major cause of failure was shorting of the first interconnect aluminum to the substrate through pin holes in the thermally grown oxide; consequently it was felt necessary to minimize the amount of the aluminum on the first interconnect and have the level of redundancy individual components. At first approach to the design attempted to accommodate the entire low level logic section in one chip. This was later deemed unfeasible, in that the complexity of the first interconnect required for the three phase generator was greater than that required for the five bit binary; and to impose this increased complexity on the entire device would severely limit yield. Therefore, it was decided to break the 44 gates of the low level logic into two chips, one containing five bit binary and the other containing the thirteen gates of the three-phase generator, plus an output buffer gate. The first chip, the N, by 32 function measures .285 by .285". The second chip measures .190 by .285". At this time JPL expressed a desire to be able to operate at 4.8 kc sometime in the future.

This was accomplished by bringing the output of the third binary out on a separate pin, putting the input to the fourth binary on an ajacent pin. For 38.4 kc operation, these two leads are shorted. For 4.8 kc operation, they are opened and 4.8 kc applied to the input of the fourth binary. The entire device draws three preceding binaries draw current in this mode of operation, but no signal path exists through them. The third chip in the system was the high voltage NPN which measures .130 by .130". The basic mask set was the same as the low level logic, although it would have been possible to reduce the size of the chip by redisigning specifically for this application, and it would have been possible to avoid multi-layer interconnects on this chip. It was felt economically advantageous to do it with the same mask set as the low level logic, since the overall package size was determined by the low level logic section anyway. Since the complexity of the multilayer interconnect on this section of the device is considerably less than on the low level logic section. The fourth chip was the high voltage PNP output switch, the substrate of which is mounted on an isolated island.

Multilayer Interconnect Process Development

Consider the requirements of the materials and processes involved in fabricating a no caps, multi-layer interconnected device. The first metal must make ohmic contact to silicon, adhere well to thermally grown silicon dioxide; be easily etchable in a substance that does not attack the oxide; the dielectric deposited over these interconnects must have the following properties:

1) Adhere well to thermally grown silicon dioxide as well as to the metal of the first interconnect.

2) Be pin-hole free.

3) Not introduce significant capacitance between the two layers

4) Be configurable by anyone of several techniques.

5) Must also be impermeable to any solvents that will attack the first interconnect.

Several systems answer some of these requirements to a greater or lesser degree. One system considered was aluminum oxide formed by anodization of the first aluminum interconnect. However, grave difficulties arise in forming the oxide on vertical steps. This can be overcome by a separate masking step. Another grave difficulty is in configurating the contact openings in the aluminum oxide. Most significantly the capacitance per cross over would be excessively high.

Another system is aluminum silicon dioxide aluminum. There are various techniques for evaporating silicon dioxide. The approach chosen by Westinghouse in the first part of the program was reactive evaporation. In this approach, silicon monoxide is evaporated from a Tantalum boat in an oxygen atmosphere. After this step, contact openings are etched in the oxide and the aluminum of the second interconnect deposited and configurated in the usual manner. Several problem areas existed in this process. One was

the control of the etching of the oxide. The etchant in use at that time attacked the aluminum as well as evaporated oxide, consequently when contact openings were etched in the oxide, the underlying aluminum areas were destroyed in some sections of the device.

Two possible solutions existed: 1) evaporate a barrier metal over the first interconnect which was not attacked by the oxide etch; 2) formulate an etch which would selectively dissolve the oxide and not attack the aluminum and for which an adequate photo resist exists. It was found that a dilute solution of hydrofluoric and phosphoric acids fulfilled the requirements of approach number 2. Several runs were made and a weakness in this design became apparent.

In areas where contact openings in the second oxide did not register perfectly with the first interconnect, the thermally grown oxide on the silicon was exposed to etch solution. The rate of solution of thermal oxide in this etch is many times greater than the rate of solution of evaporated oxide. Consequently wide spread disastrous undercutting resulted. This problem was solved by making pads on the first interconnect larger than the contact opening. However, the major problem in this approach was in control of the composition of the evaporated oxide. By the reactive evaporation approach, an oxide intermediate in composition between SiO and SiO_2 is attained. The range of composition over which this oxide has the necessary properties is extremely small. If the oxide approaches SiO in composition, it has excellent insulating properties and is pin-hole free. However, it is of such composition that it cannot be etched by buffered HF solutions.

If it approaches SiO_2 in composition, it is easily etchable but the incidence of pin holes increases and the number of shorts between first and second interconnects becomes excessive. Two possible solutions to this problem existed: 1) to find an etch which would attack SiO but not aluminum or SiO_2. An extremely unlikely set of conditions to be met. The other was to investigate the possibility of using a metal other than aluminum for the first interconnect which would not be attacked by the SiO etchant and therefore would act as a barrier to attack of the first oxide. However, this approach would meet with many problems, the primary one being the inherent porosity of evaporated thin films would make it difficult to fabricate a film of density sufficient to be a barrier to any etchant. The third possibility was to evaporate silicon monoxide over a positive photoresist. This process then became the standard one. Photoresist is applied to aluminized areas which were desired to be kept free of oxide. This was facilitated by using a resist which deploymerized upon exposure to ultra violet light, therefore a light field mask can be used. Step two - evaporate silicon monoxide over the entire surface including areas covered by photoresist. Step three - after evaporation, a high pressure solvent spray is directed at the surface to remove the photoresist. In areas overlying the photoresist, the oxide cracks, allowing penetration of solvent and subsequent solution of the photoresist. Further solvent spray removed all resist and overlying oxide.

The entire process of development is completed in 60 seconds exposure to the spray. This approach has several advantages and is the basic one in use at this time.

The advantages are:

1. Extremely sharp resolution, much higher than attainable by etching.

2. Silicon monoxide is extremely easy to evaporate if the problem of controlling oxide composition by oxygen pressure is removed.

3. A pin hole free oxide of excellent electrical characteristics is achieved.

At this time, further difficulty was encountered. This was opening of the second interconnect over steps in the oxide. This was due to the fact that standard aluminum evaporations took place from a source normal to the surface of the wafer. On vertical surfaces such as the step-over first interconnect, very little material is deposited. During etching, these areas became much thinner and can become a hot spot or undercut to the point of opening. This condition was somewhat alleviated by evaporating aluminum from multiple line sources at an angle of incidence at 60^{o} the surface of the wafer. Using this approach, the first large scale array was fabricated, a six gate binary containing 54 components was fabricated, packaged, tested and delivered to JPL.

At this time a further difficulty was encountered. This was in the etching of the second interconnect. The aluminum was approximately 10,000Å thick and to avoid the undercutting at this step. Previously described control of etching was extremely critical to the successful fabrication.

When extended to large area arrays, this control becomes impossible to achieve, due to the uneven thickness of the aluminum and the uneven etching rate of aluminum over large areas. So that it was felt necessary to use a material rejection mask to configurate the second interconnect. This mask works in a manner identical to that described for the configuration of silicon monoxide using positive photoresist.

The first seven attempts to fabricate devices of moderate size produced three functioning six gate binaries, one of which was packaged and shipped to JPL for evaluation purposes. The aluminum being evaporated from multiple high angle of incidence line sources. However, the thickness attainable by this technique is not very great. The problem is that the resist is suceptible to destruction by heating and if an evaporation takes place over a long period of time or at an extremely high filament temperature or in close proximity to the filaments (at least one of these conditions is necessary to achieve thickness) very hard setting or carbonization of the resist occurs. Other alternative is to apply the aluminum in multiple evaporation, however, this leads to an undesirable oxide barrier layer between the various aluminum evaporations, even if the devices are kept in vacuums.

The failure mode resulting from thin aluminization is discontinuity of the second interconnect aluminum through the opening from the top of the oxide to the top of the first interconnect aluminum.

This lack of continuity between the two layers is a result of using positive photoresist to configurate the evaporate oxide. Referring to Figure 5, if the contact openings are configurated by etching, a cross section through the opening appears as in Figure IB. During subsequent metal evaporation, a thin layer of aluminum will be deposited on areas "A". In the case of oxide evaporated over photoresist, the ideal case appears as in Figure IA; in practice however, the cross section is the one shown in Figure IC. It can be readily seen that even with high angle of incidence metallization sources, the area "A" would receive little or no metal.

The following approach was made to solve this problem:

After the oxide has been evaporated and removed from contact areas, aluminum of a thickness slightly greater than the oxide thickness is evaporated over the entire device. The same contact opening mask as was used on the oxide contact opening is used to expose a negative photoresist on the aluminum. The device is then etched in an aluminum etchant, leaving the contact openings filled with aluminum and all other areas free. Figure II shows a cross section through the contact at this point in the process. The second interconnect is then applied in the normal manner; a cross section of the final structure is shown in Figure 6 . At this time another failure mechanism became apparent, in the configuration of the contact filling aluminum by etching. If perfect alignment with the first interconnect was not attained, a narrow band of 1st interconnect aluminum was exposed to etch and during configuration was attached and opened. Two approaches were made to alleviate this problem.

In the first, aluminum for the contact hole filling operation was evaporated through a positive photoresist mask and in the second an oversize contact mask was made to insure alignment at the contact areas.

First approach is unfeasable due to the previously mentioned difficulty involved in building up thick layers through a positive mask. The second was unfeasable due to the extremely close spacing of some of the contacts. At this time, enough data on yield levels had accumulated to make possible a re-evaluation on the redundancy level required. Since the inception of the program, on the yield had increased to a point well in excess of 95% and it was decided to lower the redundancy to the gate level. On this approach, whole gates are connected on the first interconnect. Testing is then done on the gate level and the free selected gates are connected on the second interconnect. The major contributing factor to a yield improvement was an improvement in the thermally grown oxide that reduced to an extremely low level the number of alloy shorts from first interconnect to silicon.

The advantage to gate-level redundancy are obvious; testing time is considerably reduced by a factor of approximately 15; the number of cross-overs was reduced by 50% and the number of contact openings, always a potential failure point, was reduced to 20% of the original number. The one possible disadvantage is the reduction in overall reduction devices attainable per wafer did not materialize. The first device run at the gate level was 40% functional, two binarys of the five were operational. The use of positive photoresist to configurate the contact hole filling and the second interconnect aluminum proved to be an unworkable system for the following reason:

After the application of the photo-resist and immediately prior to evaporation of the aluminum, ie, during the operation of the pump-down cycle in evaporation, a thin barrier layer of organic material outgases from the photoresist and prevents adequate adhesion of the aluminum to the silicon monoxide and imposes a high resistance barrier layer between the aluminum of the first and second interconnect. This difficulty is non-existant on the oxide evaporation step because the total amount of photo-resist present on the surface is extremely minute. In all of the aluminum steps, however, an extremely high percentage of the surface is covered with organic material and very small areas are left open. The difficulty experienced in attempting to configurate second interconnect and contact hole-filling aluminum by etching was due to the slight permiability of silicon monoxide to aluminum etchant especially along vertical surfaces on the first interconnect where the oxide is extremely thin. Two approaches were taken to solve this problem, one was the use of a multi-metal system, the second interconnect of which could be configurated by etching in a substance that did not attack the metal of the first interconnect.

Several systems were investigated such as aluminum for the first interconnect and nickel-gold or titanium gold for the second interconnect. The use of either nickel or titanium underline the gold of the gold of the second interconnect was necessary to insure adequate adhesion to the silicon monoxide. Strong oxide bonds were achieved between these metals and oxides of silicon. The process worked extremely well as far as adhesion lack of shorting and all make contact with the first interconnect was concerned, however the major difficulty was encountered in configurating the second interconnect.

This was a two-step process, photo-resist was first applied to the surface of the gold, the gold was etched in a solution that did not attack nickel and then the nickel was etched in a solution that did not attack gold. This was a step that was possible to monitor visually and so at the time the multi-metal layer approach was deemed unfeasible. The second approach taken was to attempt to apply a substance to the surface of the silicon monoxide which was compatible with it with the metal of the second interconnect and which sealed the permiability and porosity of the silicon monoxide. The system developed was to deposit silicon monoxide in the normal manner and then deposit pyrolytic SiO_2 over it. The special pyrolitic process was developed for this program that insured deposition of an oxide at low temperatures. The normal high temperature oxide process could not be used because alloyed aluminum silicon areas exist on the wafer and the process was far higher than the eutectic between these two substances.

A workable low-temperature process was developed that deposited pyrolitic oxide at 280°C. This process requires one additional masking step to remove SiO_2 from the contact areas. The thick layer of aluminum can then be deposited over the device and configuration of the second interconnect achieved by etching. The increased thickness of the aluminum insured continuity through the contact openings and over high verticle steps over the first interconnect. This process proved workable and is the one standardized upon by Westinghouse.

The second attempt at this process is the five-bit binary section of the subsystem was fabricated. At this time, all effort was expended on fabricating a three-phase generator chip since enough material of each of the other devices was in existance to fabricate

one system, however, the slight mis-sizing of the second interconnect mask of the three-phase generator made it impossible to fabricate this device without first resizing the mask. At this time the funds on the contract were expended and Westinghouse stopped work until further funding became available. The first task performed when this funding became available was an extremely accurate resizing of the second interconnect mask, however further difficulties were encountered in the 3-phase generator portion of the device. These were simple yield failures and the capability to push enough material through did not exist at Westinghouse, therefore another approach was taken to maximize the yield. This was to use a three JK flip-flop approach shown in Figure . The advantage of this approach was to reduce pre-testing time a considerable reduction in the number of cross-overs, a considerable reduction in the number of contact openings to be made from first and second interconnect out of the great increase in size of these contacts. Also to further insure adequate low contact resistance between the first and second interconnect the device is etched in an etch that will attack aluminum oxide but not aluminum for 10 minutes immediately prior to second interconnect evaporation and kept in an inert atmosphere for transfer from the etch to the evaporator. This was the technique by which the 3-phase generator was successfully produced.

The output section of the 3-phase generator has presented some unique problems in integrated circuits.

NON-LINEAR LOAD SWITCH

Initial design consideration indicated that the 50 volt square wave output switches could be made by using an NPN switching transistor with a field effect load resistor as shown in Figure 1. This device would limit the current flow in the "on" condition and allow the output to approach the 52 volt supply in the "off" condition. However, in order to obtain a triode region resistance of small enough value to meet the 50 $\pm$ 1 volt output requirement, pinch off current greater than 15 milliamps would have been required due to the physical limitations of the device structure. This would have resulted in a power dissipation of greater than .37 watts per output switch, an intolerable situation for this application. For this reason, a circuit with a "switching load" was designed for performing the high voltage output. This circuit shown in Figure 9 provides low power dissipation because a negligible current flows during the ground portion of the cycle.

The necessity of both NPN and PNP structures greatly complicated the processing for producing a single chip as shown in Figure 6. For reasons of increased reliability and to decrease the complexity of processing, the decision was made to fabricate the switch in two separate operations. The dotted lines on Figure 6 indicate the portions as divided. Figure 7 shows the structure proposed for the NPN portion of the switch. Figure 8 shows that proposed for the PNP.

The NPN portion of the output switch was fabricated and typical parameters were as shown below:

OUTPUT

V_{CER} = 68 volts

h_{FE} = 30

R_{Load} = 5K

V_{Offset} = 100 millivolts at I_B = 1.6 ma, I_c = 0

V_{CBO} = 85 volts

$V_{Isolation}$ = 110 volts

Samples of these devices were tested functionally under environmental conditions of -55°C to + 100°C. Rise and fall times of less than 5 micro seconds were maintained over the complete range. The offset voltage was less than 200 millivolts under all conditions. However, the yields on this device were quite low due to the difficulty of achieving isolation.

A selective high concentration boron diffusion was used to obtain isolation during a long high temperature diffusion cycle. This has serious disadvantages in obtaining isolation at the low concentration end of the diffusion profile, as it had to penetrate through the moderately high sub-layer concentration. Experiments showed that by using a selective diffusion of high concentration "N" type dopant, prior to growing the epitaxial layer, the isolation problem was greatly simplified. The sub-layer was diffused selectively in areas that did not require the isolation diffusion. Thus the boron diffusion only needed to diffuse through the single top layer of N type material which has a moderate resistivity.

This configuration as shown in Figure 9 was quite successful and has become the standard method for fabricating high breakdown transistors at Westinghouse.

Some difficult problems were met in building the PNP portion the output switch, principally that of obtaining good electrical isolation of components. One problem came from the high vapor pressure of phosphorus. When a P-type epitaxial layer is grown over the selective N-type (phosphorus), diffusions into the substrate, the phosphorus dopant tends to re-deposit over the entire epitaxial junction interface, producing an N-type layer. This effect is referred to as "swamping". Several methods can be used to reduce this effect: (1) using a lower N-type sub-deposition (phosphorus) concentration; (2) etching more of the selective diffused substrate before epitaxial growth; (3) growing a more concentrated (lower resistivity) P-type layer epitaxially; (4) injecting dopant at a very high rate during the initial growth period. Many considerations limit the exclusive use of any one of these methods and tests showed that moderate use of each was the best plan. Thus, as shown in Figure 6, after phosphorus sub-deposition, a high concentration P+ layer is epitaxially grown, followed by a lower concentration P layer with sufficiently high resistivity to sustain the required 52 volt breakdown. The initial P+ layer also helps lower the collector series resistance which was higher than desirable in early runs.

This was necessitated by the mounting potential being established at the ground level for the majority NPN devices. If five layers were not obtained, the device would be shorted and a diode forward bias would be obtained to the ground level, thus preventing proper operation of the circuit. The subdeposition isolation bucket shown

in Figure 4 is a critical portion of the isolation. The concentration must be high enough not to be overcome by the P epitaxial growth. However, it must be low enough not to out-diffuse and compensate the P collector tub region. The N-type isolation diffusion must be obtained from top and bottom due to the high concentration P first epitaxial layer. The isolation of this device has proven to be quite difficult. One of the major problems encountered has been that of "swamping out" of the sub-tub impurities. The high vapor pressure of the sub-deposition results in a distribution of N impurity along the interface of the substrate epitaxial. Incomplete electrical isolation from component to component is the consequence. This problem was overcome after properly adjusting epitaxial growth conditions.

A second problem which has proved equally difficult to solve was that of growing a high resistivity P epitaxial layer on top of the first moderate resistivity layer. The first layer was required to obtain moderate to low collector series resistance. Several runs were processed which resulted in low collector-emitter breakdown. The primary cause for this was out-diffusion of the sub-epitaxial layer during the vapor phase growth of the top layer, and additional diffusion of the higher impurity region into the upper low concentration region during subsequent diffusion processing. The solution to both of these problems was obtained by experiments resulting in improved techniques.

A third problem encountered in the basic PNP structure was that of obtaining good alloy contact. The material most commonly used for interconnection of integrated circuits is aluminum. It dopes P-type and works well for making contact to NPN structure because

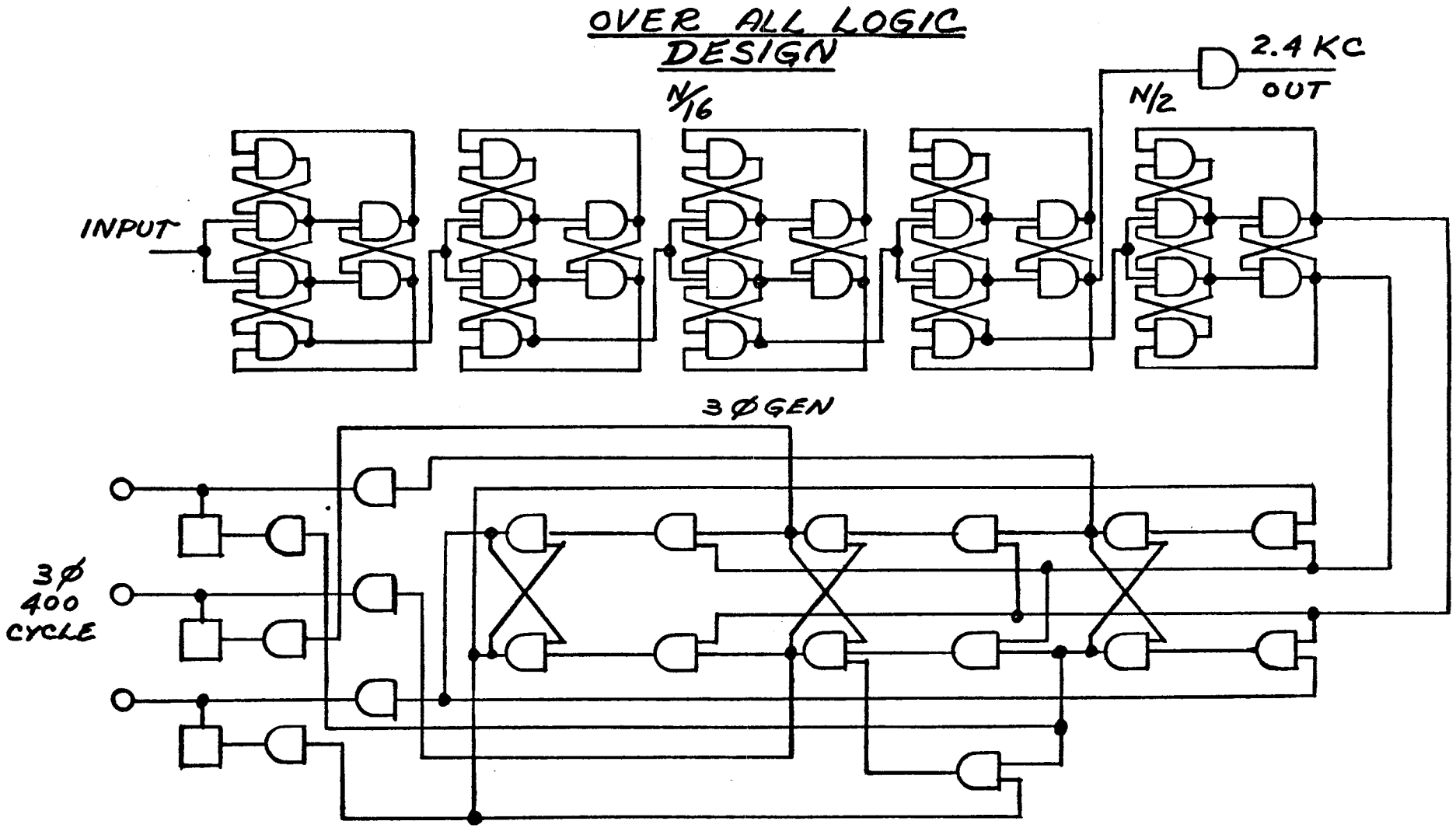
the emitter and collector region are high concentration N-type and the base is of a moderate P-type. The base of a PNP structure is of moderate N doping and rectifying contacts are obtained from aluminum alloyed to the base region. A test wafer proved that this took place at the concentration levels being used. To eliminate this problem of junction formation, several contact materials were considered: 1) gold, 2) antimony doped gold, 3) doped aluminum to reduce its P concentration, 4) doped silicon, 5) an N+ diffusion under the contacts. Considerable effort was directed towards solution of the moderate concentration N to metallic contact bond. Experiments were performed with doped aluminum and silver alloys, and some simultaneous evaporation of different metals. Several of the techniques used provided non-rectifying contact, but had an undesirably high ohmic resistance. At the conclusion of these experiments, the amount of effort required for a complete solution by this technique appeared to be too long for incorporation into this project. A satisfactory process for gold contact formation was perfected and used as an interim solution. However, it is considered to be undesirable for high temperature storage applications due to the formation of a brittle gold aluminum complex. For this reason an N+ diffusion in all N regions was incorporated so that alloyed aluminum contacts could be made without rectification.

The disadvantage of this system is a requirement for an additional photomasking and one additional diffusion. However, quite good results were obtained by this process. Of the thirteen runs processed for this particular circuit, eight were rejected due to poor isolation and leaky junctions. V_{CEO} values were below that of the design center. Three completed runs suffered from the same difficulty.

Due to the complexity of the five layer device, it was decided to isolate the PNP in mounting in the "Proposal for Continued Effort on the Molecular Electronics Power Supply Synchronizer".

By July 1965, sufficient PNP units had been produced to complete the project. These units met all parameter specifications. The final configuration is shown in Figure 8 .

One of the basic problems which has caused fabrication difficulties in all devices is that of soft junction breakdown, particularly isolation. This soft reverse characteristic can be in some cases attributed to trace metallic ions in the bulk of the semiconductor material. Prevention of the exposure of the material to metallic substances is almost impossible. The most outstanding example is the heater coils used in the furnace to generate temperatures in the order of 1200°C. There are however, methods for removing these contaminates by using gettering to draw them out of the silicon material. Copper, gold and iron are three of the metals which posses a very large gradient in their temperature solubility curves, which results in precipitation of those metal ions present in the semiconductor material into localized areas. These areas, most generally cause a premature, localized breakdown through the nucleation of foreign material. The incorporation of a gettering phase following all other processing has resulted in a considerable improvement in all junctions of NPN and PNP alike. The results obtained have shown a much more uniform isolation characteristic which has been one of the primary failure mechanisms. Leakage currents were shown to be reduced from 1 to 2 orders of magnitude in most cases.



JPL THREE PHASE POWER SYNCHRONIZER

FIG 1

LOW VOLTAGE NPN

(DIFFUSED DOUBLE EPITAXIAL)

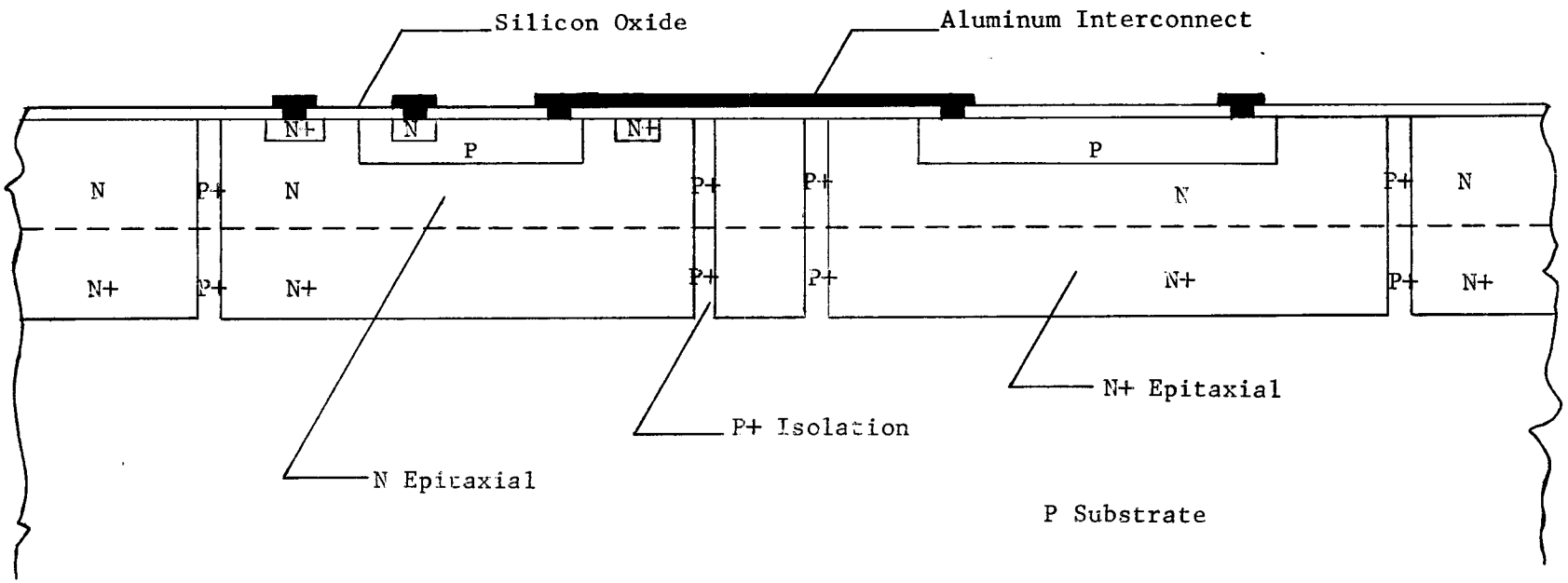


FIGURE 2

NPN TRIPLE DIFFUSED

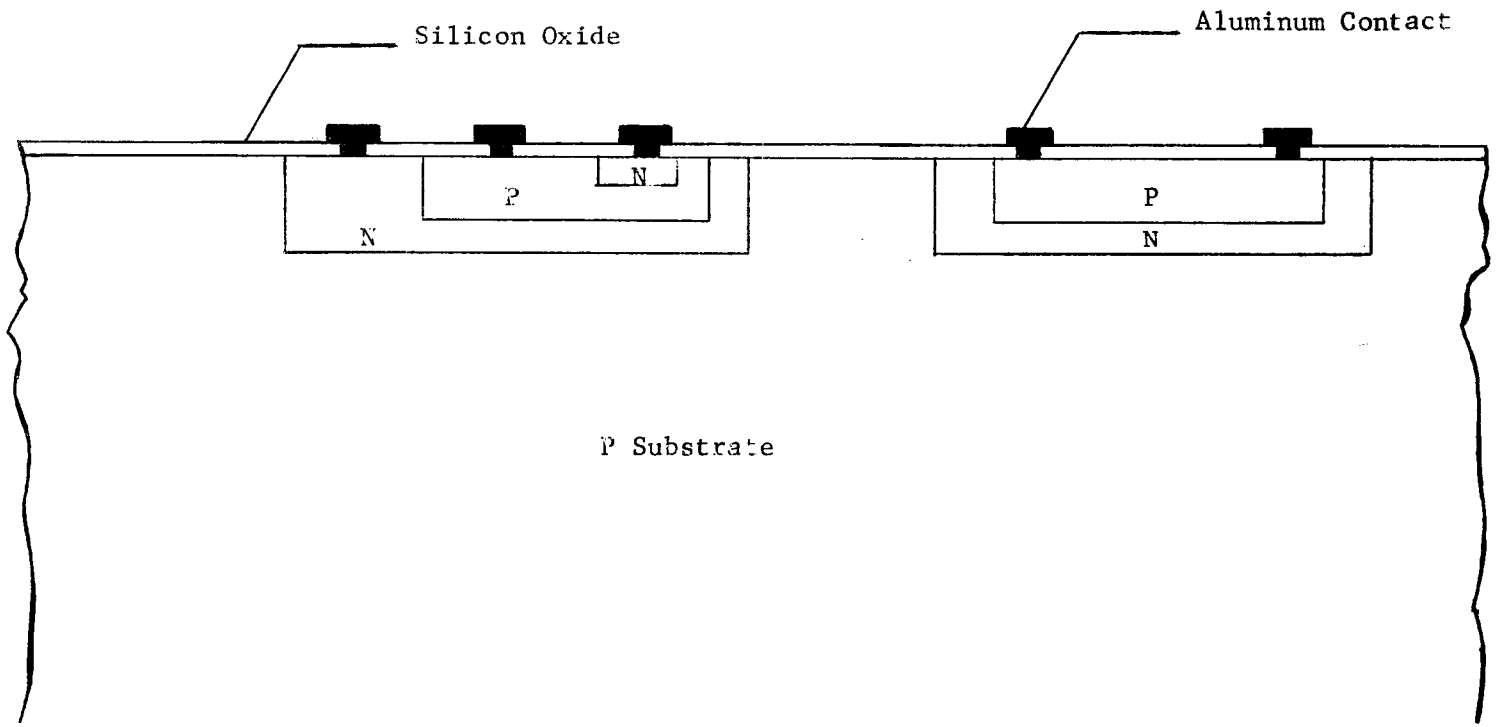


FIGURE 3

LOW VOLTAGE NPN

(DIFFUSED SINGLE EPITAXIAL WITH
COLLECTOR SUB-DEPOSITION)

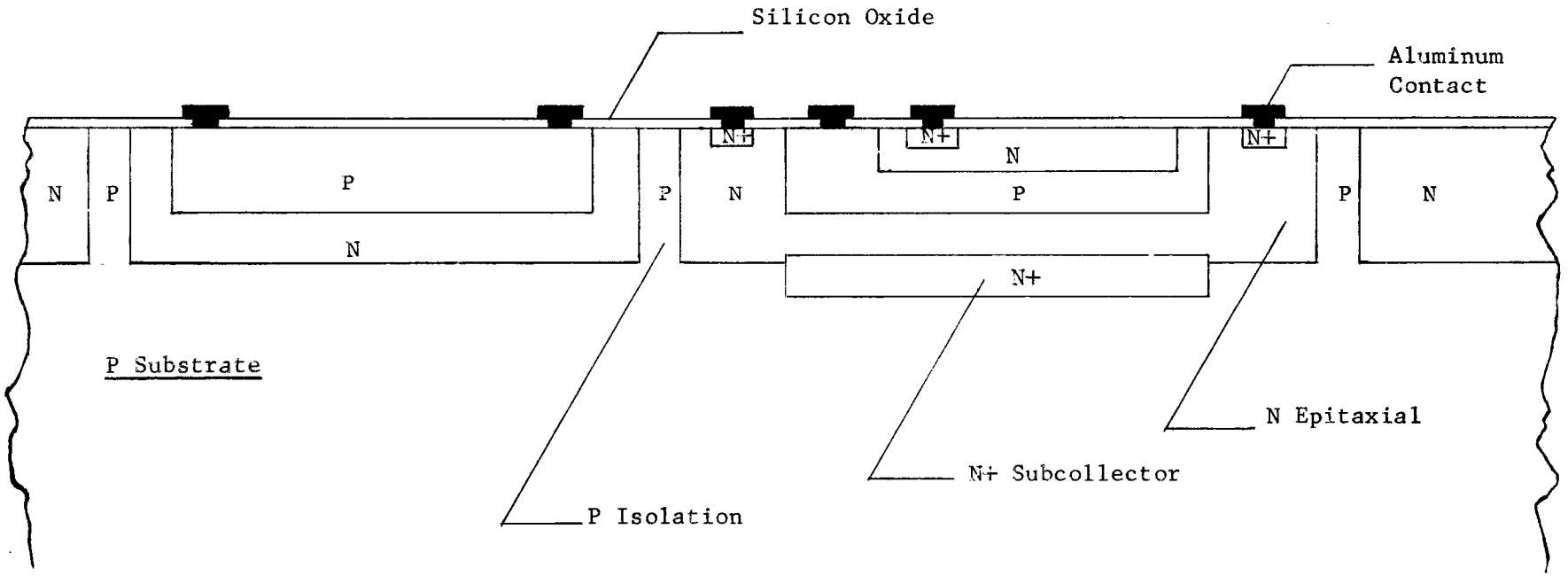
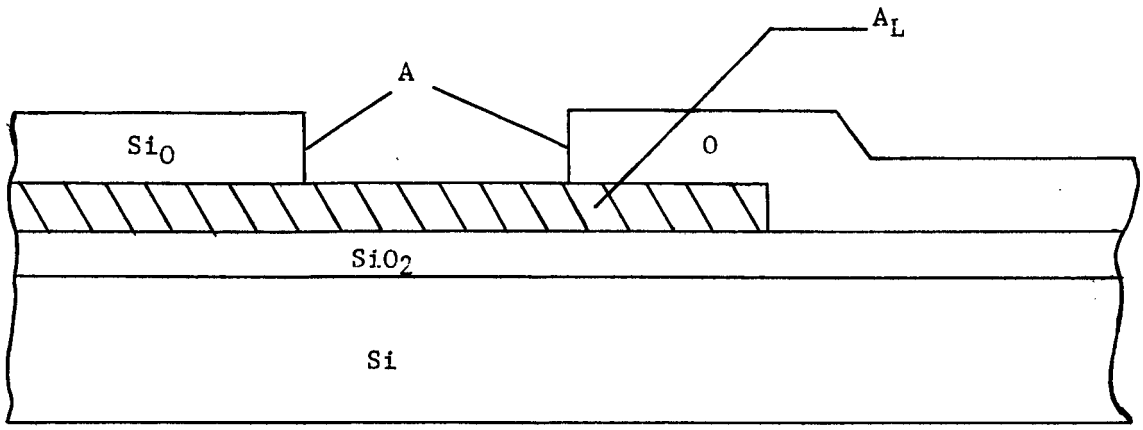
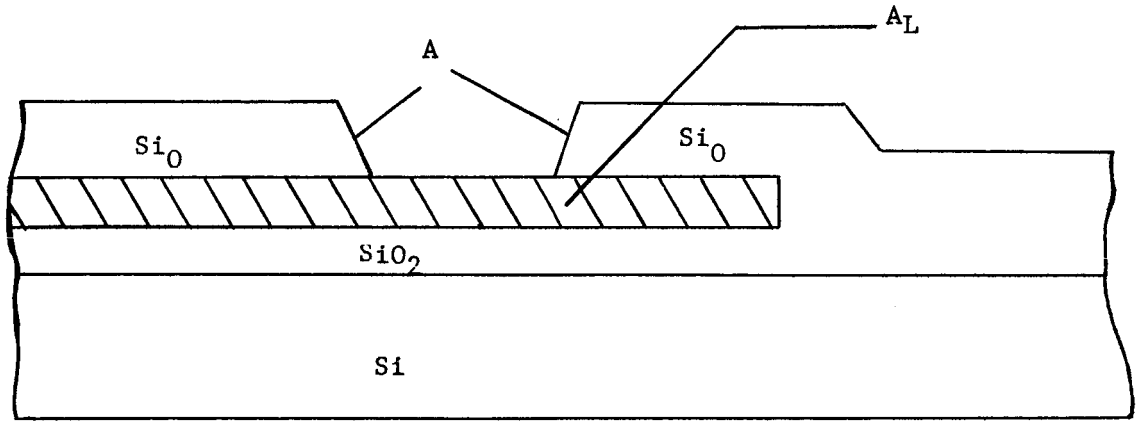


FIGURE 4





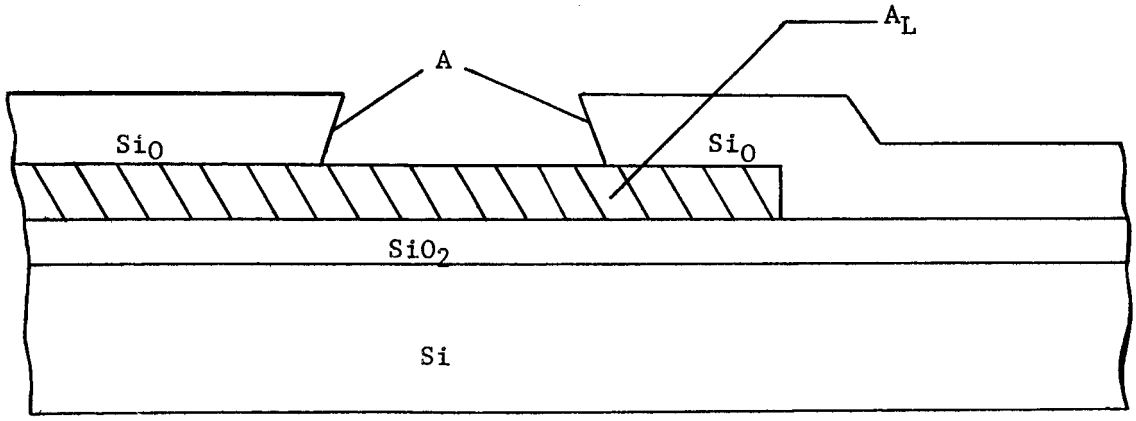
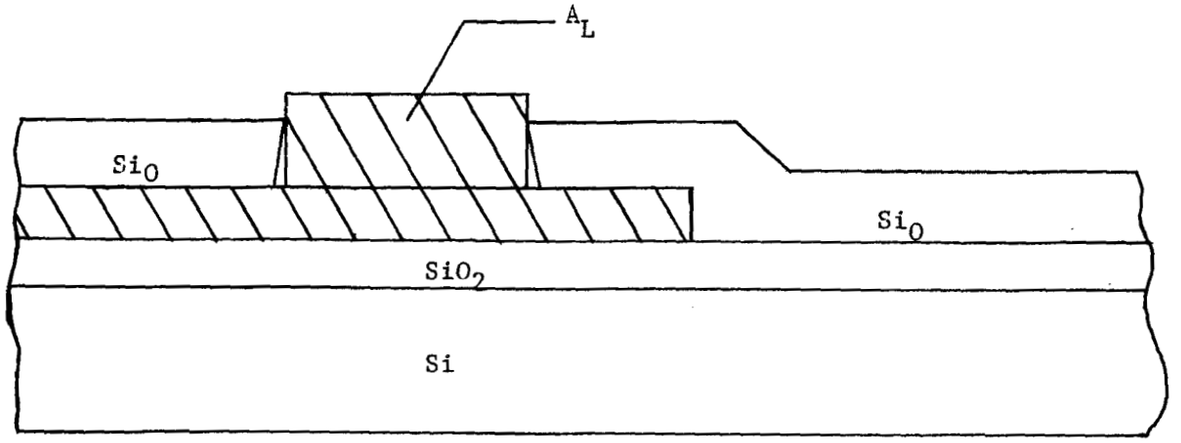


FIGURE 5



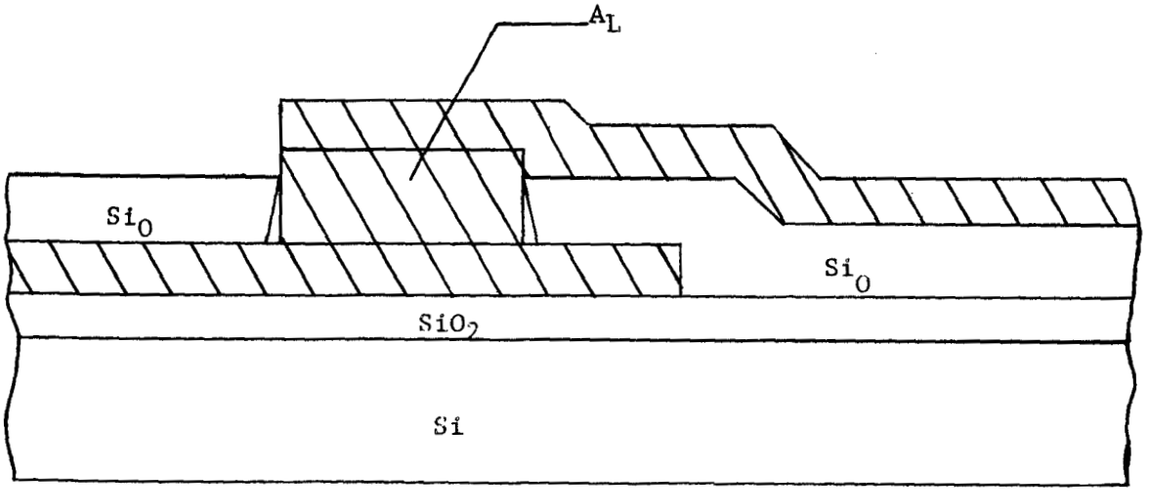


FIGURE 6

DUAL PNP TRANSISTORS

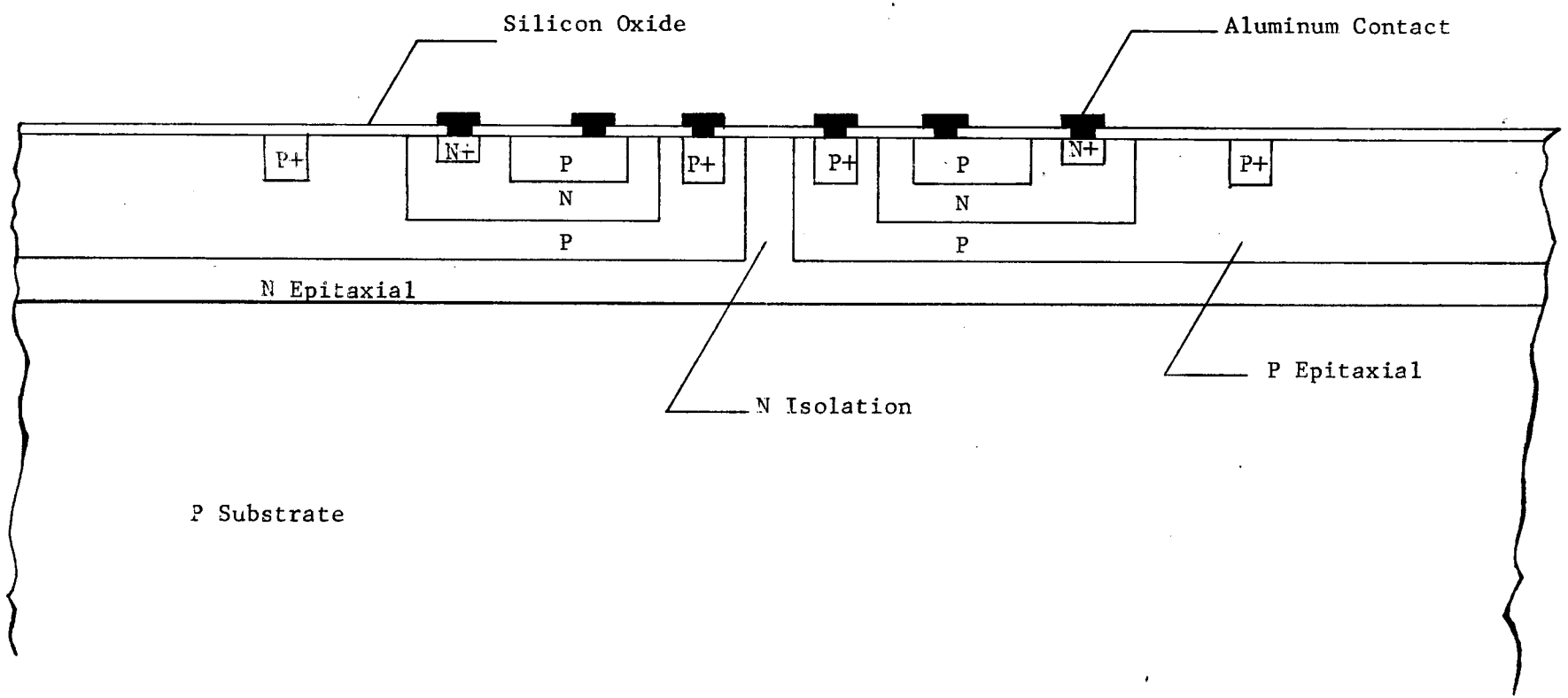


FIGURE 7

PNP STRUCTURE

(DIFFUSED SINGLE EPITAXIAL WITH
COLLECTOR SUB-DEPOSITION)

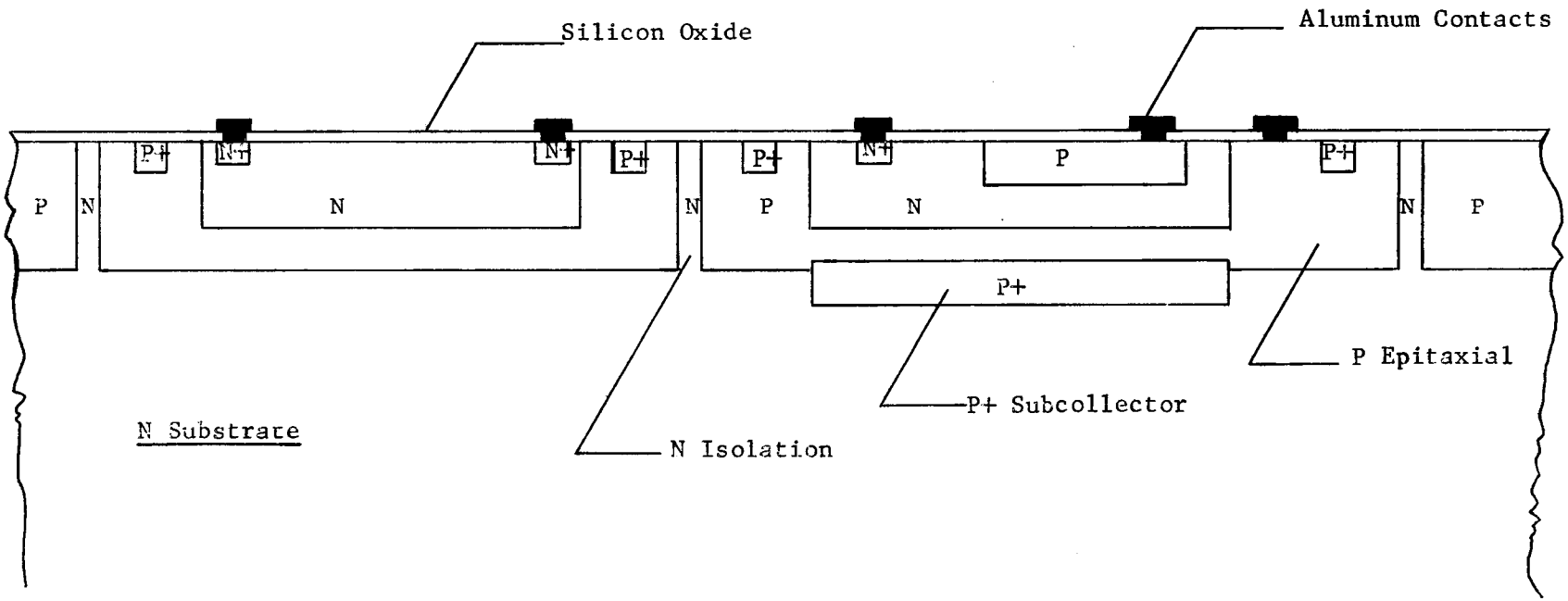
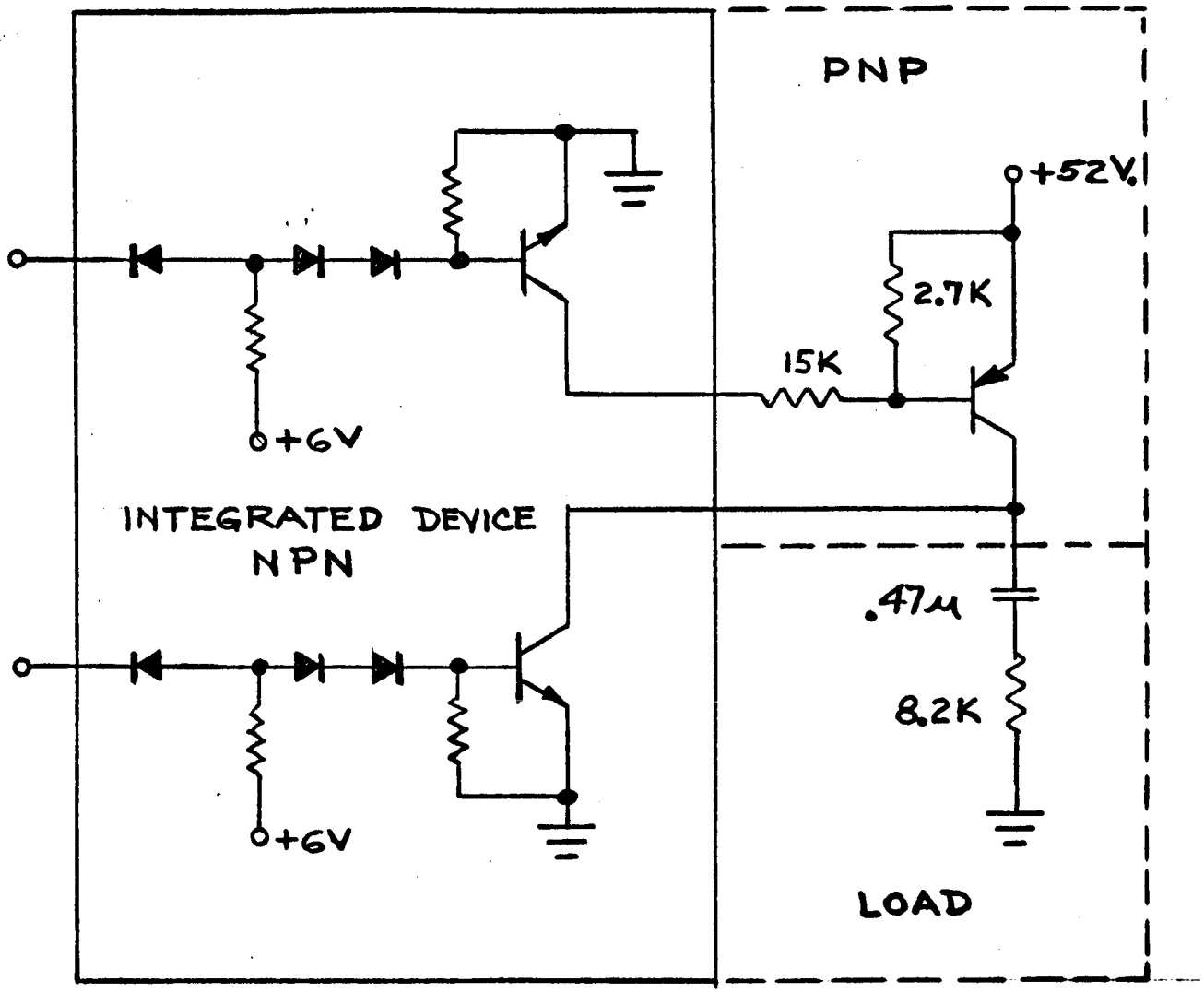


FIGURE 8



CIRCUIT OF NON LINEAR LOAD SWITCH

FIGURE 9