EES SERIES REPORT NO. 11

REPORTS ON

HYBRID - COMPUTER HARDWARE

ENGINEERING EXPERIMENT STATION

COLLEGE OF ENGINEERING

THE UNIVERSITY OF ARIZONA, TUCSON

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Reports on

HYBRID-COMPUTER HARDWARE

Engineering Experiment Station
College of Engineering
The University of Arizona, Tucson

The University of Arizona Analog/ Hybrid Computer Laboratory

by GRANINO A. KORN*

LABORATORY FACILITIES

The Electrical Engineering Department's Analog Computer Laboratory was started in 1958 with an old repetitive computer and a handful of plug-in operational amplifiers. The former was eventually put out of the way, and the latter were assembled into two small but flexible computers complete with homemade removable patchboards. Through the personal kindness of Dr. Arnold Beckman we next received a stack of used EASE components, including thirty old 1048 amplifiers and power supplies. With it and a modern shielded patchbay, a digital readout, and various other hardware bought with State funds, we were able to construct our up-to-date "slow" analog computer, which is still in operation. (However, the 1048 amplifiers are now being replaced with ±100-volt transistor amplifiers.) In 1960, we painted the word "Hybrid" on the laboratory door and were in the digital-logic business for good! ASTRAC I, a digitally-controlled, ±-100-volt iterative differential analyzer, was supported by our department budget alone. APE 1, a miniature ASTRAC developed as a teaching aid in statistics, was an NSF project. The development of our model hybrid-code differential analyzer, to the best of my knowledge the first implementation of Dr. Skramstad's invention, as well as the current ultra-fast, all-solid-state ASTRAC II iterative differential analyzer, are jointly supported by Air Force Office of Scientific Research (AFOSR) and NASA.

Our laboratory is not a computer center; it is mainly concerned with the study and development of computing devices, systems, and techniques. We like to keep our maintenance load as small as possible and will, therefore, keep only our "slow" analog computer, the new fast ASTRAC II, and three small machines. Several other older computers, including ASTRAC I, will be transferred to other electrical engineering laboratories.

*Dr. Korn was presented on page 229 of the April 1965 issue of Simulation.

Figure 1 — The University of Arizona Electrical Engineering School ACL (Analog/hybrid Computer Laboratory)

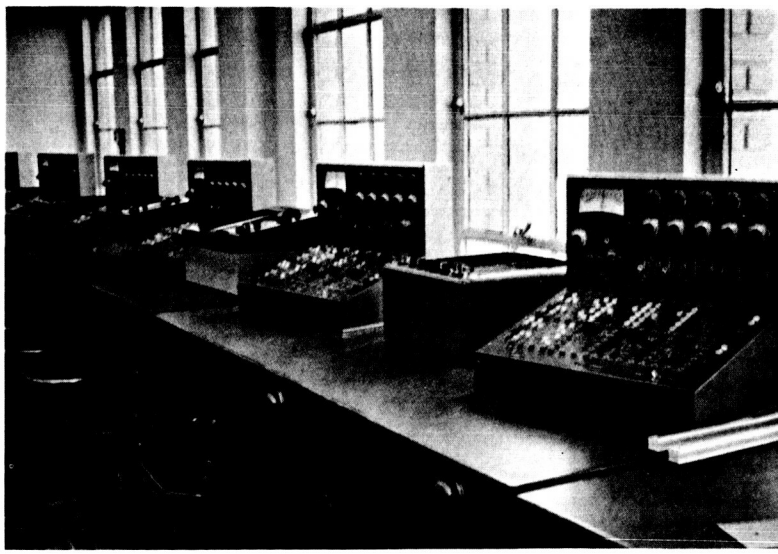

Figure 2 — The University of Arizona Sophomore Analog-computer Laboratory, developed by Professor G. Peterson, has ten ±10v transistor computers, each with 10 amplifiers, 2 multipliers. *All* engineering undergraduates (about 450 per year) take this, plus a course in FORTRAN programming.

Office of Aerospace Research, Information Research Division, Air Force Office of Scientific Research and to the Office of Space Sciences, National Aeronautics and Space Administration for their support of this study under grants AF-AFOSR 89-64 and NASA NSG / 03-002-024.

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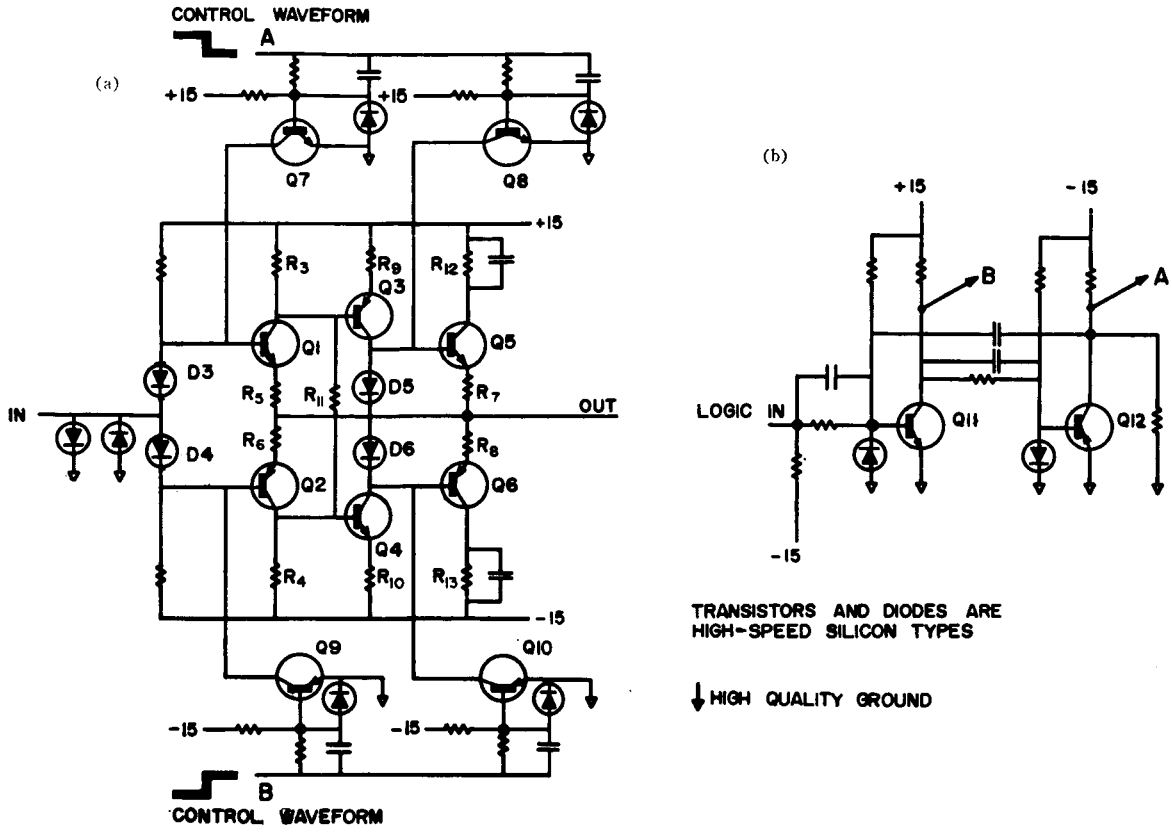


Fig. 3. Electronic switch.

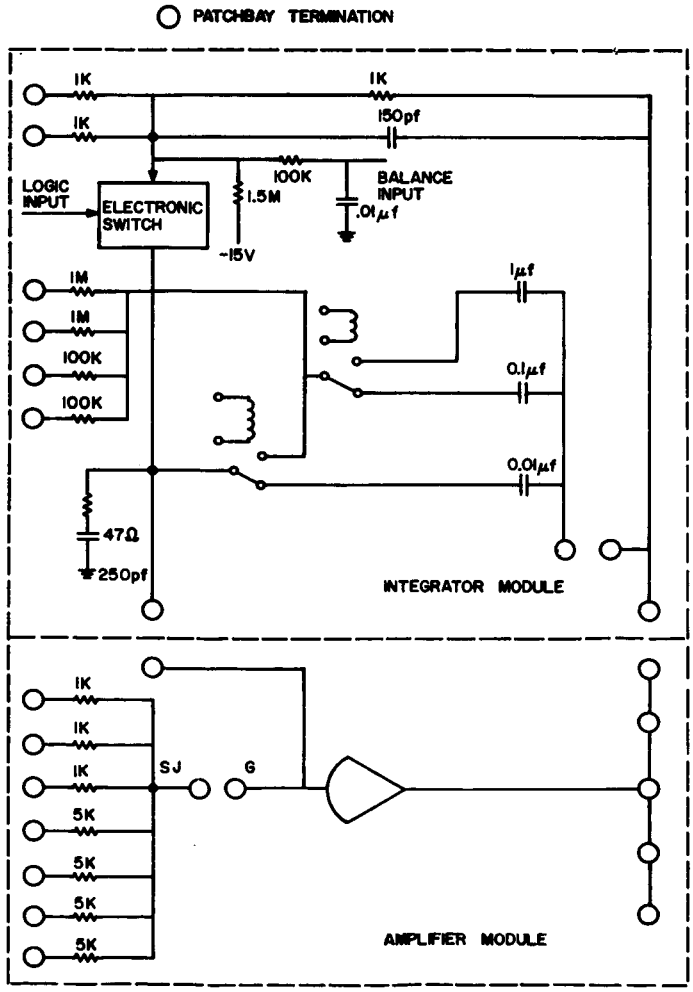


Fig. 4. ASTRAC II amplifier and integrator module circuit diagram.

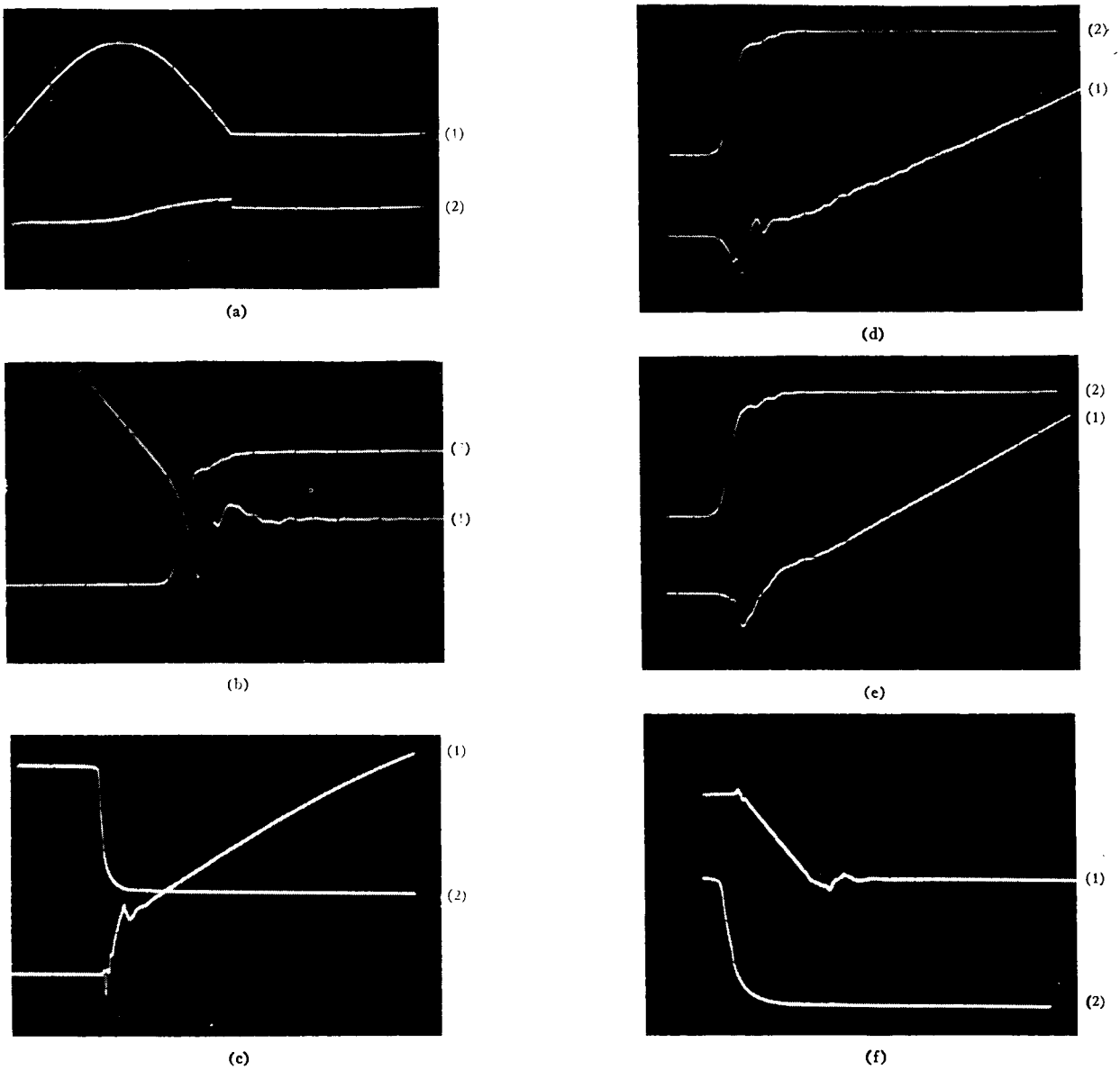


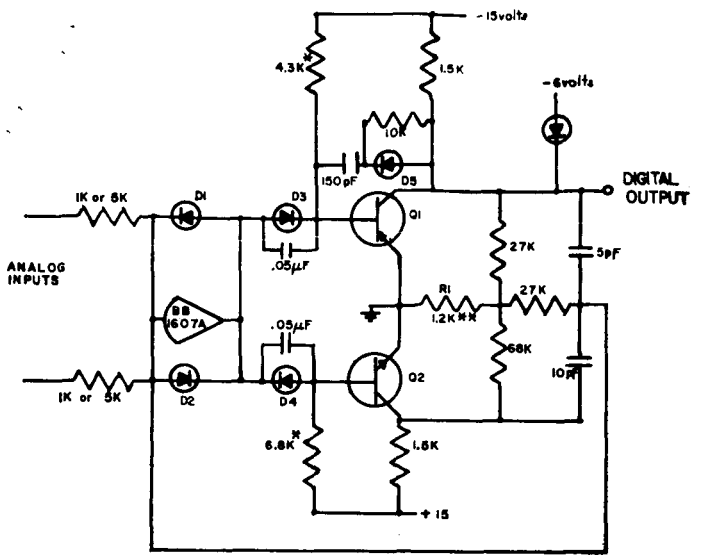
Fig. 5. (a) Sample-hold switching into HOLD. (1) Output X_0: 5 V/cm vs. 10 μs/cm; (2) Summing junction: 50 mV/cm vs. 10 μs/cm. (b) Sample-hold switching into HOLD. (1) Output X_0: 50 mV/cm vs. 100 ns/cm; (2) Switching logic: 2 V/cm vs. 100 ns/cm. (c) Sample-hold switching into TRACK. (1) Output X_0: 2 V/cm vs. 2 μs/cm; (2) Switching logic: 2 V/cm vs. 2 μs/cm. (d) Integrator switching into COMPUTE with 10^5 gain (1-kΩ summing resistor). (1) Output X_0: 200 mV/cm vs. 100 ns/cm; (2) Switching logic: 2 V/cm vs. 100 ns/cm. (e) Integrator switching into COMPUTE with 2×10^4 gain (5-kΩ input). (1) Output X_0: 50 mV/cm vs. 100 ns/cm; (2) Switching logic: 2 V/cm vs. 100 ns/cm. (f) Integrator switching into RESET. (1) Output X_0: 5 V/cm vs. 1 μs/cm. (2) Switching logic: 2 V/cm vs. 1 μs/cm.

a circuit suggested by D. Hamilton and discussed by Downey [5], the primary difference being the additional emitter-follower output stage.

The amplifier is a double-inverting high-gain device with unity negative feedback. The input stage operates as a medium-gain grounded emitter. Diodes D_3 and D_4 supply the proper bias as well as the desired temperature compensation [5], while resistors R_5 and R_6 prevent thermal runaway. The center stage has extremely high gain, which depends on R_9 and R_{10} and the external load as seen through the output follower stage. Diodes D_5 and D_6 supply the desired bias and temperature compensation for the class AB output followers. Resistors R_{12} and R_{13} act as current limiters, while resistors R_7 and R_8 again prevent thermal runaway.

The open-loop voltage gain exceeds 80 dB, with an open-loop output impedance in the order of 2 kΩ. The closed-loop gain is then unity, with an impedance of less than 0.2 ohm. As the open-loop gain of the amplifier decreases with frequency, so does the open-loop output impedance. This causes the closed-loop output impedance to remain at approximately 0.2 ohm over the entire useful bandwidth of the amplifier. To turn the amplifier OFF in the shortest possible time, both the input and output stages are switched directly by switching logic, but the second stage is always kept ON by bias current through R_3, R_4, and R_{11}. The only satisfactory way to switch the input and output stages is to individually control the bases of their four transistors by shorting them to ground in the OFF state of the switch.

The switching logic [Q11 and Q12 in Fig. 3(b)] consists of two overdriven inverting amplifiers with a limited amount of ac regeneration, which drive the four control transistors [Q7 to Q10 in Fig. 3(a)] for the switch. When a digital ZERO (0 volt) is applied to the logic input, transistor Q11 starts to conduct and forces Q12 into its active region; regeneration takes place, and both transistors are turned ON. Transistors Q7 to Q10 are then forced into saturation and turn off the input and output stages of the amplifier. The propagation delays and transition times are very short, since all the switching transistors are turned ON (not OFF), thus taking advantage of their dynamic impedance.



NOTES:
ALL DIODES IN4009
Q1 2N2907
Q2 2N2222
* ADJUST FOR ZERO DELAY
** ADJUST FOR DESIRED HYSTERESIS

Fig. 1. 100-ns regenerative comparator with 0, −6 volt logic level output for hybrid computation. Switching delay is less than 100 ns for all amplitude sine wave inputs down to the hysteresis level, and for all frequencies up to 10 kc/s. The signal ground and case ground are connected together in the amplifier case. The circuit layout is important. With a different layout, the 4.3K and 6.8K resistors may have to be adjusted for zero delay. The amplifier balance control should be adjusted for a symmetrical output square wave when the input is a 100-mV sinewave driving the circuit through a 5K input resistor. The comparator has better tolerance of power supply and ground noise when it is driven through a smaller input resistor (1K); this reduces the hysteresis. The hysteresis in the circuit shown is determined by R_1 and is ±10 mV when the comparator is driven through a 1K input resistor. This is true (static) hysteresis, and not the effect of time delay.

tively long time for the amplifier to integrate this small input and thus to switch to the other limit. The amplifier output waveform during this period is typically parabolic, i.e., the integral of an input which increases approximately linearly with time during the switching period [Fig. 2(a)]. *Also, the resulting switching time depends strongly on the rate of change of the input signal.* With most existing comparators, it is, then, necessary to have a high input-signal rate-of-change, a small input resistor, and a minimum of feedback capacitance in order to achieve rapid switching. However, for ASTRAC II such operation is not fast enough. It was found difficult to achieve less than 1/2-μ switching time (delay time+10 to 90 percent rise time) by this approach with comparator input signals crossing zero less rapidly than 10 sin 20 000π, $a \pm 10$ volts, 10 kc/s sinusoid (200 000π volts per second).

The problem was solved by a regenerative feedbank circuit, which also provides for digital output (0, −6 volts). Referring to Fig. 1, the regenerative feedback must supply a rapidly rising current to the summing junction, to speed the integration. This should occur as

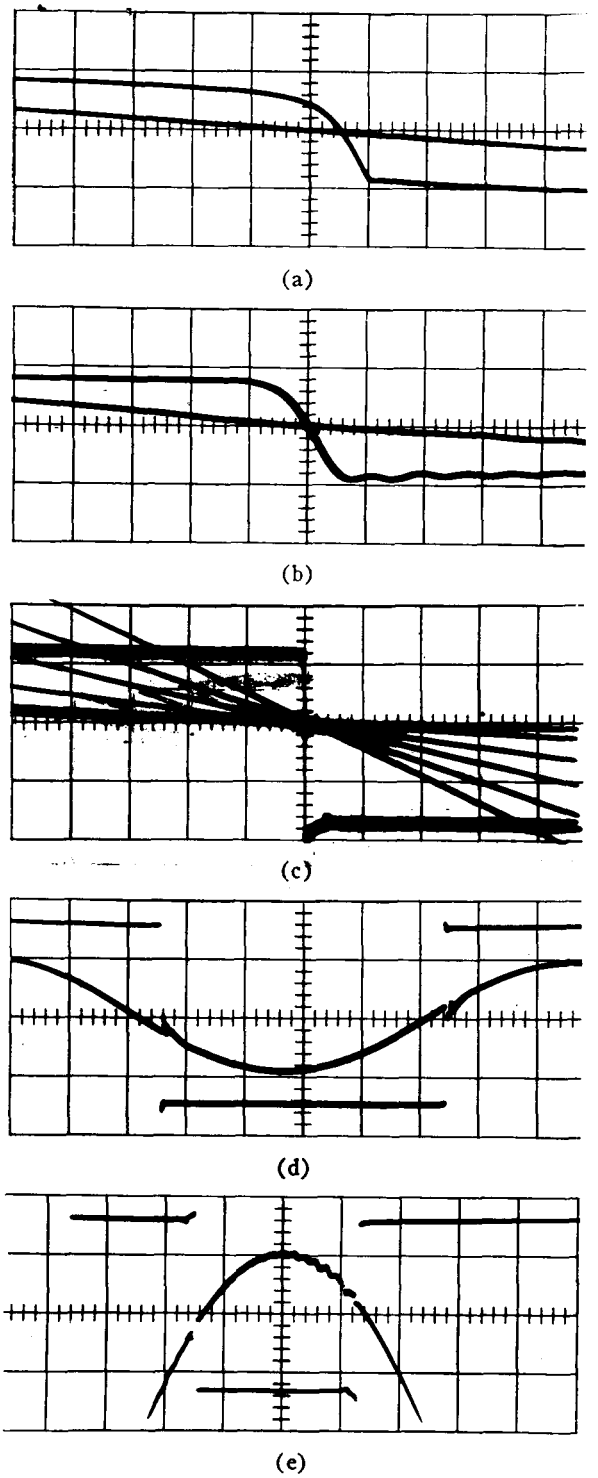


Fig. 2. Oscilloscope photographs of comparator waveforms. (a) Output of a comparator *without* regeneration; the input is a ±1-volt, 10-kc/s sine wave (time scale 1μs/cm, total switching time 1 μs). (b) Output of a comparator *with* regeneration; the input is a ±5-volt, 100-kc/s sinewave. The delay time is adjusted for slight anticipation (see also Fig. 1). Time scale is 20 ns/cm. (c) Multiple exposure shows operation for a 10-kc/s sinewave input at input amplitudes between 0.2 volt and 7.0 volts; note that the switching time is not noticeably affected (time scale is 1μs/cm). (d) Comparator input and output for small (±50 mV) 10 kc/s sinewave input. The comparator was driven through a 1K input resistor and had ±10 mV of static hysteresis, which shows up clearly (time scale, 10μs/cm). Note switching spike induced in the input circuit. (e) Comparator operation with two inputs, one a ±5.05 volt-Kc/s sinewave, and the other a −5.00 volt dc level (time scale, 10 μs/cm; input-amplitude scale 50 mV/cm). The static hysteresis is again evident.

TABLE I

SPECIFICATIONS

Delay time

Less than ±5 ns for a 10-volt, 10-kc/s sine wave driving the comparator through a 5K input resistor.

The delay time is approximately constant for all sine wave amplitudes down to the hysteresis level, and all frequencies less than 10 kc/s, i.e., the observed dynamic hysteresis remains equal to the static hysteresis ±2 mV for all signal rates-of-change from dc to a 10-volt, 10-kc/s sine wave.

The delay time approaches 50 ns on the rising edge for a 10-volt, 100-kc/s sine wave input, but remains approximately zero on the falling edge at this frequency. Above 100-kc/s, an increasing delay time becomes evident on both edges.

Rise times (10 to 90 percent)

50 ns on the rising edge at rated load.
100 ns on the falling edge at rated load.

Drift

The zero-sensing level drifts approximately 25 microvolts per degree centigrade. This is equal to the amplifier drift specification (without chopper stabilization). Chopper stabilization is optional.

Loading

Rated load is 1K and 150 pF of output loading. Much more capacitive loading is possible without significantly affecting the rising edge, but the falling edge is slowed by approximately 50 ns for every 100 pF of output loading.

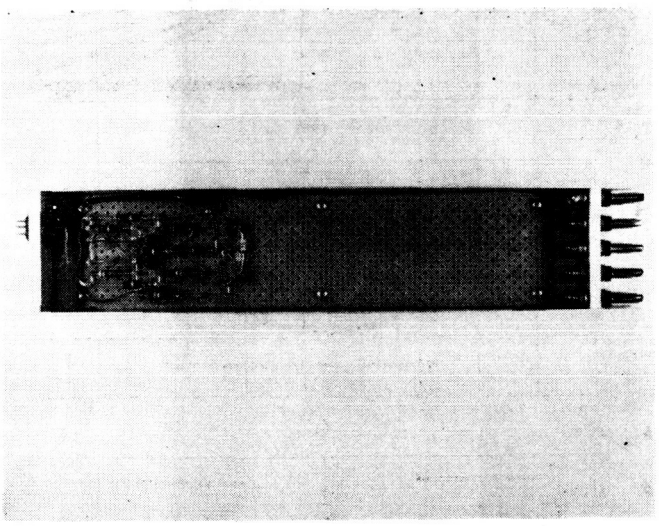


Fig. 3. Photograph of the comparator. The comparator module plugs directly into the back of a standard analog patchbay. The circuit is bottleplugged into the feedback loop of a nearby summing amplifier when comparison is desired. Shielded twinax runs from the circuit to the banna jacks which plug into the patchbay. The digital output is available at the small connector shown at the rear of the module. There is ample room in the module for other analog circuitry.

soon as possible after D_1 starts to turn OFF. Since the amplifier output will have changed by only a few mV at this time, a switched transistor Q_2 is used to supply regeneration; a Schmitt trigger was considered, but can not be switched with the small voltage change at the amplifier output. Referring again to Fig. 1, Q_2 is turned OFF by a small decrease in the output voltage which is coupled through the 0.05 μF capacitor to its base. Q_2 is capacitively coupled to the amplifier summing junction, closing the regenerative loop. The switching time, then, is limited either by the speed of the regenerative loop or by the maximum impulse of current that the amplifier can deliver to charge the feedback capacitance. For this reason, very fast transistors are used in the regenerative loop, and the amplifier must be able to supply high output current (the 1607A can supply over 50 mA for short periods). Once started, the regeneration can cause very fast switching (less than 20 ns). Two transistors permit regeneration in both directions. The comparator is also given a small amount of dc regeneration which provides static hysteresis for noise immunity. This is accomplished by resistive feedback from the transistor collectors (Fig. 1). Degenerative feedback around transistor Q_1 was added to increase the rise time from 10 ns to 50 ns; this increase reduces switching noise in the computer. This degeneration only operates in one direction because of D_5, and does not affect the fall time. The rise time is unaffected by normal loading; it takes 10 000 pF of capacitive loading to slow the rise time by 100 ns. The fall time is 40 ns without load, and 100 ns with 1 kΩ and 150 pF of output loading. Since the output operates directly into digital logic, no Schmitt trigger is required. Comparator latching can be obtained by driving an uncommitted flip-flop in the computer digital logic. Photographs showing comparator switching delay and rise time appear in Fig. 2. Table I gives the measured specifications for the comparator. These were measured *in the computer*, with the comparator constructed in a shielded box that plugs directly into a standard shielded analog-computer patchbay (Fig. 3).

ACKNOWLEDGMENT

The project described in this report is part of a hybrid analog-digital computer study directed by Prof. G. A. Korn.

A Fast Mode-Control Switch for Iterative Differential Analyzers

H. R. ECKES, MEMBER, IEEE

Abstract—**Operation of fast analog-hybrid computers at kilocycle iteration rates requires wideband amplifiers, low computing impedances, and electronic track-hold and integrator mode-control switching within tens of nanoseconds. This paper describes the design and circuit analysis of a new switched-amplifier mode-control circuit designed for the University of Arizona's ASTRAC II iterative differential analyzer. The bandwidth of the circuit in track is down 3 dB at 2.5 Mc, which accounts for a phase shift of 0.005 radian (<0.3 deg) at 10 Kc. The circuits switch into COMPUTE (HOLD) in less than 80 ns; two or more integrators switch within 20 ns of each other. Voltage drift in the TRACK or RESET mode is within ±50 μV/°C between −20 to +60°C.**

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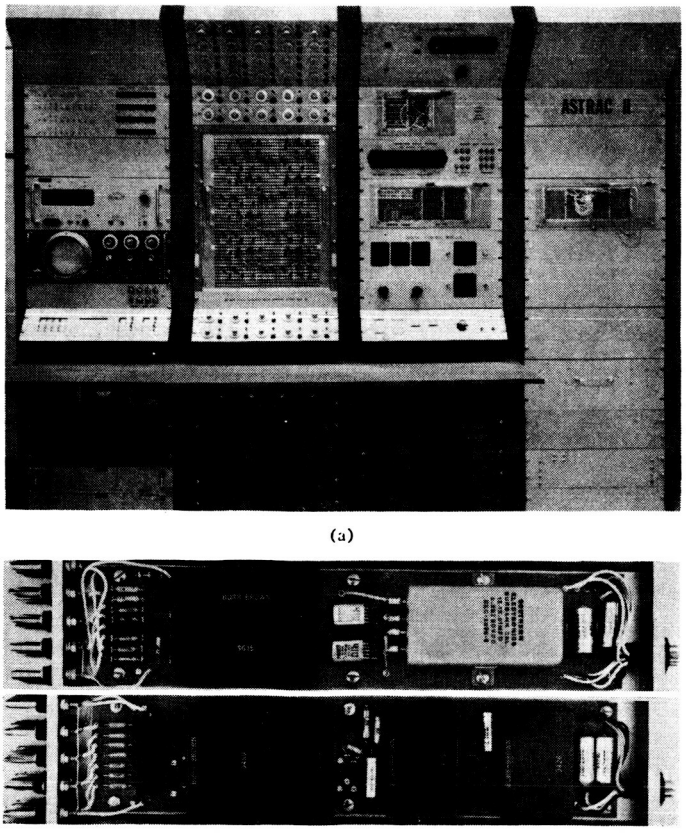
The author is with the Department of Electrical Engineering, University of Arizona, Tucson, Ariz.

Introduction

To exploit the possibilities of fast iterative analog-computer operation in connection with iterative optimization and particularly statistical studies (Monte-Carlo simulation), many modern analog-hybrid computers feature electronic mode-control switches to switch electronic integrators into COMPUTE, RESET, and HOLD, so that substantially increased computing speeds are made possible [1]. While some commercial analog-hybrid computers can furnish reset pulses at iteration rates up to 1 kc, actual computation at such speeds is commonly so inaccurate as to be impractical. The University of Arizona ASTRAC II [Fig. 1(a)] project represents, perhaps, the first successful attempt at iterative computation at 1-kc iteration rates with realistic accuracy. To appreciate the technical problems inherent in such an attempt at fast computation, consider the following requirements:

1) To obtain a dynamic error (phase-shift error) of 0.1 percent at 10 kc in an ordinary phase inverting amplifier, the amplifier-gain-bandwidth product must be of the order of 20 Mc; i.e., phase-inverter response will be 3 dB down at about 10 Mc.
2) To prevent dynamic errors due to spurious distributed capacitances, computing resistors (summing resistors in summing amplifiers and integrators) should not exceed 5 K [2], [3]. With such low computing impedances, fast computers will require low-voltage-high-current opertation with a voltage range not larger than ±20 volts.
3) Since a 20-volt peak-to-peak 10-kc sine wave implies voltage rates of change as high as $2\pi \times 10^5$ volts per second, readout accuracy within 0.2 percent requires mode control and readout (sample-hold) switch timing within 30 ns.



(a)

(b)

Fig. 1. (a) ASTRAC II. (b) ASTRAC II amplifier and integrator modules.

Switch-Circuit Requirements

The ASTRAC II iterative differential analyzer now under development at the University of Arizona satisfies the first two requirements with the aid of ±10-volt transistor feedforward amplifiers having a unity-gain bandwidth of 20 Mc and capable of full output up to 1 Mc. Amplifiers and low-impedance computing networks are mounted in shielded boxes plugged directly into the rear of a standard shielded analog-computer patchbay without any signal wiring whatsoever [Fig. 1(b)].

Measured circle-test data indicate 10-kc dynamic errors within 0.1 percent of half-scale for phase inverters and integrators, and within 0.5 percent of half-scale for quarter-square multipliers. *The most difficult requirement to satisfy is that for accurate mode-control switches which must not only be extraordinarily fast, but which must also work with the 1 K and 5 K computing resistances used in ASTRAC II.* The low computing impedances preclude the use of saturated-transistor switches, whose forward resistances cannot be reduced much below 20 ohms. It is for this reason that the ASTRAC II mode control employs *switched feedback amplifiers* whose output impedances can be reduced below 0.2 ohm. While a fast switch built on this principle is relatively elaborate and expensive, a single switch suffices for each integrator, and the same switch-integrator circuit is useful for both integration and track-hold operation (Fig. 2).

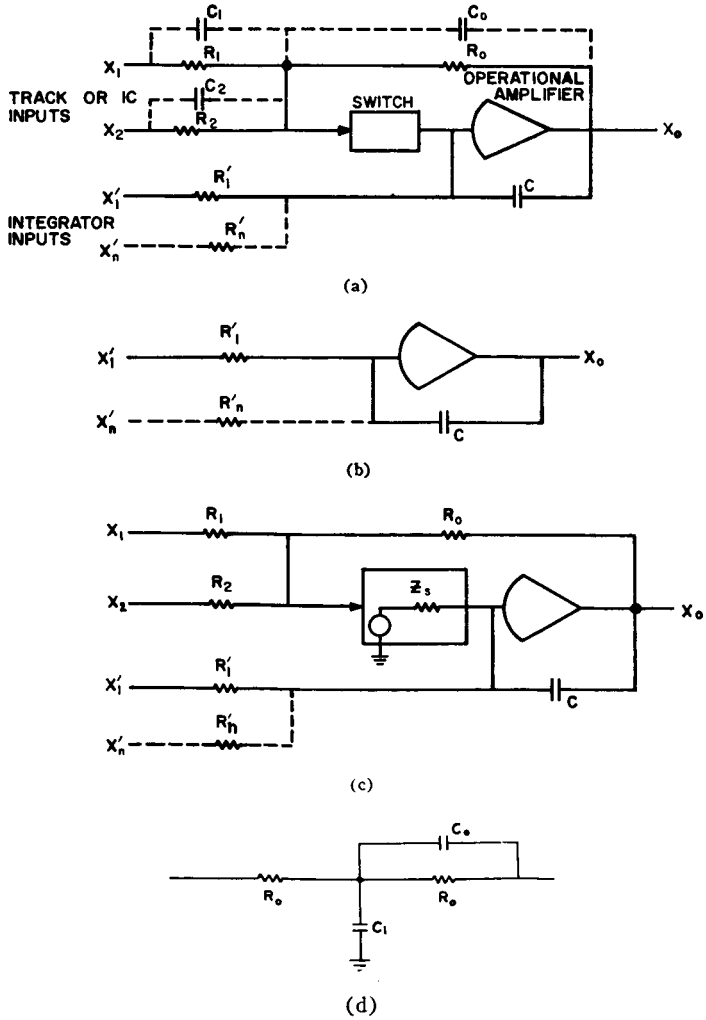


Fig. 2. (a) Switched-integrator or track-hold circuit. (b) Equivalent circuit in HOLD or COMPUTE. (c) Equivalent circuit in TRACK or RESET. (d) Modified feedback network replacing impedance R_0 of (a).

Since the same circuit is used for both integration and track-hold, the switch time delays going into COMPUTE and HOLD will be very nearly the same. It is the *difference* in these delays which determines the timing error. Switching time from HOLD to TRACK is not critical, for it is only necessary to allow sufficient time for the holding capacitor to charge to the voltage on the TRACK or IC inputs. Another advantage is that switching is accomplished at the summing junction of the operational amplifier. This allows the input of the electronic switch to be limited to below one volt, so that fast low-voltage switching logic can be used.

Figure 2 illustrates the operation of the switch. In HOLD, or COMPUTE [Fig. 2(b)], the switched input circuit is effectively out of the picture, and the circuit holds the voltage on capacitance C when the integrator input resistors are not used, or integrates the integrator inputs.

In TRACK or RESET [Fig. 2(c)], actually both track and integrator inputs are effective. *But if the internal impedance Z_s of the switch is small compared to the integrator input resistors, then the current from the switch is so much larger than that from the integrator input that it alone determines the output* X_0 [4]. If an integrator input of 10 volts is to contribute less than 10-mV error in RESET, we must have

$$\frac{Z_s}{R_1'} < \alpha \times 10^{-3}\left(1+\frac{R_0}{Z_1}\right)^{-1} \tag{1}$$

where α is the voltage gain of the switch and Z_1 is the parallel combination of R_1 and R_2 [Fig. 2(c)]. In ASTRAC II, the smallest computing resistance is 1 kΩ, but, to allow for parallelled integrator inputs, we require

$$Z_s < 0.25 \text{ ohm.}$$

This can only be obtained with a switched amplifier employing feedback to reduce Z_s.

Referring again to Fig. 2(a), the size of the storage capacitance C is determined by two conflicting requirements:

1) Input errors due to voltage and current offset integration and switching spikes decrease with increasing C.
2) The small-signal frequency-response in TRACK and also the maximum voltage rate of change in TRACK improve as C decreases.

Resistors R_0 and R_1 should be below 5 K to minimize stray-capacitance effects. Capacitor C_0 is required to decrease the amplitude peaking in TRACK, which is due to phase lag within the feedback loop; the system might actually become unstable if C_0 is omitted. When small values of R_0 and R_1 are used, C_1 is usually not required.

The circuit of Fig. 2(d), suggested by R. Whigham, can be used to replace the feedback impedance R_0 of Fig. 2(a) to decrease the dynamic tracking error at the higher computing frequencies.

When an integrator is used for track-hold, the impedance Z_1' to ground associated with the integrator input resistors $R_1' \cdots R_n'$ in Fig. 2(a) should remain open ($Z_1' = \infty$), since the integrator output offset voltage in HOLD is given by [2]

$$e_d \approx -E_d - \frac{1}{Z_1'C}\int_0^t E_d dt - \frac{1}{C}\int_0^t (i_d + i_s)dt \tag{2}$$

where E_d and i_d are the operational amplifier input offset voltage and current, while i_s is the OFF output leakage current of the switched amplifier.

The Switched Amplifier Circuit

The switched amplifier is a high-current gain/unity-voltage gain circuit which is switched from the active state to the off state.

The amplifier portion (Q1 to Q6) of Fig. 3(a) is the outgrowth of

A Fast Analog Comparison for Hybrid Computation

ROBERT H. WHIGHAM

Abstract—**This paper describes the design of a new exceptionally fast analog comparator with digital output for hybrid computation. A wide-band dc amplifier with regenerative feedback permits high-speed comparator operation within 100 ns of zero crossing for all input rates of change between zero and 5×10^6 volts/second. Static hysteresis between ±10 mV and ±40 mV improves noise immunity. Drift is less than 25 microvolts per degree centigrade without chopper stabilization, which is optional. A simple two-transistor circuit provides both the regeneration and the digital output.**

AN ANALOG COMPARATOR supplies one of two output-voltage levels (digital output) in accordance with the sign of an analog input voltage, or a sum of such input voltages. Analog comparators are the basic analog-to-digital converters in hybrid computers. Such comparators have two somewhat distinct types of applications in modern iterative differential analyzers. One is to change the computer program *between* analog-computation runs or iterations, and the other is to change the computer program *during* an analog-computation period. In the first type of application the comparator is driven, directly or indirectly, by the output of a sample-hold unit and need not be fast, but in the second application the switching takes place while signals are rapidly changing and must be very fast indeed if appreciable errors are to be avoided. For example, the absolute error caused by a time delay Δt in a sinusoid of frequency f is

$$|E| < |100 \sin(2\pi f \Delta t)| \approx 200\pi f \Delta t \text{ percent.}$$

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The author is with the Analog-Hybrid Computer Lab., University of Arizona, Tucson.

If the maximum frequency of the signal is assumed to be equal to 16 times the iteration frequency f_I of the computer, and if the switching delay Δt is 100 ns or 10^{-7} seconds, the error is

$$|E| \approx 200\pi(16f_I)10^{-7} = 10^{-3}f_I \text{ percent.}$$

The error at an iteration frequency of 100/second is, then, 0.1 percent; but at 1000/second, the error is 1.0 percent, which is not tolerable. Thus, a 100 ns switching time is not satisfactory for a 1000/second iteration rate, except for very slow solution signals.

On the other hand, extremely fast switching (10 ns) tends to induce excessive noise spikes in the ground system of the computer. For that reason, 100 ns switching times were considered desirable.

To minimize the switching time in an analog comparator the fastest possible amplifier is required. For this reason the Burr Brown 1607A, used throughout ASTRAC II, was chosen. This ±10-volt amplifier combines low drift (chopper stabilization is available) with a 20-Mc/s, 0-dB bandwidth. Another good choice is the Philbrick type SP456.

In the circuit of Fig. 1, a pair of diodes (D_1, D_2) limit the amplifier output excursion to prevent time delay caused by amplifier overload. When the input signal crosses zero, say from a negative to a positive value, diode D_1, which had been conducting, turns OFF (crosses the knee of its transfer characteristic) when the amplifier output has changed only a little. Now the amplifier, which is loaded by stray capacitance and has several picofarads of feedback capacitance due to the diodes, acts like an analog integrator. We are, then, integrating the comparator input signal, which is still quite small (having just crossed zero). Hence, it may take a rela-

When the input to the switching logic changes to digital ONE (-6 volts), all the switching transistors are turned OFF, which allows the amplifier to function in its operating region. Propagation delays and transition times are longer due to the increased impedance levels; but this poses no problem, since delays going into TRACK (RESET) are not critical. Resistor R_{11} in the circuit of Fig. 3(a) keeps Q_4 and Q_5 from turning off when the amplifier is in the OFF state. This allows smoother transition from the OFF to the ON state of the amplifier.

Circuit Performance

The University of Arizona ASTRAC II [6] uses the mode-switching circuit of Fig. 2 for both integration and analog storage. The circuit employs the Burr-Brown 1607A, a 20-Mc, ± 10-volt operational amplifier, and the electronic switch discussed in the preceding section (developed at Burr-Brown for the University of Arizona). The electronic switch, three integrating capacitors (0.01 μF, 0.1 μF, and 1 μF), a high-impedance summing network for real-time simulation, and relays for automatic time-scale changes are mounted in shielded boxes [Fig. 1(b) and Fig. 4]. These units plug into the back of the patchbay assembly directly above the associated operational amplifier. Each switch or amplifier takes up a 5 by 3 hole front-panel module.

The following dynamic performance data was measured *in the computer*, at the front of the ASTRAC II patchbay. The holding capacitance was 0.01 μF; the output of the operational amplifier was loaded with a 1-kΩ resistor in parallel with a 100-pF capacitor (the assumed standard load for a track-hold circuit). In TRACK, the small-signal frequency response has a 3-dB peak between 1 and 2 Mc and is down 3 dB at just above 2.5 Mc. The phase shift at 10 kc is 0.005 rad (<0.3 deg), which causes a maximum tracking error of 0.5 percent, with a slightly smaller holding error (approximately 0.4 percent). The fact that the holding error is smaller than the tracking error is discussed in the appendix of Eckes [7]. In TRACK, rated output of ± 10 volts is obtained up to approximately 50 kc before the electronic switch causes current limiting. The circuit switches into COMPUTE (HOLD) in less than 80 ns; *two or more integrators switch within 20 ns of one another.*

When the feedback network R_0 of Fig. 2(a) was replaced by the circuit shown in Fig. 2(d) the dynamic performance in the TRACK mode was improved by a factor of two up to 10 kc. The values of C_0 and C_1 were found to be critical.

The effect of the switched amplifier's input offset voltage and current is externally adjusted to zero; the input offset voltage drift is less than 50 μV/°C, and the input offset current drift is less than 30 nA/°C. The measured output leakage current in the OFF (HOLD or COMPUTE) state is less than 1 nA at 25°C.

Figure 5 shows waveforms of interest. The sample-hold input for the TRACK mode was a ± 10-volt, 10-kc sine wave, while the input in the INTEGRATE mode was approximately -10 volts. Switching spikes going into HOLD (COMPUTE) were reduced by a 47-ohm resistor in series with a 250-pF capacitor from the summing junction to ground.

Acknowledgment

The author wishes to thank H. Koerner of Burr-Brown Research Corporation, Tucson, Ariz., and Prof. G. A. Korn, Department of Electrical Engineering, University of Arizona, Tucson, for their many helpful suggestions.

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Reduction of digital noise in hybrid analog-digital computers

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In a computer system combining fast analog computing elements with digital circuits, the effect of digital-circuit noise on the analog computation is becoming a matter of increasing concern. In a hybrid computer using, say, 5-Mc digital modules, 10- to 30-Mc radio-frequency noise due to the leading and trailing edges of digital pulses, and especially due to ringing in digital circuits, can whistle through the entire computer installation with the greatest of ease.

Since modern analog-computer amplifiers have gain-bandwidth products between 1 and 30 Mc, such radio-frequency noise can be rectified in nonlinear circuit elements and cause dc offsets and can even trigger the faster types of analog comparators, even though such fast noise waveforms are not noticeable on low-frequency oscilloscopes and recorders.

Noise spikes as high as 500 mV are no rarity. Careful attention to the details listed in the following can, however, reduce digital noise (possibly with the exception of switching spikes caused by the analog switches themselves) to peak values below 10 to 50 mV.

If you are fortunate enough to be able to specify a completely new hybrid system, you can benefit from what many of us have found out the hard way: *the usual commercially available digital modules, with their 3- to 12-volt logic levels and large pulse currents, are not really suitable for use in hybrid analog-digital circuits.* What is really wanted is microcircuit logic designed for supply-power conservation in aircraft and space vehicles. Such logic modules generally have only half-volt logic levels and are designed to minimize pulse currents, thereby minimizing radio-frequency radiation at its source. 30-Mc micrologic circuits minimize power-supply current variations and also permit very fast pulse rise and fall times, which gets such rf as is radiated further away from the analog-computer passband. Wherever possible, logic circuits should have a conducting ground plane associated with each circuit card; it would be even better to employ multiple-layer cards, with each power-supply voltage in a complete conducting plane.

With old or new digital logic, the following techniques will help to reduce digital noise.

1. *Reduce digital noise at its source.* This problem is well discussed in reference 1. Avoid transmission-line loading of diode transistor logic; wires from each circuit should fan out, never reach multiple destinations by going on from point to point; you might as well put an antenna on the roof. Terminate long lines carrying digital signals in low impedances. Design digital circuits so that pulse-tops are flat with a minimum of ringing or tilt. Ordinary clamping diodes may not achieve this.

When using digital patchbays, try to control flip-flops with dc reset lines and keep fast clock pulses away from the patchbay as much as possible. Use shielded patchbays if you can afford them.

2. *Grounding and Shielding.* The subject of analog-computer ground systems is treated in references 2 and 3. The essential point is to have not only separate signal-ground, power-ground, digital-ground, relay-ground, and potentiometer-ground returns to a common point but also, in fast hybrid computers, it may be necessary to have separate ground returns from individual potentiometers, switches, and amplifiers. Similarly, analog power-supply voltages may have to go to individual amplifiers from a common large copper bar to avoid common inductive impedances and power-supply busses. Laminated power-supply busses with built-in ground planes may help. Ground and power-supply lines longer than a few inches should be shielded.

Analog and digital components should be in separate shielded enclosures, *with the common ground system somewhere near the boundary of the two.* Analog computing elements should be in individual shielded cans.

A special problem is posed by analog switches and comparators, which usually need both analog and digital ground connections; sometimes the two ground circuits must have a common return. In such cases, the comparator or switch in question should have its ground returned to the computer common-ground point in an individual shielded two-conductor cable, which also contains the digital-signal line. In general, it is best to keep all such circuit elements near the analog patchbay.

3. *Decoupling Filters.* With a reasonably designed ground system, the most important noise-reduction measure is to keep as much of the radio-frequency noise as possible off power-supply and ground lines and to keep the remainder out of the analog computing elements. For this reason, *every digital circuit card and every analog computing element should have a decoupling filter on each power-supply line.* Such a decoupling filter should consist of a radio-frequency choke (of the order of 100 mH in series, plus a shunt capacitor to power ground). Most present-day computing elements already have the capacitors, but lack the series chokes. Electrolytic shunt capacitors designed for decoupling at signal frequencies must be paralleled by noninductive mica or ceramic capacitors for proper radio-frequency bypassing. In addition, it may be useful to operate analog and digital power supplies from two different phases of the power line, and to place all 60-cycle ac lines in conduits, with commercial radio-frequency interference filters ahead of the dc power supplies.

Where lines to relays, such as mode-control of time-scale relays operated by digital circuits, enter the analog computer, each relay line should have an LC decoupling filter, so that no radio-frequency signals can enter the analog computer by way of the relay lines.

ACKNOWLEDGMENT

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A HYBRID-CODE DIFFERENTIAL ANALYZER *

by Emmett Pearse O'GRADY **

ABSTRACT. — In a hybrid-code differential analyzer system, variables and parameters are represented by the combination of a coarse n-bit number and a continuously variable analog interpolation voltage. The hybrid-code system combines analog elements accurate to within p per cent of half-scale with the n-bit digital system to form an overall system with greatly improved accuracy within $(p/2^n)$ per cent of half-scale. This paper describes a hybrid-code system employing a 5-bit-plus-sign number and an analog channel accurate to within one per cent of analog half-scale. Results of the sine-loop test verify that the predicted theoretical performance is achieved in practice. Further experiments study the performance of the hybrid-code system with a passive RC integrator replacing the active integrator in the analog channel of the hybrid-code integrator. Results of the sine-loop test indicate that sufficient accuracy for practical applications cannot be achieved with a realizable passive RC integrator.

Introduction.

Considerable interest is being shown in the development of hybrid and combined diffrential analyzers which capitalize on the best features of both analog and digital computing elements. Hybrid systems often provide an analog computer with digital storage and decision-making capability. Combined systems utilize a digital computer for operations such as coordinate transformations, precision function generation, and data storage, which are best suited to digital techniques, and analog elements for operations such as addition and integration, where higher speed and less accuracy are permissible.

This paper treats a differential analyzer employing hybrid-code representation of variables ; that is, each variable or parameter is represented by a combination of a coarse n-bit word and a continuously variable analog interpolation voltage. Accuracy depends on the number of bits used and on the analog-element accuracy. The system described employs a 5-bit word.

The experiments described here study two aspects of hybrid-code computing. First, they verify that hybrid-code techniques provide a method for combining a digital system with n bits and an analog system accurate within only p per cent of half-scale to obtain an overall hybrid-code system with greatly improved accuracy of $(p/2^n)$ per cent of half-scale. While such verification has been obtained for a system with $n = 3$, a more practical system requires five or more bits. This study provides a convincing verification of hybrid-code accuracy.

Second, it was suggested by previous investigators [1, 2] that if the number of bits is increased, a relatively accurate hybrid system can be maintained with simple passive elements replacing operational amplifiers in the analog channel. A system with 5 bits permits a comparison of results obtained using a passive RC integrator and those obtained using an active integrator. The passive-integrator tests determine how well accuracy can be maintained when the active analog integrator is replaced by a realisable RC integrator.

Earlier work in the area of hybrid-code systems has been carried out by H. Skramstad, H. Schmid, J. Wait, and others [1-8]. Wait's prototype system, based on a modification of Skramstad's original proposal, was the first complete operational unit. It employed a 3-bit word and an analog channel with nominal accuracy of 1 per cent of half-scale to achieve over-all hybrid-code accuracy within 0.125 per cent of half-scale.

Hybrid-code theory [1-5].

General Theory : In a hybrid-code system a variable X is represented in the form

$$X = X_D + X_A ,$$

where X_D is an n-bit-plus-sign number, and X_A is a continuously variable analog interpolation voltage between $-E$ and $+E$ volts. Either one bit or E volts represents one machine unit (m.u.). The variable X can be considered as a binary number, in which X_D contains the n most significant bits, and X_A represents the remaining less significant bits. In the computer to be described, X_D is a 5-bit plus sign number, and E equals 10 volts. Digital parts of variables are represented in a 2's complement code. The hybrid-code representation is illustrated in figure 1.

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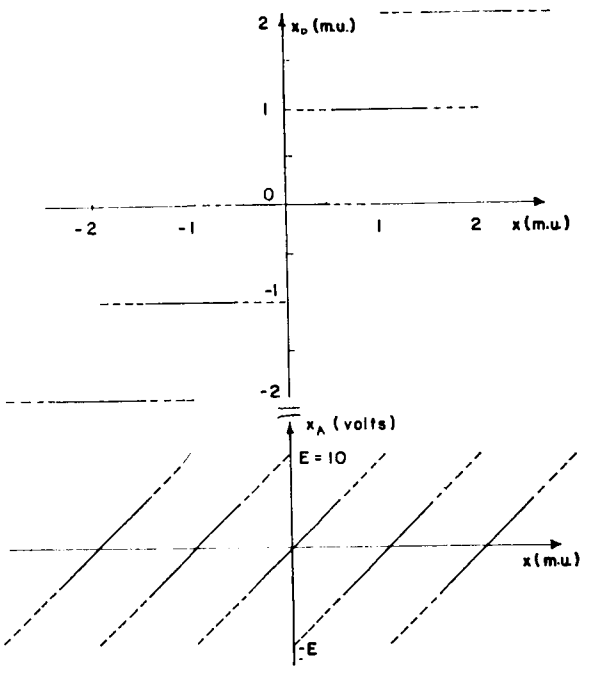


Fig. 1. — Hybrid-code representation of variables.
The value of the variable X (for $|X| < 3$ m.u.) is given by the sum, $X = X_D + X_A$, of the variables shown above. Note that there are two equivalent representations of each value of X. For example, $X = 1.6$ m.u. is given by the sum of $X_D = 1$ m.u. and $X_A = 6.0$ volts or by the sum of $X_D = 2$ m.u. and $X_A = -4.0$ volts. In the system described the range of X is given by $|X| < 32$ m.u.

The independent variable, t, is divided into a sequence of COMPUTE and HOLD periods as illustrated in figure 2. Each COMPUTE period is T seconds long ; each HOLD period is T_H seconds. During COMPUTE periods the digital part of each variable is held constant, and computation is performed by analog elements such as integrators and D/A multipliers. At the end of each COMPUTE period, the analog part of each variable is monitored. If its magnitude exceeds 1/2 m.u. (5 volts), a ± 1 m.u. increment (carry) is added to the digital part of the variable and subtracted from the analog part during the ensuing HOLD period. Note that analog computation is performed during COMPUTE periods, and digital computation, which takes the form of updating digital registers, is performed during HOLD periods.

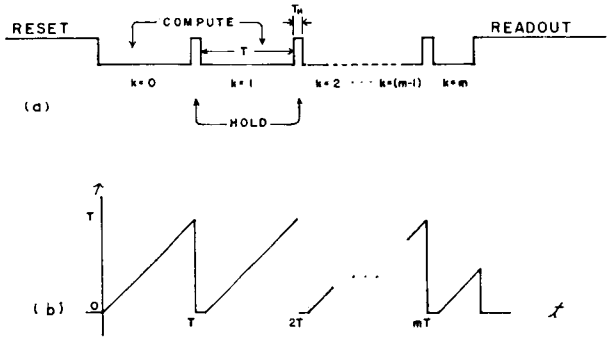


Fig. 2. — (a) Modes of the system during a computation (computing run), and (b) representation of the independent variable, t.

In the RESET state, initial conditions are applied to integrators. During each COMPUTE period analog computation is performed. During each HOLD period digital updating is performed. The READOUT state occurs after a preset number $(m + \tau/T)$ of COMPUTE-HOLD periods. At this time, the value of the readout variable is held and displayed. Note that $T \gg T_H$.

The computer has two additional states (modes), RESET and READ OUT. In the RESET mode, variables are set to zero ; then initial conditions are applied to integrators. READ OUT occurs after a preset number of COMPUTE-HOLD periods ; at that time the digital and analog parts of a selected variable are displayed by a read out system.

Variables are subject to the following scaling restrictions :

$$|\dot{X}| , |X| < 2^n \text{ m.u.} \qquad (1)$$

$$|d\dot{X}/dt| , |dX/dt| \leqslant \left(\frac{1}{2T}\right) \text{m.u. sec}^{-1}. \qquad (2)$$

The first resctriction insures that digital registers do not overflow; the second restriction insures that the digital part of each variable can change by only 1 m.u. after any COMPUTE period and that the magnitude of the analog part of each variable remains less than E volts. This permits a simple form of ternary data transfer.

These restrictions determine the hybrid bandwidth. Assuming a full-scale sine wave,

$$X = 2^n \sin (2\pi B_H t) .$$

Then,

$$\dot{X} = 2^n (2\pi B_H) \cos (2\pi B_H t) ,$$

also,

$$\dot{X} \leqslant (1/2T) \text{ m.u. sec}^{-1}.$$

Thus,

$$B_H = \frac{1}{4\pi 2^n T} .$$

We call B_H the full-scale bandwidth of the hybrid-code system. Since the analog channel accepts the full rate of change, $(1/2T)$ m.u. sec.$^{-1}$, the analog elements must have a bandwidth, B_A, such that

$$B_A \geqslant 2^n B_H = \frac{1}{4\pi T} . \qquad (3)$$

In calculating B_H, the HOLD periods have been neglected : the actual bandwidth is $B_H \left(1 - \frac{T_H}{T + T_H}\right)$ which is about 2.4 cycles per second for this system.

In general, if the analog part of a variable is accurate within p per cent of analog half-scale (1 m.u.), the hybrid-code variable is accurate to $p/2^n$ per cent of hybrid half-scale (2^n m.u.). In effect, the use of hybrid-code techniques increases analog accuracy by a factor 2^n. In terms of a straight digital solution, the use of analog interpolation eliminates truncation and round-off errors due to quantized variables.

Integration Principles : Hybrid-code techniques can be illustrated by a specific example, the hybrid integrator. The following notation is used :

In general	During the k^{th} COMPUTE period
$X = X_D + X_A$	$X_D = {}^kX_D$
$\dot{X} = X_D + \dot{X}_A$	$\dot{X}_D = {}^k\dot{X}_D$
$X_0 = X_{D0} + X_{A0}$	$t = kT + \tau$

A hybrid integrator with gain a performs the operation

$$X\,(mT + \tau) = {}^mX_D + X_A\,(mT + \tau)$$
$$= a \int_0^{mT+\tau} \dot{X}\,dt + X_0$$

where it is assumed that $|\dot{X}|$ and $|X|$ meet the scaling requirements of equation (1). Maximum gain is determined by the scaling restrictions. The change in X during a single COMPUTE period, ΔX, is

$$\Delta X = a \int_{kT}^{kT+T} \dot{X}\,dt \leqslant a\,|\dot{X}|_{max}\,T.$$

To satisfy equation (1),

$$\Delta X \leqslant a\,T\,2^n.$$

To satisfy equation (2),

$$\Delta X \leqslant \tfrac{1}{2}\ \text{m.u in T seconds.}$$

Thus,

$$a\,T\,2^n \leqslant \tfrac{1}{2}$$

and,

$$a \leqslant \frac{1}{2^{n+1}\,T} \qquad (4)$$

The system described uses the maximum gain, 15.625.

Consider integration for a period $(mT + \tau)$ as illustrated in figure 3. We may write :

$$X\,(mT + \tau) = X_{D0} + a \int_0^{mT+\tau} \dot{X}_D\,dt$$
$$+ a \int_0^{mT+\tau} \dot{X}_A\,dt + X_{A0}$$
$$= [X_{D0} + aT \sum_{k=1}^{m-1} {}^k\dot{X}_D]$$
$$+ [a\,{}^m\dot{X}_D\,\tau + a \int_0^{mT+\tau} \dot{X}_A\,dt + X_{A0}]. \qquad (5)$$

To use hybrid-code techniques, we note that if $aT = (\tfrac{1}{2})^i$, the first bracketed expression in (5) is a binary number (X_D) for integral values of i and can be generated and stored with digital precision. The second bracketed expression can be represented by an analog

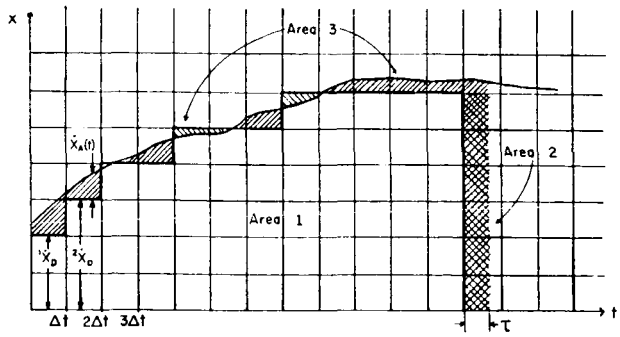


Fig. 3. — Graphical representation of hybrid-code integration (from Wait, Ref. 3).

voltage (X_A). Figure 4 illustrates a hybrid integrator generating the expression (5). Its digital channel includes the n-bit plus sign input ($\dot{X}$) register, the $(n + 2)$-bit plus sign R register, and two D/A multipliers. The analog channel includes an analog inte-

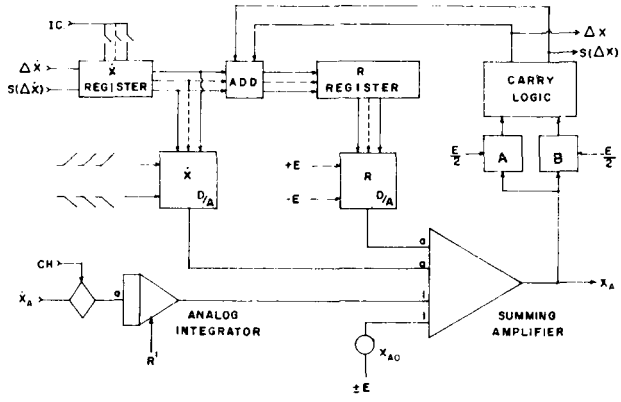


Fig. 4. — Hybrid-code integrator.

grator, the summing amplifier, and the analog initial-condition circuit. Note that the digital part of the hybrid integrator output is accumulated by the input register of the following computing element(s). During a computer run, the integrator performs the following operations in generating expression (5) :

1. At the start of the RESET period digital registers are reset and the analog integrator capacitor is discharged. Then $\dot{X}_{D0}$ and X_{D0} are applied to the $\dot{X}$ and X registers.
2. During a computing run increments in $\dot{X}_D$ are received from the preceding element(s) and accumulated in the $\dot{X}_D$ register.
3. The quantity $R = aT \sum_{k=1}^{m-1} {}^k\dot{X}_D - N$, where N is the sum of the output carries generated in operation 8, is accumulated in the R register. The number ${}^k\dot{X}_D$ is added to the lower order bits at the start of each HOLD period to form the term $aT \sum_{k=1}^{m-1} {}^k\dot{X}_D$.

4. During COMPUTE periods the R D/A multiplier converts the quantity R to a d-c voltage that is a component of X_A.

5. The term $a\,{}^{k}\dot{X}_D\,\tau$ is obtained from a D/A multiplier with output proportional to a linear interpolation voltage (area 2 of figure 3).

6. The term $\int_0^{mT+\tau} \dot{X}_A\,dt$ is the output of the analog integrator (area 3 of figure 3).

7. X_{A0} is the analog part of the initial condition.

8. The terms obtained in operations (4) to (7) are summed to form X_A. Comparators A and B monitor X_A at the end of each COMPUTE period. If $X_A \geqslant 5$ volts, a CARRY is generated adding 1 m.u. to X_D and subtracting 1 m.u. from X_A. Subtraction from X_A is accomplished by subtracting 1 m.u. from the R register. If $X_A \leqslant -5$ volts, 1 m.u. is subtracted from X_D and added to X_A.

An Improved Hybrid-code Differential Analyzer.

The system used in performing tests is an improved version of that described in Ref. 2. It employs a 5-bit-plus-sign word and an analog channel with nominal accuracy of 1 per cent. To study errors occuring in a sine loop two integrators and an inverter are necessary to implement $d^2X/dt^2 = -\omega^2X$. In addition, a master control clock and readout system are required to provide accurate timing of operations and readout of variables.

Digital information is stored in two's complement form. The scaling restrictions mentioned earlier insure that each variable changes by either 0 or ± 1 m.u. during each HOLD period. This permits a simple ternary form of digital information transfer between elements : a pulse on the (ΔX) line indicates that there is an increment, and the dc-level in the S line gives its polarity.

Integrator descriptions : Referring to figure 4, each integrator includes an input ($\dot{X}$) register, an R register, two D/A multipliers, an analog integrator, a summing amplifier, and two comparators. The input register is a 5-bit-plus-sign reversible counter which receives S and ($\Delta\dot{X}$) signals from previous elements. The $\dot{X}_D$ initial condition is set with toggle switches on the front panel and is applied to the $\dot{X}$ register during the RESET period. The R register is a 7-bit-plus-sign register. During each HOLD period the magnitude ${}^{k}\dot{X}_D$ in the $\dot{X}$ register is added to the five least significant bits of the R register, and the two most significant bits are determined by the sign of ${}^{k}\dot{X}_D$, the presence of a carry from the fifth bit, and the presence of a carry at the integrator's output.

The D/A multipliers convert ${}^{k}\dot{X}_D$ and R_D to analog signals during COMPUTE periods. The six bit $\dot{X}$ D/A multiplier is shown in figure 5 ; the eight bit R multiplier is similar. This type of unit is discussed in reference [9]; its accuracy is better than 0.5 per cent of half scale.

The integrator and summer are operational amplifier circuits. Vacuum tube amplifiers were used because they were readily available. In studying the errors introduced by a passive RC integrator the RC network was simulated with an operational amplifier feedback circuit.

The comparators are described in reference [10]. Because carries are generated when X_A exceeds $\frac{1}{2}$ m.u., rather than 1 m.u., it is possible to use a relatively simple comparator accurate to about $\frac{1}{2}$ volt.

Master Control Clock [11] : The master control clock generates precise (0.05 per cent) time intervals $T = 1$ millisecond and $T_H = 0.04$ milliseconds and commands precise readout time. Accurate timing is derived from a 100 kc crystal oscillator. The number of COMPUTE periods is preset with a thumbwheel switch between zero and one thousand periods in steps of one hundredth of a period. Either repetitive or manual (single-run) operation is available. The master clock also generates signals which load digital initial conditions during the RESET period and controls a subroutine clock which sequences digital updating operations during each HOLD period. The subroutine clock generates nine pulses which sequence the addition of ${}^{k}\dot{X}_D$ and, if present, the integrator output carry to the R register of each integrator.

Readout System [12] : The readout system includes a digital register identical to the integrator input register and an analog sample-hold circuit. The digital and

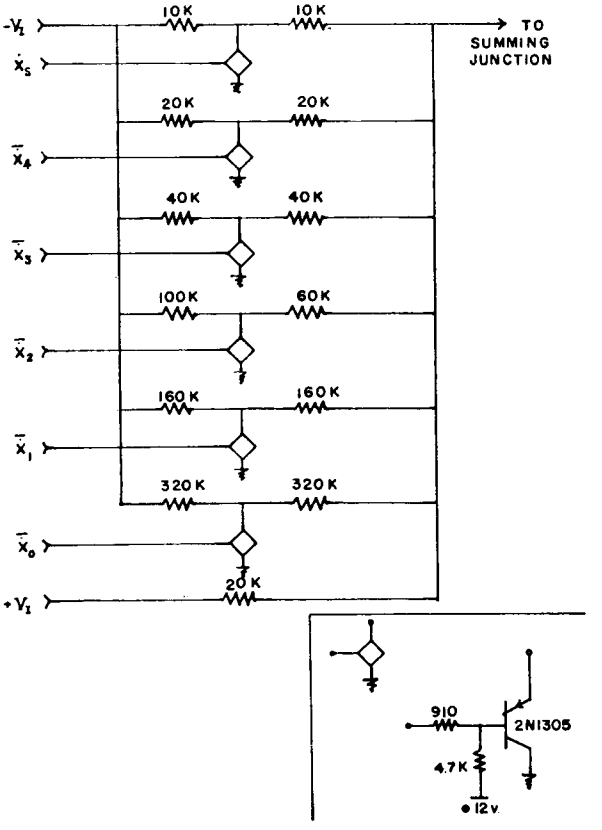
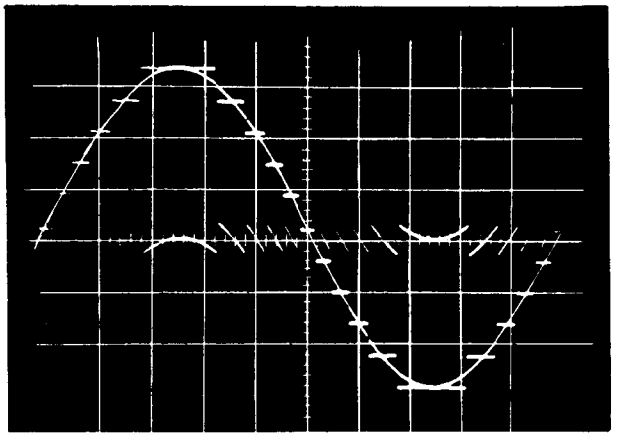
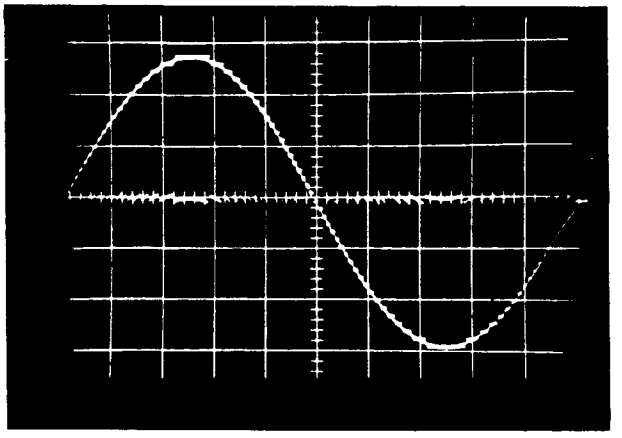


Fig. 5. — 6-bit D/A multiplier.

analog parts of the readout variable are patched to the readout system. The initial digital value is set with toggle switches, and increments are received during the computer run. During computation X_D is displayed by lights on the frontpanel, and X_A is tracked by a fast transistorized sample-hold circuit. At the end of the preset number of COMPUTE periods a readout signal from the master clock places the sample-hold circuit in its hold state, holding the readout value of X_A. The readout value of X_D is held in the digital register and displayed on the frontpanel lights. The readout value of X_A is displayed on a digital voltmeter. The sample-hold circuit is described in reference [13]. It can track a ten volt sine wave with less than 5 degrees phase shift at 4 kc., and can hold within 20 millivolts for $\frac{1}{2}$ second. By changing a switch setting X_D can be converted to an analog voltage and summed with X_A to form the analog signal X for oscilloscope display of the readout variable. This is illustrated in figure 6.



(a)



(b)

Fig. 6. — Photographs showing X, X_D, and X_A for

(a) 5 m.u. sine wave and

(b) 20 m.u. sine wave.

Tests, Results, and Discussion.

To test the system the differential equation

$$\ddot{Y} + \left(\frac{10^3}{64}\right)^2 Y = 0, \quad Y(0) = 30 \text{ m.u.}$$

was solved. The computer setup for this equation is the sine-loop or circle test (fig. 7). It was selected because :

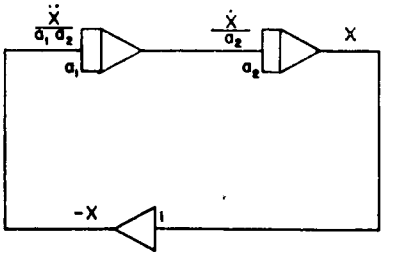


Fig. 7. — Sine loop (circle) test
$a_1 = a_2 = 15.625$.

1. It provides an indication of combined error effects on computer solutions of linear differential equations [5].
2. Earlier results indicate that it is the most stringent test of a hybrid code system [3].
3. Its solution ranges over the full scale of positive and negative values, and the exact analytical solution can be accurately calculated for any time.

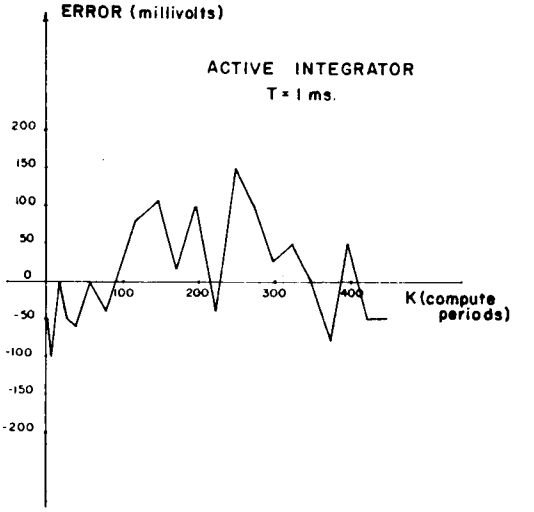


Fig. 8. — Results, employing active analog integrator.

Note that the magnitude of a 30 m.u. sine wave is equivalent to 300 volts.

Results Using Active Analog Integrator : Figure 8 shows the results obtained with a 5-bit digital channel and an operational amplifier analog integrator. The error, the difference in millivots between the hybrid-code solution and the correct solution, in this case 30 sin (k/64) m.u., is plotted against the number of COMPUTE periods. The absolute error is typically less than 100 millivolts (0.032 per cent of half scale). The maximum error is 150 millivolts (0.047 per cent); the

average error and the *rms* error over one cycle of the solution ($k = 400$ periods) are 11 millivolts (0.003 per cent) and 64 millivolts (0.020 per cent) respectively. The sine wave frequency is 2.5 cps.

Discussion : The results compare favorably with those obtained previously by Wait [3] with a 3-bit digital channel and an active analog integrator. His results showed a maximum absolute error of 130 millivolts (0.163 per cent of half scale) and average error and rms error over one cycle of 17.0 millivolts (0.021 per cent) and 61 millivolts (0.076 per cent) respectively. His solution frequency was 8.0 cps, and the COMPUTE period's duration was 1.25 milliseconds.

The results verify the predicted accuracy of $(p/2^n) = (1/32)$ per cent of half-scale. In addition, by shortening the COMPUTE period to 1 millisecond the bandwidth-error quotient has been increased by 20 per cent over previous results. Note, however, that the COMPUTE period cannot be further shortened indefinitively, for switching errors in the integrator and D/A multipliers and phase shift around the sine loop become major sources of error as the period is shortened.

Results Using Passive Analog Integrator : (see fig. A-1) The results obtained with a simulated passive RC integrator seplacing the active integrator are shown in figure 9 for RC time constants of 1, 5, and 10 seconds. The results are shown for approximately one cycle of the solution. As expected, relatively accurate results are obtained with time constants long compared to the solution time ; accuracy decreases as the time constant decreases, and the error increases with time. With a time constant $\tau = 5$ seconds, the maximum error is 250 millivolts (0.078 per cent). With $\tau =$ 1 second, the error is 670 millivolts (0.21 per cent) after 225 COMPUTE periods and 1.1 volt (0.344 per cent) after 400 periods.

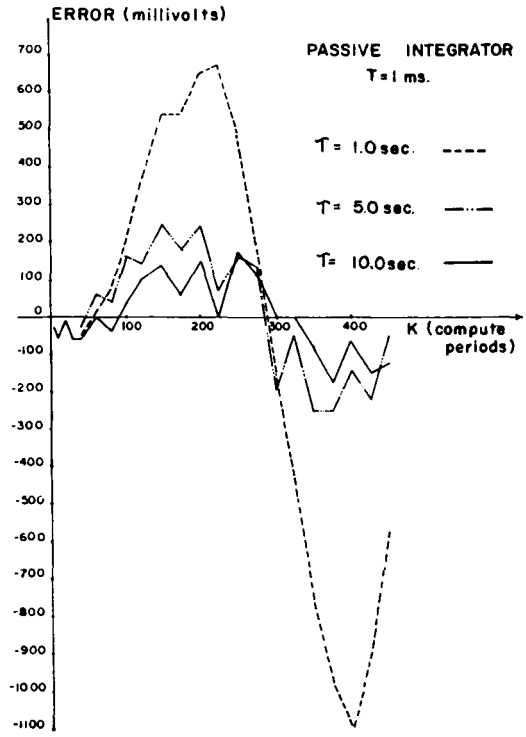


Fig. 9. — Results, employing passive analog integrator.

Discussion : It is not possible to specify the overall hybrid-code accuracy required without knowing the specific nature of the problem being solved. However, for the purpose of discussion, consider the desired analog accuracy to be $p = 8$ per cent of analog half-scale over one cycle of the sinusoidal solution. This corresponds to an accuracy of 0.25 per cent of hybrid half-scale.

In the Appendix, some considerations in the realization of a passive analog integrator for a hybrid code system are considered. It is found that there are practical limitations on the combination of integrator gain and time constant obtainable in practice. In particular, for the system under consideration a realizable passive integrator with the necessary rate-gain has a time constant less than 0.1 second. The passive-integrator tests show that a time constant greater than 1.0 second is necessary to achieve he desired accuracy. Clearly, a 5-bit system with COMPUTE period of 1.0 millisecond and passive analog channel does not provide the desired accuracy.

It is necessary to consider whether the desired accuracy-bandwidth can be achieved through a further increase in the number of bits and/or an increase in the clock rate, thus shortening the COMPUTE period. Increasing the number of bits both increases the accuracy and decreases the bandwidth by the same factor ; the bandwidth/error quotient is unaltered. This means that the passive integrator can have a lower gain but must have a correspondingly longer time constant. This method does not alleviate the realization problem.

The prospect of increasing the clock rate is inviting because, if a given analog accuracy can be maintained, this directly increases the bandwidth/error quotient. However, it requires increasing the analog integrator gain ; and, perhaps more important generally, it increases the bandwidth required in the analog channels. The latter requirement is seen in the need for faster switching in the D/A multipliers and integrator and in phase shift in the summing amplifier due to its distributed capacitance and that of its feedback resistor and the resistive networks of the D/A multipliers. The requirement of higher gain is sufficient to eliminate this as a method for increasing the bandwidth/error quotient of the 5-bit system.

The effect of the timing and phase-shift errors introduced by increasing the clock rate is illustrated in figure 10, which shows the results obtained with the 5-bit system when the COMPUTE period was shortened to 0.25 milliseconds. The analog channel employed the active integrator. The rapid increase of the error clearly indicates the deterioration of the accuracy of the analog channel as a result of increasing the clock rate. The same analog channel which introduces less than 1 per cent analog error with T = 1.0 milliseconds introduces more than 10 per cent error with T = 0.25 milliseconds. These results indicate a general problem faced

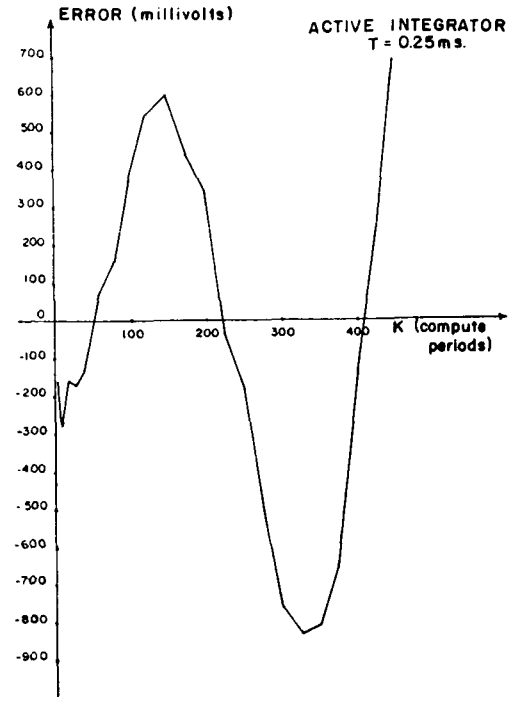


Fig. 10. — Results, employing shorter COMPUTE period.

in attempting to increase the bandwidth/error quotient by increasing the clock rate.

Finally, consider the prospect of both increasing the number of bits and shortening the COMPUTE period. The effect of the former adjustment is to increase the accuracy and decrease the bandwidth, while that of the latter is to increase the bandwidth. One hopes for an overall effect of increasing the accuracy and maintaining or increasing the bandwidth.

As an example, consider an 8-bit system with $T = 50$ microseconds as mentioned in reference [2]. From equation (3) the necessary analog bandwidth is 1.6×10^3 cps. From equation (4) the necessary rate gain is about 40. At this operating frequency the summing amplifier's feedback resistor would have to be of the order of 10 K or smaller to reduce phase shift. The passive integrator tests give a rough estimate of the time constant required to obtain a given accuracy; namely, a time constant longer than about 10 periods of the sine wave is required for 5 per cent accuracy over one cycle of the sine wave. The sine wave period for the 8-bit system is 161 milliseconds, calling for a time constant of about 1 second. It is shown in the Appendix that with 10 K feedback resistor the combination of rate-gain of 40 and time constant of 1 second is not practically realizable.

Conclusions.

The experiments employing the active analog integrator provide a convincing verification of the theoretically predicted accuracy of a hybrid-code system. Using an analog channel with nominal accuracy of 1 per cent of half-scale and a 5-bit plus sign digital channel, the results were well within the predicted accuracy of $(p/2^n)$ per cent (0.031 per cent) of half-scale. This accuracy was obtained while maintaining a full scale hybrid-code bandwidth of 2.5 cps, resulting in a bandwidth/error quotient considerably greater than had been previously obtained.

The experiments employing a simulated passive integrator show that for a 5-bit system sufficient accuracy cannot be achieved with a practically realizable passive analog integrator. Further, in attempting to increase the bandwidth/error quotient by increasing the clock rate (shortening the COMPUTE period), one is faced with the problems of switching errors and limited summing amplifier frequency response. Finally, the results suggest that even for a system with a greater number of bits and a shorter COMPUTE period, a realizable passive analog integrator does not in general provide an admissible combination of accuracy and bandwidth. It is unlikely that a hybrid-code system employing a passive analog channel would provide a bandwidth/error quotient sufficient for practical application.

APPENDIX

Considerations for a Realizable Passive Analog Integrator.

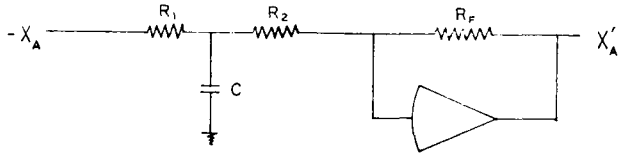


Fig. A-1. — Passive analog integrator and summing amplifier.

A passive integrator and the analog summing amplifier are shown in figure A-1. The transfer function of the combination is given by the expression

$$X'_A/\dot{X}_A = \frac{R_t}{R_1 + R_2} \times \frac{1}{1 + S\,CR_1R_2/(R_1 + R_2)}$$

which has the form

$$X'_A/\dot{X}_A = \alpha \times \frac{1}{1 + S\tau}$$

where (α/τ) is the rate-gain and τ is the time constant of the integrator. The transfer function can also be written in the form

$$X_A/\dot{X}_A = \frac{\alpha}{\tau S}\left[1 - \frac{1}{1 + S\tau}\right] \qquad \text{(A-1)}$$

where the first term on the right hand side of equation (A-1) is the transfer function of an ideal integrator with gain of (α/τ) and the second term represents the error due to the non-idealness of the integrator. For accurate integration τ should be large enough to make the error terme negligible.

The hybrid-code configuration places restrictions on the possible values of the circuit elements. For example, in this system the summing amplifier also

serves as the output stage of two D/A multipliers, both of which require that $R_f = 10$ K. Also, by equation (3), the rate-gain must satisfy the inequality

$$\frac{\alpha}{\tau} \leqslant \frac{1}{2^{n+1}\,T}. \qquad \text{(A-2)}$$

Ordinarily, (α/τ) is chosen so as to satisfy the equality sign ; otherwise extra bits are required in the R register.

Equation (A-2) and the definition of the time constant require that the elements satisfy the expressions

$$\frac{\alpha}{\tau} = \frac{R_f}{CR_1R_2} = \frac{1}{2^{n+1}\,T} \qquad \text{(A-3)}$$

and

$$\tau = \frac{CR_1R_2}{R_1 + R_2}. \qquad \text{(A-4)}$$

By equation (A-3)

$$R_2 = \frac{R_f\,2^{n+1}\,T}{CR_1}$$

By equation (A-4)

$$R_2 = \frac{\tau\,R_1}{CR_1 - \tau}$$

Equating the above expressions, cross-multiplying, and dividing by the coefficient of R_1^2 yield the quadratic equation

$$R_1^2 - \left[\frac{2^{n+1}\,T\,R_f}{\tau}\right] R_1 + \left[\frac{2^{n+1}\,T\,R_f}{C}\right] = 0. \qquad \text{(A-5)}$$

The solution of equation (A-5) for R_1 is

$$R_1 = \frac{1}{2}\left[\frac{2^{n+1}\,T\,R_f}{\tau} \pm \sqrt{\left(\frac{2^{n+1}\,T\,R_f}{\tau}\right)^2 - 4\left(\frac{2^{n+1}\,T\,R_f}{C}\right)}\right].$$

For physical realizability, R_1 must be real valued which requires that

$$\left[\frac{2^{n+1}\,T\,R_f}{\tau}\right]^2 \geqslant 4\left[\frac{2^{n+1}\,T\,R_f}{C}\right]. \qquad \text{(A-6)}$$

For fixed values of n, T, R_f, and τ the inequality (A-6) specifies the minimum value of C for a physically realizable passive integrator.

Table A-1 lists the minimum values of C for a system with $n = 5$ bits, T = 1.0 millisecond, and feedback resistor values of 10 K and 100 K, and time constants of 0.1, 1.0, and 10.0 seconds.

TABLE A-1

Minimum capacitor values for time constants of 0.1, 1.0, 10.0 seconds and feedback resistors of 10 K and 100 K

($n = 5$ bits, T = 1 m sec.)

τ	R_f	
	10 K	100 K
.1	62.5 μf	6.25 μf
1.0	6 250 μf	625 μf
10.0	625 000 μf	62 500 μf

In addition to the restriction due to physical realizability, there are further restrictions if the passive analog channel is to be practically realizable. The most important of these is indicated in reference 3 in the results of tests determining the affect of gain errors in the integrator and in the summing amplifier. The results show that in an open-loop integration using an active analog integrator the solution error introduced by an artifical 10 per cent error in the analog integrator gain buildt up almost linearly with time and exceeds 15 per cent of analog half-scale after only 75 milliseconds. The conclusion to be drawn from these results is that it is necessary to maintain an accurate analog integrator gain, even when using a passive integrator.

Since the integrator gain (rate-gain) is a function of C, it is necessary to use an accurate, stable capacitor in the passive analog integrator. Such capacitors are both bulky and expensive for values greater than 1 microfarad.

In addition $\dot{X}_A$ is the output of a summing amplifier and takes on values as large as 10 volts. Most operational amplifiers deliver a maximum current of less than 50 milliamperes. For an amplifier with limited current capacity, this restricts the minimum value of R_1 that can be supplied with current. For example, an amplifier with 25 milliampere current capacity requires that R_1 exceed 400 ohms. Assuming the minimum value of C, the expression for R_1 is

$$R_1 = \frac{2^n\,T\,R_f}{\tau}.$$

With $n = 5$ bits, T = 1 millisecond, and $R_f = 10$ K, R_1 is given by the equation

$$R_1 = \frac{320}{\tau} \text{ ohms}.$$

With $n = 8$ bits, T = 50 microseconds, and $R_f = 10$ K, R_1 is given by the equation

$$R_1 = \frac{128}{\tau} \text{ ohms}.$$

Both of the aboven equations indicate that τ should be of the order of 0.1 second at most in order that a summing amplifier be capable of driving R_1.

Because it requires such a large capacitor value and such low resistances, a passive integrator with time constant longer than about 0.1 second is considered impractical.

ACKNOWLEDGEMENT

The project described in this report is part of a hybrid analog-digital computer study directed by Professor G.A. Korn. The writer is very grateful to the

COURSE PROGRAM

The impact of modern simulation methods has penetrated the University of Arizona well beyond the confines of the Electrical Engineering Department. The Nuclear- and Chemical-Engineering Departments have full-size commercial analog computer installations and at least five other departments operate smaller analog computers. Starting in 1965, every engineering student (not just electrical engineers) must take a one-year course covering basic FORTRAN digital-computer programming plus five analog simulation experiments in a new sophomore simulation laboratory developed by Professor G. Peterson. The Analog/Hybrid Computer Laboratory will, therefore, no longer have to teach elementary simulation. The ACL senior and graduate courses in hybrid computation are strongly hardware oriented and emphasize the design of computing devices for control and instrumentation systems, as well as iterative-computer techniques. The laboratory also offers a two-semester sequence of courses in statistical communication theory (preceded, incidentally, by a required additional semester of statistics in the Mathematics Department). In all courses taught in our laboratory, the usual final examination is replaced by a term-paper project which is due a full year after completion of the lecture course. Graduating seniors, of course, have less time to complete their projects; nevertheless, research participation by undergraduates has been quite successful and is a welcome relief from an otherwise abstract and relatively dry modern engineering curriculum.

INSTRUCTION THROUGH MEANINGFUL DEVELOPMENT PROJECTS

As is now well known, analog-hybrid-computer *applications* fit into engineering instruction in a multitude of ways. The *design* of computer components and systems also presents interesting and challenging student projects related to many basic electrical-engineering subjects (e.g., electronics, feedback theory, logic design, network synthesis, random-process theory), and such projects can be of manageable size and reasonable cost. Projects coordinated through two or three yearly budgets can yield respectable computer systems; such coordination makes small development projects more meaningful and closer to true industrial practice. Accordingly, our development work is organized into major projects, usually Ph.D. thesis assignments, each supported by three to five M.S. theses and group of graduate and undergraduate term-paper projects. Each Ph.D. thesis involves experimental and theoretical research, but the Ph.D. candidate is also truly a project engineer responsible for schedules, budgets, purchases, supervision of graduate and undergraduate projects supporting his thesis, and for the hiring and training of undergraduate student technicians. M.S. candidates similarly have their thesis work supported by term-paper projects involving breadboard circuits, tests, or feasibility studies. Thus they, too, begin to acquire experience as project leaders.

Besides the design of fast hybrid-analog/digital components and systems culminating in the new ASTRAC II system, our engineering research is concerned with applications to random-process studies, statistical measurements, and optimization experiments. In addition we are beginning to develop digital programs for a small stored-program computer to be used with ASTRAC II. We are, finally, also interested in the human-engineering aspects of all-digital differential-equation solvers.

Since 1958, the laboratory's publications include 110 ACL memos, of which some 60 have been published in reputable journals or conference proceedings. We have also produced several books, and chapters in engineering handbooks related to our work. This is the result of a conscious effort to get our students to report their development work in writing.

PERSONNEL

The typical half-time assistant takes between three and four semesters to complete his M.S. degree, takes the graduate hybrid course, and helps around the laboratory during his first semester; after this, he should be ready to start on a project of his own, teach the undergraduate laboratory, and supervise undergraduate term papers. Whenever possible, we try to use graduate students as engineers, not as technicians, and hire undergraduate technicians for routine work. As a part of our design effort, we conscientiously attempt to keep assembly jobs sufficiently simple for these student technicians, many of whom receive their first training in our laboratory; we use, for instance, wirewrap conections instead of soldering whenever possible, and buy, rather than assemble digital-logic circuits.

Many of our M.S. graduates have decided to stay for a Ph.D. degree, so that we have, as yet, relatively few graduates who have left the University. We believe that our project-engineering approach has been a successful one, for some of our Ph.D. candidates have turned out to be capable project leaders. Two have accepted professorships at other engineering schools and have started analog/hybrid-computer laboratories of their own. Several have responsible positions in the aerospace and computer industries; one is vice-president/engineering of an instrument company.

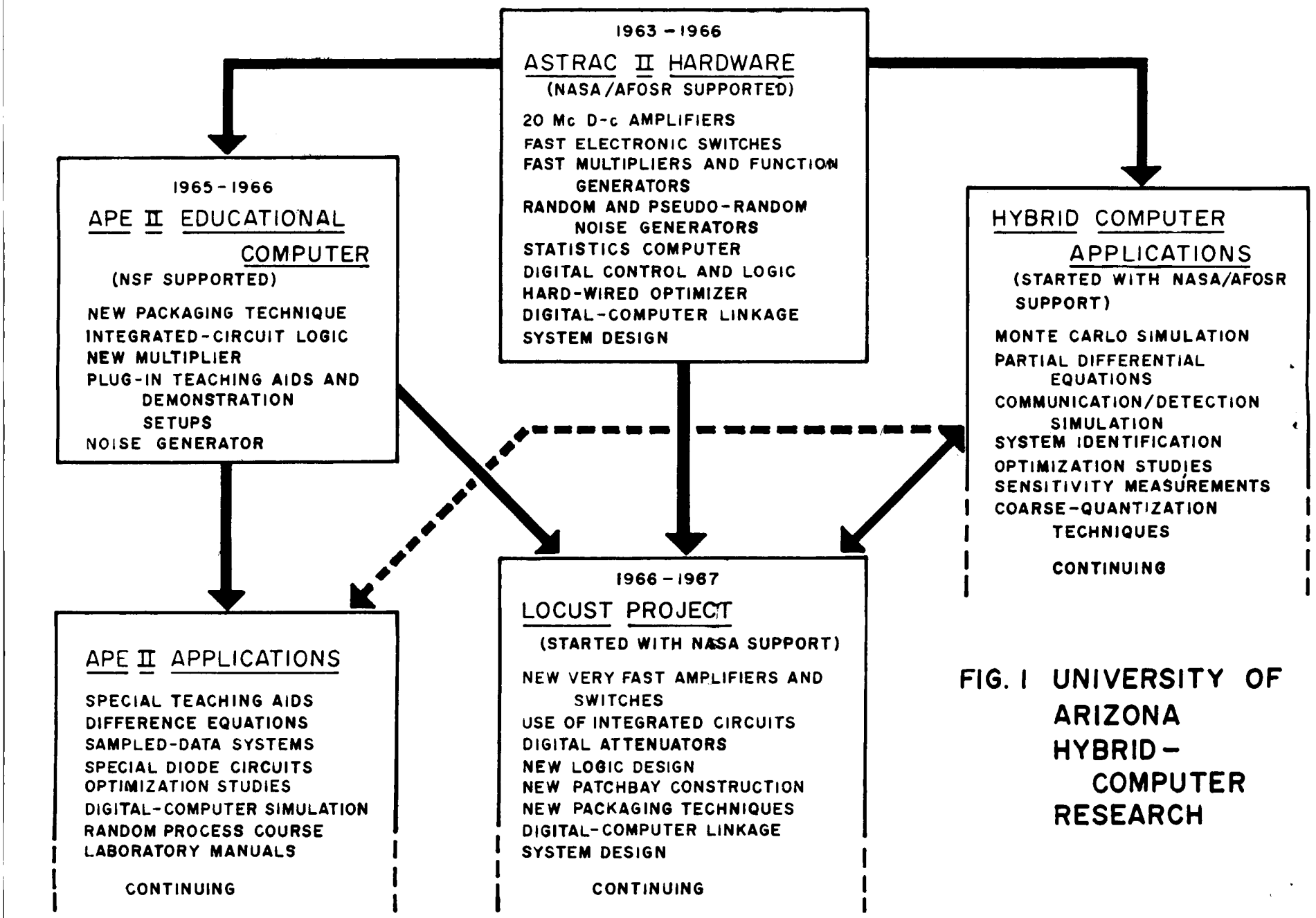


FIG. 1 UNIVERSITY OF ARIZONA HYBRID-COMPUTER RESEARCH

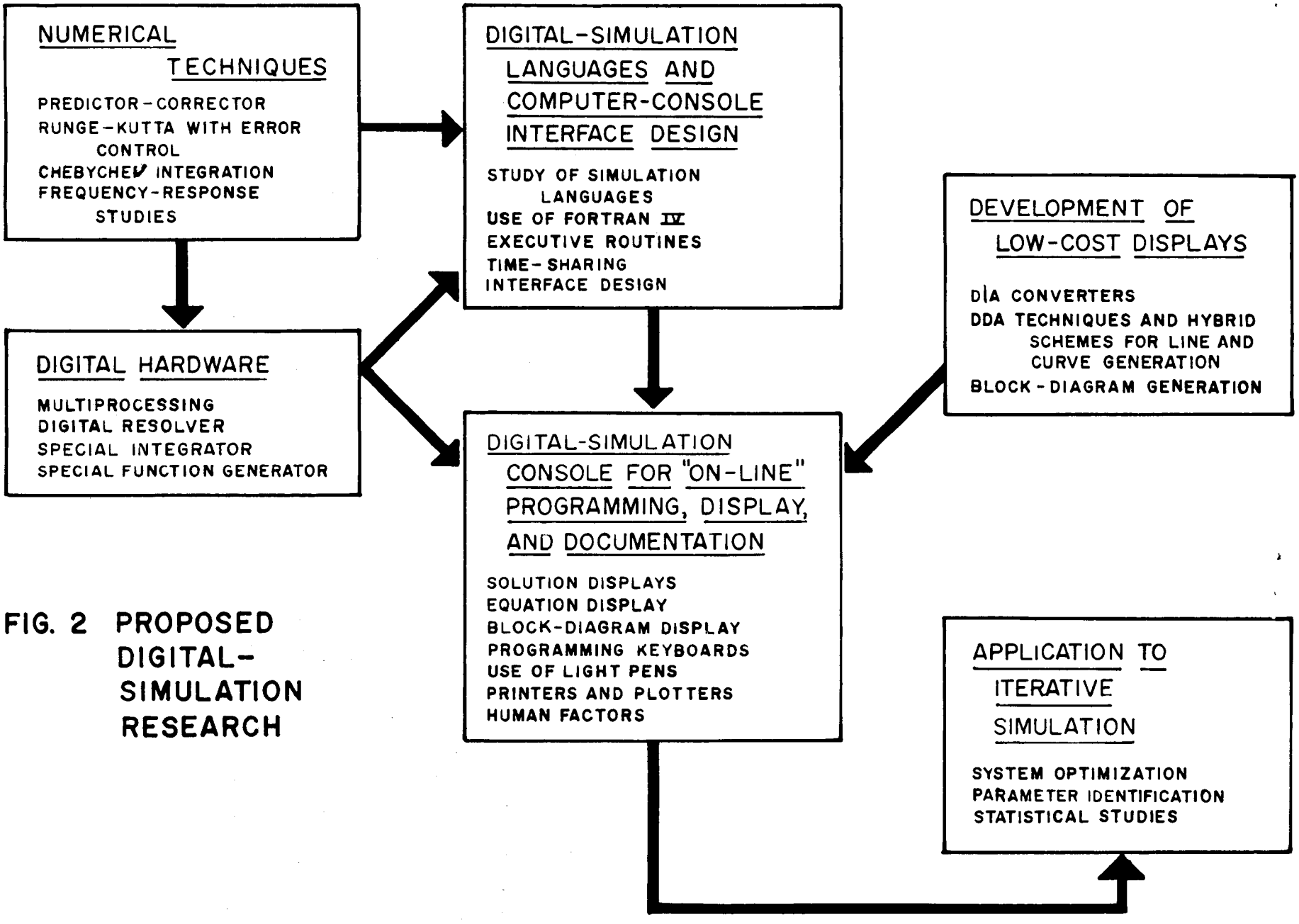


FIG. 2 PROPOSED DIGITAL-SIMULATION RESEARCH

Uniform graphics for *SIMULATION*

The symbols and the methods of laying out analog and hybrid computer diagrams presented here are advocated to alleviate the confusion caused by the uncoordinated invention of new symbols and diagramming practices. The increasing use of hybrid techniques and equipment has aggravated an already bad situation to the point that it is often no longer possible for one worker in our field to read another's diagram. Usually this is because symbols are devised and diagrams are drawn to include details peculiar to a particular kind of equipment. Such a wiring, or "patching," diagram is of course necessary for setting up and checking out an actual simulation, but hardware-peculiar details are only confusing to those with other kinds of equipment. With few exceptions, the use of a simplified signal-flow diagram to illustrate technical articles is much more effective.

With the foregoing in mind an SCi committee composed of

GEORGE BURGIN
JOE HUSSEY
HANS JORGENSEN
GRANINO KORN
JOHN McLEOD

selected the symbols and offers the following suggestions for their use. Primary considerations were current usage, clarity, and simplicity. We devised no new symbols and, unless there were overriding indications to the contrary, we adopted those already in widest use. Clarity and simplicity, we believe, will be enhanced by the choice of unique shapes to represent different components, and the elimination of all unnecessary details in diagrams.

There was no intent on the part of our committee to set up standards for the industry. However, all diagrams appearing in *SIMULATION* will be prepared according to the committee's recommendations (as they may be modified from time to time), and we hope that these recommendations will prove attractive to others. Suggestions for modifications and additions are solicited.

General rules

The following methods and symbols are recommended for the illustration of *technical articles* prepared for *publication*. Unless the purpose of the article is to describe the use of a particular kind of equipment, and the hardware details are pertinent to the subject, such illustrations should *not* be "hardware-peculiar." In other words, the objective should be to show signal flow, rather than "patching" details.

The primary, or overall, system diagram should show only the essential signal flow. Where it is necessary to show details, separate diagrams should be made and referenced to the primary diagram by enclosing the detailed area of the primary diagram in dotted lines with suitable notation.

The direction of signal flow should be indicated by arrowheads except where the shape of the symbols makes the direction of flow obvious. Primary signal flow (with the exception of feedback loops) should be from left to right, and, if practical, each "line" of symbols should be made to read like the mathematical relation it represents.

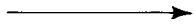
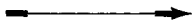
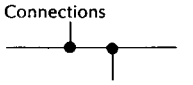
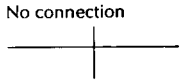
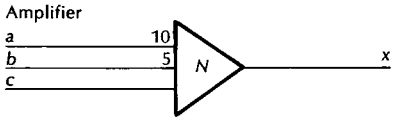
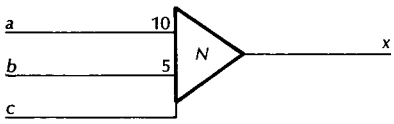
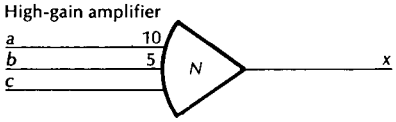
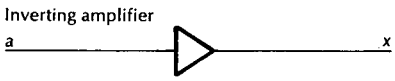
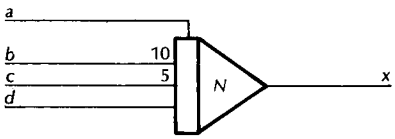
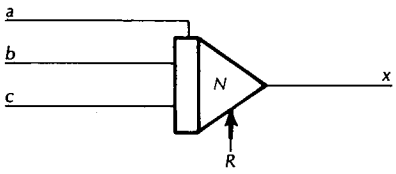
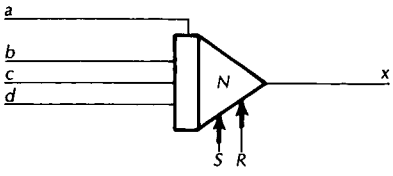
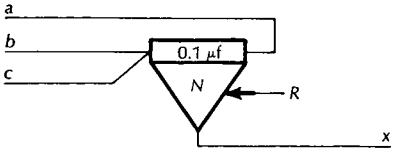
The choice of whether to end a line and label it (preferably with the symbol of the variable that the signal represents) when it reaches the right-hand side of the diagram, and then indicate its continuation with the same label as it enters again at the left-hand side, instead of drawing in the connection, should be made on the basis of clarity; if a line returning the signal from right to left will cross many other lines and be hard to follow, it should not be drawn in.

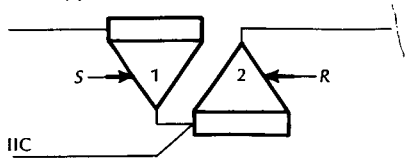
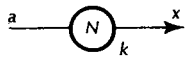
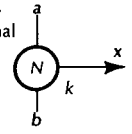
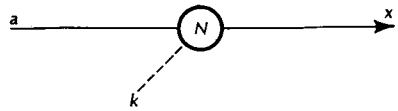
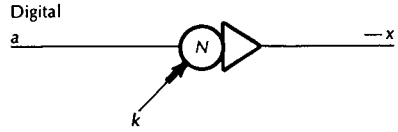
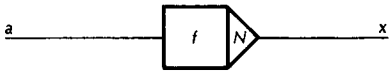
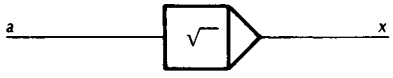
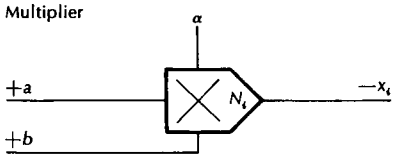
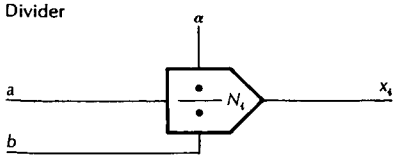
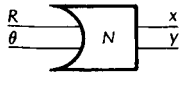
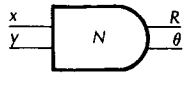
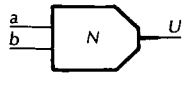
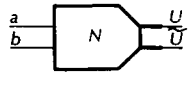
If a diagram involves a number of identical circuits, only one should be shown in detail, while the others should be indicated by boxes with appropriate notation.

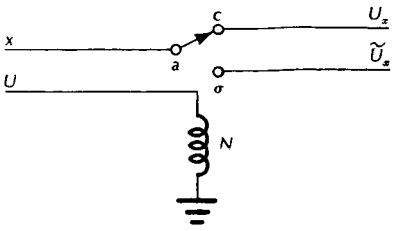
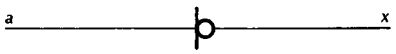
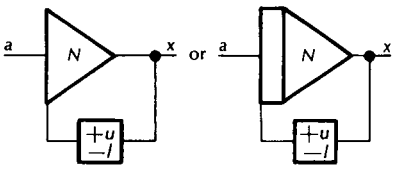
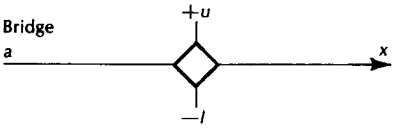
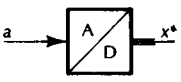
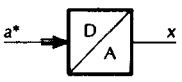
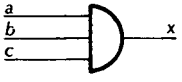
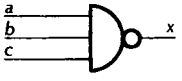
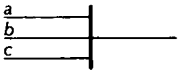
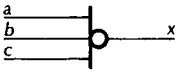
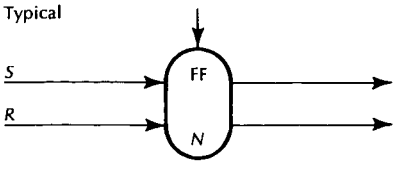
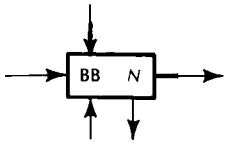
Components should not be numbered unless they are referred to by number in the text.

All amplifier gains should be shown just outside the amplifier at the point where the input enters. Unity gains should not be labeled.

Always apply the test of clarity and simplicity. Ask yourself: "Is this the most understandable way to diagram this *for those unfamiliar with the hardware, and less familiar with the subject, than I?*"

ELEMENT	SYMBOL	FUNCTION	NOTES
Signal flow	Analog  Binary 		Distinction as to kind of signal is made only at beginning and end of line, and then only where there are two or more kinds of signals to be shown on one diagram. Arrowheads should be omitted only if direction of signal flow is obvious.
	Digital word  Mechanical		
	Connections  No connection 		
Summers	Amplifier 	$x = -(10a + 5b + c)$	No arrows; shape clearly indicates direction of flow. No label on unity-gain input. "N" indicates where number of amplifier should be placed if, *and only if,* referred to in text.
	Summing amplifier (with high-gain input) 	$x = -(10a + 5b + \mu c)$	Label high-gain input "SJ" or "G" only if pertinent; the point at which c enters (at top or bottom of symbol) indicates a gain of μ.
	High-gain amplifier 	$x = -\mu(10a + 5b + c)$	Note that the numbers at the inputs are now only relative gains; μ, an unspecified large number which is a function of the particular amplifier, is the overall gain.
	Inverting amplifier 	$x = -a$	When amplifiers are used *only* to change signal sign they should be smaller. Orientation should be that which makes for greatest graphical simplicity, *i.e.,* they may be shown in vertical, or in feedback, paths.
Integrators	Standard 	$x = -a - \int_0^t (10b + 5c + d)dt$	Standard integrator mode is that of basic problem. The point at which a enters (at top *or* bottom of symbol) indicates that it sets the initial value of x, so it is redundant to label it IC.
	Two-mode 	RESET when $R = 1$ COMPUTE when $R = 0$	Arrows indicating mode control should be shown only when two or more integrators are operating in different modes simultaneously. The mode-control input should then be labeled or coded to indicate the controlling mode.
	Three-mode 	RESET when $R = 1$ or $R = S = 1$ HOLD when $S = 1$, $R = 0$ COMPUTE when $R = S = 0$	
	Track-hold 	TRACK when $R = 1$ HOLD when $R = 0$	When used in this way the size of the integrating capacitor may be important, as it affects the tracking lag. In such cases the value should be indicated as shown. The quantity tracked or held is $-(a + b + c)$.

ELEMENT	SYMBOL	FUNCTION	NOTES
Integrators (continued)	Memory pair 	Integrator 1 in Track for $S=1$ Integrator 2 in Track for $R=1$	Integrator 1 in TRACK for $S=1$, integrator 2 is TRACK for $R=1$. In certain iterative problems y is required to have some value for the first iteration; thus an "initial" initial condition must be furnished as shown.
Potentiometers	Two-terminal  Three-terminal 	$x=ka$ (load connected) $a=1, b=0$ (load connected)	The mathematical relationship shown for the three-terminal pot is given only to define k. It will not usually hold during problem solution because if b were always zero a two-terminal pot could be used. If it is desirable to define k in any other way, its meaning should be clearly indicated.
	Servo-set 	$x=ka$	This should be used only if the fact that N is servo-set is significant to the solution of the problem, as, for instance, when it must be automatically reset after each run of an iterative problem.
	Digital 	$x=k*a$	As shown, the symbol indicates a digital pot with integral (committed) inverting amplifier. The symbol for non-inverting digital pots should not include the amplifier. *Indicates quantized value.
Function generators	Arbitary 	$x=f(a)$	The number N should be used only when the function generator is referred to by number in the text, *or* when it is desirable to explain what the function f is, either by a footnote, or by a separate graph.
	Mathematical functions (typical) 	$x=\sqrt{a}$	In cases where the function generated can be represented by a standard mathematical symbol, the f should be replaced by the symbol.
	Multiplier 	$x=\frac{ab}{\alpha}$ $x=\frac{\alpha a}{b}$	These symbols should be used for all analog multipliers and dividers; if the *kind* is significant to the solution of the problem, it should be so stated in the text and/or noted on the diagram. Because equipment differs, the sign of the output for specified signs of both inputs should be given, otherwise inversion will be assumed. The number N should be used only if the component is referenced in the text, *or* if more than one channel of a multichannel device is used. In the latter case the subscript, in this case i, identifies the channel. In many cases, it will be found that a drawing can be simplified and clarified by drawing the same multichannel device in more than one signal flow path. In this case the number would be the same, but the subscript would be different for each channel.
	Divider 	$\alpha=$ reference voltage	
	Resolvers Polar to rectangular  Rectangular to polar 	$x=R\cos\theta$ $y=R\sin\theta$ $\theta=\arctan y/x$ $R=\sqrt{x^2+y^2}$	If a resolver has additional outputs they should be shown only if used.
	Comparators With binary output  With true and false binary outputs 	$U=1\ (a<b)$ $U=0\ (a>b)$ $\tilde{U}\neq U$	The symbol for a relay comparator can, of course, be made by combining either of these symbols with that of a relay.

ELEMENT	SYMBOL	FUNCTION	NOTES
Relay		$U_x = x$ $(U=0)$ $\tilde{U}_x = x$ $(U=1)$	If the diagram is drawn as shown, the designations of arms and contacts are superfluous. However, it is often desirable, for clarity, to show the relay coil in one place on a diagram and the contacts in signal-flow paths elsewhere. In this case, N_{oa} would designate the normally Open $(U=0)$ contact of channel a, relay N; N_{aa} the Arm of channel a of relay N, etc.
Digital inverter		$x = \tilde{a}$	The tilde (~) is used instead of a bar to indicate negation. This is recommended because of the many other meanings of a bar over a variable.
Digital/analog switch		$U_a = a$ $(U=1)$	ON when binary signal, U, is digital "one."
Limiters	Feed-back 	$x = -a$ $(l < a < u)$ $x = -l$ $(a < l)$ $x = -u$ $(a > u)$	u = larger value at which output is limited l = smaller value at which output is limited
	Bridge 	$x = a$ $(l < a < u)$ $x = l$ $(a < l)$ $x = u$ $(a > u)$	
Converters	Analog-to-digital 		*Indicates quantized value.
	Digital-to-analog 	$x^* = a$ $x = a^*$	
Diode	Solid state 	$x = a$ $(a > x)$ $x = 0$ $(a < x)$	
Diode gates	AND 	AND $x = a \cdot b \cdot c$	Output is high (logic 1) if and only if all inputs are high.
	NAND 	NAND $x \neq a \cdot b \cdot c$	Output is low (logic 0) if and only if all inputs are high.
	OR 	OR $x = a + b + c$	Output is high (logic 1) if and only if at least one input is high (*i.e.*, any or all of the inputs are high).
	NOR 	NOR $x \neq a + b + c$	Output is low (logic 0) if and only if at least one input is high (*i.e.*, any or all of the inputs are high).
Flip-flop	Typical 		As there are many kinds of flip-flops, symbolic representation of the operation of any but the simplest is not advised; if the operation is not obvious, an explanation in the text or a footnote with the diagram is recommended.
Black box		This is Black Box number N, to be used if no symbol is given here, *or in case of doubt!* It can have any number of inputs and outputs, but the nature of the signals should be indicated and all signal-flow directions should be designated by arrowheads. Here there are three analog inputs giving rise to one analog and one binary output.	The function of a "black box" can often be made obvious by properly labeling the inputs and outputs. However, if it is not obvious, the function should be explained in the text or by a footnote with the diagram. If internal details are of interest, they should be shown in an appropriately labeled auxiliary diagram.