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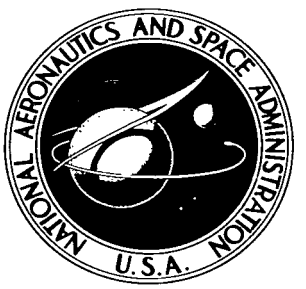




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# EVOLUTION OF SATELLITE PFM ENCODING SYSTEMS FROM 1960 TO 1965

*by Hosea D. White, Jr.*

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## ABSTRACT

The optimum small scientific satellite system is assumed to be one in which the experimenter merely designs a sensor to measure the phenomena of interest, mounts it on a spacecraft, and later receives a "perfect" master data tape from the ground station. Thus, much of the experimenter's burden of the electronics design and testing now required on the spacecraft would be eliminated.

Although this optimum concept may never be attained, the purpose of this paper is to show how, over the past 5 years, an attempt to approach it has been made: The PFM encoding system has been expanded to encompass more spacecraft electronics in a central package and to incorporate hardware to permit much of the time correction and error detection to be done by computer programming on the ground.

The "functional complexity" of the encoding system is shown to have increased by a factor of 20 from Explorer XII (designed in 1960) to IMP F (designed in 1965); yet the volume has remained about the same, and low power (about 1.2 watts) has been maintained. The Explorer XII encoder took about 200 transistors, and IMP F (Super IMP) would take about 4000 if conventional circuits were used. The circuit design approaches taken in Super IMP are analyzed; and the use of a completely different approach, using MOSFET blocks, is discussed. This approach has resulted in an impressive decrease in electrical parts count and an even more impressive decrease in the "dangerous" nonresistor parts count.

CONTENTS

# EVOLUTION OF SATELLITE PFM ENCODING SYSTEMS FROM 1960 TO 1965*

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## INTRODUCTION

Pulse-Frequency-Modulation (PFM) telemetry encoding systems are used on small scientific satellites where weight and power are at a premium. These usually are satellites that measure both fields and particles and so have both analog and digital sensor outputs.

The optimum small scientific satellite telemetry system is assumed to be one in which the experimenter merely designs a sensor to measure the phenomena in which he is interested, mounts it on a spacecraft, and later receives a "perfect" master data tape from the ground station during flight (Figure 1). This master data tape would be edited in such a way that time is correct and all errors are either corrected or flagged. The edited master data tape then could be used as an input to the experimenter's computer program, and should be of such quality that the results could be trusted without concern about timing errors or computer-program "blow up."

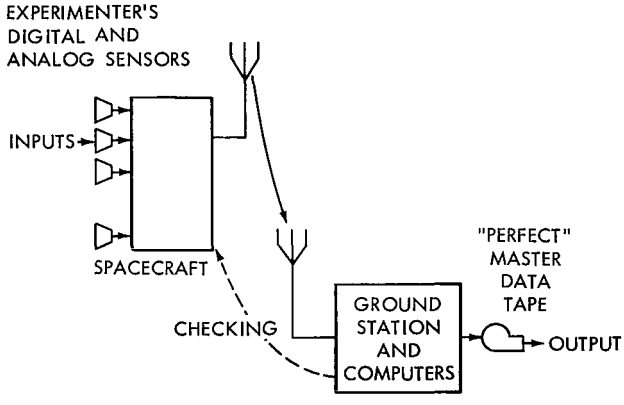



Figure 1—Optimum system for scientific satellite.

Although this optimum concept may never be reached, the purpose of this paper is to show how—over the past 5 years—an approach has been made by expanding the PFM encoding system to encompass more spacecraft electronic functions in a central package. The "functional complexity" of the Super IMP encoding system has increased by a factor of more than 20 over that used in Explorer XII (1961 $\nu$1). Yet the volume is about the same, and relatively low power (about 1.2 watts) has been maintained without going to conventional "solid circuits." The components

*Presented at the Third Space Congress, Cocoa Beach, Florida, March 1966.

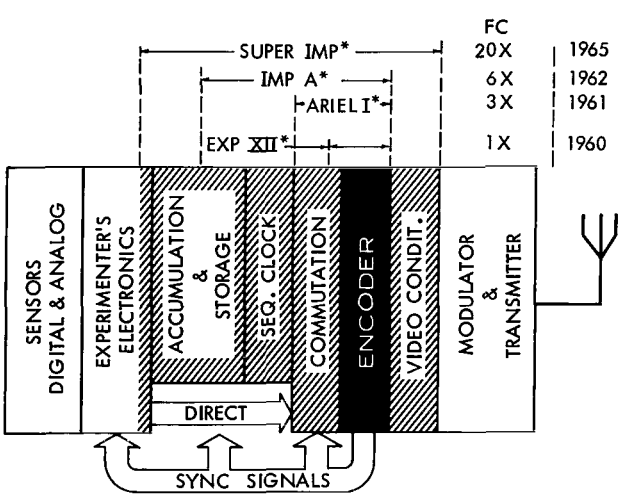
used to accomplish this (MOSFET* blocks) will be discussed briefly. Giant strides have been made in PFM data processing with the advent of IMP A (Explorer XVIII: 1963 46A). These concepts will not be discussed except to show that hardware has been installed on the satellite to allow much of the time correction and error detection to be done by computer programming on the ground.†

## THE PFM ENCODING SYSTEM

PFM telemetry has been described amply in the literature (References 1 and 2). Briefly, PFM is a form of time-division multiplex especially suitable for small scientific satellites because of its efficient use of transmitter power as a function of bit rate. The PFM encoder is the device that encodes the experimental information into a series of pulsed frequency bursts where the burst frequency contains the intelligence of a single analog parameter or the state of either 3 or 4 binary bits, depending on the satellite used. The encoding system is defined as the encoder plus other functions such as a digital data processor, in a central package.

Figure 2 shows the electronic section of a small scientific satellite, not including the power system and the structure. It illustrates the growth of the electronic systems from Explorer XII to Super IMP.

The experimenter designs various sensors and has them mounted on the spacecraft. With the optimum system described earlier, this would be the end of the experimenter's task, since all the rest would be done by the spacecraft and data processing on the ground. Since the optimum system does not yet exist, the experimenter must design special electronics to mate with the sensor; he may also wish to do on-board data processing. To accomplish on-board data processing, the analog experimenter may need many analog-to-digital (A/D) conversions. Two approaches may be taken: Each experimenter may do his own, or a central A/D converter may be time-shared among experimenters. The former approach is often used; but the latter will be employed in the Super IMP, with the encoding system supplying a calibrated A/D conversion signal for experiment on-board data processing in the "Magnetometer Autocorrelation Computer." This same A/D




* = Encoding system function
X = Approximate functional complicity

Figure 2—Evolution of the PFM encoding system.

*Metal-Oxide Silicon Field-Effect Transistor.

†Mish, William H., "A Description of the IMP-A (S-74) Ground Station Time Error Detection and Rectification Software," Goddard Space Flight Center Document X-612-64-128, October 1964; and "Timing Error, Their Detection and Correction in the IMP Information Processing System," Document X-612-64-328, October 1964.

converter will be used by other experiments; thus, a significant savings in weight and power may be achieved.

The digital experiments often require accumulation of pulses and storage of data until readout time. Also, dynamic range may be a problem, so bit compression techniques are required. In the case of the Super IMP, nine such experiments require approximately 450 bits of accumulation and storage every 5 seconds. In the past (Explorer XII and Ariel I*), each experimenter provided his own accumulation and storage and, in the case of Explorer XII, even did most of his own commutation. This resulted in a rather inefficient overall system since many experimenters did the same thing, and the connector and readout problem was rather complicated. When several experimenters require accumulation and storage, a central processor often provides these advantages:

1. More efficient use of power;
2. Reduction of interface connections;
3. Elimination of the accumulator readout problem;
4. Cost reduction, since only one development program is required;
5. Removal of burdens from the experimenter, including testing of accumulators.

The PFM encoding system provided the central processor, called a Digital Data Processor (DDP), in the IMP A satellite for the first time. This same design was used in IMPs B and C.

## IMP A Digital Data Processor

The IMP A DDP has a total experimenter capacity of 105 bits plus a 15-bit sequence clock. The IMP A accumulator breakdown is shown in Table 1. The sequence clock was used extensively in various computer programs on the ground. It was read out twice per sequence and thus could be used as an error detection device for the complete loop—including the satellite, telemetry stations, information processing line, and the computer programs. It also was successfully used in ground station time-error detection and rectification software.† The sequencing clock had a capacity of 1 month before overflow.

The IMP A digital data processor was manufactured in 2-1/3 one-inch delta-pack cards using the welded module technique. The basic electrical component was the complementary

Table 1

Accumulators used in IMP A.

| Experiment | Accumulator Breakdown* | Storage (bits) |
|---|---|---|
| Univ. of California | 2 each, 15-bit "S" | 30 |
| Univ. of Chicago | 1 each, 3-bit "S"<br>1 each, 6-bit "S"<br>1 each, 9-bit "S"<br>1 each, 12-bit "S" | 30 |
| Goddard Space Flight Center | 2 each, 6-bit "S"<br>2 each, 9-bit "S"<br>1 each, 15-bit "S" | 45 |
| Sequence clock | 1 each, 15-bit "S" | 15 |
| Total | 12 | 120 |

*"S" stands for Signal and indicates a straight binary counter from which only the count is telemetered.

*Ariel I (UK-1): 1962 o1.
†W. H. Mish, ibid.

flip-flop using 24 parts per bit and averaging about 1 milliwatt per bit. Of the 24 parts per bit, 17 were not resistors.

## Super IMP Digital Data Processor

The Super IMP has a DDP of expanded capacity and improved design. The experiment capacity of the Super IMP DDP is about 460 bits, or four times that of IMP A. In addition, most of the accumulators will use a bit compression scheme that will allow for a larger dynamic range in counting rate. The digital bit rate has been increased by a factor of 10 over that employed in IMP A, using the same transmitter power at the same range. This is accomplished by increasing the number of bits per channel from 3 to 8 and increasing the channel rate by 4. Each burst is obtained from the output of a 16-level crystal-controlled frequency synthesizer, and the frequencies will be "coherent" to a useful accuracy.

The present accumulator breakdown for the Super IMP DDP is shown in Table 2.

Table 2

Accumulators used in SUPER IMP.

| Experiment | Accumulator Breakdown* | Storage Bits |
|---|---|---|
| Appl. Phys. Lab. | 1 ea, 16-bit "ST" | 16 |
| Bell Tel. Labs. | 5 ea, 15-bit "ST" | 75 |
| U. Cal. | 2 ea, 16-bit "ST"<br>1 ea, 16-bit "S"<br>1 ea, 14-bit "S"<br>1 ea, 2-bit jammer | 64 |
| U. Chi. | 2 ea, 10-bit "ST<br>1 ea, 12-bit "ST" | 32 |
| GSFC | 4 ea, 10-bit "S"<br>1 ea, 24-bit "S" | 64 |
| SW Ctr. for Adv. studies | 9 ea, 10-bit "ST"<br>1 ea, 6-bit "S" | 96 |
| Space Tech. Labs. | 2 ea, 8-bit "S" | 16 |
| U. Iowa | 2 ea, 12-bit "ST" | 24 |
| Optical aspect | 4 ea, 12-bit "S" | 48 |
| Sequence clock | 1 ea, 16-bit "S" | 16 |
| Total | 38 | 451 |

*"ST" indicates that either Signal or Time is telemetered. These accumulators will count pulses up to a maximum and will then count clock pulses for the rest of the accumulation period. Thus, either the count S or the counting rate T will be telemetered. This scheme takes care of the overflow problem and thus extends the counting-rate dynamic range.

The maximum input rate any accumulator may accept is about 500 kc. Maximum experiment rates usually are in the order of 100 to 250 kc, so the 500 kc provides an adequate safety margin.

## The Commutator and the Encoder

It may appear strange that the commutator is a separate block in Figure 2, since it is so interrelated with the encoder. It appears as a separate block because of the nature of PFM encoding: bits were scanned 3 bits at a time and encoded into one of the eight "discrete" frequencies representing the state of the 3 bits; thus, shift registers were seldom used. Note that the Super IMP encodes 8 bits per channel instead of the 3 mentioned for Explorer XII, Ariel I (UK-1), and IMP A (Explorer XVIII).

In Explorer XII, all of the accumulation and most of the digital commutation was done by the digital experimenters. The Explorer XII encoder commutated information from 23 analog lines and 12 digital lines. The Ariel I encoder

commutated information on 100 lines from the British experiments (this was all the satellite commutation), but the experimenter did all his accumulation. The Ariel I encoding system had many improvements over that used in Explorer XII in circuit design and packaging techniques. Welded modules were used extensively for the first time at GSFC. (Reference 2 discusses these systems.)

For the purposes of this paper, note that the functional complexity increased by a factor of 3 between the two systems, with Ariel I handling information from 100 lines and Explorer XII only 35 lines. The Explorer XII system used about 200 transistors, and the Ariel I system about 600. Ariel I had two encoders: One was real time, the high-speed encoder; and the other was the low-speed encoder. The low-speed encoder was tape-recorded in the Satellite at 1/48, the information rate of the real-time encoder. On command from a ground station, the taped output was played back 48 times faster than the recorded speed.

## FUNCTIONAL COMPLEXITY

The ambiguous term *functional complexity (FC)* is used here to connote "usefulness" of the system or "what the system does for the experimenter." Although impossible to measure accurately, it is as good a term as any to illustrate the purpose of this paper.

The encoder on Explorer XII, to be used as a reference, is arbitrarily assigned a functional complexity of 1 (FC = 1X). Various other PFM satellites before and after this are not described here. In general, the ones before Explorer XII (Vanguard III, Explorers VIII and X, etc.) would have an FC of less than 1. It should be noted the IMPs D and E (Anchored IMPs) designed in 1965, are about midway between IMPs A, B, C and F, G in functional complexity.

Table 3 summarizes a few of the significant features illustrated by FC. It should be noted that the values of FC were assigned subjectively and not by a mathematical method, so the values may be subject to argument.

Table 3 illustrates one rather interesting fact: The transistor count is approximately directly proportional to FC. If this were extrapolated to the Super IMP encoding system, we would expect about 4000 transistors. This would be the case if IMP F were made exactly like IMP A, and probably would result in a system too complicated, too heavy, and too large to fly on a small scientific satellite. Work has been done to reduce this count by using conventional components, and this would eliminate about 1000 transistors. However, the capacitor and diode count would not be reduced. It was assumed that the nonresistors (transistors, capacitors, and diodes) were not as reliable as the resistors; in fact, the resistors were regarded as completely reliable. (Note that these assumptions are the author's.)

Table 3 illustrates another important consideration: that of interconnecting signal wires. The signal wires are defined as the wires from the experiment to the encoder commutator and do not include Performance Parameter (PP) lines. The signal wires of course, must be commutated and encoded to be of any use to the experimenter. The Ariel I encoder is a good example of how not to save wires, since 100 information lines were sent to the encoder. Of these, 51 were

Table 3

PFM Encoding System Functional Complexity (FC), 1960 to 1965.

| Year Designed | Encoding System Used On Satellite | Functional Complexity | Number of DDP Bits | Number of Lines Commutated | Number of Input Signal Lines | Number of PP Lines | Comments | Approx. Transistor Count |
|---|---|---|---|---|---|---|---|---|
| 1960 | Explorers XII, XIV,* XV, XXVI | 1X | 0 | 35 | 19 | 16 | Taken as FC = 1X printed circuit boards | 200 |
| 1961 | Ariel I | 3X | 0 | 100 | 100 | 0 | Two encoders, welded modules | 600 |
| 1962 | IMPs A, B, C | 6X | 105 + clock | 159 | 35 | 15 | First DDP, all modules and interconnects welded | 1200 |
| 1965 | IMPs F, G (Super IMP)† | 20X | 445 + clock | 508 | 73 | 36 | Time-share A/D converter bit rate x 10 IMP A | New approach necessary |

*Explorer XIV (1962 B$\gamma$1), Explorer XV (1962 B$\lambda$1), and Explorer XXVI (1964 86A) used essentially the same systems.
†IMPs D and E (Anchored IMPs) have a FC of about 10X and use MOSFETS.

accumulator output lines and could have been saved by having the encoding system do the accumulation and commutation. Also, a shift-register scheme could have been used; but that would have added considerable hardware. There was a good reason for direct scanning of the Ariel I digital wires in that some encoder cards were placed directly in the experimenter package to facilitate integration. The experimenters, however, would have preferred that the accumulation be done in an encoding system DDP.

According to the table, then, the DDP "saved" 124 signal lines for IMP A and 435 signal wires on Super IMP, since the commutation is incorporated into each DDP bit. It is clear that "direct scan" (as used in Ariel I) would not be feasible in Super IMP, and the digital experimenters would be forced to use shift registers if they did their own accumulation. Some of the digital experiments are not amenable to accumulators on Super IMP. Thus these experiments do use shift registers and thus do their own commutation. The shift registers are grouped under "Experimenter's Electronics" rather than "Commutation" in Figure 2. The output of the shift registers are scanned 4 bits at a time by the commutator.

It is interesting to note that less signal lines (i.e., a smaller harness) are required on Super IMP than were required on Ariel I, although the functional complexity increased by 20/3 and the commutated lines have increased by a factor of 5. The reason, of course, is that the DDP supplies many output bits (automatically commutated) for each signal line received.

## SUPER IMP CIRCUIT DESIGN AND FABRICATION TECHNIQUES

Since the PFM encoding system has been doing more and more for the experimenter in an attempt to approach the optimum system for small scientific satellites, the parts count has increased drastically. In the author's opinion the IMP A, with a functional complexity of 6X, is about the limit for reliable operation using conventional components.

Figure 3 illustrates the problem. The parts used for 2 DDP bits, with their readout gates (i.e., built-in commutators), are shown. The reduction in parts is obvious. The major reason for the failure of the solid-circuit approach (the two flat packs in Figure 3) is the low-power requirement with adequate noise rejection and sufficient speed.

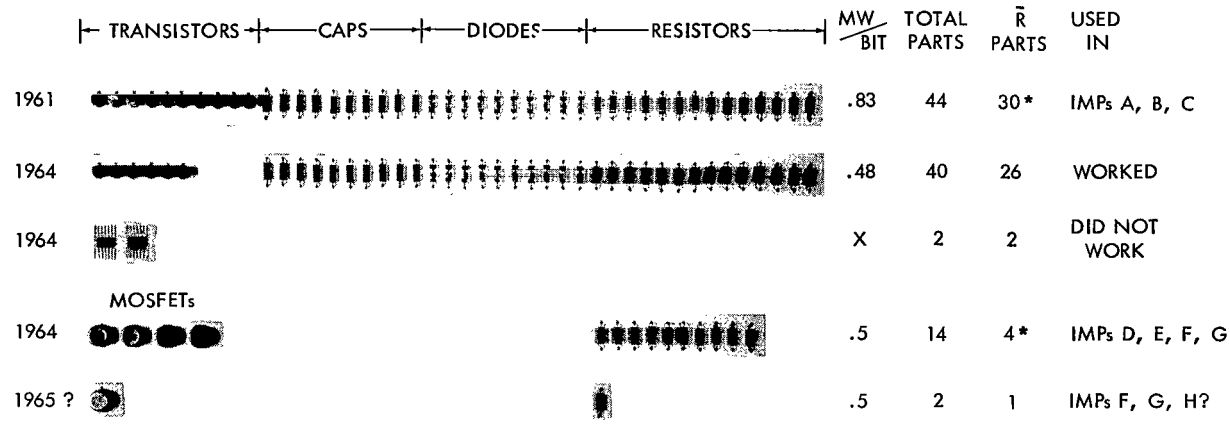



Figure 3—The parts used for 2 DDP bits, from 1961 to 1964.

Figure 3 was made before the last approach (called SECOND MOSFET APPROACH) was actually used in IMP's F & G; thus, some of the nomenclature on the figure is incorrect.

### Approaches Taken

The IMPs F and G encoding system is functionally much more complex than that of IMP's A, B, and C. If a measure of the functional complexity is the number of binary stages required, IMP F is approximately 3.6 times as complex as IMP A: IMP A has about 140 binary stages, and IMP F has about 500.

The IMP A encoding system had approximately 5000 electrical parts, of which 3000 were not resistors. If IMP F used the same circuit design and fabrication technique it would have approximately 18,800 electrical parts, of which 11,500 would not be resistors. None of these figures includes welds.

Several approaches have been taken in an attempt to reduce the IMP's F and G parts count; the main ones are listed:

1. Redesign of electrical circuits (binaries and logic circuits) and improved system design (sexidecimal bursts instead of octal bursts, to make the logic based on a system divisible by 2 instead of 3) in order to reduce the number of parts. This has been done; and it is estimated that approximately 5500 parts can be saved, resulting in a "conventional" design with 13,200 parts—of which 8600 are nonresistors. This still is an awesome number of parts.

2. Monolithic solid-circuit approach. In this approach, two types of low-power elements were used. The elements were a BINARY BLOCK (at 0.5 mw/bit) and a low-power LOGIC BLOCK (at approximately 0.1 mw/logic function). The two blocks would be used in approximately 65 percent of the system, and "conventional" components in the rest. Both blocks were based on the improved circuit design above. This approach was abandoned because the MOSFET approach seemed much better.

3. First MOSFET approach, (actually used in IMPs D & E). Here again, two basic building blocks were used: a MOSFET BINARY (with resistors added externally) and a LOGIC BLOCK. Two promising things happen with this approach: One is that about 93 percent of the system will be MOSFET blocks or resistors; and the other is that the total parts count goes down to about 5200 parts, where only 1700 are nonresistors. Thus, this approach results in about the same number of total parts used in the IMP A encoding system but has even less nonresistor parts than IMP A. Note again that IMP F has about 3.6 times the functional complexity of IMP A.

4. Second MOSFET approach. New blocks were obtained, where two binary bits and their readout gates as well as the associated resistors were integrated on a single chip. The logic blocks described above and these new blocks permitted a 50% size reduction of a kind that the nonresistor parts were reduced to about 800.

In all the foregoing, it is assumed that resistors are an order of magnitude more reliable than nonresistors (capacitors, diodes, transistors, or MOSFETs) and may be weighted accordingly in a mathematical reliability analysis.

The second approach listed above (the monolithic solid-circuit approach) was more desirable than the first, but was abandoned because of schedule problems (approximately 8000 parts were required; but this figure may be off by 50 percent).

The third approach listed (the first MOSFET approach) appeared to be by far the best from its electrical properties, reduction of parts, and schedule. Its disadvantage was that less was known about its long-term reliability than was known about the conventional approach. Indeed, it turned out that the MOSFETs required shielding because their gate thresholds shifted as a function of radiation (Reference 3). IMPs D and E have been designed, manufactured and tested with this approach, and IMPs F and G (Super IMPs) were also designed with this method. The package for the Super IMP encoding system came out as a 7-1/2 inch delta pack which would require about 7 pounds of shielding. This was too heavy, so another approach, the second MOSFET approach,

was used. (Note that the first MOSFET approach was entirely adequate for IMPs D and E because its functional complexity was about 1/2 that of IMPs F and G and came out as a 3-1/2 inch delta pack.) Also the shielding required on IMPs D and E was less because it will be a lunar orbiter.

The fourth approach listed (the second MOSFET approach) was used in order to reduce the size of the encoding system package (Figure 3, bottom row). The prototype for IMPs F and G has been manufactured into a 3-1/2 inch delta pack by using this approach. The new building blocks required for this approach were also manufactured by GME on a very short time scale. In this report we shall not elaborate further on this second MOSFET approach except to say that it will probably open new horizons in small scientific satellite systems. These new blocks incorporate up to 50 MOSFETs and 16 very large value polycrystalline silicon resistors on a monolithic chip in such a way that highly reliable low power circuits may be used. The use of this new technology will be the subject of another paper.

## First MOSFET Approach Expanded

Since all approaches except the MOSFET approach are familiar to most readers of this paper, and since the MOSFET is a new device, this section will give some of its electrical properties that are useful in IMP encoding system design.

A primary design constraint is power, which must be relatively low. Since a great deal of accumulation and storage is done in the encoding system digital data processor, binary counters are used. One primary problem, then, is how to make a low-power binary, at reasonable speeds (up to 500 kc), that is electrically quiet and that will perform for 1 year in orbit over the temperature range of -30° to +60°C. In the past (IMP A), complimentary flip-flops were used with considerable success. A two-transistor "low-power" flip-flop which eliminates half the transistors has been developed. Either of these devices operates on the principle of using low voltages (supply) and reasonably low resistor values (up to about 200 K). The fact that the supply voltages are low implies that the "trigger" voltages must be low, and this means that the noise rejection threshold is low.

The MOSFET binary works on a different principle to achieve low power: It uses large voltages and large resistors. The supply voltages have a difference of potential of 10.5 volts, and it takes a "trigger" of about 5 volts (large) to flip them; this gives excellent noise rejection. It should be pointed out here that all capacitors and diodes have been eliminated in the binary design and that the device uses a double-input threshold level "flipping" technique. Indeed, a binary stage consists of one TO-5 can and four large-value resistors while a complimentary flip-flop requires 4 transistors, 6 resistors, 5 capacitors, and either 4 or 8 diodes depending on speed requirements. Thus, the low-power MOSFET has five discrete parts, and the low-power complimentary flip-flop has up to 23 parts; this is a parts reduction of better than 4 to 1 and is a "nonresistor" parts reduction of up to 17 to 1! The fact that the resistors are external enables the designer to obtain an efficient speed-versus-power profile. Thus, a 0.1-mw low-speed MOSFET flip-flop is obtained by using 2-megohm resistors. The external high-value resistors used with the MOSFET

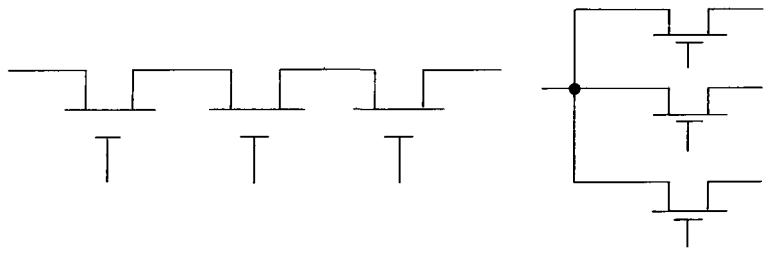
binary protect against the possibility that a "short" in a MOSFET binary could cause a catastrophic failure by "deadheading" the line. This is particularly important since about 88 percent of the binaries are such that a failure will cause loss of data from only part of a single experiment. The rest of the experiments still would provide useful information.

An especially promising feature of the MOSFET approach is the elimination of many stages in the electrical testing of modules and of the individual discrete components that go into the modules.

Another desirable quality of the MOSFET is that it is a voltage (not current) operated device. The input impedance at its gate is many megohms; thus, no steady-state power is required to operate MOSFETs in a logic function (i.e., it is not necessary to supply "base current").

The MOSFET essentially has no "offset" voltage; it acts like an open circuit when off and a resistor (less than 3K) when on. When off, the leakage is very low. This feature is useful in commutating devices.

Another unique property of the MOSFET is that it is symmetric (the source cannot be distinguished from the drain). This, of course, means that a simple monolithic logic block can be made from MOSFETs and can be arranged in many different logic configurations. The LOGIC blocks used are as follows:



It is up to the designer to utilize the many ways that the blocks can be connected, and the things he can do with MOSFET logic blocks, with very few parts and with considerable power savings are quite surprising.

On some occasions, transistors are required and can be mated very well with MOSFET logic when required.

There is good evidence to indicate that the manufacturing process steps required to make an all-MOSFET monolithic chip are considerably fewer than those for conventional integrated circuits. The blocks have worked well, and the foregoing example is given to illustrate that the manufacturing processes may be simpler than those of integrated circuits.

## EVALUATION OF FIRST MOSFET APPROACH

### Circuit Design Using Individual MOSFETs

Several different binaries were designed and breadboarded at Goddard Space Flight Center. These binaries were operated in an extremely simple system to check their noise rejection and speed-power profile. The disadvantage of this binary is that it takes 12 MOSFETs and 4 resistors and that its standby power is twice that of the other binaries breadboarded. The advantage gained is that it is a threshold double-input direct-coupled device (i.e., master-slave binary) which can be manufactured with no capacitors or diodes. Good speed versus power was not obtained with the breadboard because of excessive capacitances, but this problem was largely solved by GME in a monolithic package.

### Specification for the Two Basic Building Blocks

It was decided to have the 12 MOSFETs of the binary in an integrated package and to mount the chip in a TO-5 header. The four resistors were to be placed external to the package for three basic reasons:

1. The speed versus power can be tailored.

2. The metal-oxide silicon (MOS) technology had not advanced to the point where it was practical to put large-value MOS resistors on the chip.

3. The binary cannot "deadhead" the line if the large-value resistors are external.

The TO-5 package was chosen because it is more easily welded to than the flat pack.

### System Check Using Many MOSFETs (Breadboard)

A representative encoding system was breadboarded. This system has about two-thirds the functional complexity of the IMP A and contains the circuits that produce the new functions to be used in IMPs F and G (16-level oscillator, A/D converter, "S-T" accumulators, etc.). It contains 127 binary blocks and 208 logic blocks with only 17 transistors. The breadboard was made with 8-pin "tube sockets" such that the production MOSFETs were "plugged" closed as soon as they arrived. Breadboarding with MOSFET blocks turned out to be much simpler than with conventional design. The electrical design and MOSFET performance were evaluated with this system. The system worked very well.

### Welded MOSFET Encoding System Package

The breadboard MOSFETs were removed and were welded into a package (delta pack), and complete system checks were performed with simulated experiment inputs. The package was potted. The welded modules were layed out and fabricated at GSFC. It was necessary concurrently

to lay out the welded modules and build a breadboard in order to meet the MOSFET schedule for test and evaluation.

The completely potted system, tested at GSFC for about 2 weeks, was very successful. The following tests were performed: initial magnetic checks, humidity, vibration, acceleration, 5 days of thermal cycling and soak in a vacuum, reentry, and final magnetic checks. The system was completely instrumented through all checks except magnetic, humidity, and acceleration.

At this writing (April, 1966) this MOSFET system is now on "burn-in" and is monitored 5 days a week for system performance. Over 11,500 hours have been logged with no failures. This is more than 3-1/2 million CAN hours or 28 million MOSFET hours without a failure.

A concurrent evaluation of individual MOSFET cans is being performed at GSFC. This evaluation is not yet completed but, to date, indicates good performance and quality control.

## CONCLUDING REMARKS

The evolution of the refined encoding system used on Super IMP from the relatively simple Explorer XII was a gradual one, with milestones occurring in the Ariel I (UK-1) and IMP A (Explorer XVIII) systems. Digital data processors, analog-to-digital converters, improved commutation, increased efficiency with crystal-controlled "digital oscillators," and a "30-day satellite clock" have been incorporated.

All the encoders mentioned were special purpose devices designed both electrically and mechanically at GSFC, although some of the actual flight units were fabricated and tested by private industry. All major improvements in concept were a result of close working relationships between the experimenters and the encoder designers, whereby the experimenters could work directly with the people who design and manufacture the flight hardware.

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