FACILITY FORM 602

N67-14216
(ACCESSION NUMBER)
(THRU)
149
(PAGES)
1
(CODE)
CR-80827
(NASA CR OR TMX OR AD NUMBER)
09
(CATEGORY)

COMPONENT MODELING HANDBOOK

R-843

JPL P.O. DB5-337357

June 1966

GPO PRICE $ ______

CFSTI PRICE(S) $ ______

Hard copy (HC) 4.00

Microfiche (MF) 1.00

ff 653 July 65

Prepared by

Kenneth O. King
Kenneth Gillett
William Libaw

PLANNING RESEARCH CORPORATION
LOS ANGELES, CALIF. WASHINGTON, D.C.

This work was performed for the Jet Propulsion Laboratory, California Institute of Technology, sponsored by the National Aeronautics and Space Administration under Contract NAS7-100.

TABLE OF CONTENTS

I. INTRODUCTION 1-1

II. DIODE MODELS 2-1

- A. Model Descriptions 2-1
- B. Model Performance 2-16
- C. Parameter Evaluation 2-25
- D. Diode Subroutine 2-31

III. TRANSISTOR MODELS 3-1

- A. Model Description 3-1
- B. Model Performance 3-4
- C. Parameter Evaluation 3-24
- D. Transistor Subroutine 3-33

IV. ZENER DIODE MODEL 4-1

- A. Model Description 4-1
- B. Model Performance 4-2
- C. Parameter Evaluation 4-4
- D. Zener Diode Subroutine 4-5

V. TUNNEL DIODE MODEL 5-1

- A. Model Description 5-1
- B. Model Performance 5-2
- C. Parameter Evaluation 5-4

VI. CONTROLLED RECTIFIER MODEL 6-1

- A. Model Description 6-1
- B. Model Performance 6-5
- C. Parameter Evaluation 6-28

VII. P-CHANNEL JUNCTION FIELD EFFECT TRANSISTOR MODEL 7-1

- A. Model Description 7-1
- B. Model Performance 7-4
- C. Parameter Evaluation 7-7

VIII. N-CHANNEL JUNCTION FIELD EFFECT TRANSISTOR MODEL 8-1

IX. NON-LINEAR INDUCTOR MODEL

A. Model Description

B. Model Performance

C. Parameter Evaluation

D. Non-Linear Inductor Subroutine

I. INTRODUCTION

This document contains nonlinear mathematical models for a number of electronic components. These models were developed for use with the TAG computer program for static and dynamic circuit analysis. Components modeled herein are the diode,transistor, zener diode, tunnel diode, controlled rectifier, junction field-effect-transistor, and saturating inductor.

In developing each model, consideration of device physics and of numerical circuit analysis have been omitted in the interest of simplicity and brevity. Rather, attention has been concentrated on describing the model and its performance and on evaluating model parameters. This should permit the user to "build" models of particular components and to understand how his models will perform. FORTRAN programs for some of the more widely used components are provided.

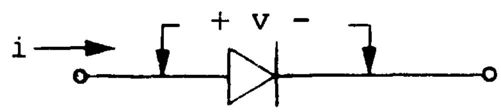
This present version of the modeling handbook does not attack certain important modeling problems. These include problems of model accuracy and suitability to different types of circuits, problems of parameter interdependence, temperature dependence and distribution, computer computation of model parameters from device measurement or specifications. As computer analysis of circuits grows in importance and use, these and other modeling problems should be studied and solved.

II. DIODE MODELS

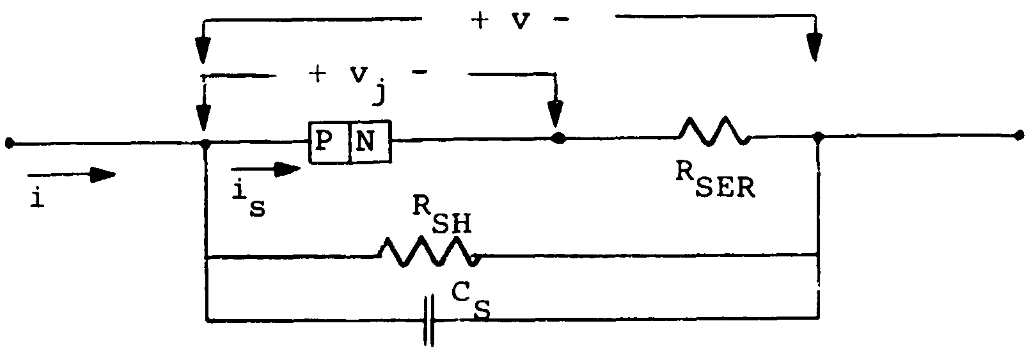
A. Model Descriptions

1. Classical Model

For a diode symbolized as follows:

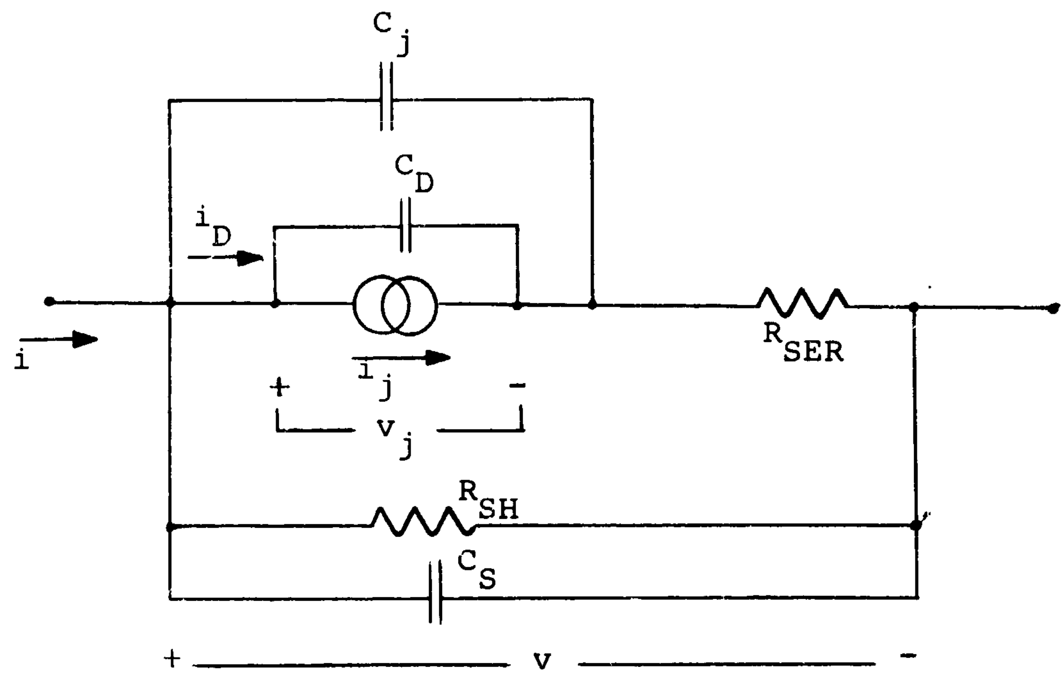


we may separate the behavior due to the junction and the diffusion of minority carriers from the behavior resulting from other phenomena and draw a model as follows:



Here the block PN symbol represents an idealized junction diode whose mode of conduction is solely diffusion.

The ideal diode may be further broken down into 3 components, a current generator, a junction capacitance and a diffusion capacitance to arrive at the following general model.



a. Static Model

1) Static model for junction (excluding R_{SER} and R_{SH}). The equation for i_j, which represents the static portion of the diffusion current, is as follows:

$$i_j = I_S\ (\exp(v_j/V_o) - 1)$$

where I_S and V_o are positive qualities and functions only of temperature; v_j is the voltage across the junction depletion region. This equation is plotted in the upper part of Figure 2-1.

I_S generally does not correspond to the actual diode leakage current but is often orders of magnitude smaller. I_S increases with temperature in such a manner as to

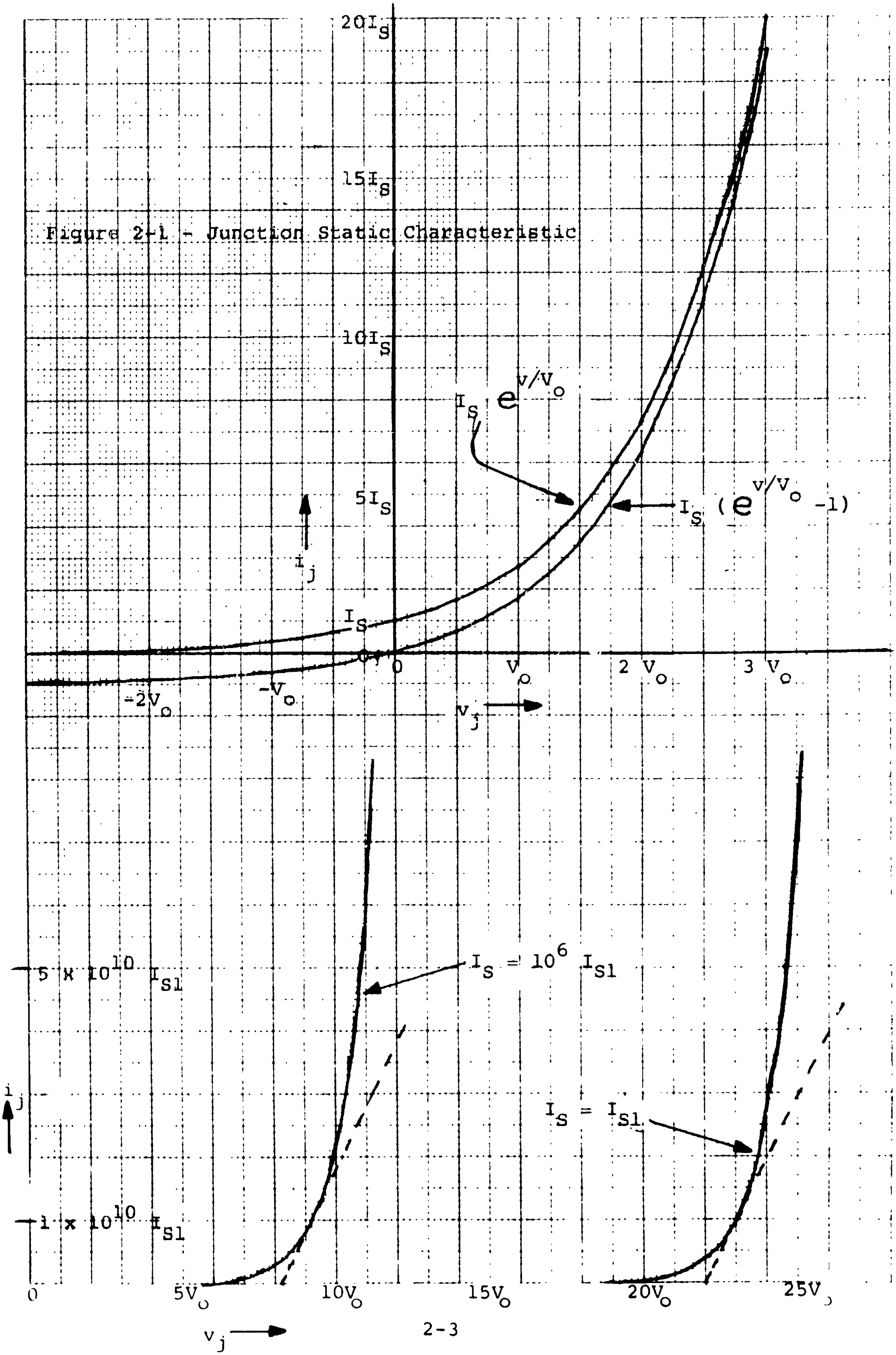


Figure 2-1 - Junction Static Characteristic make the voltage at a given current increase with temperature at a rate between 2 and 3 mv per degree C.

V_o lies between .026 and .052 volts at 25^{o}C and is proportional to temperature in degrees Kelvin.

Solving the i_j equation for voltage gives:

$$v_j = V_o \ln\left(1 + \frac{i_j}{I_S}\right)$$

It is evident that for $i_j \gg I_S$,

$$i_j \cong I_S \exp(v_j/V_o)$$

$$v_j \cong V_o \ln(i_j/I_S)$$

a) Dependence on I_S: At a given temperature, V_o can be regarded as having the same value for all diodes of a given type, with different values of I_S being responsible for different behavior. Thus, for V_o = .026 volts, at i_j = 1 ma, 2 silicon diodes of the same family might have I_S of $.1 \times 10^{-12}$ and $.2 \times 10^{-12}$, resulting in a v_j of .598 and .580, respectively. A germanium diode with the same V_o and i_j might have $I_S = .1\text{x}10^{-6}$ corresponding to a v_j of .239.

To illustrate the significance of I_S, curves for 2 diodes whose I_S's are in ratio of 10^6 are plotted in the bottom of Figure 2-1.

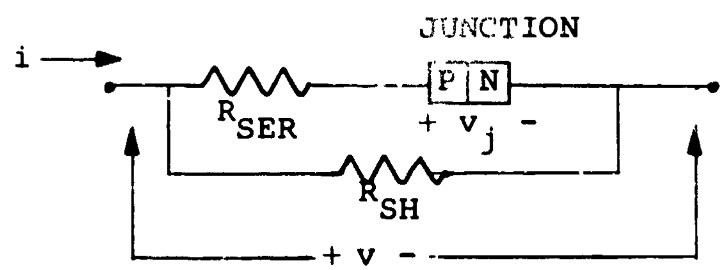
b) Small Signal Conductance: The slope of the $i_j - v_j$ curve, which represents the small signal conductance, g_D, is determined as follows:

$$g_D = \frac{di_j}{dv_j} = \frac{I_S}{V_o} e^{v_j/V_o} = \frac{i_j}{V_o} \frac{e^{v_j/V_o}}{e^{v_j/V_o} - 1}$$

For $i_j \gg I_S$, $g_D = \frac{i_j}{V_o}$

Thus, two vastly different diodes with equal V_o will have the same conductance at a given current, as shown in the bottom of Figure 2-1.

2) Static Additions to Junction Model - In the interests of more accurate modeling, it is often necessary to add a small series resistor, significant at large forward currents, and a large shunt resistor, significant at most reverse voltages. Thus the model symbols and equations become:



For positive currents, $v \cong v_j + iR_{SER}$

For negative voltages, $i \cong \frac{v}{R_{SH}} - I_S$

b. Diode Model, Dynamic Components

1) Junction Capacitance (Barrier Capacitance, Depletion Layer Capacitance) - The junction capacitance is a non-linear function which varies with the junction voltage. Its model equation is as follows.

$$C_j = \frac{K}{(V_K - v_j)^N}$$

v_j = voltage across diode junction depl. region

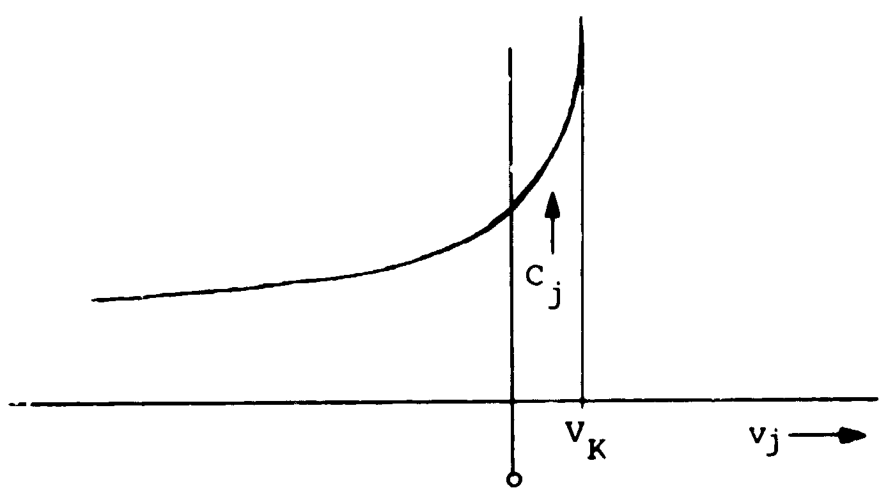
V_K = contact potential, $\approx .7$ to 1.0 for S_i @ 25^oC

$V_K >$ any operating v_j, otherwise $C \rightarrow \infty$

V_K is a function of doping, etc.

K = proportionality constant that determines the magnitude of C

N = junction grading constant; .5 for abrupt junction, .33 for uniformly graded junction.



2) Diffusion Time Constant (or Diffusion Capacitance) - In the classical model, the diffusion time constant, τ, is used to represent the charge storage behavior of the diode. τ is the proportionality constant between the stored charge and the diffusion current, i_D, through the diode.

The effects of the diffusion time constant can be represented in the circuit model as a non-linear diffusion capacitance, C_D, where

$$C_D = \tau g_D = \tau \frac{di_j}{dv_j} \cong \tau \frac{i_j}{V_o}$$

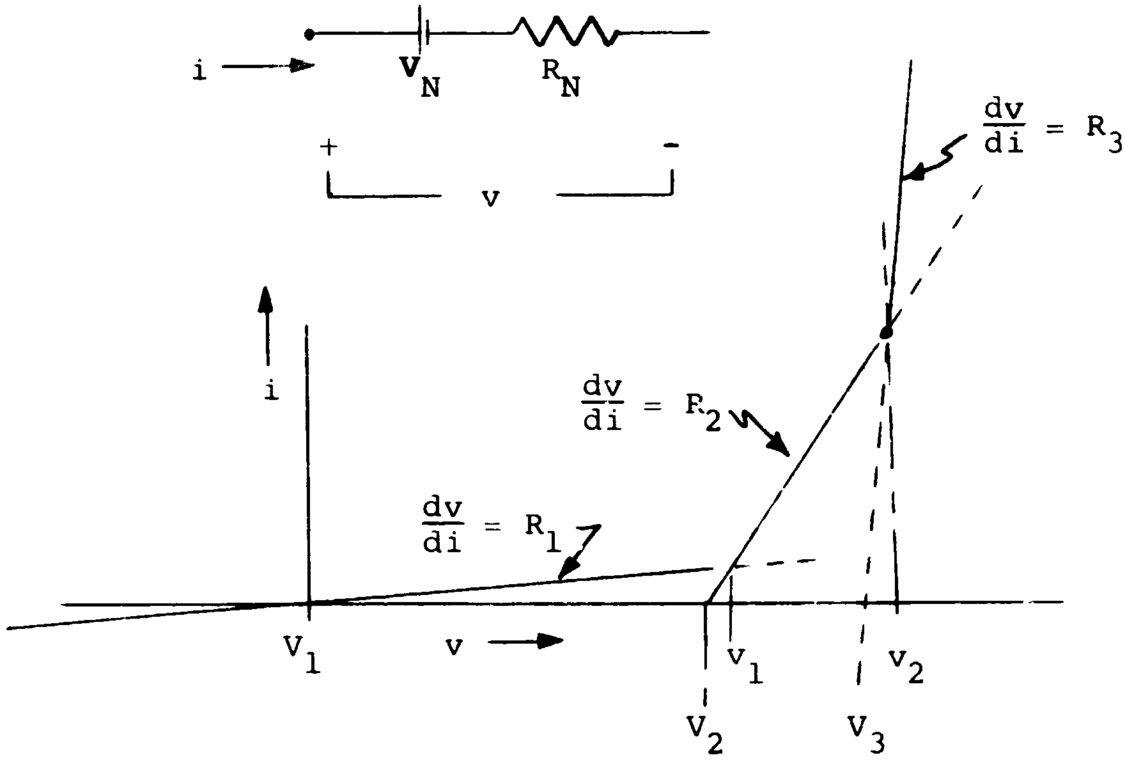
and g_D is the small signal conductance or slope of the i_j, v_j characteristic.

3) Case Capacitance - There is usually a small fixed capacitance associated with the diode case. This is shown as C_S in the model.

2. Piece-wise Linear Classical Model

Linear segmented models are less accurate, but may permit faster computation.

a. Static Model - Here the junction current generator and the series and shunt resistors are replaced by the series combination of a voltage source and a resistor.

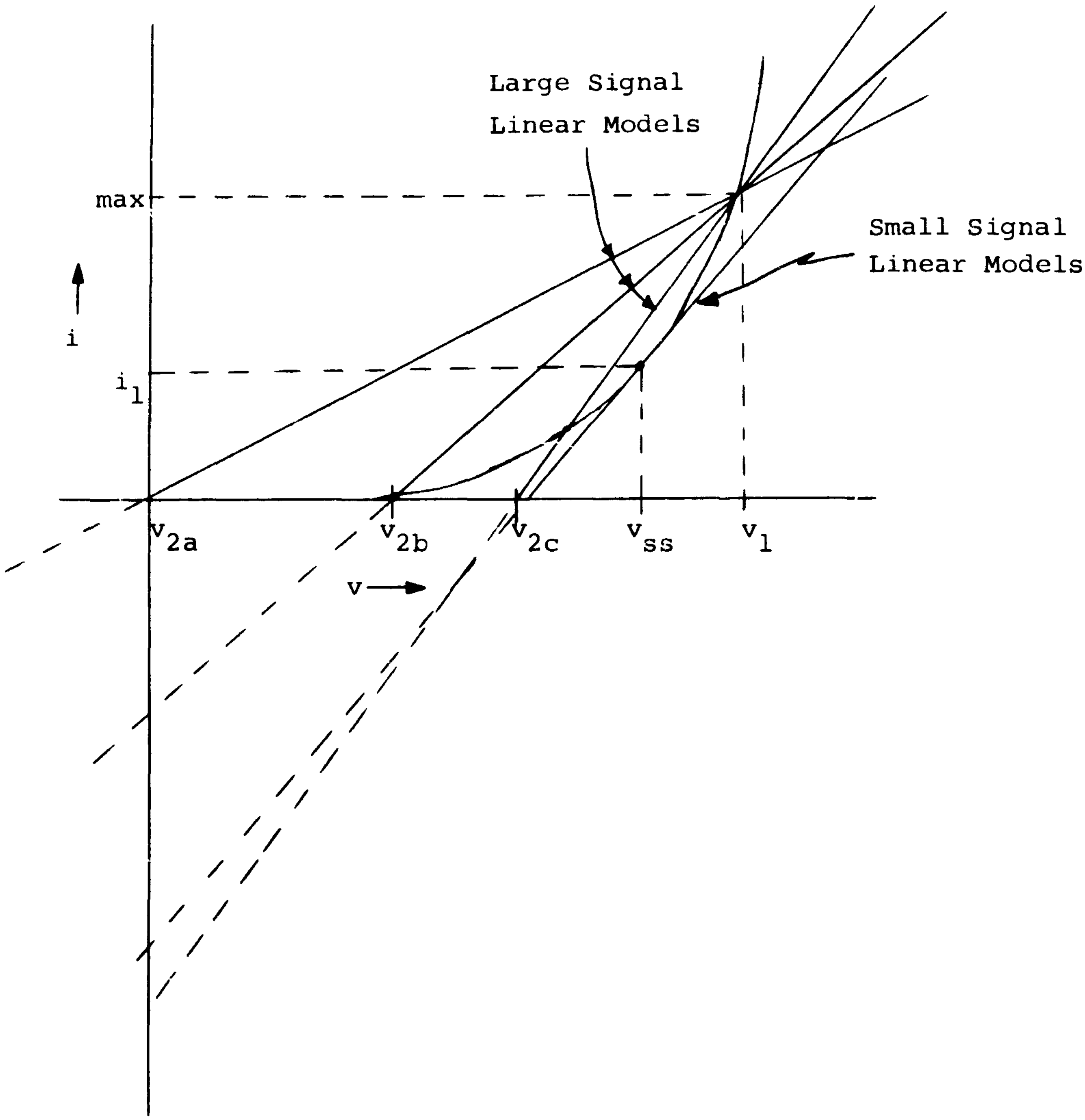


$$i = \frac{v - V_1}{R_1} \qquad \text{for } v \leq v_1$$

$$i = \frac{v - V_2}{R_2} \qquad \text{for } v_1 < v \leq v_2$$

$$i = \frac{v - V_3}{R_3} \qquad \text{for } v_2 < v \leq v_3$$

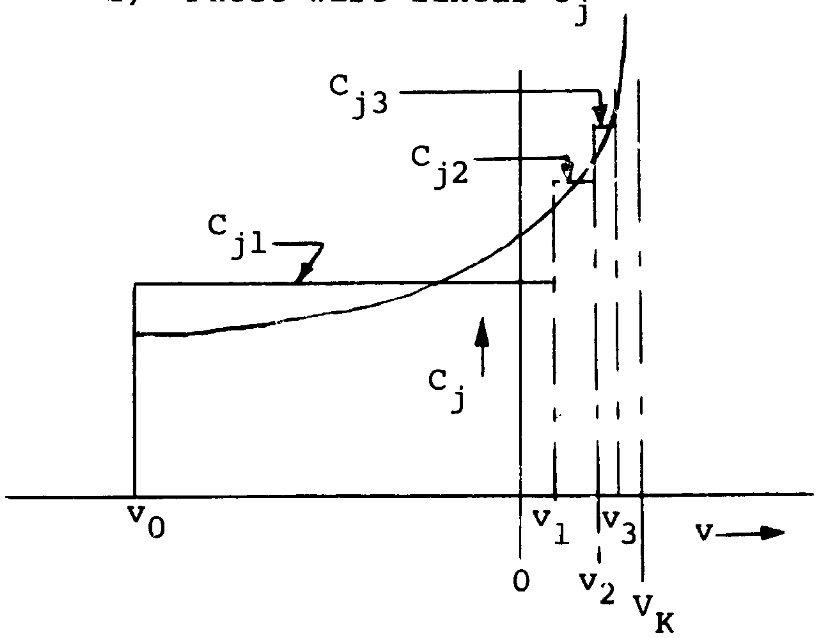
1) Linear Models - The limiting case of the piece-wise linear model is the one-piece linear model. Several such models are shown graphically below.



The linear models may be divided into two groups, the large signal linear models and the small signal linear models. For the large signal models, the linear approximation is selected to fit <u>two points</u> on the curve. For the small signal model, the linear approximation is made to fit the <u>slope</u> of the curve at a point.

b. Dynamic Model

1) Piece-wise linear C_j



$$C_{j1} = \frac{Q_{01}}{V_0 - V_1}$$

$$Q_{01} = \int_{-V_0}^{-V_1} C\, dv = K \int_{-V_0}^{-V_1} (V_K - v)^{-N}\, dv$$

$$Q_{01} = K \left. \frac{(V_K - v)^{-(N-1)}}{1 - N} \right|_{-V_0}^{-V_1}$$

NOTE: Piece-wise linear (1 segment) C can be used with basic non-linear diode, as C_j non-linearity is not of first-order importance.

2) Piece-wise linear C_D

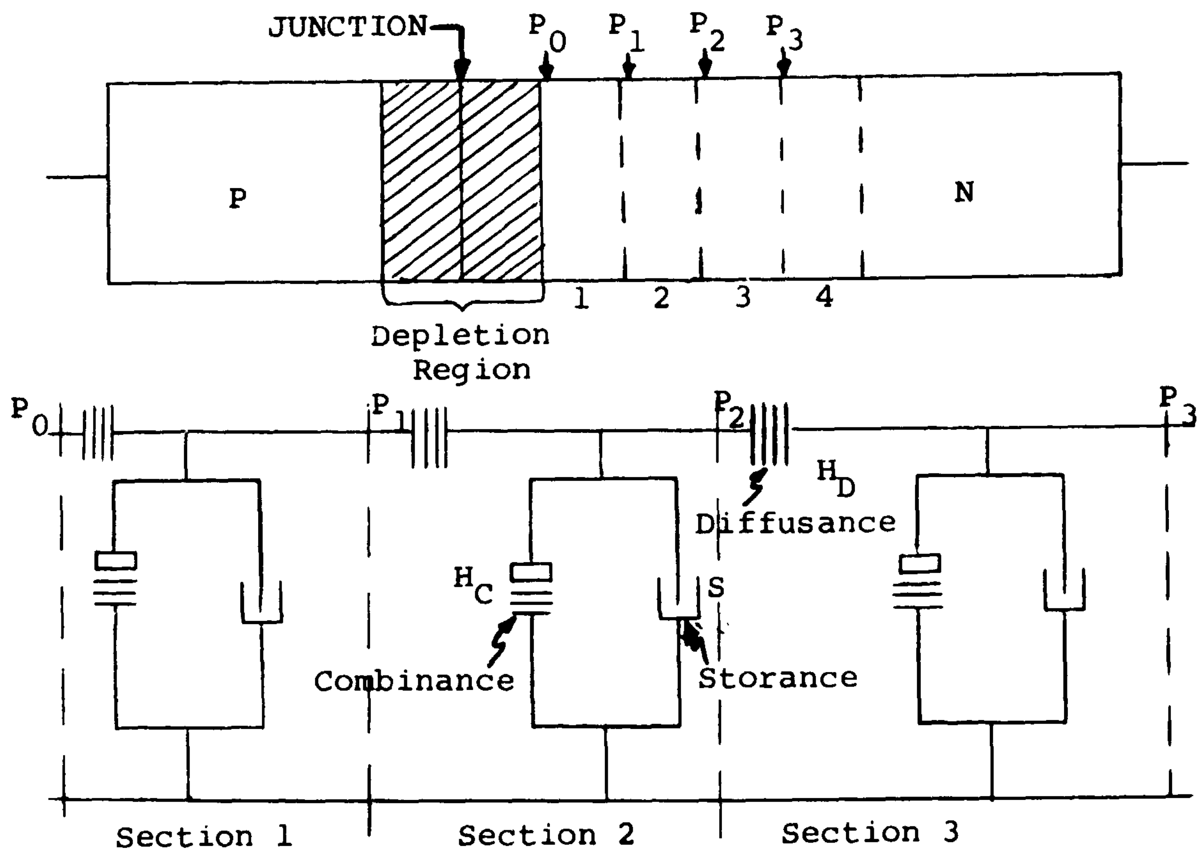
$$C_{D1} = \frac{\tau}{R_1} \quad \text{for } v \leq v_1$$

$$C_{D2} = \frac{\tau}{R_2} \quad \text{for } v_1 < v \leq v_2$$

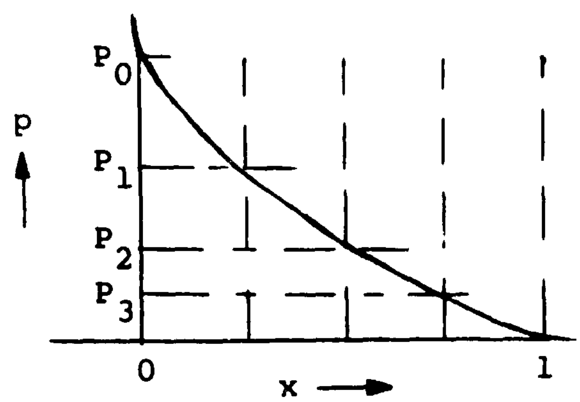
$$C_{D3} = \frac{\tau}{R_3} \quad \text{for } v_2 < v \leq v_3$$

3. Linvill Lumped Diffusion Model

Here the distributed properties of the semiconductor are lumped for sections and represented by diffusances, combinances, and storances. These elements relate to excess carrier density, p, and current, i.



$$p_o = p_s \left(e^{v/V_o} - 1 \right)$$

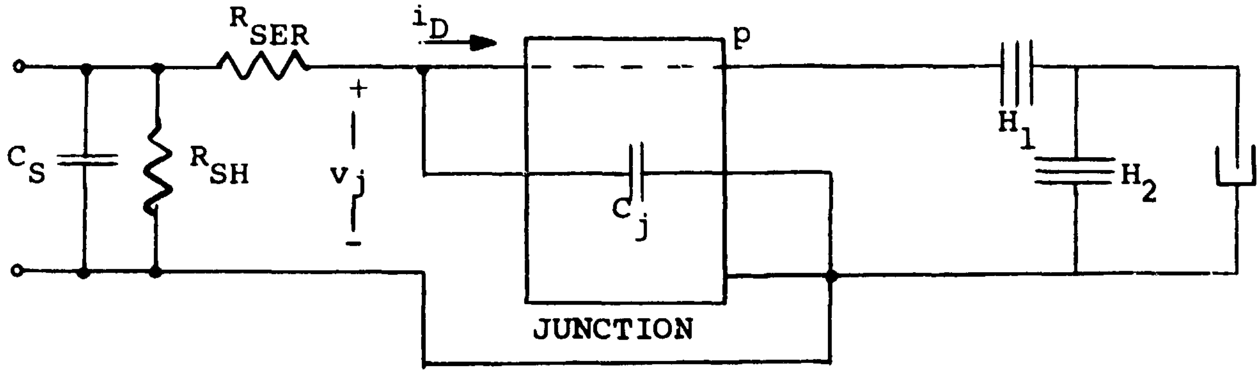


For a diffusion diode, the continuous properties of recombination, charge storage and diffusion are replaced with lumped elements called combinance, storance, and diffusance respectively. These elements are analagous to conductances and capacitances; they differ from the normal electrical elements in that they relate current and excess minority carrier density rather than current and voltage. The word "carriance" can be coined as an analog for the electrical "admittance".

It is possible to develop a variety of lumped models depending on how many pi, tee, or L sections are used. Here we will describe the simplest lumped model that is significantly different than the classical model. This is a single section, 3 carriance model in the form of an L, here called the "single-L".

In contrast to the non-linear diffusion capacitance of the classical model, the storances and the other carriances are all linear elements.

The schematic diagram for this model is as follows, where p represents excess carrier density



Excess carrier density is related to junction voltage as follows:

$$p = P_S \left(e^{v_j/V_o} - 1 \right)$$

where P_S is the saturation excess carrier density. The steady state current,

$$i_{DC} = p \left(\frac{H_1 \ H_2}{H_1 + H_2} \right)$$

thus

$$i_{DC} = P_S \left(\frac{H_1 \ H_2}{H_1 + H_2} \right) \left(e^{v_j/V_o} - 1 \right)$$

This permits identification of the Linvill model parameters in terms of the Ebers-Moll parameters,

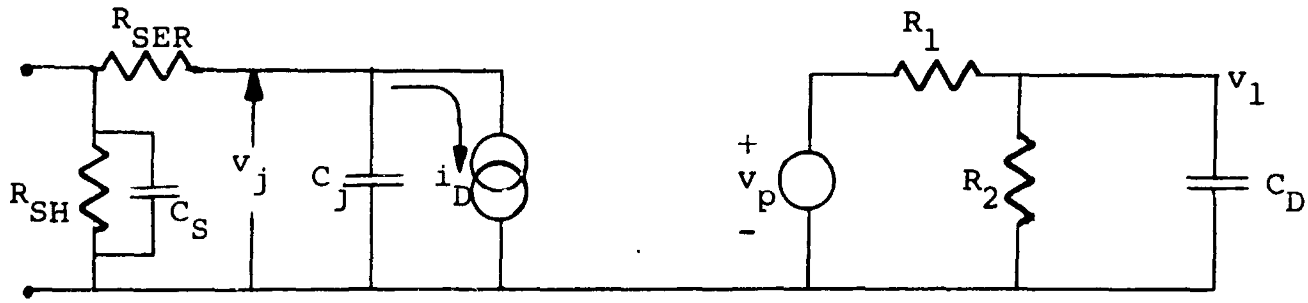
$$I_S = P_S \left(\frac{H_1 \ H_2}{H_1 + H_2} \right)$$

As the carriance level (similar to admittance or impedance level) is both unknown and unimportant for external purposes, the term

$$\frac{H_1 \ H_2}{H_1 + H_2}$$

can be arbitrarilly set equal to 1. This makes P_S numerically equal to I_S.

The diagram above is not a complete and clear model. Therefore it is replaced by the circuit model below, which uses R's and C's to model the carriances and uses 2 generators to make explicit the behavior of the junction in converting between voltage and excess carrier density.



The equations for the two generators are:

$$v_p = V_{ps}\,(e^{v_j/V_o} - 1)$$

$$i_D = (v_p - v_1)/R_1$$

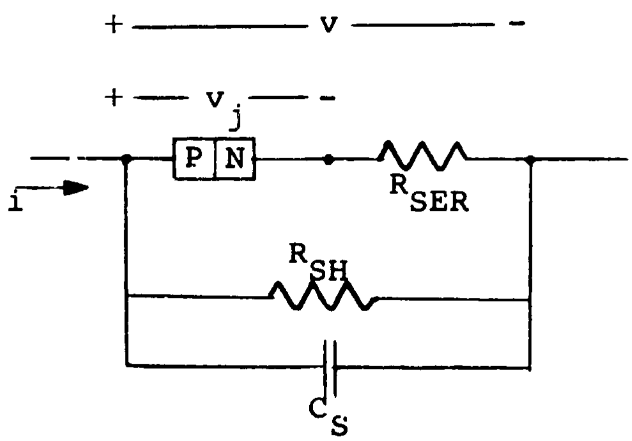
By setting $R_1 + R_2 = 1$, $V_{ps} = I_S$.

Defining the diffusion time constant, $\tau = R_2 C_D$.

With one exception, all the parameters are defined similarly to those of the classical model. The exception is the value of R_2, which is generally between 0.5 and 1.0, depending on the diode type.

B. Model Performance

1. Classical Diode



a. Static Forward Current: For forward current, the equations are simplified with very little error by assuming R_{SH} to be infinite.

Then $i \cong i_j$

and $v \cong V_o \ln\left(1 + \frac{i}{I_S}\right) + i\, R_{SER}$.

b. Static Reverse Current: For reverse voltage, the equations are simplied with very little error by assuming R_{SER} to be zero.

Then $v \cong v_j$

and $i \cong I_S \;(e^{v/V_o} - 1) + \frac{v}{R_{SH}}$

c. Dynamic Forward Step Response - The voltage response of the diode to an applied step of forward current can be approximated by considering it to consist of 2 sequencial phases. During the first or delay phase, the voltage rises almost linearly due to the junction and stray capacitance, the time constant or diffusion capacitance having little effect. During the second or charge phase, the voltage rises very little and thus the junction and stray capacitances have little effect, but the diffusion capacitance charges for a period about 2 time constants.

d. Dynamic Reverse Step Response - The voltage response can again be approximated by 2 phases, a storage time and a recovery time. During the storage time, the diffusion capacitance is dominant and the time constant governs the response as follows:

$$t_S = \tau \ln \frac{i_F - i_R}{-i_R}$$

During the storage time the voltage changes very little. During the recovery time, the voltage falls almost linearly due to the junction and stray capacitance, the diffusion capacitance playing almost no part.

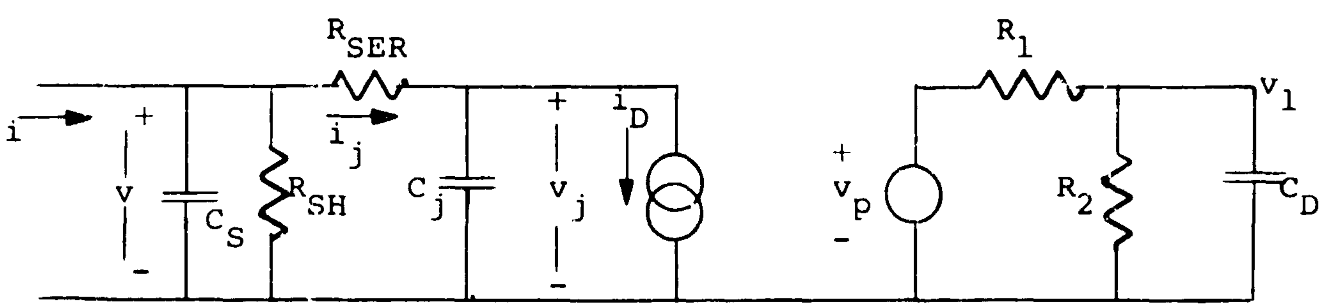
2. Lumped L Model

a. Static Behavior - The static behavior of this model is essentially the same as that of the classical model, where

$$I_S = V_{ps}/(R_1 + R_2)$$

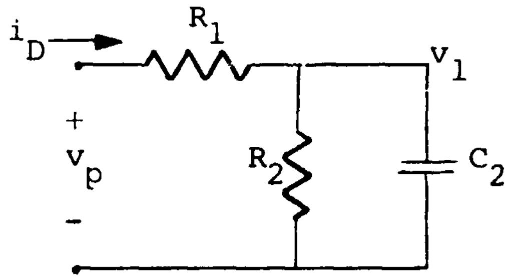
and $$R_1 + R_2 = 1 \text{ ohm.}$$

b. Dynamic Behavior - The dynamic performance differs from the classical model performance in the relationship between v_j and i_D. To analyze this relationship, we replace the complete circuit model,

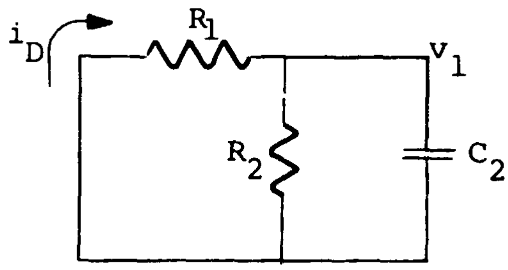


with 2 regional models as follows.

The first model is applicable when v_j is positive and uses no approximations.



The second model is applicable when v_j is not positive. It approximates a very small negative v_p with a short circuit as follows.



The response of the entire model to large steps of input voltage with a series input resistor is approximated analytically by these regional models if it is assumed that the diode forward voltage drop is small and the junction and stray capacitances are negligable. It is the turn-off response that is of primary interest. Thus we assume the diode to be in steady state with a forward current i_{DF} when the current is step changed to i_{DR}. The differential equations for v_p and v_1 can be written by inspection from the first or forward model.

$$v_p = (i_{DF} - i_{DR})\, R_2\, e^{-t/R_2C} + i_{DR}\,(R_1 + R_2)$$

$$v_1 = v_p - i_{DR}\, R_1$$

The v_p equation can be solved for the time required to reduce v_p to zero, the storage time,

$$t_S = R_2C\left[\ln \frac{i_{DF} - i_{DR}}{-i_{DR}} + \ln \frac{R_2}{R_1 + R_2}\right].$$

Let $R_1 + R_2 \equiv 1$ and $R_2C \equiv \tau$

then

$$t_S = \tau\left[\ln \frac{i_{DF} - i_{DR}}{-i_{DR}} + \ln R_2\right]$$

As v_p is reduced from a positive value to zero at $t = t_S$, and recalling from the model description that

$$v_p = V_{ps}\,(\exp(v_j/V_o) - 1),$$

it is evident that v_j switches from a positive value to a zero value. At this point in time, we switch to the second equivalent circuit.

Here, the diode diffusion current, i_D, is no longer a function of the external circuit. Instead it decays to zero strictly as a function of the internal parameters. We determine this current fall time by defining a new time variable, and a new current variable,

$$t' = t - t_S; \text{ and } i_{DRR}$$

and noting that $v_1 = -i_{DRR}R$ @ $t' = 0$,

then

$$i_{DRR} = \frac{-v_1}{R_1} = i_{DR}\, e^{-t'/R_1\tau} .$$

The time for the current to fall to $-.1\ i_F$,

$$t'_{IF1} = R_1 \tau \ln \frac{i_R}{-.1 i_F}$$

$$t'_{IF1} = (1 - R_2)\tau(\ln \frac{-i_R}{i_F} + 2.3)$$

The time for the current to fall to $.1 i_R$,

$$t'_{IF2} = R_1 \tau \ln \frac{i_R}{.1 i_R}$$

$$t'_{IF2} = 2.3\ (1 - R_2)\tau$$

The general equations for storage time and current fall time for the family of single-L models were developed above. To permit comparison between members of this model family, other models, and actual diodes, it is desirable to normalize the equations. This normalization is best done by equating the storage time, t_S, at a particular value of $-i_{DR}/i_{DF}$. For convenience here, we chose $-i_{DR}/i_{DF} = .2$, where $t_S = t_{S.2}$ for each of the models.

To do this we solve the storage time equation for the value of τ that will result in a storage time of $t_{S.2}$ at $-i_R/i_F$ equal to .2.

$$t_{S.2} = \tau \ln \frac{1 + .2}{.2} + \tau \ln R_2$$

$$t_{S.2} = 1.79\,\tau + \tau \ln R_2$$

$$\tau = t_{S.2}/(1.79 + \ln R_2)$$

To obtain the corresponding value of C,

$$C = \frac{\tau}{R_2}$$

$$C = t_{S.2}/(1.79 + \ln R_2)(R_2)$$

Using these equations, we evalue the model parameters for several values of R_2

R_2	R_1	τ	C
1.0	0	.559 $t_{S.2}$	.559 $t_{S.2}$
.9	.1	.594 $t_{S.2}$	.660 $t_{S.2}$
.8	.2	.639 $t_{S.2}$	.798 $t_{S.2}$
.7	.3	.696 $t_{S.2}$	.994 $t_{S.2}$
.6	.4	.782 $t_{S.2}$	1.304 $t_{S.2}$
.5	.5	.912 $t_{S.2}$	1.82 $t_{S.2}$
.4	.6	1.292 $t_{S.2}$	3.23 $t_{S.2}$
.3	.7	1.70 $t_{S.2}$	5.52 $t_{S.2}$

Figure 2-2 shows storage time vs. $(i_{DF}-i_{DR})/-i_{DR}$ for the above 8 models. As shown, these curves are straight lines on semi-log paper. The time, after t_S, for current to fall to $-.1i_{DF}$, t_{IF1}, may be displayed as straight lines on semi-log paper by plotting against $-i_{DR}/i_{DF}$, as shown in the same figure. The single-L model with $R_2 = 1.0$ has equations and performance that are exactly equivalent to those of the classical model. It is apparent for these models, that increasing R_1 decreases the storage time for large i_{DR}, and increases the time after t_S for the current to fall to $.1i_{DF}$.

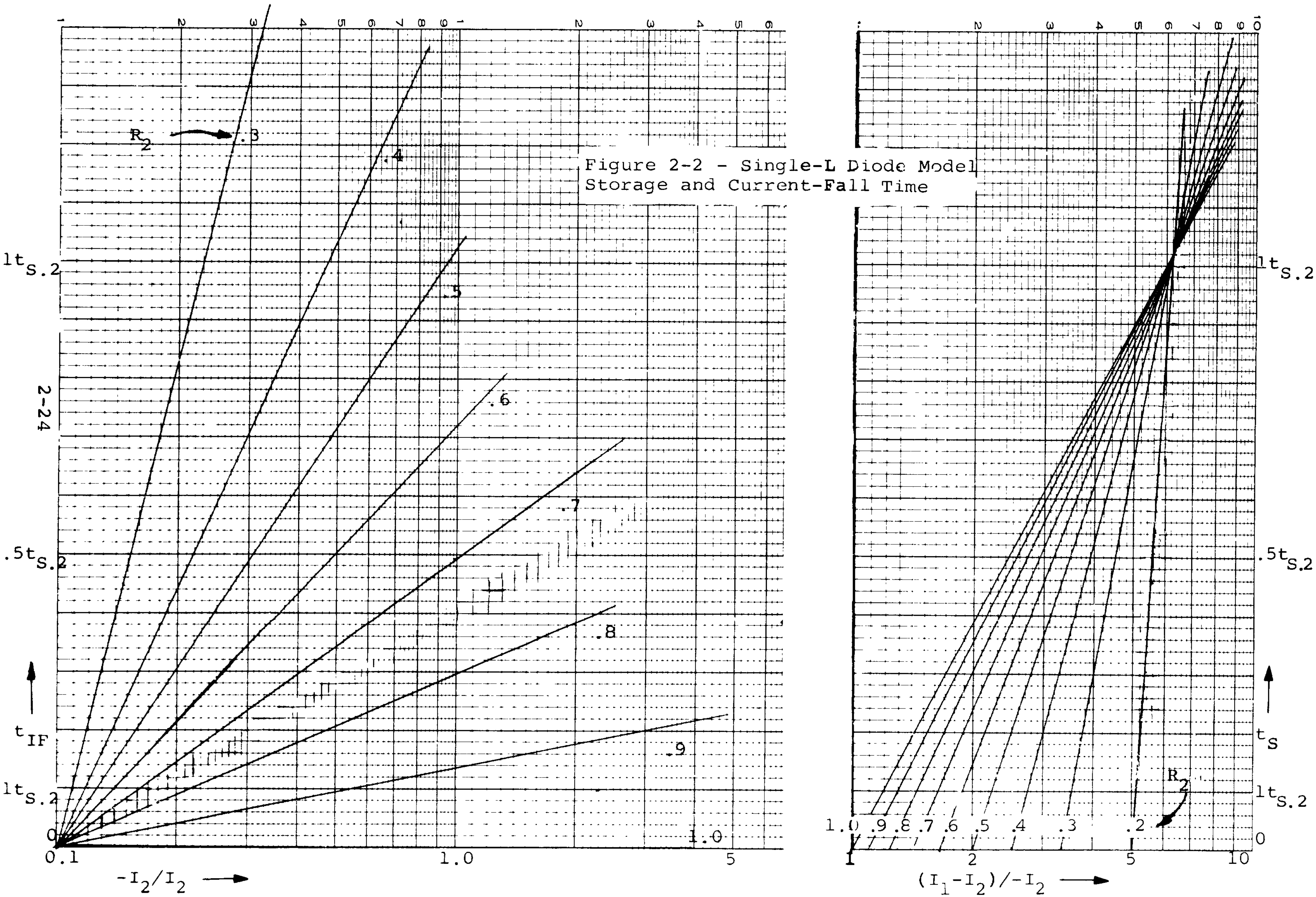


Figure 2-2 - Single-L Diode Model Storage and Current-Fall Time

C. Parameter Evaluation

The models described are not, in general, accurate over the entire working range of the diodes. Thus, it is usually necessary to generate the parameter values for a specific operating range of voltages and currents. For this reason, and also because of the resultant mathematical problems, the suggested technique for parameter evaluation is not to make N operating point measurements and solve the resultant equations for the N parameter values. Rather it is proposed to make suitable approximations where possible to simplify the equations for the parameters.

1. Classical Model

a. V_o: V_o should be determined from 2 data points, at forward currents much smaller than i_{MF}, the maximum forward current used for the diode. Calling these points i_1, v_1 and i_2, v_2, and assuming that the voltage drop across R_{SER} is negligable, then from the junction current equation,

$$V_o = (v_1 - v_2)/\ln (i_1/i_2)$$

where i_1 and i_2 are assumed to be much larger that I_S.

b. I_S: I_S can be obtained from one of the data point equations and checked at the other.

$$I_S = i_1 \exp(-v_1/V_o)$$

check $i_2 = I_S \exp(v_2/V_o)$

c. R_{SER}: R_{SER} can now be obtained from the i_{MF}, v_{MF} data point.

$$R_{SER} = \frac{1}{i_{MF}} \left(v_{MF} - V_o \ln \frac{i_{MF}}{I_S} \right)$$

d. R_{SH}: R_{SH} can be obtained from the data point for the maximum reverse voltage used, i_{MR}, and v_{MR}.

$$R_{SH} = \frac{v_{MR}}{I_S + i_{MR}}$$

e. V_K, K, N: These parameters, used in the junction capacitance equation, should be evaluated as follows.

V_K: Although V_K may vary with the diode type and with temperature, it is suggested that $V_K = 1.0$ volt be used, for simplicity, for all diodes.

K: Use the measured small-signal capacitance at zero volts, C_O, with the junction capacitance equation to obtain $K = C_o$.

N: Use the measured small-signal capacitance @ v_{MR}, C_{MR}, with the junction capacitance equation to obtain

$$N = \frac{\ln (K/C_{MR})}{\ln (V_K - v_{MR})}$$

f. C_S: If C_S is known, it should be subtracted from the data points used in the previous section to obtain the junction capacitance parameters.

g. τ: τ is obtained from storage time data. If only a single data point in the range of use, t_S at i_F and i_R, is available, then

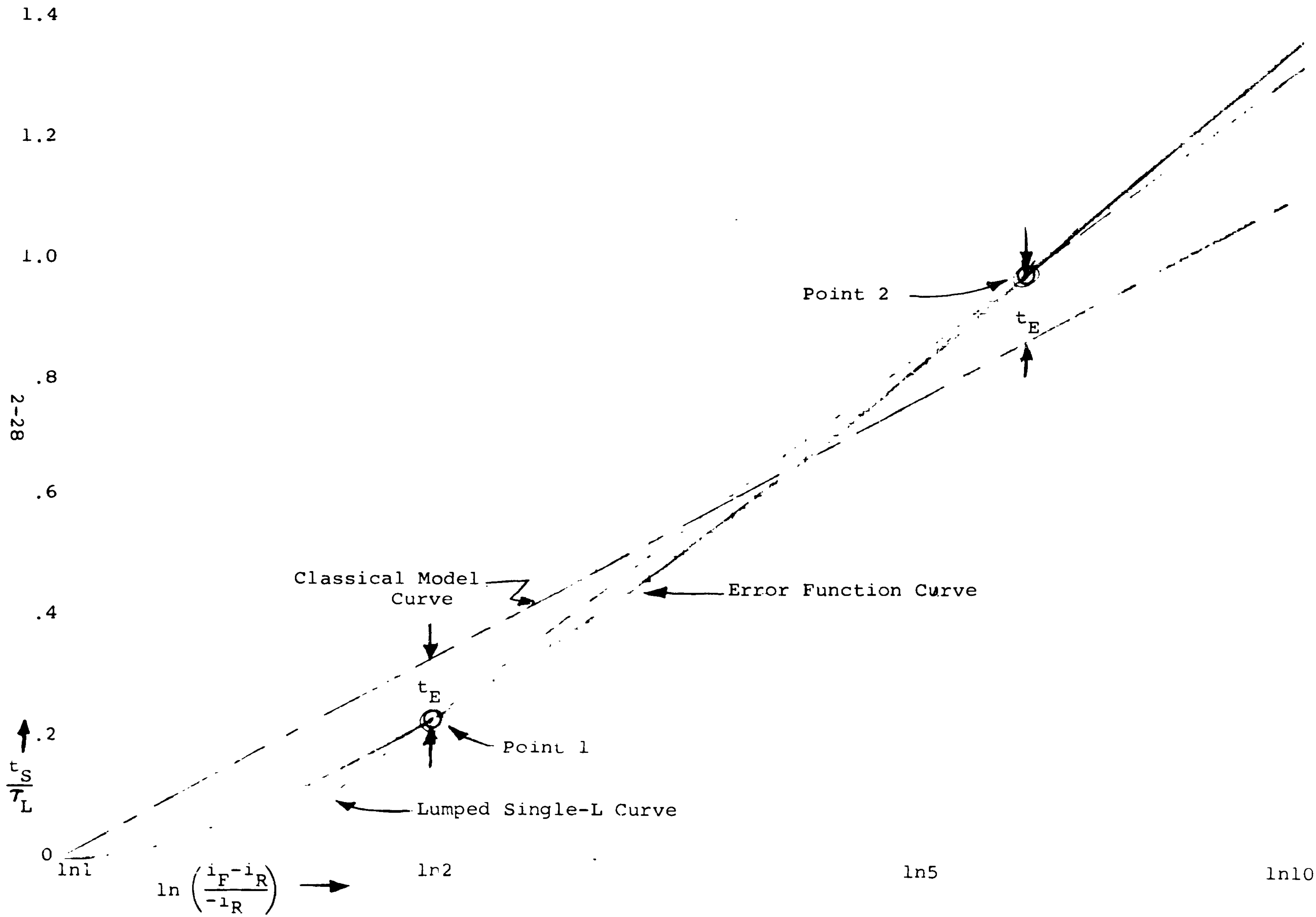
$$\tau = t_S/\ln\left(\frac{i_F - i_R}{-i_R}\right)$$

If it is possible to pick 2 data points in the range of use, then the first, t_{S1} @ i_{F1} and i_{R1}, should be chosen at a small ratio i_{F1}/i_{R1}, and the second, t_{S2} @ i_{F2} and i_{R2}, should be chosen at a large ratio i_{F2}/i_{R2}. Consider the 2 data points plotted an a graph of

$$t_S \text{ vs. } \ln\left(\frac{i_F - i_R}{-i_R}\right).$$

For most diodes, data points will fall on a curve somewhere between a classical model straight line through the origin and an Error Function concave curve. The curves are shown in Figure 2-3.

To fit a classical model τ to the 2 data points, set the positive time error at point 1, t_{E1}, equal to the negative time error at point 2, t_{E2}. Thus, the equations for the 2 points are


1.4
1.2
1.0
.8
.6
.4
.2
0
$\frac{t_S}{\tau_L}$
Point 2
t_E
Classical Model Curve
Error Function Curve
t_E
Point 1
Lumped Single-L Curve
ln1
ln2
ln5
ln10
$\ln\left(\frac{i_F - i_R}{-i_R}\right)$

$$t_{S1} + t_E = \tau \ln \frac{i_{F1} - i_{R1}}{-i_{R1}}$$

$$t_{S2} - t_E = \tau \ln \frac{i_{F2} - i_{R2}}{-i_{R2}}$$

Solving for τ,

$$\tau = (t_{S1} + t_{S2}) \Big/ \left(\ln \frac{i_{F1} - i_{R1}}{-i_{R1}} + \ln \frac{i_{F2} - i_{R2}}{-i_{R2}} \right)$$

The error, t_E, may now be calculated and checked with the above equations.

2. Lumped Single-L Model

With the exception of storage time parameters, the parameters of this model are very similar to those of the classical model.

a. V_o: Identical to classical model.

b. V_{ps}: Set V_{ps} equal numerically to I_S in the classical model.

c. R_{SER}: Identical to classical model.

d. R_{SH}: Identical to classical model.

e. V_K, K, N: Identical to classical model.

f. C_S: Identical to classical model.

g. R_1, R_2, C_D: These parameters control the storage time and current-fall time behavior. Assume 2 data points such as those described for the classical model. The Single-L model parameters are evaluated to fit both points exactly as shown in the storage time curve previously described.

To evaluate the parameters, note first that R_1 and R_1 are defined such that $R_1 + R_2 = 1$.

Next, to simplify the notation, define

$$x = \ln \frac{i_F - i_R}{-i_R}$$

Then determine x_o, the horizontal axis intercept of the straight line through the points t_{S1}, x_1 and t_{S2}, x_2. At this point, t_S equals zero for the model.

$$x_o = x_1 - \left(\frac{x_2 - x_1}{t_{S2} - t_{S1}}\right) t_{S1}$$

Then, from the storage time equation,

$$t_S = R_2 C \ (x + \ln R_2),$$

solve for R_2:

$$o = R_2 C \ (x_o + \ln R_2)$$

$$\ln R_2 = -x_o$$

$$R_2 = \exp(-x_o)$$

Next, using the same equation with point 2, solve for C:

$$t_{S2} = R_2 \; C \; (x_2 - x_o)$$

$$C = \frac{t_{S2}}{R_2 \; (x_2 - x_o)}$$

Lastly, solve for R_1:

$$R_1 = 1 - R_2 \; .$$

D. Diode Subroutine

```
      SUBROUTINE DIODE (VFD,FID,CTD,DATA,DIDI,LALGFT,KTDC)
      SUBROUTINE DIODE (VFD,FID,CTD,DATA,DIDI,LALGFT,KTDC)
C     CLASSICAL NON-LINEAR DIODE MODEL
C     ARG(1)  = VFD      DIODE TERMINAL VOLTAGE (PLUS FOR P POSITIVE)
C     ARG(2)  = FID      DIODE BRANCH CURRENT (PLUS FOR FLOW P TO N)
C     ARG(3)  = CTD      DIODE TOTAL TERMINAL CAPACITANCE
C     ARG(4)  = DATA     DIODE PARAMETER ARRAY
C     ARG(5)  = FIDI     DIODE INITIAL CURRENT
C     ARG(6)  = LALGFT   FLAG = 1 ON FIRST PASS THROUGH SUBROUTINE
C     ARG(7)  = KTDC     FLAG SET TO 1 FOR DC CASE , TO 0 FOR TRANSIENT
C     BULK RESISTANCE MUST BE INCLUDED IN EXTERNAL CIRCUIT IF DESIRED
C     DATA(1) = IS       REVERSE SATURATION CURRENT
C     DATA(2) = GL       REVERSE LEAKAGE CONDUCTANCE
C     DATA(3) = TAU      CHARGE RECOVERY TIME CONSTANT
C     DATA(4) = VK       DIODE CONTACT POTENTIAL
C     DATA(5) = N        JUNCTION GRADING CONSTANT
C     DATA(6) = K        DEPLETION CAPACITANCE CONSTANT
C     DATA(7) = CSD      STRAY AND CASE CAPACITANCE
C     DATA(8) = VO       THERMAL POTENTIAL KT/Q
      DIMENSION DATA(8)
      IF(KTDC-1) 10,1,1
    1 IF(LALGFT-1) 5,5,10
C     ID = ID(INITIAL)
    5 FID=FIDI
      GO TO 15
C     ID = VD*GL + IS*(EXPF(VD/VO)-1)
   10 FIC=DATA(1)*(EXPF(VFD/DATA(8))-1.)
      FID=FIC+VFD*DATA(2)
      IF(KTDC-1) 11,15,15
C     CD = CSD + K/((VK-VD)**N) + (TAU/VO)*(ID+IS)
   11 CTD=DATA(7)+DATA(6)/((DATA(4)-VFD)**DATA(5))+(DATA(3)/DATA(8))
     1*(FIC+DATA(1))
   15 CONTINUE
      RETURN
      END(1,0,0,0,0,0,1,0,0,0,0,0,0,0,0)
```

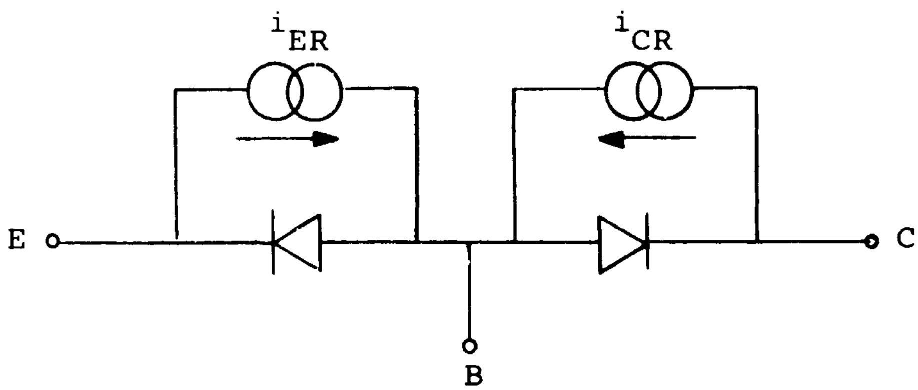
III. TRANSISTOR MODELS

A. Model Description

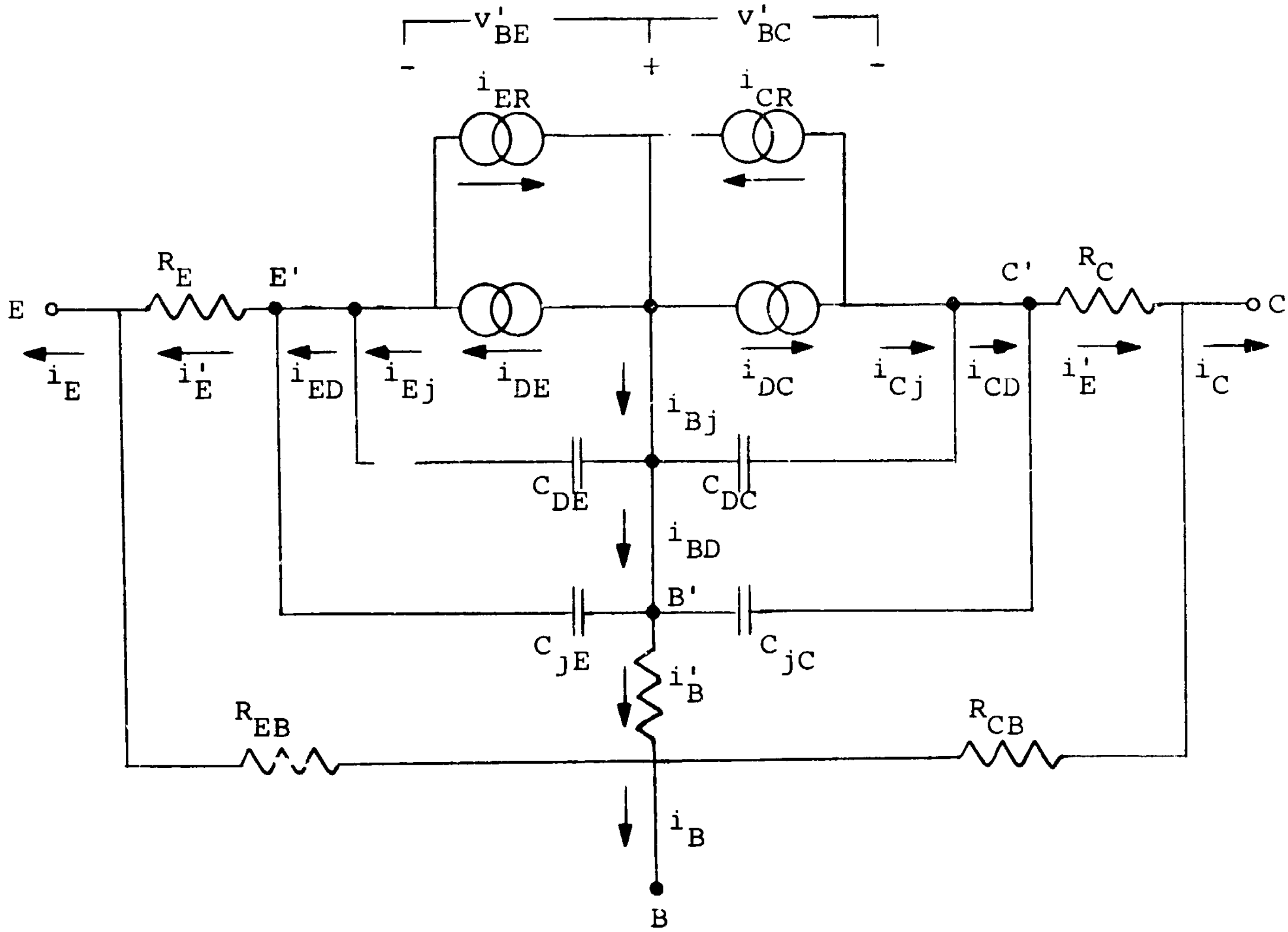
1. Ebers-Moll Transistor Model

The Ebers-Moll transistor model is strongly based on the diode model. It views the transistor as composed of an emitter diode and a collector diode with current generators across each diode to represent the transportation of current carriers through the base region.

A general schematic of the model is as follows.



The character of the diodes has been described previously. Each of the 2 current generators develops a current proportional to the junction current of the other diode. Thus $i_{CR} = \alpha_N i_{Ej}$ and $i_{ER} = \alpha_I i_{Cj}$, where the alphas are proportionality constants representing the fraction of emitter junction current reaching the collector and vice versa. The detailed model is shown below.



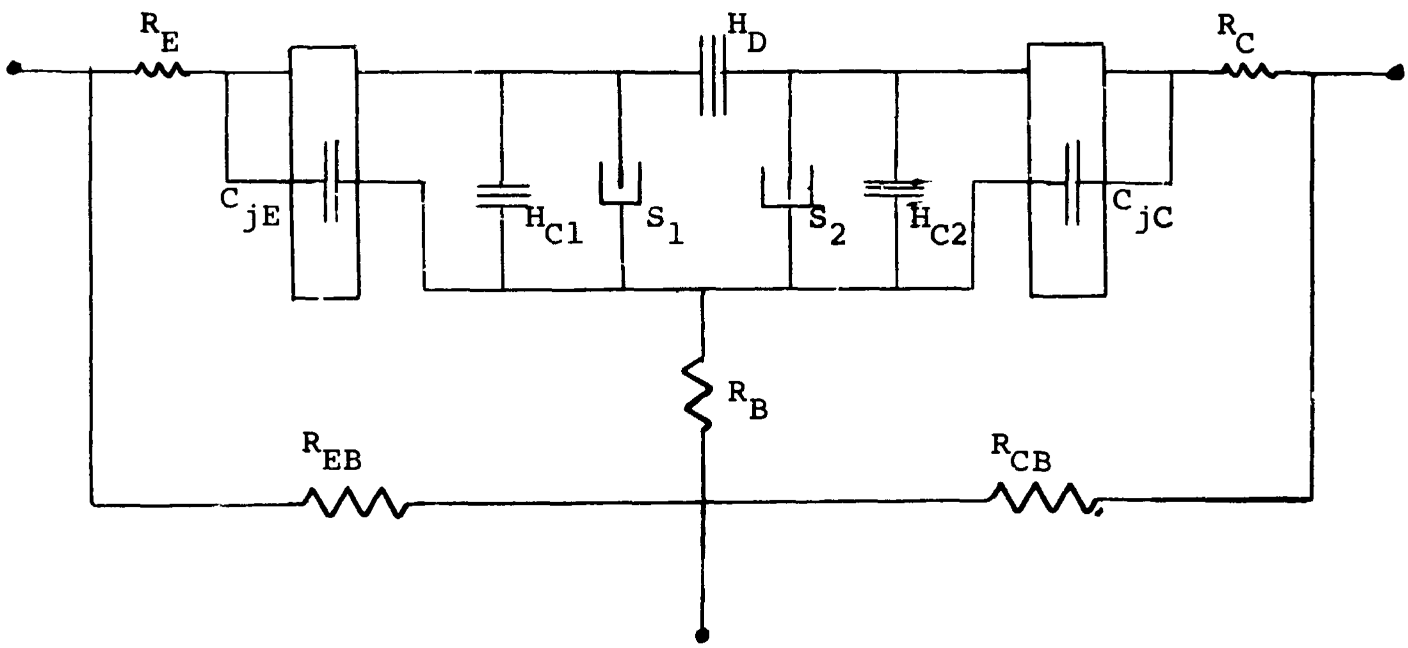
In the original Ebers-Moll formulation, the alphas were regarded as frequency-dependent with single-pole roll-off characteristics. Here, with constant alphas, these diffusion poles result from the presence of the diffusion capacitors.

The model parameter are subject to one additional constraint as follows,

$$\frac{\alpha_N}{\alpha_I} = \frac{I_{SC}}{I_{SE}} \quad .$$

2. Linvill Lumped Transistor Models

A variety of multilumped models can be made for transistors as well as for diodes. The simplest model, which is functionally identical to the Ebers-Moll model, is as follows.

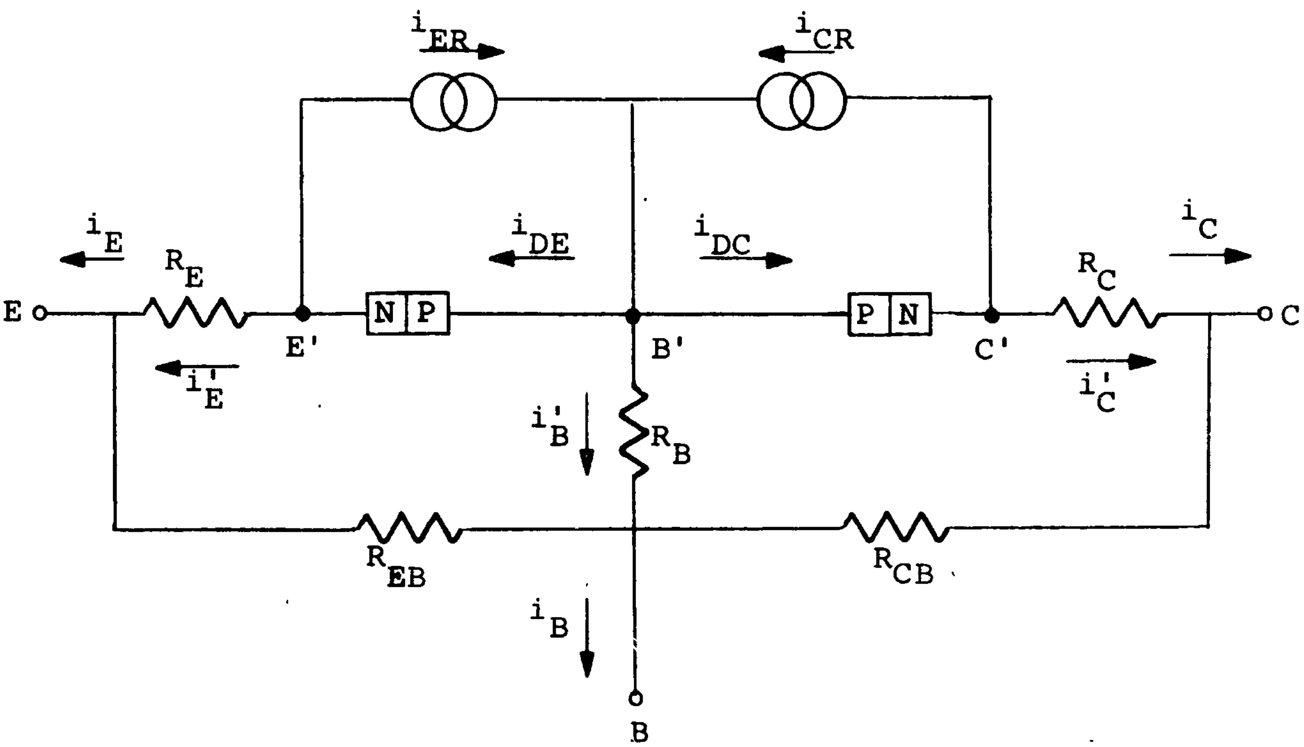


In this model, H_{C1} carries the normal region recombination current, S_1 contains the normal region stored charge and H_D carries the diffusion current. H_{C2} and S_2 are for the inverted recombination current and charge.

B. Model Performance

1. Ebers-Moll Model

a. Analytic Solutions of Static Equations



As the transistor equations are somewhat more complex than those of the diode, we will first develop the equations for the idealized transistor without series and shunt resistors, using a "prime" symbol to denote the idealized terms. The equations in this section are static (D.C.) only.

The basic equations for the "components" of the model are as follows. For the 2 junctions,

$$i_{DC} = I_{SC} \left(e^{v'_{BC}/V_o} - 1 \right) \tag{1}$$

$$i_{DE} = I_{SE} \left(e^{v'_{BE}/V_o} - 1 \right) \tag{2}$$

where V_O and I_S both are positive for an NPN transistor and both negative for a PNP transistor.

For the 2 current generators,

$$i_{CR} = \alpha_N \, i'_E \tag{3}$$

$$i_{ER} = \alpha_I \, i'_C \tag{4}$$

Additionally, the 2 saturation currents and the 2 alphas are related by the following equation:

$$\frac{I_{SC}}{I_{SE}} = \frac{\alpha_N}{\alpha_I} \; . \tag{5}$$

It is to be noted that for the model above, the alpha current sources generate currents proportional to the external currents, not the internal junction currents. This convention results in the following relationship between external and junction currents.

Summing currents at the nodes,

$$i'_C = i_{DC} - i_{CR} \quad ; \quad i'_E = i_{DE} - i_{ER}$$

$$i'_C = i_{DC} - \alpha_N i'_E \quad ; \quad i'_E = i_{DE} - \alpha_I i'_C$$

$$i'_C = i_{DC} - \alpha_N (i_{DE} - \alpha_I i'_C)$$

$$i'_C = \frac{i_{DC} - \alpha_N \, i_{DE}}{1 - \alpha_N \alpha_I} \tag{6}$$

Similarly,

$$i'_E = \frac{i_{DE} - \alpha_I \, i_{DC}}{1 - \alpha_N \alpha_I} \tag{7}$$

The relationship between base-emitter voltage and base and collector currents is developed as follows.

From (2)

$$v'_{BE} = V_o \ln \left(\frac{I_{SE} + i_{DE}}{I_{SE}} \right)$$

but

$$i_{DE} = i'_E + \alpha_I \, i'_C$$

and

$$i'_E = -i'_C - i'_B$$

therefore

$$i_{DE} = -i'_B - (1 - \alpha_I) \, i'_C$$

and

$$v'_{BE} = V_o \ln \left(\frac{I_{SE} - i'_B - (1 - \alpha_I)\, i'_C}{I_{SE}} \right) \tag{8}$$

In a similar manner, it can be shown that

$$v'_{BC} = V_o \ln \left(\frac{I_{SC} - \alpha_N\, i'_B + (1 - \alpha_N)\, i'_C}{I_{SC}} \right) \tag{9}$$

The equation for collector-emitter voltage can now be developed,

$$v'_{CE} = v'_{BE} - v'_{BC}$$

Substituting (8) and (9),

$$v'_{CE} = V_o \ln \left(\frac{I_{SC}(I_{SE} - i'_B - (1 - \alpha_I)\, i'_C}{I_{SE}(I_{SC} - \alpha_N\, i'_B + (1 - \alpha_N) i'_C} \right) \tag{10}$$

Under most normal conditions, the base current is much greater than the saturation currents and equation (8) may be simplified.

Thus for $i_B \gg I_{SC}$; in terms of i'_B,

$$v'_{BE} \cong V_o \ln \left(\frac{-i'_B - (1 - \alpha_I) i'_C}{I_{SE}} \right)$$

$$v'_{BE} \cong V_o \ln \left(\frac{-i'_B\, (1 + (1 - \alpha_I) i'_C / i'_B)}{I_{SE}} \right)$$

$$v'_{BE} \cong V_o \left[\ln \frac{-i'_B}{I_{SE}} + \ln \left(1 + \frac{(1 - \alpha_I) i'_C}{i'_B} \right) \right] \qquad (8a)$$

in terms of i'_C,

$$v'_{BE} \cong V_o \ \ln \left(\frac{-i'_C \left(\frac{i'_B}{i'_C} + (1 - \alpha_I) \right)}{I_{SE}} \right)$$

$$v'_{BE} \cong V_o \left[\ln \frac{-i'_C}{I_{SE}} + \ln \left(\frac{i'_B}{i'_C} + 1 - \alpha_I \right) \right] \qquad (8b)$$

Equation (10) may also be simplified when the currents are large compared with the saturation currents; using (5),

$$v'_{CE} \cong V_o \ \ln \left[\frac{\alpha_N \ (-i'_B - (1 - \alpha_I) i'_C}{\alpha_I \ (-\alpha_N i'_B + (1 - \alpha_N) i'_C} \right] \qquad (10a)$$

The following form is also useful:

$$v'_{CE} = V_o \left[\ln \left(\frac{-\alpha_N}{-\alpha_N + (1 - \alpha_N) \frac{i'_C}{i'_B}} \right) + \ln \left(\frac{1 + (1 - \alpha_I) \frac{i'_C}{i'_B}}{\alpha_I} \right) \right]$$

(10b)

The equations for v'_{CE} are of use primarilly for a saturated transistor, as v'_{CE} is almost independent of the current in the active region. Thus it is also useful to develop an equation for collector current in the active region. From (10),

$$i'_C = \frac{i'_B\left[\frac{-\alpha_N}{\alpha_I} + \alpha_N \exp(v'_{CE}/V_o)\right] + \alpha_I i_{SC}(1 - \exp(v'_{CE}/V_o))}{\frac{\alpha_N}{\alpha_I} - \alpha_N + (1 - \alpha_N)\exp(v'_{CE}/V_o)} \tag{11}$$

for $v_{CE} >> V_o$,

$$i'_C \cong \frac{i'_B\,\alpha_N - I_{SC}\,\alpha_I}{1 - \alpha_N}$$

and for $i'_B >> I_{SC}$,

$$i'_C \cong i'_B\left(\frac{\alpha_N}{1 - \alpha_N}\right) \tag{11a}$$

The above equations are developed for the "intrinsic" transistor defined by the "primed" currents and voltage. Equations (8), (10), and (11), the equations for base voltage, collector voltage, and collector current may now be modified to account for the series and shunt resistors.

For $i_B >> I_{SC}$ and $i_B >> \dfrac{v_{CB}}{R_{CB}}$,

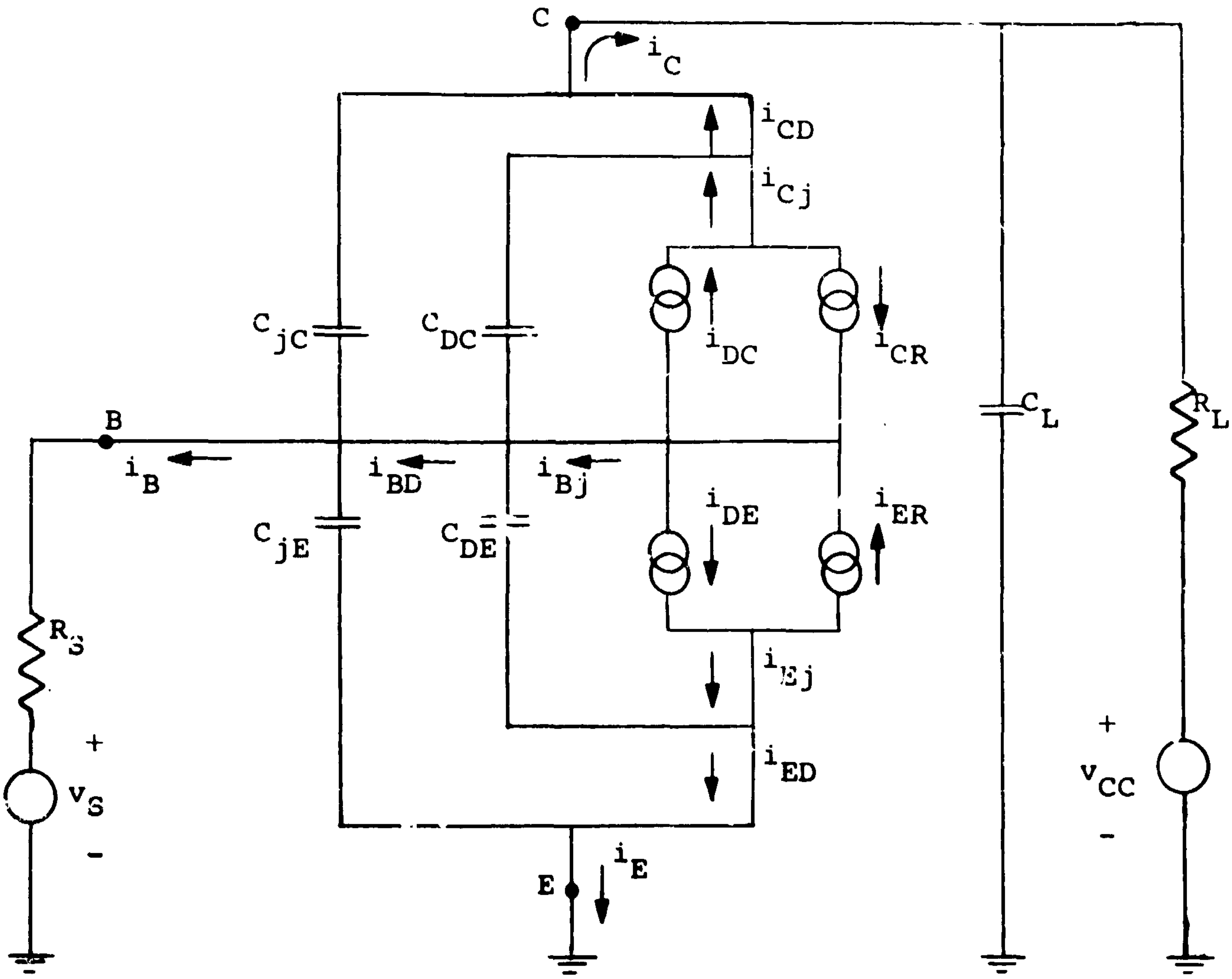
$$v_{BE} = v'_{BE} - i_B R_B - (i_B + i_C) R_E \tag{12}$$

$$v_{CE} = v'_{CE} - i_C R_C - (i_B + i_C) R_E \tag{13}$$

$$i_C \cong i_C' - \frac{v_C}{R_{CB}} \frac{\alpha_N}{1 - \alpha_N} \tag{14}$$

b. Analytic Solutions of Transistor Dynamic Equations

Approximate solutions for the current step response of the grounded-emitter RC-loaded transistor circuit will be developed. The circuit, with the Ebers-Moll dynamic transistor model, is as follows (series and shunt resistors are omitted from the model here in the interests of simplicity):



1) Cut-off Region Solution - The cut-off region is formally defined by both the emitter-base diode and the collector-base diode being reverse biased. However, as our purpose here is to develop an approximate equation for the delay time of the collector response to a base step of voltage through a source resistance, we will extend the definition. Thus we say the transistor is virtually cut-off until the collector current reaches 1% of its final value, i_{CF}.

Within this region, we can simplify the circuit by neglecting the diffusion capacitances. Thus

$$C_{DE} \cong 0$$

$$C_{DC} \cong 0$$

Also for $-i_B \gg I_{SE}$,

$$i_{DC} \cong 0 \ .$$

For an initial base voltage, v_{BO}, and a base voltage, v_{BX}, corresponding to .01 i_{CF}, the charge-equivalent linearized junction capacitances, C_{jEL} and C_{jCL}, may be calculated. By further assuming that the net change of collector voltage during the delay time is zero, we can write an equation for the base input capacitance, C_{BI}:

$$C_{BI} = C_{jEL} + C_{jCL} \tag{1}$$

Lastly, by assuming negligable base input conductance during this delay period, the delay equation can be written by inspection:

$$t_D = R_S C_{BI} \ln \frac{v_S - v_{BO}}{v_S - v_{BX}} \qquad (2)$$

where

$$v_{BX} \cong V_o \ln \frac{-.01\ i_{CF}}{I_{SE}} \qquad (3)$$

2) Normal Region Solutions - The normal region is defined by the emitter-base diode being forward biased and the collector-base diode being reverse biased. In this region it is possible to make two simplifying approximations. For $v_{CB} \geq 0$ and $-i_B \gg I_{SE}$,

$i_{DC} \cong 0$ and $C_{DC} \cong 0$.

Then, summing currents at the base node, using linearized equivalents for the junction capacitances,

$$i_B + i_{DE} - i_{CR} - i_{ER} + (C_{DE} + C_{jEL}) \frac{dv_{BE}}{dt} + C_{jCL} \frac{dv_{BC}}{dt} = 0 \qquad (1)$$

Noting that $i_{CR} = \alpha_N (i_{DE} - i_{ER})$ (2)

and $i_{ER} = \alpha_I (i_{DC} - i_{CR})$ (3)

which 2 equations can be reduced to

$$i_{CR} = i_{DE} \times \frac{\alpha_N}{1 - \alpha_N \alpha_I} \tag{2a}$$

and

$$i_{ER} = i_{DE} \times \frac{-\alpha_N \alpha_I}{1 - \alpha_N \alpha_I} \tag{3a}$$

Thus

$$i_{DE} - i_{CR} - i_{ER} = i_{DE} \left(\frac{1 - \alpha_N}{1 - \alpha_N \alpha_I} \right)$$

and

$$i_B + i_{DE} \left(\frac{1 - \alpha_N}{1 - \alpha_N \alpha_I} \right) + (C_{DE} + C_{jEL} + C_{jCL}) \frac{dv_B}{dt} - C_{jCL} \frac{dv_C}{dt} = 0 \tag{1a}$$

where the single subscript voltages are ground referenced.

Noting that $C_{DE} \cong \tau_{DE} \dfrac{i_{DE}}{V_o}$ (4)

and that

$$\frac{dv_B}{dt} \doteq \frac{dv_B}{di_{DE}} \frac{di_{DE}}{dt} \tag{5}$$

$$i_B + i_{DE} \left(\frac{1 - \alpha_N}{1 - \alpha_N \alpha_I} \right) + \tau_{DE} \frac{di_{DE}}{dt} + (C_{jEL} + C_{jCL}) \frac{dv_B}{dt} -$$

$$C_{jCL} \frac{dv_C}{dt} = 0 \tag{1b}$$

Defining the base diffusion current, i_{BD}, as the base current exclusive of the junction capacitance currents, then (1b) may be partitioned into

$$i_{BD} + i_{DE}\left(\frac{1-\alpha_N}{1-\alpha_N\alpha_I}\right) - \tau_{DE}\frac{di_{DE}}{dt} = 0 \qquad (7)$$

and

$$i_B - i_{BD} + (C_{jEL} + C_{jCL})\frac{dv_B}{dt} - C_{jCL}\frac{dv_C}{dt} = 0 \qquad (1c)$$

Solving (7) for i_{DE}, using the Laplace Transform and denoting the initial value of i_{DE} as i_{DEO},

$$i_{BD} + I_{DE}\left(\frac{1-\alpha_N}{1-\alpha_N\alpha_I} + \tau_{DE}\, s\right) - \tau_{DE}\, i_{DEO} - 0 \qquad (7a)$$

$$I_{DE} = \frac{-I_{BD} + \tau_{DE}\, i_{DEO}}{1-\alpha_N + (1-\alpha_N\alpha_I)\tau_{DE}\, s}\,(1-\alpha_N\alpha_I) \qquad (7b)$$

Defining the Normal Region common-base shorted-collector time constant,

$$\tau_N = (1-\alpha_N\alpha_I)\,\tau_{DE} \qquad (8)$$

and the Normal Region common-emitter shorted collector time constant,

$$\tau_{\beta N} = (\beta_N + 1)\tau_N \tag{8}$$

where

$$\beta_N = \frac{\alpha_N}{1 - \alpha_N} \quad ,$$

Then from (7b),

$$I_{DE} = \frac{-(\beta_N + 1)(1 - \alpha_N \alpha_I)\; I_{BD} + \tau_{\beta N}\; i_{DEO}}{1 + \tau_{\beta N}\; S} \tag{7c}$$

Then from (2a),

$$I_{CR} = \frac{-\beta_N\; I_{BD} + \tau_{\beta N}\; i_{CRO}}{1 + \tau_{\beta N}\; S} \tag{9}$$

where

$$i_{CRO} = \frac{\alpha_N}{1 - \alpha_N \alpha_I}\; i_{DEO}$$

is the initial collector generator current.

Next, summing currents at the collector node,

$$i_C + i_{CR} + C_{jCL} \frac{dv_{CB}}{dt} = 0 \tag{6}$$

Expanding (6) to include the separate external currents at the collector node,

$$C_L \frac{dv_C}{dt} + \frac{v_C - v_{CC}}{R_L} + i_{CR} + C_{jCL} \frac{dv_{CB}}{dt} = 0 \tag{6a}$$

$$(C_L + C_{jCL}) \frac{dv_C}{dt} - C_{jCL} \frac{dv_B}{dt} + \frac{v_C}{R_L} - \frac{v_{CC}}{R_L} + i_{CR} = 0 \qquad (6b)$$

Solving (6b) for v_C, using the Laplace Transform, and defining

$$C_p = C_L + C_{jCL} \qquad (10)$$

and

$$\tau_p = R_L C_p \ , \qquad (11)$$

$$\tau_p \frac{dv_C}{dt} - C_{jCL} R_L \frac{dv_B}{dt} + v_C - v_{CC} + i_{CR} R_L = 0 \qquad (6c)$$

To simplify this equation, assume $\frac{dv_B}{dt}$ is negligably small compared to $\frac{dv_C}{dt}$. Then

$$\tau_p \frac{dv_C}{dt} + v_C - v_{CC} + i_{CR} R_L \cong 0 \qquad (6d)$$

Transforming (6d) and denoting the initial collector voltage as v_{CO},

$$\tau_p (V_C S - v_{CO}) + V_C - V_{CC} + I_{CR} R_L = 0 \qquad (6e)$$

Assuming a step for v_{CC},

$$V_{CC} = \frac{v_{CC}}{S} \qquad (12)$$

Then

$$V_C = \frac{\tau_p v_{CO}}{\tau_p S + 1} + \frac{v_{CC}}{S(\tau_p S+1)} - \frac{I_{CD} R_L}{\tau_p S+1} \qquad (6f)$$

Returning to the base equation (8), we repeat the simplifying assumption that $\frac{dv_B}{dt}$ is negligably small compared to $\frac{dv_C}{dt}$.

Then

$$i_B - i_{BD} - C_{jCL} \frac{dv_C}{dt} \cong 0 \qquad (8a)$$

Transforming (8a),

$$I_B - I_{BD} - C_{jCL} (V_C S - v_{CO}) = 0 \qquad (8b)$$

Assuming that v_S is a step of amplitude large compared to v_B, then i_B is also a step and

$$I_B \cong \frac{i_B}{S} \qquad (13)$$

and

$$\frac{i_B}{S} - I_{BD} - C_{jCL} (V_C S - v_{CO}) = 0 \qquad (8c)$$

$$I_{BD} = \frac{i_B}{S} - C_{jCL} (V_C S - v_{CO}) = 0 \qquad (8d)$$

Substituting (8d) in (9a)

$$I_{CR} = \frac{1}{1+\tau_{\beta N} S}\left[-\beta_N\left(\frac{i_B}{S} - C_{jCL}(V_C S - v_{CO})\right) + \tau_{\beta N} i_{CRO}\right] \tag{14}$$

Substituting (14) into (6f),

$$V_C = \frac{\tau_p\, v_{CO}}{\tau_p S+1} + \frac{v_{CC}}{S(\tau_p S+1)} - \tag{14a}$$

$$\frac{R_L}{(\tau_p S+1)(\tau_{\beta N} S+1)}\left(\frac{-\beta_N i_B}{S} + \beta_N C_{jCL} V_C S - \beta_N C_{jCL} v_{CO} + \tau_{\beta N} i_{CRO}\right)$$

$$V_C\left(1 + \frac{\beta_N R_L C_{jCL} S}{(\tau_p S+1)(\tau_{\beta N} S+1)}\right) = \frac{\tau_p\, v_{CO}}{\tau_p S+1} + \frac{v_{CC}}{S(\tau_p S+1)} - \tag{14b}$$

$$\frac{R_L}{(\tau_p S+1)(\tau_{\beta N} S+1)}\left(\frac{-\beta_N i_B}{S} - \beta_N C_{jCL} v_{CO} + \tau_{\beta N} i_{CRO}\right)$$

$$V_C = \frac{\dfrac{(\tau_p v_{CO} S + v_{CC})(\tau_{\beta N} S+1)}{S} + \dfrac{R_L \beta_N i_B}{S} + R_L \beta_N C_{jCL} v_{CO} - R_L \tau_{\beta N} i_{CRO}}{\tau_p \tau_{\beta N} S^2 + (\tau_p + \tau_{\beta N} + \beta_N R_L C_{jCL})\, S + 1} \tag{14c}$$

$$V_C = \frac{\tau_p \tau_{\beta N} v_{CO}\, S + \tau_A\, v_{CO} + \tau_{\beta N}(v_{CC} - R_L i_{CRO}) + \dfrac{v_{CC} + R_L \beta_N i_B}{S}}{\tau_p\, \tau_{\beta N} S^2 + (\tau_A + \tau_{\beta N})\, S + 1} \tag{14d}$$

where $\tau_A = ((\beta + 1)\, C_{jCL} + C_L)\, R_L$ (15)

$$V_C = \frac{v_{CO}\, s + \dfrac{\tau_A v_{CO}}{\tau_p \tau_{\beta N}} + \dfrac{v_{CC} - R_L i_{CRO}}{\tau_p} + \dfrac{v_{CC} + R_L \beta_N i_B}{\tau_p \tau_{\beta N}\, s}}{s^2 + \dfrac{(\tau_A + \tau_{\beta N})\, s}{\tau_p \tau_{\beta N}} + \dfrac{1}{\tau_p \tau_{\beta N}}} \tag{14e}$$

$$V_C = \frac{v_{CO}}{s} + \frac{\dfrac{v_{CC} - v_{CO} - R_L i_{CRO}}{\tau_p} + \dfrac{v_{CC} - v_{CO} + R_L \beta_N i_B}{\tau_p \tau_{\beta N}\, s}}{s^2 + \dfrac{\tau_A + \tau_{\beta N}}{\tau_p \tau_{\beta N}}\, s + \dfrac{1}{\tau_p \tau_{\beta N}}} \tag{14f}$$

Denoting the poles and the driving voltages as

$$\tau_1,\ \tau_2 \equiv \frac{1}{2}\left(\tau_{\beta N} + \tau_A \pm \sqrt{(\tau_{\beta N} + \tau_A)^2 - 4\tau_{\beta N}\tau_p}\right) \tag{16}$$

$$v_1 \equiv v_{CC} - v_{CO} + \beta_N R_L i_B \tag{17}$$

$$v_2 \equiv v_{CC} - v_{CO} - R_L i_{CRO} \tag{18}$$

The Inverse Transform of (14f) is

$$v_C = v_{CO} + \frac{\tau_{\beta N} v_2}{\tau_1 - \tau_2}\left(\exp(-t/\tau_1) - \exp(-t/\tau_2)\right) + v_1\left(1 - \frac{\tau_1 \exp(-t/\tau_1) - \tau_2 \exp(-t/\tau_2)}{\tau_1 - \tau_2}\right) \tag{19}$$

Equation (19) is the general response to a step of base current and collector supply voltage with initial conditions v_{CO} and i_{CRO} (note that i_{CRO} results from an initial base voltage, v_{BO}). This voltage response equation is considerably simplified when the initial rates of change of collector and base voltages are zero. Under these conditions it can be seen from (6b) that $v_2 = 0$. Thus v_2 is zero when the transistor is in an active region steady state when the drive step is applied. Note that v_2 is, in general, not zero when the transistor is leaving the saturation region and entering the active region in response to a base step. As indicated previously, equation (19) is applicable only within the active region.

This region is defined such that i_{CR} is large compared to I_{SE} and $-i_{ER}$ is smaller than I_{SC}. To aid in the use of the collector voltage equation, the equation for i_{CR} is developed below.

From (6d)

$$i_{CR} = \frac{v_{CC} - v_C}{R_L} - C_p \frac{dv_C}{dt} \qquad (20)$$

(20a)

$$i_{CR} = \frac{v_{CC}}{R_L} - \frac{v_{CO}}{R_L} - \frac{\tau_{\beta N} \; v_2}{(\tau_1 - \tau_2)R_L} \left(\exp(-t/\tau_1) - \exp(-t/\tau_2)\right) -$$

$$\frac{v_1}{R_L}\left(1 - \frac{\tau_1 \exp(-t/\tau_1) - \tau_2 \exp(-t/\tau_2)}{\tau_1 - \tau_2}\right) -$$

$$\frac{C_p \tau_{\beta N} v_2}{\tau_1 - \tau_2}\left(\frac{-\exp(-t/\tau_1)}{\tau_1} + \frac{\exp(-t/\tau_2)}{\tau_2}\right) -$$

$$C_p \; v_1 \left(\frac{-\exp(-t/\tau_1) + \exp(-t/\tau_2)}{\tau_2 - \tau_1}\right)$$

$$i_{CR} = -\beta_N i_B + \frac{v_1}{\tau_1 - \tau_2}\left(C_1 \exp(-t/\tau_1) - C_2 \exp(-t/\tau_2)\right) -$$

(20b)

$$\frac{\tau_{\beta N} v_2}{\tau_1 - \tau_2}\left(\frac{C_1}{\tau_1} \exp(-t/\tau_1) - \frac{C_2}{\tau_2} \exp(-t/\tau_2)\right)$$

where $C_1 \equiv \frac{\tau_1}{R_L} - C_p$

and $C_2 \equiv \frac{\tau_2}{R_L} - C_p$

3) Saturation Region Solutions - The approximate solution to the step response of a saturated transistor was developed by Moll. We described the results here, using notation consistant with that of the previous section.

The saturation region is defined by both the emitter-base diode and the collector base diode being forward biased. In this region, two simplifying approximations are made, both based on the relatively small variations possible for v_B and v_C. First, the junction capacitances have negligable effect and may be neglected. Second, the base and collector circuits may be regarded as current sources.

Assuming that i_b was at a steady state value of i_{B1} prior to zero time, and that i_b steps to a value of i_{B2} at zero time, and that $i_c = I_c$ both prior to zero time and during the storage time. Then for

$$\tau_I = (1 - \alpha_N \alpha_I) \tau_{DC}$$

where

$$\tau_{DC} \cong C_{DC} \frac{V_o}{i_{DC}}$$

$$i_{er} = \frac{-\alpha_I}{1 - \alpha_N \alpha_I} \Big[\alpha_N i_{B2} - (1 - \alpha_N) i_c - \qquad (1)$$

$$\frac{\alpha_N (i_{B1} - i_{B2})}{\tau_y - \tau_x} (\tau_x \exp(-t/\tau_x) - \tau_y \exp(-t/\tau_y)) \Big]$$

$$i_{cr} = \frac{-\alpha_N}{1-\alpha_N\alpha_I}\left[i_{B2} + (1-\alpha_I)\, i_c - \frac{i_{B1}-i_{B2}}{\tau_y - \tau_x}\left((\tau_x - \tau_I)\exp(-t/\tau_x) - (\tau_y - \tau_I)\exp(-t/\tau_y)\right)\right] \quad (2)$$

where

$$\tau_N = 1/\omega_N \; ; \; \tau_I = 1/\omega_I \quad (3)$$

$$\tau_x = 1/\omega_x \; ; \; \tau_y = 1/\omega_y \quad (4)$$

and

$$\omega_x, \omega_y = \frac{1}{2}\left((\omega_N + \omega_I) \pm \sqrt{(\omega_N + \omega_I)^2 - 4\omega_N\omega_I(1-\alpha_N\alpha_I)}\right) \quad (5)$$

The storage time, t_s, is the time required for i_{er} to get to zero. At $t = t_s$, i_{cr} is, in general, not equal to i_c. The equations are valid only for times such that neither i_{cr} nor i_{er} change their polarity.

2. Linvill-Lumped Model

As the performance of the simple lumped model described in the previous section is identical with that of the Ebers-Moll model, separate equations for it will not be developed.

It is worth noting here that the Single-L lumped diode model may be used in place of the Ebers-Moll diode model for either or both diodes within the Ebers-Moll transistor model.

C. Parameter Evaluation

The transistor models, even more than the diode models, are accurate over only a limited range of operating points. This is so primarily because the model uses constant alphas, whereas the transistor alphas vary appreciably with current level. The relative complexity of the transistor model makes it highly advisable to select a set of data points such that each parameter is evaluated as independently of the others as possible.

1. Ebers-Moll Model

a. V_o

From the model performance section,

$$v'_{BE} = V_o \ln\left(\frac{I_{SE} - i'_B - (1 - \alpha_I)i'_c}{I_{SE}}\right) .$$

For $|i_B| \gg |I_{SC}|$ and $\alpha_I \ll 1$, $v'_{BE} \cong V_o \ln \frac{i'_E}{I_{SE}}$

For 2 data points, i'_{E1}, v'_{BE1}, and i'_{E2}, v'_{BE2} ,

$V_o \cong (v'_{BE1} - v'_{BE2})/\ln (i'_{E1}/i'_{E2})$

If the 2 data points are chosen at relatively low currents such that the voltage drops across the bulk emitter and base resistors, $i'_E R_E$ and $i'_B R_B$, are less than a few millivolts, then the same equation is approximately valid for the terminal parameters:

$V_o \cong (v_{BE1} - v_{BE2})/\ln(i_{E1}/i_{E2})$

b. I_{SE}

I_{SE} can be obtained from 1 of the above data points and checked at the other.

$$I_{SE} = -i_{E1} \exp(-v_{BE1}/V_o)$$

c. α_N

Alpha-normal should be determined at a current level in the center of range of use, with a data point i_{B3}, i_{C3}, at a collector-emitter voltage, v_{CE3}. For a transistor used as a switch, v_{CE3} should be just outside of saturation; for a linear application, the middle of the operating region should be used.

If i_{B3} is much greater than the collector-base leakage current, v_{CB}/R_{CB}, then

$$\alpha_N = \frac{i_{C3}/i_{B3}}{(i_{C3}/i_{B3}) + 1} \quad .$$

If i_{B3} is not considerably greater than the leakage current, then an additional data point, i_{C4}, i_{B4} is needed, where $i_{C4} \ll i_{C3}$.

Letting $i_{C3} - i_{C4} = \Delta i_C$

and $i_{B3} - i_{B4} = \Delta i_B$,

$$\alpha_N = \frac{\Delta i_C/\Delta i_B}{(\Delta i_C/\Delta i_B) + 1}$$

d. α_I

For those very rare applications where a transistor is used in the inverted region, α_I can be evaluated in a manner similar to α_N.

For most applications, the primary effect of α_I is on the collector-emitter saturation voltage. This suggests evaluating α_I from a deep saturation data point. From the previous section, for $-i_B \gg I_{SC}$,

$$v'_{CE} = V_o \ln \left[\frac{\alpha_N \, (-i'_B - (1-\alpha_I) i'_C}{\alpha_I \, (-\alpha_N i'_B + (1 - \alpha_N) i'_C} \right] .$$

For $i'_C = 0$, this equation reduces to

$$v'_{CE} = V_o \ln \frac{1}{\alpha_I} .$$

Thus

$$\alpha_I = \exp(-v'_{CE}/V_o)$$

The data should be obtained at a base current, i_{B5}, within the range of use but small enough to make $i_{B5} \cdot R_E$ negligable.

Where it is advisable to determine α_I at a non-zero i_{C5}, the v'_{CE} equation may be manipulated to give

$$\frac{1 + (1 - \alpha_I) i_{C5}/i_{B5}}{\alpha_I} = \frac{-\alpha_N + (1 - \alpha_N) i_{C5}/i_{B5}}{-\alpha_N} \exp\left(\frac{v_{CE}}{V_o}\right)$$

Calling the right side of this equation "K", then

$$\alpha_I = \frac{1 + i_{C5}/i_{B5}}{K + i_{C5}/i_{B5}}$$

e. I_{SC}

No new data is needed to evaluate I_{SC}:

$$I_{SC} = \frac{I_{SE}\ \alpha_N}{\alpha_I}$$

f. R_E

R_E can be determined from 2 data-points at a fairly, high current level, such as that used for the α_N evaluation. Using v_{B3a} @ i_{B3}, i_{C3}, and v_{C3}; and v_{B3b} @ i_{B3}, and $i_C = 0$.

$$v_{BE3a} - v_{BE3b} = V_o \ln\left(1 + \frac{(1-\alpha_I) i_{C3}}{i_{B3}}\right) - i_{C3} R_E$$

$$R_E = \left(v_{BE3a} - v_{BE3b} - V_o \ln\left(1 + \frac{(1-\alpha_I) i_{C3}}{i_{B3}}\right)\right) \frac{1}{-i_{C3}}$$

g. R_B

R_B can be evaluated from 2 previous measurements, v_{BE1} and i_{B1} @ $i_C = 0$, and v_{BE3b} and i_{B3} @ $i_C = 0$.

$$v_{BE3b} - v_{BE1} = V_o \ln \frac{i_{B3}}{i_{B1}} - i_{B3} (R_B + R_E)$$

$$R_B = \left(v_{BE3b} - v_{BE1} - V_o \ln \frac{i_{B3}}{i_{B1}} \right) \frac{1}{-i_{B3}} - R_E$$

h. R_C

R_C can be determined from an additional data point in saturation at relatively high currents. Using v_{CE3c} @ i_{B3} and $.5\ i_{C3}$.

$$v_{CE3c} = V_o \ln \left(\frac{\alpha_N \left(-1 - (1-\alpha_I) \frac{.5 i_{C3}}{i_{B3}}\right)}{\alpha_I \left(-\alpha_N + (1-\alpha_N) \frac{.5 i_{C3}}{i_{B3}}\right)} \right) -$$

$$.5 i_{C3} R_C - (.5 i_{C3} + i_{B3}) R_E$$

$$R_C = \left[v_{CE3c} - V_o \ln \left(\frac{\alpha_N \left(-1 - (1-\alpha_I) \frac{.5 i_{C3}}{i_{B3}}\right)}{\alpha_I \left(-\alpha_N + (1-\alpha_N) \frac{.5 i_{C3}}{i_{B3}}\right)} \right) + (.5 i_{C3} + i_{B3}) R_E \right] \frac{1}{-.5 i_{C3}}$$

i. R_{EB}

A data point near the maximum reverse emitter-base voltage to be used is required to evaluate R_{EB}. Using i_{B6} @ v_{BE6} with $i_C = 0$,

$$-i'_B = I_{SE}\left(e^{v'_{BE}/V_o} - 1\right)$$

For an appreciable reverse voltage, $i'_B = I_{SE}$.

$$i_B = i'_B - v_{BE}/R_{EB}$$

$$i_B = I_{SE} - v_{BE}/R_{EB}$$

$$R_{EB} = \frac{-v_{BE}}{i_B - I_{SE}}$$

$$R_{EB} = \frac{-v_{BE6}}{i_{B6} - I_{SE}}$$

j. R_{CB}

Using a data point near the maximum reverse collector-emitter voltage to be used, i_{B7} @ v_{BC7} with $i_E = 0$,

$$R_{CB} = \frac{-v_{BC7}}{i_{B7} - I_{SC}}$$

k. C_{jE} parameters: V_{KE}, K_E, N_E

In most cases, the arbitrary use of $V_{KE} = 1.0$ volt should be satisfactory.

From the equation for C_{jE},

$$C_{jE} = \frac{K_E}{(V_{KE} - v_{BE})^{N_E}}$$

Using as data a small-signal measurement of C_{BE1} @ $v_{BE} = 0$ and $i_C = 0$ to evaluate K_E,

$$K_E = C_{BE1}$$

Using a similar data point, C_{BE2} @ the maximum used reverse base-emitter voltage, v_{BER}, with $i_C = 0$,

$$N_E = \frac{\ln (K_E/C_{BE2})}{\ln (V_{KE} - v_{BER})}$$

l. C_{jC} parameters: V_{KC}, K_C, N_C

Again, arbitrarily let $V_{KC} = 1.0$ volt.

Using the small signal C_{BC1} @ $v_{BC} = 0$ and $i_C = 0$ to evaluate K_C,

$$K_C = C_{BC1}$$

Using C_{BC2} @ the maximum used reverse base-collector voltage, v_{BCR},

$$N_C = \frac{\ln (K_C/C_{BC2})}{\ln (V_{KC} - v_{BCR})}$$

m. C_{DE} parameter: τ_N

τ_N is the effective time constant of the emitter junction. For a transistor that is used as a switch, τ_N is best evaluated from current step response data. For an "on" step of base current, i_{BF1}, which is small compared with a collector current, i_{CF1}, the collector current rise time is approximately defined by the following equation which is derived from the general equation in the previous section.

$$t_{IR} = (\beta_N + 1)(C_{jCL}R_L + \tau_N) \ln \frac{\beta_N i_{BF1}}{\beta_N i_{BF1} - i_{CF1}}$$

where

$$\beta_N = \frac{\alpha_N}{1 - \alpha_N} ,$$

and C_{jCL} is the linearized collector junction capacitance over the collector voltage range from $v_{CB\text{-}OFF}$ to $v_{CB\text{-}ON}$.

$$C_{jCL} = \frac{Q_{jC}}{v_{CB\text{-}ON} - v_{CB\text{-}OFF}}$$

$$Q_{jC} = K_C \left. \frac{(V_{KC} - v_{CB})^{1-N_C}}{1 - N_C} \right|_{-v_{CB-ON}}^{-v_{CB-OFF}}$$

It is apparent from the equation for t_{IR} that a more sensitive evaluation of τ_N is obtained by using a value for R_L such that

$$\tau_N \gg C_{jCL} R_L .$$

Thus for $R_L \cong 0$,

$$\tau_N = t_{IR} / ((\beta_N + 1) \ln \frac{\beta_N i_{BF1}}{\beta_N i_{BF1} - i_{CF1}})$$

whereas for $R_L \neq 0$,

$$\tau_N = -C_{jCL} R_L + t_{IR} / ((\beta_N + 1) \ln \frac{\beta_N i_{BF1}}{\beta_N i_{BF1} - i_{CF1}})$$

For linear small signal transistor applications, the collector current cut-off frequency, f_α or f_t, may be used to obtain τ_N. The data should be at a relatively high current level so that error due to C_{jE} is negligable. Here

$$\tau_N = \frac{1}{(\beta_N + 1) 2\pi f_\alpha}$$

or

$$\tau_N = \frac{1}{(\beta_N + 1) 2\pi f_T}$$

n. C_{DC} parameter: τ_I

$$C_{DC} \cong \frac{\tau_I \, i_{DC}}{(1 - \alpha_N \alpha_I) \, V_o}$$

With the exception of the rare case where a transistor is operated in the inverted region, τ_I is of interest for its contribution to the saturation region behavior. As was previously shown, the storage time in response to a step of base current is a function of the several currents, the alphas and 2 time constants, τ_x and τ_y which in turn are functions of the alphas and of τ_N and τ_I.

It was shown by Moll that a simplifying approximation for the step response storage time may be made as follows,

$$t_S \cong \frac{\tau_N + \tau_I}{1 - \alpha_N \alpha_I} \ln \frac{i_{BF} - i_{BR}}{(i_{CF}/\beta_N) - i_{BR}}$$

thus

$$\tau_I = -\tau_N + t_S(1 - \alpha_N \alpha_I)/\ln \frac{i_{BF} - i_{BR}}{(i_{CF}/\beta_N) - i_{BR}}$$

Here again the currents should be chosen near the middle of the range of interest.

D. Transistor Subroutine

```
      SUBROUTINE TRAN3(V1,V2,FI1,FI2,CCE,CCC,DATA,FI11,FI21,LALGFT,KTDC)
```

```
      SUBROUTINE TRAN3(V1,V2,FI1,FI2,CCE,CCC,DATA,FI11,FI21,LALGFT,KTDC)
```

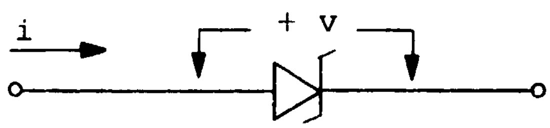

```
C     EBERS AND MOLL NON-LINEAR TRANSISTOR MODEL
C     ARG(1) = V1            EMITTER DIODE VOLTAGE (PLUS FOR P POSITIVE)
C     ARG(2) = V2            COLLECTOR DIODE VOLTAGE (PLUS FOR P POSITIVE)
C     ARG(3) = FI1           EMITTER BRANCH CURRENT (PLUS FOR FLOW P TO N)
C     ARG(4) = FI2           COLLECTOR BRANCH CURRENT (PLUS FOR FLOW P TO N)
C     ARG(5) = CCE           TOTAL EMITTER SHUNT CAPACITANCE
C     ARG(6) = CCC           TOTAL COLLECTOR SHUNT CAPACITANCE
C     ARG(7) = DATA          TRANSISTOR PARAMETER ARRAY
C     ARG(8) = FI11          INITIAL VALUE OF EMITTER CURRENT
C     ARG(9) = FI21          INITIAL VALUE OF COLLECTOR CURRENT
C     ARG(10)= LALGFT        FLAG = 1 ON FIRST PASS THROUGH SUBROUTINE
C     ARG(11)= KTDC          FLAG SET TO 1 FOR DC CASE , TO 0 FOR TRANSIENT
C     BULK RESISTANCES MUST BE INCLUDED IN EXTERNAL CIRCUIT IF DESIRED
C     DATA(1) = ISE          DATA(2) = ISC          DIODE SATURATION CURRENT
C     DATA(3) = GLE          DATA(4) = GLC          DIODE LEAKAGE CONDUCTANCE
C     DATA(5) = AN           DATA(6) = AI           COMMON BASE CURRENT GAIN
C     DATA(7) = TN           DATA(8) = TI           RECOVERY TIME CONSTANT
C     DATA(9) = VKE          DATA(10)= VKC          DIODE CONTACT POTENTIAL
C     DATA(11)= NE           DATA(12)= NC           DIODE GRADING CONSTANT
C     DATA(13)= KE           DATA(14)= KC           DIODE CAPACITANCE CONSTANT
C     DATA(15)= CES          DATA(16)= CCS          DIODE STRAY CAPACITANCE
C     DATA(17)= VO                                  THERMAL POTENTIAL  KT/Q
      DIMENSION DATA(17)
      IF(KTDC-1) 10,1,1
    1 IF(LALGFT-1) 5,5,10
C     INITIALIZE DIODE CURRENTS
    5 FI1 = FI1I
      FI2 = FI21
      GO TO 15
C     EMITTER AND COLLECTOR CURRENT CALCULATIONS
C     ISC= ISE*AN/AI
C     FIE= ISE*(EXPF(V1/V0)-1)/(1-AN*AI)
C     FIC= ISC*(EXPF(V2/V/)-1)/(1-AN*AI)
C     FI1= FIE - AI*FIC + V1*GLE
C     FI2= FIC - AN*FIE + V2*GLC
   10 AN = DATA(5)
      AI = DATA(6)
      DATA2=DATA(1)*AN/AI
      D  = 1.-AN*AI
      SIE= DATA(1)/D
      SIC= DATA2/D
      FIE= SIE*(EXPF(V1/DATA(17))-1.)
      FIC= SIC*(EXPF(V2/DATA(17))-1.)
      FI1= FIE-AI*FIC + V1*DATA(3)
      FI2= FIC-AN*FIE + V2*DATA(4)
      IF(KTDC-1) 11,15,15
C     EMITTER AND COLLECTOR SHUNT CAPACITANCE CALCULATIONS
```

```
C     CJE= KE/(VKE-V1)**NE      EMITTER JUNCTION DEPLETION CAPACITANCE
C     CJC= KC/(VKC-V2)**NC      COLLECTOR JUNCTION DEPLETION CAPACITANCE
C     CDE= (FIE+SIE)*TN/V/      EMITTER DIFFUSION CAPACITANCE
C     CDC= (FIC+SIC)*I1/VO      COLLECTOR DIFFUSION CAPACITANCE
   11 DE = DATA(9) -V1
      DC = DATA(10)-V2
      CJE= DATA(13)/DE**DATA(11)
      CJC= DATA(14)/DC**DATA(12)
      SUBROUTINE TRAN3(V1,V2,FI1,FI2,CCE,CCC,DATA,FI1I,FI2I,LALGFT,KTDC)
      CDE= (FIE+SIE)*DATA(7)/DATA(17)
      CDC= (FIC+SIC)*DATA(8)/DATA(17)



      CCE= CJE+CDE+DATA(15)
      CCC= CJC+DCD+DATA(16)
   15 CONTINUE
      RETURN
      END(1,0,0,0,0,0,1,0,0,0,0,0,0,0,0)
```

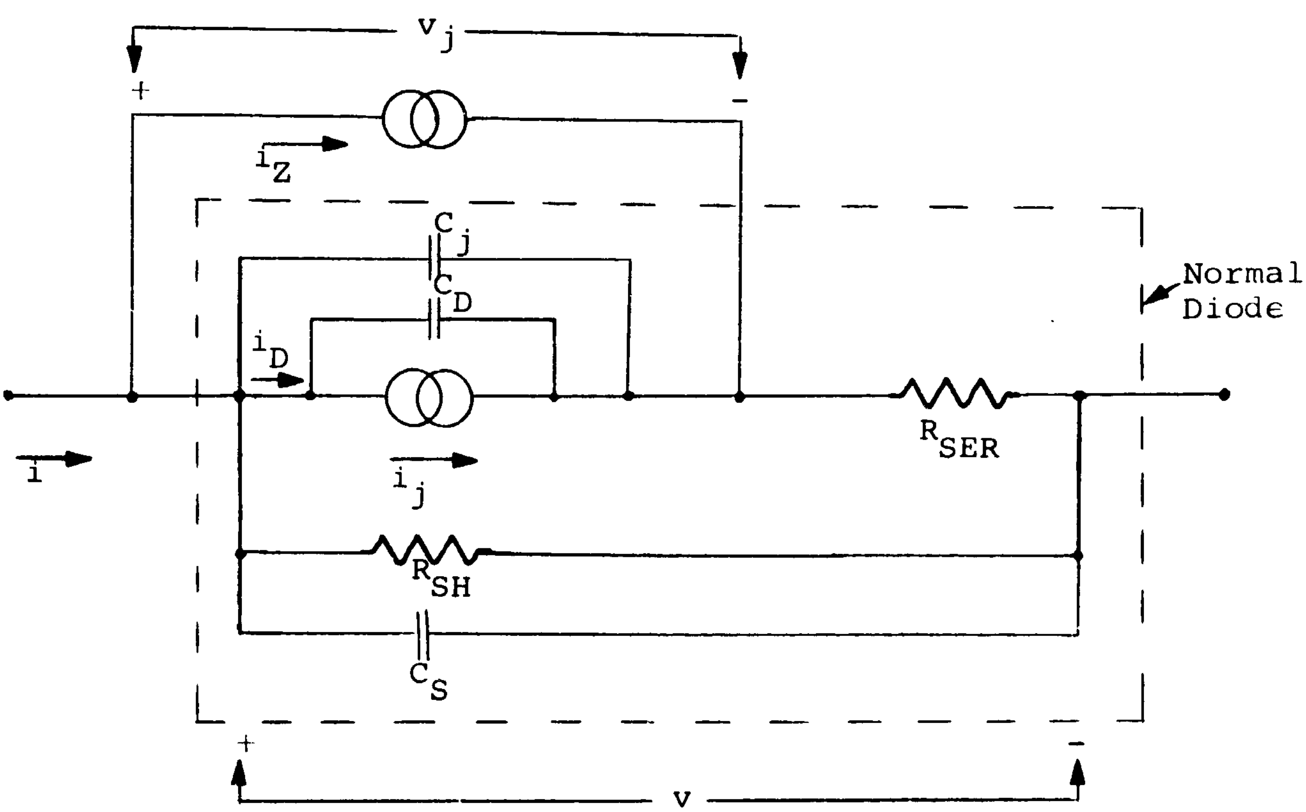
IV. ZENER DIODE MODEL

A. Model Description

For a Zener diode, normally symbolized as follows,



a model may be developed which consists of the ordinary diode model plus an additional non-linear current generator to represent the Zener or avalanche breakdown at a reverse voltage. This model is as follows.



All the components of the model except the Zener current generator, i_Z, have been previously described for the diode model. For the Zener current generator, an equation very similar in form to the diode i_j generator is suggested as follows:

$$i_Z = -I_x(\exp(-v_j/V_x) -1)$$

where both I_x and V_x are positive constants.

This model was chosen because it fits the data showing an inverse relationship between current and small signal resistance in the breakdown region.

The equations for the non-linear components of the normal diode are repeated here for convenience:

$$i_j = I_S(\exp(v_j/V_o)-1)$$

$$C_j = \frac{K}{(V_K - v_j)^N}$$

$$C_D = \tau \frac{di_j}{dv_j} \quad .$$

B. Model Performance

1. Static Forward Behavior

By neglecting the small forward value of i_Z,

$$v \cong V_o \ln \left(\frac{i}{I_S} + 1 \right) + i R_{SER}$$

Note that the forward behavior may be of very little importance in most applications.

2. Static Reverse Behavior

Neglecting the small reverse contribution of i_j and R_{SH} at relatively large reverse currents,

$$v \cong -V_x \left(\ln (-i/I_x) + 1 \right) + i R_{SER}$$

also

$$r_Z = \frac{dv}{di} \cong \frac{-V_x}{i} + R_{SER}$$

3. Dynamic Forward Step Response

The response is similar to that of a normal diode; however, Zener diodes are seldom used in a manner that would elicit this behavior.

4. Dynamic Reverse Step Response

Although normal diode charge storage and reverse recovery are present, they are not brought into play for most applications. The normal capacitive behavior of C_j is sometimes of importance.

C. Parameter Evaluation

1. Normal Diode Parameters

The normal diode parameters of a Zener diode are often of very little importance to its in-circuit use. If the Zener diode is not, under any conditions, forward biased, the normal diode components can be omitted from the model. If the Zener diode can, on occasion, be forward biased but the exact forward behavior is not of importance, crude guesses can be used for the normal parameter evaluation. It is, of course, also possible to use the procedure previously described to evaluate the normal diode parameters.

2. V_x

V_x is best determined from a data point i_1, v_1, within the "Zener breakdown" region. A relatively low current, such that i, R_{SER} is very small compared to v_1, should be used. The small signal resistance at that point, r_{Z1}, should also be determined.

Then, $V_x \cong -r_{Z1} i_1$

3. I_x

I_x can be evaluated from the same data as follows,

$$I_x \cong -i_1 \exp(v_1/V_x)$$

4. R_{SER}

Although R_{SER} is part of the normal diode, it is sometimes of importance to Zener diode operation. It can be evaluated from a second data point within the "Zener breakdown" region, i_2, v_2, and r_{Z2}, at a higher current than the first data point.

$$R_{SER} = r_{Z2} + V_x/i_2$$

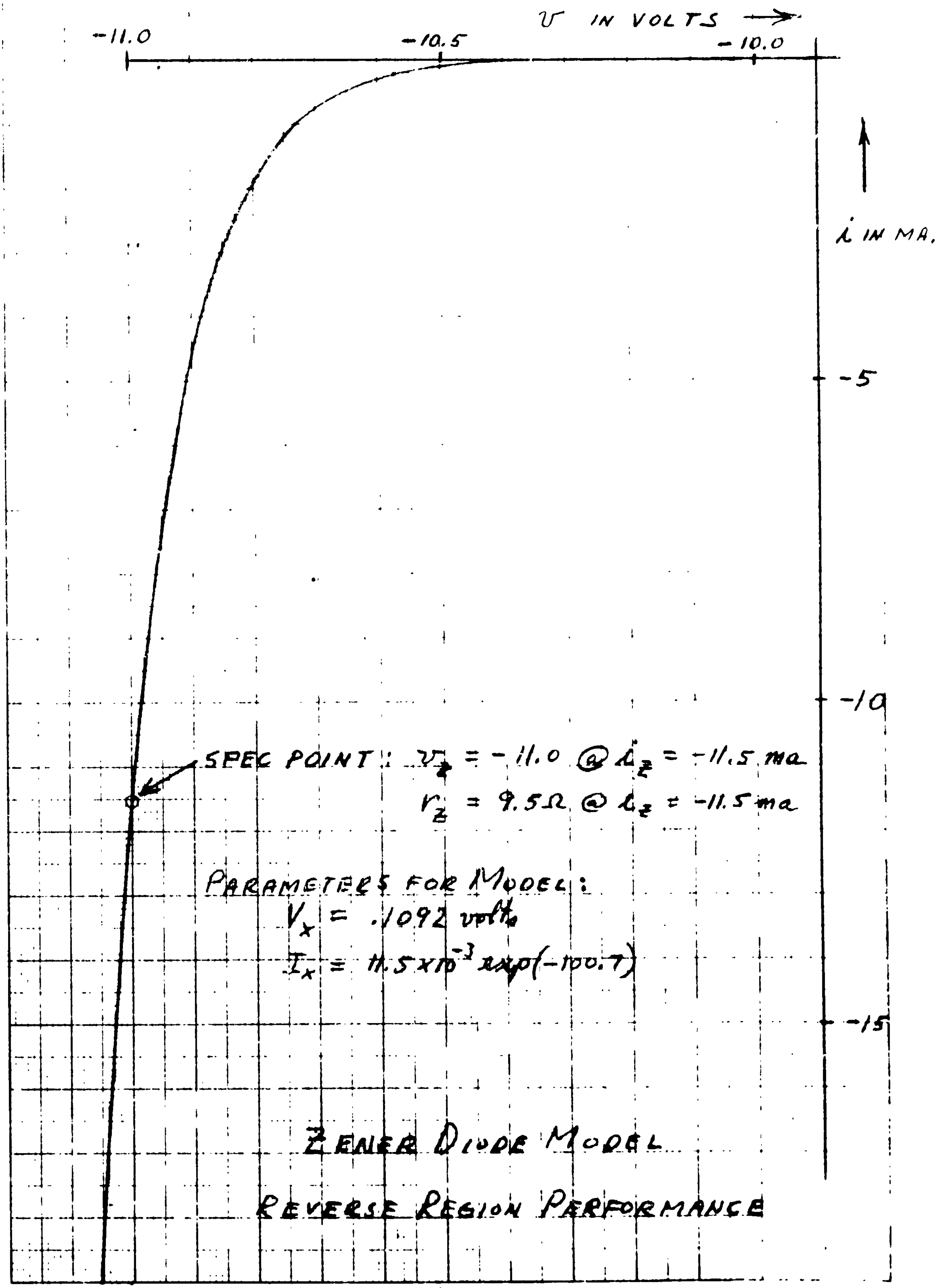
A check can now be made by calculating

$$-V_x \left(\ln\left(-i_2/I_x\right) + 1\right) + i_2 R_{SER}$$

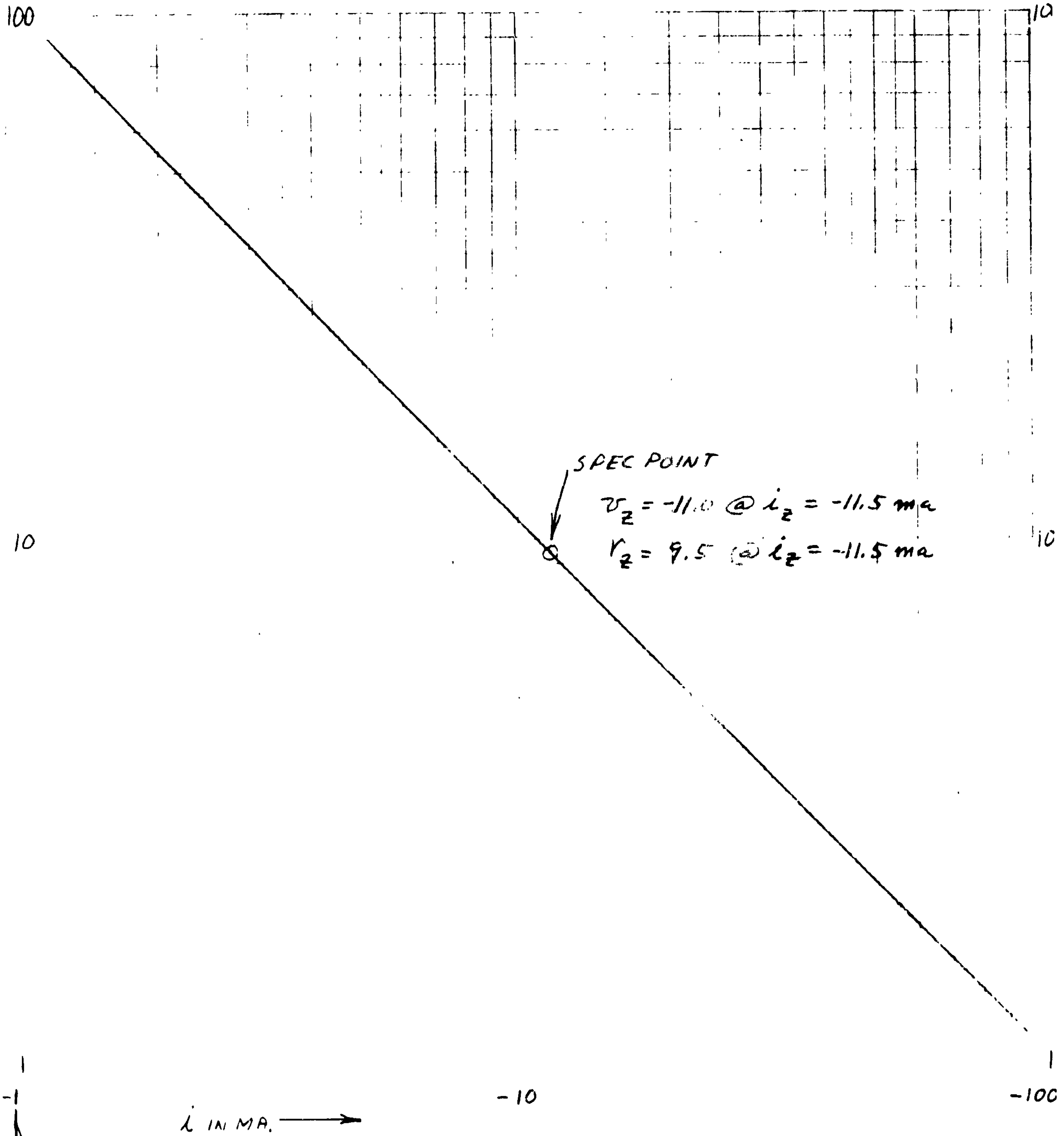
and comparing with the measured v_2.

D. Zener Diode Subroutine

```
      SUBROUTINE ZDIODE (VFD,FID,CTD,DATA,FIDI,LALGFT,KTDC)
C     NON-LINEAR ZENER DIODE MODEL
C     ARG(1) = VFD         DIODE TERMINAL VOLTAGE (PLUS FOR P POS)
C     ARG(2) = FID         DIODE BRANCH CURRENT (PLUS FOR FLOW P TO N)
C     ARG(3) = CTD         DIODE TOTAL TERMINAL CAPACITANCE
C     ARG(4) = DATA        DIODE PARAMETER ARRAY
C     ARG(5) = FIDI        DIODE INITIAL CURRENT
C     ARG(6) = LALGFT      FLAG = 1 ON FIRST PASS THROUGH SUBROUTINE
C     ARG(7) = KTDC        FLAG = 1 FOR DC CASE, = 0 FOR TRANSIENT
C     BULK RESISTANCE MUST BE INCLUDED IN EXTERNAL CIRCUIT IF DESIRED
C     DATA(1) = IS         REVERSE SATURATION CURRENT
C     DATA(2) = GL         REVERSE LEAKAGE CONDUCTANCE
C     DATA(3) = TAU        CHARGE RECOVERY TIME CONSTANT
C     DATA(4) = VK         DIODE CONTACT POTENTIAL
C     DATA(5) = N          JUNCTION GRADING CONSTANT
C     DATA(6) = K          DEPLETION CAPACITANCE CONSTANT
C     DATA(7) = CSD        STRAY AND CASE CAPACITANCE
C     DATA(8) = VO         THERMAL POTENTIAL KT/Q
C     DATA(9) = IX         ZENER CURRENT CONSTANT
C     DATA(10)= VX         ZENER VOLTAGE CONSTANT
      DIMENSION DATA(10)
      IF(KTDC-1) 10,1,1
    1 IF(LALGFT-1) 5,5,10
C     ID = ID(INITIAL)
    5 FID= FIDI
      GO TO 15
C     ID = VD*GL + IS*(EXPF(VD/VO)-1)-IX*(EXPF(-VD/VX)-1)
   10 FIC= DATA(1)*(EXPF(VFD/DATA(8))-1.)
      FIX= DATA(9)*(EXPF(-VFD/DATA(10))-1.)
      FID= VFD*DATA(2)+FIC-FIX
      IF(KTDC-1) 11,15,15
C     CTD= CSD + K/((VK-VD)**N) + (TAU/VO)*(FIC+IS)
   11 CTD= DATA(7)+DATA(6)/((DATA(4)-VFD)**DATA(5))+(DATA(3)/DATA(8))
     1*(FIC+DATA(1))
   15 CONTINUE
      RETURN
      END
```



v IN VOLTS →
-11.0
-10.5
-10.0
i IN MA.
-5
-10
-15
SPEC POINT: $v_z = -11.0$ @ $i_z = -11.5$ ma
$r_z = 9.5\Omega$ @ $i_z = -11.5$ ma
PARAMETERS FOR MODEL:
$V_x = .1092$ volts
$I_x = 11.5 \times 10^{-3} \exp(-100.7)$
ZENER DIODE MODEL
REVERSE REGION PERFORMANCE



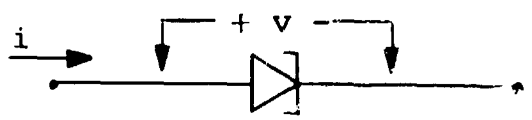
ZENER DIODE MODEL

RESISTANCE VS CURRENT

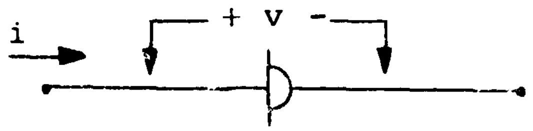
V. TUNNEL DIODE MODEL

A. Model Description

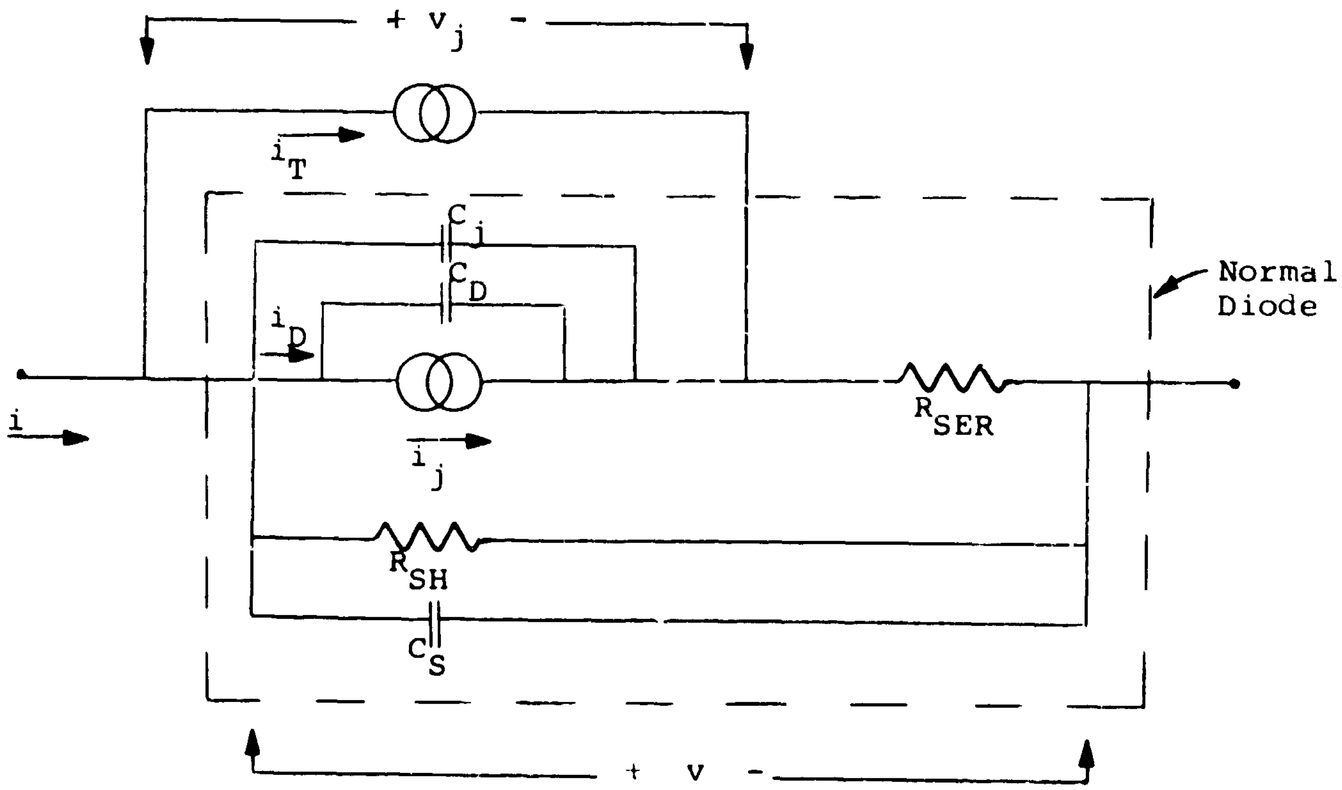
For a tunnel diode, normally symbolized as follows,



or as follows,



a model may be developed which consists of the ordinary diode model plus an additional non-linear current generator to represent the tunneling behavior at small positive and negative voltages. This model is as follows,



With the exception of the tunnel current generator, i_T, the model is identical with that of the normal diode. An empirical equation was developed for i_T as follows,

$$i_T = \frac{v_j}{R_T} \exp(-v_j/V_T)$$

where both R_T and V_T are positive constants.

The equations for the 3 non-linear normal diode components are repeated here

$$i_j = I_S (\exp(v_j/V_o) - 1)$$

$$C_j = \frac{K}{(V_K - v_j)^N}$$

$$C_D = \tau \frac{di_j}{dv_j}$$

B. Model Performance

1. Static Forward Behavior

The forward behavior is that of the normal diode in parallel with the tunnel current generator.

By differentiating the tunnel current expression with respect to v_j, the slope of the tunnel current characteristic is

$$\frac{di_T}{dv_j} = \frac{1}{R_T}\left(1 - \frac{v_j}{V_T}\right) \exp(-v_j/V_T) \; .$$

It is evident that this derivative represents the small signal tunnel conductance, g_T. Thus

$$g_T = \frac{di_T}{dv_j}$$

It can be seen that

$$\text{for} \quad v_j < V_T, \; g_T > 0$$

$$\text{for} \quad v_j = V_T, \; g_T = 0$$

$$\text{for} \quad v_j > V_T, \; g_T < 0$$

Thus the tunnel conductance changes from positive to negative polarity at $v_j = V_T$. Therefore, V_T is the approximate peak point of the diode, as the normal diode current generator, i_j, has very little effect at the low V_T voltage.

The presence of the exponential multiplier in the expression for i_T makes i_T decrease rapidly as the forward voltage increases beyond V_j. The decreasing i_T, when summed with an increasing i_j, results in a valley point of minimum current. At forward voltages greater than this valley point, the normal diode current, i_j, increasingly dominates the behavior. Thus the overall small signal conductance becomes positive as the normal diode slope, g_D, dominates the decreasing negative g_T.

2. Static Reverse Behavior

The reverse behavior is dominated by the tunnel current generator. The equation for i_T may be re-arranged.

$$\frac{v_j}{i_T} = R_T \exp\,(v_j/V_T)$$

This ratio may be defined as the large-signal tunnel resistance as it represents a vector from the origin to the operating point. It is evident that, for increasing negative voltages, this large-signal resistance decreases from a value of R_T for $v_j = 0$. Thus the reverse current rises ever more steeply for increasing negative voltages.

Accurate modeling of reverse behavior is often of little or no importance in tunnel diode applications.

3. Dynamic Behavior

The dynamic behavior is due primarily to the interaction of the static "N-shaped" i-v characteristic and the junction capacitance.

C. Parameter Evaluation

1. Normal Diode Static Parameters

V_o, I_S, and R_{SER} are the parameters to be evaluated as R_{SH} can be regarded as infinite in value. The evaluation of these parameters is somewhat more complex than it is for an "ordinary" diode because of the presence of the tunnel current generator.

To simplify the problem somewhat we shall here assume that $R_{SER} = 0$. Thus, it is necessary to evaluate only the parameters V_o and I_s. This may be done from 2 suitable data points.

One such point is V_{FP}, I_P, the Forward Peak Point. As i_T, the tunnel generator current, is virtually zero at this point, the data may be used directly in the diode equation as follows:

$$I_p \cong I_s \exp (V_{FP}/V_o)$$

The second suitable data point is the valley point. However, as both the tunnel generator, i_T, and the normal diode generator, i_j, contribute current at the valley point, the following equation is used:

$$I_v - i_{TV} \cong I_s \exp (V_v / V_o)$$

where $i_{TV} = i_T$ at $v = V_v$

These two equations may be solved for V_o and I_s after i_{TV} is determined from the tunnel current generator equation.

2. V_T

A data point at the peak point current and voltage, i_p and v_p, can be used to evaluate V_T. Assuming

$$V_T \cong v_p$$

3. R_T

a. Switch Diodes - For tunnel diodes that are used as switches, R_T should be evaluated so as to satisfy the peak point data, I_p, V_p . From the tunnel generator equation,

$$R_T = \frac{V_p}{I_p} \exp\ (- V_p/V_T)$$

where

$$V_T = V_p$$

Thus, $R_T = .369\frac{V_p}{I_p}$

b. Amplifier Diodes - For tunnel diodes that are used as small-signal negative resistance amplifiers, R_T should be evaluated to satisfy a negative small signal conductance data point, g_{N1} at i_{N1}, v_{N1}. Assuming that i_j contributes negligibly to g_{N1},

$$R_T = \frac{1}{g_{T1}} (1 - \frac{v_{jN1}}{V_T}) \exp(-v_{jN1}/V_T)$$

where

$$v_{jN1} = v_{N1} - i_{N1} R_{SER}$$

and

$$g_{T1} = g_{N1} - \frac{1}{R_{SER}}$$

Sometimes the available data takes the form of a maximum negative small-signal conductance, $g_{N\ MAX}$, at unspecified i_{NM} and v_{NM}. By differentiating the equation for g_T,

$$\frac{dg_T}{dv_T} = (2 - \frac{v_j}{V_T}) \left(\frac{-\exp(-v_j/V_T)}{R_T V_T} \right)$$

it is apparent that the maximum g_T occurs at $v_j = 2\ V_T$. Thus $g_{N\ MAX}$ occurs at $v_{NM} = 2\ V_T$. Also

$$i_{NM} = \frac{v_{NM}}{R_T} \exp \left(\frac{-v_{NM}}{V_T} \right)$$

$$i_{NM} = \frac{2\ V_T}{R_T} \exp\ (-2)$$

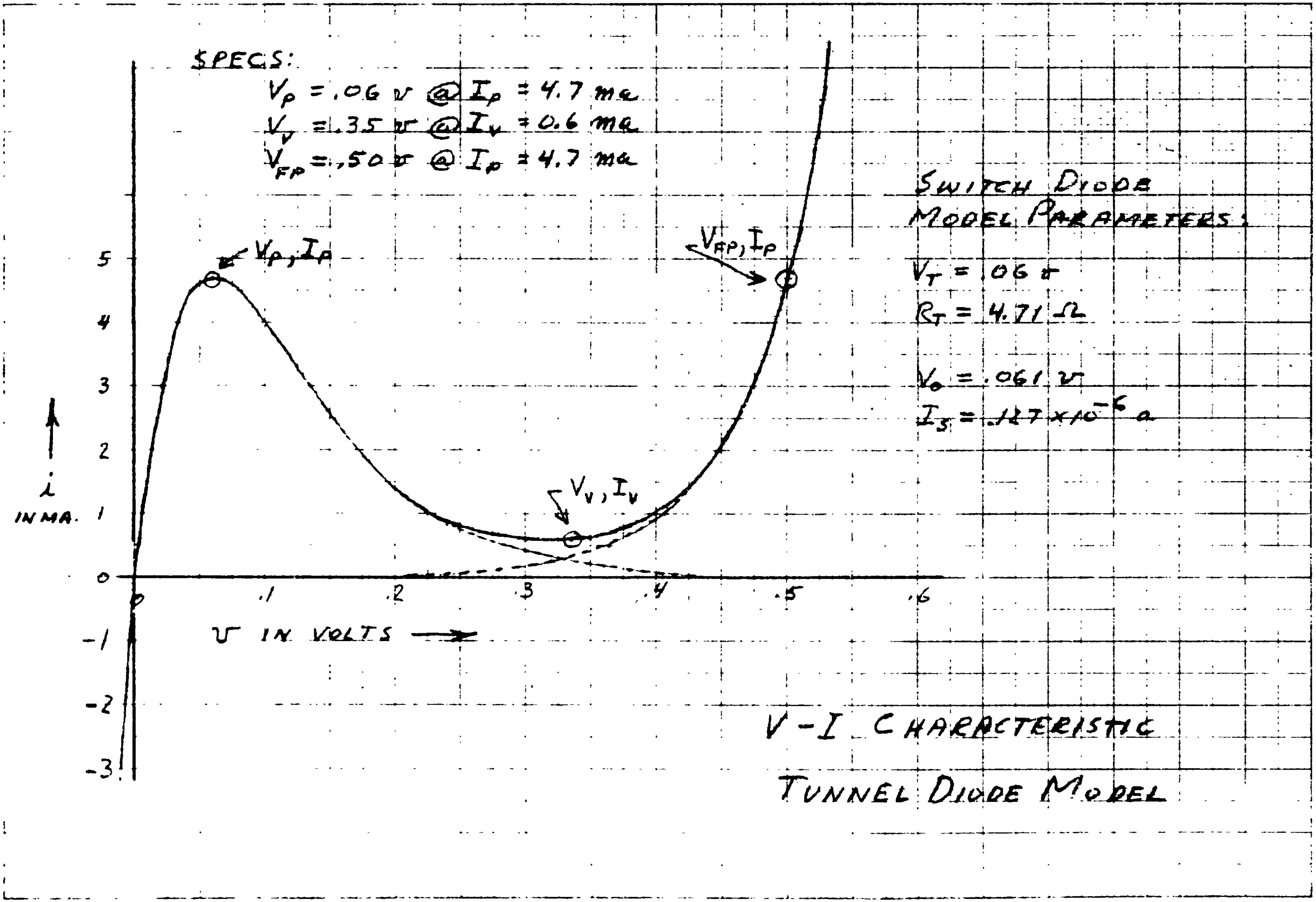
The equation for R_T becomes

$$R_T = \frac{1}{g_{TM}} \left(1 - \frac{2\ V_T}{V_T} \right) \exp(-2)$$

$$R_T = \frac{-.135}{g_{TM}}$$

where

$$g_{TM} = g_{NM} - \frac{1}{R_{SER}}$$



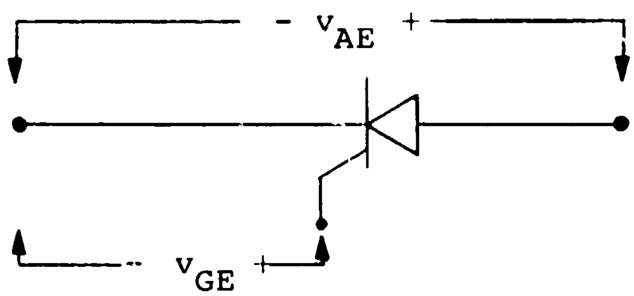
V-I CHARACTERISTIC

TUNNEL DIODE MODEL

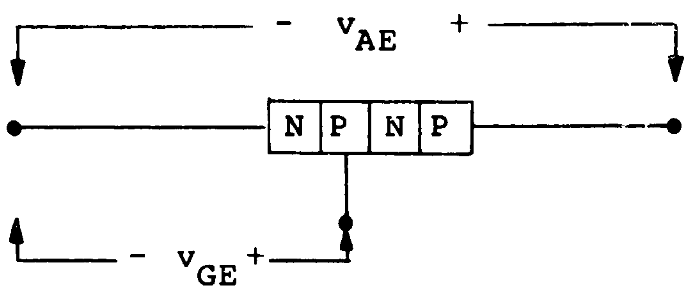
VI. CONTROLLED RECTIFIER MODEL

A. Model Description

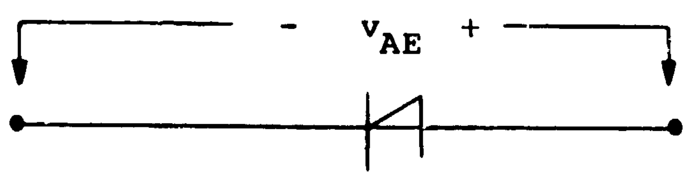
The controlled rectifier is one member of the family of PNPN 3-junction devices. The distinguishing feature of the controlled rectifier is that it is a 3-terminal device. It is usually symbolized as follows,



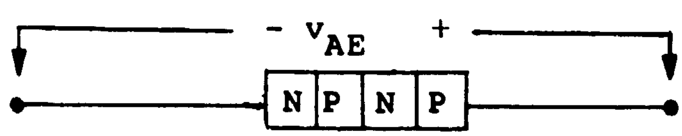
and sometimes symbolized as follows,



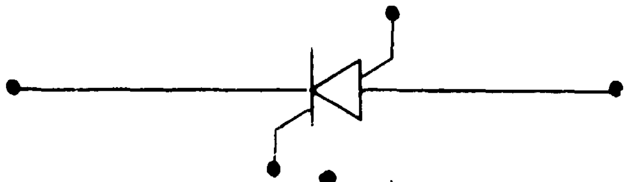
The 2-terminal member of the family is the 4-layer diode, symbolized as



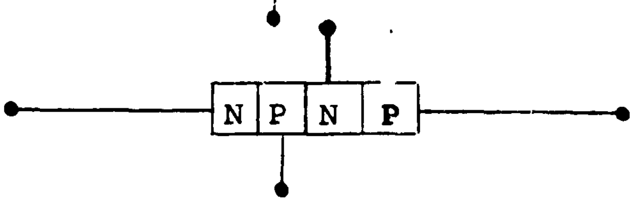
or



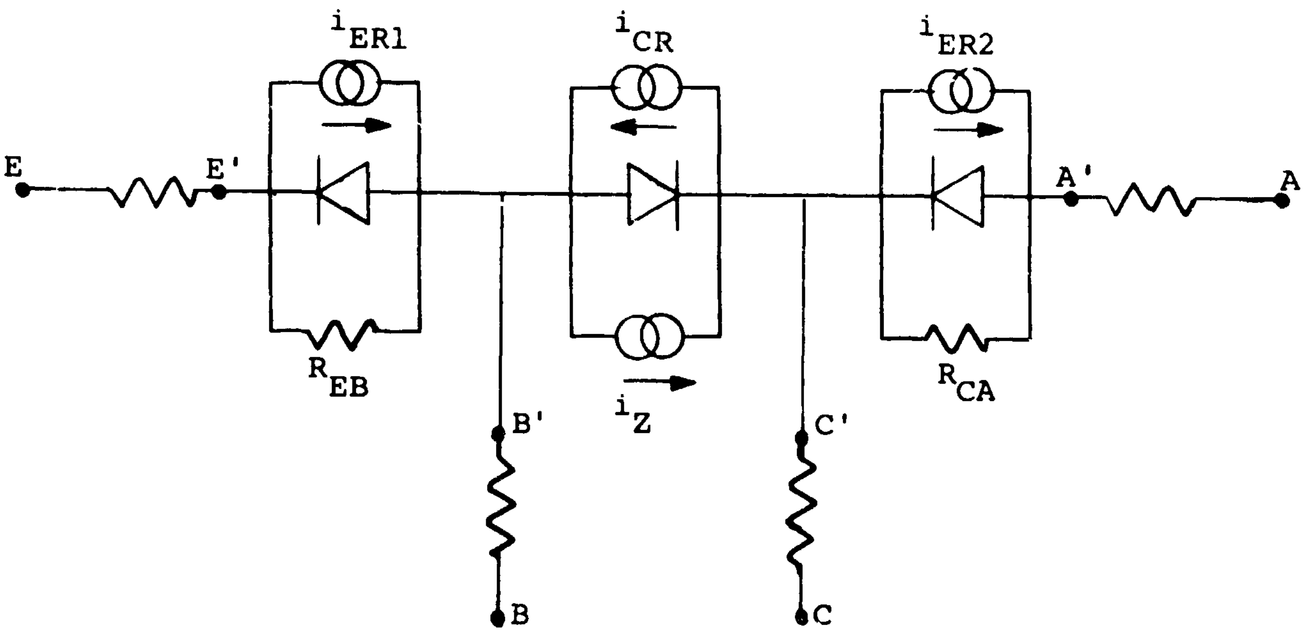
The 4-terminal member, sometimes called a controlled switch, is symbolized as



or

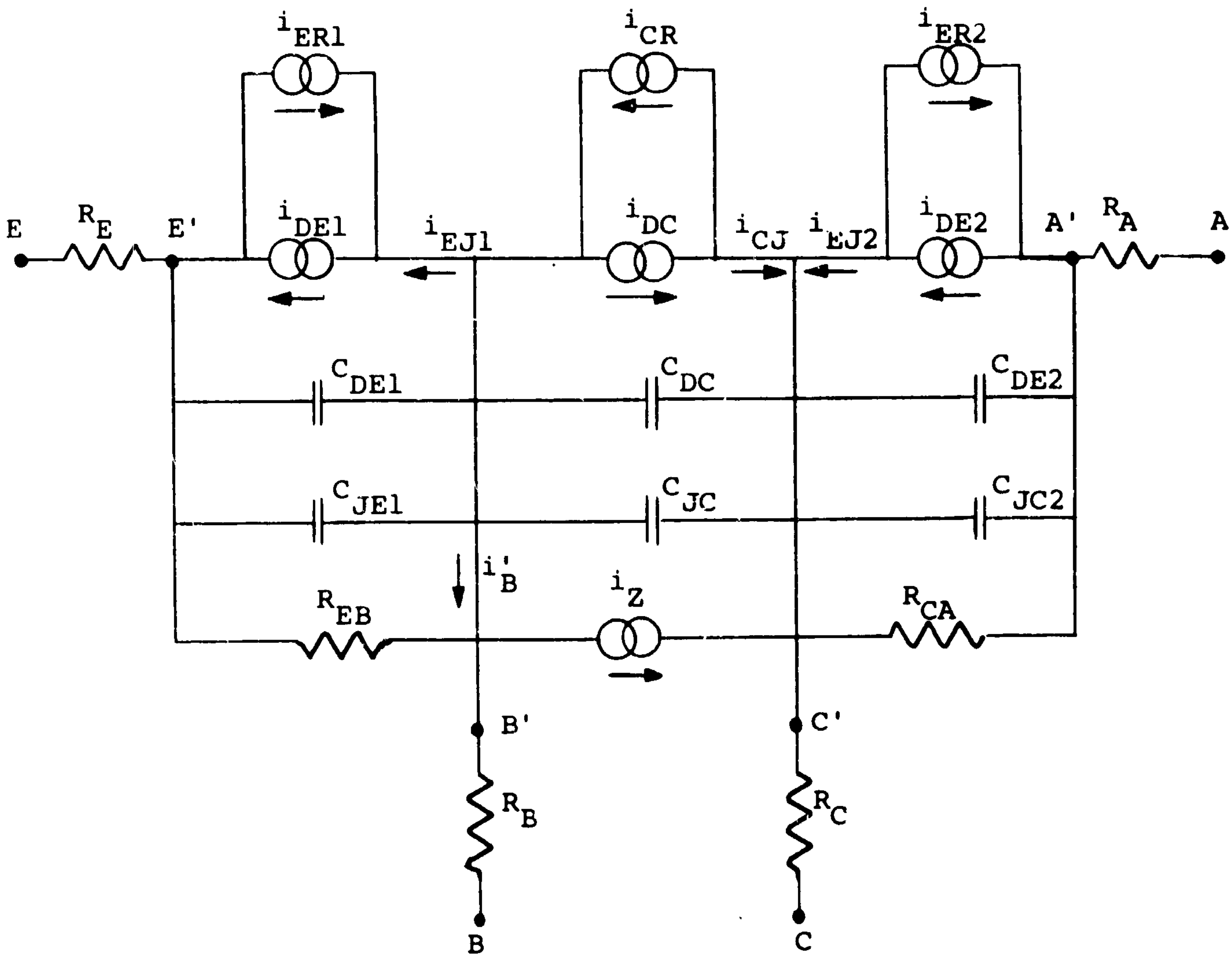


The model used here for all of the PNPN devices is an extension of the Ebers-Moll type of diode and transistor model. In terms of a diode sub-model, it appears as follows,



The 3 diodes are representive of the 3 junctions; the 3 upper current generators model the transportation of current carrier through the device. The i_{CR} generator develops a current proportional to conductive currents in each of the end diodes, with α_{N1} and α_{N2} as proportionality constants. The i_{ER1} and i_{ER2} generators develop currents related by α_{I1} and α_{I2} to the center diode current. The shunt resistors R_{EB} and R_{CA} produce the effects of current dependent normal alphas that are vital to the base or collector triggering properties of the model. The zener current generator across the center junction provides an effect similar to the voltage dependency of alpha that results in anode triggering.

Replacing the diode symbols with Ebers-Moll diode models results in a detailed model as follows.



The equations for the model current generators are as follows.

For the "diode" current generators:

$$i_{DE1} = I_{SE1} \; (\exp(v'_{BE}/V_o) \; -1)$$

$$i_{DC} = I_{SC} \; (\exp(v'_{BC}/V_o) \; -1)$$

$$i_{DE2} = I_{SE2} \; (\exp(v'_{AC}/V_o) \; -1)$$

For the "transport" current generators:

$$i_{ER1} = \alpha_{I1} i_{CJ}$$

$$i_{CR} = \alpha_{N1} i_{EJ1} + \alpha_{N2} i_{EJ2}$$

$$i_{ER2} = \alpha_{I2} i_{CJ}$$

The alphas and the saturation currents are related by,

$$I_{SC}/I_{SE1} = \alpha_{N1}/\alpha_{I1}$$

$$I_{SC}/I_{SE2} = \alpha_{N2}/\alpha_{I2}$$

For the "zener" current generators,

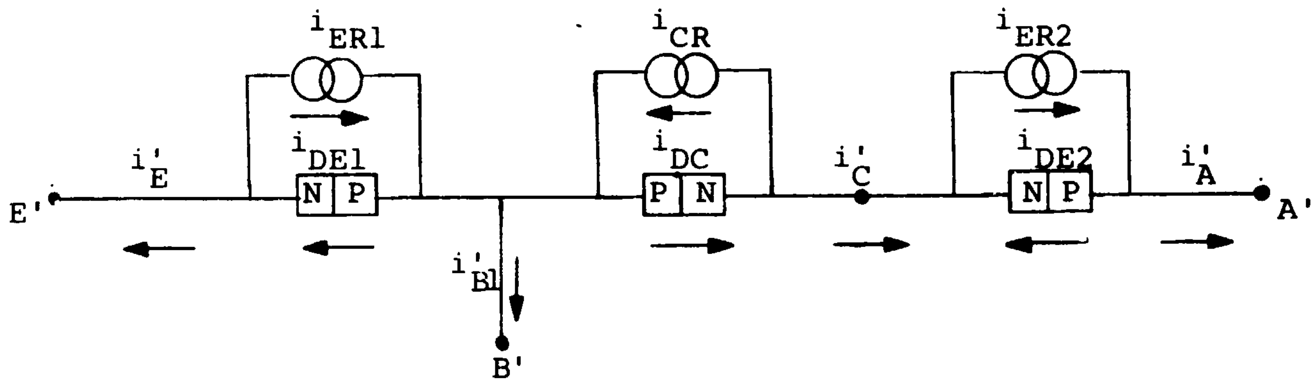
$$i_Z = -I_x(\exp(-v_{BC}/V_x)-1)$$

All of the constants above are positive.

B. Model Performance

1. Analytic Solutions of Static Equations

Because of the complexity of the model, equations will be developed initially for a model with no series resistors, shunt resistors, or zener current generators. Also, for static equations, all junction and diffusion capacitors are omitted. The resulting simplified model appears as follows,



The equations for the 3 PN junctions are:

$$i_{DE1} = I_{SE1}(\exp(v'_{BE}/V_o)-1) \quad (1)$$

$$i_{DC} = I_{SC}\,(\exp(v'_{BC}/V_o)-1) \quad (2)$$

$$i_{DE2} = I_{SE2}(\exp(v'_{AC}/V_o)-1) \quad (3)$$

For the 3 current generators,

$$i_{ER1} = \alpha_{I1} i'_C \quad (4)$$

$$i_{CR} = \alpha_{N1} i'_E - \alpha_{N2} i'_A \quad (5)$$

$$i_{ER2} = \alpha_{I2} i'_C \quad (6)$$

The constraints on the alphas are,

$$I_{SC}/I_{SE1} = \alpha_{N1}/\alpha_{I1} \tag{8}$$

$$I_{SC}/I_{SE2} = \alpha_{N2}/\alpha_{I2} \tag{9}$$

From the topology,

$$i'_E = i_{DE1} - i_{ER1} \tag{10}$$

$$i'_C = i_{DC} - i_{CR} \tag{11}$$

$$-i'_A = i_{DE2} - i_{ER2} \tag{12}$$

Substituting (4), (5), and (6):

$$i'_E = i_{DE1} - \alpha_{I1} i'_C \tag{10a}$$

$$i'_C = i_{DC} - \alpha_{N1} i'_E + \alpha_{N2} i'_A \tag{11a}$$

$$-i'_A = i_{DE2} - \alpha_{I2} i'_C \tag{12a}$$

Thus the PN junction currents in terms of the external currents are

$$i_{DE1} = i'_E + \alpha_{I1} i'_C \tag{10b}$$

$$i_{DC} = i'_C + \alpha_{N1} i'_E - \alpha_{N2} i'_A \tag{11b}$$

$$i_{DE2} = -i'_A + \alpha_{I2} i'_C \tag{12b}$$

From the topology

$$i'_{B1} + i'_E + i'_C = 0 \tag{13}$$

$$i'_C - i'_A = 0 \tag{14}$$

$$i'_E + i'_{B1} + i'_A = 0 \tag{15}$$

then

$$i_{DE1} = -i'_{B1} - i'_A + \alpha_{I1}(+i'_A) \tag{10c}$$

$$i_{DE1} = -i'_{B1} - i'_A\ (1-\alpha_{I1}) \tag{10d}$$

$$i_{DC} = +i'_A + \alpha_{N1}(-i'_{B1} - i'_A) - \alpha_{N2}i'_A \tag{11c}$$

$$i_{DC} = -\alpha_{N1}i'_{B1} + (1-\alpha_{N1} - \alpha_{N2})i'_A \tag{11d}$$

$$i_{DE2} = -i'_A + \alpha_{I2}(+i'_A) \tag{12c}$$

$$i_{DE2} = -(1-\alpha_{I2})i'_A \tag{12d}$$

Solving (1), (2), and (3) for the voltage across each junction,

$$v'_{BE} = V_o\ \ln(1 + (i_{DE1}/I_{SE1})) \tag{1a}$$

$$v'_{BE} = V_o\ \ln\left(\frac{I_{SE1} - i'_{B1} + (1-\alpha_{I1})(-i'_A)}{I_{SE1}}\right) \tag{16}$$

$$v'_{BC} = V_o\ \ln\ (1 + (i_{DC}/I_{SC})) \tag{2a}$$

$$v'_{BC} = V_o\ \ln\left(\frac{I_{SC} - \alpha_{N1}i'_{B1} + (1-\alpha_{N1} - \alpha_{N2})i'_A}{I_{SC}}\right) \tag{17}$$

$$v'_{AC} = V_o\ \ln\ (1 + (i_{DE2}/I_{SE2})) \tag{3a}$$

$$v'_{AC} = V_o\ \ln\left(\frac{I_{SE2} - (1-\alpha_{I2})\ i'_A}{I_{SE2}}\right) \tag{18}$$

For currents that are large compared to I_{SE1}, the 3 junction voltage equations can be simplified as follows:

$$v'_{BE} \cong V_o \ln\left(\frac{-i'_{B1} + (1-\alpha_{I1})(-i'_A)}{I_{SE1}}\right) \qquad (16a)$$

$$v'_{BE} \cong V_o \ln\left(\frac{-\alpha_{N1} i'_{B1} + (1-\alpha_{N1}-\alpha_{N2}) i'_A}{I_{SC}}\right) \qquad (17a)$$

$$v'_{AC} \cong V_o \ln\left(\frac{(1-\alpha_{I2})(-i'_A)}{I_{SE2}}\right) \qquad (18a)$$

For very small α_{I1} and α_{I2}, the above equations may be further simplified.

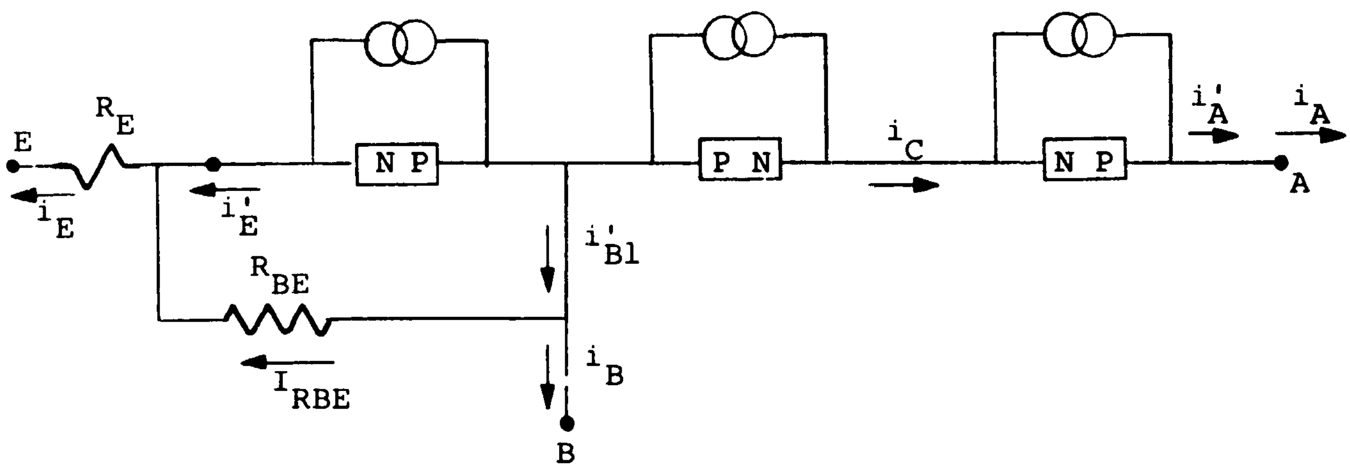
$$v'_{BE} \cong V_o \ln\left(\frac{-i'_{B1} - i'_A}{I_{SE1}}\right) \qquad (16b)$$

$$v'_{BC} \cong V_o \ln\left(\frac{-\alpha_{N1} i'_{B1} + (1-\alpha_{N1}-\alpha_{N2}) i'_A}{I_{SC}}\right) \qquad (17b)$$

$$v'_{AC} \cong V_o \ln\left(\frac{-i'_A}{I_{SE2}}\right) \qquad (18b)$$

At this point, we shall add to the basic model above, those components that are needed for a complete model. The most important component to be added is R_{BE}, the resistor shunting the base-emitter junction. It will be shown that adding this resistor produces the effect of an α_N that increases with current, which is fundamentally necessary for SCR operation. Additionally R_E, a series emitter resistor, is used to provide a saturation anode voltage that increases with high anode current. The remaining series and shunt resistors are not vital to a model that is not intended to be too precise. Also, as SCR's are seldom anode voltage triggered, the zener current generator that simulates this effect is omitted.

Thus the following complete static model will be used for the SCR.



The "unprimed" and "primed" currents are related as follows:

$$i_E' = i_E - i_{RBE} \tag{19}$$

$$i_{B1}' = i_B + i_{RBE} \tag{20}$$

$$i_A' = i_A \tag{21}$$

where

$$i_{RBE} = v_{BE}'/R_{BE} \quad . \tag{22}$$

The "primed" voltage equations become

$$v_{BE}' \cong V_o \ln\left(\frac{-i_B - i_{RBE} - i_A}{I_{SE1}}\right) \tag{16c}$$

$$v'_{BC} \cong V_o \ \ln\left(\frac{-\alpha_{N1}(i_B+i_{RBE})+(1-\alpha_{N1}-\alpha_{N2})\,i_A}{I_{SC}}\right) \tag{17c}$$

$$v'_{AC} \cong V_o \ \ln\left(\frac{-i_A}{I_{SE2}}\right) \tag{18c}$$

Equations for the 2 important external voltages are:

$$v_{BE} = v'_{BE} + i_E \times R_E \tag{24}$$

$$v_{BE} = v'_{BE} - (i_B + i_A)\ R_E \tag{24a}$$

$$v_{AE} = v'_{AC} - v'_{BC} + v'_{BE} + i_E R_E \tag{25}$$

$$v_{AE} = v'_{AC} - v'_{BC} + v'_{BE} - (i_B + i_A)\ R_E \tag{25a}$$

Among the 4 terms in the expression for v_{AE}, it is $-v'_{BC}$, the voltage across the center junction that is of most interest. It is now examined in greater detail.

a. <u>Saturation Region</u>:

The saturation region is distinguished from the normal active region by

$$v'_{BC} > 0 \tag{26}$$

Therefore from (17c), $-\alpha_{N1}(i_B+i_{RBE})+(1-\alpha_{N1}-\alpha_{N2})\,i_A > I_{SC}$ or, as $I_{SC} \ll i_{RBE}$,

$$-\alpha_{N1}(i_B+i_{RBE})+(1-\alpha_{N1}-\alpha_{N2})\,i_A > 0 \tag{27a}$$

$$-i_A > \frac{\alpha_{N1} i_{RBE} - \alpha_{N1}(-i_B)}{\alpha_{N1} + \alpha_{N2} - 1} \tag{27b}$$

The above equation is written in terms of $-i_A$ and $-i_B$, as polarities chosen are such as to make these quantities normally positive.

The shunt resistor current, i_{RBE}, is a function of the junction voltages, which prevents a simple exact explicit solution of the equations. However, useful results may be made by assuming i_{RBE} to be constant, which is approximately true for all but very small and very large base and anode currents.

Note here that for the model chosen, the alphas are constants. Also to fit SCR performance wherein an anode current greater than some minimum can be supported in saturation with zero base current, it is necessary that

$$\alpha_{N1} + \alpha_{N2} > 1 \ . \tag{28}$$

From (27b) it is apparent that

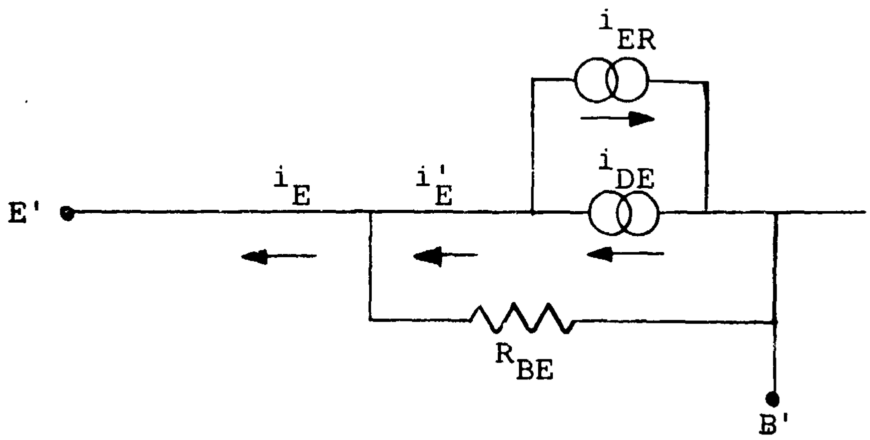
$$\text{for } -i_B = 0, \quad -i_A \underset{\sim}{>} \frac{\alpha_{N1} i_{RBE}}{\alpha_{N1} + \alpha_{N2} - 1} \tag{27d}$$

$$\text{for } -i_A = 0, \quad -i_B \underset{\sim}{>} i_{RBE} \tag{27e}$$

Equation (27d) approximately defines the Holding Current, the minimum anode current that will be supported in saturation with no base current. Equation (27e) indicates what is apparent from the model schematic, that the base current must be greater than the current in the shunt base-emitter resistor to provide saturation with zero anode current.

b. Effective Alpha-normal vs. Actual Alpha-normal:

At this point it is of value to examine in greater detail the interaction between the emitter diode shunt resistor, R_{BE}, and the constant α_{N1} that produces an effective alpha normal, α'_{N1}, that increases with current. The D.C. base-emitter circuit is as follows:



From (16), for current large compared with I_{SE1} and for negligably small α_{I1},

$$v'_{BE} = V_o \ln \frac{-i'_{B1} - i'_A}{I_{SE1}}$$

From (15)

$$v'_{BE} = V_o \ln \frac{i'_E}{I_{SE1}}$$

The normal alpha affects model performance through (5)

$$i_{CR} = \alpha_{N1} i'_E - \alpha_{N2} i'_A \tag{5}$$

We may write an equation similar to (5) using α'_{N1} and i_E:

$$i_{CR} = \alpha'_{N1} i_E - \alpha_{N2} i'_A \tag{5a}$$

thus

$$\alpha'_{N1} i_E = \alpha_{N1} i'_E$$

and

$$\alpha'_{N1} = \alpha_{N1} \frac{i'_E}{i_E}$$

From the topology,

$$i_E = i'_E + v'_{BE}/R_{BE}$$

$$i_E = i'_E + \frac{V_o}{R_{BE}} \ln \frac{i'_E}{I_{SE1}}$$

thus,

$$\alpha'_{N1} = \alpha_{N1} i'_E/(i'_E + \frac{V_o}{R_{BE}} \ln \frac{i'_E}{I_{SE1}})$$

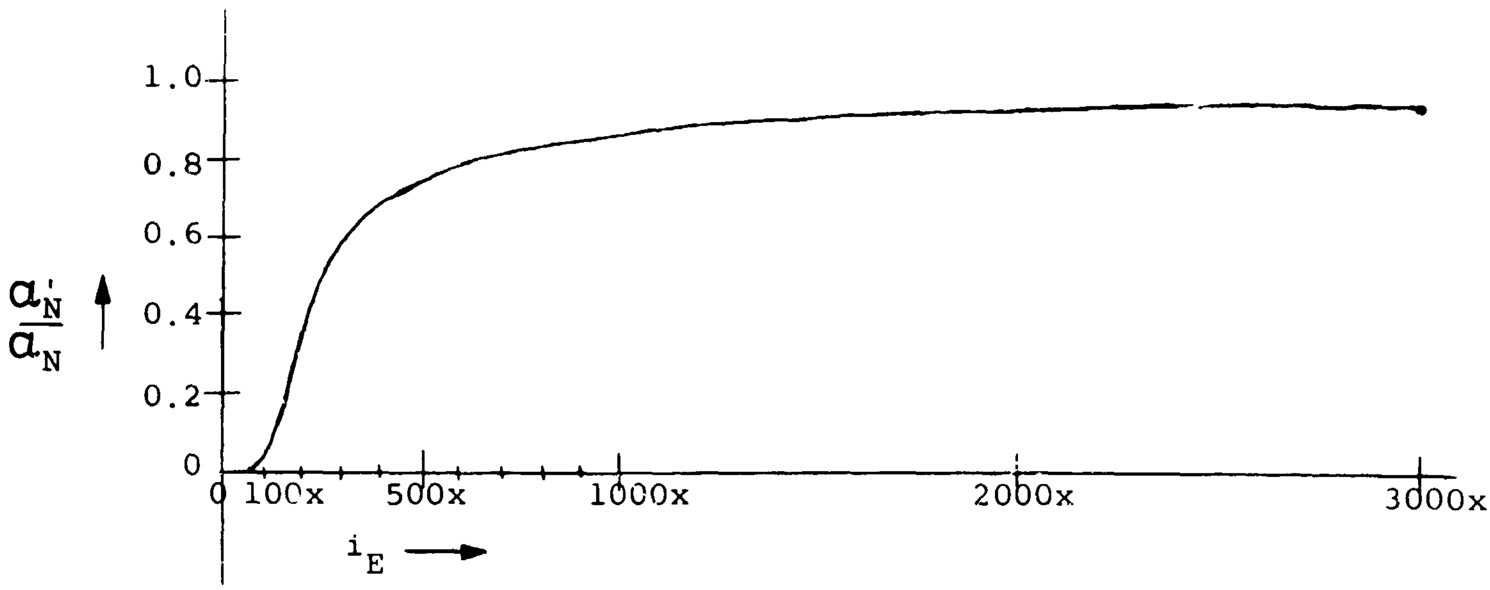
By arbitrarily assuming some values, this expression may be plotted.

Assume $i'_E = x$ @ $v'_{BE} = .500$

and $i_{RBE} = 100x$ @ $v'_{BE} = .500$

and $\frac{V_o}{\ } = .026$

For these values, α'_{N1}/α_{N1} vs. i_E is plotted below on a linear scale



It is evident for the example values that α'_N, the effective alpha, increases rapidly for emitter currents from 100x to 500x and more gradually thereafter.

c. Normal Active Region:

The normal active region is defined by

$v'_{BE} > 0$, $v'_{AC} > 0$, and

$$v'_{BC} < 0 \tag{29}$$

Therefore, similar to (27b),

$$-i_A < \frac{\alpha_{N1} i_{RBE} - \alpha_{N1}(-i_B)}{\alpha_{N1} + \alpha_{N2} - 1} \tag{30}$$

The Normal Active Region may be further divided into a Forward Blocking Region and a Negative Anode Resistance Region. In the Forward Blocking Region, normal transistor behavior is displayed. As base or anode current is further increased, the small signal resistance, $r_A = -dv_{AE}/di_A$, decreases from a large positive value and becomes negative. Once in this Negative Anode Resistance Region, increasing current will drive the device to the Saturation Region.

d. <u>Small Signal Anode Resistance</u>:

An approximate expression for r_A, the small signal anode resistance or slope of the anode V - I characteristic, may be obtained as follows. For the region where currents are large compared to the saturation currents and where I_{RBE} is reasonably approximated as constant, (25a) may be differentiated with respect to i_A.

$$r_A = \frac{-dv_{AE}}{di_A} = -\frac{dv'_{AC}}{di_A} + \frac{dv'_{BC}}{di_A} - \frac{dv'_{BE}}{di_A} + R_E$$

where

$$\frac{-dv'_{AC}}{di_A} = V_o \frac{1}{-i_A}$$

and

$$\frac{dv'_{BC}}{di_A} = V_o \frac{\alpha_{N1} + \alpha_{N2} - 1}{\alpha_{N1}(i_B + i_{RBE}) + (\alpha_{N1} + \alpha_{N2} - 1) i_A}$$

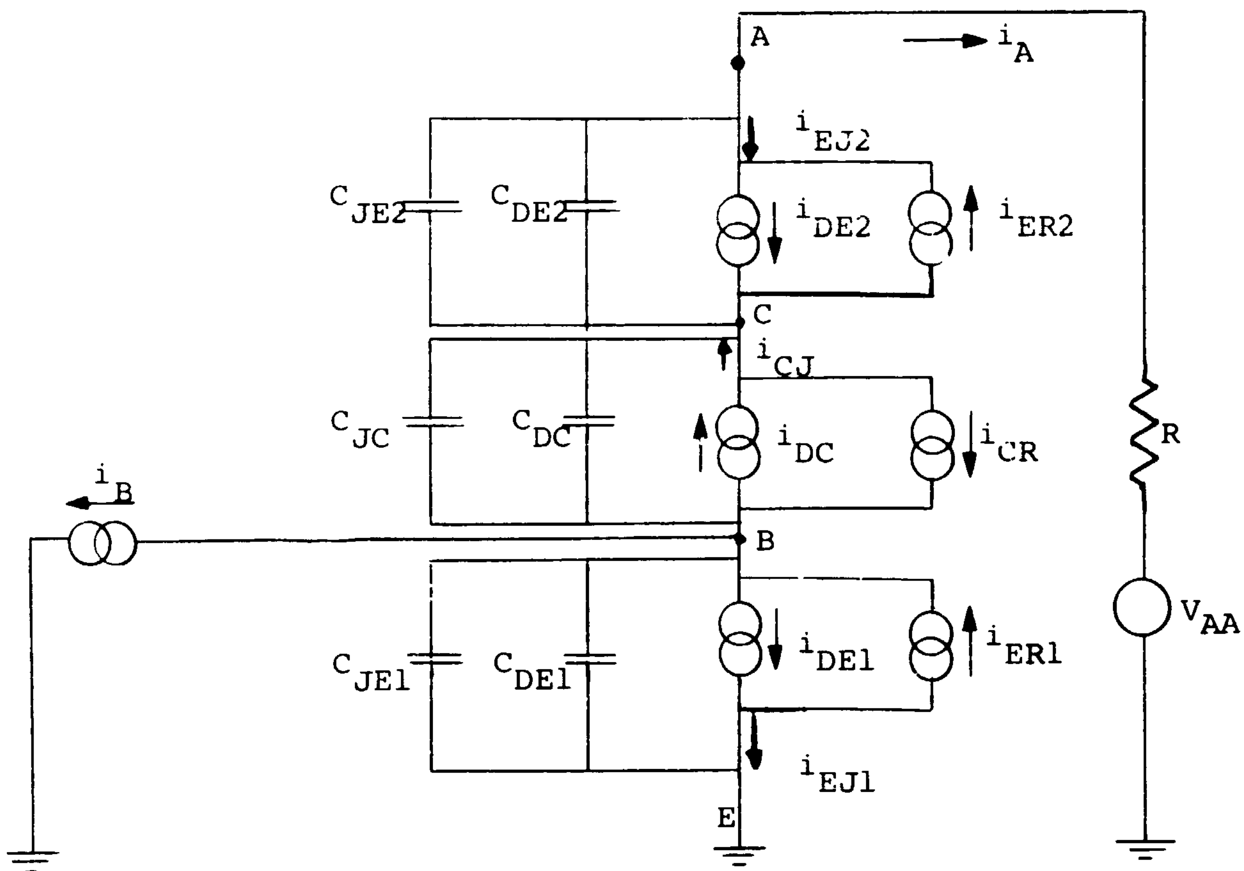
and

$$-\frac{dv'_{BE}}{di_A} = V_o \frac{1}{-i_B - i_{RBE} - i_A}$$

It is apparent that the small signal resistances of the emitter and anode diodes are positive resistances that decrease with increasing current, and that the center or collector diode develops the negative resistance.

2. Analytic Solutions of SCR Dynamic Equations

The approximate step-response will be developed for the simplified circuit below.



a. Turn-on Step Response:

As the current level is usually quite large, the junction capacitances contribute little and thus will be valued at zero. Also, as the center diode is back biased, C_{DC} is very small during the transient and thus will be valued at zero.

The following equations will develop the collector current response to a base current step.

Summing currents at the base, collector, and anode nodes provides the 3 basic equations.

$$i_B + i_{EJ1} + i_{CJ} + C_{DE1} \frac{dv_{BE}}{dt} = 0 \tag{1}$$

$$i_{CJ} - i_A = 0 \tag{2}$$

$$i_A + i_{EJ2} + C_{DE2} \frac{dv_{AC}}{dt} = 0 \tag{3}$$

It is desired to solve the above equations for i_A in response to a step of i_B. To solve, note that from the topology,

$$i_{EJ1} = i_{DE1} - i_{ER1} \tag{4}$$

$$i_{CJ} = i_{DC} - i_{CR} \tag{5}$$

$$i_{EJ2} = i_{DE2} - i_{ER2} \tag{6}$$

and from the previous section,

$$i_{ER1} = \alpha_{I1} i_{CJ} \tag{7}$$

$$i_{CR} = \alpha_{N1} i_{EJ1} + \alpha_{N2} i_{EJ2} \tag{8}$$

$$i_{ER2} = \alpha_{I2} i_{CJ} \tag{9}$$

the 3 "transportation" current generators may be solved for in terms of the 3 "diode" current generators as follows,

$$i_{ER1} = \frac{-\alpha_{N1}\alpha_{I1} i_{DE1} + \alpha_{I1} i_{DC} - \alpha_{N2}\alpha_{I1} i_{DE2}}{1 - \alpha_{N2}\alpha_{I2} - \alpha_{N1}\alpha_{I1}} \qquad (10)$$

$$i_{CR} = \frac{\alpha_{N1} i_{DE1} - (\alpha_{N1}\alpha_{I1} + \alpha_{N2}\alpha_{I2}) i_{DC} + \alpha_{N2} i_{DE2}}{1 - \alpha_{N2}\alpha_{I2} - \alpha_{N1}\alpha_{I1}} \qquad (11)$$

$$i_{ER2} = \frac{-\alpha_{N1}\alpha_{I2} i_{DE1} + \alpha_{I2} i_{DC} - \alpha_{N2}\alpha_{I2} i_{DE2}}{1 - \alpha_{N2}\alpha_{I2} - \alpha_{N1}\alpha_{I1}} \qquad (12)$$

Substituting in (4), (5), (6), respectively,

$$i_{EJ1} = \frac{(1-\alpha_{N2}\alpha_{I2}) i_{DE1} - \alpha_{I1} i_{DC} + \alpha_{N2}\alpha_{I1} i_{DE2}}{D} \qquad (13)$$

$$i_{CJ} = \frac{-\alpha_{N1} i_{DE1} + i_{DC} - \alpha_{N2} i_{DE2}}{D} \qquad (14)$$

$$i_{EJ2} = \frac{\alpha_{N1}\alpha_{I2} i_{DE1} - \alpha_{I2} i_{DC} + (1-\alpha_{N1}\alpha_{I1}) i_{DE2}}{D} \qquad (15)$$

where

$$D = 1 - \alpha_{N2}\alpha_{I2} - \alpha_{N1}\alpha_{I1} \qquad (16)$$

At this point, the equations may be simplified a bit by noting that for the turn-on response it is a fair approximation to let $i_{DC} = 0$. Substituting (13) into (1),

$$i_B + K_1 i_{DE1} + K_2 i_{DE2} + C_1 \frac{dv_{BE}}{dt} = 0 \qquad (1a)$$

and as $\tau_{DE1} = C_{DE1} \dfrac{dv_{BE}}{di_{DE1}}$

$$i_B + K_1 i_{DE1} + K_2 i_{DE2} + \tau_{DE1} \frac{di_{DE1}}{dt} = 0 \qquad (1b)$$

Substituting (14) into (2),

$$K_5 i_{DE1} + K_6 i_{DE2} - i_A = 0 \qquad (2a)$$

Substituting (15) into (3),

$$i_A + K_3 i_{DE1} + K_4 i_{DE2} + C_2 \frac{dv_{AC}}{dt} = 0 \qquad (3a)$$

and as $\tau_{DE2} = C_{DE2} \dfrac{dv_{AC}}{di_{DE2}}$

$$i_A + K_3 i_{DE1} + K_4 i_{DE2} + \tau_{DE2} \frac{di_{DE2}}{dt} = 0 \qquad (3b)$$

where

$$K_1 = \frac{1 - \alpha_{N1} - \alpha_{N2}\alpha_{I2}}{D} \; ; \quad K_2 = \frac{\alpha_{N2}(\alpha_{I1} - 1)}{D}$$

$$K_3 = \frac{\alpha_{N1}\alpha_{I1}}{D} \; ; \quad K_4 = \frac{1 - \alpha_{N1}\alpha_{I2}}{D}$$

$$K_5 = \frac{-\alpha_{N1}}{D} \; ; \quad K_6 = \frac{-\alpha_{N2}}{D}$$

Taking Laplace transforms, from (1b),

$$I_B + K_1 I_{DE1} + K_2 I_{DE2} + \tau_{DE1} (I_{DE1} S - i_{DE10}) = 0 \qquad (1c)$$

where i_{DE10} is an initial condition having value of zero for the turn-on step response. Thus

$$I_B + (K_1 + \tau_{DE1} S) I_{DE1} + K_2 I_{DE2} = 0 \qquad (1d)$$

from (2a),

$$K_5 I_{DE1} + K_6 I_{DE2} - I_A = 0 \qquad (2b)$$

from (3b),

$$I_A + K_3 I_{DE1} + K_4 I_{DE2} + \tau_{DE2} (I_{DE2} S - i_{DE20}) = 0 \qquad (3c)$$

where i_{DE20} is an initial condition having value of zero for the turn-on step response. Thus,

$$I_A + K_3 I_{DE1} + (K_4 + \tau_{DE2} S) I_{DE2} = 0 \qquad (3d)$$

Substituting (2b) into (1d),

$$I_B + \frac{K_1 + \tau_{DE1} S}{K_5} I_A + \frac{K_2 K_5 - (K_1 + \tau_{DE1} S) K_6}{K_5} I_{DE2} = 0 \qquad (17)$$

Substituting (2b) into (3d)

$$\frac{K_5 + K_3}{K_5} I_A + \frac{K_4 K_5 + K_5 \tau_{DE2} S - K_3 K_6}{K_5} I_{DE2} = 0 \qquad (18)$$

Solving (18) for I_{DE2} and substituting in (17)

$$I_B + \left(\frac{K_1 + \tau_{DE1} S}{K_5}\right) I_A + \left(\frac{K_5 K_2 - K_1 K_6 - K_6 \tau_1 S}{K_5}\right)\left(\frac{-(K_5+K_3)}{K_4 K_5 - K_3 K_6 + K_5 \tau_{DE2} S}\right) I_A = 0$$

$$I_A = -I_B \left[\frac{K_5 K_5 \tau_{DE2}\left(S + \frac{K_4}{\tau_{DE2}} - \frac{K_3 K_6}{K_5 \tau_{DE2}}\right)}{\tau_{DE1}\left(S + \frac{K_1}{\tau_{DE1}}\right) K_2 \tau_{DE2}\left(S + \frac{K_4}{\tau_{DE2}} - \frac{K_3 K_6}{K_5 \tau_{DE2}}\right) - (K_5 + K_3)\,\tau_{DE1} K_6 \left(S + \frac{K_5 K_2}{K_6 \tau_{DE1}} - \frac{K_1}{\tau_{DE1}}\right)} \right] \tag{19a}$$

As the possibilities of simplifying the algebra for the relatively general case of (19a) seem small, some further simplifying assumptions will now be made.

Assume $\alpha_{N1} = \alpha_{N2} = \alpha_N$ (20)

and $\alpha_{I1} = \alpha_{I2} = 0$ (21)

and $\tau_{DE1} = \tau_{DE2} = \tau_{DE}$ (22)

These assumptions result in a considerable simplification, as follows:

$$I_A = \frac{\alpha_N I_B}{\tau_{DE}} \quad \frac{S + 1/\tau_{DE}}{S^2 + \frac{2}{\tau_{DE}} S + \frac{1 - 2\alpha_N}{\tau_{DE}^2}} \tag{19b}$$

This may factored into

$$I_A = \frac{\alpha_N I_B}{\tau_{DE}} \quad \frac{S + 1/\tau_{DE}}{(S + S_1)(S + S_2)} \tag{19c}$$

$$S_1 = \frac{1}{\tau_{DE}}\left(1 + \sqrt{2\alpha_N}\right) \tag{23}$$

$$S_2 = \frac{1}{\tau_{DE}}\left(1 - \sqrt{2\alpha_N}\right) \tag{24}$$

For a step, i_{B1}, of base current,

$$I_B = i_{B1}/S \tag{25}$$

$$I_A = \frac{\alpha_N i_{B1}}{\tau_{DE}} \quad \frac{S + 1/\tau_{DE}}{S(S + S_1)(S + S_2)} \tag{19d}$$

Taking the inverse transform,

$$i_A = \frac{\alpha_N i_B}{1-2\alpha_N}\left[1 - \frac{1 - \sqrt{2\alpha_N}}{2}\, e^{-S_1 t} - \frac{1 + \sqrt{2\alpha_N}}{2}\, e^{-S_2 t}\right]$$

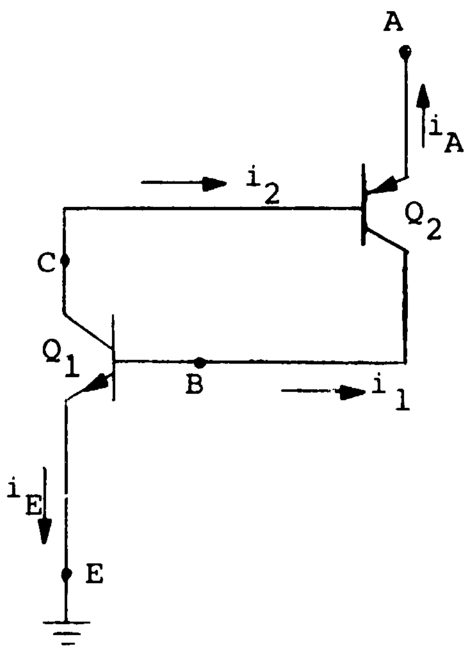
It is worthy of note that the i_A response is quite different in character for $\alpha_N < 0.5$ than for $\alpha_N > 0.5$. For the first case, the 2 expontional terms decay with time and i_A approaches a constant value. For the second case, one of the exponentials grows with time and i_A is limited only by factors external to the equations, such as the device entering the saturation region.

The equations solved were, for simplicity, of a model without a shunt base-emitter resistance. Thus a model with this resistance will not perform exactly like the equations do. This discrepancy should be small at high currents. The choice of constant equal α_N's and τ_{DE}'s is unlikely to be highly valid for an SCR device, resulting in discrepancies between device and model performance. Should these prove important, it may be necessary to develop solutions of the equations without using these simplifying assumptions.

b. Turn-off Step Response:

The device is assumed to be in saturation with anode current i_{A1} and zero base current when a (reverse) anode current step, i_{A2}, is applied. The relationship between storage time and device parameters under these conditions will be developed first. Then the relationship between maximum permissible rate of reapplication of anode voltage and device parameters will be examined.

1) Storage Time - Although the equations could be developed from the model as in the prevous section, a different and simpler approacn will be used. Assuming a symmetrical device, where all "subscript 1" parameters are identical to their "subscript 2" counterparts, a "2 transistor" model, as follows, will be used.



As the external base current is zero,

$$i_A = -i_E \tag{1}$$

During the storage time, due to the symmetry,

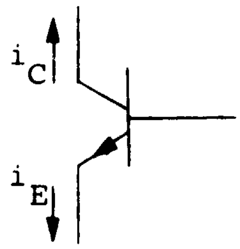
$$i_1 = i_2 \tag{2}$$

thus the transistors are identical with identical currents (except for polarity) and we may examine the storage time of only one of them.

Ebers-Moll provide the following approximate equation for a transistor with initial emitter and collector currents, i_{E1} and i_{C1}, and an applied emitter step of i_{E2}.

$$t_S = \tau_S \ln \frac{i_{E2} - i_{E1}}{i_{E2} + i_{C1}/\alpha_N} \tag{3}$$

where polarities are as follows,



Also from Ebers-Moll, the approximation

$$\tau_S = \tau_N + \tau_I \tag{4}$$

These equations permit the evaluation of τ_I (and C_{DC}) from anode turn-off storage time data by substituting in (3)

$$t_S = \tau_S \ln \frac{-i_{A2} + i_{A1}}{-i_{A2} + .5\ i_{A1}/\alpha_N} \tag{3a}$$

2) Maximum Rate of Reapplication of Anode Voltage

At t_S, the storage time ends, effectively all the charge stored in the model center diode diffusion capacitance is removed and the center diode is no longer forward biased. At this point there still remains charge in the diffusion capacitances of the two end diodes and thus there would still be a normally decreasing anode-emitter current if anode voltage were reapplied. When the anode voltage is reapplied it generates a base current through the center diode junction capacitance

$$\left(C \frac{dv}{dt}\right).$$

The combination of the existing end diode charges and the "applied" base current can cause the model to re-enter saturation rather than turn-off completely.

If it is assumed that this re-saturation results primarily because of the rate of reapplication of anode voltage (i_B) and negligibly because of the storage active region charge, a simple conclusion may be drawn as follows.

$$i_{BF} = C_{JC} \frac{\quad}{dt} \qquad (5)$$

where i_{BF} is the base current to trigger the model.

C. Parameter Evaluation

Evaluation of the parametersof the SCR model poses some unique problems. These result from the contrast between the relative complexity of the model and the relative simplicity of the applications to which the device is put. The device has 3 junctions, compared with 2 for the transistor and 1 for the diode. Further, device operation is strongly dependent on non-linear current-dependent alpha-normal plus one or more linear resistors shunting the junctions. The alphas are also voltage dependent providing an anode voltage sensitivity that results in an anode breakover voltage. This latter effect can be modeled with an avalance current generator shunting the center junction while retaining the linear alphas.

The combination of non-linear effective alphas and 3 junctions results in quite complex device dynamic behavior as well, even if the simple single lump diffusion capacitance concept is used with the normal junction capacitance model.

In contrast to this device and model complexity is the fact that the device is most often used as a triggered power switch in circuits where the exact detailed static and dynamic performance are not important. Thus device data sheets generally provide more data about device thermal properties than about electrical properties.

To accommodate to this situation, it is suggested that

1. Unimportant parts of the model should be omitted.

2. Parameters not vital to the gross performance be evaluated arbitrarilly with a "reasonable" value.

3. Symmetrical parts of the model be given identical values where doing so will aid or simplify parameter evaluation.

These guidelines are used below.

1. V_o

V_o directly, controls direct the small-signal low-current forward resistance of the junctions and indirectly affects the junction reverse leakage currents.

Arbitrarily, let V_o = .026 volts @ 25°C.

2. α_{N1} and α_{N2}

An approximate value for the normal alphas may be obtained by first assuming $\alpha_{N1} = \alpha_{N2}$, then use (27d) to approximately define the Anode Holding Current,

$$-I_H \cong \frac{\alpha_{N1} i_{RBE}}{\alpha_{N1} + \alpha_{N2} - 1}$$

Then use (27e) to approximately define the Gate Current to Fire,

$$-I_{GF} \cong i_{RBE}$$

From these, defining $R = I_H/I_{GF}$,

$$\alpha_{N1} = \alpha_{N2} = \frac{R}{2R-1}$$

Note, however, that alpha must be greater than .5 and less than 1.

3. α_{I1} and α_{I2}

The inverse alphas primarily affect the low-current anode saturation voltage. They are generally quite small, and the low-current saturation voltage is usually not important.

Arbitrarily, let $\alpha_{I1} = \alpha_{I2} = .01$

4. R_{BE} and R_{AC}

From the Gate Current to Fire and (27e)

$$i_{RBE} \cong -I_{GF}$$

Arbitrarily assume a base voltage of 0.50 volts for which almost all the input current goes through R_{BE} and almost none through the base-emitter junction.

Then $\quad R_{BE} \cong \dfrac{.5}{-I_{GF}}$

Arbitrarily, let $R_{AC} = 1000\ R_{BE}$

5. I_{SE1}, I_{SC}, and I_{SE2}

From (16), assuming 1% of I_{GF} enters the base at $v_{BE} = .5$ volts,

$$.5 \cong .026 \ln \left(1 - \frac{.01\ I_{GF}}{I_{SE1}}\right)$$

$$\exp(.5/.026) = \left(1 - \frac{.01\ I_{GF}}{I_{SE1}}\right)$$

$$I_{SE1} = .01\ I_{GF}/(1-\exp(.5/.026))$$

from (8)

$$I_{SC} = \alpha_{N1}\ I_{GF}/(1-\exp(.5/.026))$$

from (9)

$$I_{SE2} = .01\ I_{GF}/(1-\exp(.5/.026))$$

6. R_E, R_A, and R_B

Where the SCR is not used at high currents or high dissipation or where the increase in saturation anode voltage with current is not important, R_E may be omitted from the model. Otherwise, a low current and a high current point may be used to evaluate R_E.

$$R_E = \frac{V_{AH} - V_{AL}}{I_{AL} - I_{AH}}$$

Arbitrarily, let $R_A = R_B = 0$.

7. i_Z

Where necessary a Zener current generator can be used to simulate the voltage dependence of alpha that results in an anode breakover voltage. In most application, this generator may be omitted.

8. C_{JC}, C_{JE1}, C_{JE2}

For each of the three diodes in the model, the junction capacitance should exhibit the usual voltage dependence as follows:

$$C_J = -\frac{K}{(V_K - v)^N}$$

However, it is quite consistant with the lack of precision used this far in parameter evaluation to adopt a linear junction capacitance. Thus

$$C_J = K$$

C_{JC} or K_C may be evaluated by using the specified maximum rate of reapplication of anode voltage with the Gate Current to Fire spec.

$$C_{JC} = -I_{GF}/(dv_A/dt)$$

As neither C_{JE1} nor C_{JE2} are of great importance to normal device operation, it is suggested that they be set equal to C_{JC}.

Thus $C_{JE1} = C_{JE2} = C_{JC}$.

9. C_{DE1}, C_{DE2}, and C_{DC}

As with the diode and transistor models, the diffusion capacitances are represented by the diffusion time constants. For simplicity,

let $\tau_{DE1} = \tau_{DE2} = \tau_{DE}$

The SCR turn-on time can be used to evalute τ_{DE}.

From the dynamic analytic solutions,

$$i_{A1} = \frac{\alpha_N i_{B1}}{1-2\alpha_N}\left(1 - \frac{1-\sqrt{2\alpha_N}}{2} e^{-S_1 t_t} - \frac{1+\sqrt{2\alpha_N}}{2} e^{-S_2 t_t}\right)$$

where

$$S_1 = \frac{1}{\tau_{DE}} (1 + \sqrt{2\alpha_N})$$

and

$$S_2 = \frac{1}{\tau_{DE}} (1 - \sqrt{2\alpha_N})$$

This equation cannot be solved explicitly for τ_{DE} when given α_N, i_{A1}, i_{B1}, and t_t. However, i_A vs. t may be plotted for a normalized τ_{DE}, permitting a graphical solution for τ_{DE}.

The total turn-on time t_t is composed of a delay, t_D, and a rise, t_r.

It is noted here that, in general, the model will not have the same ratio of t_D/t_r as does the device. This is so because the current dependence of the device alpha is only roughly modeled with a shunt linear resistor.

The inverted time constant, τ_I, associated with the base-collector diode of the model may be evaluated from storage time data

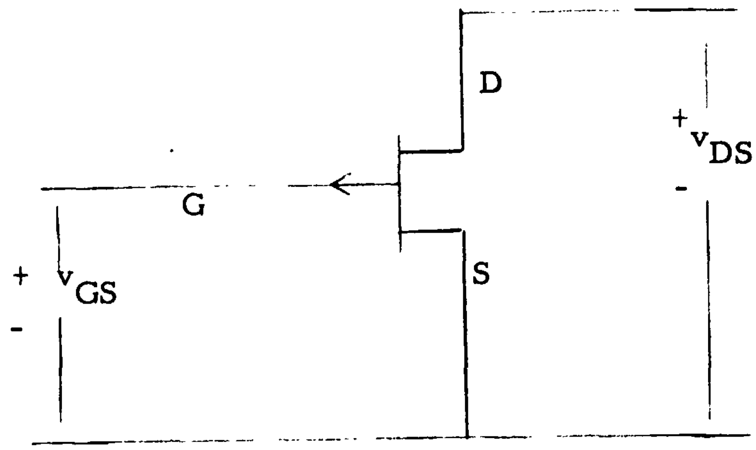
$$t_S \cong \tau_S \ln \frac{I_{A2} - I_{A1}}{\frac{.5 I_{A1}}{\alpha_N} - I_{A2}}$$

$$\tau_{DC} \cong \tau_S - \tau_{DE}$$

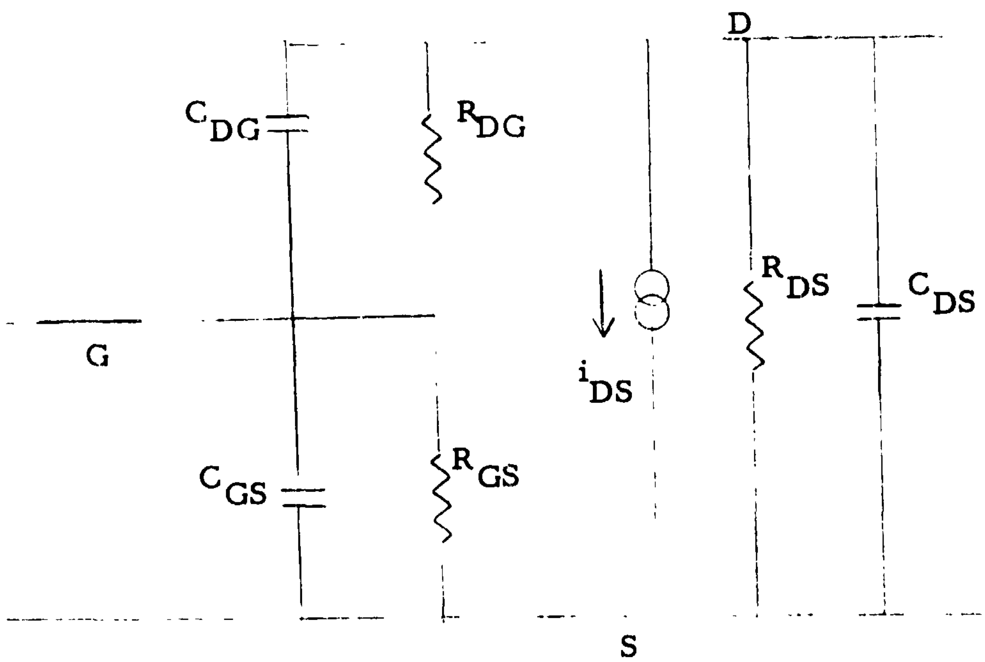
VII. P-Channel Junction Field Effect Transistor Model

A. Model Description

For P-channel junction FET, device and polarities are symbolized as follows.



A preliminary model for this device has been developed. This model is symbolized as follows.



1. Equation for i_{DS}

The general equation assigned to i_{DS} is as follows:

$$i_{DS} = I_{DSS}\left(1-\frac{v_{GSX}}{V_p}\right)^{K_1}\left(1-\exp\left(\frac{K_2\ v_{DS}}{V_p - v_{GSX}}\right)\right)$$

where v_{GSX} is defined for each region in the following paragraphs and the remaining parameter are defined subsequently.

a. Normal Active Region v_{GSX}

In the Normal Active Region, v_{GS} is positive and v_{DS} is negative.

Fr $V_p > v_{GS} \geq 0$ and $v_{DS} \leq 0$, $v_{GSX} = v_{GS}$

b. Inverted Active Region v_{GSX}

In the Inverted Active Region, $v_{GS} - v_{DS}$ is positive and v_{DS} is positive.

For $V_p + v_{DS} > v_{GS} \geq v_{DS}$ and $v_{DS} \geq 0$, $v_{GSX} = v_{GS} - v_{DS}$

c. Conducting Gate Region v_{GSX}

Operation with the Gate conducting is not well defined for the FET. This is handled mathematically by preventing the model from entering this region.

For $v_{GS} < 0$ and $v_{DS} \leq 0$,

$v_{GSX} = 0$.

For $v_{GS} < v_{DS}$ and $v_{DS} \geq 0$

$v_{GSX} = -v_{DS}$

d. Cut-Off Region

For $v_{GS} \geq V_p$ and $v_{DS} \leq 0$, $v_{GSX} = V_p$

For $v_{GS} \geq V_p + v_{DS}$ and $v_{DS} \geq 0$, $v_{GSX} = V_p$

e. Other Parameters

1. Drain saturation current, $I_{DSS} = i_{DS}$ at $v_{GS} = 0$ and $v_{DS} \leq -2V_p$

2. Gate pinch-off voltage,

$V_p = v_{GS}$ for $i_{DS} = -1 \times 10^{-6}$ and $v_{DS} < -V_p$

3. K_1 is a constant that influences the transconductance. It is usually given the value 2 for silicon diffused-junction devices.

4. K_2 is a constant that influences the output conductance at v_{DS} near zero. It is given the value of 2 in the absence of contrary information.

2. Other Components of Model

a. Fixed Resistors

All the fixed resistors will have large values as they are intended to simulate the device leakage currents. Even when not important for circuit performance, at least 2 of the 3 should be used to provide D.C. "connectivity" for TAG.

b. Capacitors

The drain-gate capacitor, C_{DG}, is of primary importance for most dynamic applications. The other 2 capacitors may often be omitted.

B. Model Performance

1. Large Signal Static Normal Active Region

Ignoring the "leakage" resistors, the drain source current generator characterizes the output characteristics of the device. These output characteristics are plotted in Exhibit 1 for several values of gate-source voltage.

It is to be noted that the model is not "permitted" to perform in the region where the gate is forward biased. Also, the "breakdown" characteristics of the device at high voltages are not present in the model.

2. Static Operation as a Voltage-Variable-Resistor

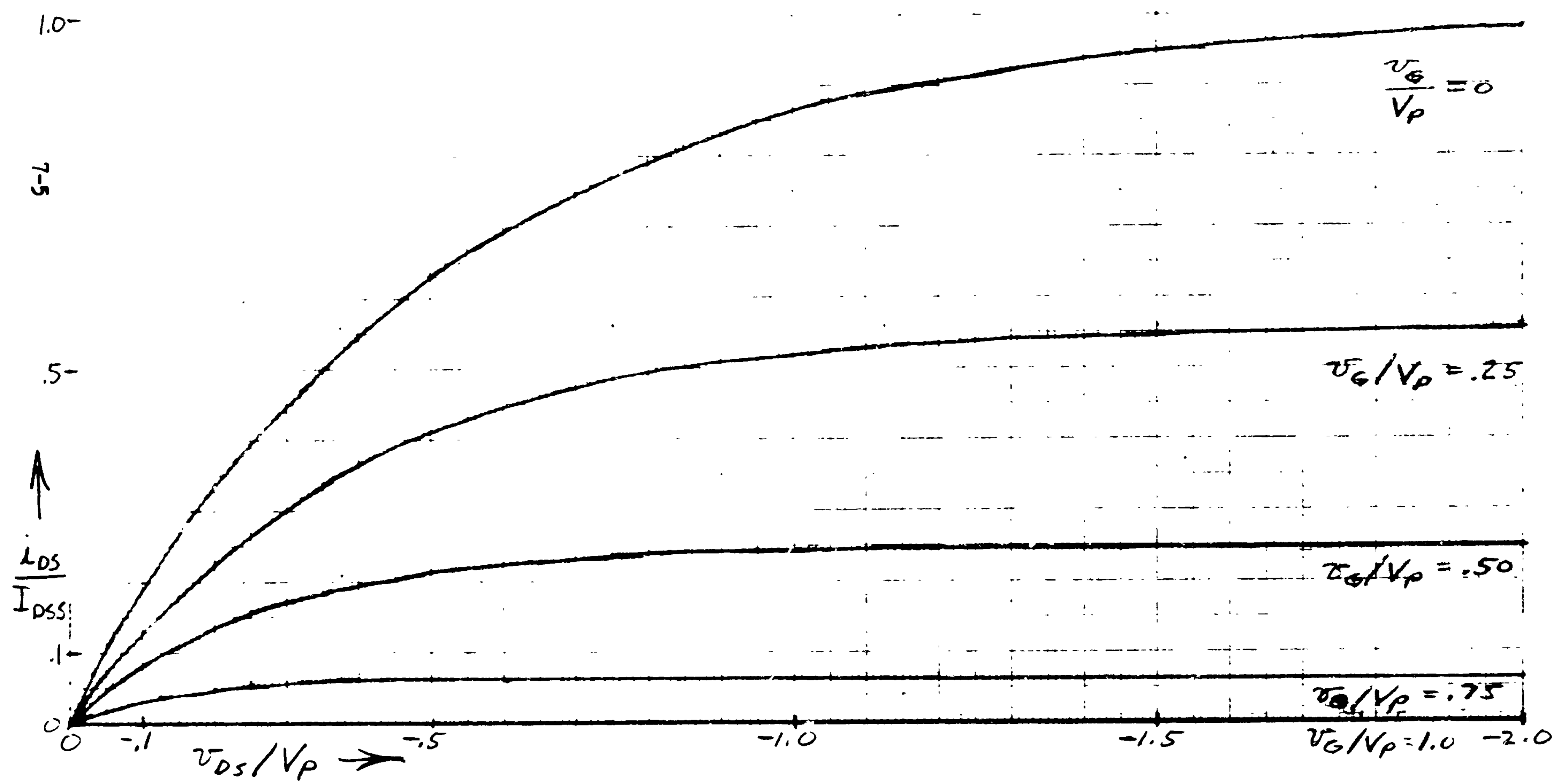
For this type of operation, v_{DS} is generally within the range of $\pm 0.1\ V_p$. The performance of the i_{DS} current generator (ignoring the leakage resistors) in this area is shown in Exhibit 2. Note that the output characteristics are only approximately linear. Also note that a gate voltage somewhat greater than Vp is required to cut off the current for positive v_{DS}.

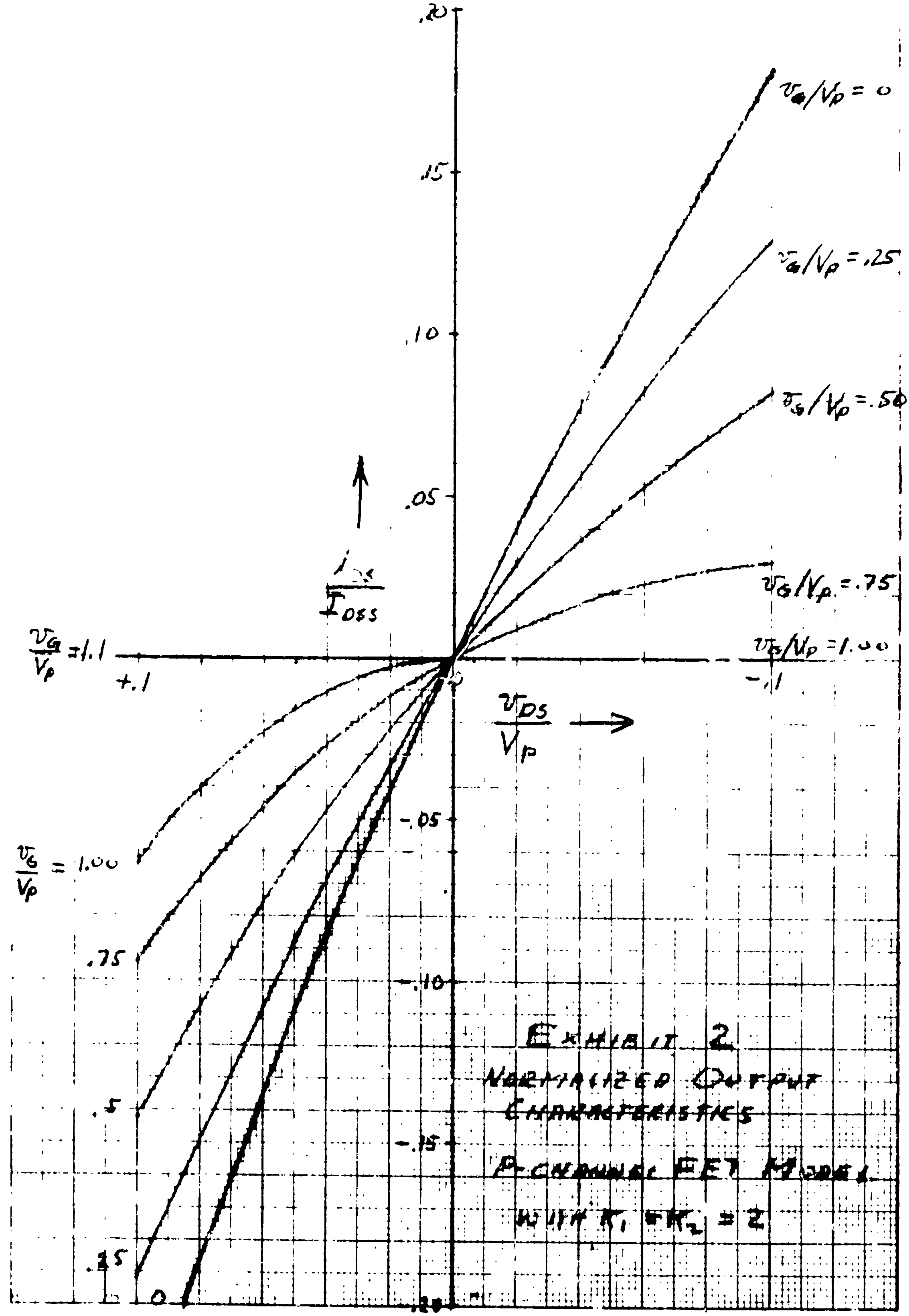
EXHIBIT 1

NORMALIZED OUTPUT CHARACTERISTICS

P-CHANNEL FET MODEL

WITH $K_1 = K_2 = 2$




.20
.15
.10
.05
-.05
-.10
-.15
$v_G/V_p = 0$
$v_G/V_p = .25$
$v_G/V_p = .50$
$v_G/V_p = .75$
$v_G/V_p = 1.00$
$\frac{i_{DS}}{I_{DSS}}$
$\frac{v_G}{V_p} = 1.1$
+.1
-.1
$\frac{v_{DS}}{V_p}$
$\frac{v_G}{V_p} = 1.00$
.75
.5
.25
0
EXHIBIT 2
NORMALIZED OUTPUT CHARACTERISTICS
P-CHANNEL FET MODEL
WITH $K_1 = K_2 = 2$

C. Parameter Evaluation

Although it is possible to get the constants K_1 and K_2 from device data, for simplicity here we assume values of 2 for both of them.

1. Normal Active Pinch-off or Saturation Region Parameters

Very often, specification or test data provides values for both I_{DSS} and V_p. Sometimes, only one of these two parameters is provided, plus a parameter called g_{fs}, the forward incremental transconductance in the pinch-off region. The relationship of g_{fs} to I_{DSS} and V_p is as follows.

In the Normal Active Region, the expression for i_{DS} becomes:

$$i_{DS} = I_{DSS}\left(1 - \frac{v_{GS}}{V_p}\right)^2\left(1 - \exp\left(\frac{2v_{DS}}{V_p - V_{GS}}\right)\right)$$

For $-v_{DS} > 2V_p$ the exponential term approaches unity and i_{DS} may be approximated as follows.

$$i_{DS} \cong I_{DSS}\left(1 - \frac{v_{GS}}{V_p}\right)^2$$

Differentiating with respect to v_{GS},

$$\frac{di_{DS}}{dv_{GS}} \cong \frac{-2I_{DSS}}{V_p}\left(1 - \frac{v_{GS}}{V_p}\right)$$

Defining $g_{fs} \cong \left.\frac{di_{DS}}{dv_{GS}}\right|_{-v_{DS} > 2V_p}$,

$$g_{fs} \cong \frac{-2I_{DSS}}{V_p}\left(1 - \frac{v_{GS}}{V_p}\right) .$$

This equation may be used to relate g_{fs} , I_{DSS} and V_p at any point in the Normal Active pinchoff region.

At times the forward transconductance at zero gate voltage, g_{fso}, is given. It is apparent that

$$g_{fso} \cong \frac{-2I_{DSS}}{V_p}$$

2. Pre-pinchoff Region (Voltage variable resistor) Parameter

The parameter of primary interest here is r_{dso} the incremental output resistance at $V_{GS} = V_{DS} = 0$. The relationship of r_{dso} to the other parameters is derived as follows. Starting with the general equation for i_{DS}, for v_{GSX} constant, differentiate with respect to v_{DS}:

$$\frac{di_{DS}}{dv_{DS}} = I_{DSS} \left(1-\frac{v_{GSX}}{V_p}\right)^{K_1} \left(\frac{-K_2}{V_p - v_{GSX}}\right) \exp\left(\frac{K_2 v_{DS}}{V_p - v_{GSX}}\right)$$

$$@\ v_{DS} = 0, \ \frac{di_{DS}}{dv_{DS}} = I_{DSS} \left(\frac{V_p - v_{GSX}}{V_p}\right)^{K_1} \left(\frac{-K_2}{V_p - v_{GSX}}\right)$$

$$\frac{di_{DS}}{dv_{DS}} = \frac{-K_2 I_{DSS}}{V_p} \left(\frac{V_p - v_{GSX}}{V_p}\right)^{K_1 - 1}$$

$$\text{For } K_1 = 2, \ \frac{di_{DS}}{dv_{DS}} = \frac{-K_2 I_{DSS}}{V_p} \left(\frac{V_p - v_{GSX}}{V_p}\right)$$

$$\text{For } v_{GSX} = 0, \ \frac{di_{DS}}{dv_{DS}} = \frac{-K_2 I_{DSS}}{V_p}$$

$$\text{let } r_{dso} = 1/\left(\frac{di_{DS}}{dv_{DS}}\right)\Bigg|_{v_{GS}=0}$$

$$\text{Then } r_{dso} = \frac{-V_p}{K_2 I_{DSS}}$$

It is evident that K_2 can be determined from this equation if the other three quantities are given. On the other hand, using the suggested approximate value of $K_2=2$,

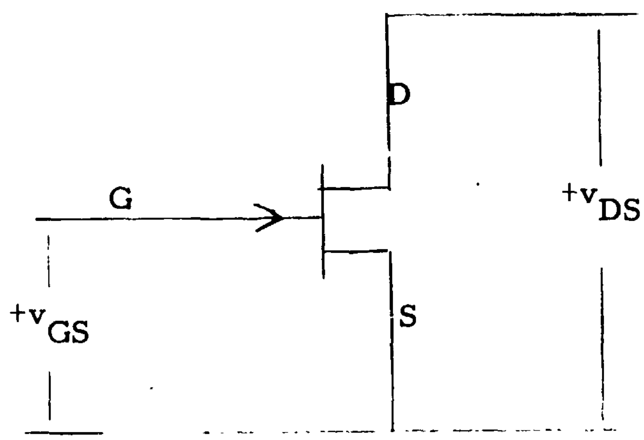
$$r_{dso} = \frac{-V_p}{2I_{DSS}}$$

$$\text{And incidentally} \qquad r_{dso} = \frac{1}{g_{fso}}$$

VIII. N-channel Junction Field Effect Transistor Model.

A. Model Description

For a N-channel junction FET, device and polarities are symbolized as follows:



The model for this device is identical to that for the P-channel junction FET, except for the opposite polarities of v_{GS}, v_{DS}, and i_{DS}.

IX. NON-LINEAR INDUCTOR MODEL

A. Model Description

Most practical low frequency inductive devices employ as a flux storage media one of the many metallic alloy or ferritic materials characterized by a high flux storage capacity per unit magnetizing force. Typical of the alloys are 4-79 Molybdenum Permalloy, Supermalloy, and 50:50 nickel-iron alloy. These materials generally display a B-H curve similar to that shown in figure 1 below.

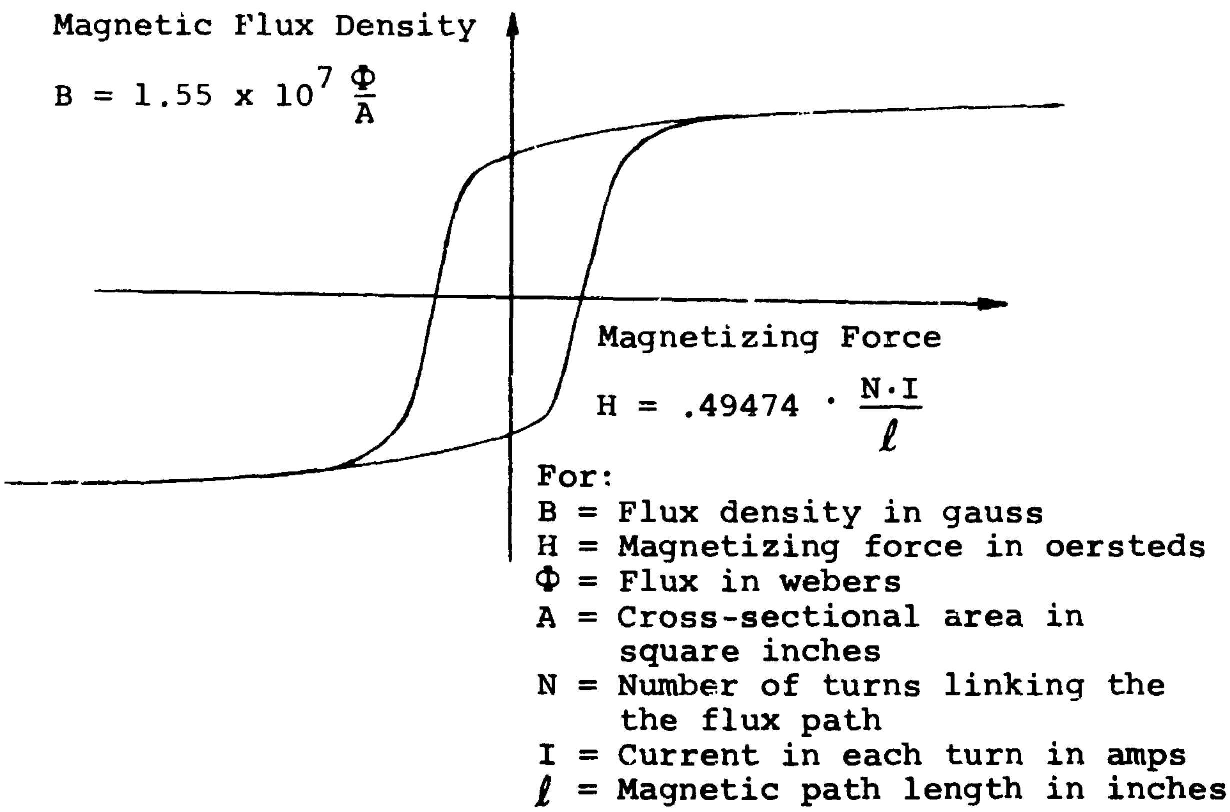


Figure 1 Typical B-H curve for high flux density magnetic materials.

This report develops and demonstrates a mathematical model for such magnetic core materials which is composed of three linear segments chosen in such a manner as to form a best fit approximation to such B-H curves. Figure 2 shows the results of fitting such a model to the B-H curve of Figure 1.

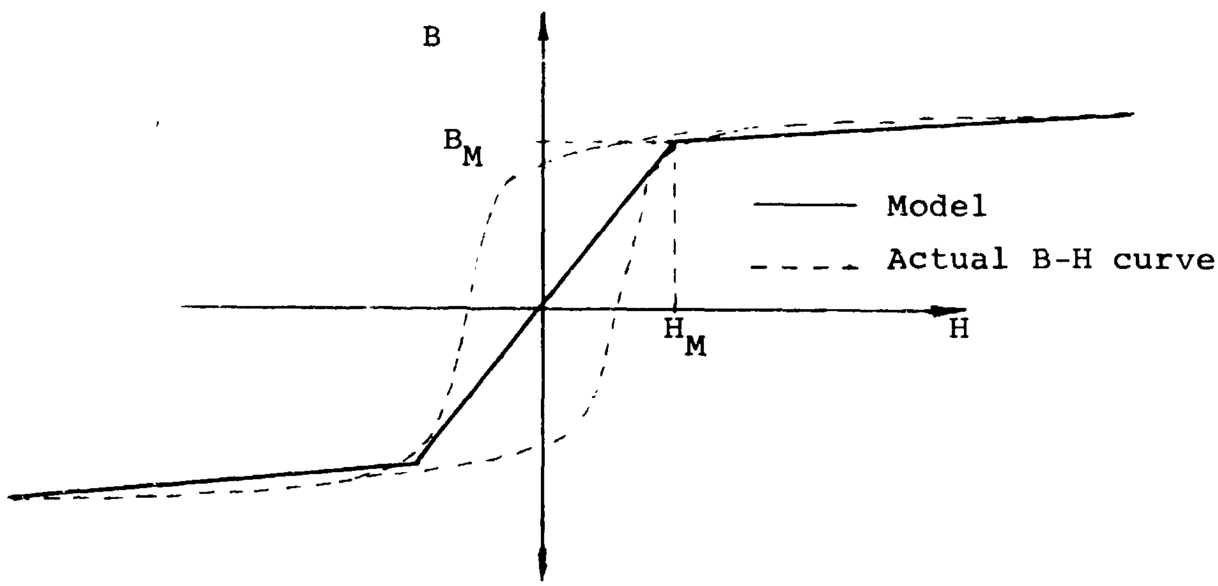


Figure 2 Three piece linear approximation to B-H curve

Once an inductive device has been built, its terminal properties become the most important characteristics defining its behavior. For this reason the model equations developed here will be in terms of device terminal parameters. These parameters will be related to magnetic core material properties by a set of equations presented at the end of this section. As illustrated in figure 3, the terminal properties of an inductive device are the time integral of the terminal voltage Φ_T and the magnetization current, I_{MAG}, flowing through the device.

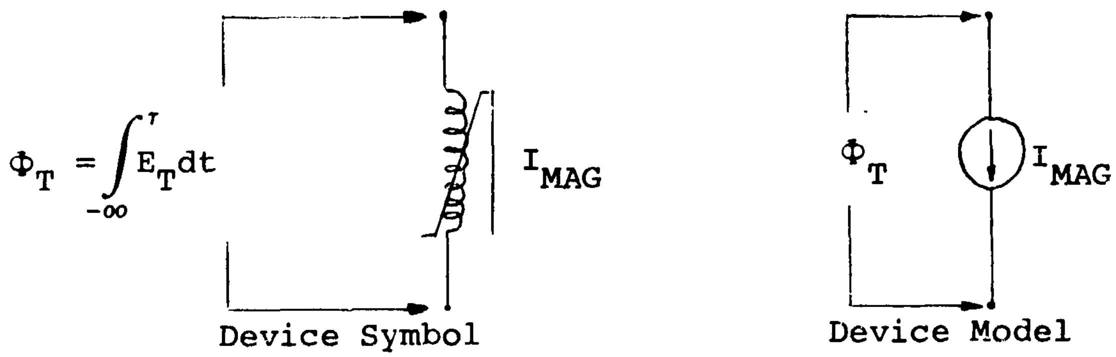


Figure 3 Symbolic representation of device and model terminal variables.

Figure 4 shows an idealized Φ - I_{MAG} curve fitted by the proposed three piece linear segmented model. The salient features of this curve are defined in terms of device terminal variables Φ_T and I_{MAG}. The model clearly displays three states labled the negative saturation, high inductance, and positive saturation regions. Each state corresponds to one of the three segments of the model. If we define a constant S which takes on the value -1 in the negative saturation region, 0 in the high inductance region, and +1 in the positive saturation region, the model may be expressed by the single equation given below. This equation expresses the magnetization current as a function of the time integral of terminal voltage for all three regions of the model.

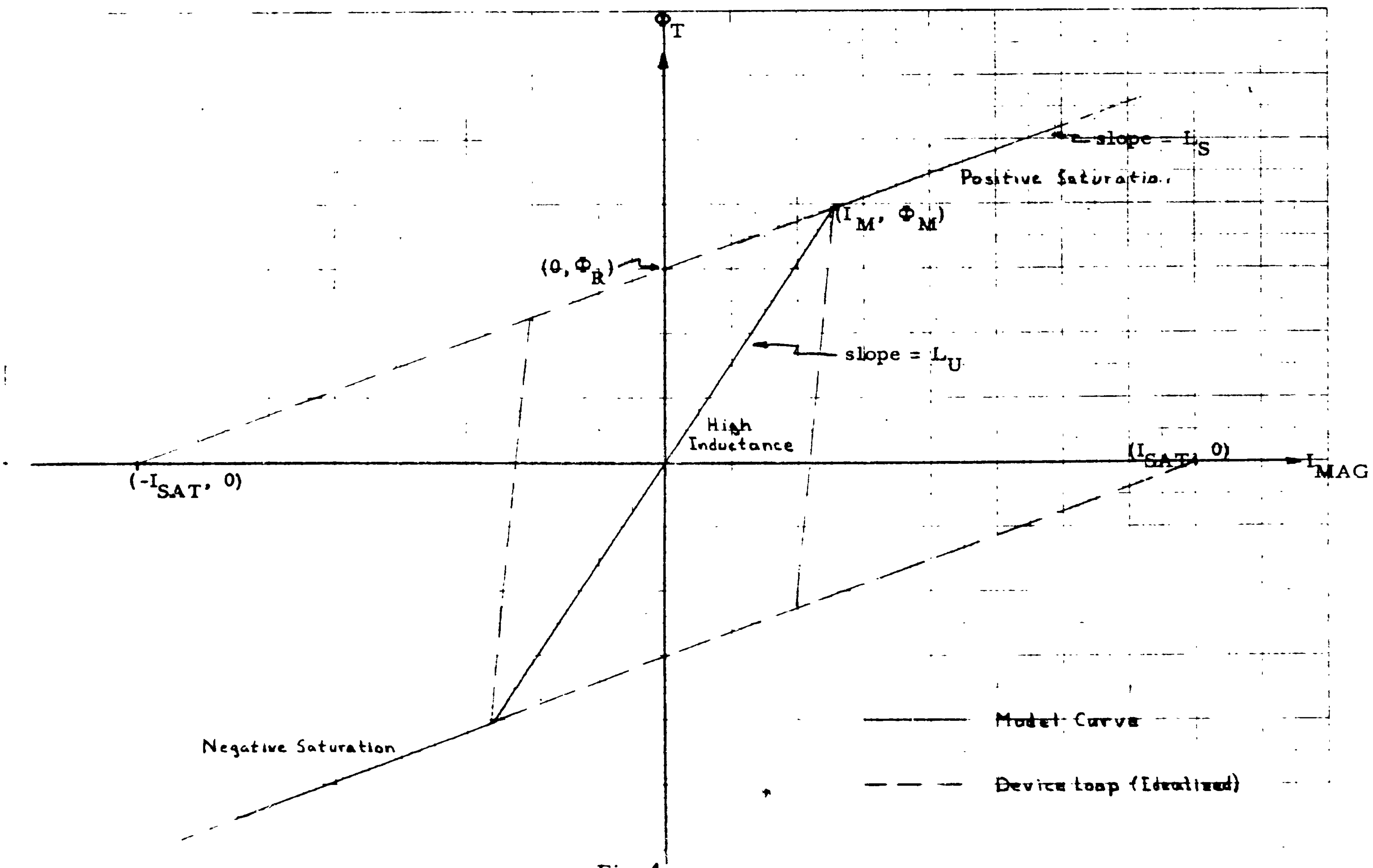


Fig. 4
Linear Approximation to Φ-I Loop

$$I_{MAG} = \frac{\Phi_T}{L} - S \cdot I_{SAT}$$

where: $\Phi_T = \int_{-\infty}^{T} E_T \, dt$

S = state constant

= -1 in the negative saturation region

= 0 in the high inductance region

= +1 in the positive saturation region

L = Terminal inductance

= L_U in the high inductance region

= L_S in both saturation regions

I_{SAT} = The extrapolated value of the saturation region magnetizing current for zero impressed flux.

By making appropriate changes in the values of L and S each time the boundary between two segments is traversed the desired non-linear function is created.

Given the following set of basic inductor parameters the required terminal parameters I_{SAT}, L_U, L_S and Φ_M may be calculated using the formulas given below.

Given: N = Number of turns linking inductor core

l = Length of magnetic path in inches

A = Cross-sectional area of magnetic path in square inches

B_M = Magnetic flux-density at the boundary between the high inductance and saturation regions in gausses.

U_U = Average permeability in high inductance region in gauss/oersted

U_S = Average permeability in saturation region in gauss/oersted

For Φ_T in volt-secs and I_{MAG} in amps

$$\Phi_M = 6.4516X10^{-8} \cdot N \cdot A \cdot B_M \text{ in volt-secs}$$

$$L_U = N^2 \frac{U_U \cdot A}{3.133X10^{>}.1} \qquad \text{in henrys}$$

$$L_S = L_U \cdot \frac{U_S}{U_U} \qquad \text{in henrys}$$

$$I_{SAT} = \frac{\Phi M}{L_U} \cdot \left(\frac{U_U}{U_S} - 1 \right) \qquad \text{in amps}$$

B. <u>Model Performance</u>

The performance of the piecewise linear inductor model developed above is now analyzed as it responds within the circuit of figure 5. A voltage step of amplitude E is applied to the non-linear L through resistor R.

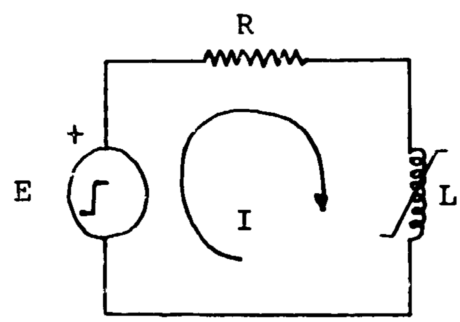


Figure 5 Non-linear inductor test circuit

The current in a series RL circuit to which a voltage step E has been applied is:

$$I = \frac{E}{R}\left(1 - e^{-\frac{R}{L}t}\right)$$

In the unsaturated region, $L = L_U$, and in the saturated region, $L = L_S$. A separate equation must therefore be required to define the time response of the circuit in each region.

$$I_U = I_{MAX}\left(1-e^{-\frac{R}{L_U}t}\right) \quad \text{for } 0<t<tx$$

$$I_S = I_{MAX}\left[1-(1-K)\,e^{-\frac{R}{L_S}(t-tx)}\right] \quad \text{for } t_x<t,$$

where t_x is the time at which $\Phi_T=\Phi_M$,

$$K = {}^{I_M}/_{I_{MAX}}, \quad I_{MAX} = \frac{E}{R}, \text{ and } I_M = \frac{\Phi_M}{L_U}$$

By using K as an independent variable, t_x may be calculated as a function of K. The effect is equivalent to changing the value of the unsaturated inductance while holding all other parameters constant.

$$I_M = I_{MAX}\left(1 - e^{-\frac{R}{L_U}t_x}\right)$$

$$K = 1 - e^{-\frac{R}{L_U}t_x}$$

$$e^{-\frac{R}{L_U}t_x} = 1 - K$$

$$t_x = -\frac{L_U}{R}\log_e(1-K)$$

But, $\Phi_M = L_U I_M = L_S (I_M + I_{SAT})$.

Solving for L_U, $L_U = \frac{L_S I_{SAT}}{K I_{MAX}} + L_S = \frac{\Phi_M}{K I_{MAX}}$

$$\text{So } t_x = -\frac{L_S}{R} \log_e (1-K) \left(\frac{I_{SAT}}{K I_{MAX}} + 1 \right)$$

or

$$= -\frac{\Phi_M}{R K I_{MAX}} \log_e (1-K)$$

t_x is plotted in fig. 6 as a function of K. The limiting value of t_x as $K \rightarrow 0$ is derived from:

$$e^{-\frac{R}{L_U} t_x} = 1-K$$

$$1 - \frac{R}{L_U} t_x \approx 1-K$$

$$\therefore t_x = \frac{L_U}{R} K = \frac{\Phi_M}{I_M R} \cdot \frac{I_M}{I_{MAX}} = \frac{\Phi_M}{R I_{MAX}}$$

This corresponds to a value of $L_U = \infty$

The equations for I_U and I_S as functions of time are developed, using values of K from 0 to 1, and L_S held constant at .1R. Some of these pairs of equations are also plotted in fig. 6, using the time constant $\frac{\Phi_M}{R I_{MAX}} = \frac{\Phi_M}{E}$

to normalize the time axis.

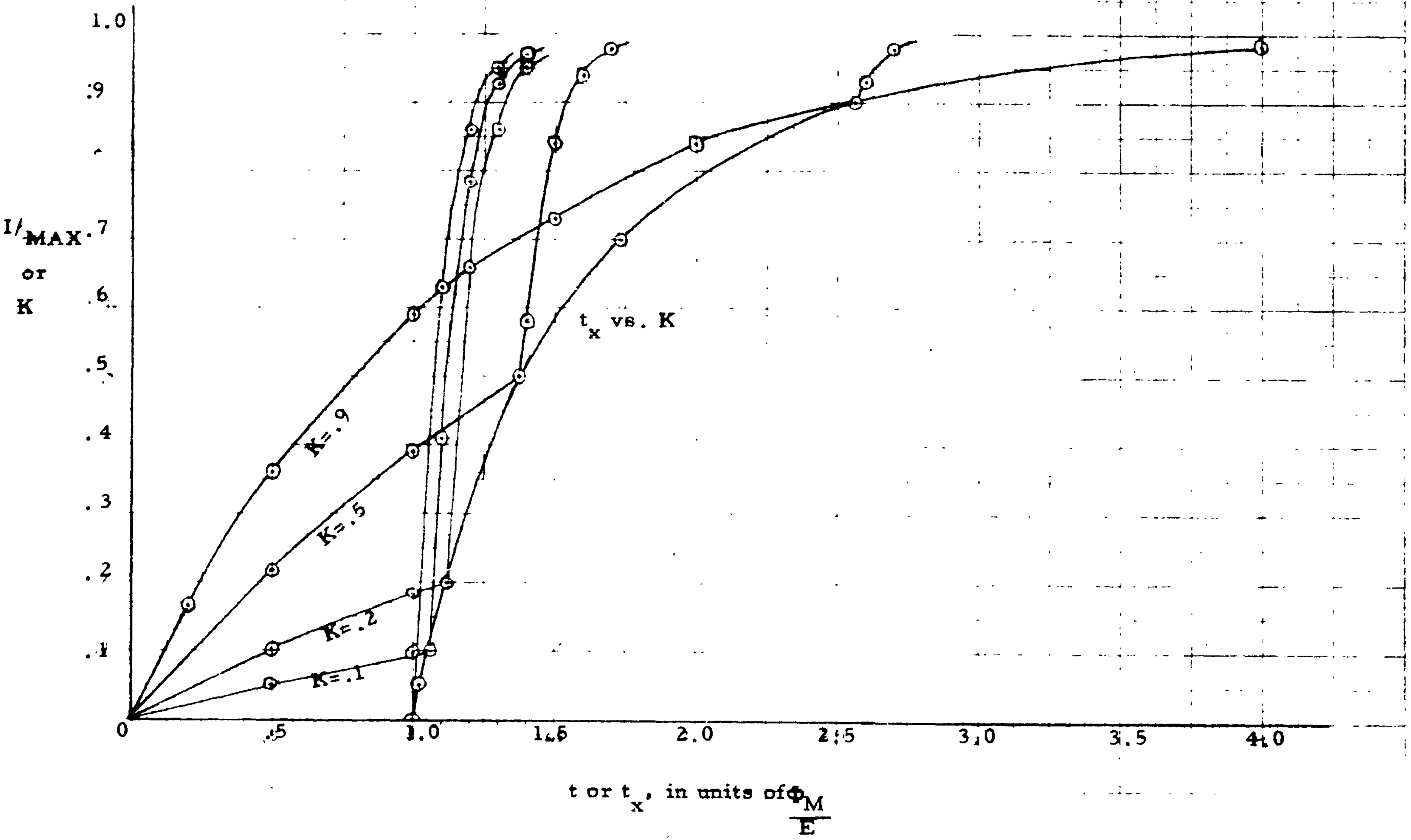


Fig. 6
Inductor Current vs. Time

C. Parameter Evaluation

The mathematical model of the non-linear inductor developed in section A provides an equation for calculating I_{MAG}, the current through the inductor, as a function of Φ_T, the time integral of the voltage applied across the inductor. This equation is reproduced below.

$$I_{MAG} = L^{-1} \cdot \Phi_T - S \cdot I_{SAT}$$

where, for $|\Phi_T| \leq \Phi_M$, $S = 0$. and $L = L_U$.

for $\Phi_T \geq \Phi_M$, $S = +1$ and $L = L_S$

and, for $\Phi_T \leq -\Phi_M$, $S = -1$ and $L = L_S$

Given the inductor core parameters, N, A 1, B_M, U_U and U_S, the required terminal parameters, Φ_M, L_U, L_S, and I_{SAT} may be calculated using the formulas provided at the end of section A. Parameters B_M, U_U, and U_S may be graphically evaluated from a B-H loop by fitting a suitable set of three straight line segments directly to the given curve. This is demonstrated in figure 7.

Evaluation of the terminal parameters of an inductive device which has already been built may be accomplished by by observing the current response of the device to the test voltage wave form shown in figure 8. The time response of the current may be displayed on an oscilloscope by using either a current probe or a small resistor in series with the inductor. Each voltage pulse should be of sufficient duration to drive the core over the entire region of probable operation. The time between the pulses should be sufficient to insure that the

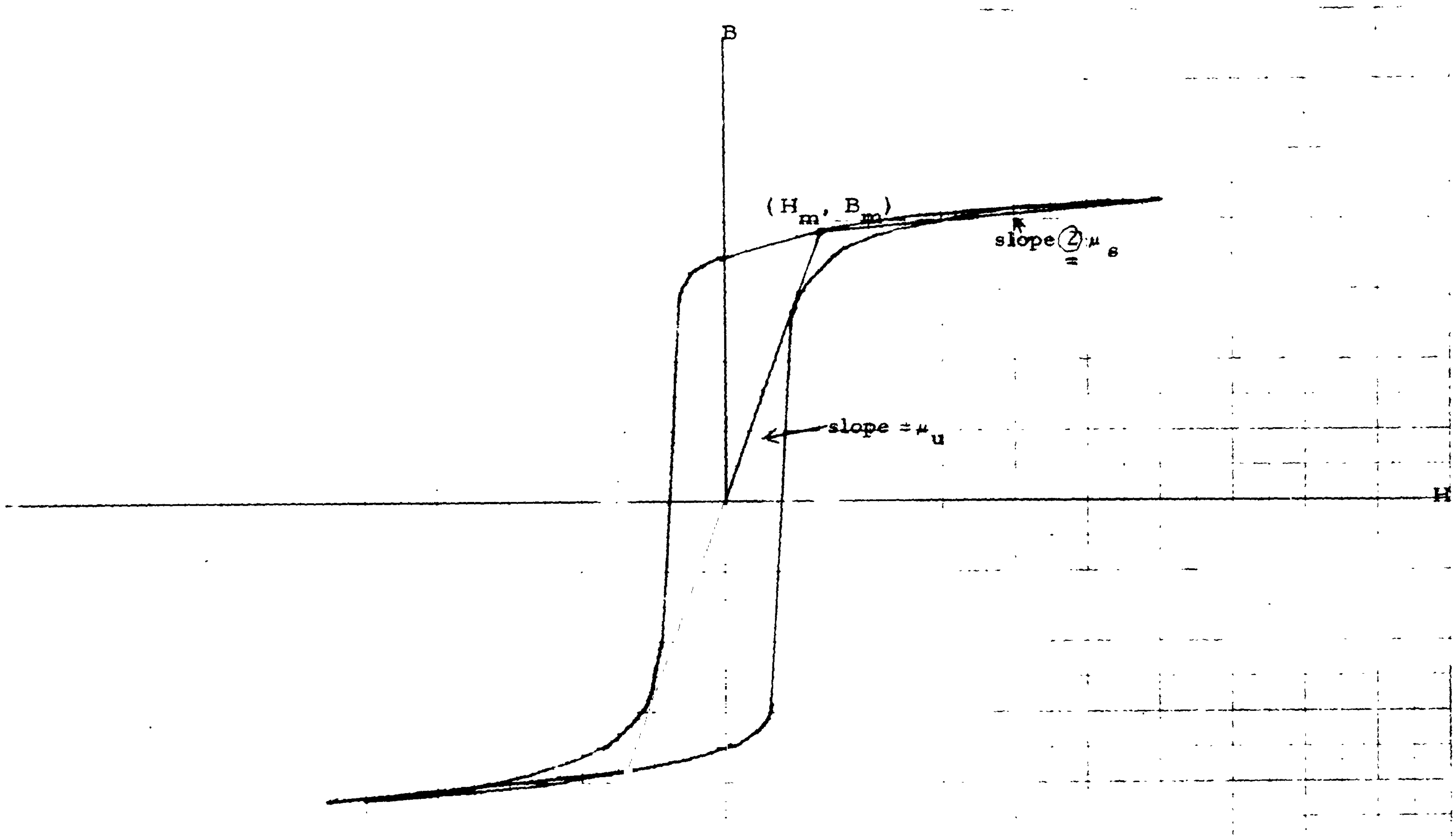


Fig. 7.
Graphical Fitting of Linear Model to B-H Loop

magnetization current decays to zero between pulses. The current waveform to be expected during each positive pulse is shown in figure 9.

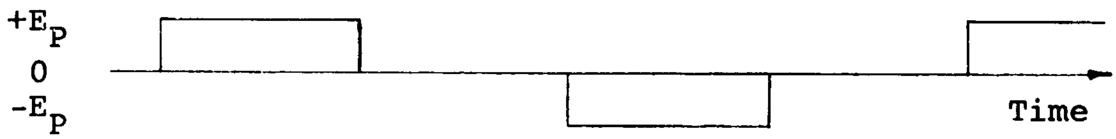


Figure 8 Test voltage wave form.

This will produce a half hysteresis loop from which Φ_M, L_U, and L_S may be graphically determined. These may be transformed into normalized core material constants by assuming N = 1, A = 1, and l = 1. Under these conditions:

$$U_U = 3.133 \times 10^{>} \times L_U$$

$$U_U/U_S = L_U / L_S$$

$$B_M = \frac{\Phi M \times 10^8}{6.4516}$$

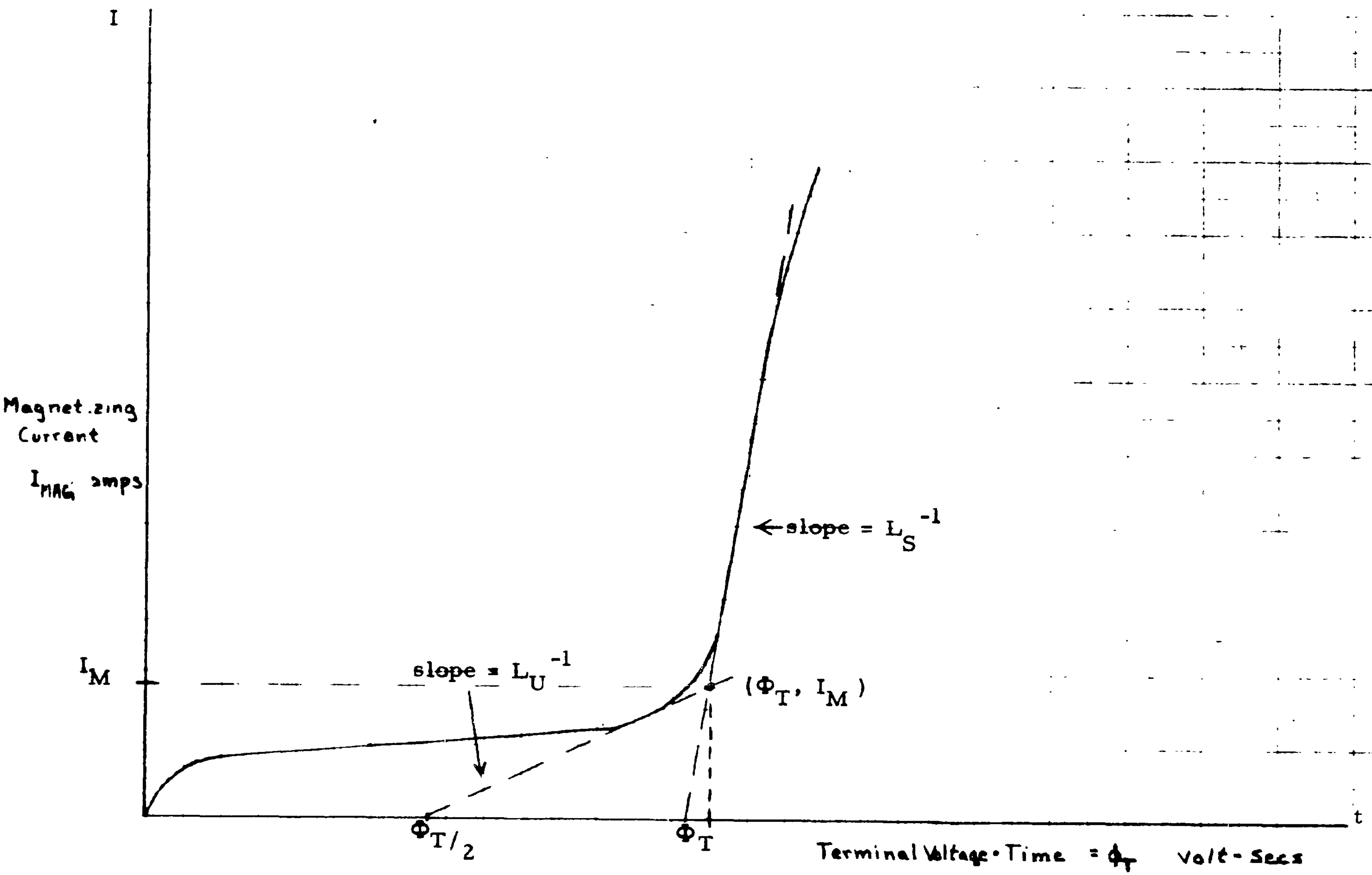


Fig. 9.
Derivation of L_U and L_S from Experimental Curve

D. Non-Linear Inductor Subroutines

```
      SUBROUTINE PLIND(FLUX,RIND,STATE,CISAT,FLXSTI,FLXSTJ,FLXIN,DATA,
     1LLCNT,LALGFT,I)
      CALL PLIND(SSXXYY,RIND1,STATE1,CISAT1,$1FLXST1,$JFLXSTJ,FLXINI,
C    1DATA1,LLCNT,LALGFT,I)
C     SIXXYY = RIND1 * (SSXXYY + FLXIN1) - STATE1 * CISAT1
C     SUBROUTINE PLIND IS A PIECEWISE LINEAR INDUCTOR CONTROL SUBROUTINE
C     FOR THE TAG CIRCUIT ANALYSIS PROGRAM.
C     PLIND CONTROLS THE LINEAR INDUCTOR MODEL IMPLEMENTED BY THE
C     CURRENT SOURCE DESCRIPTION STATEMENT SHOWN ABOVE BY VARYING THE
C     VALUES OF RIND1 AND STATE1 DEPENDING UPON THE FLUX LEVEL IMPRESSED
C     ACROSS THE DEVICE.
C     FOR FLUX LEVELS BETWEEN + AND - FLUXMX, STATE = 0. AND THE CORE
C     EXHIBITS A PERMEABILITY OF UMAX YIELDING A RECIPROCAL TERMINAL
C     INDUCTANCE RIND = RCPL0.
C     FLUXMX CORRESPONDS TO A LEVEL OF FLUX DENSITY WITHIN THE CORE OF
C     BMAX.
C     FOR FLUX LEVELS ABOVE + FLUXMX, STATE1 = +1. AND THE CORE EXHIBITS
C     A PERMEABILITY EQUAL TO USAT = UMAX/URATIO YIELDING A RECIPROCAL
C     TERMINAL INDUCTANCE RIND = RCPL1.
C     FOR FLUX LEVELS BELOW - FLUXMX. STATE1 = -1. AND THE CORE AGAIN
C     EXHIBITS A PERMEABILITY EQUAL TO USAT AND A RECIPROCAL TERMINAL
C     INDUCTANCE RIND = RCPL1.
C     THE TERM - STATE1*CISAT SPECIFIES THE ZERO FLUX LEVEL MAGNITIZING
C     CURRENT INTERCEPT FOR THE THREE REGIONS OF OPERATION. THIS
C     INTERCEPT CURRENT EQUALS 0 IN STATE 0 SINCE THIS MODEL EXHIBITS NO
C     HYSTERESIS AND -CISAT AND +CISAT IN THE +1 AND -1 STATES
C     RESPECTIVELY.
      STOP FUNCTION IDENTIFICATION INTEGERS I AND J MUST BE UNIQUELY
C     CHOSEN SO THAT J = I + 1 AND NO OTHER STOP FUNCTION IS IDENTIFIED
C     BY EITHER OF THE SAME NUMBERS. THIS ALLOWS THE USER TO DISTINGUISH
C     ALL THE VARIABLES ASSOCIATED WITH A GIVEN INDUCTOR BY APPENDING
C     THE INTEGER I TO THE END OF THE NAME OF EACH ASSOCIATED VARIABLE
C     AS SHOWN ABOVE. A SECOND EXAMPLE IS SHOWN BELOW OF THE CALL PLIND
C     AND CURRENT SOURCE DESCRIPTION STATEMENTS AS THEY SHOULD ACUALLY
C     APPEAR IN THE DEVICE DESCRIPTION PORTION OF THE TAG DESCRIPTION
C     DECK.
C     CALL PLIND(SS0103,RIND1,STATE1,CISAT1,$1FLXST1,$2FLXST2,FLXIN1,
C    1DATA1,LLCNT,LALGFT,1)
C     SI0103 = RIND1*(SS0103 + FLXIN1) - STATE1*CISAT1
C     ARG(1)  = FLUX     - TIME INTEGRAL OF VOLTAGE BETWEEN NODES XX AND
C                          YY IN VOLT-SECS
C     ARG(2)  = RIND     - RECIPROCAL OF INCREMENTAL INDUCTANCE
C                          IN AMPS/VOLT-SEC
C     ARG(3)  = STATE    - STATE FLAG - INDICATES PRESENT STATE OF CORE -
C                          -1 FOR NEG SAT - 0 FOR U=UMAX - +1 FOR POS SAT
C     ARG(4)  = CISAT    - EXTRAPOLATED VALUE OF INDUCTOR CURRENT AT ZERO
C                          TERMINAL FLUX FOR STATES +1 AND -1  IN AMPS
C     ARG(5)  = FLXSTI   - LOWER FLUX LIMIT STOP FUNCTION
C     ARG(6)  = FLXSTJ   - UPPER FLUX LIMIT STOP FUNCTION
C     ARG(7)  = FLUXIN   - INITIAL VALUE OF TERMINAL FLUX  IN VOLT-SECS
C     ARG(8)  = DATA     - 6 MEMBER ARRAY OF CORE AND WINDING PARAMETERS
C     ARG(9)  = LLCNT    - STOP FUNCTION FLAG - NOMINALLY EQUAL TO -1
C                          EQUAL TO N AT FLXSTN = 0.
      ARG(10) = LALGFT   - INITIALIZING FLAG - EQUAL TO 1 ON FIRST PASS -
C                          EQUAL TO 2 THEREAFTER
C     ARG(11) = I        - LOWER LIMIT STOP FUNCTION IDENTIFYING INTEGER
C     DATA(1) = PTURNS   - NUMBER OF TURNS IN PRIMARY WINDING
C     DATA(2) = PATHLN   - MAGNETIC MEAN PATH LENGTH IN INCHES
C     DATA(3) = CSAREA   - MAGNETIC CROSS SECTIONAL AREA IN SQUARE INCHES
C     DATA(4) = BMAX     - MAXIMUM FLUX DENSITY IN GAUSSES
```

```
      DATA(5) = UMAX     - AVERAGE MAXIMUM PERMEABILITY IN GAUSS/OERSTED
      DATA(6) = URATIO   - RATIO OF PERMEABILITIES   UMAX/USAT
      DIMENSION DATA(6)
      CALCULATE TOTAL TERMINAL FLUX
      TFLUX = FLUX + FLXIN
      IF(LALOFT-1) 100,100,110
  100 CONTINUE
      CALCULATE MAXIMUM WINDING FLUX IN VOLT-SECS
      FLUXMX = 6.4516E-8 * BMAX * CSAREA * PTURNS
      FLUXMX=6.4516E-8*DATA(4)*DATA(3)*DATA(1)
      CALCULATE MAXIMUM RECIPROCAL WINDING INDUCTANCE IN AMPS/VOLT-SEC
      RCPL0 = 3.1550E+7 * PATHLN / ( UMAX * PTURNS **2 * CSAREA )
      RCPL0=3.1550E+7*DATA(2)/(DATA(5)*DATA(1)**2*DATA(3))
      CALCULATE SATURATED RECIPROCAL WINDING INDUCTANCE IN AMPS/VOLT-SEC
      RCPL1 = RCPL0 * URATIO
      RCPL1=RCPL0*DATA(6)
      CALCULATE ABSOLUTE VALUE OF ONE STATE CURRENT INTERCEPT IN AMPS
      CISAT = RCPL0 * FLUXMX * (URATIO - 1.)
      CISAT=RCPL0*FLUXMX*(DATA(6)-1.)
      CALCULATE THE ABSOLUTE VALUE OF THE BREAK POINT FLUX IN VOLT-SECS
      FLXBKP = FLUXMX
      CALCULATE THE ABSOLUTE VALUE OF THE BREAK POINT FLUX ROUND OFF
      GUARDBAND IN VOLT-SECS
      DFLXBP = FLXBKP * 5.E-7
      CALCULATE ACTUAL UPPER BREAKPOINT FLUXES IN VOLT-SECS
      FLUXHH = + FLXBKP + DFLXBP
      FLUXHL = + FLXBKP - DFLXBP
      CALCULATE ACTUAL LOWER BREAKPOINT FLUXES IN VOLT-SECS
      FLUXLH = - FLXBKP + DFLXBP
      FLUXLL = - FLXBKP - DFLXBP
      DETERMINE INITIAL STATE OF CORE
      IF(TFLUX-FLUXLH)10,11,11
   10 STATE=-1.
      GO TO 15
   11 IF(TFLUX-FLUXHL)13,13,12
   12 STATE=+1.
      GO TO 15
   13 STATE= 0.
   15 CONTINUE
      IF(STATE) 104,106,108
  104 CONTINUE
      FLUXH = FLUXLH
      FLUXL = -1.E30
      RIND = RCPL1
      GO TO 109
  106 CONTINUE
      FLUXH = FLUXHH
      FLUXL = FLUXLL
      RIND = RCPL0
      GO TO 109
  108 CONTINUE
      FLUXH = +1.E30
      FLUXL = FLUXHL
      RIND = RCPL1
      GO TO 109
  109 CONTINUE
C     CALCULATE INITIAL VALUE OF MAGNITIZING CURRENT
      FI00I = RIND * TFLUX - STATE * CISAT
C     OUTPUT INITIAL VALUES AND CALCULATED CONSTANTS
      WRITE OUTPUT TAPE 6,1000,(DATA(I),I=1,6)
```

```
1000 FORMAT (1H1/20X,15HCORE DATA ARRAY//
    120X,8HPTURNS =,E16.8,6H TURNS,14X,21HPRIMARY WINDING TURNS/
    220X,8HPATHLN =,E16.8,7H INCHES,13X,21HMEAN MAG. PATH LENGTH/
    320X,8HCSAREA =,E16.8,10H INCHES**2,10X,20HCROSS SECTIONAL AREA/
    420X,8HBMAX   =,E16.8,8H GAUSSES,12X,20HMAXIMUM FLUX DENSITY/
    520X,8HUMAX   =,E16.8,16H GAUSSES/OERSTED,4X,20HMAXIMUM PERMEABILIT
    6Y/20X,8HURATIO =,E16.8,8H (RATIO),12X,21HRATIO OF UMAX TO USAT)
     WRITE OUTPUT TAPE 6,1001,FLUXMX,CISAT,RCPLO,RCPL1
1001 FORMAT (1H0/    20X,31HCALCULATED INDUCTANCE CONSTANTS//
    120X,8HFLUXMX =,E16.8,10H VOLT-SECS,10X,53HSATURATION FLUX LEVEL -
    2ALSO EQUAL TO BREAKPOINT FLUX/
    320X,8HCISAT  =,E16.8,5H AMPS,15X,54HMAGNITUDE OF FLUX AXIS INTERCE
    4PT CURRENT IN SATURATION/
    520X,8HRCPLO  =,E16.8,14H AMPS/VOLT-SEC,6X,39HRECIPROCAL INDUCTANCE
    6 FOR HIGH U REGION/
    720X,8HRCPL1  =,E16.8,14H AMPS/VOLT-SEC,6X,42HRECIPROCAL INDUCTANCE
    8 FOR SATURATED REGION)
     WRITE OUTPUT TAPE 6,1002,TFLUX,FIOUT,STATE
1002 FORMAT(1H0,/20X,27HINITIAL STATE OF INDUCTANCE//
    120X,8HTFLUX  =,E16.8,10H VOLT-SECS,10X,30HINITIAL VALUE OF TERMINA
    2L FLUX/
    320X,8HIMAG   =,E16.8,5H AMPS,15X,36HINITIAL VALUE OF MAGNITIZING C
    4URRENT/
    520X,8HSTATE  =,F5.1,31X,21HINITIAL STATE OF CORE/ )
     GO TO 120
 110 IF(LLCNT - (I + 1)) 111,111,120
 111 IF(LLCNT - 1) 120,130,140
 120 CONTINUE
C    CALCULATE VALUES OF FLUX LIMIT TRIGGER FUNCTIONS
     FLXST1 = + TFLUX - FLUXL
     FLXST3 = - TFLUX + FLUXH
     RETURN
 130 IF(STATE) 150,160,170
 150 GO TO 220
 160 CONTINUE
     FLUXH = FLUXLH
     FLUXL = -1.E30
     STATE= -1.
     RIND = RCPL1
     GO TO 120
 170 CONTINUE
     FLUXH = FLUXHH
     FLUXL = FLUXLL
     STATE= 0.
     RIND = RCPLO
     GO TO 120
 140 IF(STATE) 170,190,200
 190 CONTINUE
     FLUXL = FLUXHL
     FLUXH = +1.E30
     STATE= +1.
     RIND = RCPL1
     GO TO 120
 200 GO TO 230
 220 WRITE OUTPUT TAPE 6,1010
1010 FORMAT (1H0,33HLOWER TRIGGER FIRED IN REGION -1.)
     GO TO 120
 230 WRITE OUTPUT TAPE 6,1020
1020 FORMAT (1H0,33HUPPER TRIGGER FIRED IN REGION +1.)
```

END