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A DIGITAL INTERFACE FOR THE COMPUTER CONTROL OF A REMOTE MANIPULATOR

Report 1-66-49

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1966

ERRATA

P 33	Line 13	fli-flop should read flip-flop
P 43	Line 2	flip-flops should be flip-flop
	Line 5	flip-flops should be flip-flop
	Last Line	SKA '0240 should be SKS '0240
P 49	Line 1	Delete dots (.....) after Hand Rotation
P 78	Line 2	during should be driving
P 80	Parts List	Missing wattage values are all .25W
	Schematic	Table referenced is Table 11
P 84	Schematic	Voltages missing: -18v, collector supply; -6v, clamp supply; +12v, base bias supply.
		Unmarked resistor is R5
P 96	Schematic	Arrow (↑) To Light Panel missing
P 100	SG Gate at B-11	Inputs missing: Input 5 IFRDY- Input 6 START+
P 104	Figure 60	Page number should be 103
P 106	HD Gate at B-14	Input missing: Input 6 LDBFR +
P 107	Line 1	Add 116 after DDP-
	Line 6	Underline: S-PAC Instruction Manual (1mc).
	Line 17	Underline: Model 3000 Manipulator: Specifications and Description

ABSTRACT

A general purpose interface for communication between a DDP-116 Computer and an arbitrary input/output device was designed and implemented. Its use and operation is described, both from the viewpoint of a programmer and a device.

An additional digital logic system was constructed to multiplex the interface input/output lines with the servo loops of a seven-axis remote manipulator.

A General Mills Model 100 manipulator was modified to give it motions comparable to those of a PAR Model 3000.

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CHAPTER I

INTRODUCTION

Background

A Remote Manipulator or "mechanical arm" as it is sometimes called, is a remotely controlled device that is commonly used to perform tasks that a man cannot perform, either because of his strength limitations or because the task is to be performed in a man-alien environment such as a high radioactivity area.

One of the first and simplest remote manipulators was probably a stick or tree branch with which prehistoric man stirred his fire. This was a simple task which required a simple manipulator and the simplest of controls.

As the complexity of the task has increased the complexity of the manipulator has increased also, to the point where the control of the manipulator is many times a more formidable problem than the task itself.

This can be especially true in the case of a multiple axis manipulator in which each axis must be positioned by an operator so that the task may be performed. The positioning of several axes and the performance of a task usually requires a highly skilled operator, and may consume a considerable amount of time.

The possibility of using a digital computer as an aid in reducing the required operating time is currently under investigation in the Digital Systems Laboratory at Case Institute of Technology.

In order that this investigation be conducted the experimental system illustrated in Figure 1 has been implemented. It consists of:

1. A Computer Control Company DDP 116 real-time computer with a teletype input/output.
2. A digital communication and control channel.
3. An axis servo system with manual inputs[1].
4. A seven-axis remote manipulator.

Thesis Area

The areas of the over-all system with which this thesis is concerned are the digital communication and control channel and the manipulator proper.

The digital channel is conveniently divided into two sections: a general purpose section, called the General Purpose

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[1] P. W. Hammond, "A Computer Controlled Positioning System for a Remote Manipulator", M.S. Thesis, Case Institute of Technology, Cleveland, Ohio, 1966.

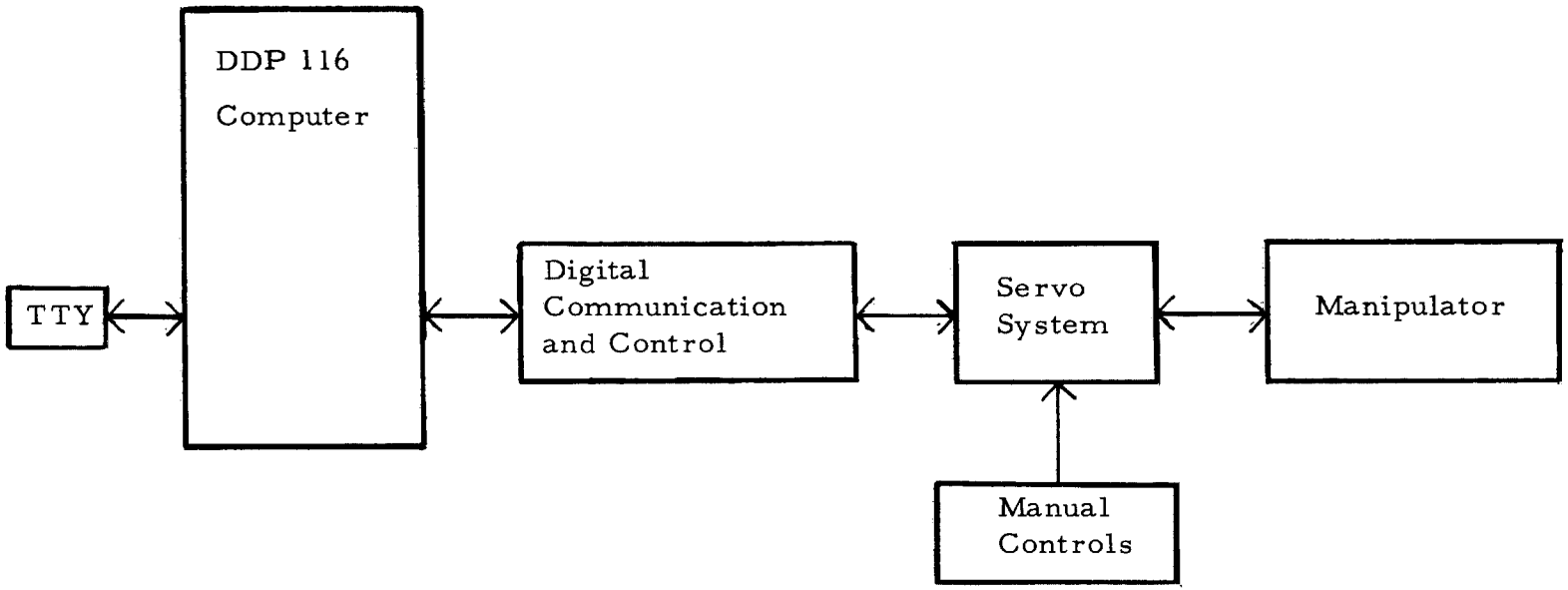


Figure 1 Experimental System

Interface, which may be used by a variety of Input/ Output (I/ O) devices; and a special purpose section, called the Manipulator Logic, which is particular to the operation of the manipulator. These two sections are described in Chapters II and III respectively.

Chapter IV describes the manipulator and some of the modifications that have been made to it.

CHAPTER II

THE GENERAL PURPOSE INTERFACE

Introduction

This chapter and Appendix I form an entity within themselves. Sufficient information is presented to enable those with only rudimentary knowledge of computer programming to connect a system to the General Purpose Interface.

To facilitate the understanding of the General Purpose Interface a brief description of the DDP 116 Input/Output (I/O) operation is given. A more complete discussion may be found in the publications: Programmers Reference Manual for the DDP 116 General Purpose Computer; and Interface Manual for the DDP 116 General Purpose Computer. (both, Framingham: Computer Control Company, 1965.)

DDP 116 I/O Structure

The DDP 116 communicates with its I/O devices through an input/output bus structure which consists of a sixteen line data input bus, a sixteen line data output bus, a ten line address bus, and several control lines. Table 1 lists these I/O bus lines. All I/O devices time share these common lines, and each must be

TABLE 1

DDP 116 INPUT/OUTPUT BUS LINES

Mnemonic	Name	Description
$INB_{\emptyset 1-16}$-	Input Bus	Transmits data from device interface to computer.
$OTB_{\emptyset 1-16}$-	Output Bus	Transmits data from computer to device interface.
ADB_{11-16}-	Address Bus	Specifies I/O device selected.
$ADB_{\emptyset 7-1\emptyset}$-	Address Bus	Specifies function selected device is to perform.
OCPXX-	Output Control Pulse	Prepares device for a specific mode of operation.
OTPXX-	Output Timing Pulse	Indicates time at which device interface may take data from output bus.
RRLXX-	Reset Ready Line	Timing pulse that signals the device interface that an I/O transfer has been made.
DRLXX-	Device Ready Line	Response to computer that device is ready in the condition tested.
PILXX-	Priority Interrupt	Device requests service from computer in normal I/O control.
SMKIX-	Priority Interrupt Mask Line	Pre-decoded output command that indicates the OTB contains a new setting for the interrupt mask flip-flop.
DAL$\emptyset$3-	Device Address Line	Signals device interface that a DMC I/O transfer is to take place.

TABLE 1 (Continued)

Mnemonic	Name	Description
DILØ3-	Device Interrupt Line	Device interface demands service from computer in DMC control,
ERLXX-	End of Range Line	Signal to device interface indicating that the end of the memory block assigned has been reached and that no further DMC demands can be issued by the interface.
STOPX-	Stop DMC Line	Signals DMC that device cannot handle any further I/0. Restores program control in DMC block transfer mode.
NCOXX-	System Normalize	Conditions flip-flops in interface when power is turned on.
MSTCL-	Master Clear	Conditions flip-flops in interface when master clear button is pressed.

equipped with a suitable control interface that will allow the device to have access to the lines only while the computer is communicating with it. A simplified diagram of the I/O structure is shown in Figure 2.

The computer is responsible at all times for determining which device is connected to the bus, and whether the function is a data transfer, a sense status or a control command. In a typical I/O operation the computer sends out on the address bus a six bit device address and a four bit function code. Each device monitors the address bus and, when its particular address appears, decodes the function code to determine what function it is to perform. If the function is a data transfer or a sense status, the device replies with an indication of its condition and the computer takes the appropriate action based on the reply. If the function is a control command the device does not reply and the computer assumes the command was executed.

The I/O functions are initiated by the I/O instructions listed in Table 2. Bits seven through sixteen of the instruction word are gated onto the address bus to form the device address and function code. Bits one through six are used by the computer to determine the operation. The instruction word format is

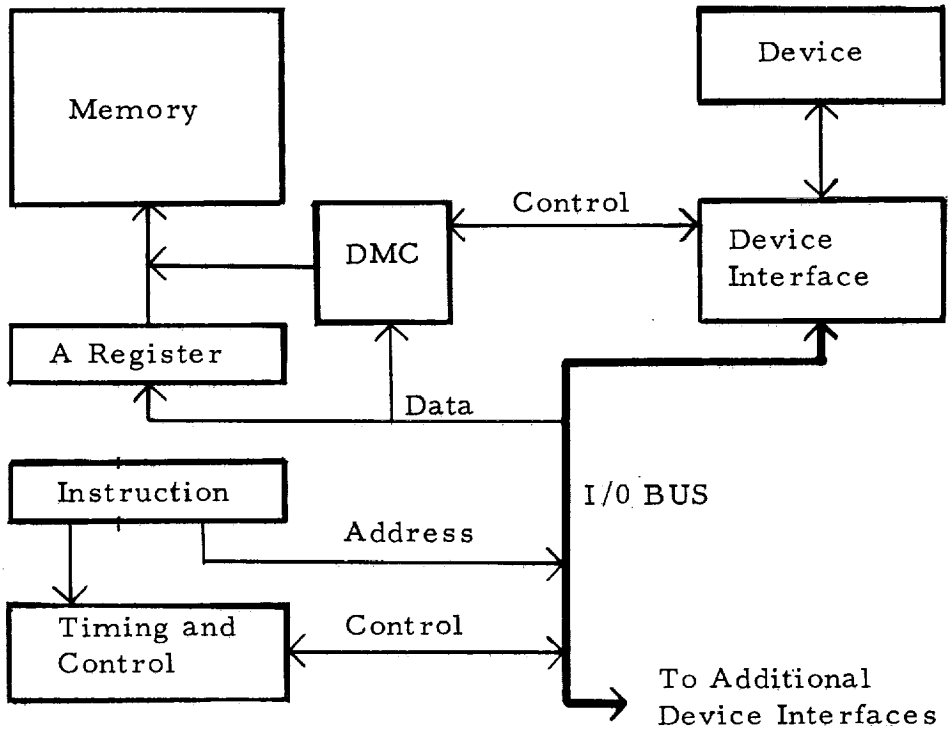


Figure 2 DDP 116 I/0 Structure

TABLE 2

DDP-116 I/O INSTRUCTIONS

Mnemonic	Op Code	Description
OCP	'14*	Control command; used to send a pulse to the device interface to establish a condition in the interface or device.
SKS	'34	Sense status; used to test a condition in the interface or device. If the condition is true the DRLXX- line is grounded and the next instruction is skipped. If DRLXX- is not grounded the next instruction is executed.
OTA	'74	Outputs data word from the A register over the output bus. Performs an SKS to determine if interface can take data. If the SKS is true the computer issues OTPXX- and RRLXX- and the next instruction is skipped.
INA	'54	Performs an SKS to determine if interface has data. If the SKS is true the input bus is strobed into the A register and the next instruction is skipped.

* The symbol (') indicates an octal number.

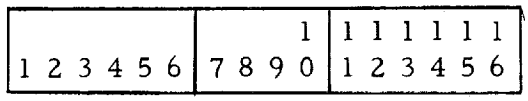


Figure 3 Instruction Word

illustrated in Figure 3.

Direct Multiplexed Channel (DMC) Control

DMC control is a hardware feature that permits data transfers with a minimum of program control. Data transfers are over the standard I/O bus with a block of memory that is assigned by setting up its starting and terminating addresses in standard memory locations. Once DMC control is initiated, by a special control command, data transfers take place on demand from the device, without program intervention.

Each device that is to use DMC control is assigned a single DMC channel with its own address line and interrupt line. Conditioning and testing of the device are done with the normal control command (OCP) and sense status (SKS) instructions.

When a DMC controlled device demands service the DMC suspends programming at the end of the current instruction and initiates a data transfer. The transfer can be either in a time-sharing or block transfer mode. In the time-sharing mode programming is resumed after a single word transfer is initiated. In the block transfer mode program execution is suspended until the entire memory block has been transferred.

General Purpose Interface

The General Purpose Interface (GPI) provides a communication and control link between the DDP 116 and an arbitrary external device. It is designed to relieve the device of most of the logic requirements necessary for communication with the computer. Address and function decoding are done within the GPI, and discrete control command and sense status lines are provided for the use of the device. A sixteen-bit buffer and a ready flip-flop synchronize I/O transfers with the computer processing cycles. DMC operation is also available.

Figure 4 shows the interconnecting lines between the computer and the GPI, and the lines available to the device. Tables 1, 3, and 4 list these lines and their uses.

Basically, I/O transfers take place in the following manner: During an I/O cycle the computer determines the state of the ready flip-flop, if it is set the computer assumes that an I/O transfer has been made between the GPI and the device and initiates an I/O transfer with the GPI. When the transfer is completed the computer resets the ready flip-flop and goes on to other programmed instructions. The device can also determine the state of the ready flip-flop and if it is reset assume that an

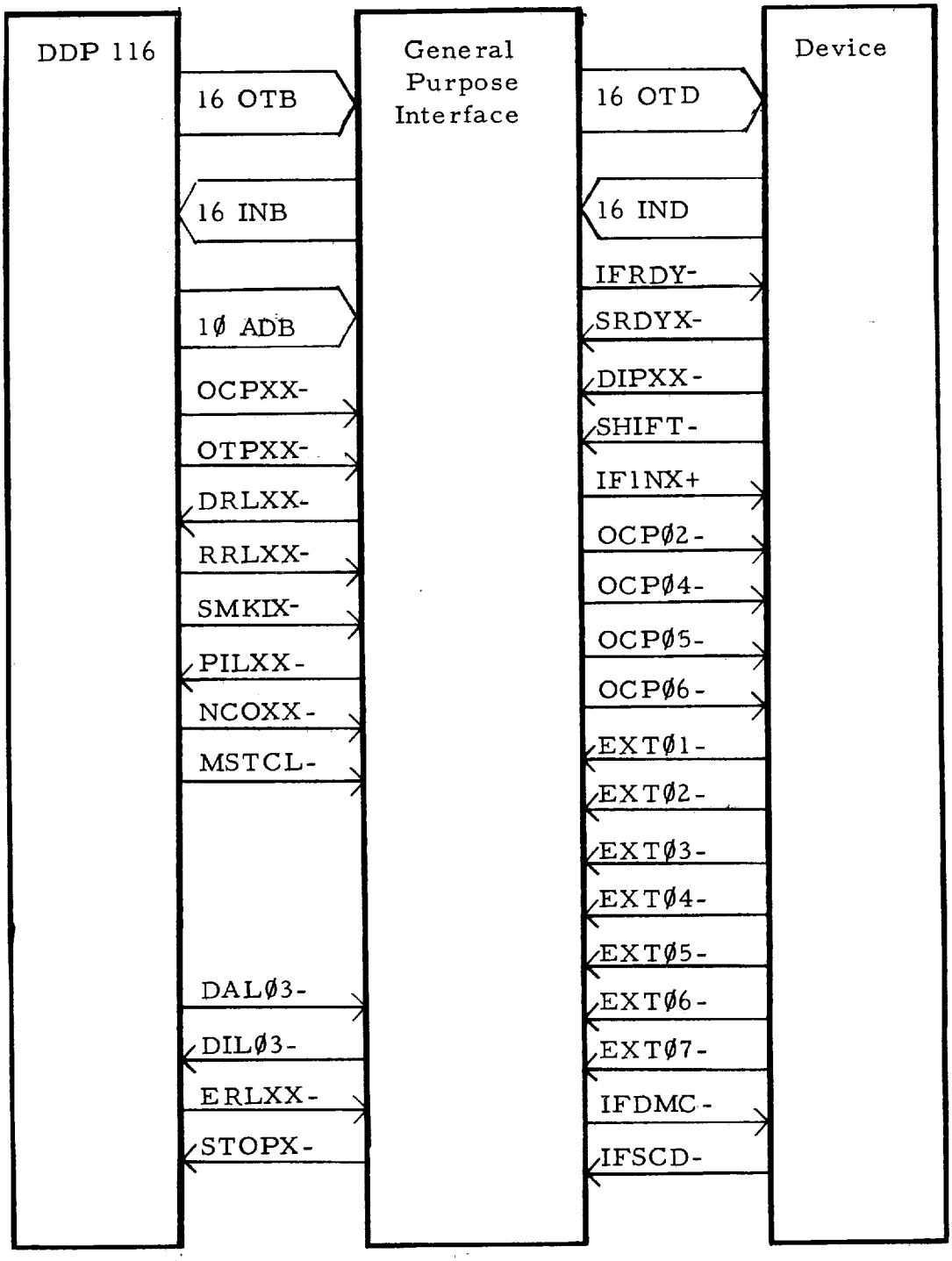


Figure 4 GPI Interconnections

TABLE 3

GPI OUTPUT LINES

Mnemonic	Name	Description
$OTD_{\emptyset 1\text{-}16}$-	Output Data	Transmits data from interface to device. Logical 1 0 volt Logical 0 -6 volt
IFRDY-	Interface Ready	Ready flip-flop, reset side. Logical 1 0 volt Logical 0 -6 volt
IFDMC-	Interface in DMC Control	DMC flip-flop, reset side. Logical 1 0 volt Logical 0 -6 volt
IFINX+	Interface in Input Mode	Input/output mode flip-flop. Input -6 volt Output 0 volt
OCPØ2-, OCPØ4-, OCPØ5-, OCPØ6-	Output Control Pulse	Discrete OCP lines for use of device. Active 0 volt Quiescent -6 volt

TABLE 4

GPI INPUT LINES

Mnemonics	Name	Description
$IND_{Ø1-16}$-	Input Data	Transmits data from device to interface Logical 1 0 volt Logical 0 -6 volt
EXTØ4-	External Line	Device activates PILXX- by grounding this line.
EXTØ1-, EXTØ2-, EXTØ3-, EXTØ5-, EXTØ7-, EXTØ7-	External Line	Conditions in device that are to be tested are connected to these lines. Logical 1 0 volt Logical 0 -6 volt
IFSCD-	Interface Stop Code	Device resets IFDMC- and activates STOPX- when DALØ3- is activated. Logical 1 0 volt Logical 0 -6 volt
DIPXX-	Drop In Pulse	Loads input data into GPI buffer. Active 0 volt Quiescent -6 volt
SRDYX-	Set Ready	Leading edge sets GPI buffers to all ones in output mode. Trailing edge sets the ready flip-flop. Active 0 volt Quiescent -6 volt
SHIFT	Shift Pulse	Trailing edge shifts contents of GPI buffer one place to right Active 0 volt Quiescent -6 volt

I/O transfer between the GPI and computer has been made. The device then initiates an I/O transfer with the GPI and sets the ready flip-flop on completion of the transfer.

Table 5 is a list of the I/O instructions pertinent to the use of the GPI. The GPI address is '40 and it has been assigned mask bit 8 and DMC channel 3.

GPI Output Signal Characteristics

The GPI output lines listed in Table 3 are driven by Computer Control Company PN-30 non-inverting power amplifiers. These amplifiers have an output drive capability of 96ma into 2000pf of stray capacitance at the O volt (current driving) level. Although some current may be drawn at the -6 volt level it is not recommended that this be done.

The characteristics that may be expected of these signals at the GPI I/O Connector are shown in Figures 5 and 6.

GPI Input Signal Requirements

The GPI input lines listed in Table 4 terminate in a specially built card in the computer. This card contains the collector load resistor and clamp diodes for an external transistor

TABLE 5

GPI I/0 INSTRUCTIONS

Instruction	Function
OTA'0040	Output from A, sense ready flip- flop
INA'0040	Input to A, sense ready flip-flop
SKS'0040	Sense ready flip-flop
SKS'0140	Sense EXTØ1-
SKS'0240	Sense EXTØ2-
SKS'0340	Sense EXTØ3-
SKS'0440	Sense not interrupting
SKS'0540	Sense EXTØ5-
SKS'0640	Sense EXTØ6-
SKS'0740	Sense EXTØ7-
OCP'0040	Enable input mode, reset buffer, reset ready flip-flop
OCP'0140	Enable output mode, set buffer, set ready flip-flop
OCP'0240	Output OCPØ2-
OCP'0340	Enable DMC
OCP'0440	Output OCPØ4-
OCP'0540	Output OCPØ5-
OCP'0640	Output OCPØ6-
OCP'0740	Reset DMC stop interrupt flip-flop

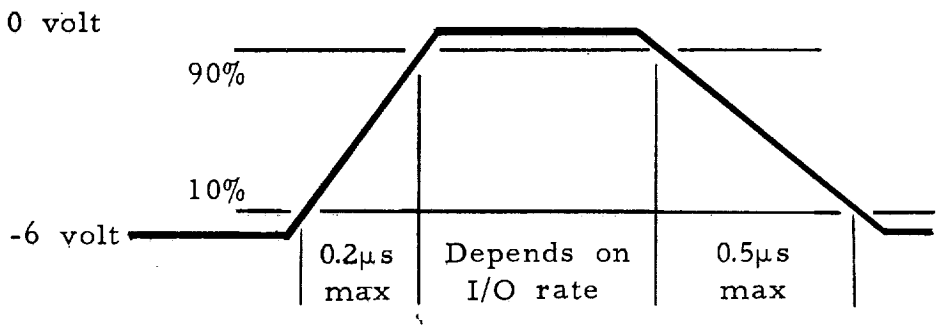


Figure 5 OTDNN-, IFRDY-, IFDMC-
IFINX+ Characteristics

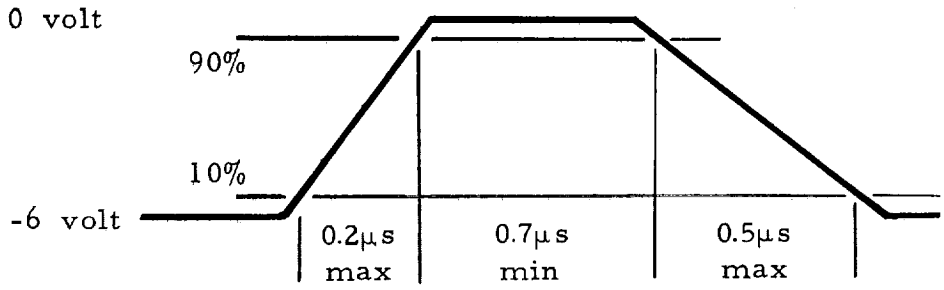


Figure 6 OCPNN- Characteristics

(see Figure 7). This method has the advantage of allowing input from a device with logic levels that are incompatable with the levels of the computer.

With the exception of the DIPXX-, SRDYX-, and SHIFT- pulses, the rise and fall times of the signals at the Interface I/O Connector are relatively unimportant. However, for reliability in timing and to present reasonable rise and fall times to the logic it is recommended that these times be no greater than 1.5 μs.

The DIPXX-, SRDYX-, and SHIFT- pulses have, in addition to the rise and fall time requirements, a minimum time that must be spent at the O volt level and a maximum repetition rate. The requirements of these signals which are to be met at the Interface I/O Connector are illustrated in Figure 8.

GPI I/O Connector

Connections are made to the GPI I/O lines through a pair of Winchester MRAC-50S connectors. Tables 6 and 7 list the connector pin assignments. Twisted pair cable is to be used in wiring from the device to the I/O connector and each signal line must have its associated ground line grounded in the device, preferably near the origin or termination of the signal. No more

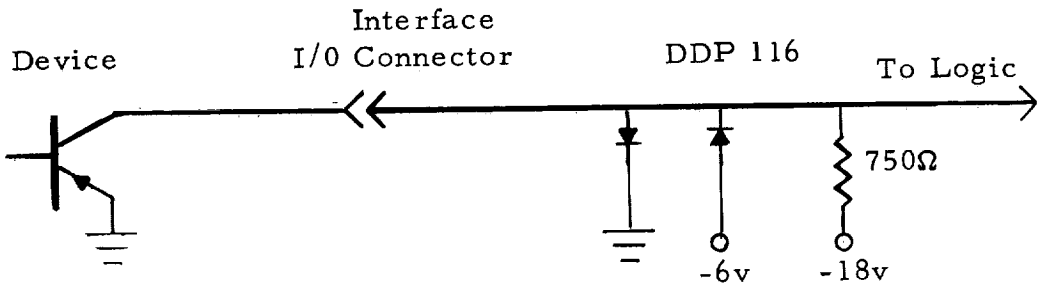


Figure 7 Input Line Termination

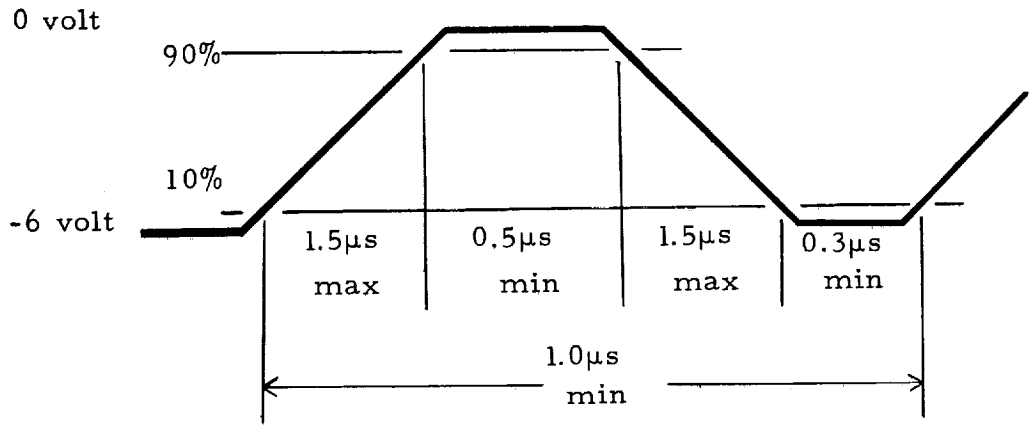


Figure 8 DIPXX-, SRDYX-, SHIFT-
Requirements

TABLE 6

GPI I/0 CONNECTOR G

Pin	Signal	Pin	Signal
A	EXTØ4-	e	OTDØ6-
B	EXTØ4-GND	f	OTDØ6-GND
C	OCPØ2-	h	INDØ6-
D	OCPØ2-GND	j	INDØ6-GND
E	IFSCD-	k	OTDØ5-
F	IFSCD-GND	m	OTDØ5-GND
H	OCPØ4-	n	INDØ5-
J	OCPØ4-GND	p	INDØ5-GND
K	SRDYX-	r	OTDØ4-
L	SRDYX-GND	s	OTDØ4-GND
M	OCPØ5-	t	INDØ4-
N	OCPØ5-GND	u	INDØ4-GND
P	SHIFT-	v	OTDØ3-
R	SHIFT-	w	OTDØ3-GND
S	OCPØ6-	x	INDØ3-
T	OCPØ6-GND	y	INDØ3-GND
U	DIPXX-	y	OTDØ2-
V	DIPXX-GND	AA	OTDØ2-GND
W	OTDØ8-	BB	INDØ2-
X	OTDØ8-GND	CC	INDØ2-GND
Y	INDØ8-	DD	OTDØ1-
Z	INDØ8-GND	EE	OTDØ1-GND
a	OTDØ7	FF	INDØ1-
b	OTDØ7-GND	HH	INDØ1-GND
c	INDØ7-		
d	INDØ7-GND		

TABLE 7

GPI I/0 CONNECTOR H

Pin	Signal	Pin	Signal
A	EXTØ1-	e	OTD14-
B	EXTØ1-GND	f	OTD14-GND
C	EXTØ2-	h	IND14-
D	EXTØ2-GND	j	IND14-GND
E	EXTØ6-	k	OTD13-
F	EXTØ-GND	m	OTD13-GND
H	IFDMC-	n	IND13-
J	IFDMC-GND	p	IND13-GND
K	EXTØ7-	r	OTD12-GND
L	EXTØ7-GND	s	OTD12-GND
M	IFRDY-	t	IND12-
N	IFRDY-GND	u	IND12-GND
P	EXTØ3-	v	OTD11-
R	EXTØ3-GND	w	OTD11-GND
S	IFINX	x	IND11-
T	IFINX-GND	y	IND11-GND
U	EXTØ5-	z	OTDIØ-
V	EXTØ5-GND	AA	OTDIØ-GND
W	OTD16-	BB	INDIØ-
X	OTD16-GND	CC	INDIØ-GND
Y	IND16-	DD	OTDØ9-
Z	IND16-GND	EE	OTDØ-GND
a	OTD15-	FF	INDØ9-
b	OTD15-GND	HH	INDØ9-GND
c	IND15-		
d	IND15-GND		

than 25 feet of cable is to be used in transmitting signals between the device and the I/O connector.

Theory of Operation

A block diagram of the GPI is shown in Figure 9. In the discussion that follows emphasis is placed on the control of I/O data transfers.

The address and function decoding logic respond to the ADBNN- lines whenever they are activated by the computer. Internal and control OCP'S are formed by ANDing the decoded Interface Function Codes (IFCNN) with the computer originated OCPXX-.

The SKS and interrupt logic ANDs the condition to be tested with the appropriate IFCNN to activate the DRLXX-line and ORs IFRDY-, IFSFX- and EXTØ4- to activate the PILXX- line. PILXX- is inhibited when the mask flip-flop is reset or during DMC operations.

The buffer and I/O gating stores and channels the data to be transferred. A zeros dropin is used when loading the buffer from the computer and a ones dropin when loading it from the

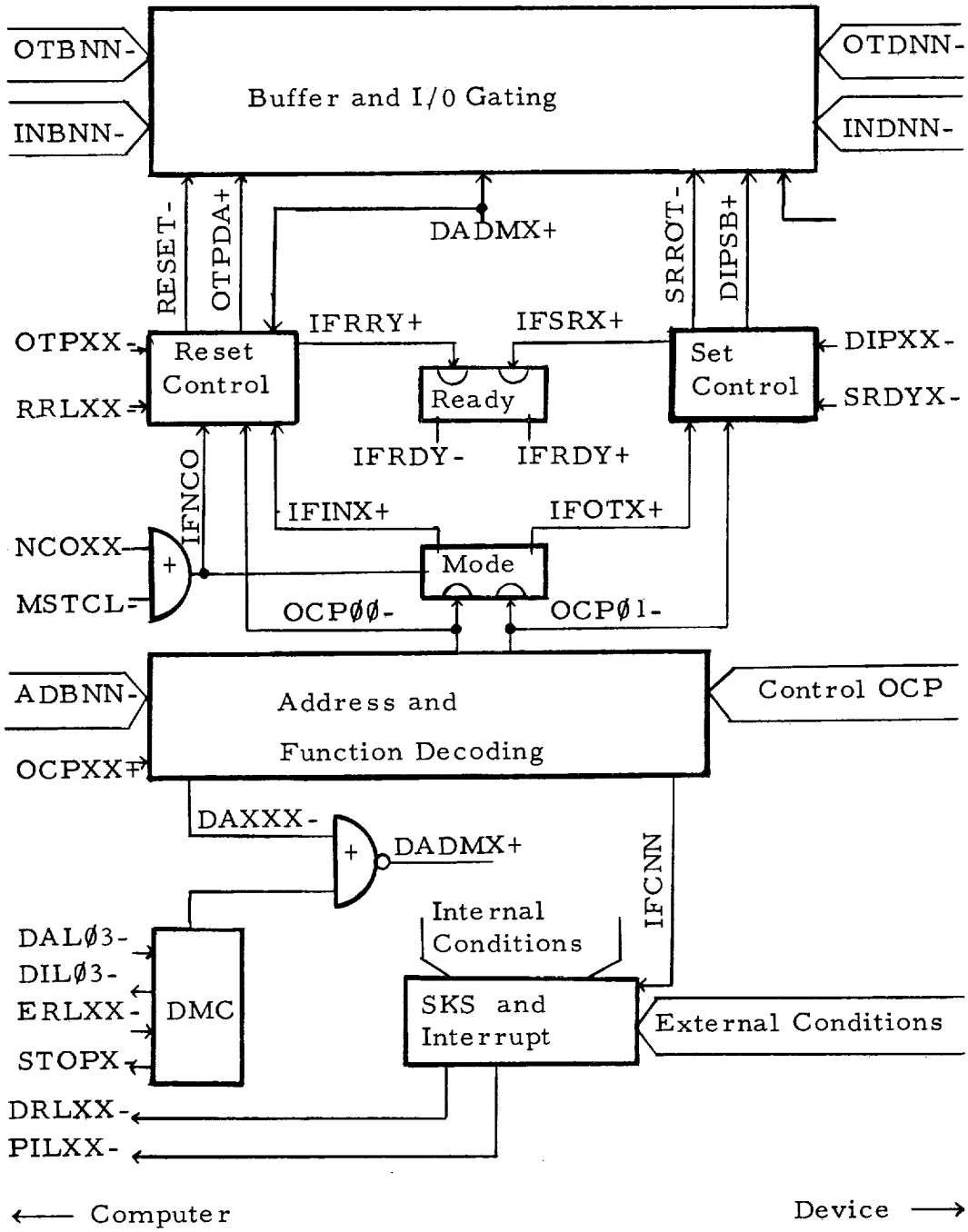


Figure 9 GPI Block Diagram

device. The reset and set controls perform the logic functions to accomplish this.

Input Data Transfers

The GPI is prepared to receive data from the device either by IFNCO-, which normalizes all control flip-flops and resets the buffer, or by an OCP'0040 I/0 instruction which outputs OCPØØ-. OCPØØ- sets the mode flip-flop to input (IFINX+), activates RESET- to reset the buffer, and causes IFRRX+ to reset the ready flip-flop. The ready flip-flop is reset on the trailing edge of IFRRX+. The device may then load the buffer by sending a DIPXX- pulse to form DIPSB+ (Dropin Pulse or Set Buffer) which sets those bits that have a logical one on their respective INDNN- lines (ones dropin). The ready flip-flop is set on the trailing edge of IFRRX+ which is derived from the device originated SRDYX- pulse. After the computer has taken the data from the buffer the RRLXX- pulse is issued which forms RESET- and IFRRX+. The buffer may again be loaded and the sequence repeated. Figure 10 shows the relative timing of the signals.

Output Data Transfers

An OCPØ1- pulse sets the mode flip-flop to output (IFOTX+), activates SBROT- (Set Buffer on Output) and forms DIPSB+. SBROT- acts as a pseudo INDNN- line with all ones, which DIPSB+

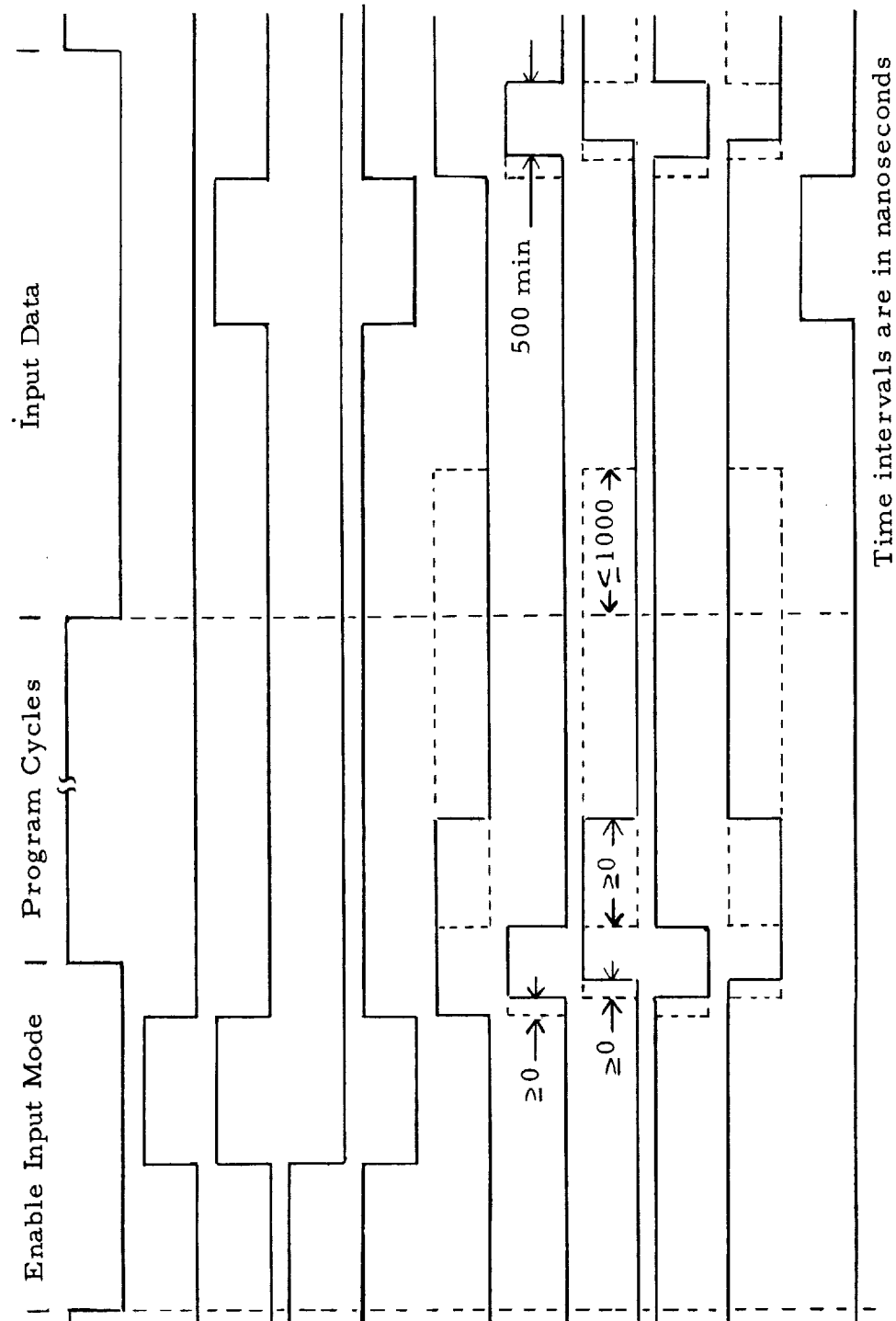


Figure 10 Input Data Transfers

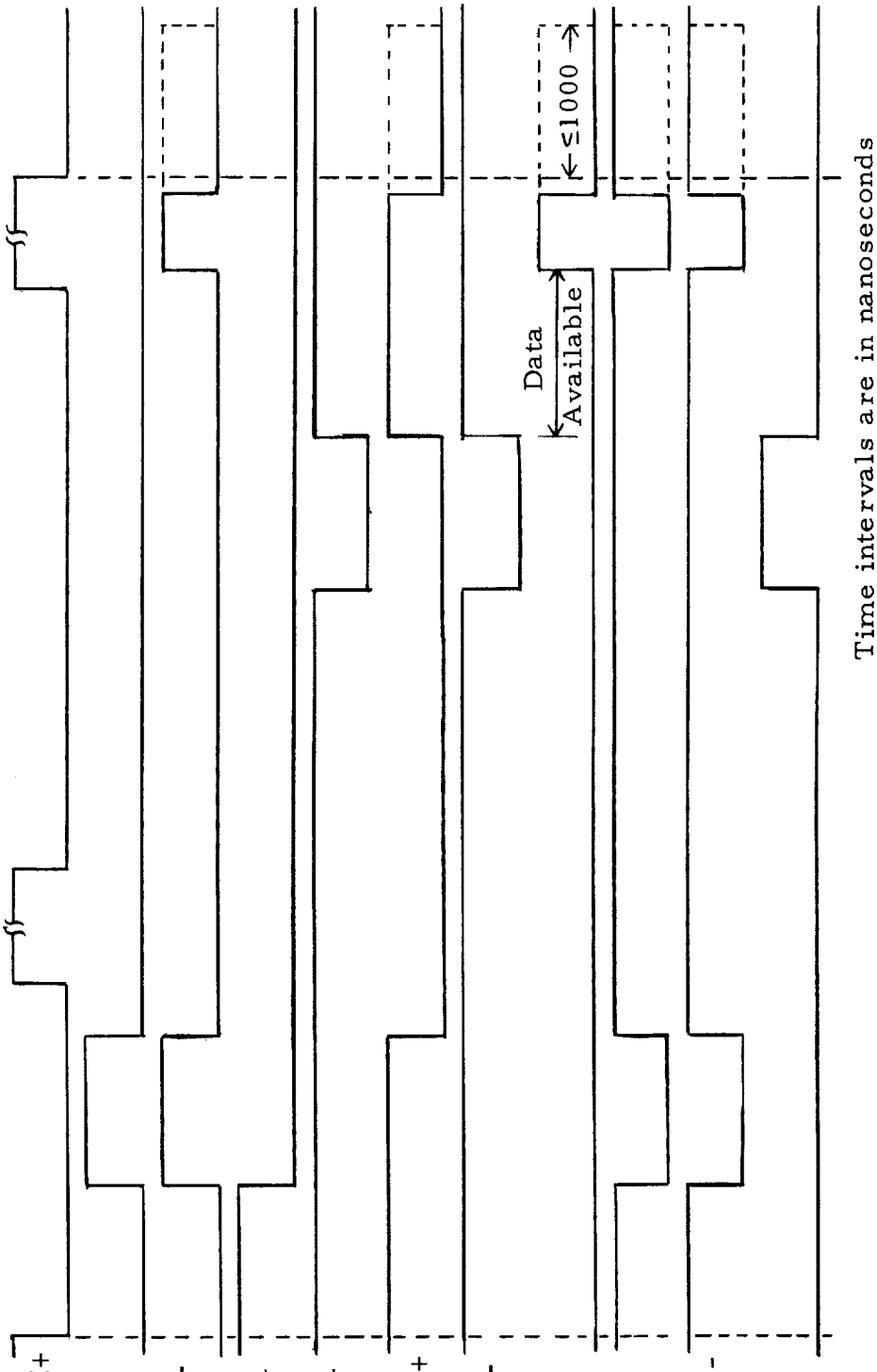
loads into the buffer. IFSRX+ is also derived from OCPØ1-. Data is loaded into the buffer by OTPDA+ (Output Pulse to Device Addressed) which resets those bits that have a logical zero on their respective OTBNN- lines (zeros dropin). OTPDA+ is formed from the OTPXX- pulse issued by the computer. RRLXX- is issued at the same time as OTPXX- and forms IFRRX+. After the data has been taken from the OTDNN- lines a SRDYX- pulse from the device makes up SBROT-, DIPSB+ and IFSRX+. Figure 11 shows the relative timing of the signals.

Shifting

Each shift pulse from the device shifts the contents of the buffer one bit to the right and a zero into the most significant bit. The shift occurs on the trailing edge of the shift pulse. Serial data may be entered on any of the INDNN lines by a sequence of DIPXX- and SHIFT- pulses or taken off any of the OTDNN lines by a series of SHIFT- pulses. In addition, blocks of input data may be packed in the buffer by loading the higher order bits with a block, shifting the block its length and loading another block. Output data may be blocked in a similar manner.

DMC Logic

I/0 transfers take place under DMC control in essentially the same manner as just described.



Time intervals are in nanoseconds

Figure 11 Output Data Transfers

The notable differences are the substitution of the DMC address (DALØ3-) for the standard address from the address bus, suspension of normal interrupts (PILXX- inhibited), and the activation of DIPØ3- by IFRDY to inform the computer that a buffer/device data transfer has been executed.

IFDMC- is set by an OCP'0340 and reset by an ERLXX- from the computer or by an IFSCD- from the device. IFSCD- also activates STOPX-. When IFDMC- is reset IFSFX+ (DMC Stop Interrupt Flip-flop) is set to activate PILXX-. IFSFX+ is reset by OCP'0740.

CHAPTER III

THE MANIPULATOR LOGIC

Introduction

The basic function of the Manipulator Logic is to multiplex the single I/O data channel from the General Purpose Interface to provide communication with each of the seven manipulator axis channels. A synchronizing pulse from the computer initializes a three-bit axis counter which is used to sequentially select axis channels for data transfer.

The computer generated digital position commands for each axis are stored by the manipulator logic in separate ten-bit axis buffers and converted to analog voltages by the servo system.

When operating the manipulator manually, position feedback to the computer can be accomplished by either of two analog to digital conversion techniques. The first is implemented by the manipulator logic, or hardware, and is conveniently referred to as the Hardware Analog to Digital mode or HAD mode for brevity. The second is done by a computer program, or software, and is correspondingly named the Software Analog to Digital mode (SAD mode). Either of these modes may be selected by program control.

In the HAD mode, each buffer functions as a bidirectional (up-down) counter, whose counting direction is controlled by a pair

of binary error signals from the servo system, to implement a tracking analog to digital converter.

In the SAD mode, buffer counting is inhibited and the binary error signals are sent to the computer in the form of a fourteen-bit error word. The software then adjusts the contents of each buffer until the error word is all zeros.

Figure 12 is a block diagram of the manipulator logic showing one axis channel.

Multiplexing

The axis counter is normally in the zero state (all bits reset) addressing axis zero. The synchronizing pulse from the computer initiates an axis counter clear cycle (to insure that the counter starts with the correct axis) and causes the counter to be set to one. When the ready flip-flop in the General Purpose Interface is reset, a sequence of timing pulses is generated that will load the GPI buffer on input mode or the axis buffer on output mode, set the ready flip-flop, and increment the axis counter.

Data is loaded into the axis buffers by a double ended drop in. The output data lines are inverted, and the normal and inverted lines applied to the set and reset level controls of their corresponding bits in all axis buffers simultaneously. A buffer load pulse is gated to the AC set and reset inputs of the buffer being addressed

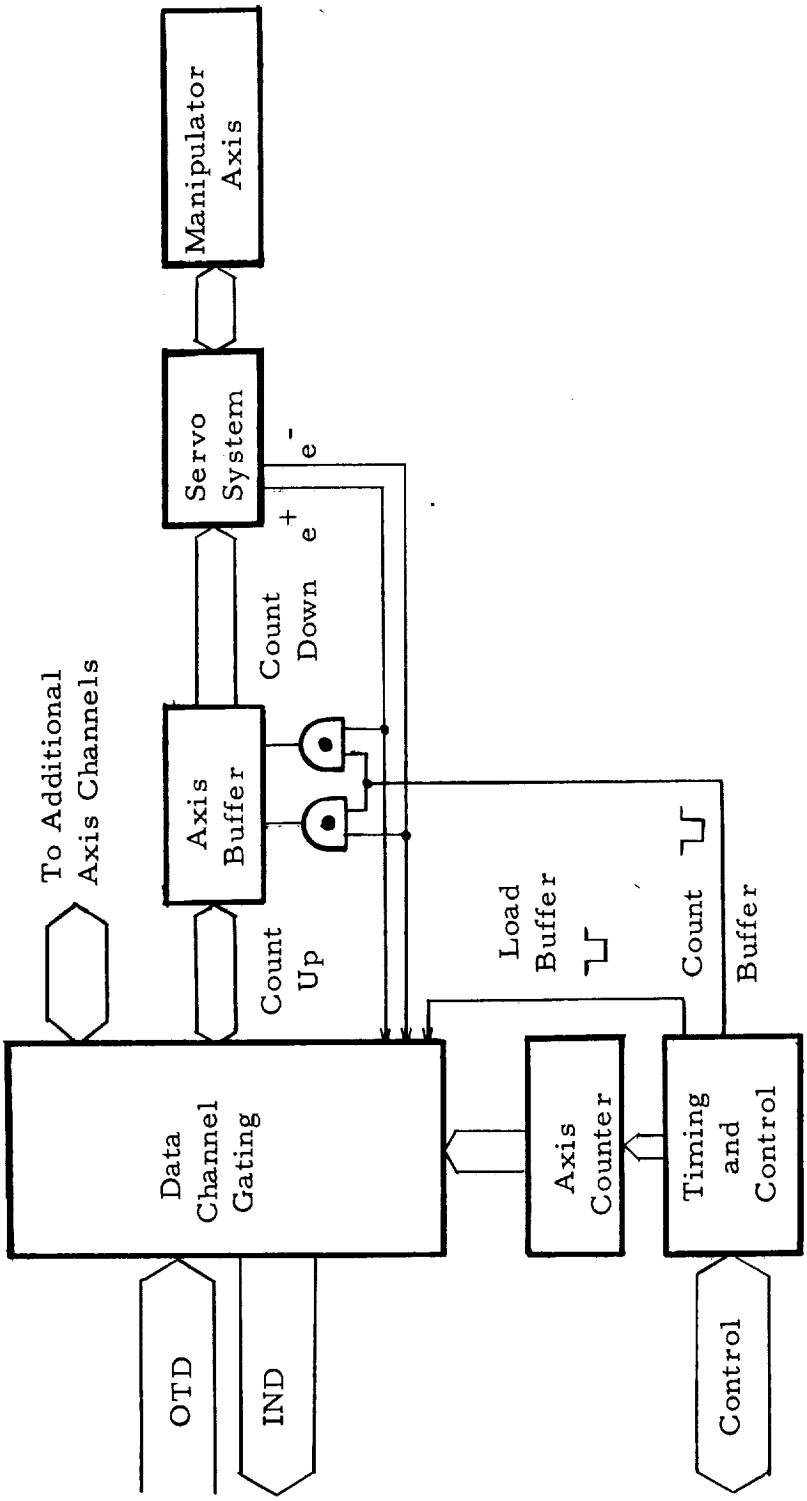


Figure 12 Manipulator Logic Block Diagram

to load the buffer.

Whenever a buffer is being addressed by the axis counter its contents are gated onto the input data lines to be loaded into the GPI buffer. Figure 13 illustrates the logical connection for bit 16 of Axes 1 and 2.

Figure 14 is a timing chart of the multiplexing operation. An OCPØ4- pulse sets the counter clear flip-flop (CLEAR+) and delay flip-flop DELY1+. The first clock pulse after CLEAR+ and DELY1+ have been set, sets DELY2+ and the next clock pulse resets CLEAR+ and DELY2+. Resetting CLEAR+ resets DELAY1+ which sets the start flip-flop, START+. Setting START+ sets the axis counter to one. On the first clock pulse after START+ is set, and the ready flip-flop (IFRDY-) is reset, a synchronizing fli-flop, SYNCX+, will be set. The clock is inverted to form CRDYX- which is AC coupled to a standard nand gate to form SRDYX- and DIPXX- to set the ready flip-flop and load the GPI buffer in input mode. A buffer load pulse, LDBFR+, is derived from CRDYX+ in output mode and gated to the buffer being addressed. The trailing edge of CRDYX+ increments the axis counter at the same time as SYNCX+ is reset by the clock. When IFRDY- is reset by the computer SYNCX+ will again be set by the clock and the sequence repeated.

It is not necessary to address all seven axes since the OCPØ4- causes a counter clear before setting the axis counter to

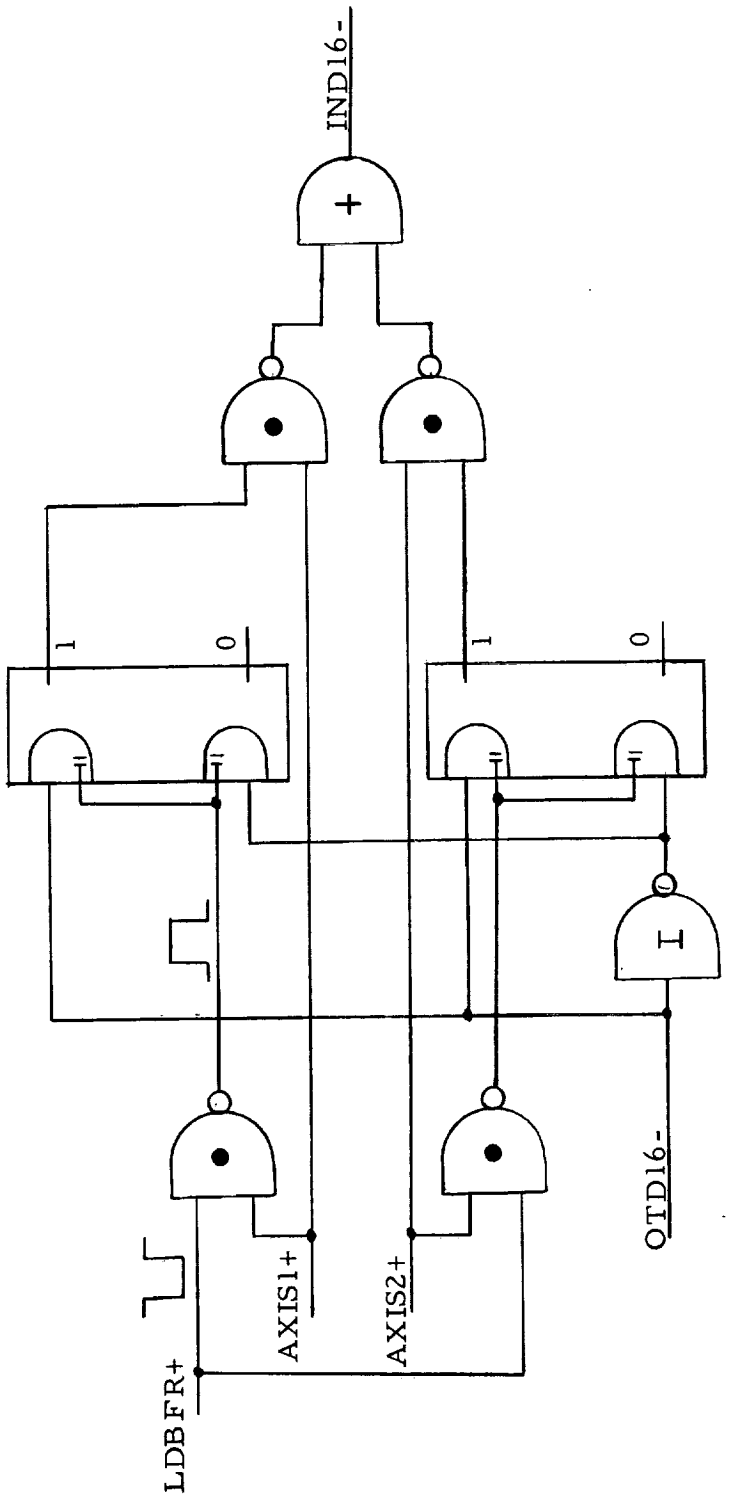


Figure 13 Data Channel Gating

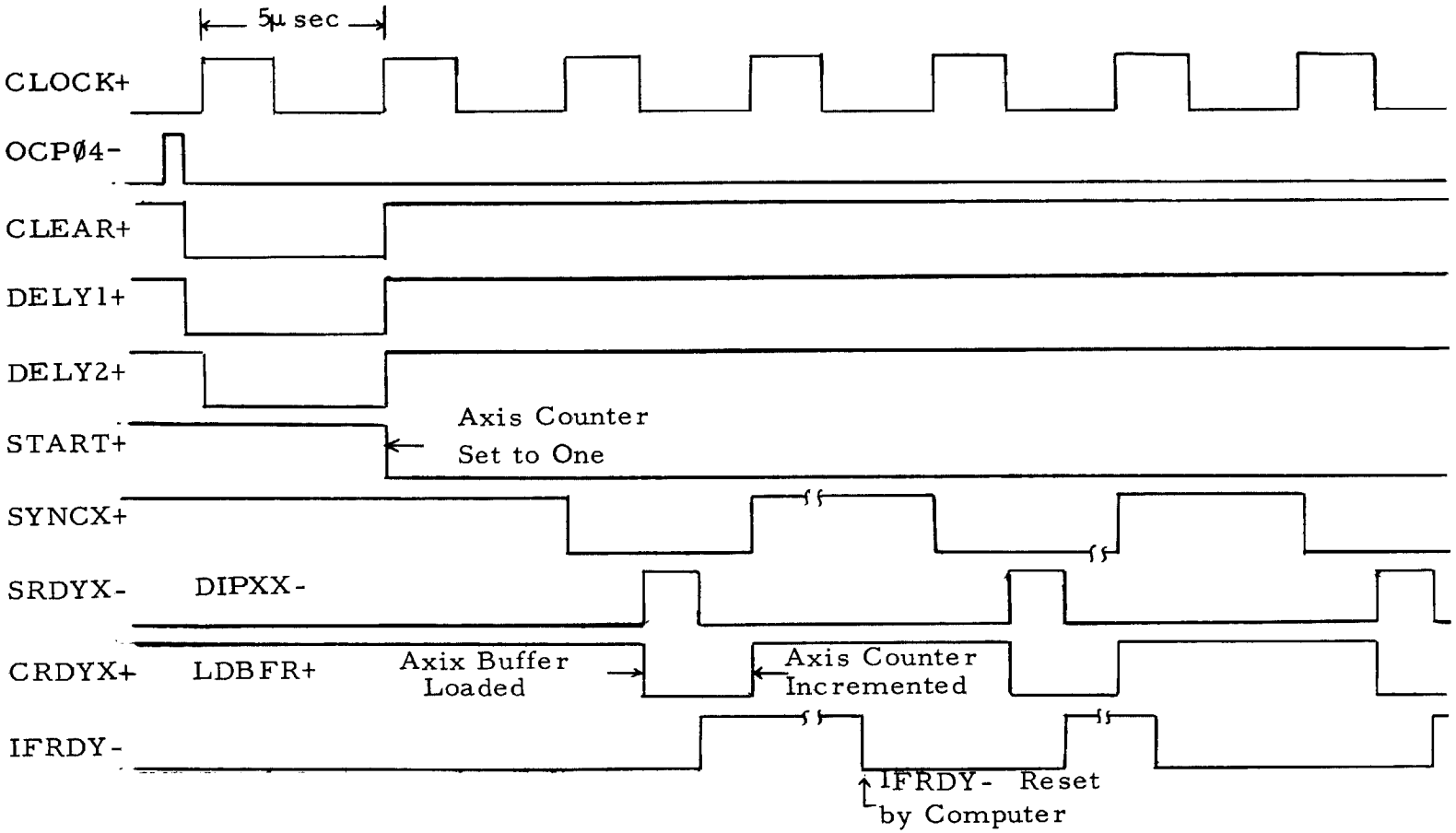


Figure 14 Multiplexing Timing

one. In addition, an OCPØ2- will initiate a counter clear but will not set DELY1+, so that START+ will not be set. START+ is reset on a counter clear or by an axis counter overflow.

Manual-Auto Selection

Manual and Automatic position commands originate from the operator's control panel and the computer, respectively. Relays in the servo system select one of these sources under control of a Manual-Automatic flip-flop in the logic. This flip-flop must be carefully controlled when a transition from Manual to Automatic is to be made since the axis buffers may be in a random state. The flip-flop will be set to Manual if any of the following conditions are true:

a. Manual-Auto toggle switch on operator's control panel in Manual.

b. Manipulator Logic not connected to GPI.

c. GPI in input mode.

d. Computer power off.

All of these conditions are under human control and can be used as "emergency halts" to automatic manipulator movements that might damage equipment or injure personnel.

If none of the conditions a, b, c, or d are true the flip-flop will be set to Auto on the following conditions:

e. Approximately 10 milliseconds after the last axis buffer has been counted to a no error condition.

f. Approximately 20 milliseconds after the GPI has been put into the output mode and no error exists.

g. Immediately by an OCP'0240 instruction.

Bidirectional Counting

The axis buffers are wired for ten bits of bidirectional counting in the manner illustrated in Figure 15, which is a three-bit implementation of the well-known[2] logical equations:

$$T_{Au} = B \cdot C \cdot Pu$$

$$T_{Bu} = C \cdot Pu$$

$$T_{C} = Pu$$

for up counting, and;

$$T_{Ad} = \overline{B} \cdot \overline{C} \cdot Pd$$

$$T_{Bd} = \overline{C} \cdot Pd$$

$$T_{Cd} = Pd$$

2 H. W. Mergler, et. al., "Digital Control Systems Engineering", Case Institute of Technology Summer Program Notes, Cleveland, Ohio, 1962. Vol. I, p. 4 - 8.

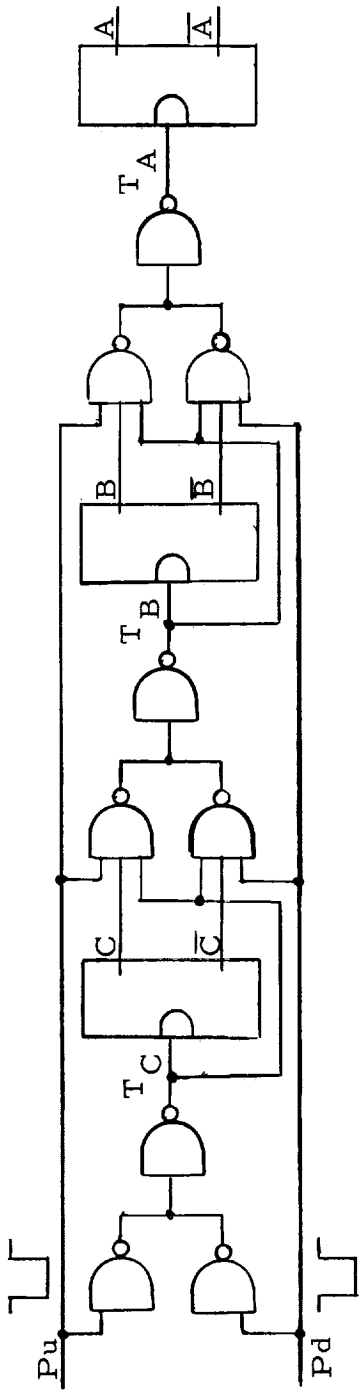


Figure 15 Three Bit Up-Down Counter

for down counting.

The T input equation for flip-flop A implemented by the three nand gates is:

$$T_A = B \cdot T_B \cdot Pu + \overline{B} \cdot T_B \cdot Pd$$

which, since $Pu \cdot Pd = 0$, reduces to

$$T_A = (T_{Au} + T_{Ad}) = (B \cdot C \cdot Pu + \overline{B} \cdot \overline{C} \cdot Pd)$$

In a general form the T input equations for the Nth bit of an M bit bidirectional counter are:

$$T_N = (N^{-1} \cdot Pu + \overline{N}^{-1} \; Pd) \cdot T_N{}^{-1}$$

Since triggering occurs on the trailing edge of the count pulses (Pu or Pd) there is no carry propagation time. However, the count pulse must remain negative long enough to ripple through all the gates preceding the Mth T input.

Counting Pulses

The counting pulses for the axes buffers originate from a low frequency oscillator in the servo system. The output of the oscilla-

tor is passed through several nand gates, shaped, and steered to the up or down count lines by the binary error signals. The shaping gates are also used to inhibit the oscillator output in the SAD and Auto modes, when buffer counting is not desired.

Error Word

Whenever the START+ flip-flop is reset (axis counter in zero state) the fourteen-bit error word formed from the binary error signals is gated onto the input data lines. The error word is loaded into the GPI buffer by an OCP'0640 instruction which issues an OCPØ6- to form DIPXX- and SRDYX-.

The error word is formated into seven two-bit groups, each group represents the error in its associated buffer relative to a no error condition, i.e., a positive error (0, 1) implies that the quantity in the buffer is too large and a negative error (1, 0) that it is too small. A no error condition is indicated by (0, 0).

Programmers Information

I/0 transfers with the axis buffers may be done either by INA and OTA instructions or under DMC control. In either case the restrictions on starting and stopping the axis counter and/or mode changes about to be described should be carefully noted by the programmer.

Output transfers - The manipulator logic will leave the the ready flip-flop set after the last transfer has been completed. Therefore, before changing mode, issuing an OCP'0240 or a second OCP'0440, either SKS ready or be certain that at least 10 microseconds of real time have elapsed since the output data was put into the GPI buffer. After a mode change from input to output, SKS Auto before issuing an OCP'0440 (see Manual-Auto selection).

Input transfers - If all axes are addressed, the ready flip-flop will be reset by the computer when the last axis data is taken from the GPI buffer. A mode change, OCP'0240 or OCP'0440 may then be issued. If only some of the axes are to be addressed, the manipulator logic will load the GPI buffer with one more axis and set the ready flip-flop. For example, if only the first three axes buffers are to be read, the logic will load the fourth one into the GPI buffer and set the ready flip-flop. Therefore, before changing mode, issuing an OCP'0240 or a second OCP'0440, either SKS ready or be certain that at least 10 microseconds of real time have elapsed since the last desired input data was taken from the GPI buffer.

Mode changes - Should never be made unless the axis counter is reset.

Table 8 lists the I/O instructions pertaining to the operation of the manipulator. Figure 16 shows the format of the error word and the names of each of the seven axes. The axes are addressed in ascending order, beginning with Axis 1. The nomenclature is discussed in the following chapter.

TABLE 8

MANIPULATOR I/O INSTRUCTIONS

Instruction	Function
OCP'0040	Enables input mode, sets the mode flip-flops in the GPI to input which in turn forces manual mode on the manipulator.
OCP'0140	Enables output mode, sets the mode flip-flops in the GPI to output which in turn permits auto mode.
OCP'0240	Initiates an axis counter clear cycle. Sets SAD mode. Sets the manual-auto flip-flop to auto if permitted (see OCP'0140).
OCP'0440	Initiates an axis counter clear cycle and sets DELY1+ which permits the axis counter to be set to one at the end of the cycle.
OCP'0540	Resets SAD mode.
OCP'0640	Loads error word into GPI.
SKS'0140	Sense no error in all axes.
SKA'0240	Sense auto mode.

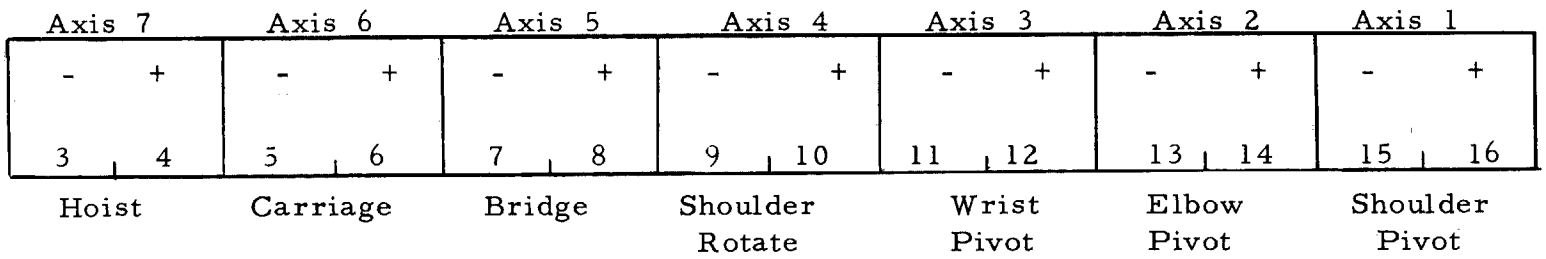


Figure 16 Error Word Format

CHAPTER IV

THE MANIPULATOR

Introduction

In order to provide a realistic experimental system a General Mills[3] Model 100 manipulator was purchased and modified to resemble a PaR[4] model 3000.

The Model 100 has a hand which pivots about a wrist attached to the lower end of a rotating hoist. The hoist is supported by a wheeled platform, or carriage assembly which is mounted on an overhead crane bridge. Typically, a Model 3000 system has, in addition to the elements of the Model 100, shoulder and elbow pivots which give it more versatility, and make it representative of the state of the art in manipulators.

The Case Manipulator is shown in Figure 17. The arm assembly, consisting of the shoulder elbow and wrist, was added to the Model 100 to increase the number of axes to seven, as in the Model 3000.

3, 4 Manufactured and distributed by Programmed and Remote Systems Corporation (PaR), St. Paul, Minnesota

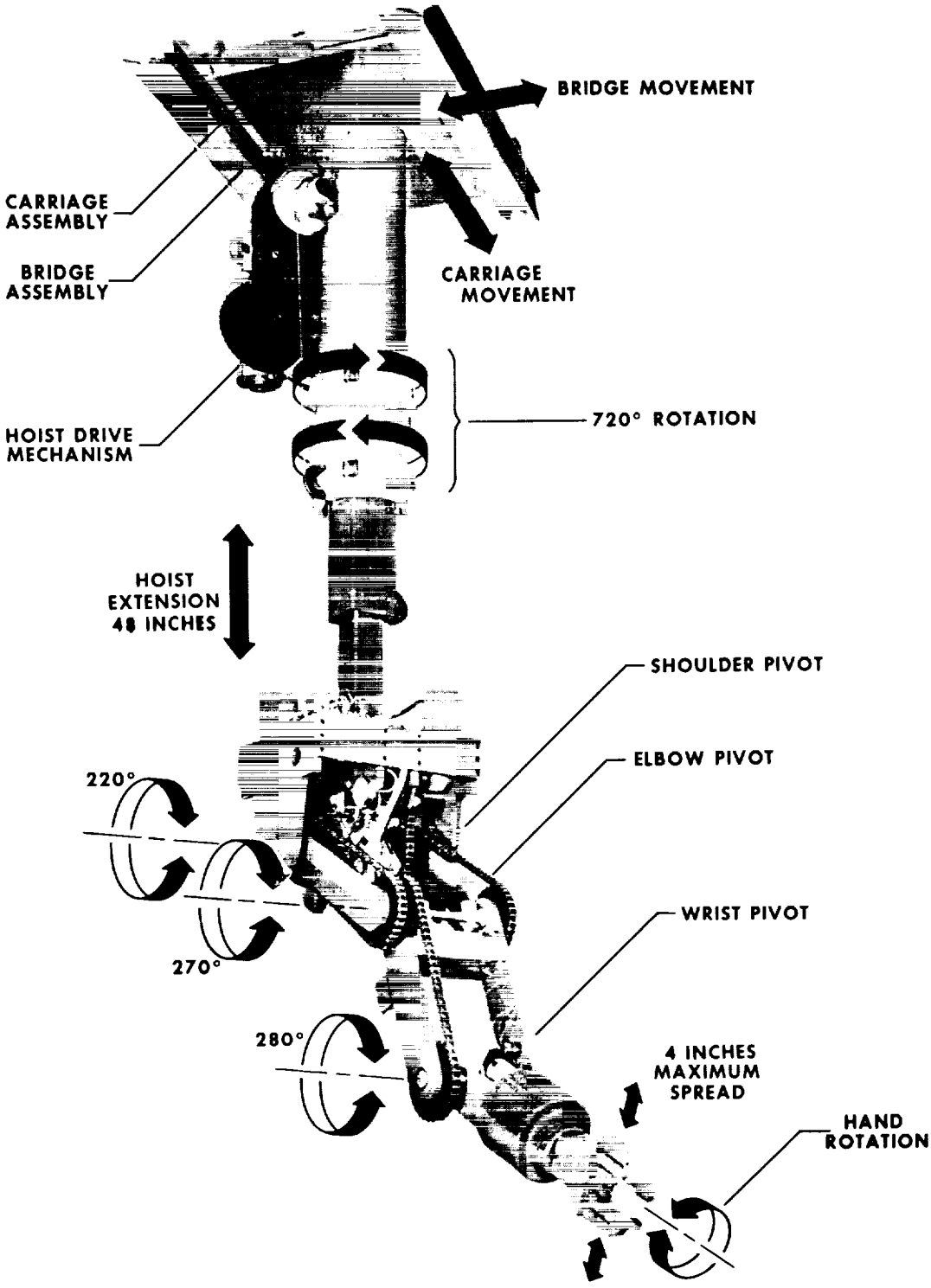


Figure 17 The Case Manipulator

Manipulator Specifications

Table 9 lists the specifications of the Case Manipulator, and compares them with the specifications of the PaR 3000. The velocities given are nominal no load maximums. Under rated load they are typically 0.6 of the no load velocities.

The absolute pivot angles specified in Table 9 are measured from a vertical line through the pivot. The relative angles are measured from the center line of the preceding member. Figure 18 illustrates these angles. Notice that the absolute angle of the hand is the same with the forearm in a different position. The absolute angle of any element is changed only when that element is pivoted.

The Arm

The various parts of the arm correspond to similar parts of the human arm. It has a reach of 42 inches from the shoulder pivot and a load capacity of 50 pounds at the hand, with the hand in any position. The basic dimensions of the arm are shown in Figure 19.

The motors and drives for the pivots are mounted in the shoulder. Power is transmitted to the pivots by roller chains and

TABLE 9

MANIPULATOR SPECIFICATIONS

Element	Case Manip.	PaR 3000
Bridge		
Travel	14.5 feet	These depend on the particular installation.
Velocity	10fpm	
Carriage		
Travel	12 feet	
Velocity	7.5fpm	
Hoist		
Travel	4 feet	
Velocity	8fpm	
(a) Shoulder Rotation		
Travel	720°	Continious
Velocity	1.5rpm	1.5rpm
Shoulder Pivot		
Travel		
Relative	220°	250°
Absolute	220°	250°
Velocity	1.5rpm	2.5rpm
Elbow Pivot		
Travel		
Relative	270°	270°
Absolute	370°	360°
Velocity	1.5rpm	2.5rpm
Wrist Pivot		
Travel		
Relative	280°	310°
Absolute	540°	610°
Velocity	1.5rpm	2.5rpm

(a) The PaR 3000 shoulder rotation is in the plane of attachment to its supporting structure. In the Case Manipulator the supporting structure (Hoist) rotates, thus rotating the shoulder.

TABLE 9 (Continued)

Element	Case Manip.	PaR 3000
(b) Hand Rotation		
Travel	Continious	Continious
Velocity	50rpm	7rpm
(b) Grip		
Opening	4 in	4 in
Velocity	120ipm	20ipm

(b) These elements are not considered in the control algorithims currently being developed, nor are they under computer control at the time of this writing. However; both items are contemplated for the future.

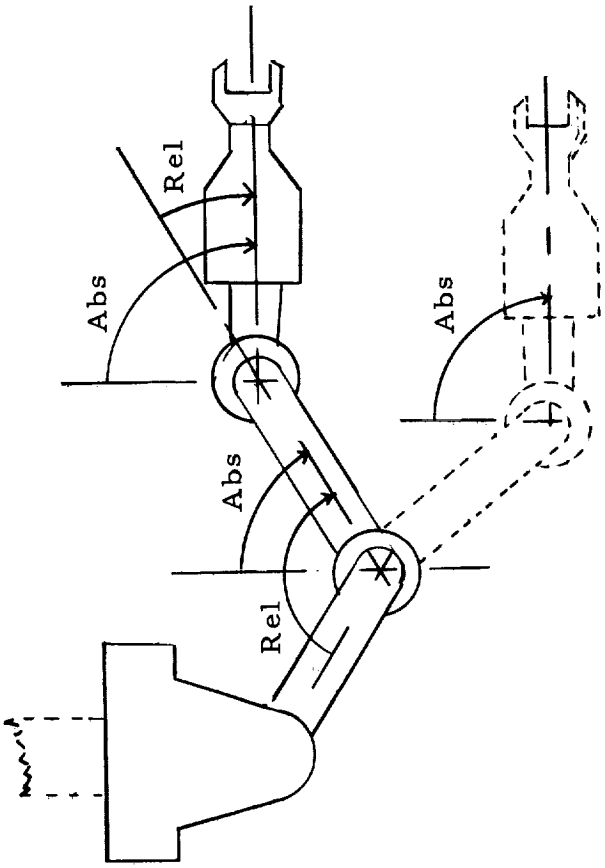


Figure 18 Absolute and Relative Angles

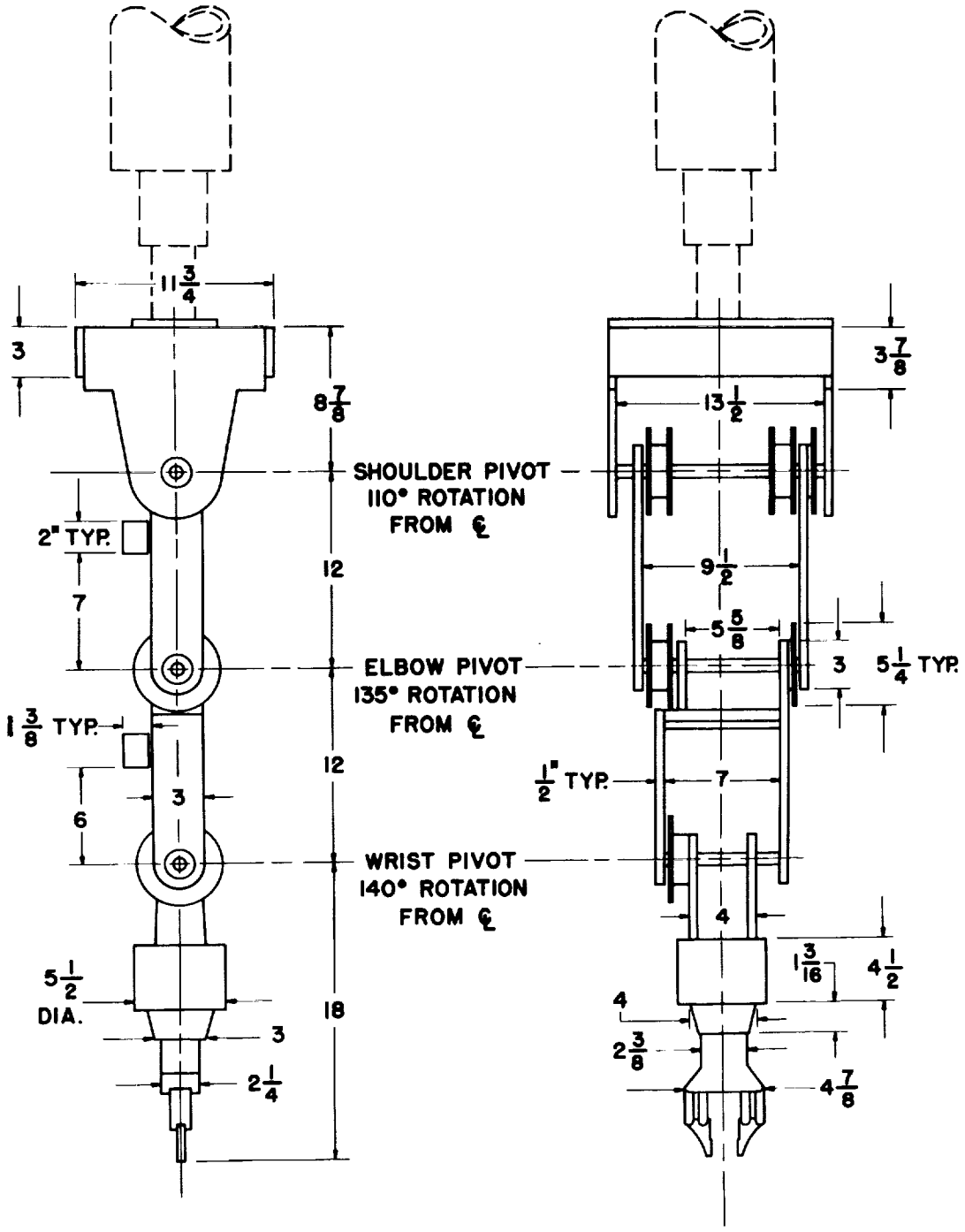


Figure 19 Arm Dimensions

sprockets mounted on the arm. Back-lash is held to a minimum by pre-loading the chain with chain tighteners. When properly pre-loaded the maximum tension in any chain, under full load, is less than 600 pounds. The chain is 1/2" pitch American Standard 40 and has an ultimate yield strength of 3700 pounds. This provides a nominal factor of safety of 6 to 1, to take into account shock loads and occasional overloads.

The motors are interlocked by limit switches on the pivots to prevent the maximum pivot angles from being exceeded.

The feedback potentiometers for the pivots are also mounted in the shoulder. They are coupled to the drive by PIC[5] timing belts and gears so that they measure the absolute pivot angles.

Figure 20 shows the mounting of some of the components in the shoulder. The umbilical cord carries the wiring for the elbow and wrist limit switches and the power to the hand motors. Power to the shoulder is via a cable through the center of the hoist.

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[5] PIC Design Corporation, Subsidiary of Benrus Watch Company, Inc., East Rockaway, Long Island, New York.

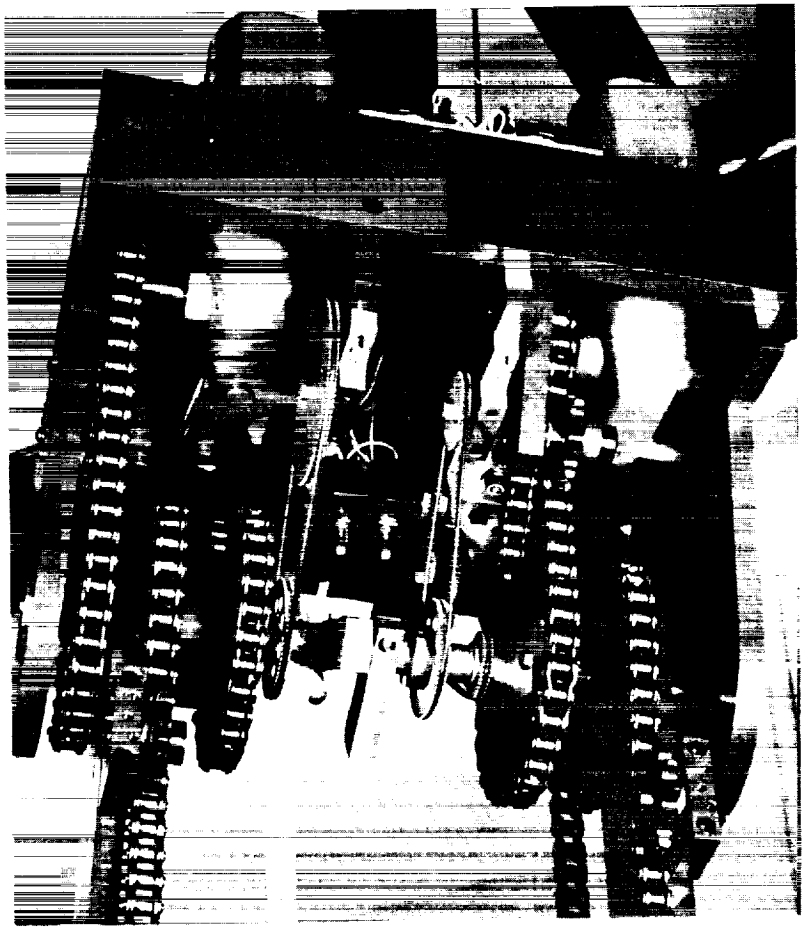


Figure 20 Shoulder

Hoist Drive

The original hoist motor on the Model 100 was a repulsion motor which was not compatible with the motor controls in the servo system. Accordingly it and its associated gear head were replaced with an assembly consisting of a universal motor and a chain reduction drive. The universal motor provided the desired compatability and the chain drive simplified the installation,

APPENDIX I

GPI Logic Diagrams

Standard Computer Control Company logic and notation is used for the General Purpose Interface to provide compatability with the DDP 116 computer. Signals are identified by a five-character alphanumeric mnemonic, followed by a sign, and occasionally by a letter to denote one of a series of lines with the same signal. The sign is plus (+) for a true (-6v) signal and minus (-) for a negated (0v) signal. Table 10 summarizes the notation used.

Bracketed numbers appearing next to the signal mnemonics indicate the drawing that shows the origin of the signal. If the origin number for a signal is absent on a particular drawing, one of the following assumptions may usually be made:

(1) The signal appears elsewhere on the drawing with an origin number.

(2) The signal originates on the drawing.

(3) The signal belongs to a class of signals whose origin is indicated elsewhere on the drawing.

TABLE 10

LOGIC NOTATION

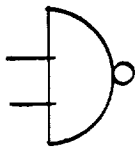
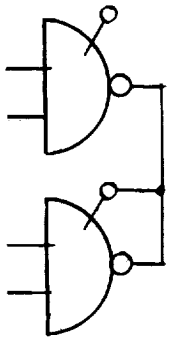
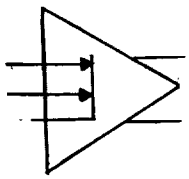
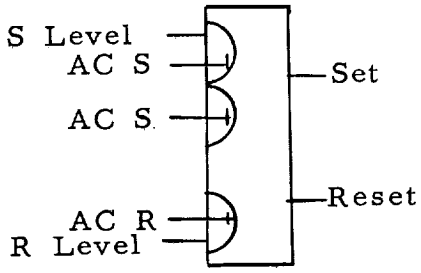
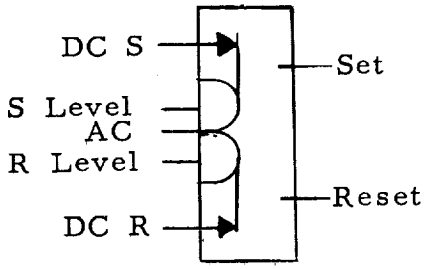
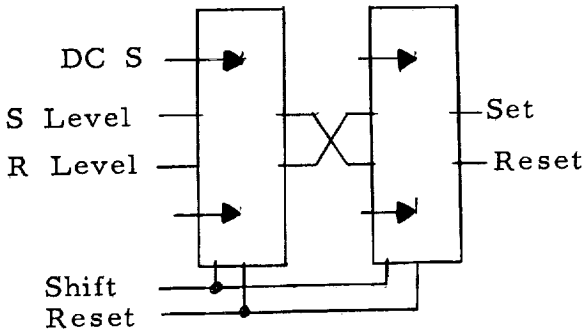
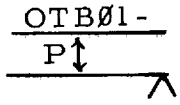
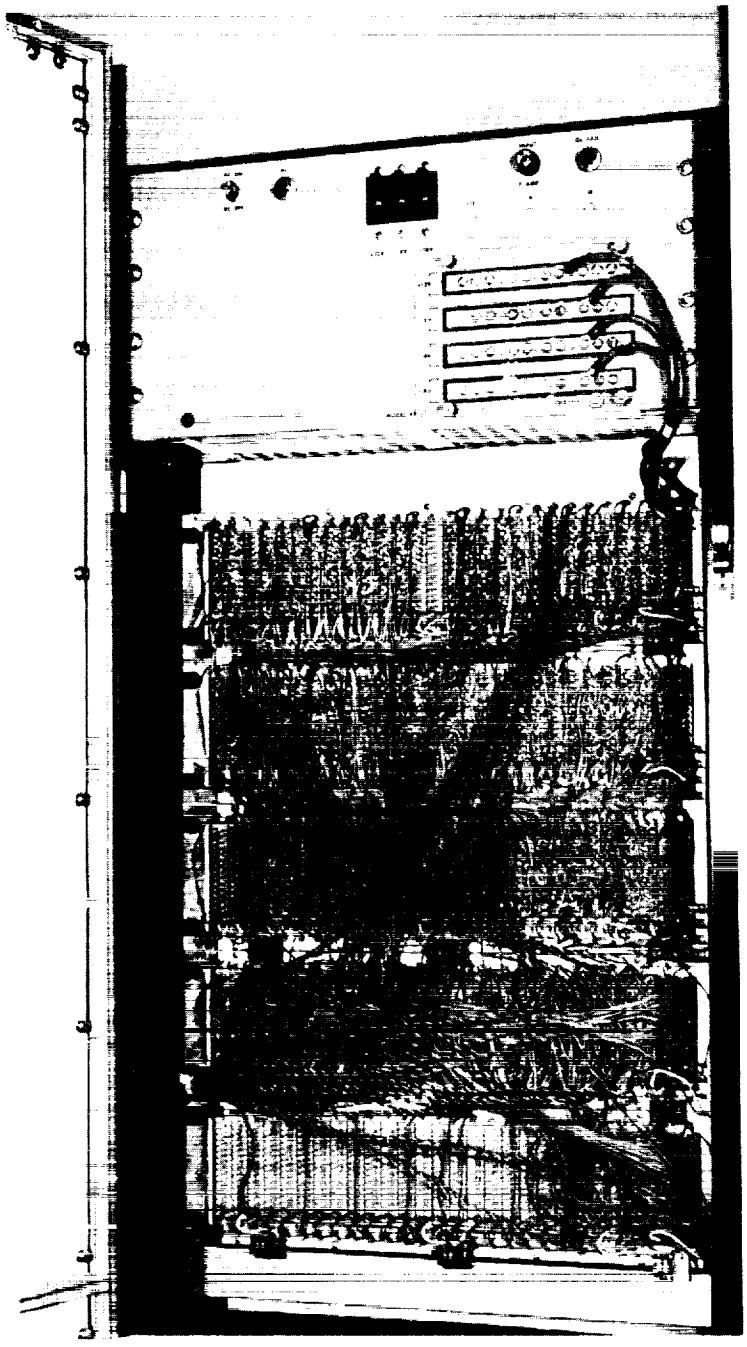
Symbol	Use
	Nand Gate.
	Nand Gate with diode cluster for expanding inputs.
	Nand Gate with seperate load circuits for paralleling outputs. The paralleled outputs perform an AND operation for ones (-6v), and an OR operation for zeros (0v).
	Non-inverting Power Amplifier.

TABLE 10 (Continued)

Symbol	Use
	Gated Flip-Flop
	Multipurpose Flip-Flop
	Shift Register
	Primary Computer Line (I/O Bus). The symbol ∧ indicates the ground return of the twisted pair.

The logic cards for the General Purpose Interface are located in racks G and H of the third computer bay. Figure 21 shows the location of the racks, and Figure 22 the placement of the cards in the racks. The logic drawings are shown in Figures 23 through 37.



Rack G

Rack H

Figure 21 Rack Location

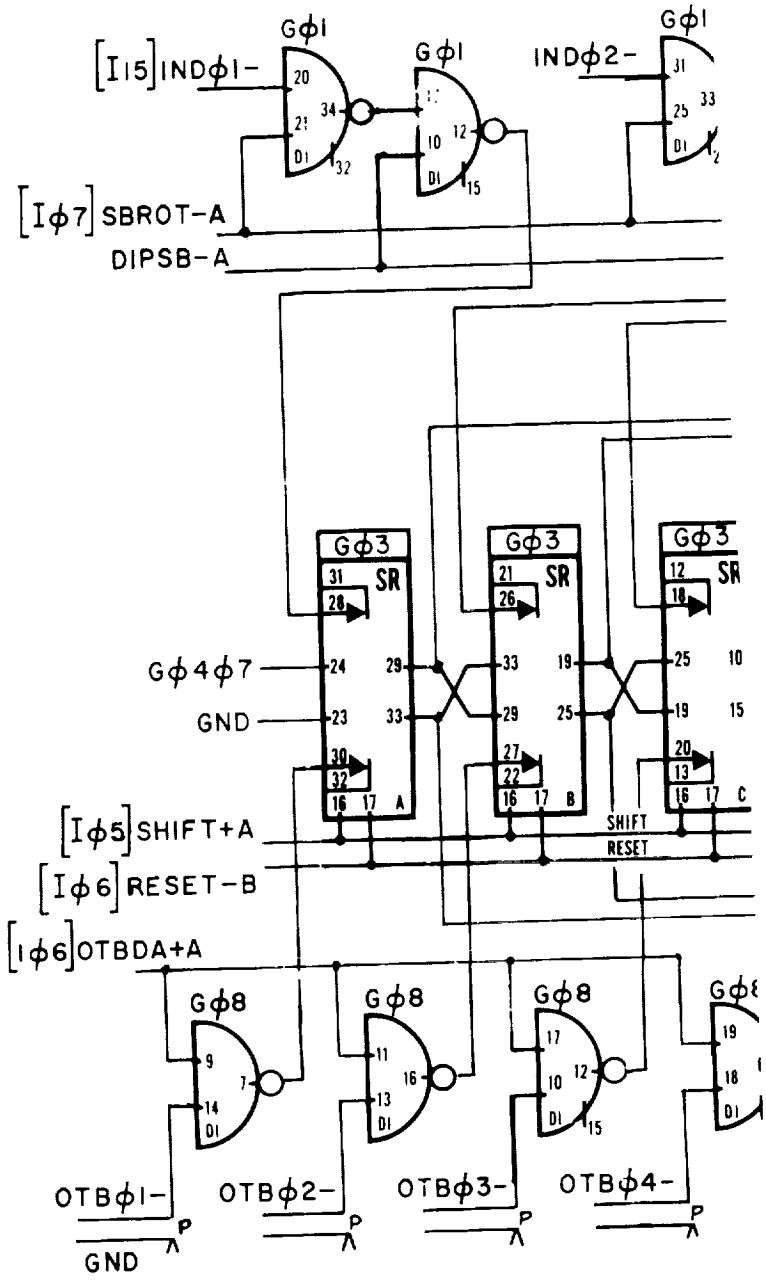
Rack G

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
DI30	PN30	SR30	DJ30	DI30	PN30	SR30	DI30	DI30	PN30	DI30	DI30	DJ30	DI30	PN30	SR30	DI30	PN30	SR30	DJ30	DI30	FA30	DI30	DC30	DI30	DC30	DI30	CONN
Buffer and Gating Bits 1 to 8								Set and Reset Control		Buffer and Gating Bits 9 to 16									DMC. Mask. Ready.		Address and Function Code						

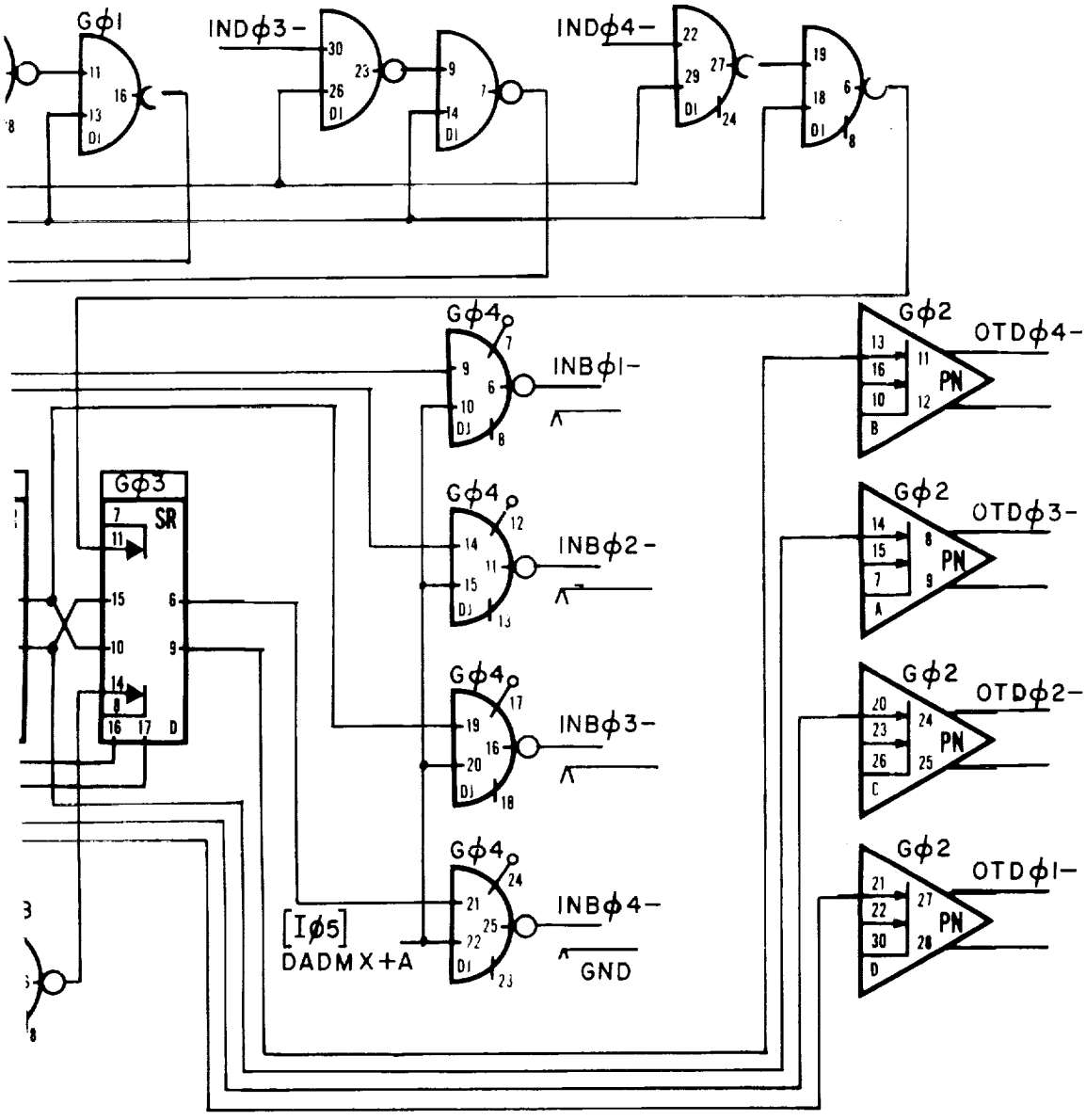
Rack H

1	19	20	21	22	23	24	25	26	27	28
EMPTY		PN30	PN30	DI30	DJ30	DJ30	DI30	DI30	PN30	CONN
				Mode		SKS		OCP		

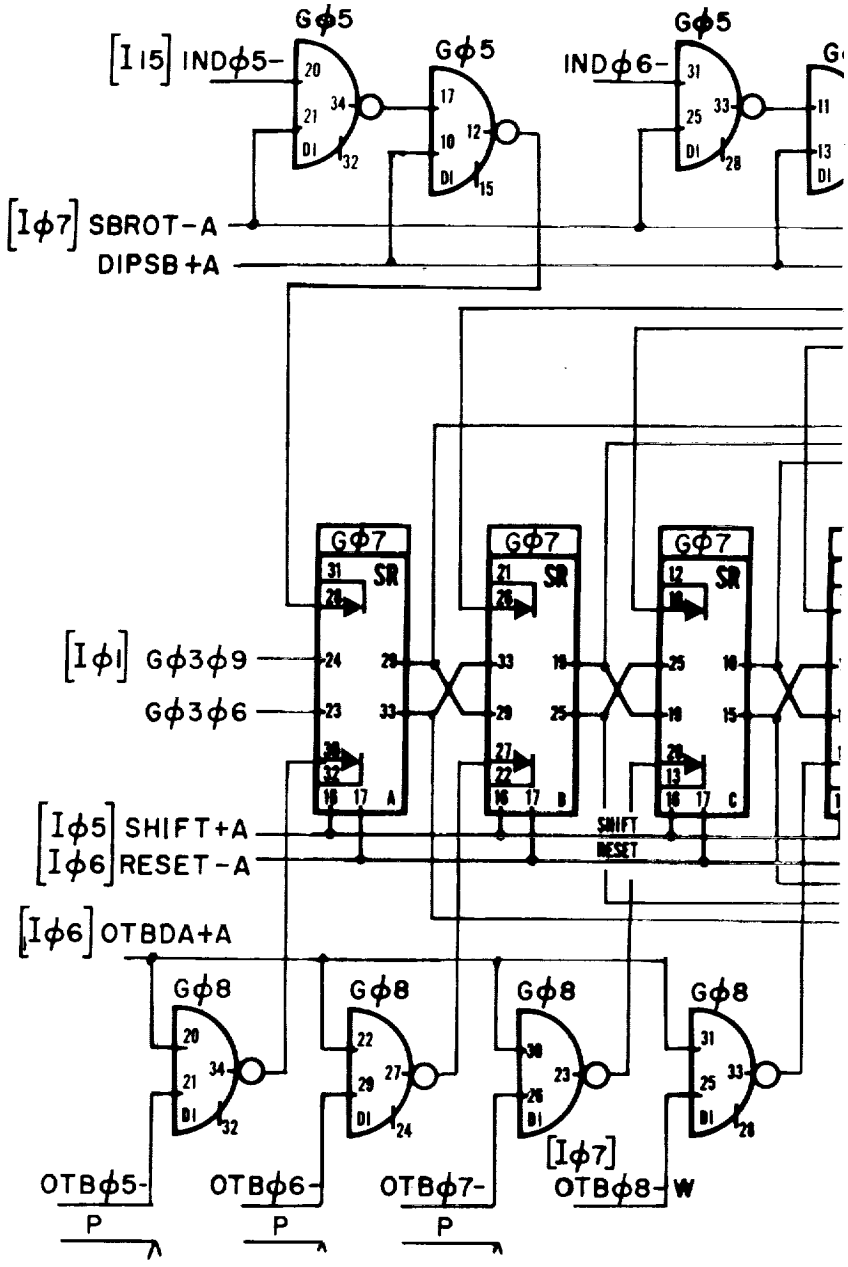
Figure 22 GPI Card Placement



DWG. Iφ1 BUFFER A

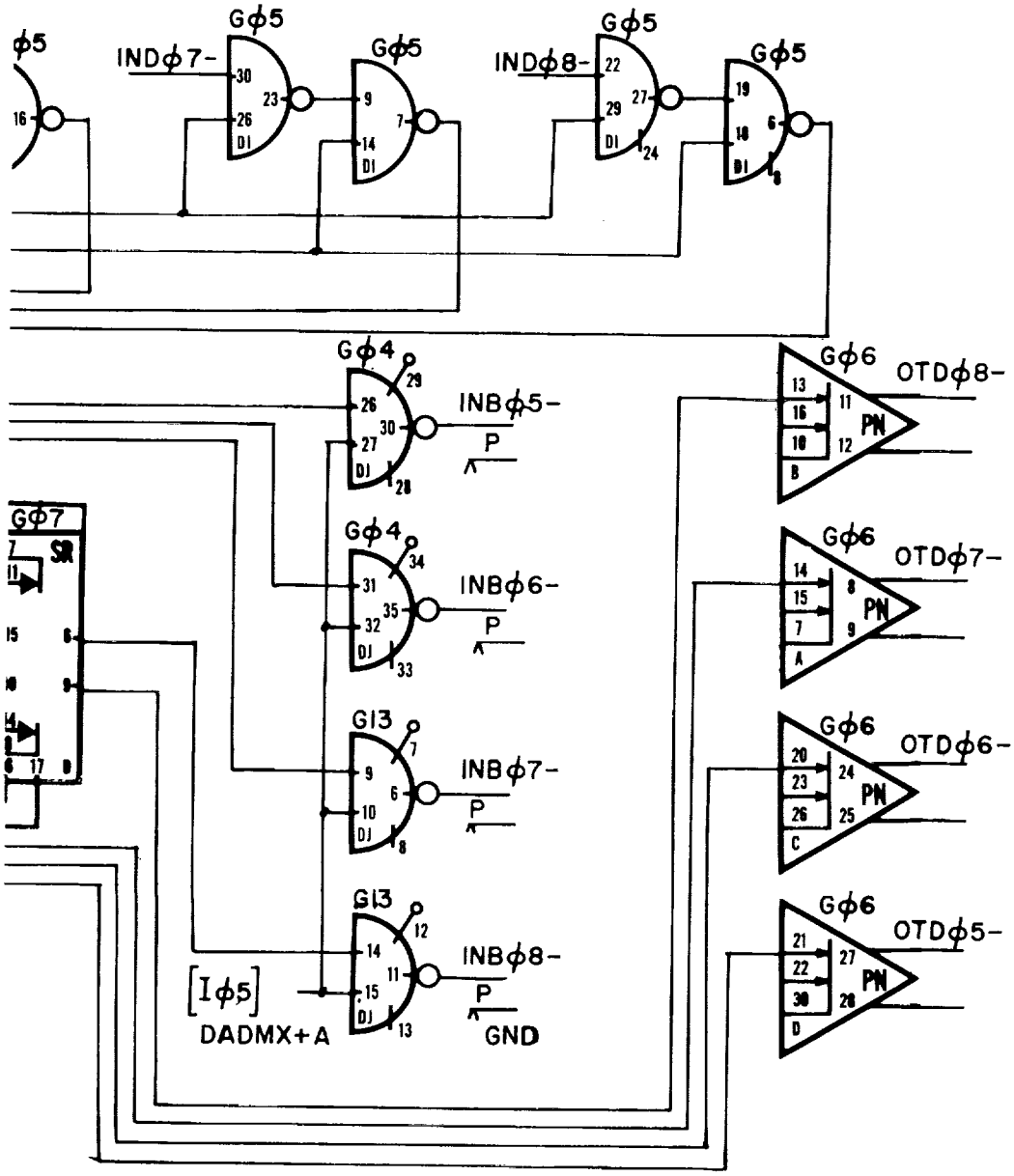


.ND GATING BITS 1 TO 4.
Figure 23

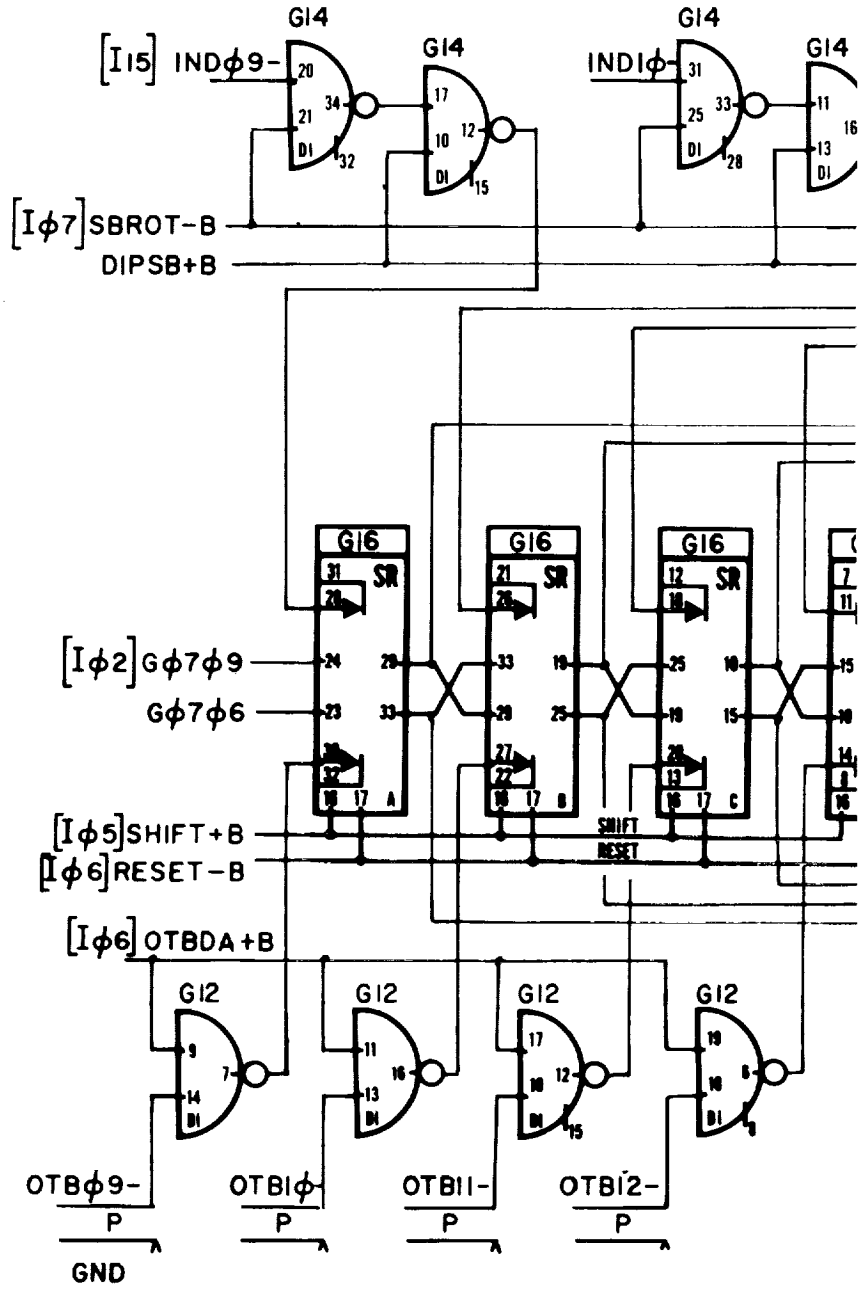


DWG Iϕ2 BUFFER AND GA

Figure

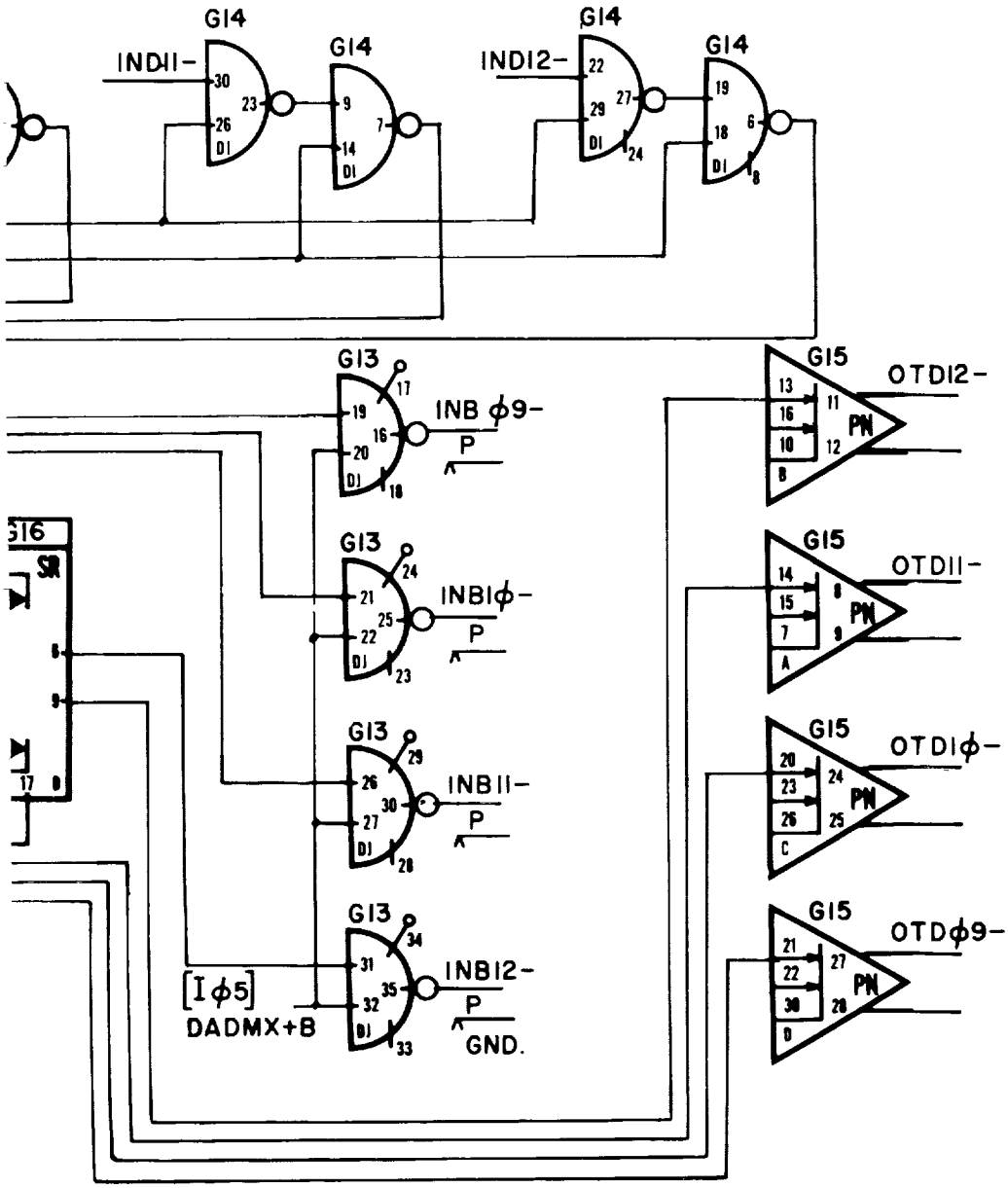


TING BITS 5 TO 8



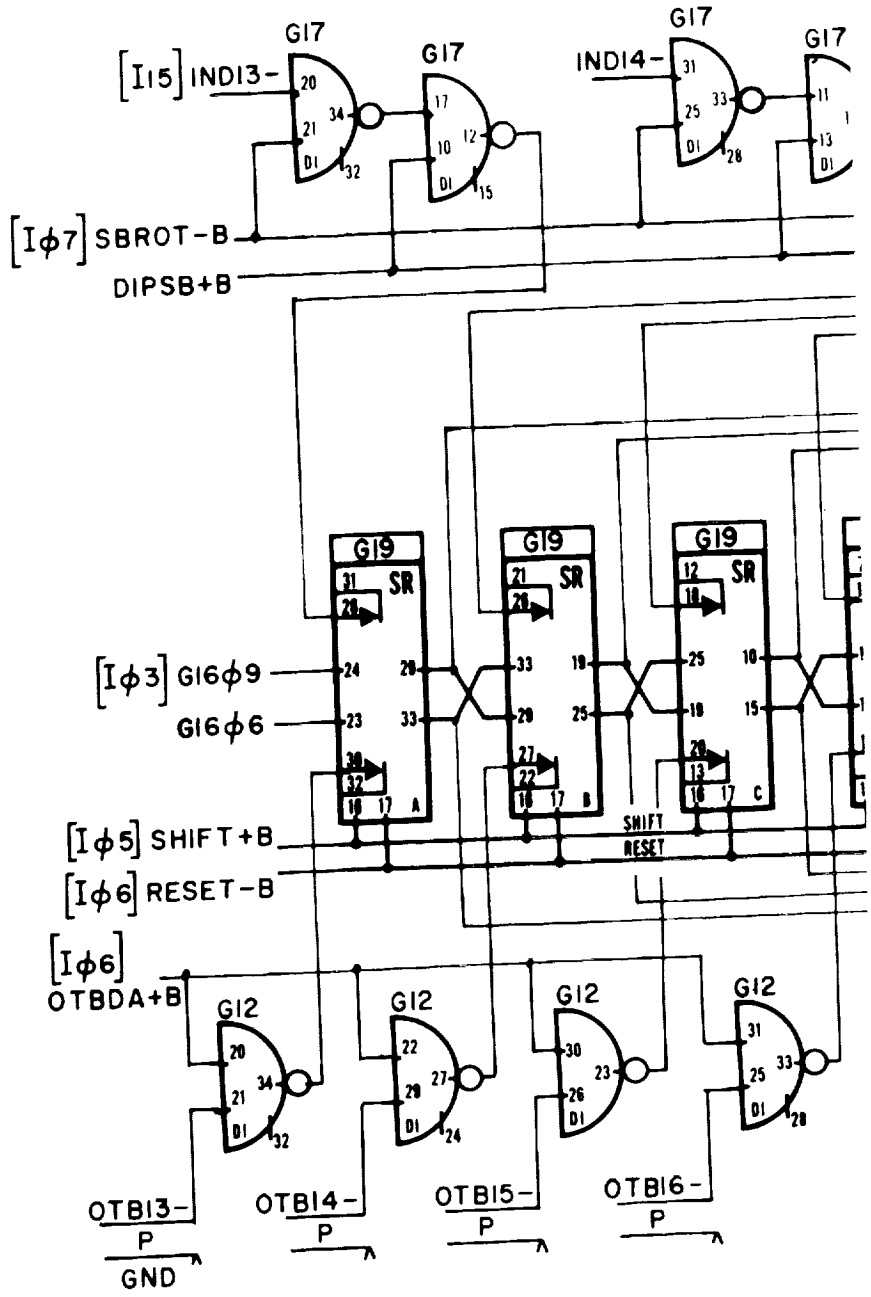
DWG. Iϕ3 BUFFER AND GATI

Figure



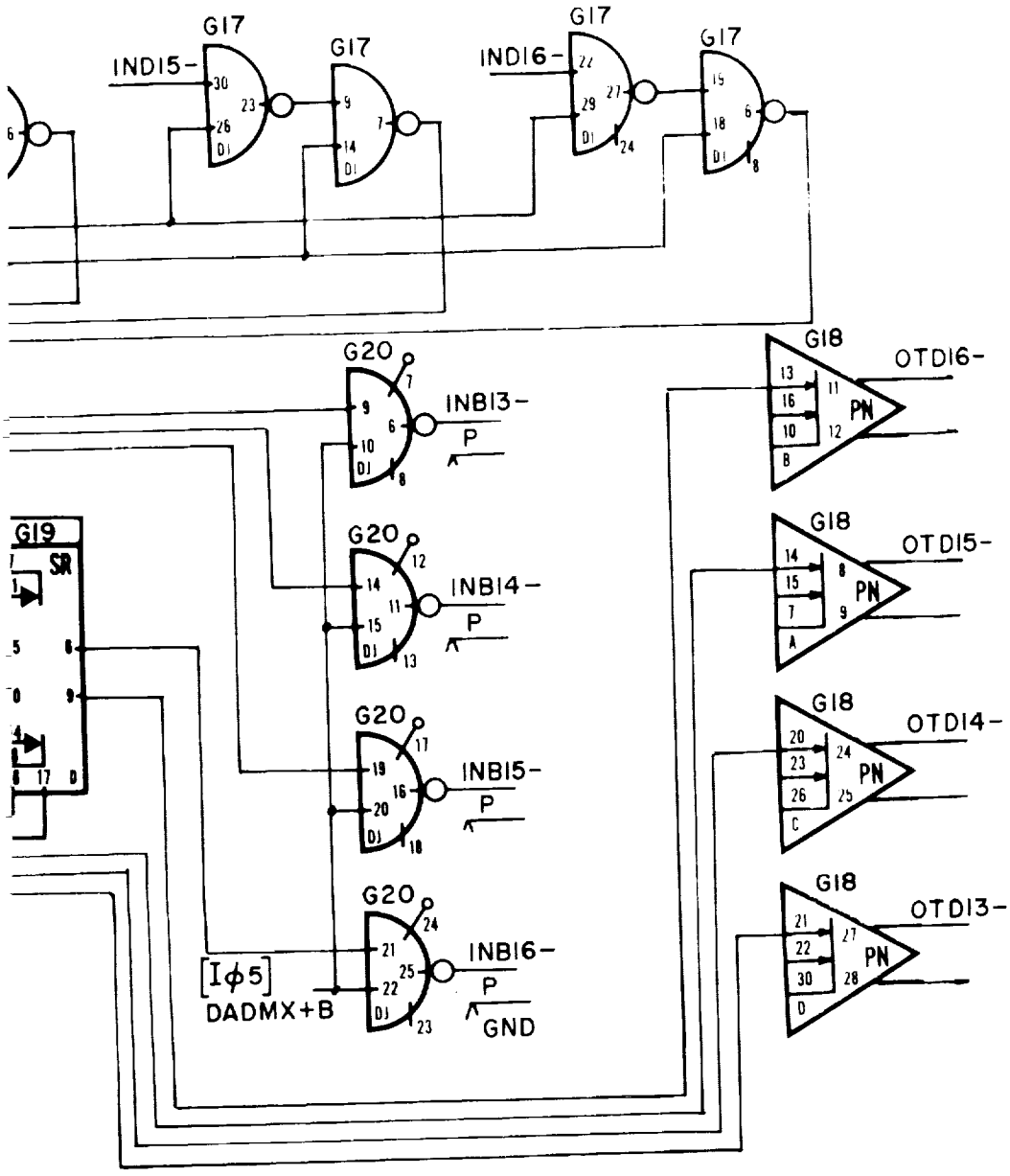
ING BITS 9 TO 12

25



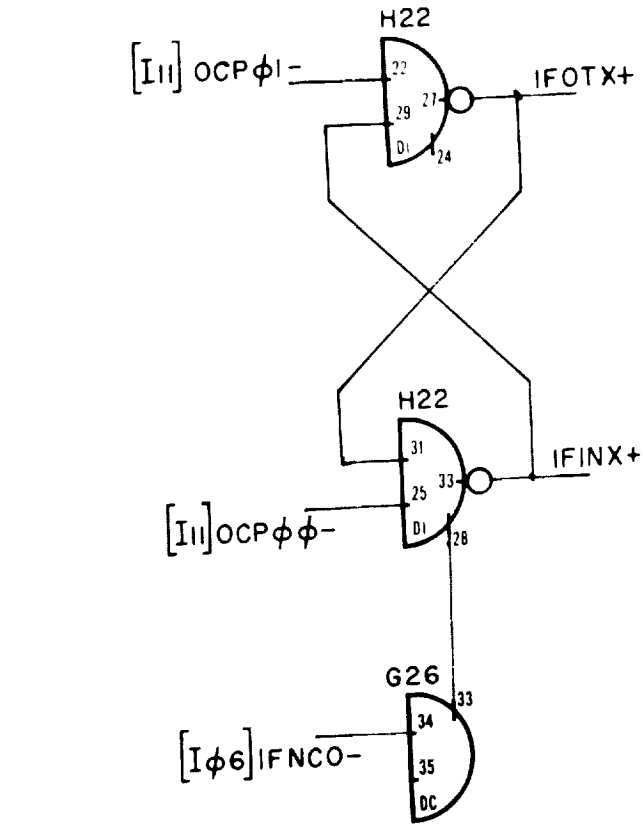
DWG. Iφ4 BUFFER AND GA

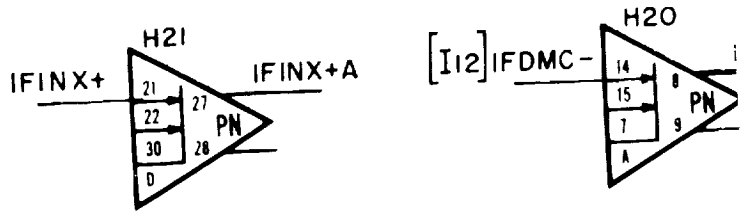
Figure



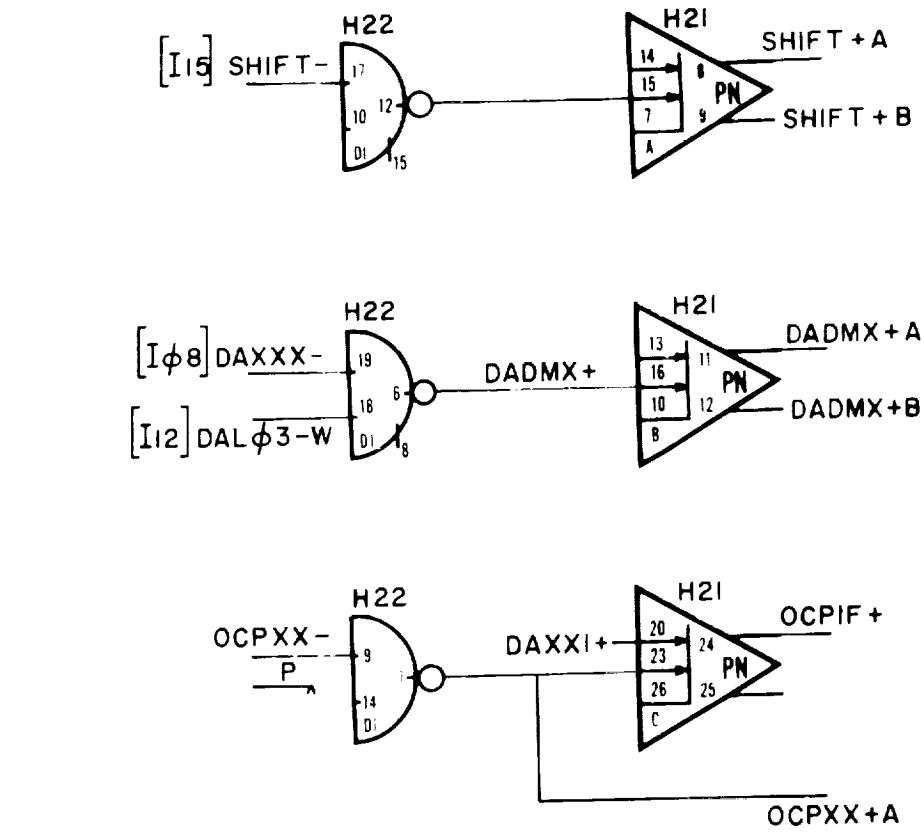
TING BITS 13 TO 16

: 26


H22
[I11] OCPϕ1-
22
29
D1
27
24
IFOTX+
H22
31
25
D1
33
28
IFINX+
[I11]OCPϕϕ-
G26
34
35
DC
33
[Iϕ6]IFNCO-

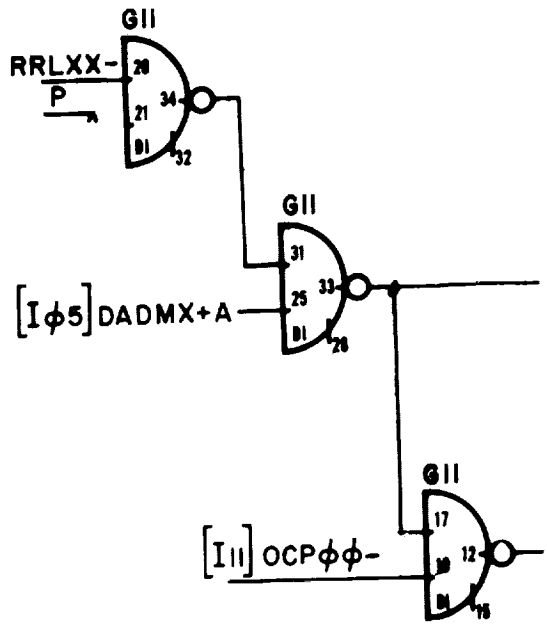

H21
IFINX+
21
22
30
D
27
28
PN
IFINX+A
[I12]IFDMC-
H20
14
15
7
A
8
9
PN

DWG Iϕ5



MODE (I/O) CONTROL

Figure27

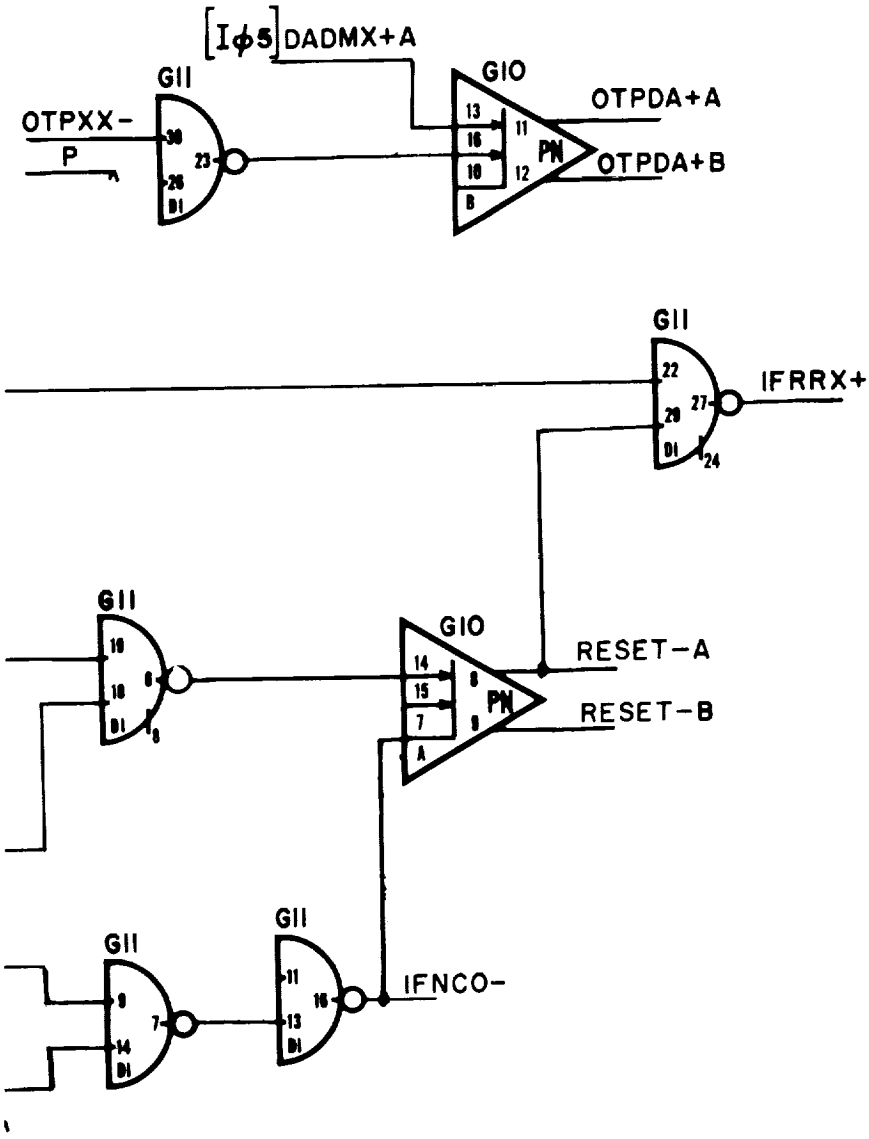


[Iϕ5]IFINX+

NCOXX-
P

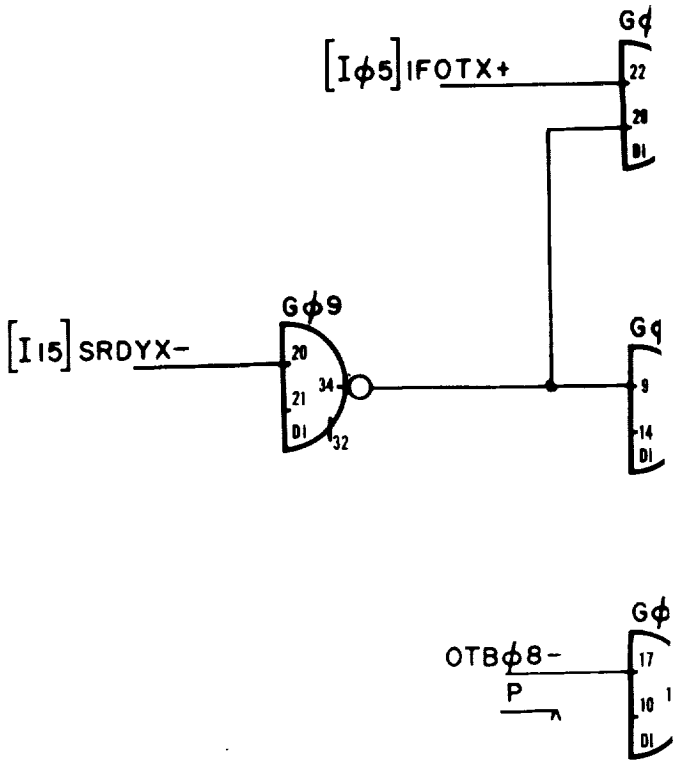
MSTRCLR-
P

DWG. Iϕ6

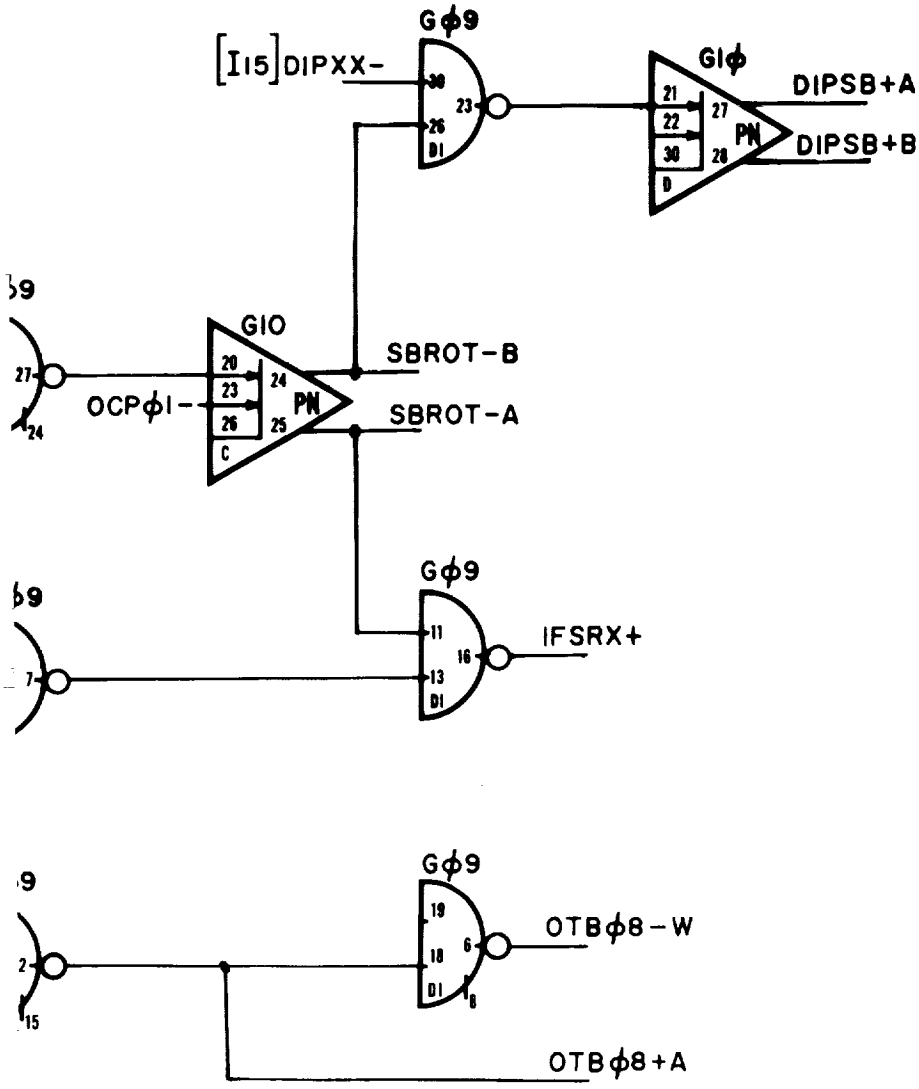


RESET CONTROL

Figure 28

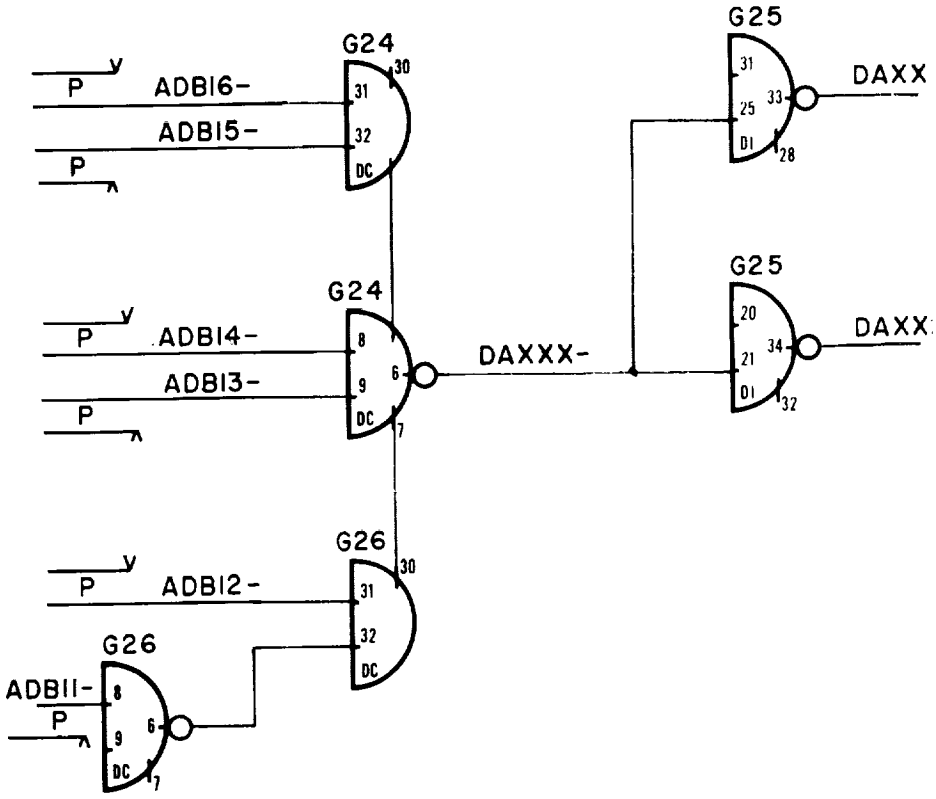

[Iϕ5]IFOTX+
Gϕ
22
20
DI
[I15]SRDYX-
Gϕ9
20
21
DI
34
32
Gϕ
9
14
DI
OTBϕ8-
P
Gϕ
17
10
DI
1

DWG. Iϕ7



SET CONTROL

Figure 29



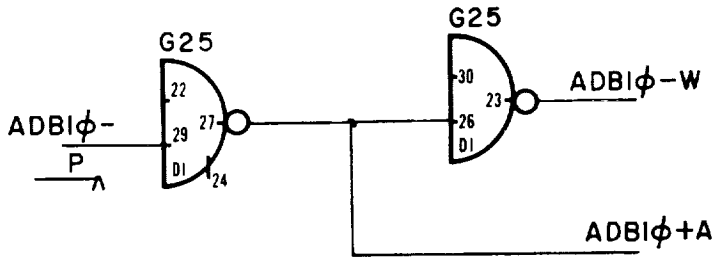
DWG. Iϕ8

ADDI

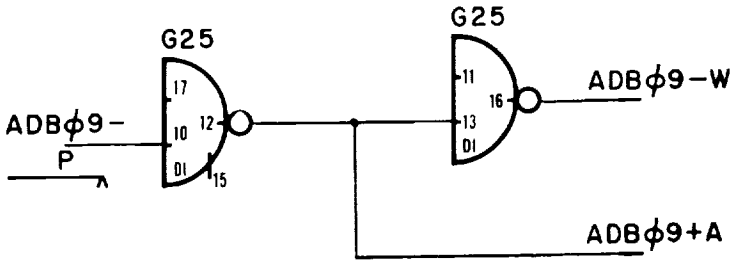
Fi

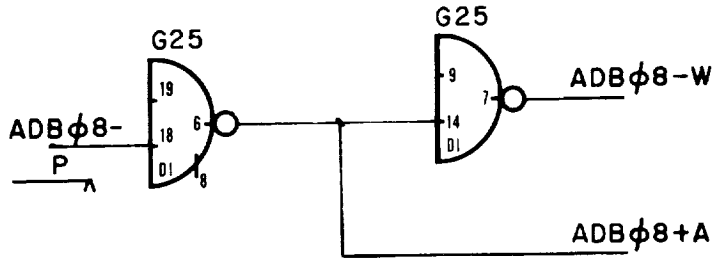
68

1+



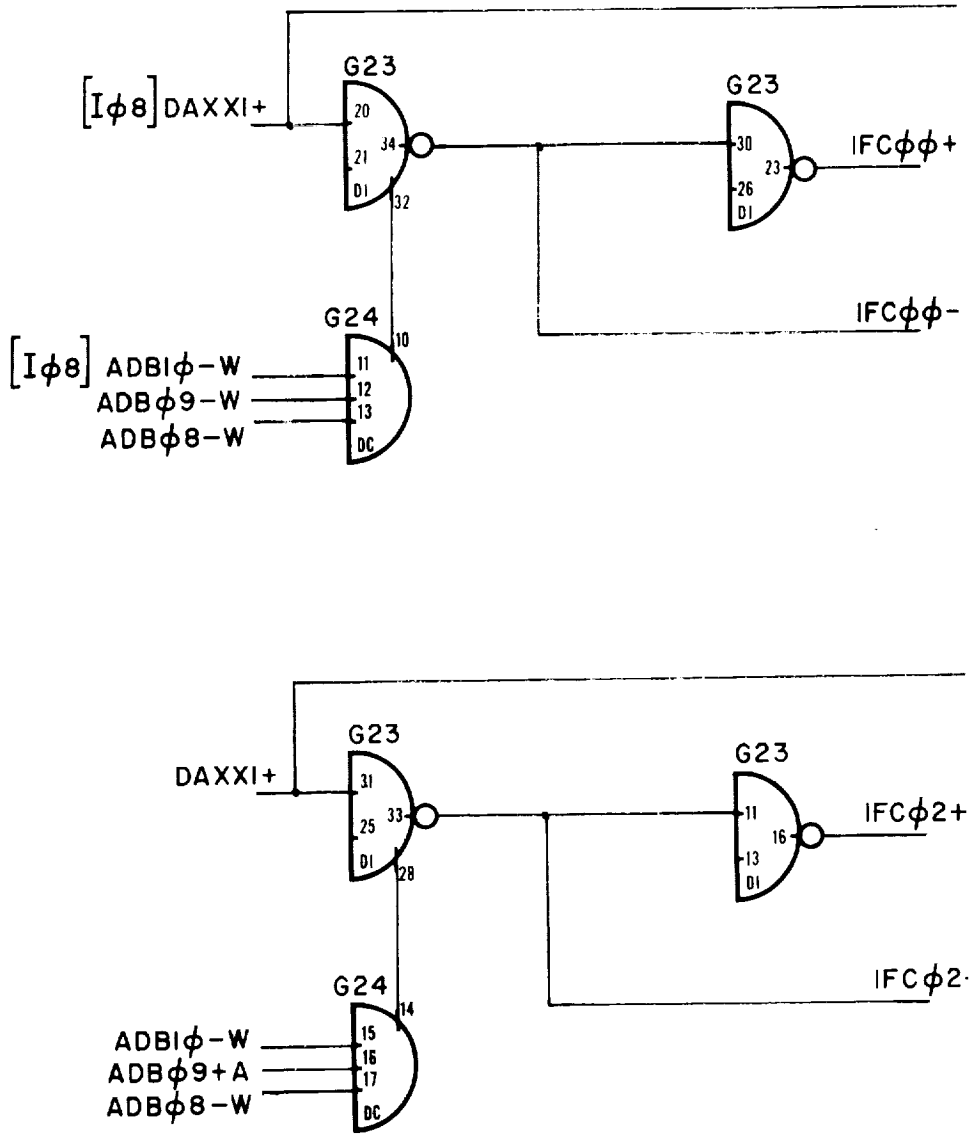
2+





RESS DECODING

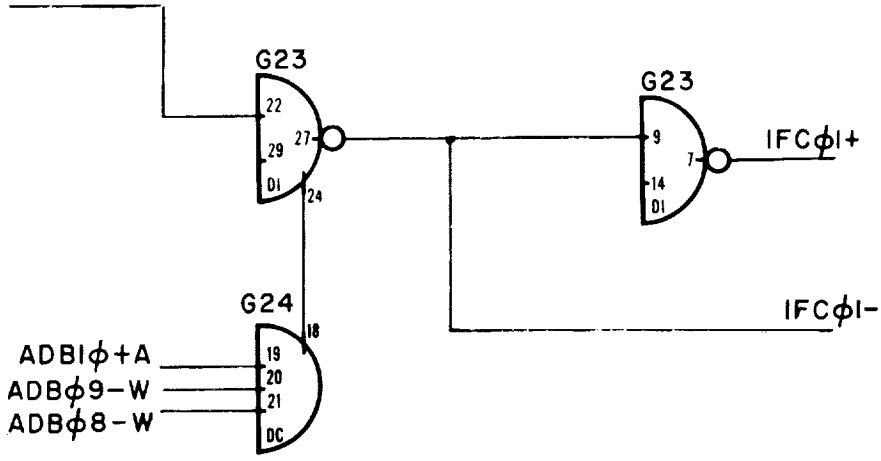
gure 30

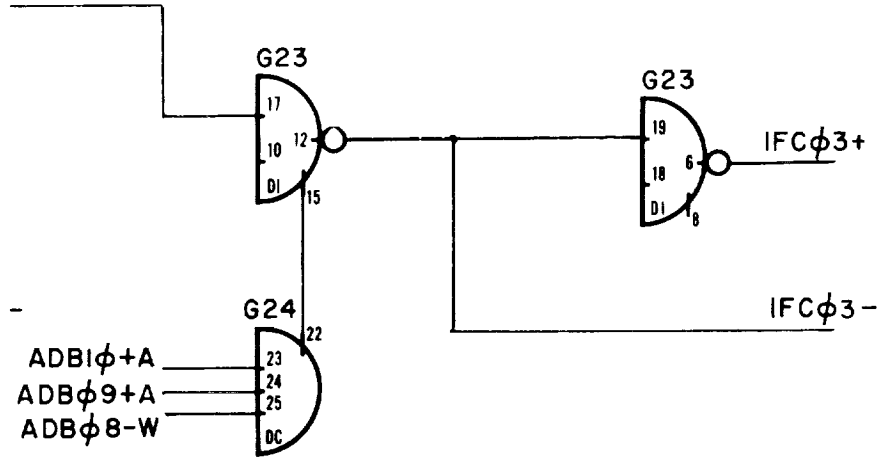


DWG. Iϕ9 FUNCTION CODE GENERAT

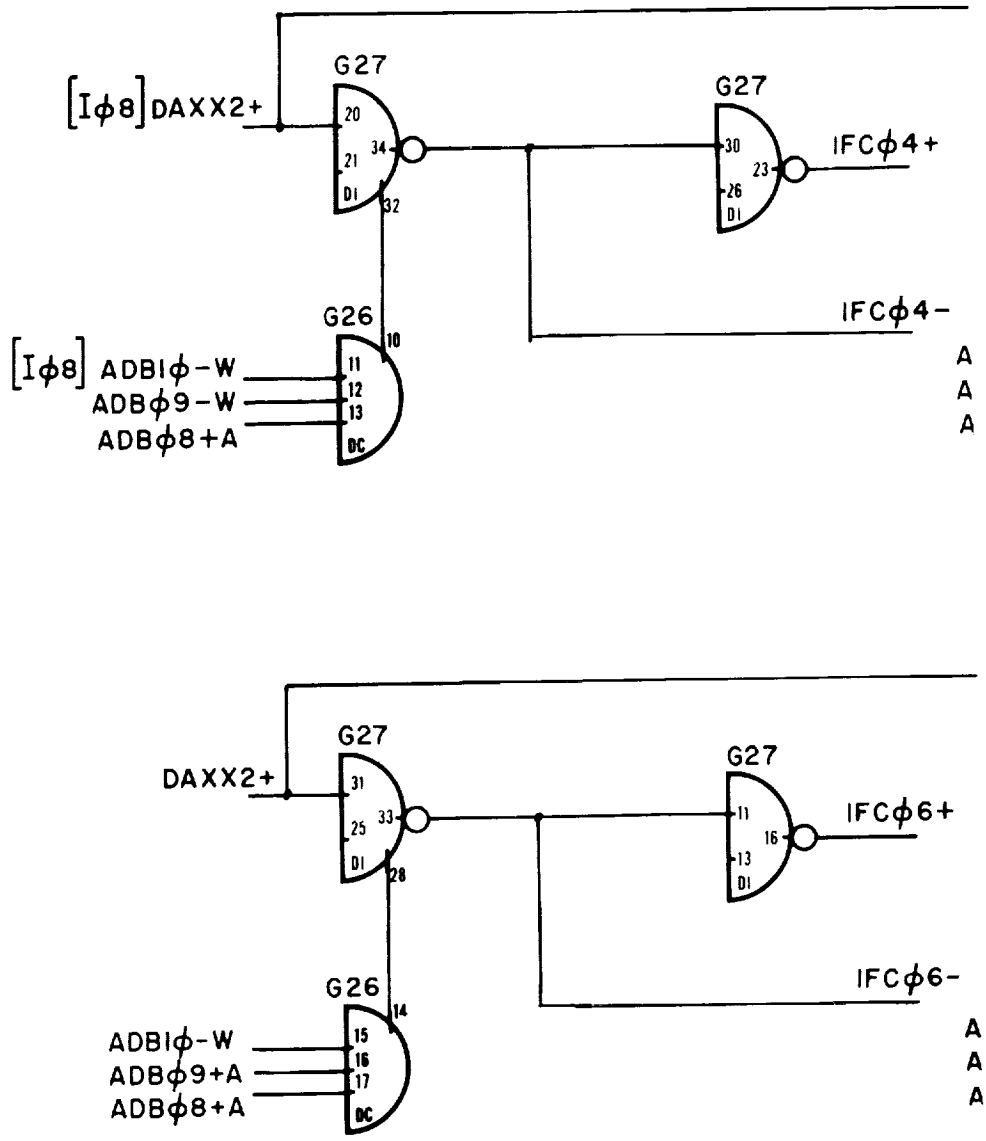
Figure 31

31-1





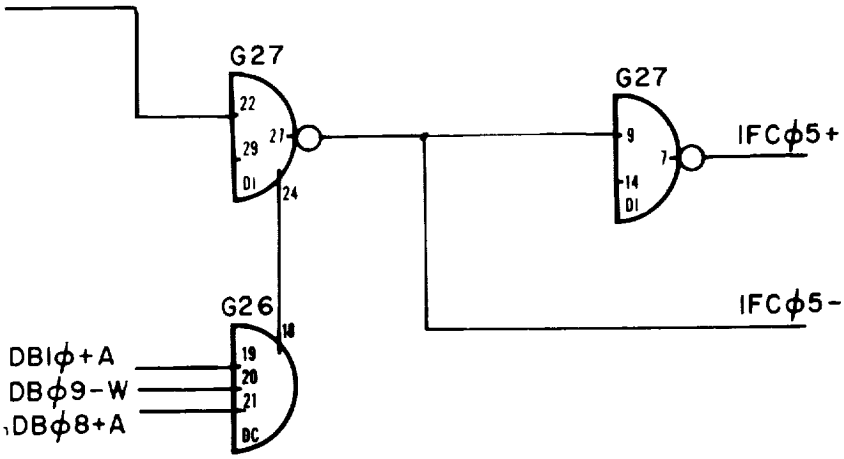
TION IFCϕϕ-ϕ3

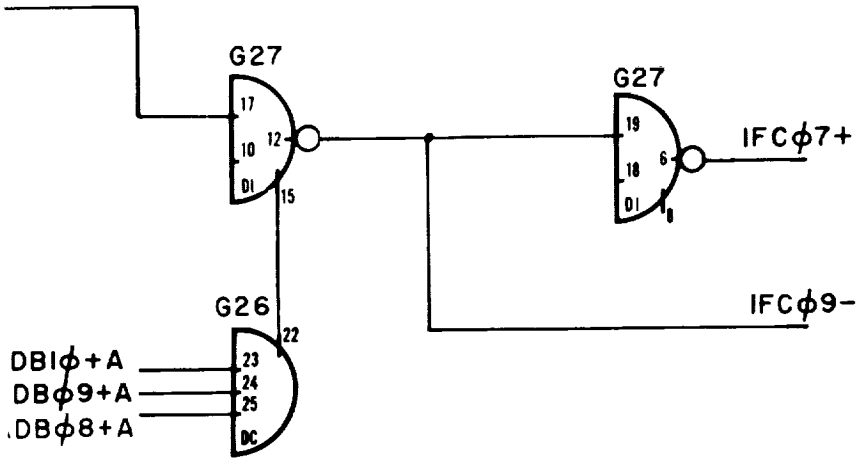


DWG. Iiφ FUNCTION CODE GENER

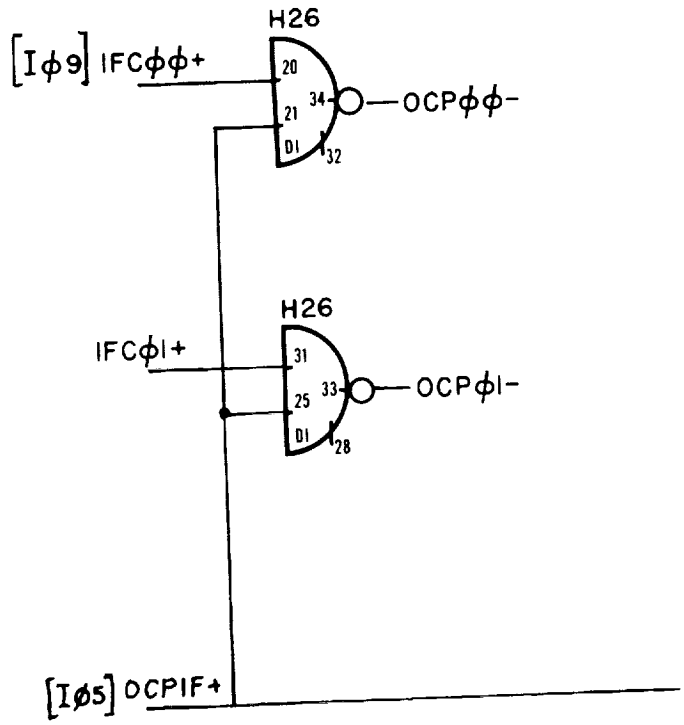
Figure 32

32-1





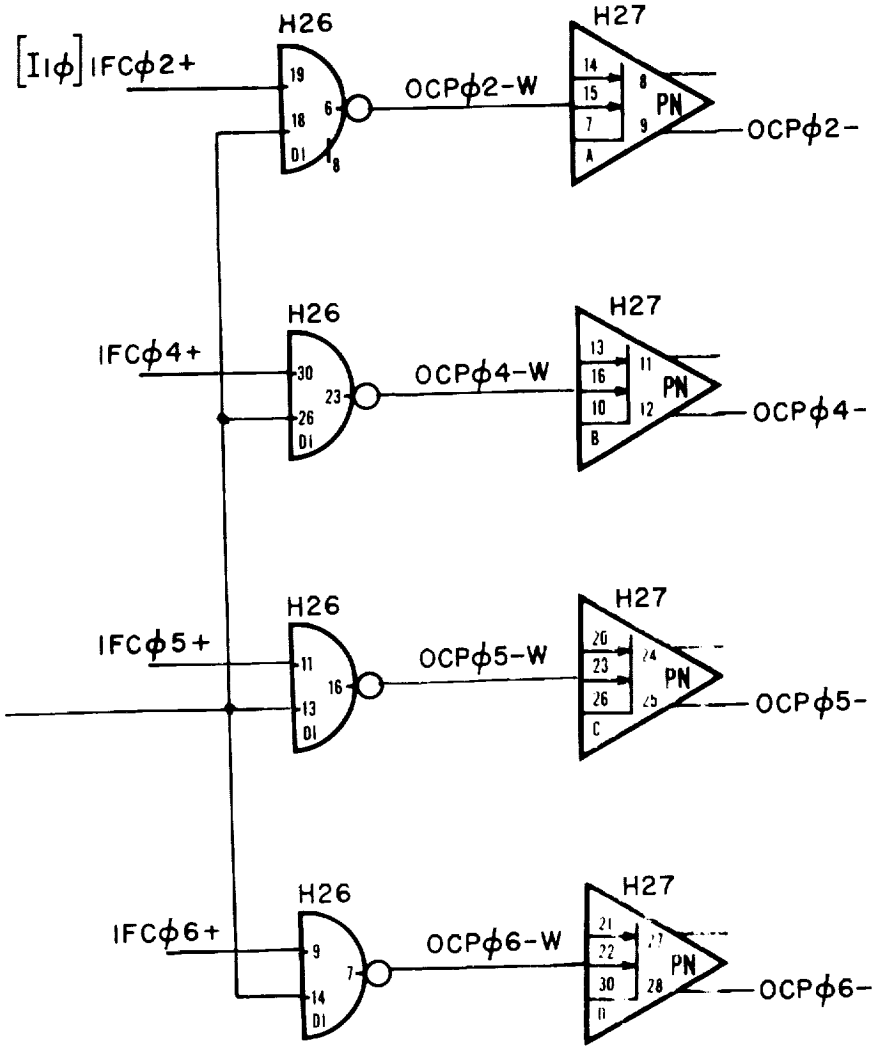
ATION IFCϕ4-ϕ7


H26
[Iϕ9] IFCϕϕ+
20
21
D1
34
32
OCPϕϕ-
H26
IFCϕ1+
31
25
D1
33
28
OCPϕ1-
[Iø5] OCPIF+

DWG. III

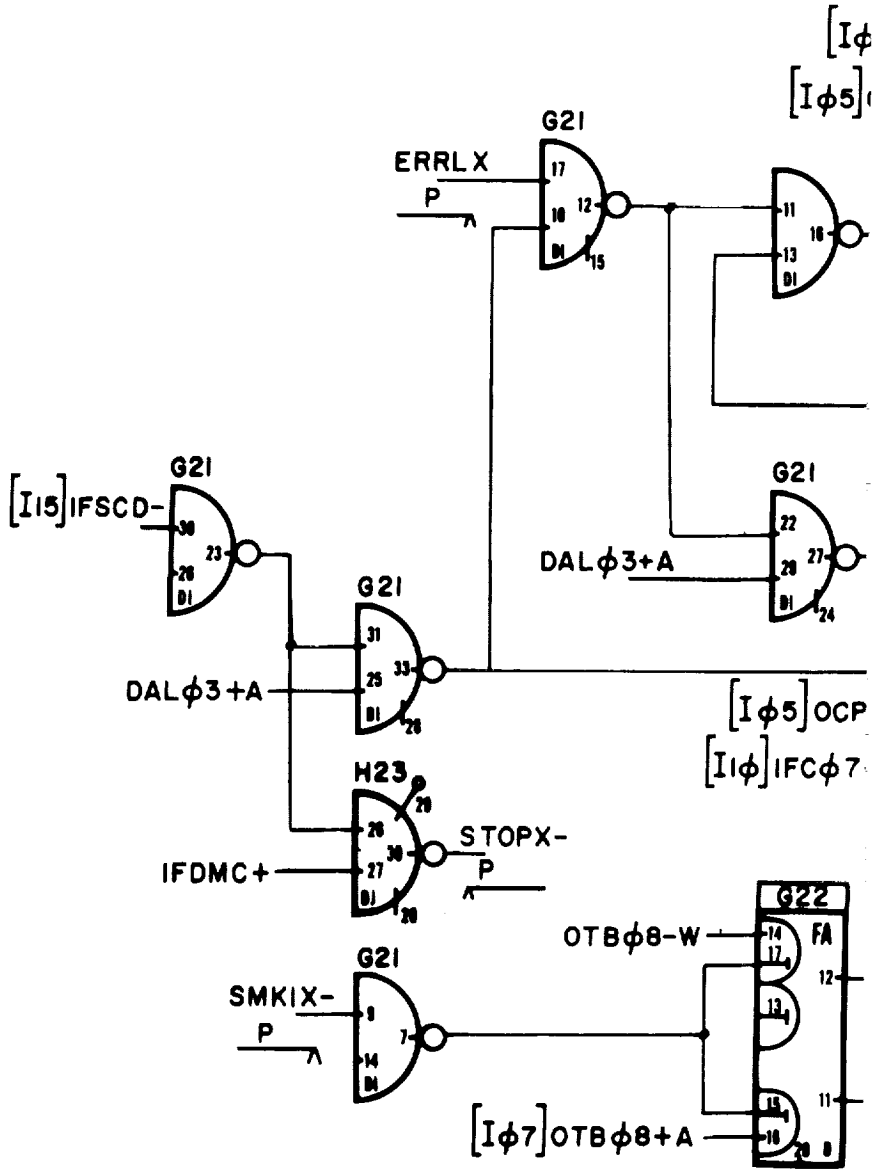
OCP (

]



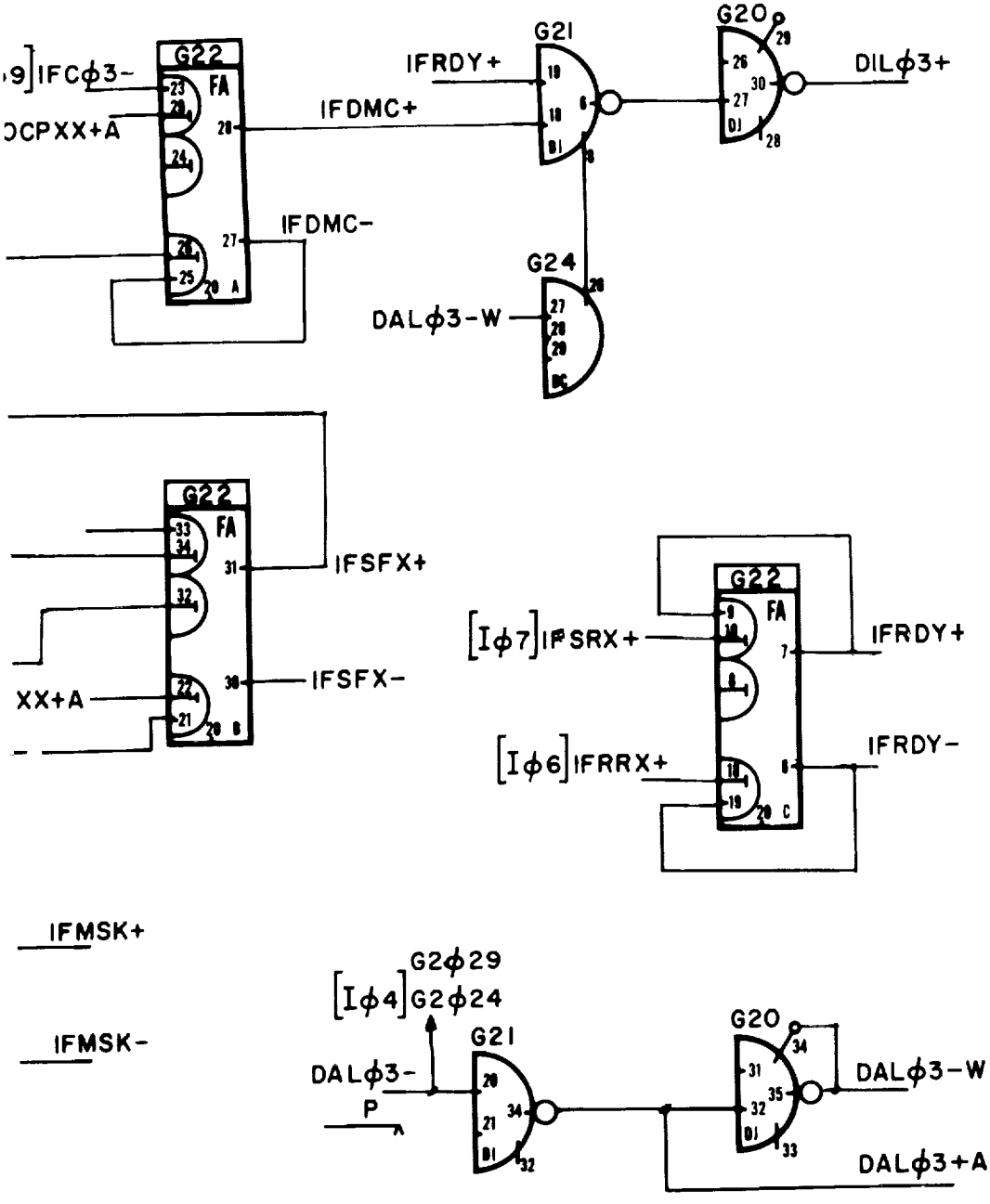
GENERATION

Figure 33



DWG. I12 DMC. MASK AN

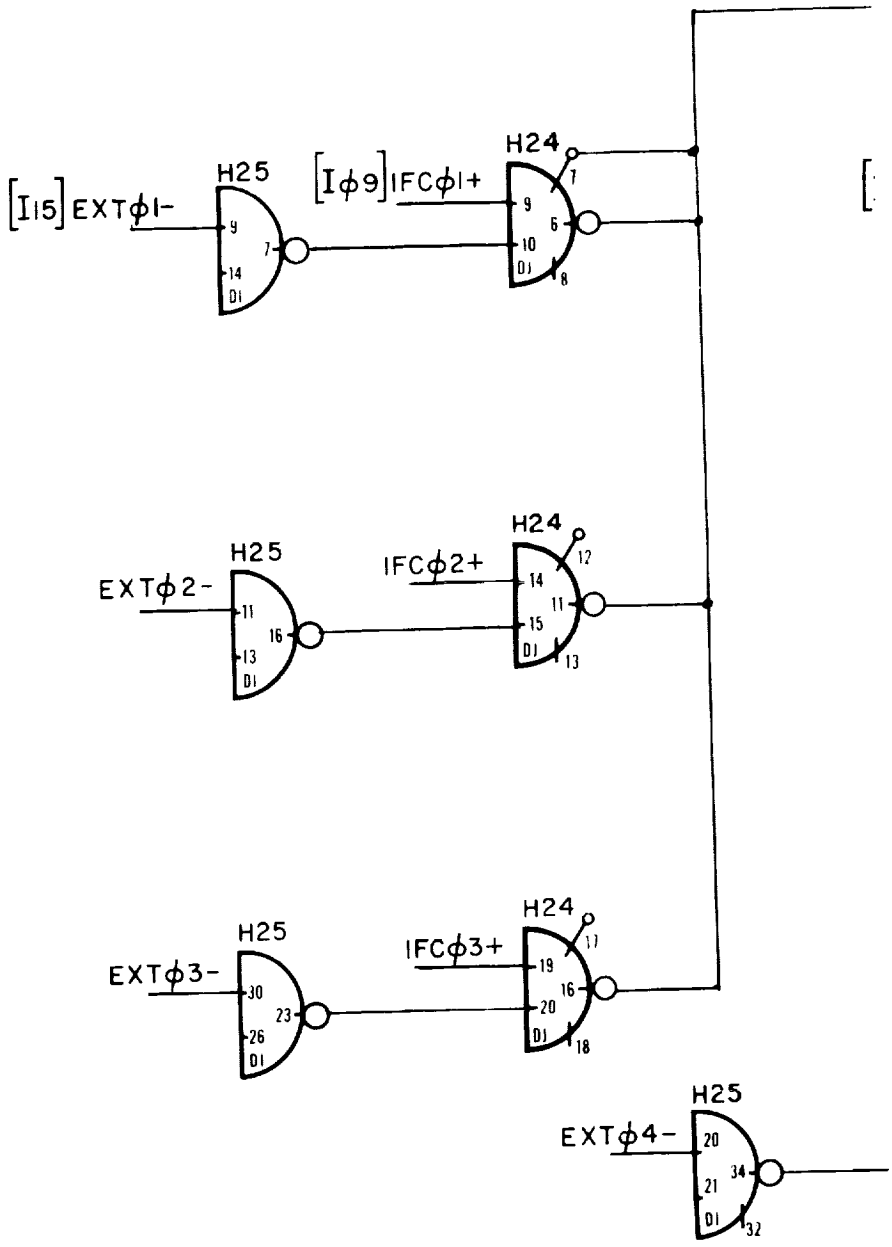
Fig



D READY CONTROL

ure 34

34-2

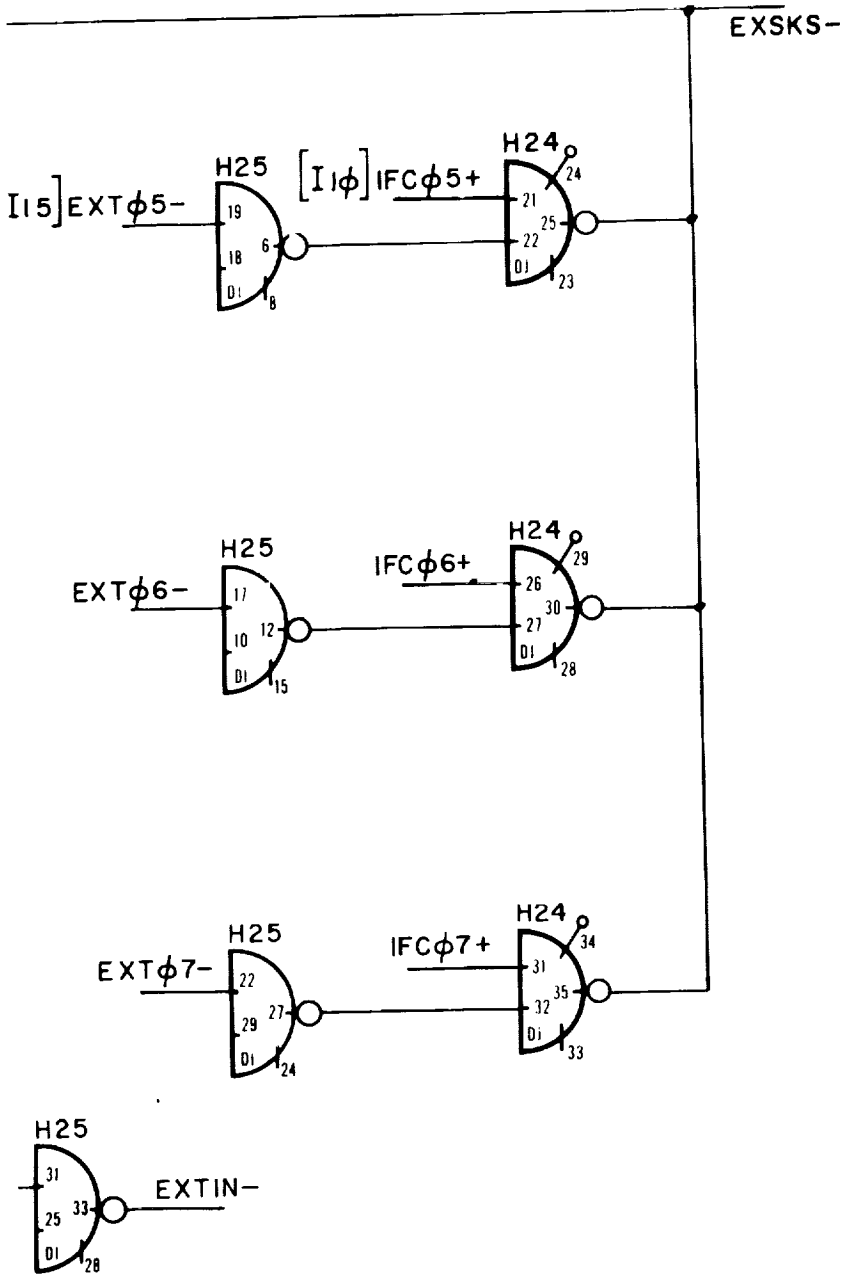


DWG. I13

EXTERNAL SKS GATING

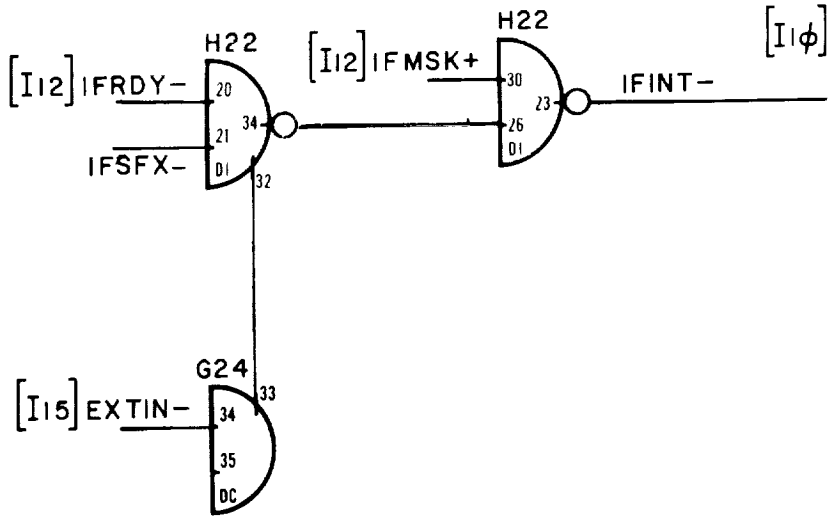
Figure 35

35-1


EXSKS-
H25
I15]EXTϕ5-
19
18
D1
6
8
[I1ϕ]IFCϕ5+
H24
21
22
D1
24
25
23
H25
EXTϕ6-
17
10
D1
12
15
IFCϕ6+
H24
26
27
D1
29
30
28
H25
EXTϕ7-
22
29
D1
27
24
IFCϕ7+
H24
31
32
Di
34
35
33
H25
31
25
D1
33
28
EXTIN-

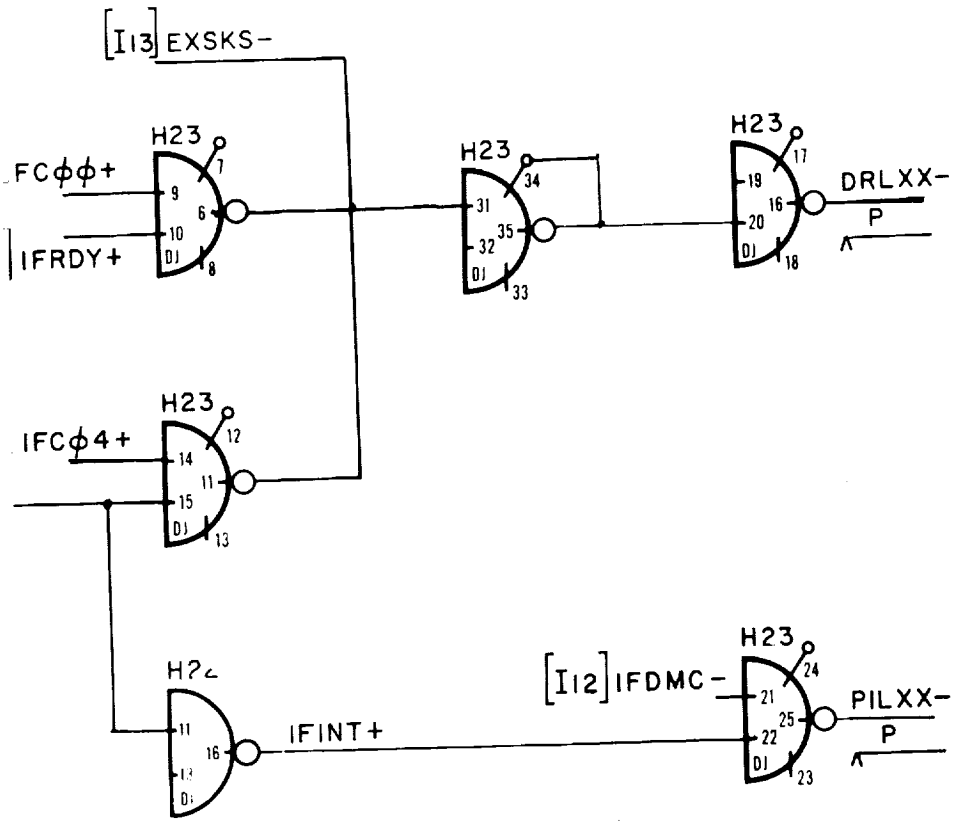
[Iφ9]

[I12]



DWG. I14

SKS A



ND INTERRUPT GATING

Figure 36

36-e

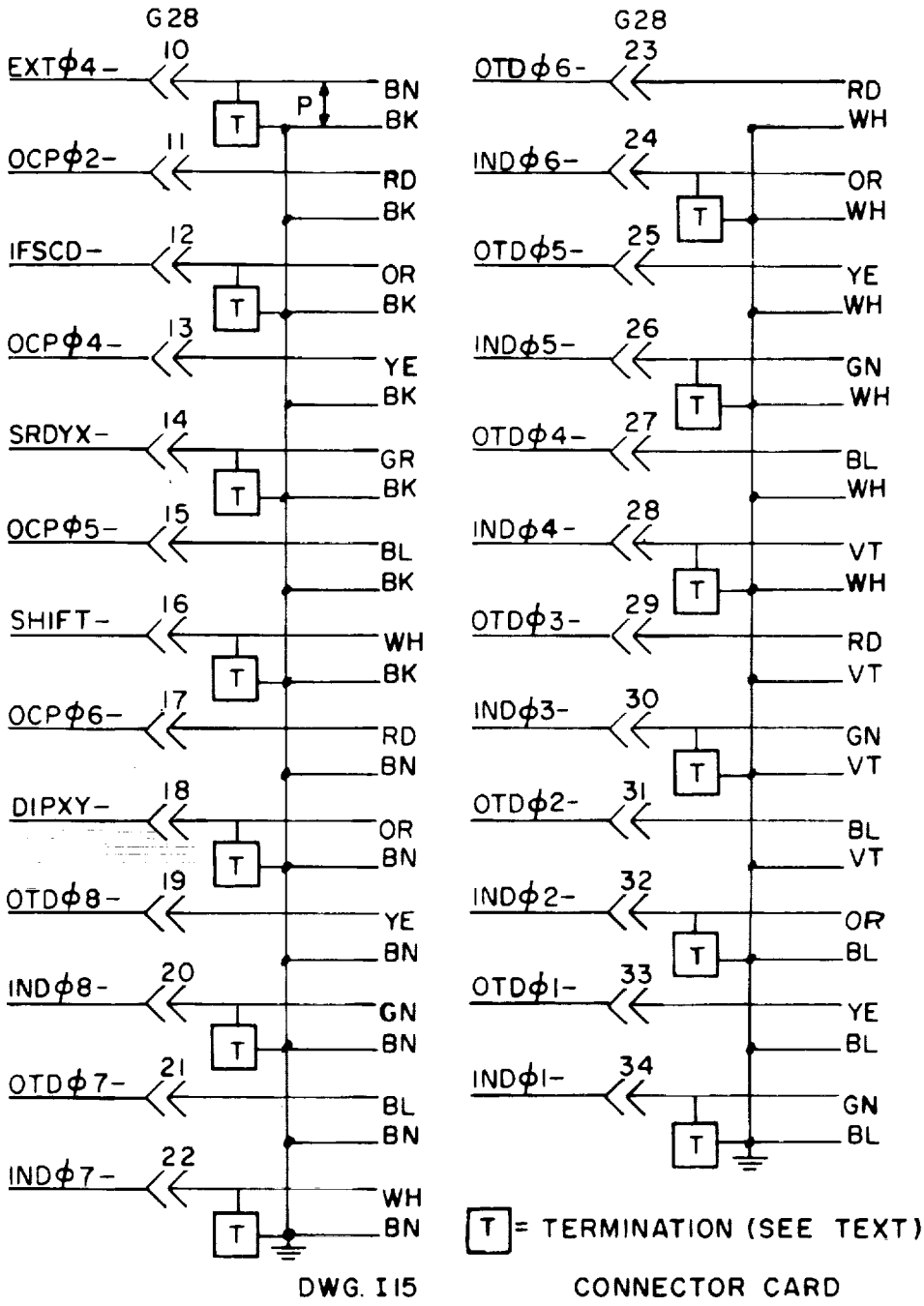
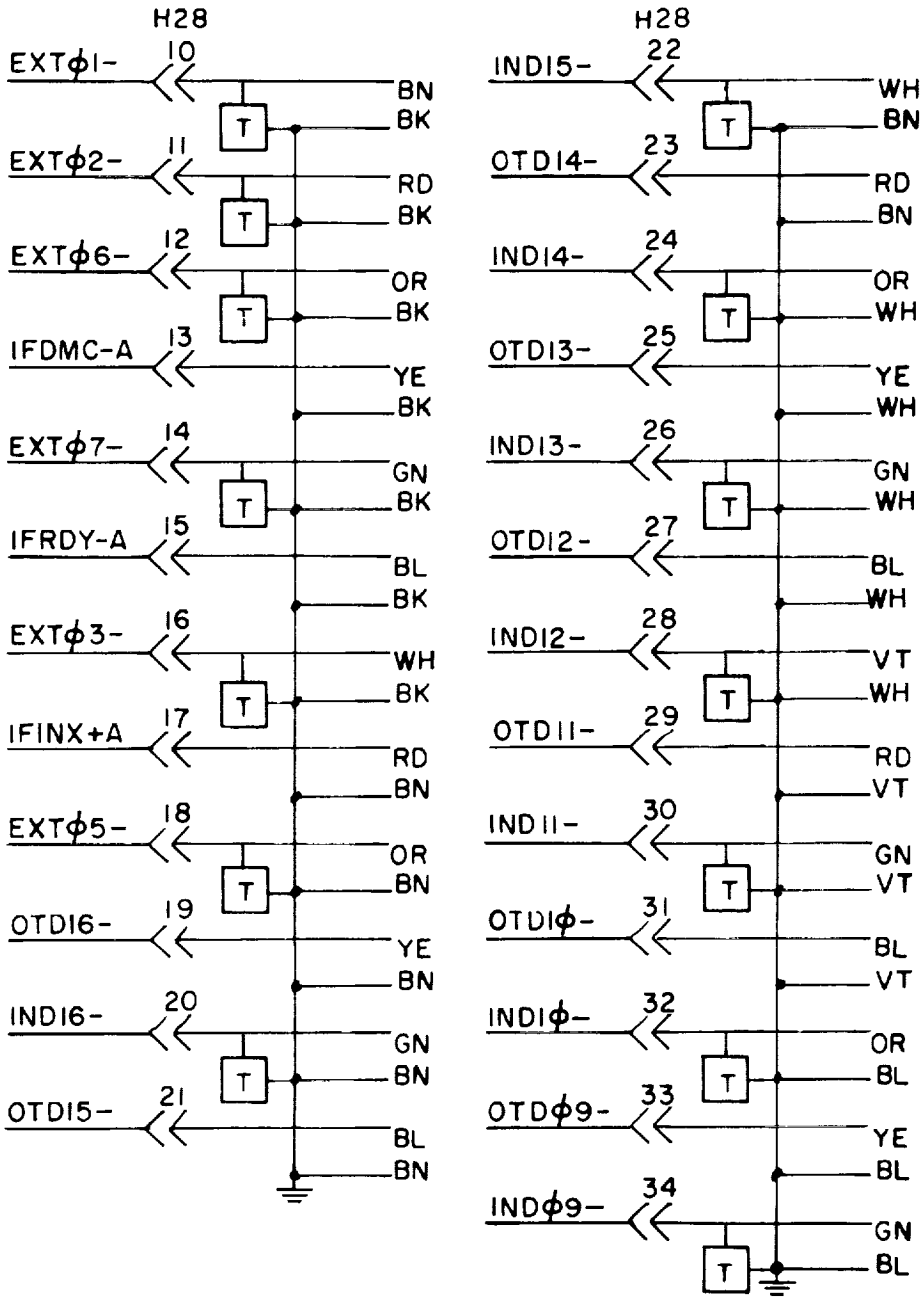

G28
EXTφ4-
10
BN
P
T
BK
OCPφ2-
11
RD
BK
IFSCD-
12
OR
T
BK
OCPφ4-
13
YE
BK
SRDYX-
14
GR
T
BK
OCPφ5-
15
BL
BK
SHIFT-
16
WH
T
BK
OCPφ6-
17
RD
BN
DIPXY-
18
OR
T
BN
OTDφ8-
19
YE
BN
INDφ8-
20
GN
T
BN
OTDφ7-
21
BL
BN
INDφ7-
22
WH
T
BN
DWG. I15
G28
OTDφ6-
23
RD
WH
INDφ6-
24
OR
T
WH
OTDφ5-
25
YE
WH
INDφ5-
26
GN
T
WH
OTDφ4-
27
BL
WH
INDφ4-
28
VT
T
WH
OTDφ3-
29
RD
VT
INDφ3-
30
GN
T
VT
OTDφ2-
31
BL
VT
INDφ2-
32
OR
T
BL
OTDφ1-
33
YE
BL
INDφ1-
34
GN
T
BL
T = TERMINATION (SEE TEXT)
CONNECTOR CARD

Figure 37


H28
EXTφ1- 10
EXTφ2- 11
EXTφ6- 12
IFDMC-A 13
EXTφ7- 14
IFRDY-A 15
EXTφ3- 16
IFINX+A 17
EXTφ5- 18
OTDI6- 19
INDI6- 20
OTDI5- 21
BN
BK
RD
BK
OR
BK
YE
BK
GN
BK
BL
BK
WH
BK
RD
BN
OR
BN
YE
BN
GN
BN
BL
BN
H28
INDI5- 22
OTDI4- 23
INDI4- 24
OTDI3- 25
INDI3- 26
OTDI2- 27
INDI2- 28
OTDI1- 29
INDI1- 30
OTDIφ- 31
INDIφ- 32
OTDφ9- 33
INDφ9- 34
WH
BN
RD
BN
OR
WH
YE
WH
GN
WH
BL
WH
VT
WH
RD
VT
GN
VT
BL
VT
OR
BL
YE
BL
GN
BL
T

37-2

APPENDIX II

LOGIC CARDS

The logic cards used in the Manipulator Logic are compatible with the standard Computer Control Company logic in the General Purpose Interface. Continuity of notation is maintained by using symbols similar to those in Appendix I.

Table 11 summarizes the logic cards and references their circuit diagrams and terminals.

TABLE 11

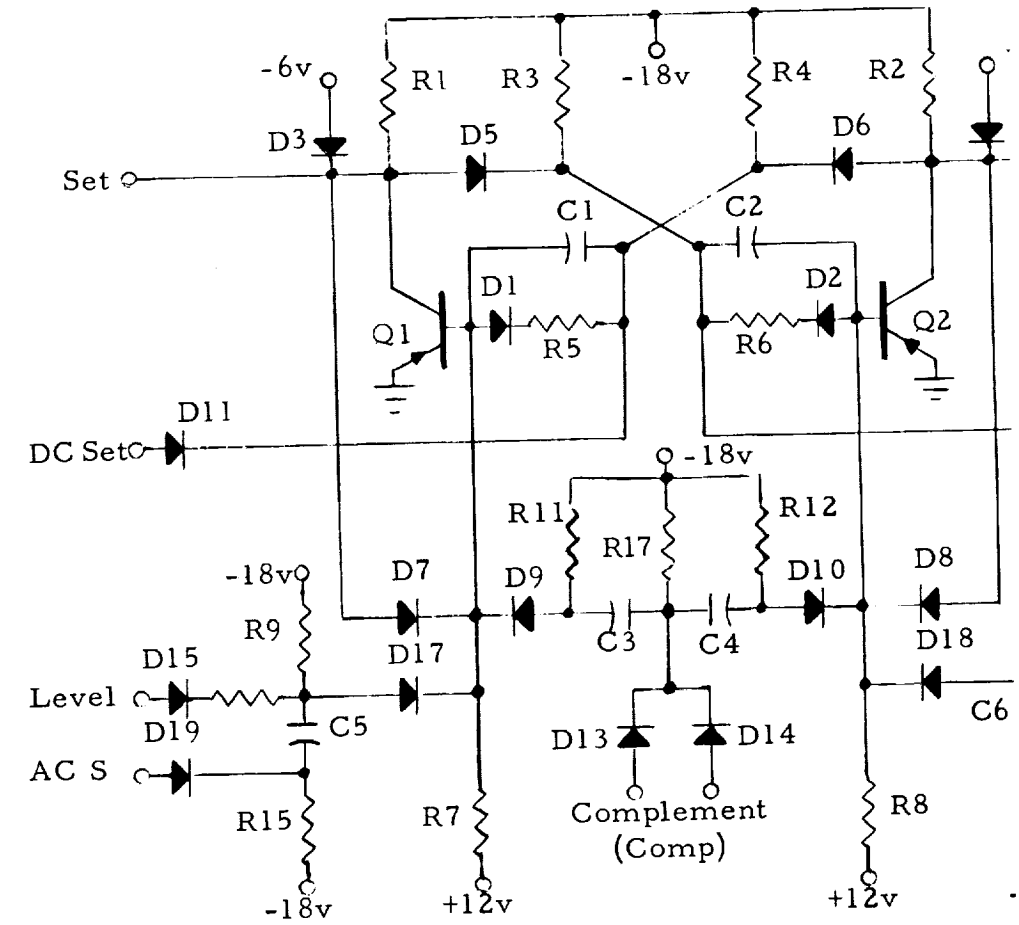
SUMMARY OF LOGIC CARDS

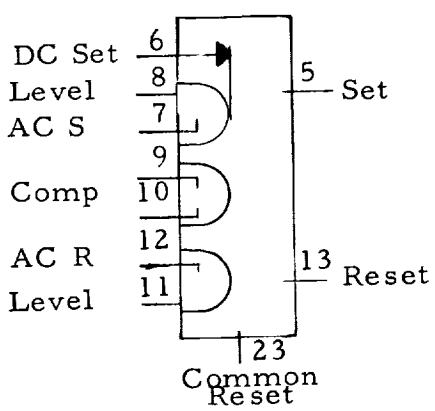
Type	Description[a]	Circuit Diagram	Terminals
FF	Flip-flops: four flip-flops per card.	Fig. 38	Fig. 38
SG	Standard Gate: 12 two-input gates per card.	Fig. 39	Fig. 39
HD	Heavy Duty version of SG.	Fig. 39	Fig. 39
CD	Computer Driver: 12 GPI input line drivers per card. Normally used in conjunction with Light Driver (LD) cards.	Fig. 40	Fig. 40
BG	Bi-directional counter Gates: specially wired version of SG. Increases effective number of input terminals by taking advantage of the fact that some gates use the same signals.	Fig. 39	Fig. 41
BD	Combination of BG and CD. Terminals 5 through 22 are CD type gates; 23 through 40 are BG type.	Figs. 39, 40	Fig. 42
AC	Axis Counter decode: Terminal connections are the same as the BG card except input terminal 10 is used only once, with output terminal 8. Uses HD components.	Fig. 39	Fig. 41

(a) Some gates have the collector load resistor omitted. These are indicated by an asterisk (*) in the symbol for the gate.

TABLE 11 (Continued)

LD	Light Driver card: Has a light during transistor on the card. Supplies base drive current for Computer Driver (CD) and D/A converters. Six per card.	Fig. 43	Fig. 43
PA	Power Amplifier: Six per card.	Fig. 44	Fig. 44
EC	Error Card: Specially wired version of SG. Functions as 14 input OR Gate. See Logic Diagrams, Fig. 60	Fig. 39	--





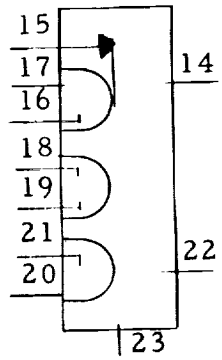


Figure 38 Circuit and Ter

9

-6v

D4

Reset

D12 Common Reset

-18v

R10

D16

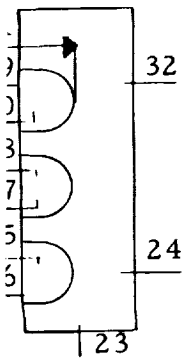
Level

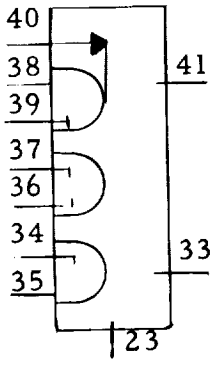
D20

AC R

R16

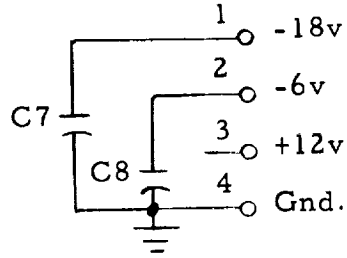
-18v





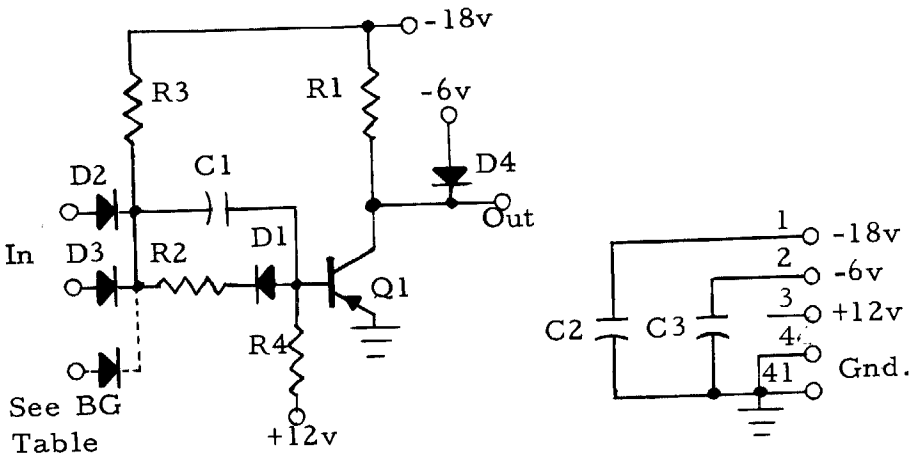
FF Parts List

R1, R2	2.2K, 1/2W
R3, R4	6.2K, 1/4W
R5, R6	2.2K, 1/4 W
R7, R8	22K, 1/4W
R9-R12	13K, 1/4W
R13, R14	390Ω, 1/4W
R15-R17	3.9K, 1/4W
C1, C2	150 pf
C3-C6	250 pf
C7, C8	.068 μf
D1, D2	IN816
D3-D20	IN276
Q1, Q2	2N1301



minals FF Type

37-2



Parts List	SG	HD
R1	2.2K .5W	5.6K
R2	2.2K .25W	1.6K
R3	6.2K .25W	4.7K .25W
R4	22K	18K .25W
C1	150 pf	150 pf
C2, C3	.068 µf	.068 µf
D1	IN816	IN816
D2 - D4	IN276	IN276
Q1	2N1301	2N1301

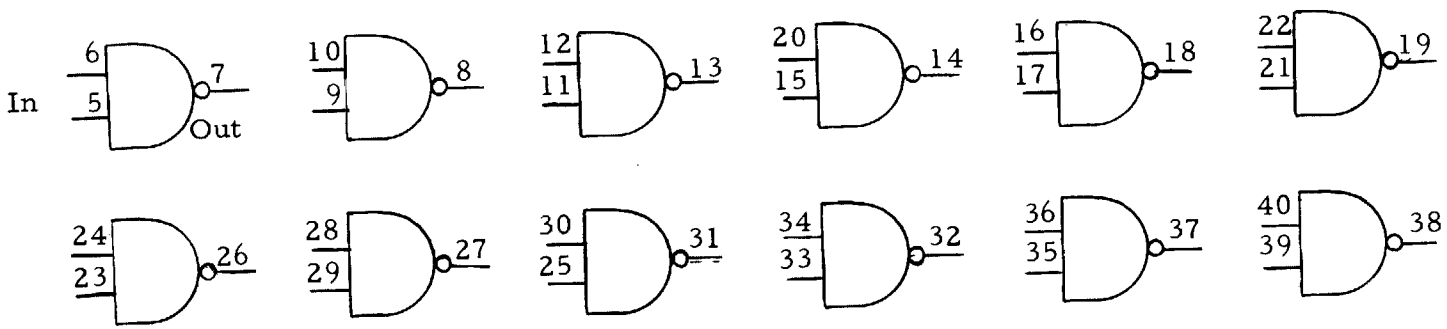
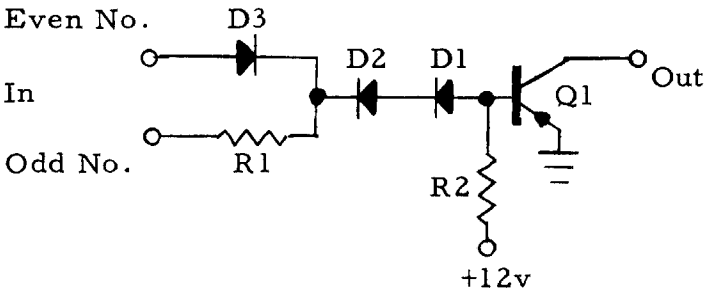
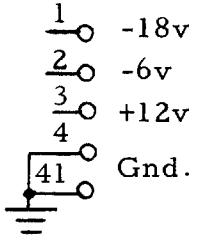


Figure 39 Circuit and Terminals SG;HD Type





Parts List

R1	1.8K .25W
R2	56K .25W
D1, D2	IN816
D3	IN276
Q1	2N1301

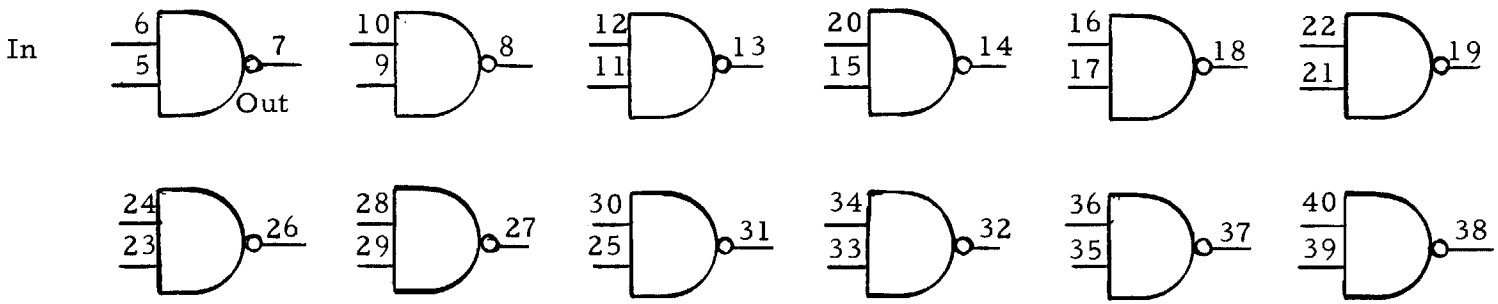
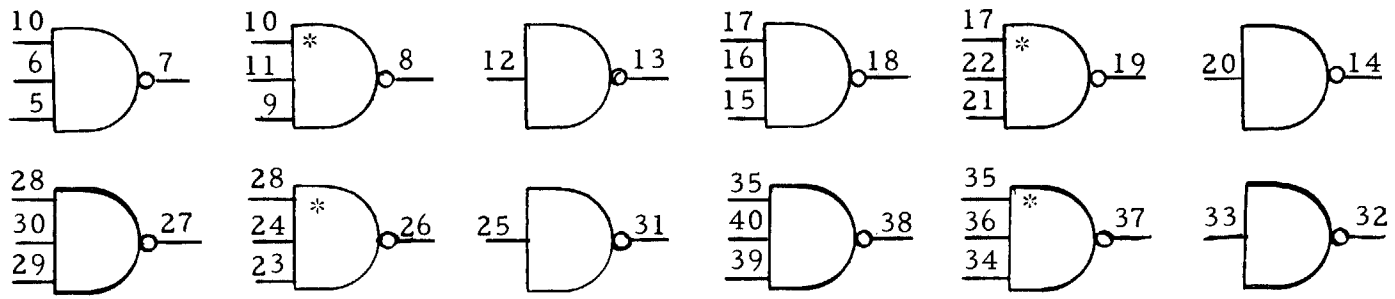
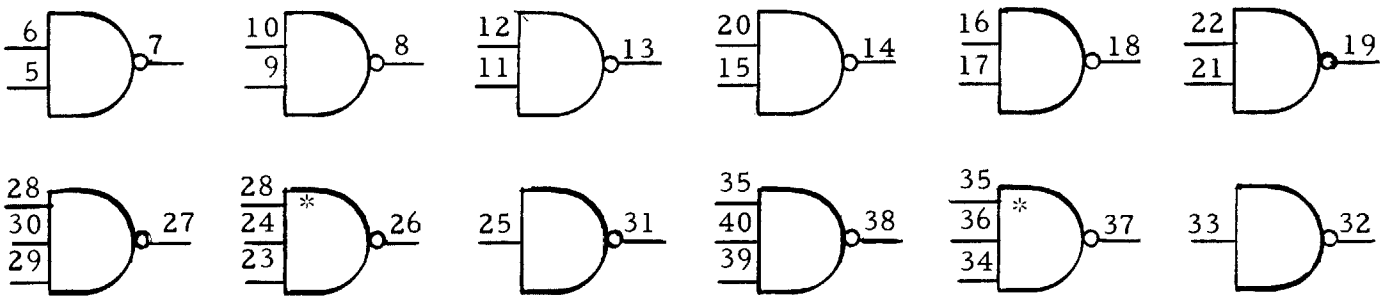


Figure 40 Circuit and Terminals CD Type



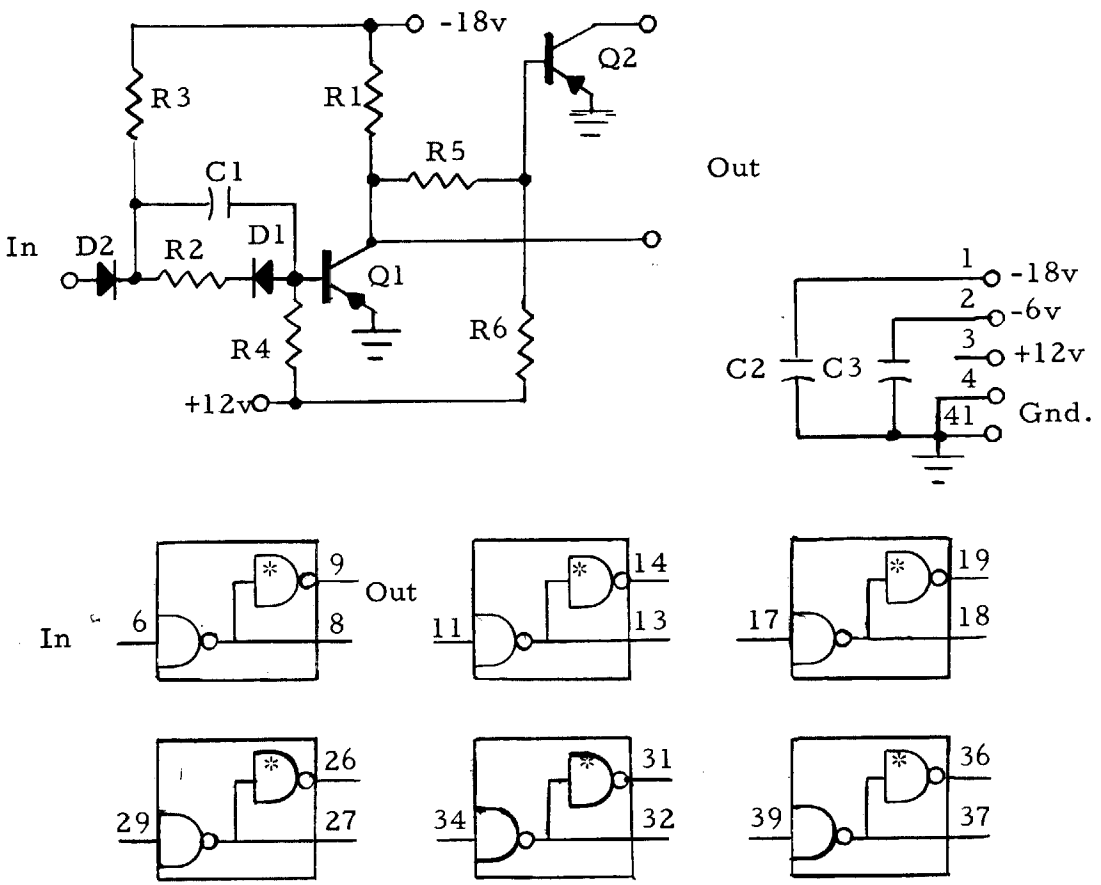
* No Collector Load BG Only

Figure 41 Terminals BG;AC Type



* No Collector Load

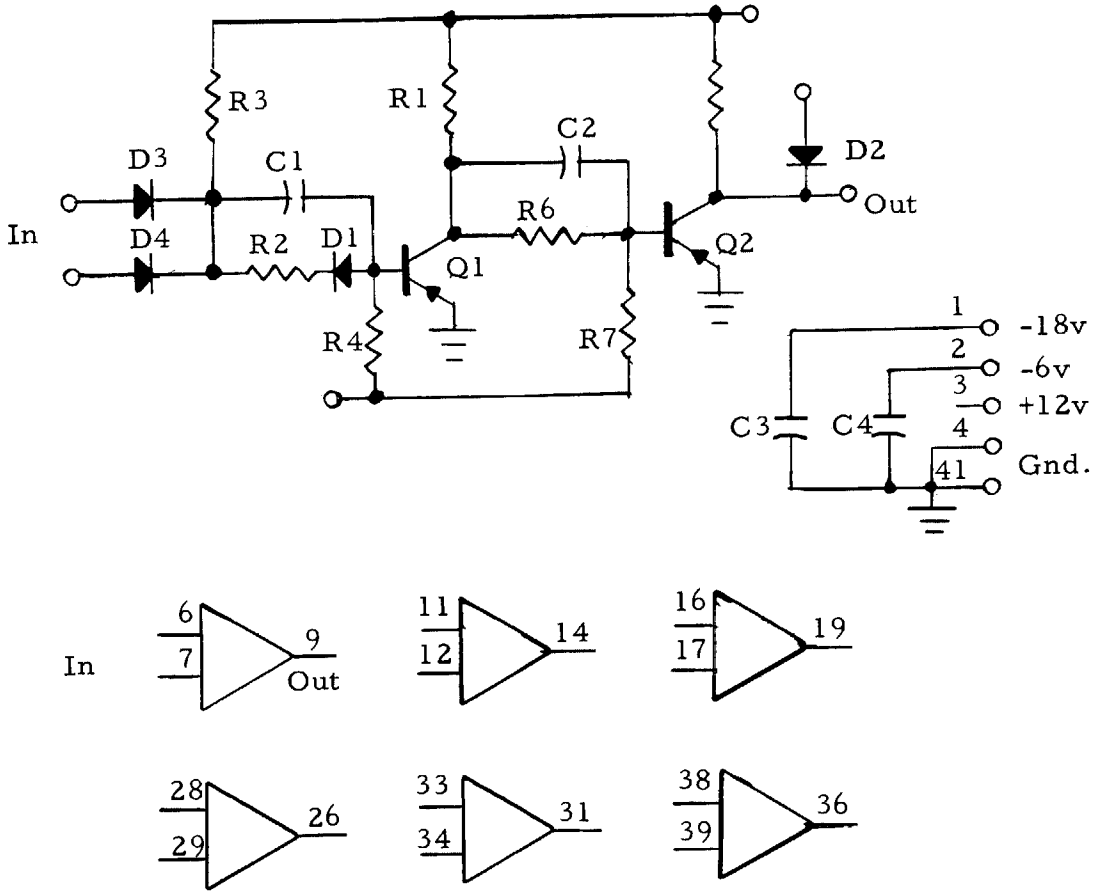
Figure 42 Terminals BD Type



Parts List

R1	1K .5W
R2	2.2K .25W
R3	6.2K .25W
R4	22K .25W
R5	2.7K .25W
R6	56K .25W
C1	150 pf
C2, C3	.068 μf
D1	IN276
D2	IN276
Q1	2N1301
Q2	2N3638

Figure 43 Circuit and Terminals, LD Type



Parts List

R1	1.2K .5W
R2	2.2K .25W
R3	6.2K .25W
R4	22K .25W
R5	1K .25W
R6	.56K .25W
R7	18K .25W
C1	150 pf
C2	1000 pf
C3, C4	.068 µf
D1, D2	IN816
D3, D4	IN276
Q1	2N1301
Q2	2N3638

Figure 44 Circuit and Terminals PA Type

APPENDIX III

MANIPULATOR LOGIC CIRCUITS

Introduction

This section contains the circuit details of the Manipulator Logic. Wiring diagrams show the logical and electrical connections of the control sections of the logic. Block diagrams and generalized schematics are used to describe the wiring of the axis buffers, which are essentially identical.

The logic cards are contained in three racks in the Manipulator Cabinet shown in Figure 45, and placed in the racks according to the diagram of Figure 46.

Bidirectional Counting Circuitry

Figure 47 illustrates the method used to describe the axis buffer bidirectional counting circuitry. Each block represents two bits of a four-bit bidirectional counter; by cascading more blocks, the schematic for a larger counter can be represented.

The details of Circuits A and B are shown in Figure 48, along with block diagrams of the seven 10 bit axis buffers. The circuit (Ckt. A or Ckt. B) and the location of the FF and BG or BD cards for a particular buffer are indicated in the blocks

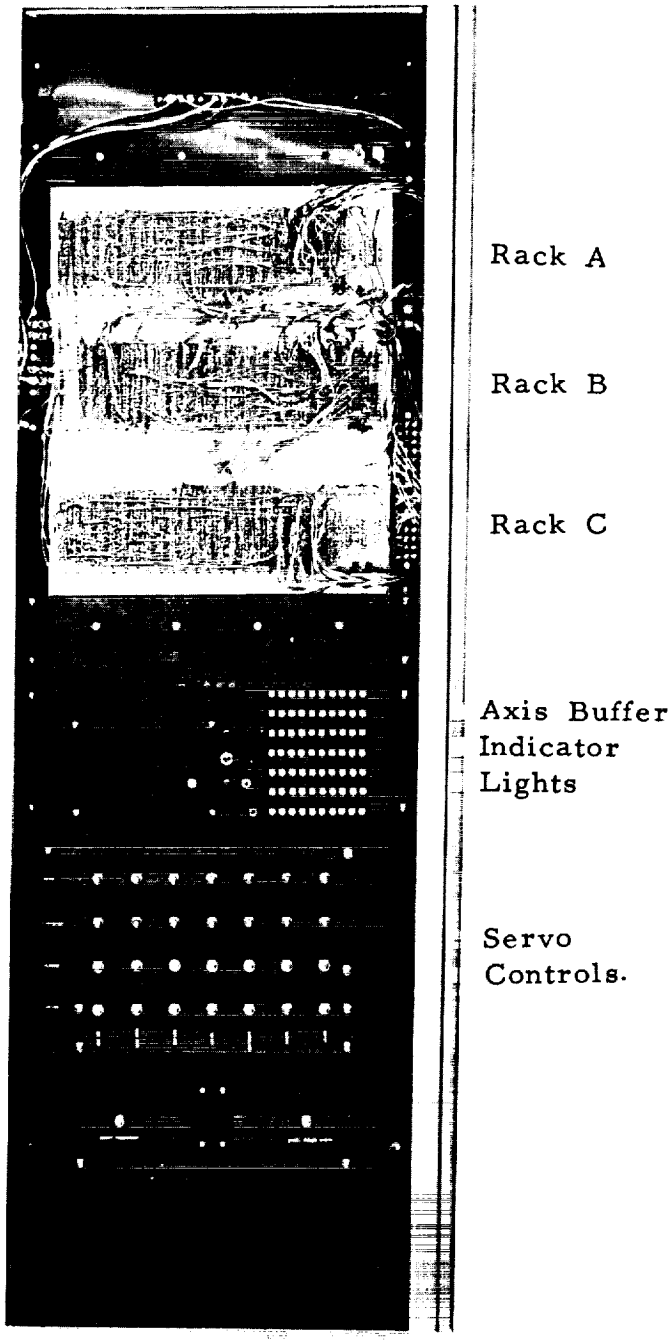


Figure 45 Manipulator Cabinent

Axis 1 Axis 2 Axis 3

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
F	B	F	B	F	B	F	B	F	B	F	B	F	B	F	B	C	C	L	L	L	L	L	D	D	D
F	G	F	G	F	G	F	G	F	G	F	G	F	G	F	D	D	D	D	D	D	D	D	A	A	A

Rack A

Control Axis 4

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
			H	S	E	P	H	S	S	S	A	F	H	F	B	F	B	F	B	C	L	L	S	D	C
			D	G	C	A	D	G	G	G	C	F	D	F	G	F	G	F	D	D	D	D	G	A	N

Rack B

Axis 5 Axis 6 Axis 7

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
F	B	F	B	F	B	F	B	F	B	F	B	F	B	F	B	C	C	L	L	L	L	L	D	D	D
F	G	F	G	F	G	F	G	F	G	F	G	F	G	F	D	D	D	D	D	D	D	D	A	A	A

Rack C

Figure 46 Card Placement

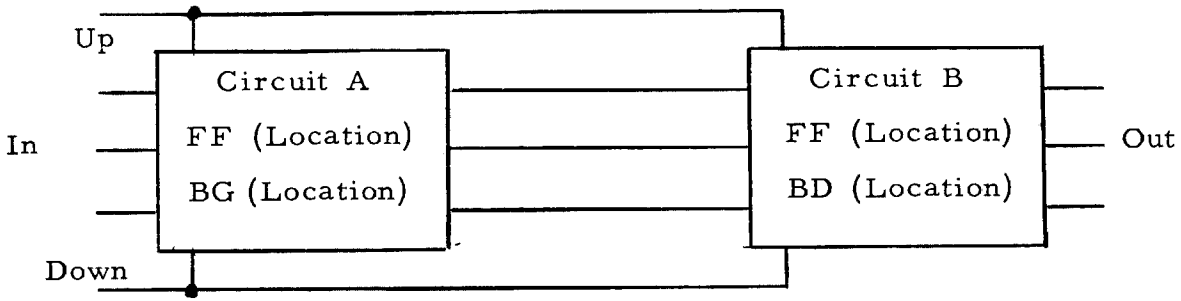
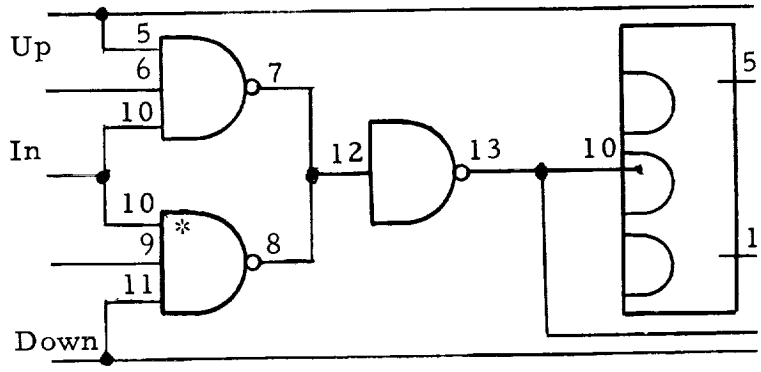
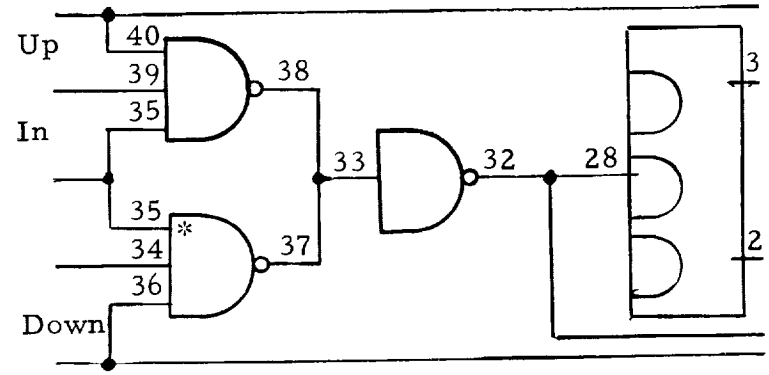


Figure 47 Bidirectional Counter - Block Diagram



Ci

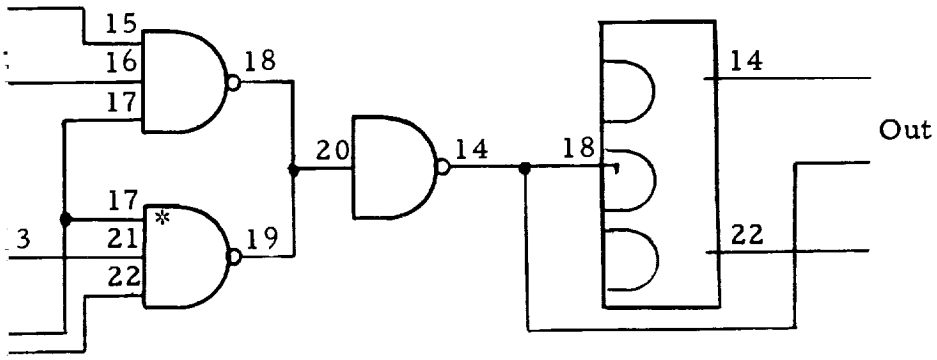


Ci

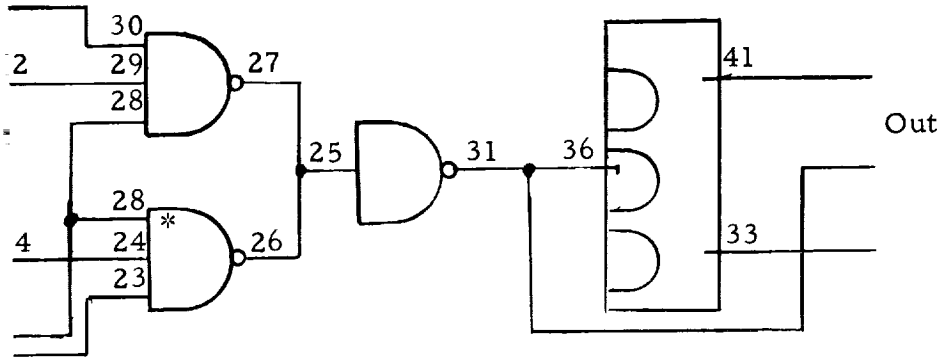
16 15	14 13	12 11	10 9	8 7
Ckt. A FF 1 BG 2	Ckt. B FF 1 BG 2	Ckt. A FF 3 BG 4	Ckt. B FF 3 BG 4	Ckt. B FF 5 BG 6
Axis 1 Rack A or Axis 5 Rack C				

16 15	14 13	12 11	10 9	8 7
Ckt. A FF 11 BG 12	Ckt. B FF 11 BG 12	Ckt. A FF 13 BG 14	Ckt. B FF 13 BG 14	Ckt. B FF 15 BD 12
Axis 3 Rack A or Axis 7 Rack C				

Figure 48 Bidir



rcuit A



rcuit B

16	15	14	13	12	11	10	9	8	7
Ckt. A FF 5 BG 6		Ckt. A FF 7 BG 6		Ckt. B FF 7 BG 8		Ckt. A FF 9 BG 10		Ckt. B FF 9 BG 10	
Axis 2 Rack A or Axis 6 Rack C									

16	15	14	13	12	11	10	9	8	7
Ckt. A FF 15 BG 16		Ckt. B FF 15 BG 16		Ckt. A FF 17 BG 18		Ckt. B FF 17 BG 18		Ckt. B FF 19 BD 20	
Axis 4 Rack B									

ectional Counter Wiring

48-2

representing that buffer. The bit numbers for each half block are shown above the blocks, and indicate the right or left half of the corresponding circuit. Use of the block diagrams is illustrated in the following example.

Example:

Find the input terminal to the gate that drives the complement input of Bit 8, Axis 3. The block diagram for Axis 3 indicates that this gate is shown in the left half of Circuit B, and is on a BD card in Rack A, location 12. Referring to Circuit B, the terminal is found to be terminal number 33.

Buffer Read In and Read Out Wiring

Figures 49 through 52 illustrate the Read In, and Figures 53 through 56, the Read Out wiring for the axis buffers. The lists in the figures specify the card location and terminal numbers of each of the terminals indicated on the schematic. Use of the lists is illustrated in the following example.

Example:

Find the input terminal to the CD gate that is activated when the buffer for Axis 5 has a one in bit 12. Referring to Figure 53, which is valid for Axis 1, Rack A or Axis 5, Rack C, it is seen from the schematic that this terminal has the code

CDIN. Entering the list at the left, under Bit 12, and proceeding to the column headed CDIN, the sequence of numbers 17-23 is found. Thus, the terminal sought is in Rack C, on the card in location 17, and is terminal number 23 of that card.

Control Logic

Figures 57 through 63 show the wiring of the control sections of the Manipulator Logic. The operation of these sections is straightforward and is described in Chapter III.

Bit	S Level	AC S	S Out	R Level	AC R	R Out	LDBFN
16	1-8	1-7	1-5	1-11	1-12	1-13	Axis 1 B-7-9
15	1-17	1-16	1-14	1-20	1-21	1-22	
14	1-29	1-30	1-32	1-26	1-25	1-24	Axis 5 B-7-26
13	1-38	1-39	1-41	1-35	1-34	1-33	
12	3-8	3-7	3-5	3-11	3-12	3-13	
11	3-17	3-16	3-14	3-20	3-21	3-22	
10	3-29	3-30	3-32	3-26	3-25	3-24	
9	3-38	3-39	3-41	3-35	3-34	3-33	
8	5-29	5-30	5-32	5-26	5-25	5-24	
7	5-38	5-39	5-41	5-35	5-34	5-33	

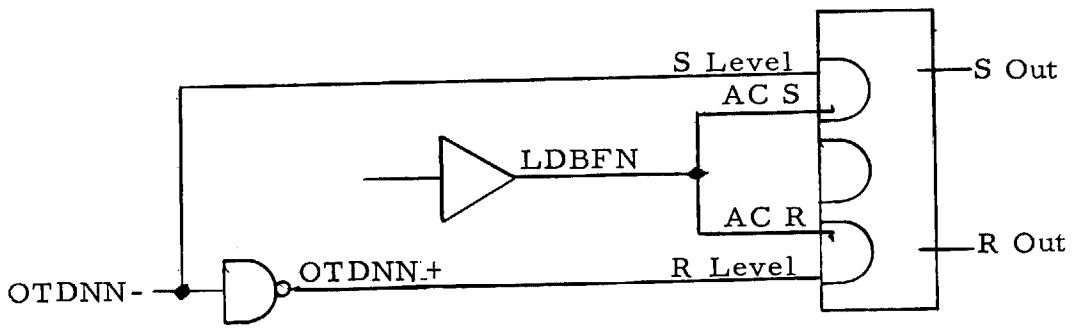


Figure 49 Read In - Axis 1 Rack A or Axis 5 Rack C

Bit	S Level	AC S	S Out	R Level	AC R	R Out	LDBFN
16	5-8	5-7	5-5	5-11	5-12	5-13	
15	5-17	51-6	5-14	5-20	5-21	5-22	Axis 2 B-7-14
14	7-8	7-7	7-5	7-11	7-12	7-13	
13	7-17	7-16	7-14	7-20	7-21	7-22	
12	7-29	7-30	7-32	7-26	7-25	7-24	Axis 6 B-7-31
11	7-38	7-39	7-41	7-35	7-34	7-33	
10	9-8	9-7	9-5	9-11	9-12	9-13	
9	9-17	9-16	9-14	9-20	9-21	9-22	
8	9-29	9-30	9-32	9-26	9-25	9-24	
7	9-38	9-39	9-41	9-35	9-34	9-33	

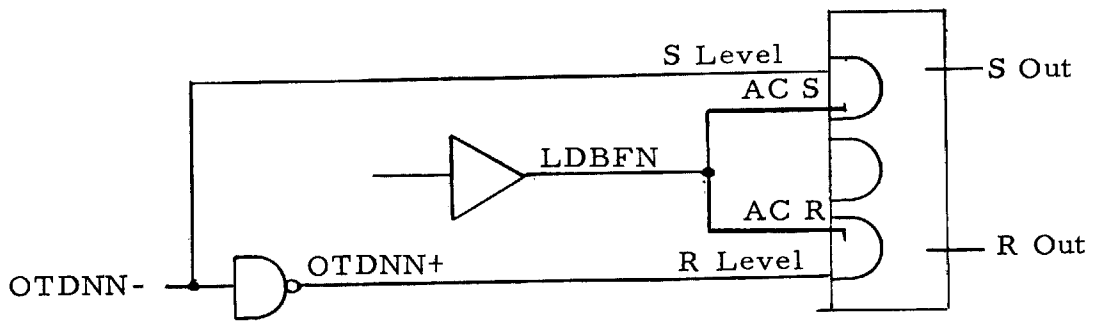


Figure 50 Read In - Axis 2 Rack A or Axis 6 Rack C

Bit	S Level	AC S	S Out	R Level	AC R	R Out	LDBFN
16	15-8	15-7	15-5	15-11	15-12	15-13	
15	15-17	15-16	15-14	15-20	15-21	15-22	Axis 3 B-7-19
14	15-29	15-30	15-32	15-26	15-25	15-24	
13	15-38	15-39	15-41	15-35	15-34	15-33	Axis 7 B-7-36
12	17-18	17-7	17-5	17-11	17-12	17-13	
11	17-17	17-17	17-14	17-20	17-21	17-22	
10	17-29	17-30	17-32	17-26	17-25	17-24	
9	17-38	17-39	17-41	17-35	17-34	17-33	
8	19-29	19-30	19-32	19-26	19-25	19-24	
7	19-38	19-39	19-41	19-35	19-34	19-33	

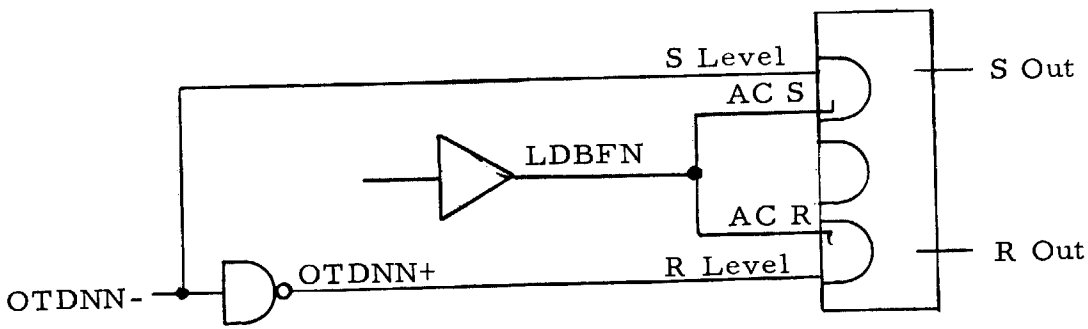


Figure 51 Read In - Axis 3 Rack A or Axis 7 Rack C

Bit	LDBF4S	AC S	S Level	S Out	LDBF4R	AC R	R Level	R Out
16	B-14-7	15-7	15-8	15-5	B-14-13	15-12	15-11	15-13
15	"	15-16	15-17	15-14	"	15-21	15-20	15-22
14	"	15-30	15-29	15-32	"	15-25	15-26	15-24
13	"	15-39	15-38	15-41	"	15-34	15-35	15-33
12	"	17-7	17-8	17-5	"	17-12	17-11	17-13
11	B-14-8	17-16	17-17	17-14	B-14-14	17-21	17-20	17-22
10	"	17-30	17-29	17-32	"	17-25	17-26	17-24
9	"	17-39	17-38	17-41	"	17-34	17-35	17-33
8	"	19-30	19-29	19-32	"	19-25	19-26	19-24
7	"	19-39	19-38	19-41	"	19-34	19-35	19-33

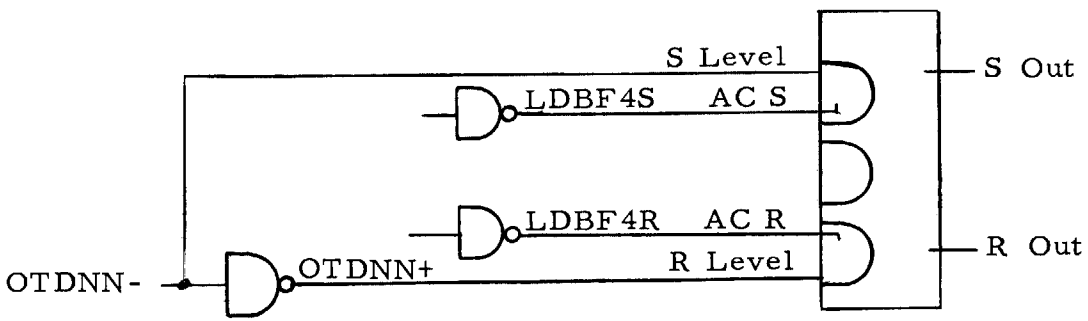


Figure 52 Read In - Axis 4 Rack B

Bit	FF	LD In	LD Out	D/A	CD In	AXISX	CD Out	Light
16	1-13	22-17	22-18	24-19	16-15	16-6	16-7	22-19
15	1-22	22-29	22-27	24-18	16-15	16-20	16-14	22-26
14	1-24	22-34	22-32	24-17	17-15	17-6	17-7	22-31
13	1-33	22-39	22-37	24-16	17-15	17-20	17-14	22-36
12	3-13	23-6	23-8	24-15	17-23	17-24	17-26	23-9
11	3-22	23-11	23-13	24-26	17-33	17-34	17-32	23-14
10	3-24	23-17	23-18	24-25	18-5	18-6	18-7	23-19
9	3-33	23-29	23-27	24-24	18-15	18-20	18-14	23-26
8	5-24	23-34	23-32	24-23	18-23	18-24	18-26	23-31
7	5-33	23-39	23-37	24-22	18-33	18-34	18-32	23-36

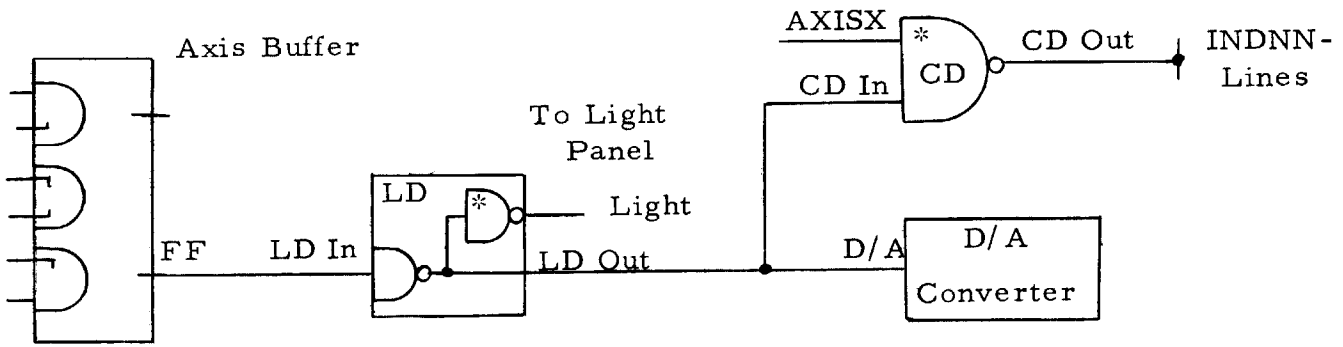


Figure 53 Read Out - Axis 1 Rack A or Axis 5 Rack C

Bit	FF	LD In	LD Out	D/A	CD In	AXISX	CD Out	Light
16	5-13	20-34	20-32	25-19	16-19	16-10	16-18	20-31
15	5-22	20-39	21-37	25-18	16-17	16-16	16-18	20-36
14	7-13	21-6	21-8	25-17	17-9	17-10	17-8	21-9
13	7-22	21-11	21-13	25-16	17-17	17-16	17-18	21-14
12	7-24	21-17	21-18	25-15	17-29	17-28	17-27	21-19
11	7-33	21-29	21-27	25-26	17-35	17-36	17-37	21-26
10	9-13	21-34	21-32	25-25	18-9	18-10	18-8	21-31
9	9-22	21-39	21-37	25-24	18-17	18-16	18-18	21-36
8	9-24	22-16	22-18	25-23	18-29	18-28	18-27	22-9
7	9-33	22-11	22-13	25-22	18-35	18-36	18-37	22-14

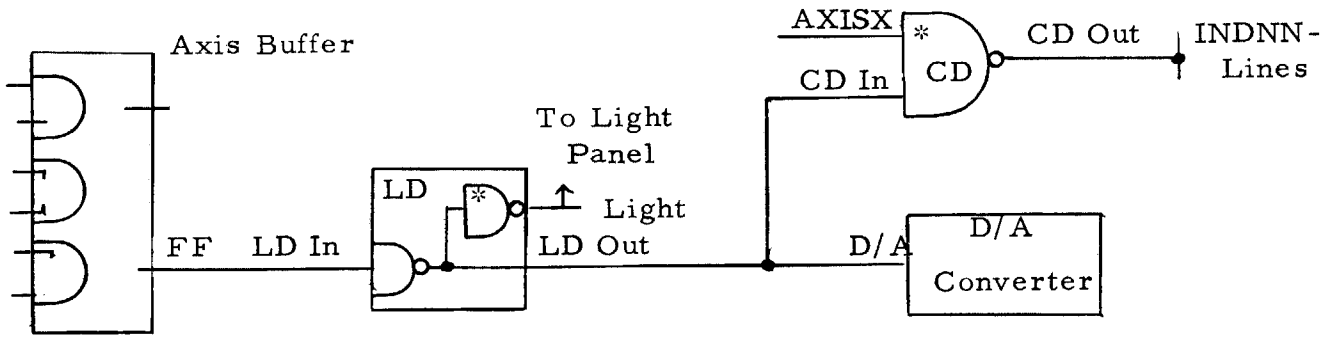


Figure 54 Read Out - Axis 2 Rack A or Axis 5 Rack C

Bit	FF	LD In	LD Out	D/A	CD In	AXISX	CD Out	Light
16	11-13	19-6	19-8	26-19	16-11	16-12	16-13	19-19
15	11-22	19-11	19-13	26-18	16-21	16-22	16-19	19-14
14	11-24	19-17	19-18	26-17	17-11	17-12	17-13	19-19
13	11-33	19-29	19-27	26-16	17-21	17-22	17-19	19-26
12	13-13	19-34	19-32	26-15	17-25	17-30	17-31	19-31
11	13-22	19-39	19-37	26-26	17-39	17-40	17-38	19-36
10	13-24	20-16	20-8	26-25	18-11	18-12	18-13	20-9
9	13-33	20-11	20-13	26-24	18-21	18-22	18-19	20-14
8	15-24	20-17	20-18	26-23	18-25	18-30	18-31	20-19
7	15-33	20-34	20-27	26-22	18-39	18-40	18-38	20-26

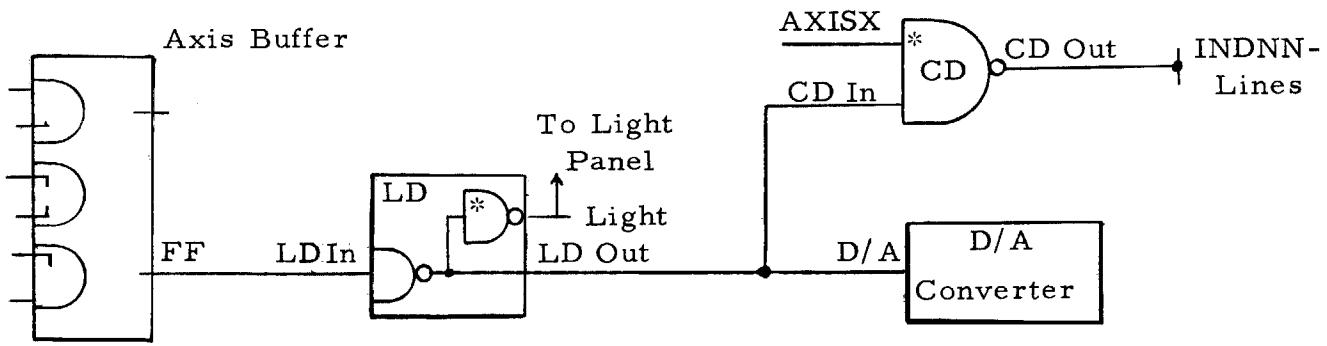


Figure 55 Read Out - Axis 3 Rack A or Axis 7 Rack C

Bit	FF	LD In	LD Out	D/A	CD In	AXISX	CD Out	Light
16	15-13	22-6	22-8	25-19	21-33	21-34	21-32	22-9
15	15-22	22-11	22-13	25-18	21-25	21-30	21-31	22-14
14	15-24	22-17	22-18	25-17	21-29	21-28	21-27	22-19
13	15-33	22-29	22-27	25-16	21-23	21-24	21-26	22-26
12	17-13	22-34	22-32	25-15	21-21	21-22	21-19	22-31
11	17-22	22-39	22-37	25-26	21-17	21-16	21-18	22-36
10	17-24	23-6	23-8	25-25	21-15	21-20	21-14	23-9
9	17-33	23-11	23-13	25-24	21-11	21-12	21-13	23-14
8	19-24	23-17	23-18	25-23	21-9	21-10	21-8	23-19
7	19-33	23-29	23-27	25-22	21-10	21-16	21-7	23-26

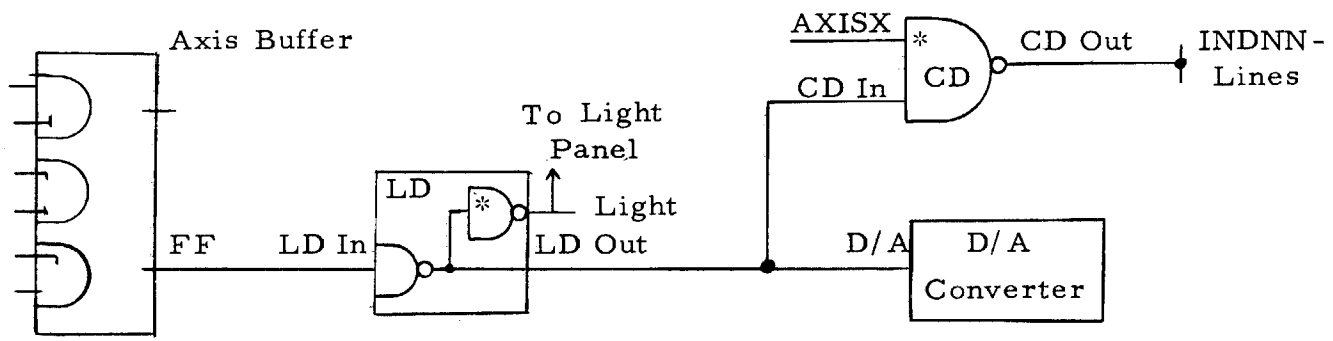


Figure 56 Read Out - Axis 4 Rack B

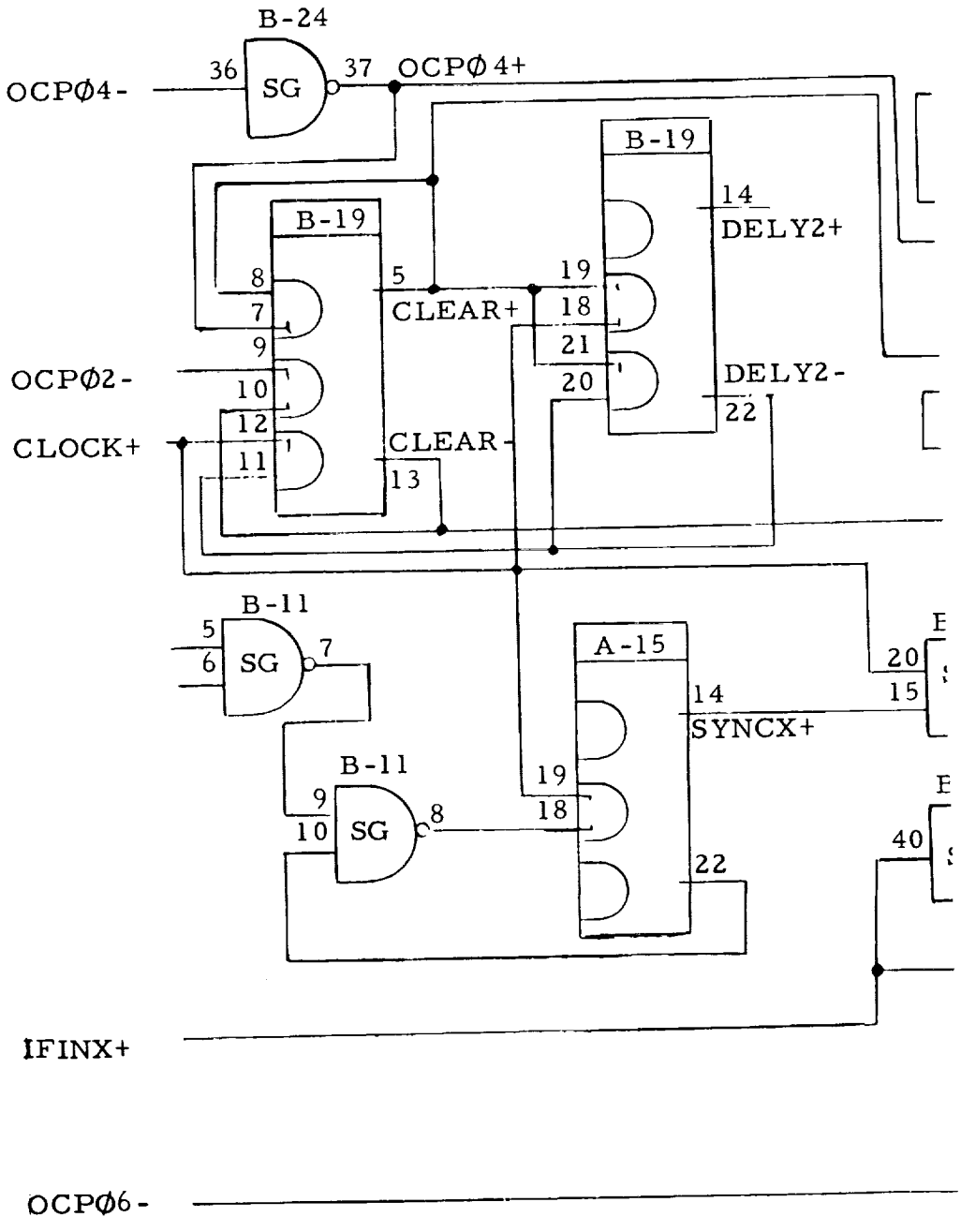
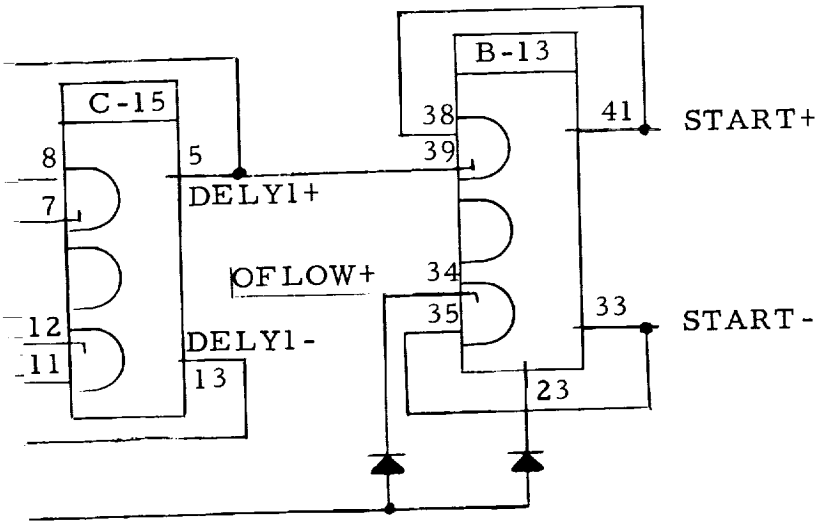
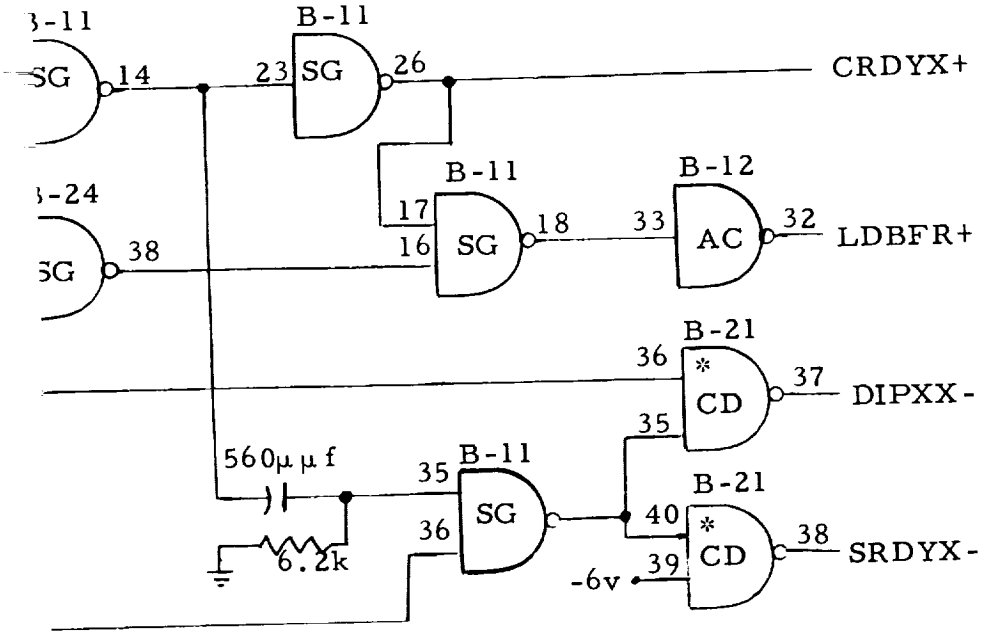


Figure 57 Timin

57-1





g and Control

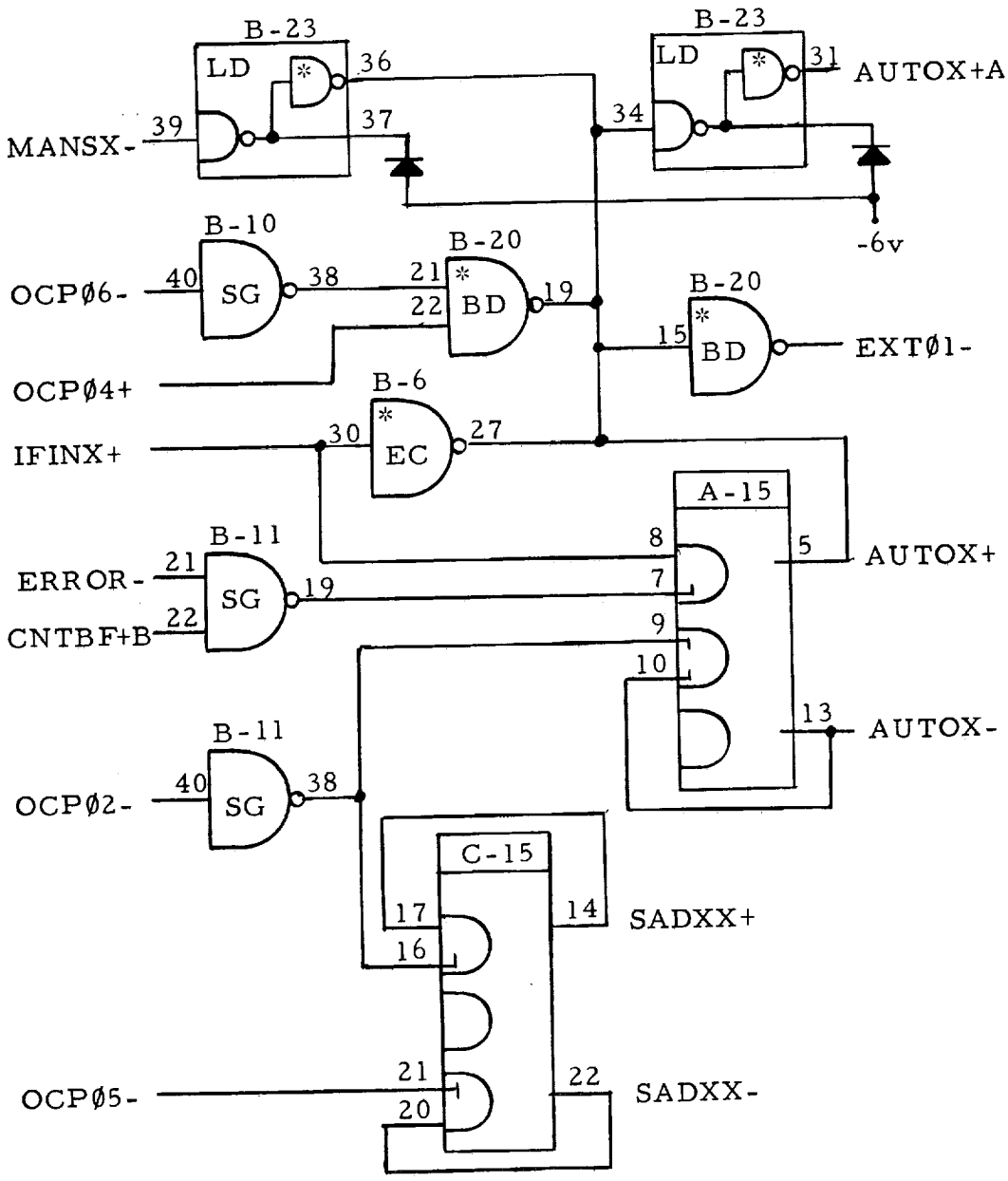


Figure 58 Manual-Auto Select

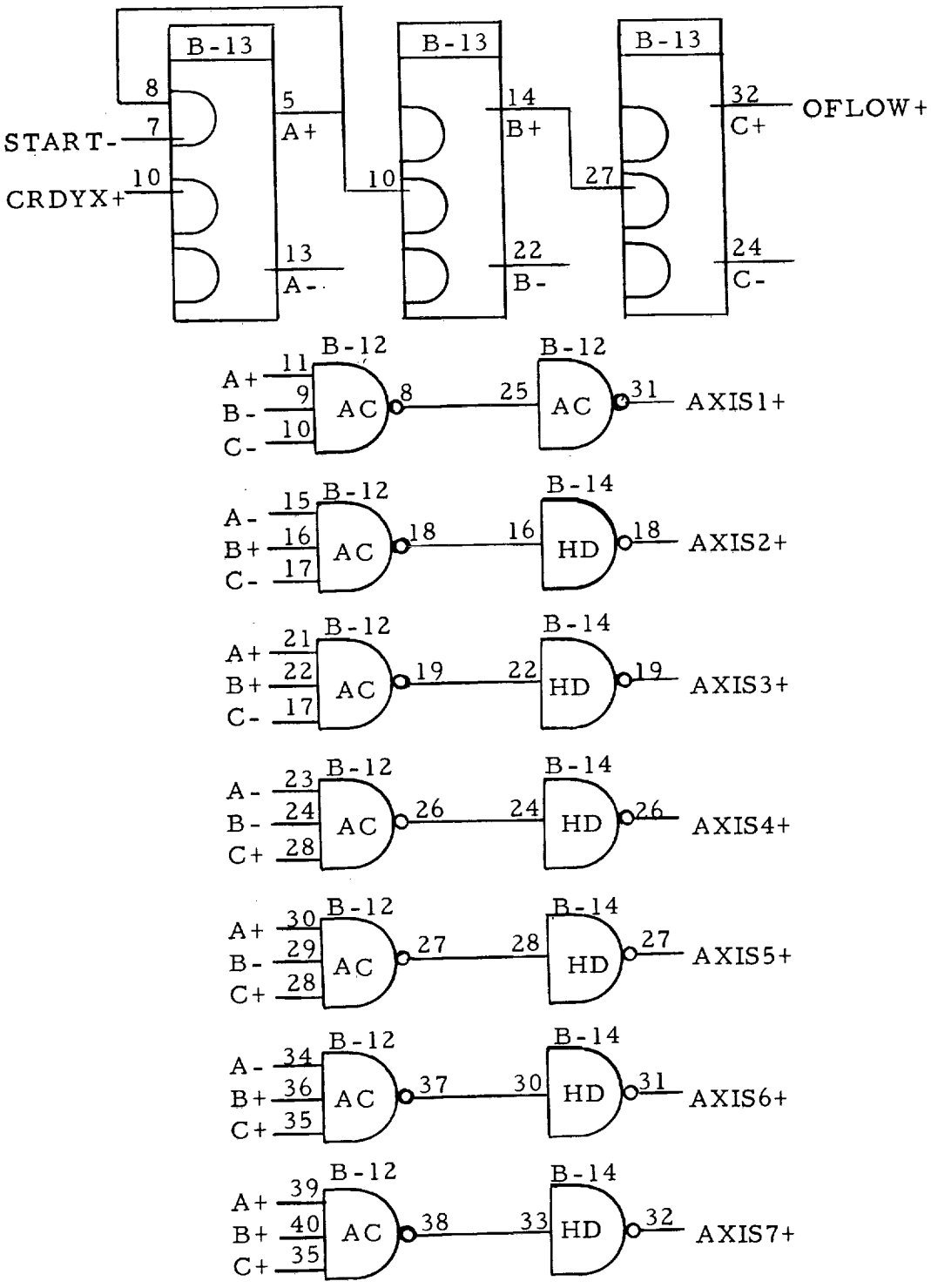


Figure 59 Axis Counter

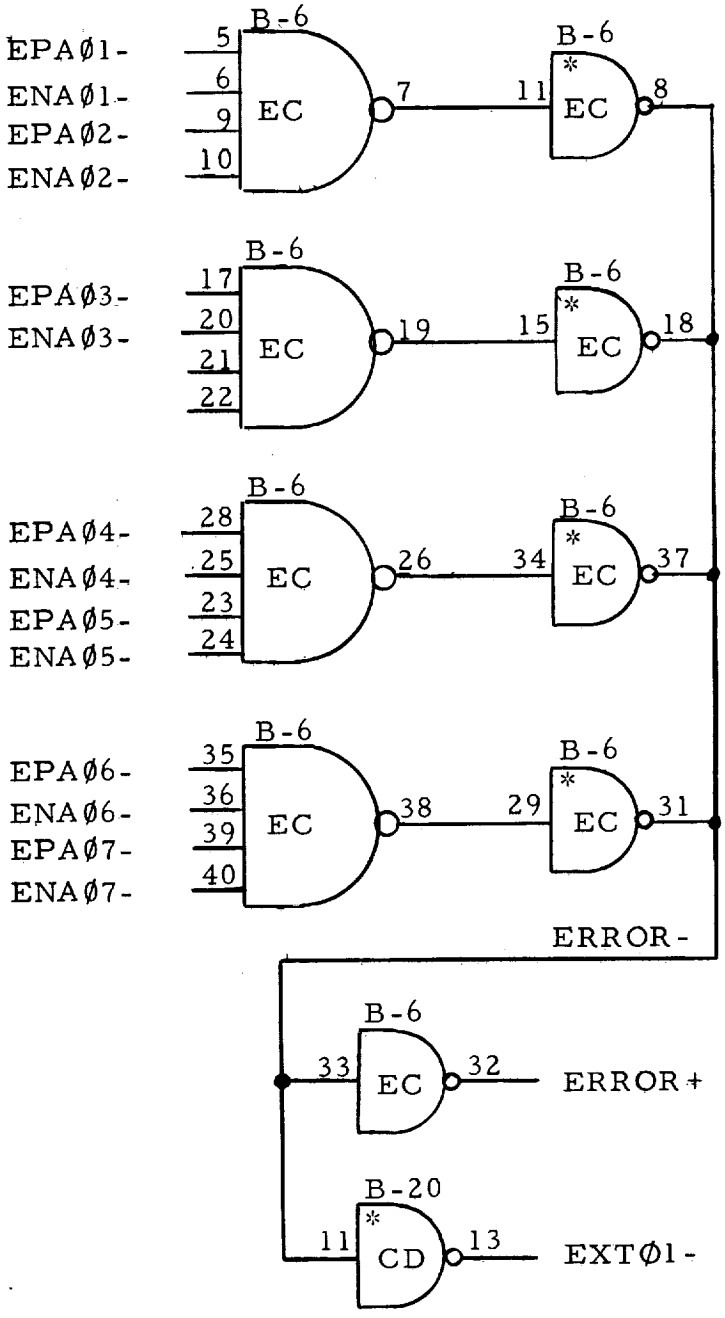


Figure 60 Error Sense

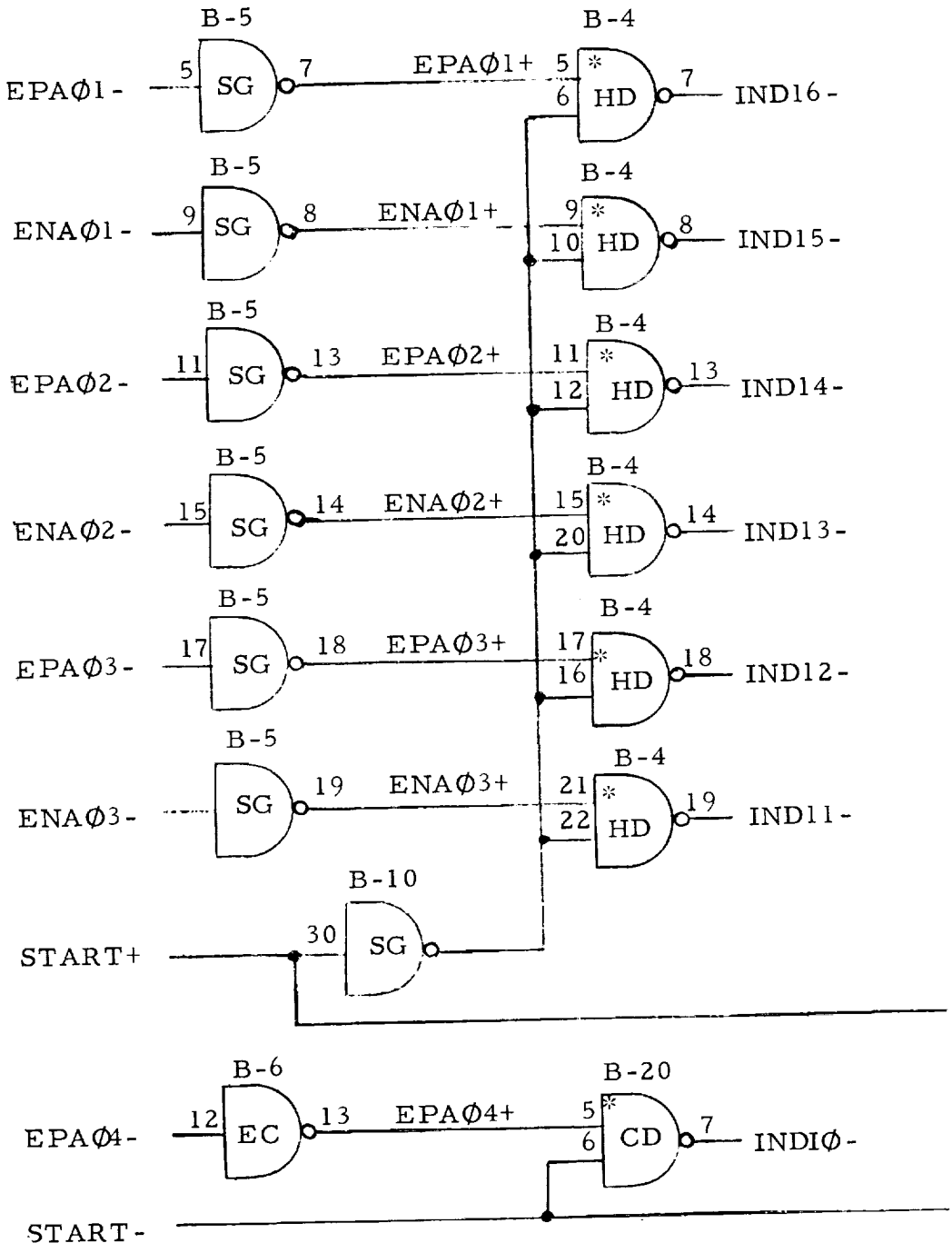
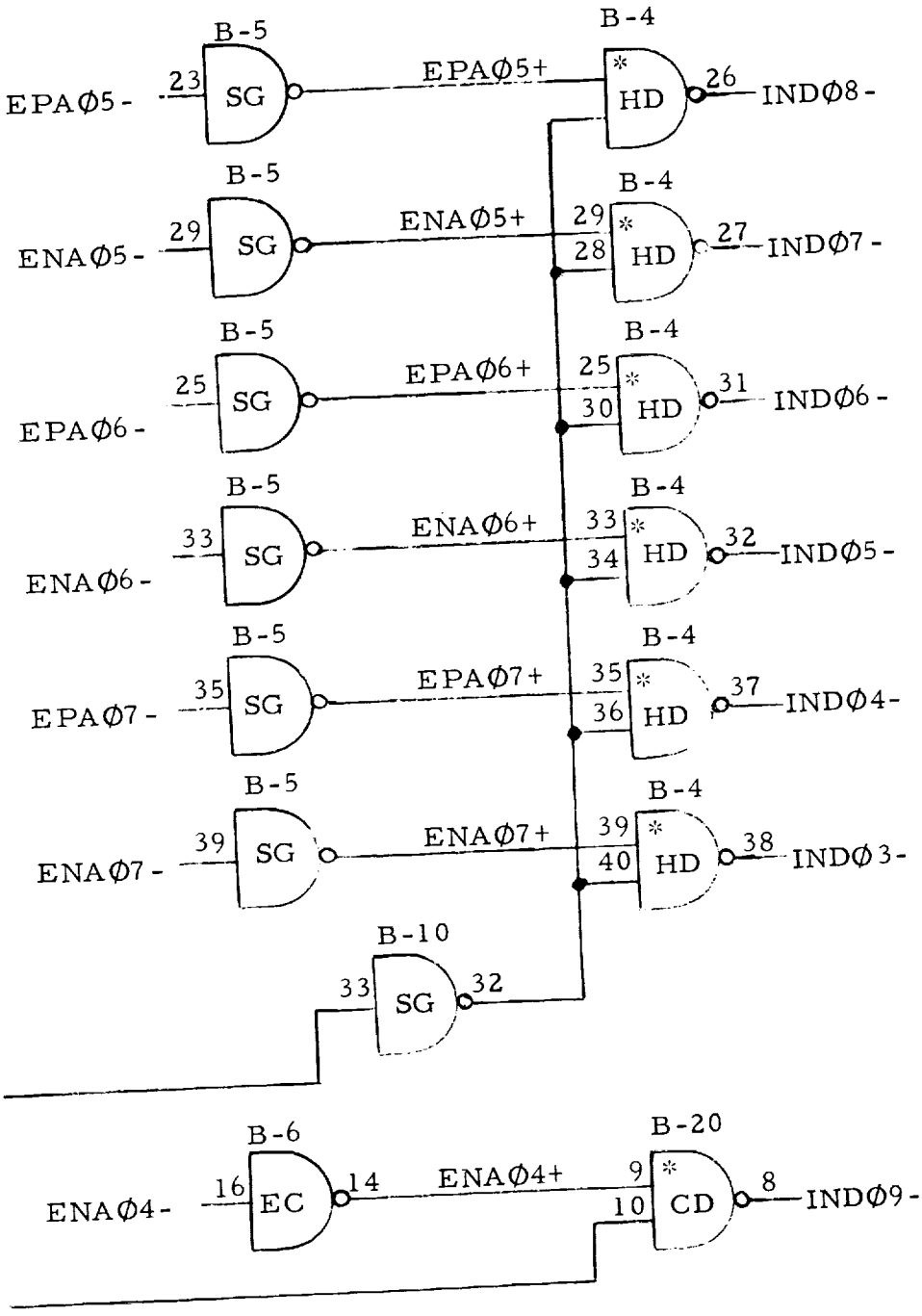


Figure 61 E

61-1


B-5
EPAØ5-
23
SG
EPAØ5+
B-4
*
HD
26
INDØ8-
B-5
ENAØ5-
29
SG
ENAØ5+
B-4
29
28
*
HD
27
INDØ7-
B-5
EPAØ6-
25
SG
EPAØ6+
B-4
25
30
*
HD
31
INDØ6-
B-5
ENAØ6-
33
SG
ENAØ6+
B-4
33
34
*
HD
32
INDØ5-
B-5
EPAØ7-
35
SG
EPAØ7+
B-4
35
36
*
HD
37
INDØ4-
B-5
ENAØ7-
39
SG
ENAØ7+
B-4
39
40
*
HD
38
INDØ3-
B-10
33
SG
32
B-6
ENAØ4-
16
EC
14
ENAØ4+
B-20
9
10
*
CD
8
INDØ9-

Error Word

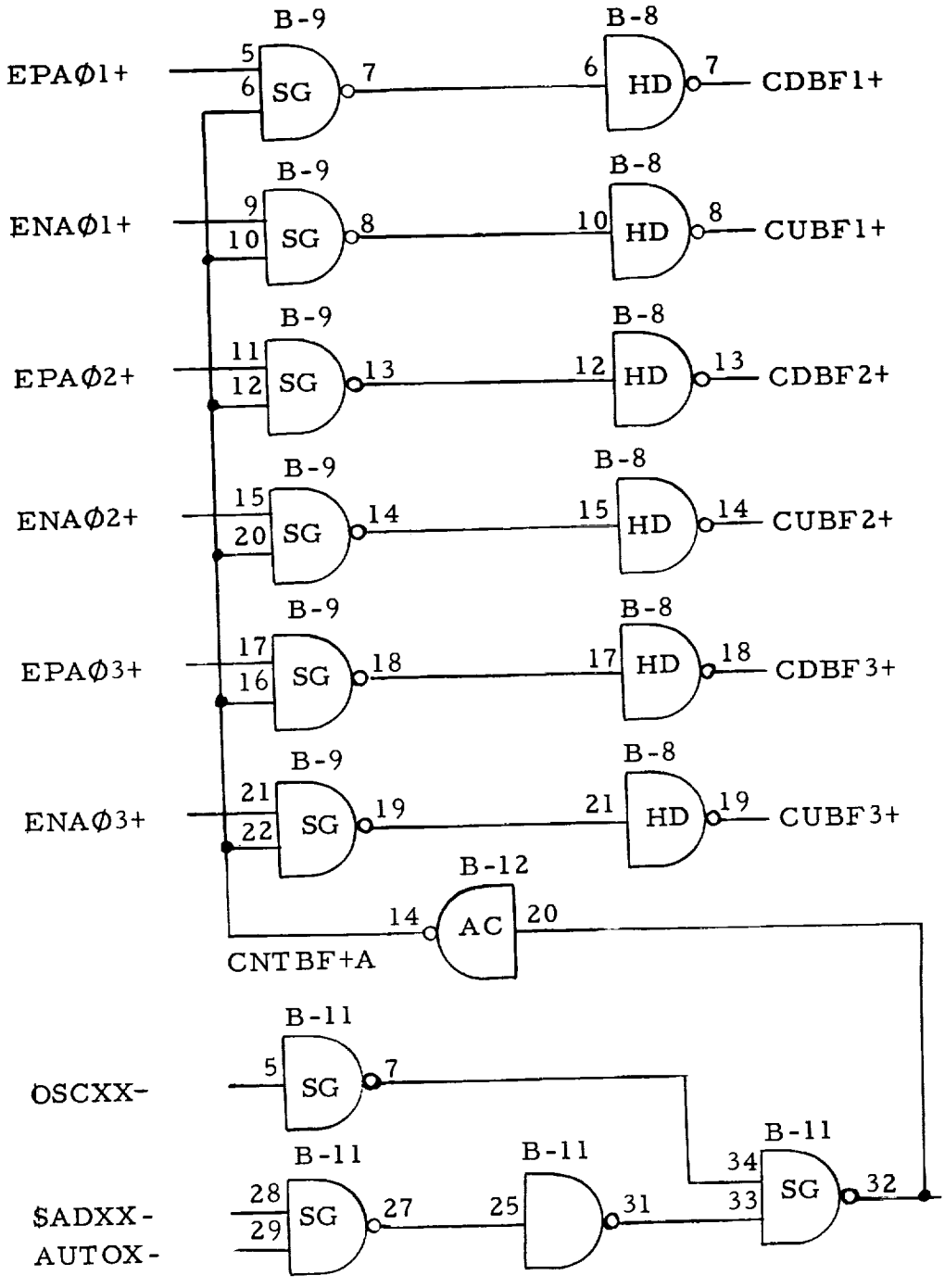
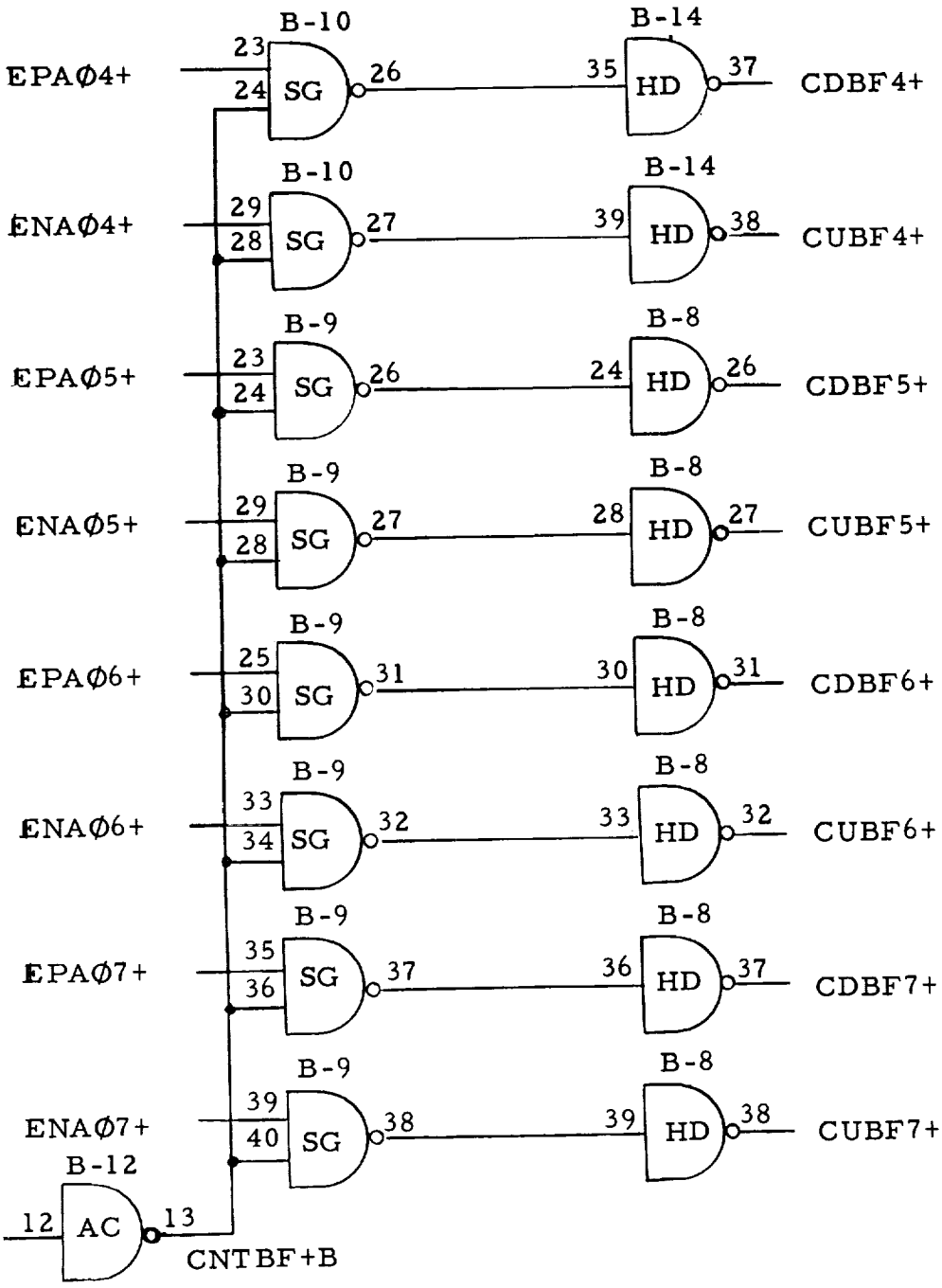


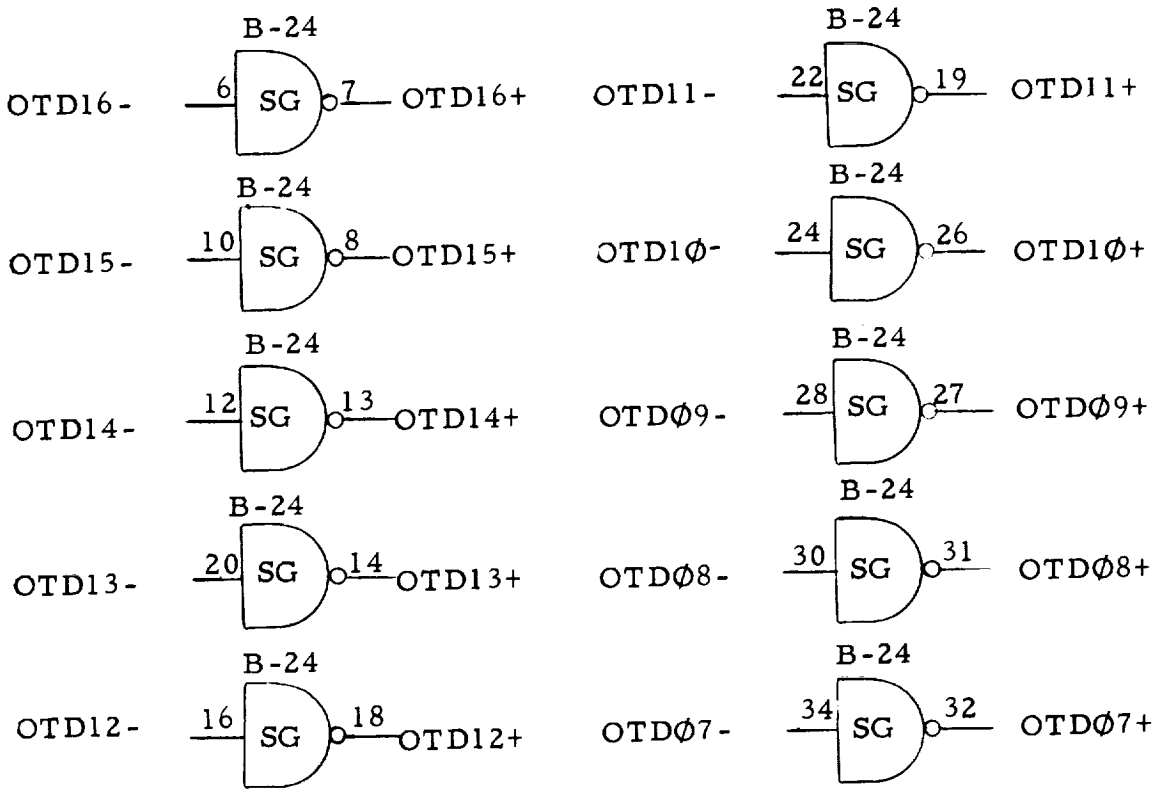
Figure 62 Coun

62-1



t Control

62-2



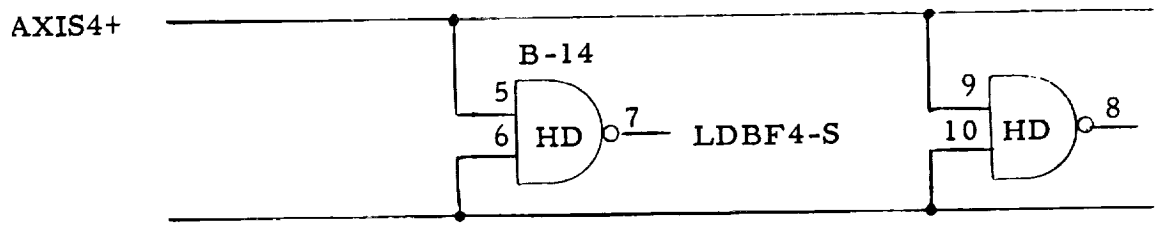
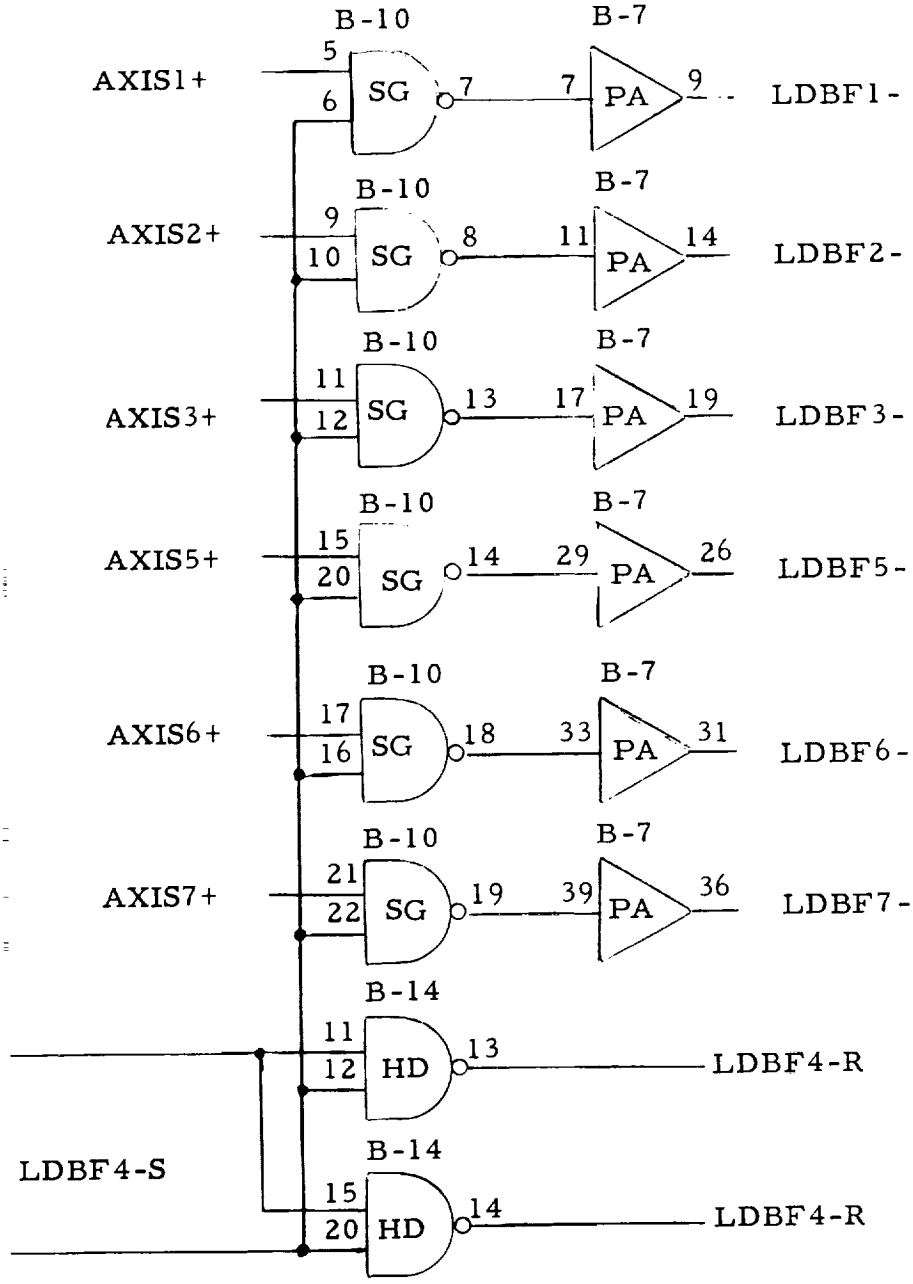


Figure 63 Buffer L


B-10
B-7
AXIS1+
5
6
SG
7
7
PA
9
LDBF1-
B-10
B-7
AXIS2+
9
10
SG
8
11
PA
14
LDBF2-
B-10
B-7
AXIS3+
11
12
SG
13
17
PA
19
LDBF3-
B-10
B-7
AXIS5+
15
20
SG
14
29
PA
26
LDBF5-
B-10
B-7
AXIS6+
17
16
SG
18
33
PA
31
LDBF6-
B-10
B-7
AXIS7+
21
22
SG
19
39
PA
36
LDBF7-
B-14
11
12
HD
13
LDBF4-R
LDBF4-S
B-14
15
20
HD
14
LDBF4-R

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BIBLIOGRAPHY

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