Report No. 03-66-87

First Quarterly Report

for

PHOTON-COUPLED ISOLATION SWITCH

(1 January - 31 March 1966)

Contract No. 951340

Prepared by

E. L. Bonin

Texas Instruments Incorporated
Semiconductor-Components Division
Post Office Box 5012
Dallas 22, Texas

for

Jet Propulsion Laboratory
California Institute of Technology
4800 Oak Grove Drive
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ABSTRACT

Development of a new type of photon-coupled switch has begun. The switch provides a transistor output electrically isolated from the driving sources and all other terminals of the switch. The device consists of a monolithic silicon integrated driver circuit which supplies bias to a gallium arsenide photon-emitting diode. The emitting diode is optically coupled to an electrically-isolated silicon phototransistor. The program has been divided into two phases:

Phase I, design and breadboarding of the driver circuit and development of the gallium arsenide emitting diode-silicon phototransistor pair

Phase II, integration of the driver circuit and prototype production of the complete isolation switch.

The design and breadboarding of the driver circuit has been completed. The circuit uses two transistors and diode input gates which will allow up to 10 inputs in the integrated design with a 14-lead miniature package.

The silicon phototransistor has also been designed and diffusion masks are in process. Noise transmissibility of the transistor in the non-conductive state was shown to be determined by the device and circuit capacitances.

Negligible changes in the important device parameters were exhibited for gallium arsenide emitting diodes, early types of emitting diode-phototransistor pair, and diode-transistor integrated circuit logic gates exposed to proton radiation.

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SECTION I

INTRODUCTION

Conventional integrated circuits lack an effective means of providing the transformer function of electrical potential isolation. The development of high efficiency semiconductor photon emitting diodes has led to a practical solution. By positioning the emitting diode in close proximity to an appropriate photodetector, the optical coupling of the devices results in an electrical signal connection with electrical isolation.

Efficient optical coupling between a GaAs p-n junction photon emitting diode and an electrically - isolated semiconductor photodetector was demonstrated in October 1961[1]. In subsequent work, GaAs emitting diodes with Si photodetectors were found to offer the greatest practical advantage of the available semiconductor systems, and several types of optoelectronic devices using this source-detector system were developed[2, 3]. These included a multiplex switch that does not use a transformer, an isolated-gate p-n-p-n-type switch, an isolated-input transistor, and an isolated-input pulse amplifier.

The present contract concerns the development of a photon coupled switch which combines a monolithic Si driver circuit for a GaAs emitting diode which is optically coupled to a Si phototransistor. The transistor output of the device is electrically isolated from the driving sources and the other terminals of the switch. This development program is divided into two phases. Phase I consists of the design and breadboarding of the driver circuit and the development of the emitting diode-phototransistor pair. In Phase II, the driver circuit is integrated in a single Si wafer and the complete isolation switch is fabricated in a miniature integrated circuit package.

This report describes the work performed during the first quarter of the contract under Phase I. Integration of the driver circuit during the second phase will be made using the same diffusion processes as for the isolated-input optoelectronic pulse amplifier, Texas Instruments type SNX1304. Detailed characterization of this device, determined for design of the driver circuit, is described. The design and breadboarding of the driver circuit has been substantially completed. Design considerations, which led to a two-transistor circuit, are discussed. In the integrated version, ten diode input-gates will be provided.

The phototransistor has also been designed and diffusion masks are in process. As described, the transistor utilizes an epitaxial collector region with a diffused base and emitter. A high-refractive-index glass bonds the GaAs emitting diode to the photo-

transistor. An analysis of the noise transmissibility of the transistor in the non-conductive state is presented which relates this parameter to the device and circuit capacitances.

Data is presented for a number of devices submitted for proton radiation. These include GaAs emitting diodes, early types of emitting diode-phototransistor pair, and diode transistor integrated circuit logic gates. These exhibited negligible changes in the important device parameters.

SECTION II

TECHNICAL DISCUSSION

A. DEVICE PARAMETER DATA

The following parameter data was measured for elements on the silicon integrated circuit of the SNX1304 using the temperature and current ranges expected for the driver circuit. The base-emitter voltage drops as a function of current at -20°C, 25°C, and 100°C for a number of transistors on the SNX1304 are given in Table I. For the same conditions, values for an emitter current of 10 μA range as much as ±5%, and for other values range only between ±1 to ±2.5%. A representative characteristic is shown in Figure 1. At the lower currents, the slopes follow the theoretical values of 51 mV/current decade at -20°C, 60 mV/decade at 25°C, and 75 mV/decade at 100°C. Series resistances account for deviations at the higher currents. The characteristics for currents below 10 mA apply directly for all but the last transistor in the driver circuit. As will be discussed in a later section, the final transistor in the driver circuit should have about 4 times the emitter area of the transistors measured. In this case, the base-emitter voltage for a given emitter current is given in Figure 1 using 1/4 of that current.

Forward, common-emitter current gains for the transistors at collector currents of 1, 7, and 30 mA at -20, 25, and 100°C are given in Table II. Current gains are substantially greater at the highest temperature; this is of importance for the driver circuit since minimum base current also occurs at the highest temperature.

Resistors for the SNX1304 are produced by either emitter, base, or collector diffusions. Resistance data at -20°C, 25°C and 100°C for several resistors made with each type of diffusion are given in Table III. Two values of resistors made with the emitter diffusion are described in the data; the temperature coefficients are different, due to the effect of contact resistances. Choosing two resistors, A8 and B1, having average coefficients for each group, a value for a temperature invariant contact resistance can be determined. Because the coefficients are equal when a contact resistance R is subtracted,

$$\frac{R_{(-20°C)}-R}{R_{(100°C)}-R} = \frac{15.7 - R}{19.1 - R} = \frac{24.5 - R}{30.5 - R} \qquad (1)$$

from which

$$R = 4.2\ \Omega.$$

Table I. Base-emitter Voltage Drop Characteristics
For Silicon Transistors in the SNX1304

Unit	V_{BE} I_E = 10 μA	V_{BE} 50 μA	V_{BE} 100 μA	V_{BE} 500 μA	V_{BE} 1 mA	V_{BE} 5 mA	V_{BE} 10 mA	V_{BE} 40 mA
T = -20°C								
Q1	0.65	0.695	0.715	0.75	0.77	0.82	0.85	0.95
Q2	0.655	0.705	0.725	0.76	0.785	0.835	0.87	0.985
Q3	0.65	0.695	0.71	0.75	0.77	0.815	0.85	0.95
Q4	0.655	0.71	0.725	0.76	0.78	0.83	0.855	0.965
Q5	0.61	0.70	0.725	0.765	0.785	0.835	0.86	0.975
Q6	0.67	0.71	0.73	0.77	0.79	0.835	0.865	0.98
Q7	0.59	0.69	0.715	0.755	0.775	0.825	0.855	0.96
T = 25°C								
Q1	0.56	0.61	0.63	0.67	0.69	0.745	0.775	0.875
Q2	0.57	0.62	0.64	0.685	0.70	0.76	0.79	0.91
Q3	0.56	0.61	0.63	0.67	0.69	0.745	0.775	0.875
Q4	0.57	0.62	0.64	0.685	0.70	0.755	0.785	0.89
Q5	0.54	0.615	0.635	0.685	0.71	0.77	0.805	0.89
Q6	0.57	0.625	0.64	0.69	0.71	0.77	0.81	0.905
Q7	0.51	0.605	0.625	0.675	0.695	0.76	0.79	0.885
T = 100°C								
Q1	0.39	0.45	0.465	0.525	0.55	0.61	0.645	0.84
Q2	0.40	0.46	0.47	0.53	0.56	0.625	0.66	0.82
Q3	0.39	0.45	0.465	0.52	0.545	0.605	0.64	0.83
Q4	0.40	0.46	0.475	0.535	0.56	0.62	0.66	0.86
Q5	0.40	0.465	0.485	0.545	0.565	0.63	0.665	0.825
Q6	0.41	0.47	0.49	0.545	0.57	0.63	0.67	0.83
Q7	0.38	0.45	0.475	0.53	0.55	0.615	0.65	0.795

V_{CB} = 1 V

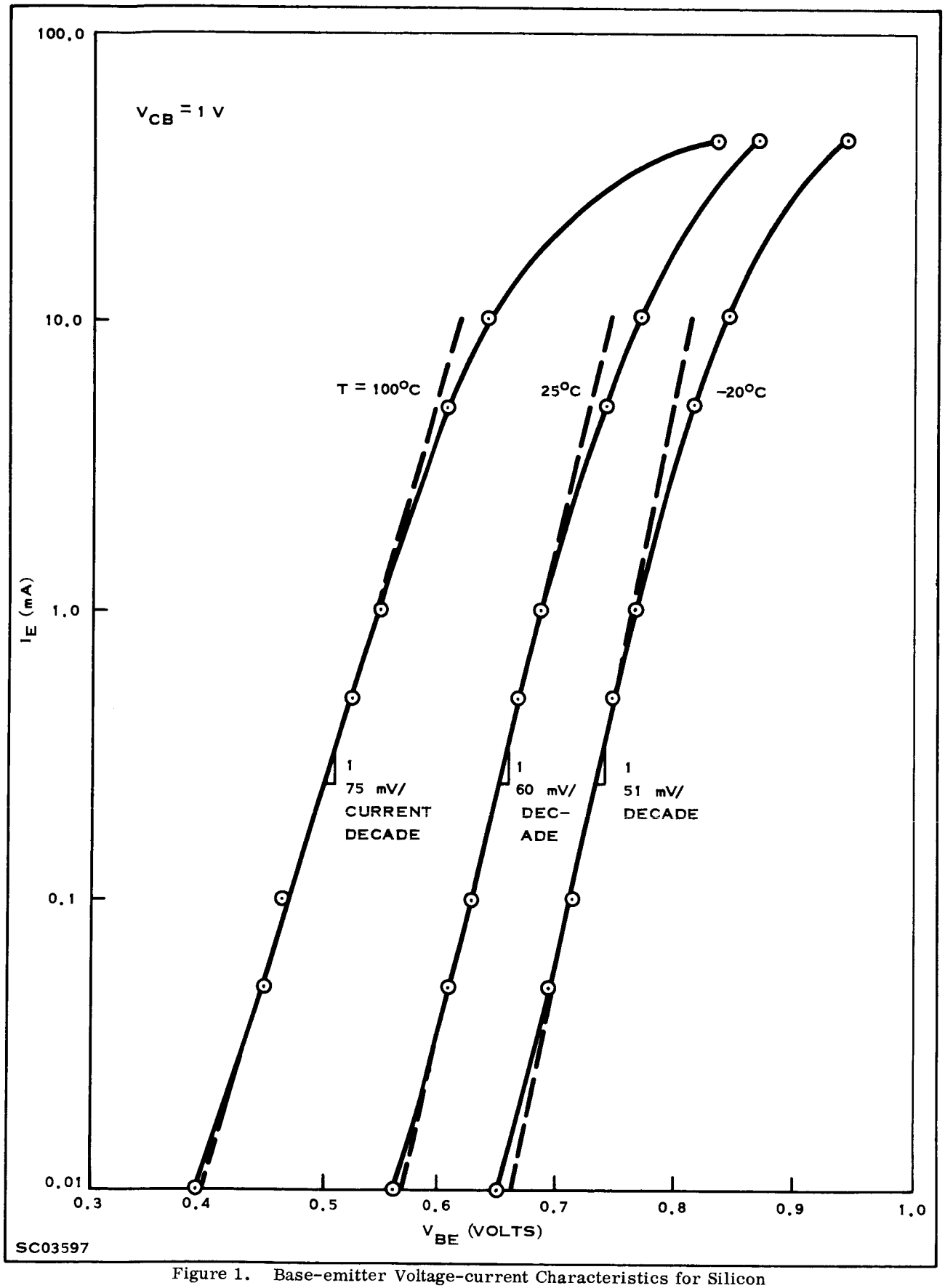

Figure 1. Base-emitter Voltage-current Characteristics for Silicon Transistor Q1 on SNX1304

Table II. Forward Current Gain Characteristics for Transistors on the SNX1304

Unit	T = -20°C			25°C			100°C		
	β_N I_C = 1 mA	β_N 7 mA	β_N 30 mA	β_N I_C = 1 mA	β_N 7 mA	β_N 30 mA	β_N I_C = 1 mA	β_N 7 mA	β_N 30 mA
Q1	118	118	79	152	159	114	204	222	162
Q2	36	44	35	60	70	57	119	108	102
Q3	133	133	86	173	175	126	212	250	178
Q4	75	80	58	100	109	81	147	156	119
Q5	70	78	55	91	103	77	141	150	113
Q6	80	77	54	102	103	76	133	142	106
Q7	105	93	75	143	152	109	222	222	158

V_{CE} = 2 V

Table III. Resistance at Several Temperatures for Diffused Resistors in the SNX 1304

Unit	Emitter Type			Base Type			Collector Type		
	T = -20°C	25°C	100°C	-20°C	25°C	100°C	-20°C	25°C	100°C
A1	16.4	18.0	19.9	4.36 K	4.50 K	4.98 K	12.7 K	16.6 K	24.6 K
A2	15.3	16.6	18.7	4.34 K	4.52 K	5.04 K	14.2 K	18.5 K	27.8 K
A3	16.0	17.4	19.5	4.80 K	4.96 K	5.62 K	13.0 K	16.9 K	25.3 K
A4	15.6	16.9	19.1						
A5	15.9	17.3	19.4						
A6	15.9	17.1	19.4						
A7	15.6	16.8	18.7						
A8	15.7	16.7	19.1						
B1	24.5	26.4	30.5						
B2	22.5	24.5	28.2						
B3	24.0	26.1	29.8						
B4	23.0	25.1	28.7						
B5	23.5	25.6	29.3						
B6	23.6	25.9	29.2						
B7	22.6	24.7	28.1						
B8	23.0	24.6	28.4						

Values in Ohms

The forward current gains of several high gain phototransistors used in a previous type of emitter diode-Si phototransistor pair were measured at several temperatures. Data is given in Table IV.

The forward voltage-current characteristics of the planar diffused GaAs emitter diodes in several SNX1304 devices at -20, 25, and 100°C are given in Table V.

Table IV. Forward Current Gains of Phototransistors

Unit No.	β_N at I_C = 1 mA	β_N at 5 mA	β_N at 10 mA	T °C
1	417	495	488	-20
2	400	467	465	-20
3	200	296	320	-20
1	527	641	625	25
2	500	618	599	25
3	263	368	396	25
1	769	894	820	100
2	769	862	787	100
3	385	513	549	100

V_{CE} = 6 V

Table V. Forward Voltage-Current Characteristics of GaAs Emitter Diodes

	T = -20° C				T = 25° C				T = 100° C			
Unit No.	V_F at I_D=1mA	V_F at 5 mA	V_F at 10 mA	V_F at 40 mA	V_F at 1 mA	V_F at 5 mA	V_F at 10 mA	V_F at 40 mA	V_F at 1 mA	V_F at 5 mA	V_F at 10 mA	V_F at 40 mA
1	1.145	1.215	1.255	1.42	1.075	1.15	1.19	1.37	0.96	1.04	1.085	1.265
2	1.16	1.21	1.23	1.315	1.07	1.14	1.17	1.26	0.96	1.04	1.08	1.18
3	1.16	1.21	1.235	1.34	1.065	1.13	1.165	1.27	0.96	1.045	1.085	1.205
4	1.155	1.22	1.27	1.44	1.07	1.14	1.18	1.36	0.955	1.04	1.085	1.23
5	1.16	1.22	1.25	1.385	1.075	1.145	1.19	1.365	0.96	1.04	1.08	1.20
6	1.15	1.215	1.26	1.39	1.065	1.13	1.17	1.32	0.96	1.04	1.085	1.24
7	1.14	1.20	1.24	1.365	1.065	1.135	1.17	1.27	0.95	1.03	1.07	1.175
8	1.15	1.205	1.235	1.325	1.07	1.14	1.17	1.27	0.95	1.03	1.07	1.18
9	1.13	1.195	1.235	1.40	1.05	1.12	1.16	1.30	0.935	1.02	1.065	1.20

Values in Volts

B. DRIVER CIRCUIT DESIGN

A number of circuits were examined for use as the driver, according to electrical characteristics described in JPL specification XOY - 50469 - DSN - C and listed in Table VI. Using calculations and breadboard measurements, one circuit was found acceptable with regard to the emitting diode current in the off and on conditions for all input and supply voltage values. The circuit selected for the driver is shown in Figure 2. Reasonable voltage tolerances for the diodes and transistors at T = -20°C, 25°C, and 100°C, from measurements on the SNX1304, are shown.

Following is a discussion of the driver circuit design using integrated circuit criteria. At -20°C, current in the on-condition is maximum since the diffused resistors have their smallest values at this temperature. This also results in a maximum power dissipation at -20°C. For the specified maximum dissipation value of 200 mW and maximum supply voltage of 4.5V, the maximum design current is 44.4 mA. To maintain a small collector-emitter saturation voltage for this relatively large current, Q2 is designed to have four times the area of Q1.

For physical size considerations on the integrated bars, resistor values at 25°C between about 10 Ω and 200 Ω will be produced with an emitter-type diffusion, to 5 kΩ with a base diffusion, and 5 kΩ to 30 kΩ with a collector diffusion.

Referring to Figure 2, current for the GaAs diode, D2, is largely controlled by the value of R3. Examination of the effect of R3 on I_{R3} gives a good measure of the available I_{D2} and is easily determined using the values in Figure 2. Besides the tolerances in Figure 2, and the rated supply voltage of 4.0 ± 0.5V, values for the relative change in R3 with temperature are needed. It will be shown that R3 requires an emitter diffusion. Considering a fixed contact resistance of 4.2 ohms for the emitter diffused resistors, as previously described, the increase in resistance from -20°C to 25°C was a factor of 1.10 for all 16 resistors measured (within measuring accuracy). Similarly, from -20°C to 100°C, all resistances increased by a factor of 1.29.

The calculated relation of I_{R3} (at -20°) to R3 (at 25°C) is given in Figure 3. The cases of both maximum and minimum available V_{R3} for the tolerance range are shown. These curves describe the effectiveness of setting R3 at 25°C to control the current range. In Figure 4, I_{R3} (-20°C) is given as a function of I_{R3} (100°C), obtained by similar calculations. For I_{R3} (100°C), V_{CC} = 3.5 V is used for describing the minimum current conditions. Thus, Figure 4 relates the maximum and minimum values of I_{R3}.

For power dissipation considerations, I_{D2} (-20°C) ≤ 44.4 mA; and thus, approximately I_{R3} (-20°C) ≤42 mA. Considering the requirements for the phototransistor in a following section, an appropriate minimum I_{D2} (100°C) ≥ 22 mA, or I_{R3} (100°C) ≥ 21 mA. Values from Figure 4 are transposed to Figure 3 to indicate the operating area for these conditions. We see that 25°C values of 78 ≤ R3 ≤ 85 Ω are satisfactory

Table VI. Proposed Electrical Characteristics

Case Temperature (unless specified otherwise); -20°C to +100°C, V_{CC} = 4.0 ±0.5 V					
Parameter	Symbol	Conditions	Value		Units
			Min	Max	
Input Voltage: at "1" level	V_i		3.0	6.0	V
at "0" level	V_i		0	1.0	V
Input Current: at "1" level	I_i	V_i = 6 V		50	μA
at "0" level	I_i	V_i = 0.1 V		-1.0	mA
Output Saturation (ON) Voltage	V_{ces}	V_i = 3.0 V, I_c = 10 mA		0.6	V
Output (ON) Current	I_c	V_i = 3 V, V_{ces} = 0.6 V	10		mA
Output Leakage (OFF) Current	I_{ceo}	V_i = 1 V, V_{ce} = 20 V, Temp. = +25°C		0.1	μA
		Temp. = +100°C		20	μA
Output Breakdown Voltage	BV_{ceo}	V_i = 0 V, I_c = 100 μA	35		V
Isolation Capacitance (between output and all other terminals)	C_{iso}	Freq. = 1.0 kHz		10	pF
Total Switching Times: Turn ON	t_1	V_{CE} = 20 V, $I_{C(peak)}$ = 10 mA		10	μs
Turn OFF	t_2	$V_{i(peak)}$ = 3 V		100	μs
Noise Transmissibility	V_n	V_{CE} = 20 V, R_C = 10 kΩ, $V_{e(peak)}$ = ±5 V, $t_r = t_f \leq$ 20 ns, $C_{(probe)} \leq$ 10 pF		2.0	V
Power Dissipation: Switch ON		V_i = 3 V, I_c = 0		200	mW
Switch OFF		V_i = 0 V, I_c = 0		1.0	mW

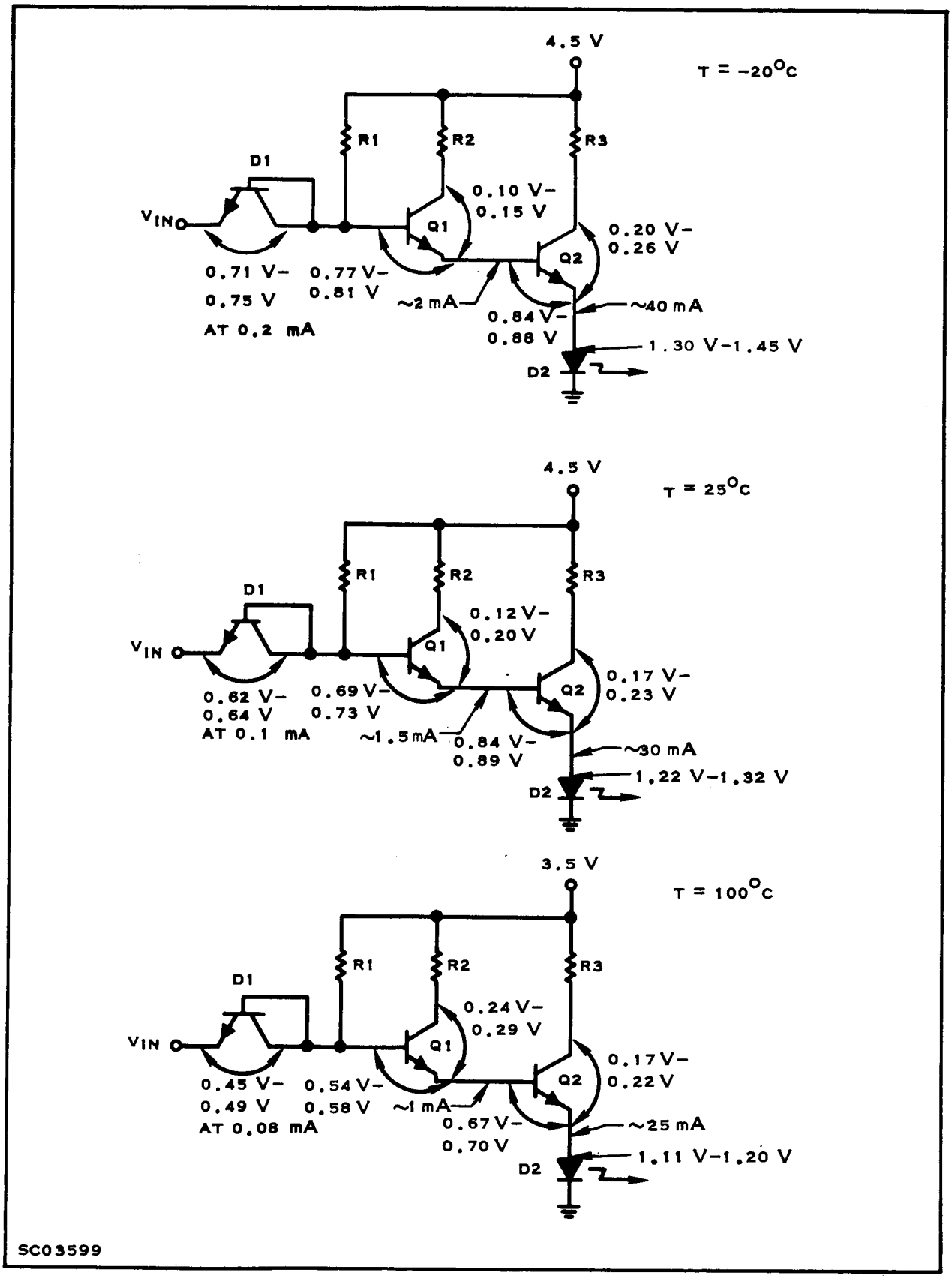

Figure 2. Basic Driver Circuit and Tolerances

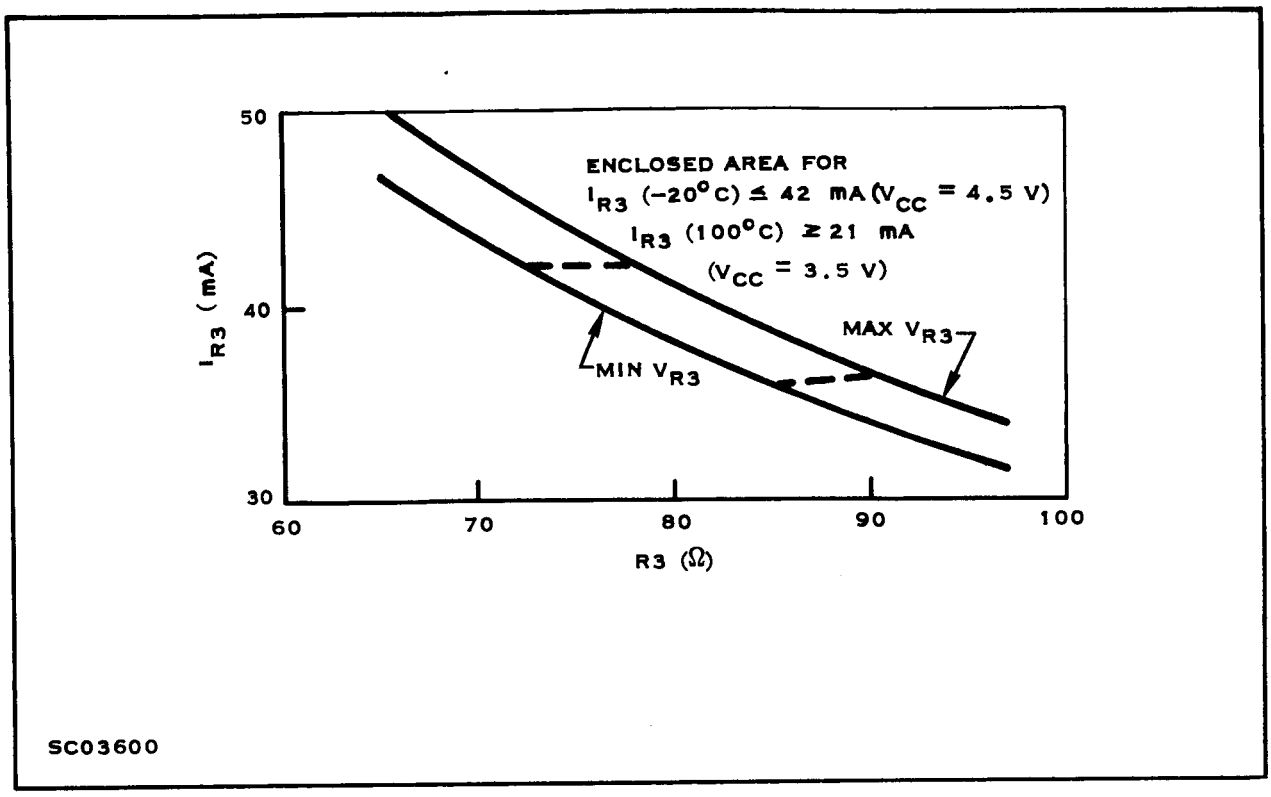

Figure 3. I_{R3} for T = -20°C versus R3 for T = 25°C

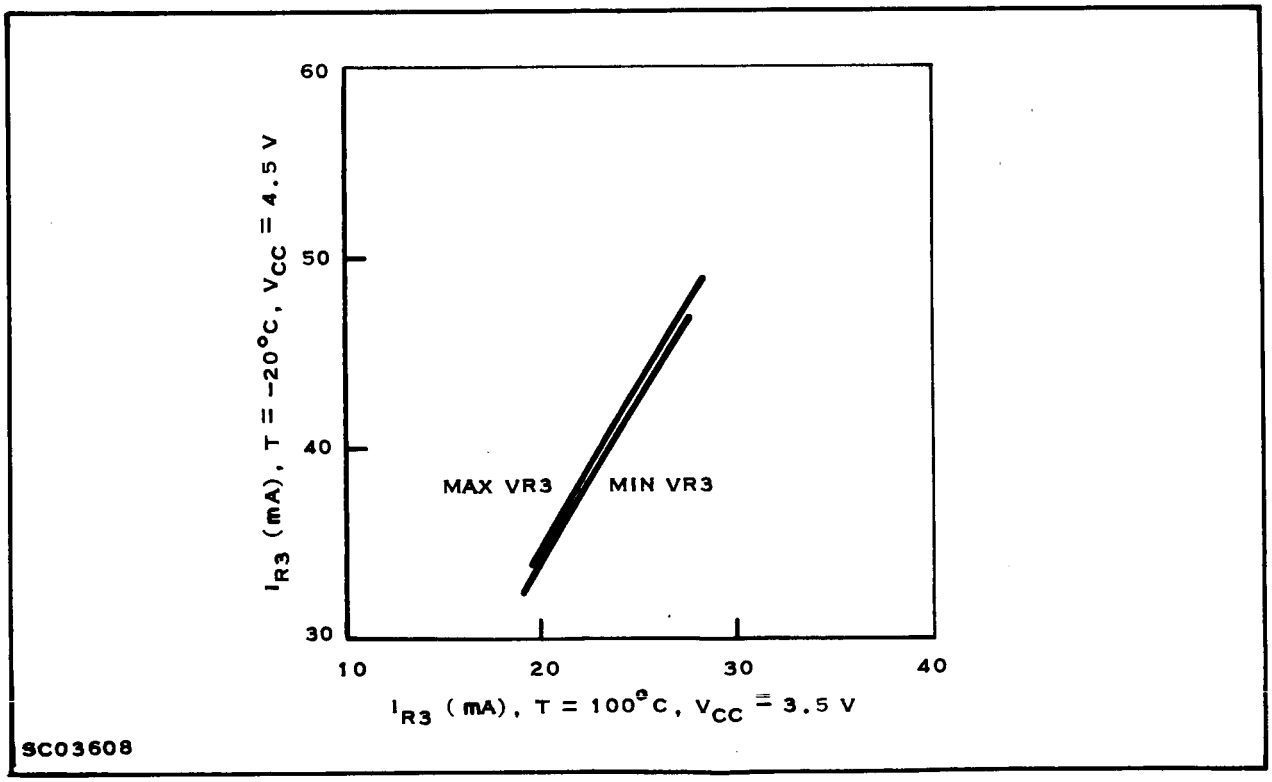

Figure 4. Maximum I_{R3} (T = 20°C, V_{CC} = 4.5V) versus Minimum I_{R3} (T = 100°C, V_{CC} = 3.5V)

for the full voltage tolerance ranges indicated in Figure 2. This is a quite reasonable range. To accomodate the expected ± 15% variation in emitter resistivity, the design value should be 98 Ω and the value may be as great as 113 Ω. Three taps will be required on the resistor to set R3 to within the calculated range. It is planned that the metallization mask will be designed after measuring the resistors, so that individual tapping during fabrication is not required, simplifing the processing considerably. For this to be effective, resistor values should vary within a narrow range, which is the case for a single diffusion run. Metallization design after testing has become a standard procedure in integrated circuits for the design of complex arrays, and this should present no additional problems for the driver circuit.

This technique of adjusting metallization to set the resistance of R3 within a narrow range can also be used for the other resistors. For example, two taps on the collector-diffused resistor can reduce the production tolerance of ± 30% to a maximum of ± 15% for R1. Similarly, two taps on a base-diffused resistor reduces the expected ± 15% production variation to about ± 8% for R2.

With the resistance tolerances discussed above, the design of the driver circuit can be completed. Using a maximum I_{R2} = 2 mA at -20°C, $R_2 \geq 1.13$ k; using the maximum V_{R2} from Figure 2 and for a ± 8% tolerance, 1.13 k ≤ R_2 ≤ 1.32 k. In this case, 1.53 mA ≤ I_{R2} ≤ 2.0 mA (and $I_{D2} \leq 44.0$ mA) for the range of tolerances. For total power in the off-condition at less than 1 mW at -20°C with V_{CC} = 4.5 V, I_{R1} ≤ 0.222 mA and $R_1 \geq 17.1$ k. For the ± 15% tolerance, 17.1 k ≤ R_1 ≤ 22.6 k. For the on-condition at T = -20°C and V_{CC} = 4.5 V, $I_{B(Q1)} \geq 0.060$ mA for which $I_{C(Q1)}$ ≤ 1.83 mA and current gain $A_{1(Q1)} \leq 30.5$. Since $I_{C(Q1)} \geq 1.53$ mA and $I_{C(Q2)} \leq 42$ mA, then $A_{I(Q2)} \leq 27.4$.

This design assumes that both transistors remain in saturation. For the integrated circuit transistors described previously for T = -20°C, one had an (unsaturated) $H_{FE} \approx 36$, and for all others $H_{FE} \geq 75$. Lower H_{FE} transistors in the saturated circuit will tend to have a (compensating) greater collector-emitter voltage. Even if Q1 is not in saturation, a safety margin is designed for Q2 (with $A_{I(Q2)} \leq 27.4$) so that Q2 will remain in saturation.

Because the Photon-Coupled Isolation Switch will be exposed to radiation, it would be well to allow for increased transistor leakage by incorporating a resistor from the base of Q2 to ground. A value at -20°C ≥ 11.7 k would allow a shunt current of up to 0.2 mA. Using a collector-diffused resistor for this high resistance value, the design value (at -20°C) should be 15.1 k with a ± 30% tolerance. This should reduce $I_{B(Q2)}$ by no more than 10%, increasing the required maximum current gain for Q2 to 30.4.

The conditions for T = 100°C must be considered. An examination of Figures 3 and 4 indicates that, for the design range, 21 mA ≤ I_{R3} (100°C) ≤ 24.3 mA. With increasing temperature from -20°C to 100°C, the base diffused resistor R2 increases by a factor of 1.16, and 1.31 k ≤ R2 ≤ 1.53 k. Similarly, collector-diffused R1 and R4

(shunt-resistor) increase by a factor of 1.65. Therefore, 33.3 k ≤ R1 ≤ 44 k and 22.6 k ≤ R4 ≤ 38 k. Using the tolerances in Figure 2 for the on-condition, $I_{B(Q1)} \geq$ 0.046 mA for which $I_{C(Q1)} \leq 1.80$ mA and $A_{I(Q1)} \leq 39$. For the shunt current at 100°C, 0.047 mA ≤ I_{R4} ≤ 0.084 mA. Then, $12 \leq A_{I(Q2)} \leq 14$. Also, $I_{D2} \geq 22$ mA. Since current gain approximately doubles from -20°C to 100°C, no problem exists for saturation at 100°C.

For circuit design at 25°C, R1 and R4 increase by a factor of 1.30 from the -20°C values, and R2 increases by a factor of 1.04. The complete driver circuit (with one input) for T = 25°C is shown in Figure 5.

The preceeding analysis was repeated for V_{CC} = 4.5 V ± 0.5 V to examine the effect on the minimum value for I_{D2} at T = 100°C. In the analysis, the same maximum power dissipation in the on-condition (200 mW) was used. Also assumed were that the percentage acceptable range for R3 was the same as for the preceeding analysis. Because they have very little effect on the result, the same values for R1, R2, and R4 were also used. The result was that I_{D2} (100°C) ≥ 20.1 mA. This compares with the previous minimum value of 22.5 mA with V_{CC} = 4.0 V ± 0.5 V. The latter figure, 22.5 mA, is more desirable, since a smaller minimum current gain for the phototransistor is required.

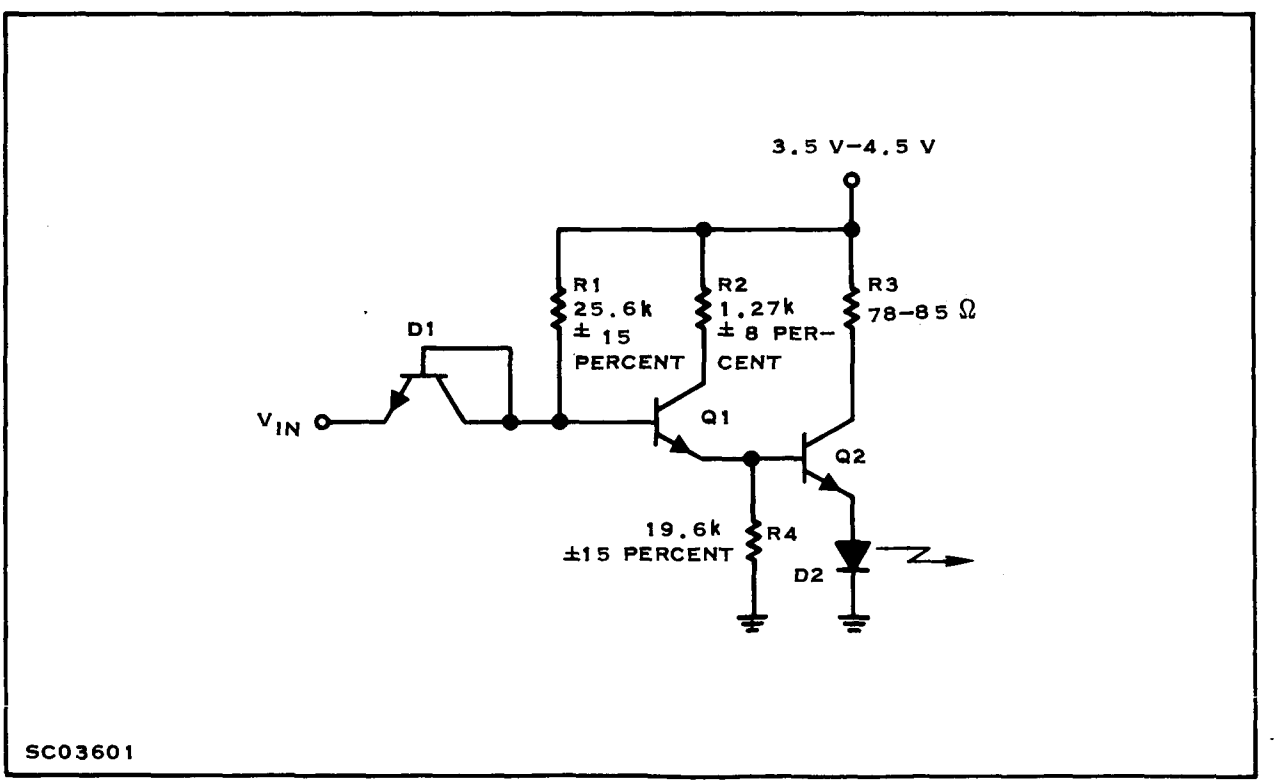

Figure 5. Complete Driver Circuit (One Input)

A first order layout of the driver circuit components and metallization on an integrated circuit bar in a 14 lead 1/8" x 1/4" package is shown in Figure 6. Ten input diodes are shown. One of the inputs has an optional connection to the common point of the input diodes, or to the anode of the light emitter diode.

C. PHOTON– COUPLED PAIR DESIGN

1. Structure

The technique to be used for bonding the GaAs photon emitting diode and Si phototransistor is illustrated in Figure 7. A SeSAs glass, on melting, wets both the GaAs and Si surfaces. The glass acts as both a non-conductive cement and a good optical coupling medium. The requirements for the glass are as follows:

Provides a good mechanical adhesion to GaAs and Si

Relatively transparent for 0.9 mμ photons of GaAs

Good thermal expansion match to GaAs and Si

Bonding temperature compatible with fabrication and reliability

High refractive index (~2.5)

Effects observed for other types of glasses, such as cracking at lower temperatures and softening at higher temperatures, should be minimal with the SeSAs glass for the temperature range of -20°C to 100°C. For added structural rigidity in the SNX1304, a small amount of an epoxy compound is applied across the glass bond.

The layout for the phototransistor is shown in Figure 8. Diffused areas for the base, emitter, collector probe point, and the contact metallization are indicated. A 22 mil diameter window is used in the base area for a good refractive index match to the coupling glass. The GaAs diode is the same as that presently used in the SNX1304.

2. Phototransistor Design

Both the efficiency of the GaAs emitter diode (D2) and the diode bias current decrease with increasing temperature. The result is that the critical temperature for the current gain of the phototransistor is 100°C.

From previous data, the increase in the current gain, H_{FE}, from 25°C to 100°C for the small area transistors on the SNX1304 bar (at 1 mA collector current) was an average factor of 1.5. From the previous tests on the high gain, large area transistors in the GaAs emitter diode-Si phototransistor pairs, the average increase of H_{FE} was about 1.40. For the present phototransistor, then, a factor of 1.4 is reasonable.

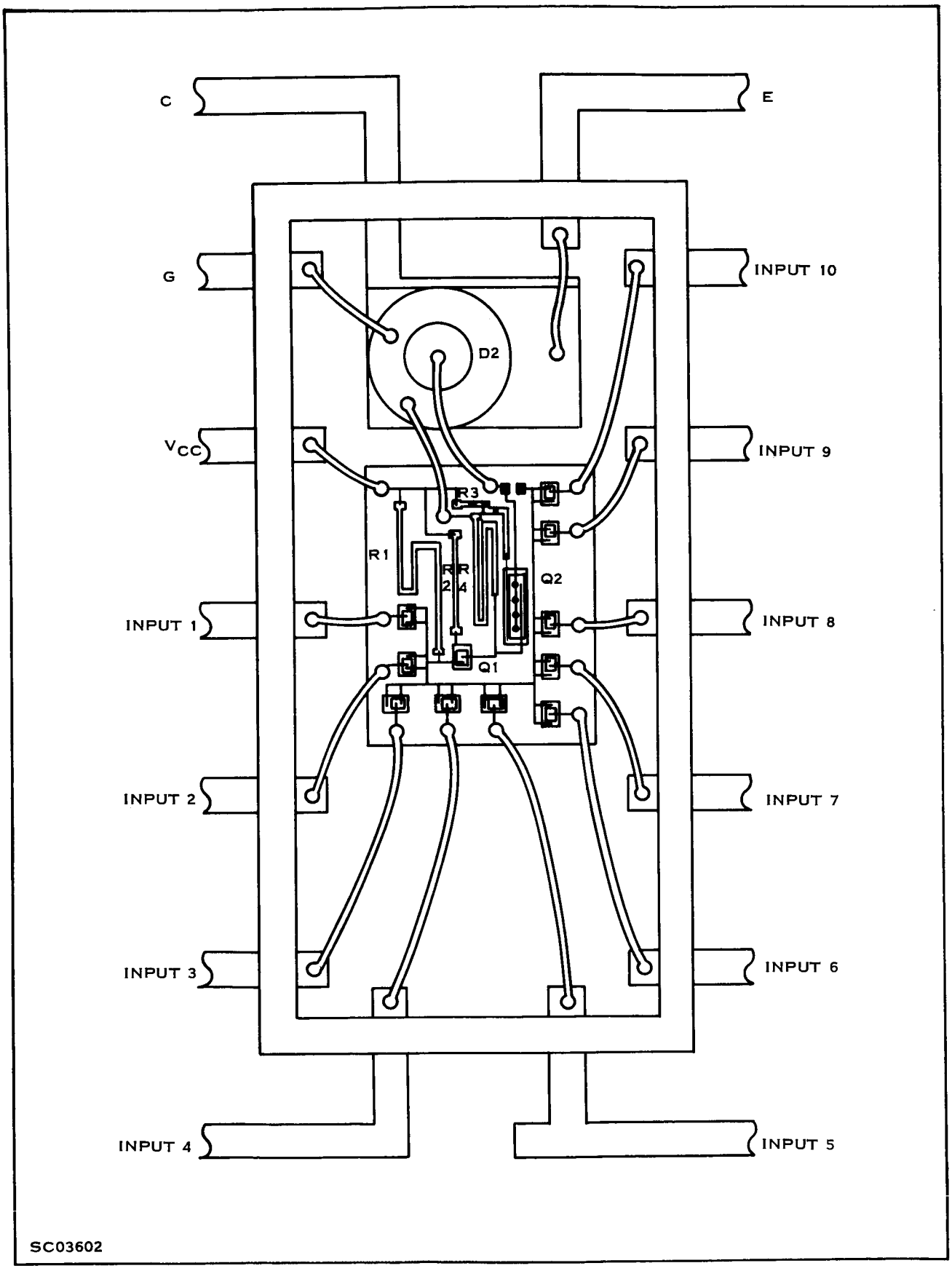

Figure 6. Isolation Switch Layout

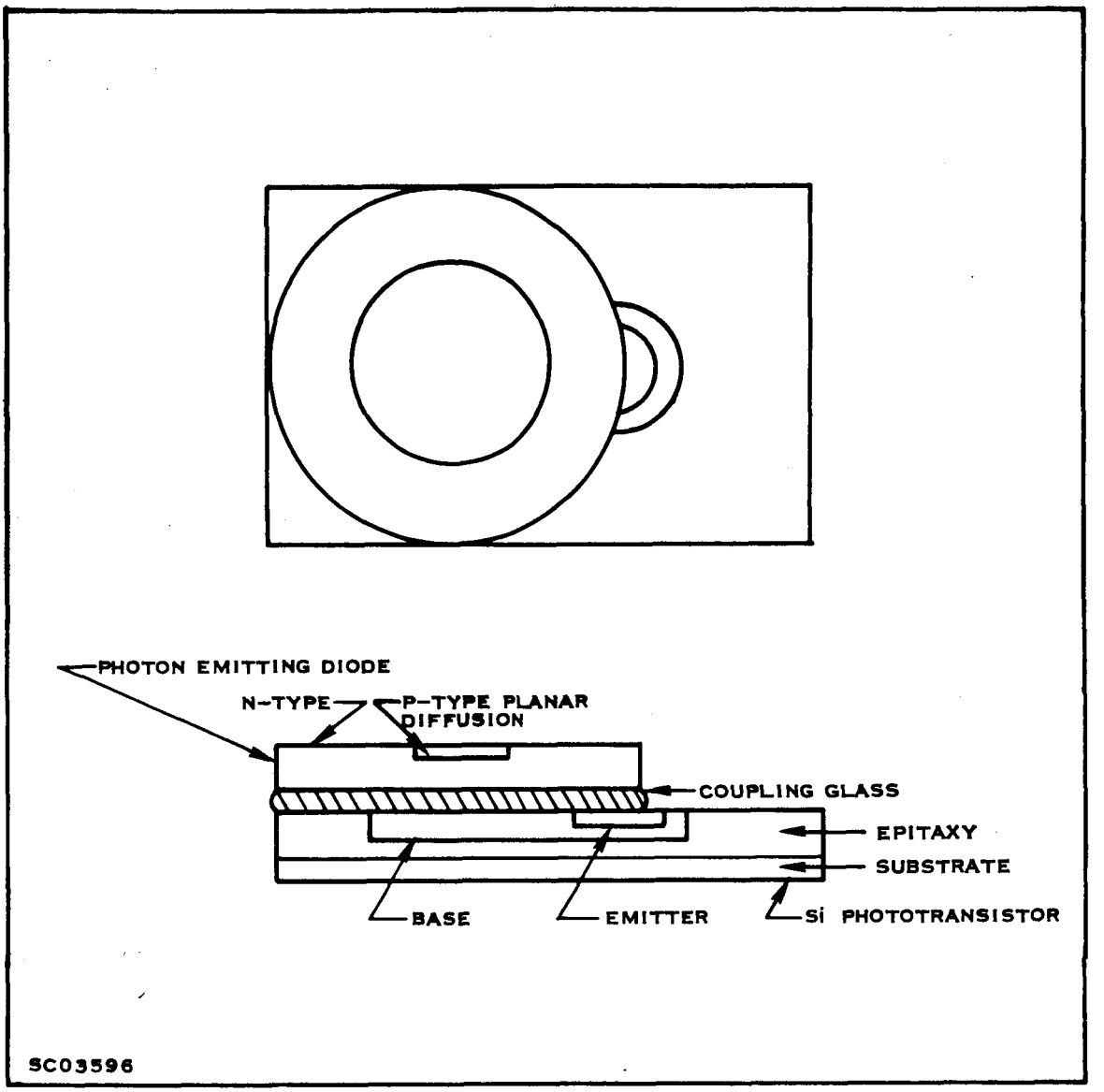

Figure 7. Cross-section of GaAs Switch

From past experience, an equivalent base current of the phototransistor ranging from 20 to 40 μA is obtained at T = 100°C for a nominal I_{D2} = 22 mA. Allowing for a 20% overdrive in base current and for aging or other effects, a 5% decrease in the output for D2 and a 15% fall in the phototransistor current gain, we obtain at a collector current of 10 mA at 25°C for minimum efficiency diodes

$$H_{FE\ (Min)} \approx \frac{10\ mA \times 1.15}{20\ \mu A \times 0.95 \times 0.8 \times 1.4} \approx 540 \qquad (2)$$

Similarly, $H_{FE\ (Min)} \approx 270$ for maximum efficiency diodes. The nominal design objective is H_{FE} = 500. This should result in devices having H_{FE} ranging between about 200 to 700; individual wafers can be probed for selection within a narrower range. This represents a reasonable compromise between H_{FE} and the range for R3.

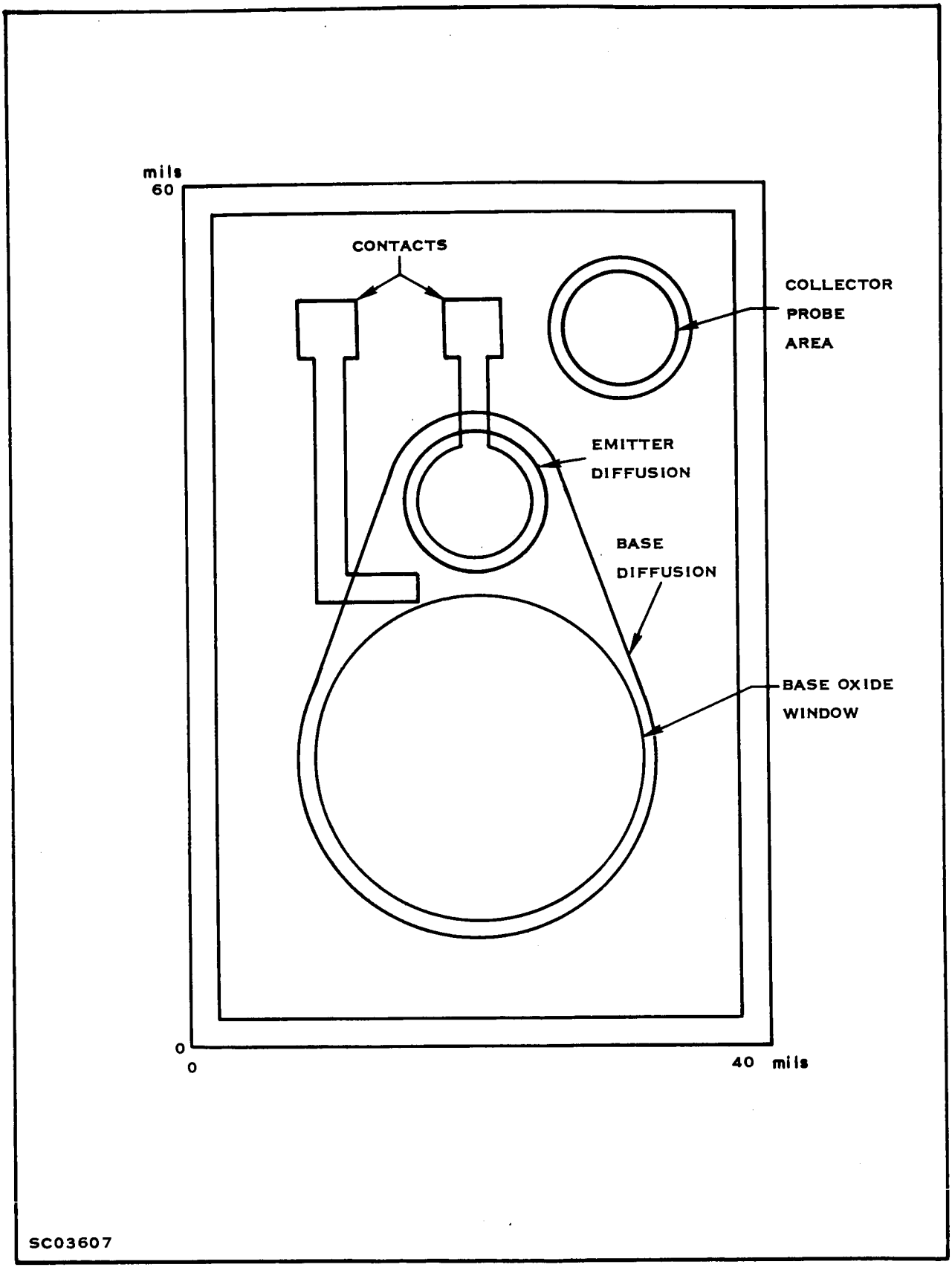

Figure 8. Phototransistor Layout

The approximate expression

$$H_{FE} = \left(\frac{BV_{CBO}}{BV_{CEO}} \right)^4 \tag{3}$$

where

BV_{CBO} = the collector-base breakdown voltage

BV_{CEO} = the collector-emitter breakdown voltage

and data from J. Shields[4] were used to obtain the graph of current gain as a function of collector impurity concentration and BV_{CEO} shown in Figure 9.

The transistor series resistance, R_C, is given by

$$R_C = \frac{\rho_C t_C}{A_E} \tag{4}$$

where

ρ_C = the collector resistivity

t_C = collector thickness

A_E = the emitter area.

Using the emitter diameter of 10 mils and a 0.7 mil thick collector region, the resistance for $\rho_C = 10\ \Omega$ cm ($N_C \approx 5 \times 10^{14}$ cm^{-3}) is about 18 ohms. This corresponds to a maximum collector-emitter saturation voltage of 0.18 volt at 25°C. The collector resistivity is approximately double[5] its value at 100°C, for which the saturation voltage has its greatest value of 0.36 volt, compared to the specification of 0.6 volt. The shaded area in Figure 9 encloses ranges of the H_{FE} between 400 and 800, transistor series resistance below 18 ohms and BV_{CEO} greater than 45 volts (35 V specification). This represents the transistor design area. The indicated collector concentration is 5×10^{14} to 1×10^{15} cm^{-3} (5 to 10 ohm-cm).

The design criteria for the transistor capacitances are discussed in the following section.

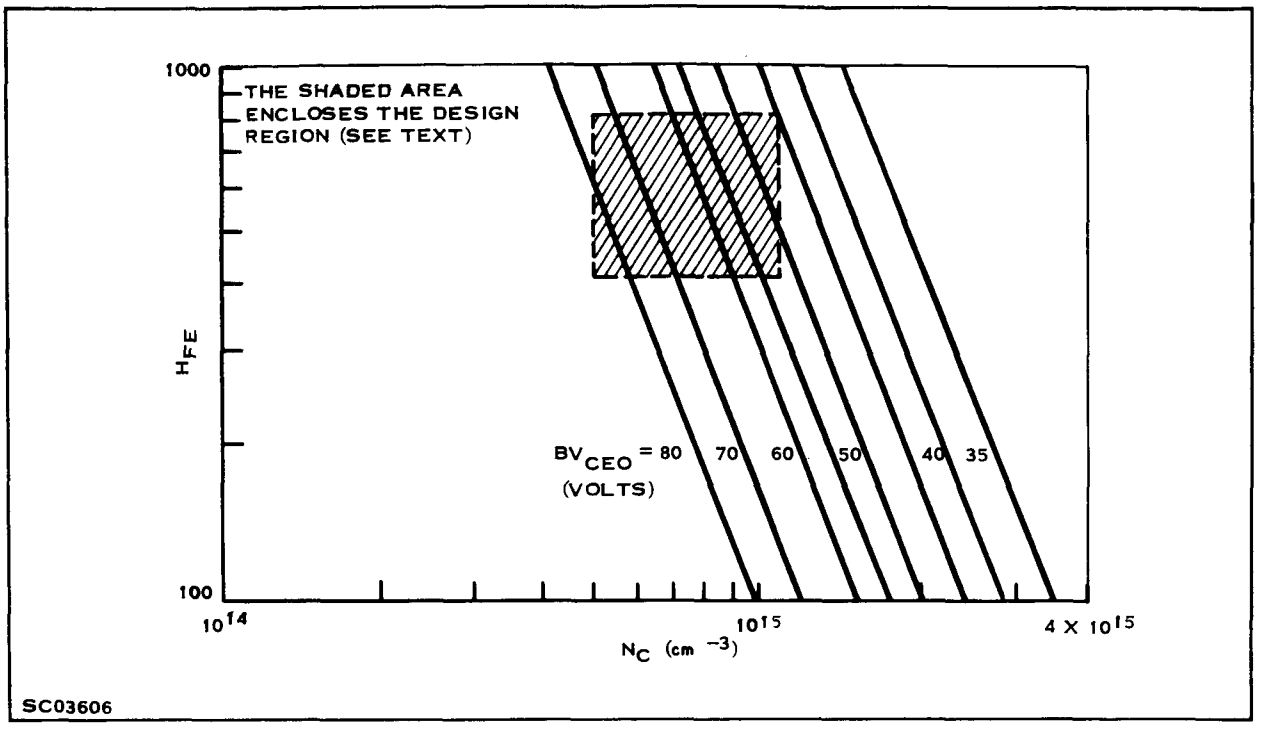

Figure 9. Phototransistor Current Gain as a Function of Collector Impurity Concentration and Collector-emitter Breakdown Voltage

3. Noise Transmissibility

In the off-condition, one requirement for the photon-coupled isolation switch is the insensitivity of the voltage at the collector of the phototransistor to noise pulses at the emitter. In order to establish an appropriate equivalent circuit for the phototransistor under these conditions, the collector transient voltages of a number of transistors were measured, using the circuit in Figure 10.

If no transistor action were involved, the expected transistor equivalent circuit would consist simply of the collector-base and emitter-base p-n junction capacitances (C_{CB} and C_{EB}, respectively). Table VII lists the measured C_{CB} (at 20 volts reverse bias), C_{EB} (at zero bias), and H_{FE} (at I_C = 10 mA, V_{CE} = 5 V) for several transistors. Also indicated are the measured collector peak transient voltages, v_C. Practically identical values of v_C were obtained for positive and negative pulses at the emitter.

Measured v_C for an open-jig and for a 10 pF capacitor inserted between the collector and emitter terminals of the jig are also indicated in Table VII. The latter were used in determining the jig parasitic capacitances. The equivalent circuit used in calculating v_C is shown in Figure 11. In the Figure, C_1 is a jig capacitance and C_2

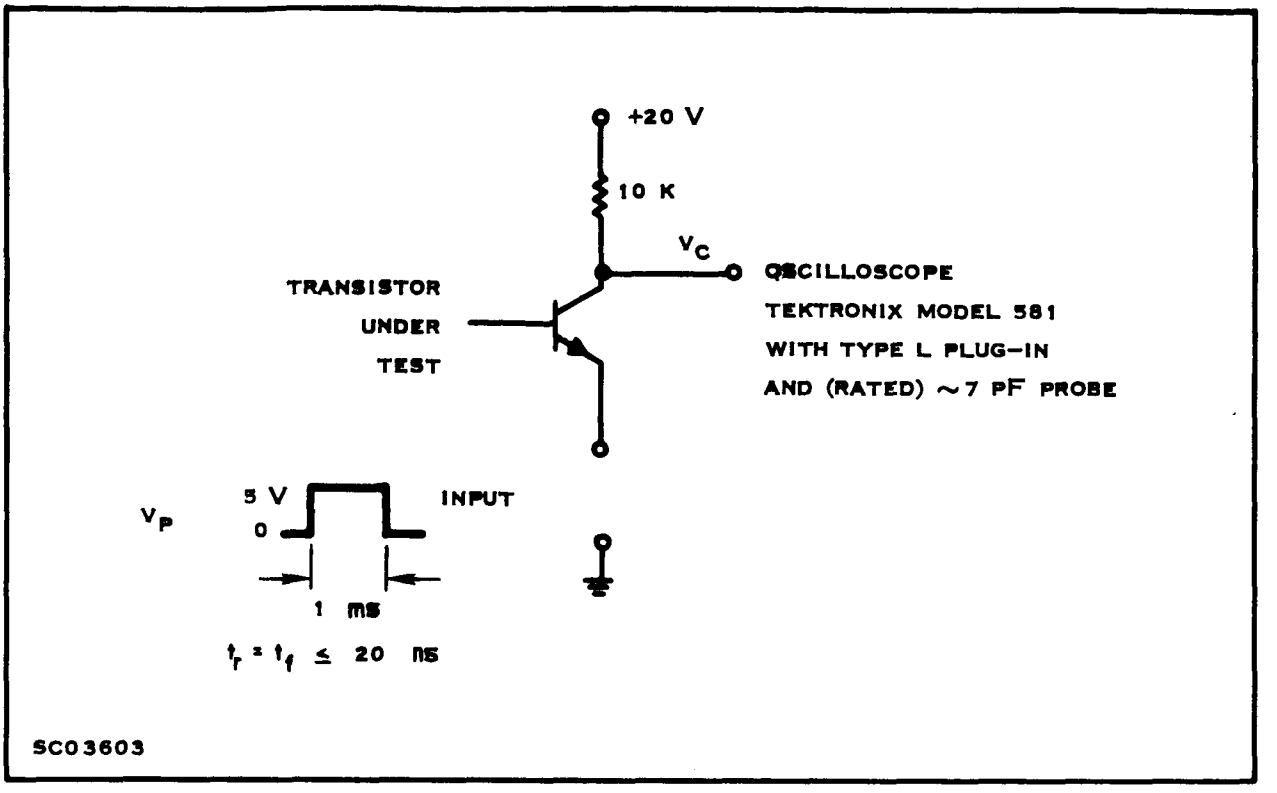

Figure 10. Circuit for Measuring Noise Transmissibility

combines jig shunt capacitance and oscilloscope probe capacitance. These are given by the simultaneous equations

$$v_{C(o)} = v_P \left(\frac{C_1}{C_1 + C_2} \right) \tag{5}$$

$$v_{C(10\ pF)} = v_P \left(\frac{C_1 + 10\ pF}{C_1 + C_2 + 10\ pF} \right) \tag{6}$$

where

$v_{C(o)}$ = the collector peak transient voltage for an open jig socket

$v_{C(10\ pF)}$ = the transient with the 10 pF capacitor in the jig

v_P = the 5 V pulse input

at the emitter. Using the measured values, we obtain, on substitution into Equations (5) and (6), $C_1 = 1.2$ pF and $C_2 = 16.8$ pF.

Table VII. Data for Noise Transmissibility Study

Transistor	V = 0 CEB (pF)	V = 20 V C_{CB} (pF)	I_C = 10 mA V_{CE} = 5 V H_{FE}	Meas V_C (V)	Calc V_C (V)
2N656(1)	125.0	28.0	26	2.8	3.0
2N656(2)	94.0	35.0	18	3.0	3.2
2N1507(1)	64.2	12.5	116	2.2	2.2
2N1507(2)	62.0	14.5	167	2.2	2.3
2N1507(3)	53.7	12.1	238	2.1	2.1
2N1711	62.1	12.8	141	2.15	2.2
2N3420(1)	860.0	92.0	47	4.2	4.2
2N3420(2)	886.0	87.5	46	4.2	4.2
PCT No. 13	7.2	8.0	308	1.2	1.2
OPEN				0.33	
10 pF				2.0	

A general formula for calculating the peak transient voltage for a transistor, derived from Figure 11, is

$$v_C = \frac{v_P \left[C_1 \left(C_{CB} + C_{EB}\right) + C_{CB}\, C_{EB}\right]}{\left(C_1 + C_2\right)\left(C_{CB} + C_{EB}\right) + C_{CB}\, C_{EB}} \qquad (7)$$

Calculated values of v_C for each transistor are given in Table VII. In Figure 12, measured v_C is plotted against calculated v_C. The good agreement indicates the equivalent circuit used is adequate; therefore, only the junction and circuit capacitances are involved in noise transmissibility.

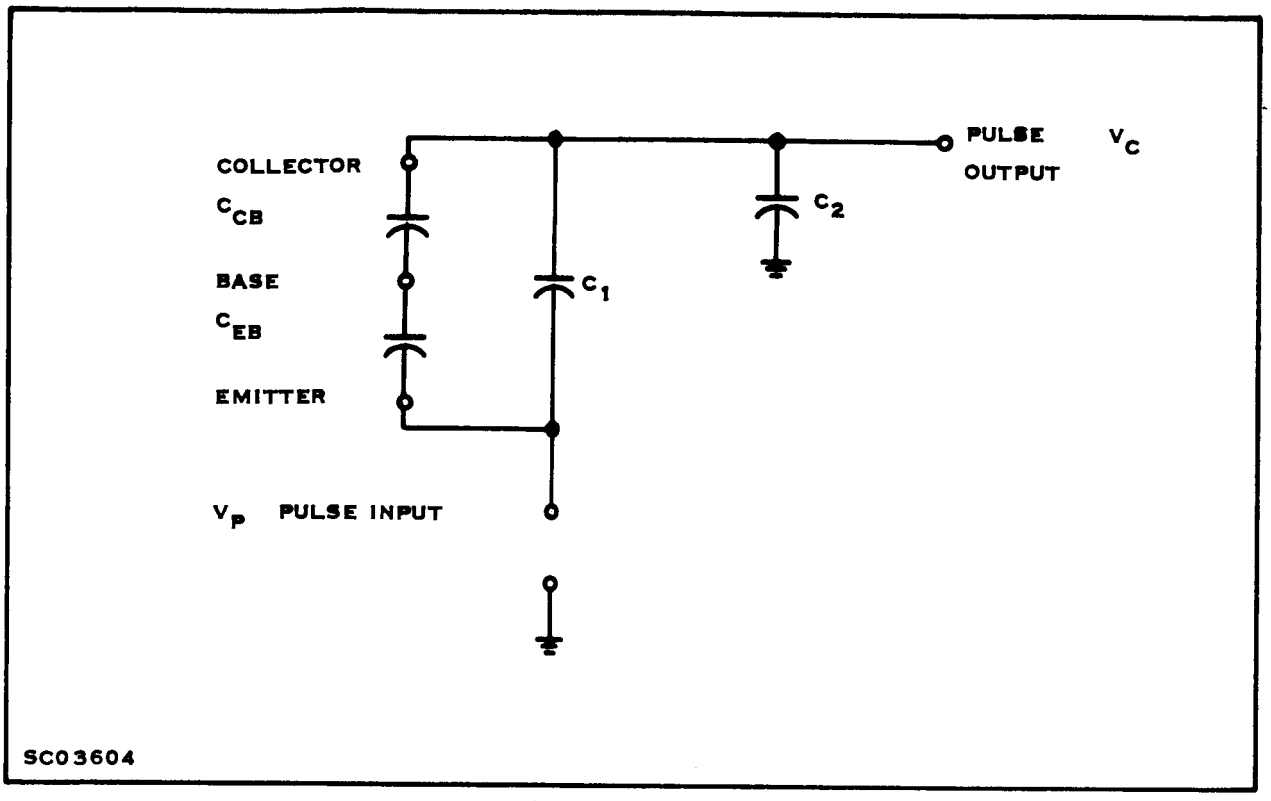

Figure 11. Equivalent Circuit Used in Calculating v_C

A test of the effect of the capacitance between the GaAs emitting diode and the phototransistor was made using PCT No. 13, a high gain, low capacitance phototransistor. For this transistor, additional capacitances up to 30 pF were connected into the circuit between the transistor base and ground. Effects of transistor action were not observed for either positive or negative pulses. Stray capacitances in the photon-coupled isolation switch to the base should be only about 1 pF, based on measurements on the SNX1304.

Using a collector potential of 20 volts (for which noise transmissibility is measured), the collector region depletes about 0.20 mils for a collector resistivity (P_C) of 5 ohm-cm and about 0.28 mils for 10 ohm-cm at 25°C. The collector-base junction area in Figure 8 is about 630 mil^2. The base capacitance C_B is given by

$$C_B = \frac{\epsilon_o \epsilon \ (630 \text{ mil}^2)}{0.20 \text{ mil}} = 8.4 \text{ pF} \qquad (8)$$

where

$\epsilon_o \epsilon$ = the permitivity of silicon.

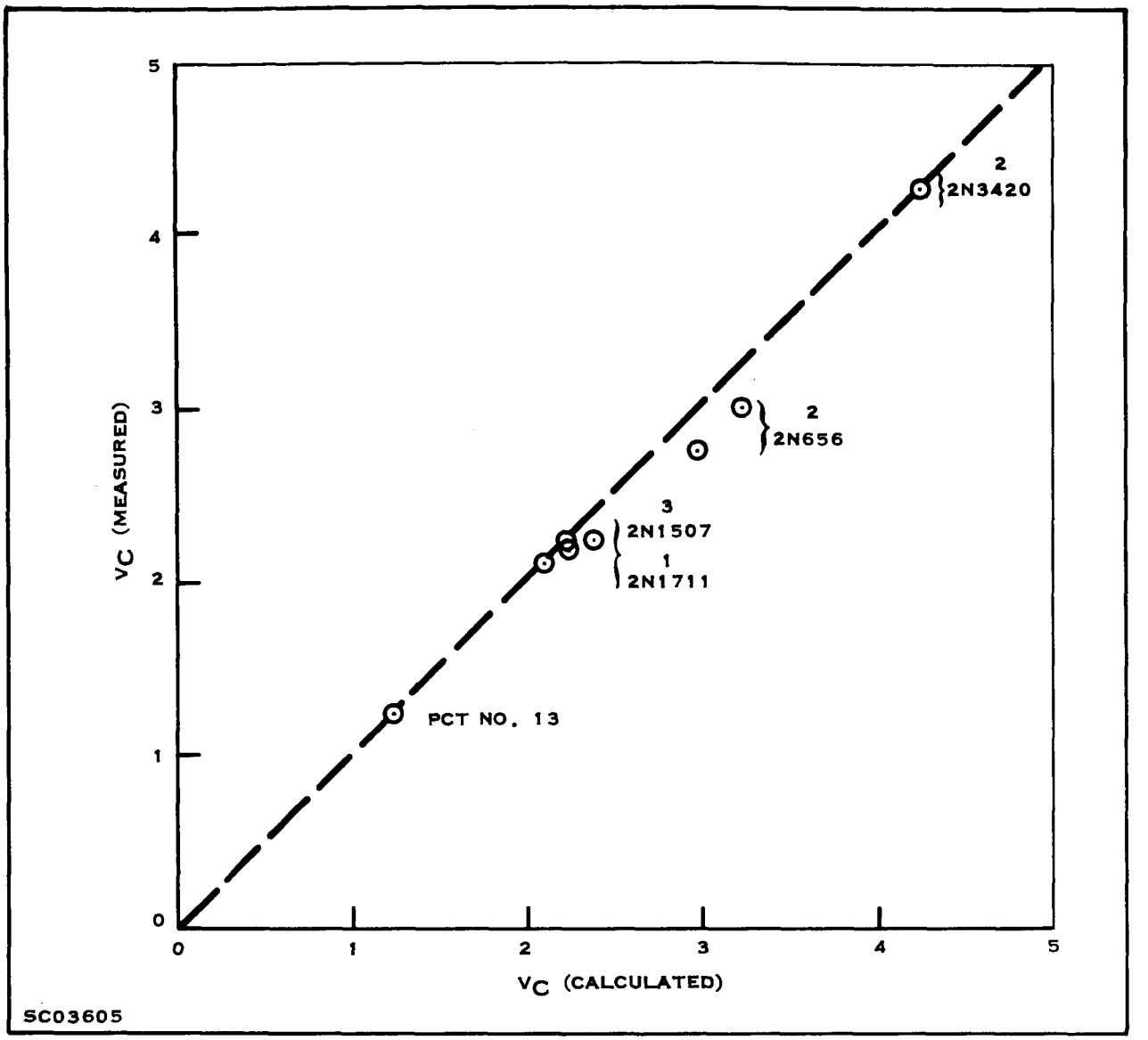

Figure 12. Comparison of Measured and Calculated Noise Transmissibility

Substituting this value into Equation (7), and using C_2 = 10 pF for the oscilloscope capacitance and C_1 = 0 to neglect stray capacitances, the emitter-base junction capacitance may be as great as 32.3 pF without exceeding the specified maximum noise transmissibility of 2 volts. This capacitance is determined largely by the base concentration below the emitter region.

D. RADIATION TESTS

Measurements were made on numerous devices submitted for proton radiation. The devices included 15 discrete GaAs light emitting diodes (5 each of types PEX1004, PEX1201, and TIXL02), 3 GaAs diode-Si phototransistor pair (type PEX4001), and 5

diode-transistor integrated circuit logic gates (type SNX1503). The devices were numbered as follows:

Unit Nos.	Type
1-3	GaAs-Si Pair
4-8	PEX1004
9-13	PEX1201
14-18	TIXL02
19-23	SNX1503

The proton radiation consisted of the following:

Unit Nos	Radiation Dosage
1, 5, 8, 10, 11, 14, 18, 19, 20.	1.2×10^{10} protons/cm^2 at 30 MeV.
2, 4, 12, 17, 21.	1.1×10^{10} protons/cm^2 at 60 MeV.
3, 6, 9, 15, 22.	1.1×10^{10} protons/cm^2 at 100 MeV.
7, 13, 16, 23.	1.6×10^{10} protons/cm^2 at 140 MeV.

Table VIII describes the data for the GaAs emitters, which consist of light output data, forward voltage, and reverse breakdown voltage. In each case little or no change occurred.

In Table IX, data for the emitter-detector pairs include transistor current gains and overall current gains for several collector currents and saturation voltages. Small decreases in the transistor current gains are indicated only for the lower current. Transistor saturation voltage data unfortunately included 2 pre-radiation values which were in error and were excluded. The one other set of saturation data (for Unit No. 1) are in close agreement.

Data in Table X for SNX1503 logic gates indicate practically identical results before and after radiation.

Table VIII. Characteristics of GaAs Light Emitter Diodes Before and After Proton Radiation

Unit No.	Pre-Radiation Tests					Post Radiation Tests				
	I_λ at I_F=0.1A	I_λ at 0.5A	V_F at 10 μA	V_F at 0.5A	V_R at 10 μA	I_λ at I_F=0.1A	I_λ at 0.5A	V_F at 10 μA	V_F at 0.5A	V_R at 10 μA
4	0.055	0.54	0.78	1.86	14	0.054	0.54	0.77	1.86	14
5	0.115	0.92	0.73	2.40	17	0.102	0.91	0.73	2.22	17
6	0.021	0.20	0.80	1.80	8	0.020	0.19	0.79	1.80	8
7	0.033	0.34	0.78	1.82	7	0.033	0.35	0.74	1.83	7
8	0.048	0.48	0.75	2.15	8	0.047	0.49	0.78	2.14	8
	I_λ at 50 mA	I_λ at 0.1A	V_F at 10 μA	V_F at 0.1A	V_R at 10 μA	I_λ at 50 mA	I_λ at 0.1A	V_F at 10 μA	V_F at 0.1A	V_R at 10 μA
9	0.115	0.32	0.80	1.30	13	0.12	0.32	0.78	1.30	13
10	0.066	0.195	0.78	1.37	10	0.070	0.196	0.76	1.37	10.4
11	0.110	0.275	0.80	1.30	9	0.111	0.273	0.78	1.31	9
12	0.093	0.225	0.80	1.33	11	0.096	0.230	0.79	1.31	11
13	0.180	0.46	0.82	1.33	13	0.182	0.445	0.80	1.32	12.6
	I_λ at 50 mA	I_λ at 0.1A	V_F at 10 μA	V_F at 0.1A	V_R at 10 μA	I_λ at 50 mA	I_λ at 0.1A	V_F at 10 μA	V_F at 0.1A	V_R at 10 μA
14	0.016	0.42	0.62	1.10	5	0.016	0.041	0.62	1.13	4.4
15	0.033	0.074	0.74	1.12	7	0.033	0.073	0.73	1.13	7.3
16	0.032	0.072	0.70	1.13	6	0.033	0.072	0.68	1.13	5.0
17	0.032	0.074	0.70	1.13	7	0.030	0.071	0.55	1.14	2.1
18	0.039	0.086	0.70	1.13	7.7	0.038	0.086	0.70	1.13	7.5

I_λ – solar cell photodetector, short-circuit current in mA

Table IX. Characteristics of GaAs Emitter Diode-Si Transistor Pairs Before and After Proton Radiation

Unit No.	I_B (μA) I_C = 0.1 mA	I_B (μA) at 1 mA	I_B (μA) at 10 mA	I_D (mA) at 0.1 mA	I_D (mA) at 1 mA	I_D (mA) at 10 mA	$V_{CE(sat)}$ (V) at I_D = 20 mA I_C = 10 mA
Pre-radiation Tests							
1	0.20	1.68	15.9	0.675	2.34	10.7	2.23
2	0.19	1.66	17.0	1.13	4.6	23.8	
3	0.63	3.75	26.1	5.2	9.1	22.8	
Post-radiation Tests							
1	0.23	1.80	16.2	0.69	2.43	10.8	2.26
2	0.25	1.75	17.2	1.18	4.8	24.0	16.0
3	0.60	3.80	26.1	5.2	9.1	23.0	14.0

I_B = transistor base current
I_D = GaAs emitter current
V_{CE} = 6 V T = 25°C

Table X. Characteristics of Diode-transistor Logic Gates-type SNX1503, Before and After Proton Radiation

Device	Input Lead	Output Lead	Pre-radiation			Post-radiation		
			V1 (V)	V2 (V)	V3 (V)	V1 (V)	V2 (V)	V3 (V)
19	9	8	1.22	1.58	0.054	1.18	1.60	0.052
	10	8	1.21	1.59	0.054	1.18	1.59	0.052
	12	11	1.21	1.59	0.056	1.20	1.60	0.055
	13	11	1.21	1.59	0.056	1.20	1.60	0.055
20	9	8	1.22	1.59	0.066	1.21	1.61	0.066
	10	8	1.22	1.60	0.066	1.20	1.61	0.065
	12	11	1.21	1.59	0.071	1.20	1.60	0.069
	13	11	1.22	1.59	0.071	1.21	1.60	0.069
21	9	8	1.24	1.61	0.070	1.22	1.62	0.070
	10	8	1.24	1.60	0.070	1.22	1.61	0.070
	12	11	1.24	1.63	0.069	1.22	1.62	0.066
	13	11	1.24	1.62	0.069	1.22	1.62	0.066
22	9	8	1.22	1.60	0.063	1.21	1.60	0.060
	10	8	1.22	1.60	0.063	1.21	1.60	0.060
	12	11	1.23	1.60	0.074	1.22	1.60	0.071
	13	11	1.23	1.60	0.074	1.22	1.60	0.071
23	9	8	1.21	1.60	0.057	1.21	1.60	0.055
	10	8	1.20	1.61	0.057	1.24	1.60	0.054
	12	11	1.21	1.76	0.055	1.20	1.61	0.052
	13	11	1.21	1.74	0.055	1.20	1.62	0.052

V_{CC} = 4.75 V

V_2 - Input turn-on threshold, output = V3 = 0.002 V above full-on output

V1 - Input turn-off threshold, output = 4.70 V.

In conclusion, no significant changes in the important device parameters are indicated for proton radiation.

SECTION III

CONCLUSIONS AND RECOMMENDATIONS

The design and breadboarding of the driver circuit has been completed.

The Si phototransistor has also been designed, and diffusion masks should be available early in the second quarter. As soon as satisfactory phototransistors are produced, GaAs photon emitting diode-Si phototransistor pair will be fabricated and submitted.

Data on discrete GaAs emitting diodes, photon coupled pair, and integrated circuit logic gates indicate no significant degradation of performance by proton radiation.

SECTION IV

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