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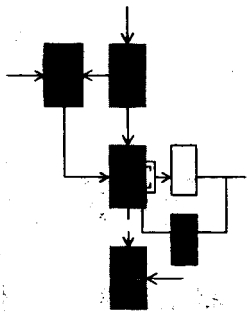

HIGH-EFFICIENCY D-C TO D-C CONVERTER-REGULATORS

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ABSTRACT

D-c to d-c converter regulators described in this report use a variable-frequency control with flyback voltage conversion to obtain regulated output voltage and high efficiency over a wide range of output power. Pulsewidth is varied to maintain output power over a wide range of input voltages.

Experimental circuits have shown conversion efficiencies near 85 percent over a 100:1 range of output power. Flyback voltage conversion results in a small, lightweight package; a 300-watt supply weighs less than five pounds, without housing.

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A. INTRODUCTION

Experiments conducted on spacecraft often require well-regulated d-c supply voltages. A typical spacecraft prime power supply consists of a battery providing an unregulated output voltage. The usual approach for supplying regulated voltages of various values from an unregulated source is by means of a d-c to d-c converter-regulator. Conventional converter-regulators consist of a voltage pre-regulator followed by a square-wave-oscillator converter and filter combination.[1,2*]

Because on-board spacecraft power is limited, a premium is placed on efficient conversion. The input-to-output power-conversion efficiency of the conventional converter is typically between 70 and 80 percent at full output power, but drops off to approximately 50 percent at one-tenth full output power. This lower efficiency at fractional loads occurs because approximately 10 percent of the full output power is consumed by the square-wave oscillator in transformer and switching losses, regardless of the power being delivered to the load, even down to a stand-by or no-load condition. This efficiency loss is not important if the output power required is constant and remains near full load, but if an electronic system has input power requirements that vary widely with time, an efficiency degradation imposes a severe penalty on either operating life or main power supply weight.

A spacecraft radar system is an example of a system in which the power required may vary from hundreds of watts to tens of watts.[3] If a conventional converter-regulator is employed, the stand-by power requirements of the converter system would be greater than the average power requirement of the radar. A radar, or any system which has widely varying power requirements, will benefit from a d-c to d-c converter-regulator which has high efficiency over a wide range of output power. Presented here is a design technique for achieving this efficiency characteristic. The design has been applied to converter

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*Superscripts refer to numbered items in the Bibliography.

regulators delivering maximum output power ranging from 1 watt to over 250 watts. These converter regulators use less than 1 percent of their full load output power in the unloaded or stand-by condition. The efficiency is greater than 80 percent over a 100:1 range of output power.

B. DESIGN CONCEPT

A conventional d-c to d-c converter exhibits efficiency loss at low output power primarily because the square-wave oscillator maintains a fixed frequency, regardless of the power transferred to the load. Thus transformer and switching losses remain essentially constant, independent of current drawn from the output terminals.

A block diagram of a converter-regulator in which stand-by losses are minimized is shown in Fig. 1. In this system, losses

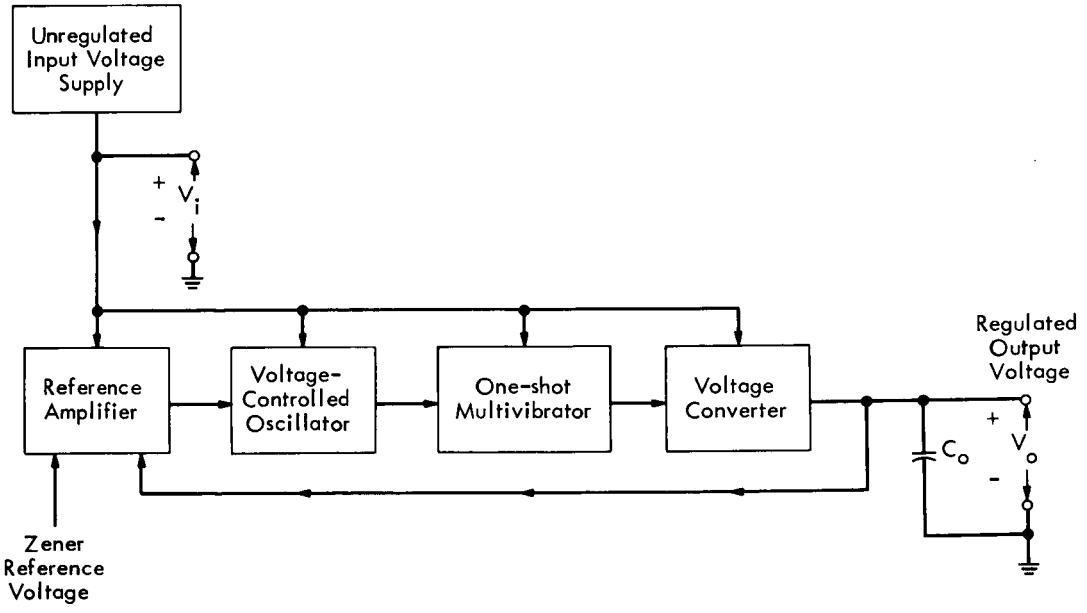


Fig. 1. System Block Diagram

are kept to a minimum because energy is transferred to the output capacitor only when required to maintain the output voltage at the

desired level. If the output capacitor is charged to the desired voltage, then any current drawn by a load acts to decrease the voltage on the output capacitor. The reference amplifier at left in Fig. 1 senses any change in output voltage by comparing the output voltage to a temperature-stable zener reference. A difference voltage due to a decrease in the output voltage is used to vary the frequency of the voltage-controlled oscillator. The voltage-controlled oscillator output is a short pulse which triggers the one-shot multivibrator. The multivibrator generates a constant-amplitude pulse of known time duration, which drives the voltage converter, transferring a pulse of energy onto the capacitor to reestablish the desired output voltage. The greater the output current drain, the more frequently the one-shot multivibrator is fired. At no load the multivibrator frequency is sharply reduced; it is fired only to replace internal circuit losses. The feedback control action is fast enough, and the energy transfer per pulse is small enough, so the d-c output voltage is regulated within a few millivolts of the desired voltage.

It also is desirable to maintain design output power, even while the unregulated main power supply voltage is falling off. In this system, multivibrator pulsewidth is varied by the unregulated input voltage in order to maintain a constant energy per pulse transferred to the output capacitor. When the unregulated input voltage drops, the multivibrator pulse width increases so that the total energy of each pulse remains constant. (This matter is discussed in detail in Appendix A.) Thus the energy transferred to the capacitor remains constant for each pulse.

The voltage-controlled oscillator, the multivibrator, and the reference amplifier are all low-power circuits designed for minimum power dissipation. Almost all of the conversion losses are in the final voltage-converter stage, and these losses are directly related to frequency. The result is that high conversion efficiency can be realized over wide ranges of power output.

C. CIRCUIT DESCRIPTION

Figure 2 shows a simplified circuit for the voltage converter, which can be thought of as a d-c to d-c transformer between the unregulated input voltage and the regulated output voltage. Idealized and actual oscilloscope waveforms are shown for the switching transistor Q_1.

The multivibrator output pulse v_{be}, Fig. 2b, controls transistor Q_1. The sharply rising v_{be} pulse saturates transistor Q_1, bringing the collector voltage to nearly ground potential, as shown in Fig. 2c. While the collector voltage is near ground potential, the unregulated input voltage appears across the primary of the output transformer. As shown in Fig. 2d the current through the coil will increase linearly for a time T, due to the primary magnetizing inductance. During the time current is increasing in the primary, the diode in the secondary circuit opposes current flow to the output capacitor. At the end of the time interval T a quantity of energy is stored in the magnetic field of the coil.

At the end of the v_{be} pulse Q_1 begins to turn off, causing the polarity of the transformer primary voltage to reverse. This flyback effect increases the collector voltage to a value greater than the input supply voltage, as shown in Fig. 2c. The energy stored in the field is transferred to the output capacitor, C_o, because a decreasing current in the primary induces a voltage in the secondary in the correct direction for current to flow through the diode. This flyback technique, that is, opening an inductive circuit to obtain an energy transfer, provides a lossless energy transfer if all components are ideal, and low-loss transfer even with nonideal elements.

A secondary winding on the flyback transformer is not necessary but is useful for several purposes. The output voltage is isolated from the primary, and output voltages can have values higher and lower than the input and of either polarity. The secondary circuit is shown in Fig. 2 with only two taps, which can represent the entire output of the voltage converter or can be considered to represent only one section

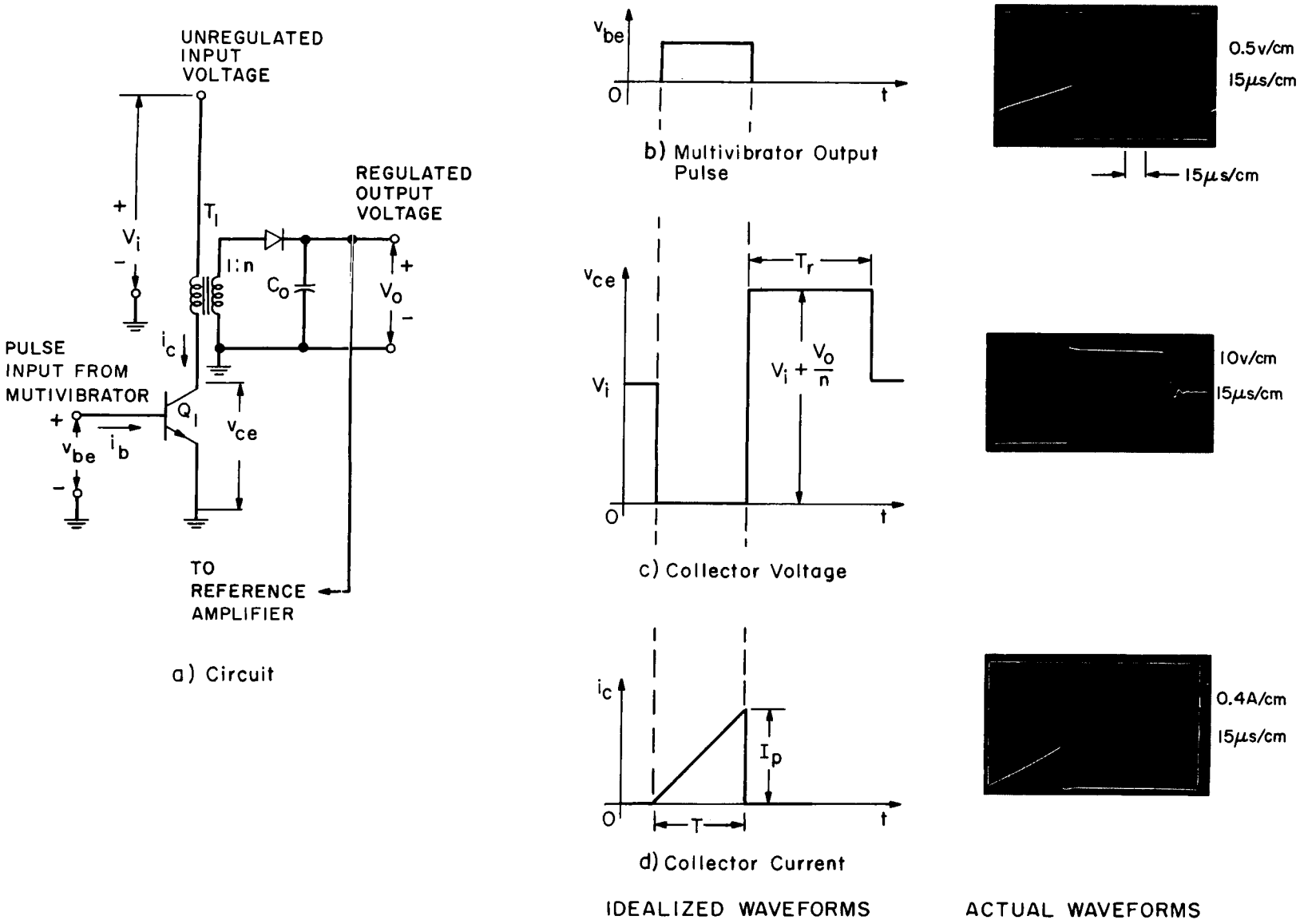


Fig. 2. Voltage Converter and Waveforms

of the output, between any two taps of a multi-tap secondary winding. When the secondary winding has multiple taps to provide multiple output voltages, each output circuit requires its own output capacitor and diode. However, obtaining well-regulated output voltages for each of several output circuits involves problems which are not discussed here.

Typical circuit schematic diagrams for the reference amplifier, voltage-controlled oscillator and multivibrator are shown in Fig. 3.

The voltage-controlled oscillator consists of an NPN transistor (Q_3) and a PNP transistor (Q_4) connected in a positive-feedback configuration. If we assume the connection from the reference amplifier to be broken (A in Fig. 3), the oscillator operates at a constant frequency determined by the R_1C_1 combination as follows: The initially uncharged capacitor C_1 begins charging toward the input voltage V_i through R_1. When the voltage on C_1 reaches a value equal to the forward bias voltage of Q_3 (approximately 0.7 volt for silicon transistors), Q_3 conducts and turns on Q_4. When Q_4 conducts it supplies more base current to Q_3, resulting in a fast-rising voltage pulse at the collector of Q_4. The regenerative action ceases when C_1 has been nearly charged to the input voltage through Q_4. At this time the polarity of the voltage on C_1 reverse biases Q_3 and the next pulse will not occur until the charging current through R_1 again forward biases Q_3. Thus the time between triggering pulses is determined by the R_1C_1 combination.

If we now assume A is reconnected, the frequency of the oscillator will be controlled by the reference amplifier, which is a differential amplifier of conventional design. When the output capacitor voltage is greater than the zener voltage, the difference voltage is amplified and base current is supplied through connection A in Fig. 3 to the base of Q_2. The effective resistance of Q_2, which can vary over a wide range, is included in the charging circuit of C_1, thus varying the time constant considerably in response to the difference between the output voltage of the converter and that of the zener reference.

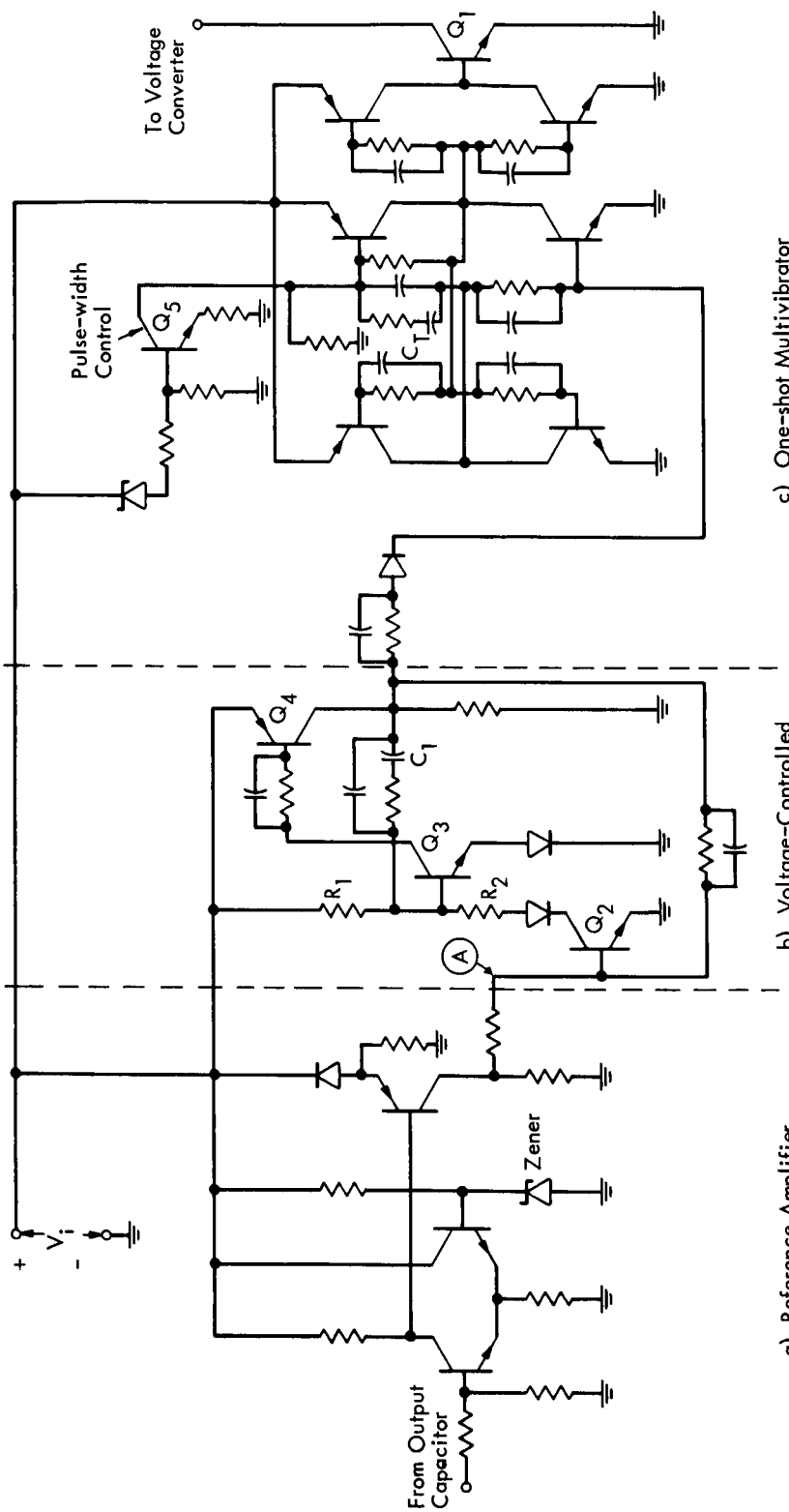


Fig. 3. Typical Circuits

The one-shot multivibrator is a standard complementary design[4] with the addition of a variable-pulsewidth feature. The multivibrator pulsewidth is controlled to be inversely proportional to the input voltage to insure that a drop in the input voltage will not result in a drop in the available output power, as discussed in Appendix A. A fraction of the main supply voltage is applied to the base of Q_5 to vary the collector current of Q_5. This varies the charging current to C_T, the multivibrator timing capacitor, which determines pulsewidth.

D. DESIGN CONSIDERATIONS

The principal factors which influence the converter design are:

(a) Maximum power output
(b) Output regulation and ripple
(c) Efficiency
(d) Weight

Each of these factors is discussed in detail below.

1. Maximum Power Output of Converter

The maximum circuit power of the converter shown in Fig. 2 is limited by the maximum allowable collector-to-emitter voltage and the peak-current capacity of transistor Q_1, as given by the following equation, derived in Appendix B.

$$P_i(\max) = \left(\frac{V_i I_m}{2}\right)\left(\frac{BV_{ce} - V_i}{BV_{ce}}\right) \qquad (1)$$

where BV_{ce} is the maximum allowable collector-to-emitter voltage before breakdown occurs

V_i is the main supply input voltage

I_m is peak allowable collector current of Q_1

This equation shows that for a given input voltage V_i, P_i is limited by I_m and BV_{ce} which become factors in the selection of transistor Q_1.

As shown in Appendix B, to approach the power output of Eq. 1 the output transformer requires sufficient inductance to satisfy the condition:

$$L = \frac{V_i T}{I_p} \tag{2}$$

In general, a magnetic core is required to provide sufficient inductance. As shown in Appendix B, to avoid saturation the core must satisfy the expression:

$$NA \geq \frac{V_i T}{B_s} \tag{3}$$

where B_s is the saturation flux density of the core

N is the number of primary turns

and A is the core cross-sectional area

The designer chooses the smallest core size which satisfies the requirements on L and NA to minimize core weight.

2. Output Ripple and Regulation

The ripple or a-c component of the output voltage is the change in output voltage caused by the transfer of energy from the primary, given by:

$$\Delta V_{oe} \approx \frac{\frac{1}{2} L I_p^2}{C_o V_o} \tag{4}$$

where L is the primary magnetizing inductance

I_p is the peak primary current

V_o is the average output voltage

C_o is the output capacitance

ΔV_{oe} is the change in output voltage due to energy transfer

This ripple component can be excessive when high output current is required at low output voltages. The ripple can be reduced by either adding more capacitance at the output or by transferring less energy per pulse. Of these two alternatives, transferring less energy per pulse is the more attractive solution since no additional weight is required. Transferring less energy per pulse (while still maintaining the same power output) generally means increasing the maximum frequency of operation. Exactly how high a frequency can be used depends upon the losses in the components, especially the switching transistor. High-speed, low-power transistors can be used to frequencies as high as 1 Mc with low losses. With higher power transistors, operation is usually limited to frequencies below 100 kc. In some applications a number of high-speed, low-power transistors have been used in parallel to obtain moderate amounts of power at a frequency of 100 kc and an efficiency of 85 percent.[5]

Output load regulation is ideally controlled by the gain of the reference amplifier. Since output power is proportional to frequency, see Appendix A, the change in output voltage corresponding to a change in output power is:

$$\Delta V_o = \frac{\Delta f}{K_1 G} = \frac{\Delta P_o}{K_1 K_2 G} \qquad (5)$$

where ΔP_o is the change in output power

ΔV_o is the corresponding change in d-c output voltage

K_1 is a constant relating frequency to control voltage for the voltage-controlled oscillator

K_2 is a constant relating output power to frequency

and G is the voltage gain of the differential amplifier

The output voltage regulation also depends on the stability of the reference voltage. The reference voltage is obtained from a temperature-stable reference diode with a temperature coefficient which is better than 0.01 percent/^{o}C. The diodes have low dynamic resistance so that the reference voltage is stable with respect to variations in the input voltage.

3. Efficiency

The power losses arising from the use of non-ideal components are described below. By far the largest power loss occurs in the voltage-converter stage of Fig. 2. The transistor, transformer, rectifier, and output capacitor all contribute to the losses.

Losses in the power-switching transistor, Q_1, can be separated into base drive losses, saturation voltage losses and switching losses. The energy loss per cycle in the transistor can be written as:

$$\text{Transistor loss per cycle} = \int_0^T v_{be} i_b dt + \int_0^T v_{ce} i_c dt + \int_T^{T_r} v_{ce} i_c dt \qquad (6)$$

The lower case letters refer to time-varying quantities as shown in Fig. 2. T is the pulsewidth and T_r is the reset time.

The base drive and switching losses can be reduced to a minimum by circuit techniques to be described below. The saturation voltage loss is primarily determined by the type of transistor used and cannot be significantly reduced by circuit techniques.

From Eq. 6 above it can be seen that base drive losses will be minimized by reducing the base drive voltage and current to minimum values required for transistor operation. Low voltages are not generally available so that a practical solution is to use a matching stepdown transformer to supply the base voltage as shown in the lower right of Fig. 7 (page 18). The primary of the matching transformer is driven by an increasing ramp of current to match the collector current of the switching transistors Q_9 through Q_{12}, in Fig. 7, which are the equivalent of Q_1 in Fig. 2. The requirement on the driving current ramp is that enough base current be supplied to hold the collector-to-emitter voltage of transistors Q_9 through Q_{12} at a low value.

An alternate method of supplying the base current is to add a feedback loop through a differential amplifier to supply just enough base current to keep transistor Q_1 slightly above saturation. A sketch of this base current feedback added to the voltage conversion stage is shown in Fig. 4. The converter shown in Fig. 6 (page 17) uses this approach. Since there is no base "overdrive" current with

this method, charge storage in the base of Q_1 is minimized, allowing the transistor to switch off more rapidly.

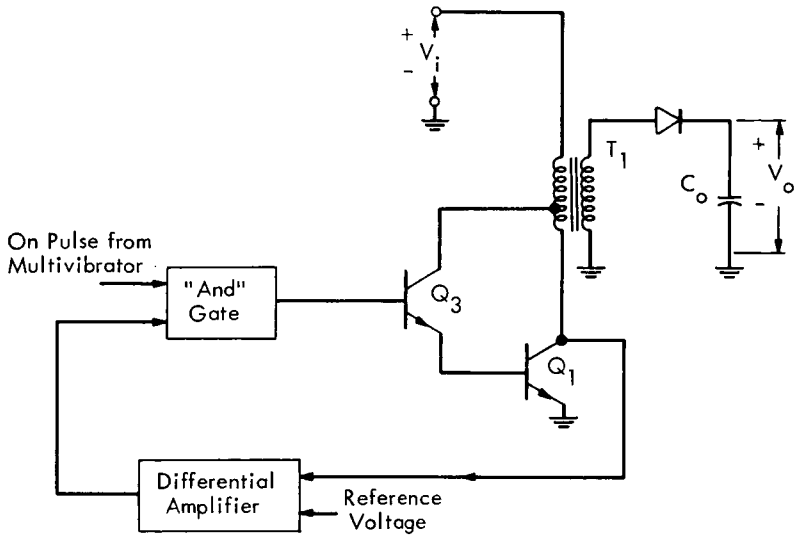


Fig. 4. Voltage Converter with Feedback to Minimize Base Current

The third term in Eq. 6 represents the loss in Q_1 during the turn-off time. Peak collector dissipation can be high during turn-off since the collector current is high and the collector voltage is increasing rapidly. High speed epitaxial transistors (with low collector-to-base feedback capacitance) can be turned off rapidly and withstand the high voltages which are generated. Turn-off times can be further reduced by removing charge stored in the base of Q_1 by pulsing another transistor connected to the base of Q_1 at turn-off. The converters of Figs. 6 and 8 (pages 17 and 20) use this technique.

The usual winding resistance, hysteresis, and eddy current losses are present in the converter output transformer. Because of the high peak currents it is important to minimize winding resistance. Assuming the primary current increases linearly, the energy lost per cycle in the winding resistance is:

$$\text{Resistive loss} = \frac{I_p^2}{3}\left[(T + T_r)\,R_p + \frac{T_r R_s}{n^2}\right] \qquad (7)$$

where I_p is the peak primary current

R_p is the primary winding resistance

R_s is the secondary winding resistance

n is the transformer turns ratio

T is the pulse width

T_r is the transformer reset time

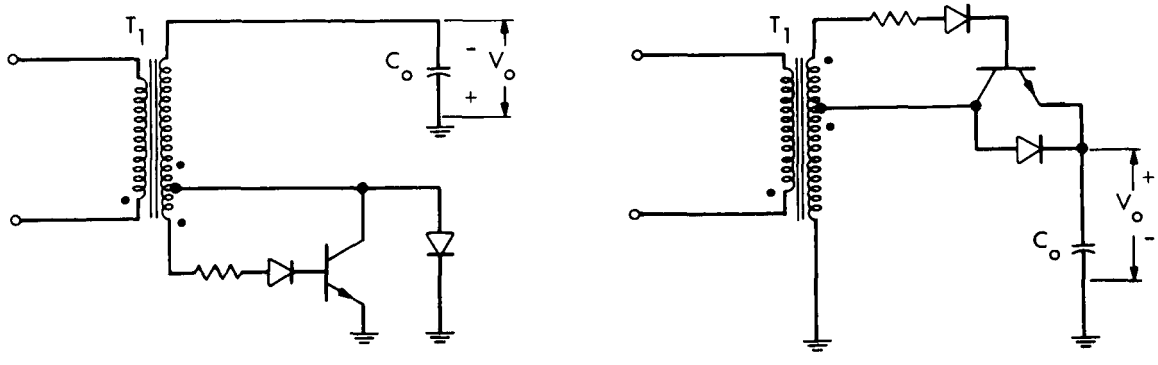
Since the peak current is typically four times the average current (see Appendix B) winding resistances must be kept small to obtain low resistive losses. Low winding resistance is achieved by using as large a wire size as will physically fit on the transformer core.

Core losses depend on the material chosen for the transformer core. An excellent choice for a core material in these applications is powdered Molybdenum-Permalloy. As expected, core losses in this material increase with increasing induction level and increasing frequency.[6] However, experience with the Molybdenum Permalloy cores has shown that core losses are quite low, even at frequencies approaching 100 kc. This material has relatively stable temperature characteristics.

A very important factor in connection with the transformer is the coupling or leakage inductance between primary and secondary windings. As mentioned earlier, the secondary winding is desirable since it provides isolation and allows the output voltage to be either higher or lower than the input voltage and of either polarity. The secondary winding must be closely coupled to the primary since otherwise a high voltage transient will be induced in the primary at the transistor turn-off time. The combination of collector current and high collector voltage results in high peak dissipation and in extreme cases will result in transistor breakdown. With good coupling the primary current at turn-off will effectively flow into the output capacitor and the primary voltage will be limited to the output voltage

divided by the transformer turns ratio. The best results have been achieved by twisting the primary and secondary windings together before winding them on a toroidal core.

Rectifier and capacitor losses occur primarily during the time when energy is being transferred to the output capacitor. Losses in the rectifier are present because of the forward voltage drop (on the order of 1 volt for silicon rectifiers). This forward drop becomes significant at low output voltages, e.g., for an output voltage of 6 volts approximately 15 percent of the output power is lost in the rectifier. It is sometimes possible to replace the diode rectifier with a transistor and thus reduce the forward voltage drop during rectification. This process is usually called synchronous rectification and some examples are shown in Fig. 5. The examples shown are limited to low output voltages (10 volts or less) because high speed, high gain silicon transistors suitable as rectifiers generally have relatively low emitter-to-base breakdown voltages.



a) Negative Output Voltage

b) Positive Output Voltage

Fig. 5. Synchronous Rectifier Circuits

The output capacitors are either tantalum or aluminum electrolytic types to obtain the required capacitance in a small size. Tantalum capacitors are roughly comparable in size to aluminum electrolytic capacitors except in very high capacitance or high voltage values, and are superior to aluminum electrolytic capacitors

in almost all performance characteristics including temperature stability, leakage current and dissipation factor. The dissipation factor is high for either capacitor type at frequencies above 10 kc. However, this has no significant effect on efficiency because (except during the initial charging process) during normal operation there is only a small a-c voltage component across the capacitor.

4. Weight

The transformer and output capacitor contribute most of the weight to this converter design. The weight of both these components is almost directly proportional to pulsewidth. Thus, the weight is reduced as pulsewidth is decreased, subject to maintaining a reasonable efficiency as previously discussed. The flyback transformer in this design is relatively light in weight when compared to a conventional transformer, that is, one which requires an appreciable primary magnetizing inductance. Only a small primary inductance, typically fractions of a millihenry, is required for a flyback transformer. Such a small inductance is easily realized with a small, light core.

E. EXPERIMENTAL RESULTS

Approximately ten different power converters using the techniques presented in this paper have been designed and tested. This section summarizes the results obtained with three of these designs. The three designs discussed are:

1. A high-power, high-voltage converter designed to supply a radar modulator.
2. A low-power, multiple-output-voltage converter.
3. A relatively simple medium power converter.

The efficiency of any converter based on the design techniques introduced here can be uniquely specified at any power-transfer level through the use of only two converter parameters, because the efficiency of the actual power-transfer circuits (transformer, switching transistors, output rectifier and capacitor) is independent of the actual power-transfer level. The two parameters specified are:

1. A stand-by or no-load power which can be measured by measuring input power required by the converter with no load connected to the output. This quantity is defined as P_S.

2. An incremental efficiency , η_i , which is measured by slightly varying the power the converter is delivering to a load and dividing this change in load power by the resultant change in input power.

The efficiency for any of the circuits described below is computed at any operating power level by the relationship:

$$\eta = \frac{\text{Power Out}}{\text{Power In}} = \frac{\text{Power Out}}{P_S + \frac{\text{Power Out}}{\eta_i}}$$

F. BREADBOARD CONVERTERS

1. High-Power, High-Voltage Converter

The circuit shown in Fig. 6 was designed to supply power at 400 volts to a radar modulator. The transmitter profile is such that approximately 300 watts are required for a 100-ms interval, followed by a period lasting from 1 to 10 seconds when no power is required.

The converter designed for this application operates from an input voltage between 23 and 33 volts. The stand-by power required is 15 mW , and an incremental efficiency of 80 percent is obtained. Regulation for this converter is within ± 2 volts (including ripple) for temperature changes from 0 to 50°C. The weight of the equipment (which can operate continuously at the 300-watt level if necessary) is less than 5 pounds.

2. Low-Power, Multiple-Voltage Converter

The circuit shown in Fig. 7, which has been reported previously,[5] delivers regulated voltages from 3 volts to 12 volts from an input voltage of 10 to 30 volts. Maximum output power is 1 watt. The stand-by power requirement is 0.5 mW, and an incremental efficiency of approximately 85 percent is obtained. Feedback is obtained from only one voltage (+ 12 v); therefore, the regulation of the other output voltages degrades as the ratios of the currents drawn from the multiple

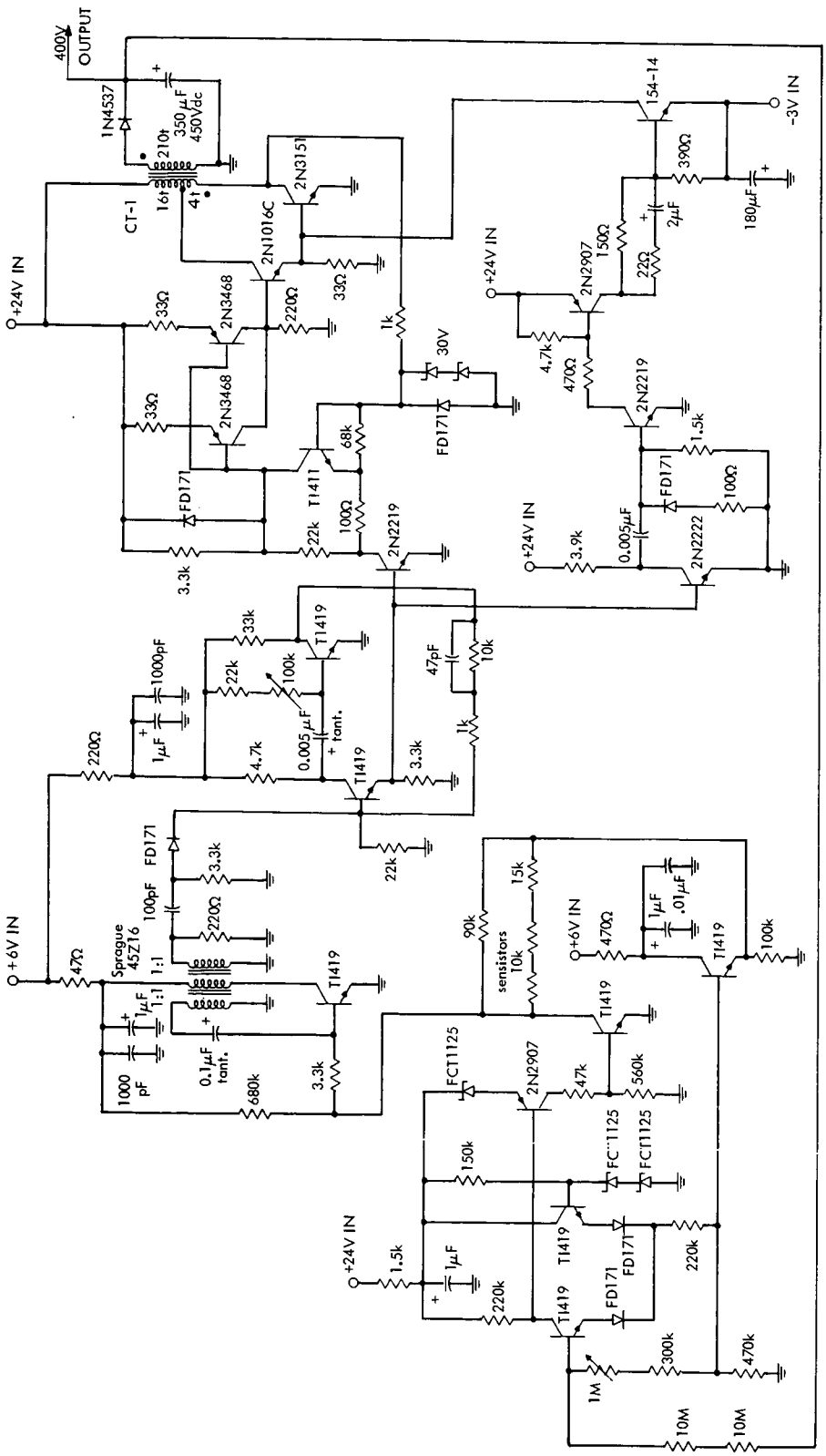


Fig. 6. High Power DC - DC Converter

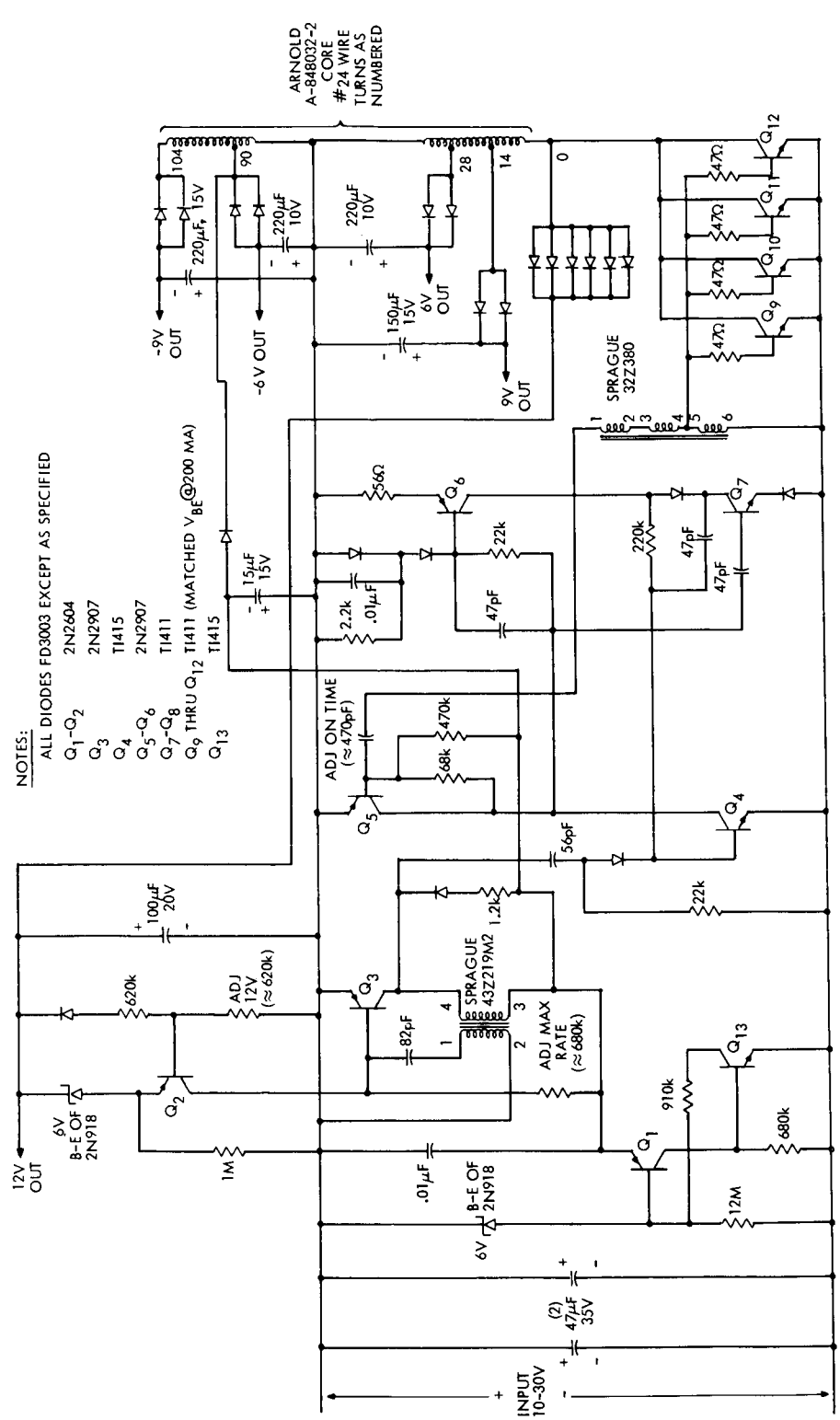


Fig. 7. Low Power DC - DC Converter

outputs change. If, however, the ratios of the currents supplied by the converter are maintained within a factor of 1.5 to 1, regulation is maintained within ± 3 percent for any combination of output power level and input voltage over the temperature range of $-60^{o}C$ to $+110^{o}C$.

3. Medium Power Converter

The circuit diagram of a relatively simple converter is shown in Fig. 8. This converter delivers a regulated +28-volt output with a maximum power output of 16 watts over a range of input voltages from 24 to 32 volts. The stand-by power is 120 mW with an incremental efficiency of 85 percent. No-load to full-load output voltage variation is less than 0.05 volt. This converter was not tested over a wide range of temperatures; however, it would be expected to exhibit the same temperature characteristics as the two previously mentioned designs.

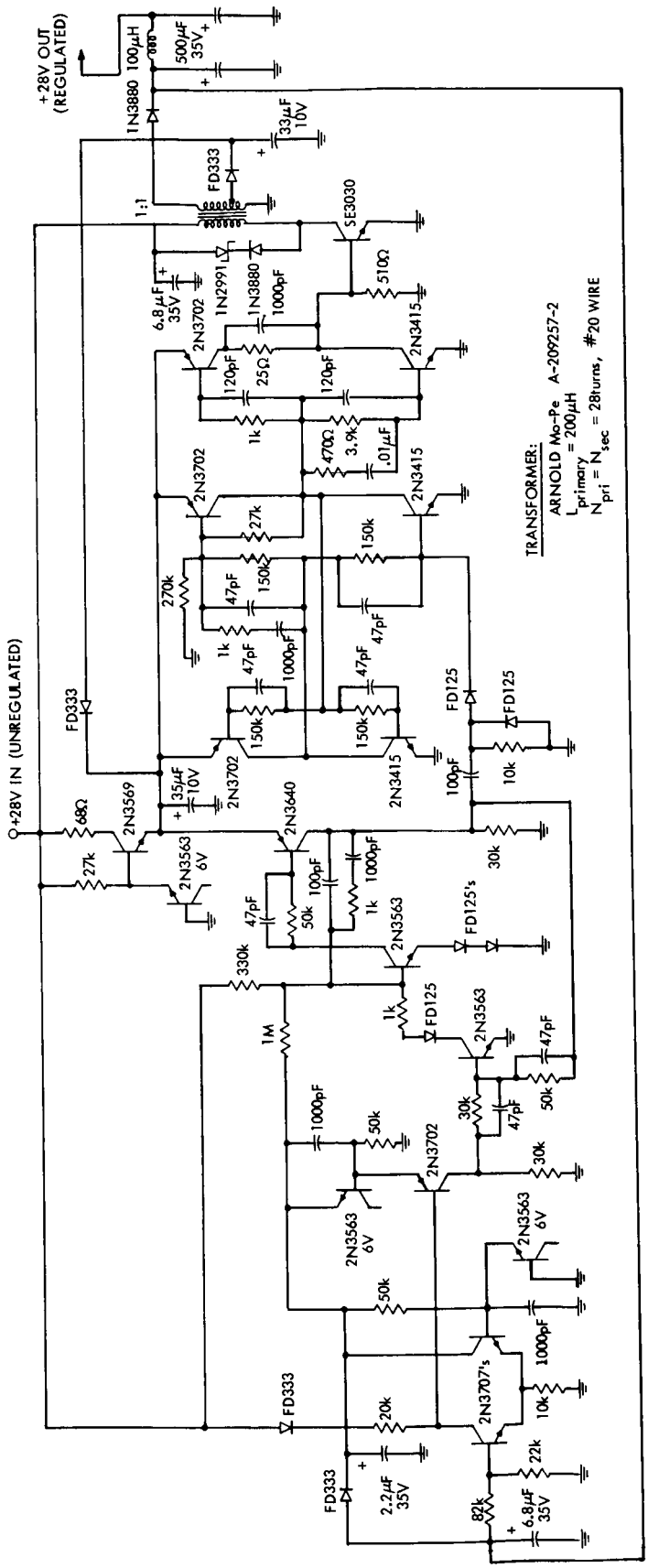


Fig. 8. 15-Watt Converter-Regulator

BIBLIOGRAPHY

1. Texas Instrument Company Engineering Staff, Transistor Circuit Design, McGraw Hill Book Company, Inc., New York, N.Y., 1963, pages 433-446.

2. Bomberger, D.C., et al., "The Spacecraft Power Supply System," NASA Special Publication SP-32, Vol. 1, June, 1963, pages 943-972.

3. M.I.T. Electronic Systems Laboratory, "Venus Radar Systems Investigations," Report No. ESL-SR-199, May, 1964.

4. Baker, R.H., "Maximum Efficiency Transistor Switching Circuits," Lincoln Laboratory Technical Report No. 110, March 22, 1956.

5. Roberge, J.K., "A Low Power High Efficiency DC-to-DC Converter," 1965 International Solid State Circuits Conference Digest, page 72.

6. Arnold Engineering Co., "Molybdenum Permalloy Powder Cores," Bulletin PC-104C, December, 1962.

APPENDIX A

Pulsewidth of the multivibrator in Fig. 3 is reduced when input voltage rises, and conversely. Therefore, a constant energy per pulse is stored in the primary inductance of the transformer. The energy stored per pulse is:

$$E = \frac{1}{2} LI_p^2 \qquad (A1)$$

where E = energy stored per pulse

L = transformer primary inductance

I_p = peak primary current

The charging current to C_T in Fig. 3 is varied so that the pulsewidth is inversely related to the input voltage by a constant K as:

$$T = K/V_i \qquad (A2)$$

Equation A2 holds only for a range of input voltages centered at the average value.

The peak collector current of Q_1 in Fig. 2 is related to the input voltage by the equation:

$$I_p = \frac{V_i T}{L} \qquad (A3)$$

Equation A3 represents a good approximation under the following three assumptions: (1) the saturation voltage of transistor Q_1 is small compared to the input voltage, (2) the input voltage remains constant over the pulsewidth, and (3) the magnetizing inductance of the primary of the output transformer is a constant and is purely inductive. Combining Eqs. A1, A2 and A3 yields:

$$E = \frac{1}{2} \frac{K^2}{L} \qquad (A4)$$

which shows that the energy stored in the field per pulse is a constant, independent of input voltage. The output power is proportional to the energy stored per pulse times the frequency. The converter operating frequency is directly proportional to the output power, regardless of changes in the input voltage.

APPENDIX B

The input power to the converter of Fig. 2 is

$$P_i = V_i(I_c)_{av} \tag{B1}$$

where $(I_c)_{av}$ is the average collector current. This expression assumes that V_i is constant and ignores the small collector-to-emitter saturation voltage across Q_1. Referring to the waveforms of Fig. 2 it can be seen that the average current (computed over one cycle) is:

$$(i_c)_{av} = \left(\frac{I_p}{2}\right)\left(\frac{T}{T + T_r}\right) \tag{B2}$$

To permit repetitive operation, the volt-time product across the transformer must be zero. This is expressed mathematically as:

$$V_i T - (V_{ce} - V_i) T_r = 0 \tag{B3}$$

where V_{ce} is the collector-to-emitter voltage of Q_1 during the reset time. Solving Eq. B3 for T_r and substituting in Eq. B2, the result is:

$$(i_c)_{av} = \left(\frac{I_p}{2}\right)\left(\frac{V_{ce} - V_i}{V_{ce}}\right) \tag{B4}$$

The maximum allowable value of $(i_c)_{av}$ is obtained for the highest value of V_{ce} which is defined as BV_{ce}, the collector-to-emitter voltage which can appear across Q_1 without transistor breakdown occurring. In the limit, as cycles of operation immediately follow one another, $(I_c)_{av}$ approaches $(i_c)_{av}$ and the maximum power input is:

$$P_i(max) = \left(\frac{V_i I_p}{2}\right)\left(\frac{BV_{ce} - V_i}{BV_{ce}}\right) \tag{B5}$$

I_p, peak design current, must be kept less than I_m, maximum allowable current for Q_1.

Equation 3 is the condition which must be met to avoid core saturation during the ON time. This condition is derived from the familiar equation:

$$v = N\frac{d\phi}{dt} \qquad \text{(B6)}$$

v is the voltage across the primary winding of transformer T1

N is the number of primary turns

ϕ is the primary flux

It is assumed that the core is initially unmagnetized, that is, at $t = 0$, $\phi = 0$. Rearranging and substituting $\phi = BA$:

$$B = \frac{\int_0^T v\,dt}{NA} \qquad \text{(B7)}$$

A is the core cross-sectional area

B is the change in flux density over the ON time, $t = 0$ to $t = T$

If v is constant and equal to V_i:

$$B = \frac{V_i T}{NA} \qquad \text{(B8)}$$

To avoid saturation, the value B must be kept less than B_s, the saturation value for the core material. This condition can be met by imposing the condition:

$$NA \geq \frac{V_i T}{B_s} \qquad \text{(B9)}$$