STUDY OF FAILURE AND RELIABILITY IN MICROELECTRONIC DEVICES

5th QUARTERLY REPORT

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1.0 INTRODUCTION

The Electronic Research Center of the National Aeronautics and Space Administration has instituted a study and test program directed towards achieving highly reliable microelectronic components. The integrated circuit program performed under this contract started two years ago with the objectives to isolate predominant failure mechanisms through testing and to develop techniques to identify and verify these failure mechanisms with a view towards developing screening techniques for high reliability devices.

The environmental stress tests had been completed several months ago and the results have been reported in previous reports. For the remainder of the presently defined program, the operating life test at elevated temperature is continuing wi th measurements being made every 1000 hours. Lots of Vendors A, B and C have completed 10,000 hours of operating life test, devices of Vendor E have completed 6000 hours of life test.

This is the Fifth Quarterly Report covering the work accomplished from September through November 1966. Results of the life test to date are tabulated and a summary is presented showing the mode of failure, the observed discrepancy, how failure was indicated and possible screening test that could be considered in the future.

TABLE I

SUMMARY OF FAILURES

LIFE TEST

DATA POINT	VENDOR A		VENDOR B		VENDOR C		VENDOR E	
	Total Number of samples	Number of Failures						
100 Hours	40	0	40	0	40	0	20	0
250 Hours	40	0	40	0	40	0	20	1
500 Hours	40	0	40	0	40	0	19	0
1000 Hours	40	1	40	0	40	1	19	0
2000 Hours	39	0	40	0	39	0	19	0
3000 Hours	39	0	40	1*	39	0	19	0
4000 Hours	39	2	40	0	39	0	19	0
5000 Hours	37	2	40	0	39	0	19	0
6000 Hours	35	5	40	1*	39	1*	19	0
7000 Hours	30	1	40	1	39	0		
8000 Hours	29	0	39	2	39	1		
9000 Hours	29	0	37	1	38	1		
10,000 Hours	29	2(note 1)	36	0	37	1		

*Device returned to test

1. Investigation is now in progress to verify these failures.

TABLE 2

SUMMARY OF FAILURES - Vendor A

LIFE TEST

DATA POINT	Total Number of Samples	Number of Failures	Device Numbers	Remarks
1000 Hour Life	40	1	43	I_8 increased from 157.0 na to 2.19 ua.
4000 Hour Life	39	2	21	I_3 increased from 11.00 na to 61.96 ma.
			27	I_3 increased from 13.20 na to 15.94 ua.
5000 Hour Life	37	2	9	I_2 increased from 29.10 na to 434.4 na
			16	I_3 leakage increased from 16.2 na to 27.00 ua.
6000 Hour Life	35	5	20	BV_9 decreased from 5.657 volts to .182 volts.
			22	BV_9 decreased from 5.649 to 2.786 volts.
			30	BV_8 decreased from 5.416 volts to .002 volts. I_8 reading of .5764 ma.
			38	BV_9 decreased from 5.737 volts to 2.200 volts. V_{SAT} increase 69%.
			39	BV_9 decreased from 5.830 volts to 3.388 volts.
7000 Hour Life	30	1		V_{SAT} Increased from .255 volts to .376 volts (47%)
8000 Hour Life	29	0		
9000 Hour Life	29	0		
10,000 Hour Life	27	2	42	V_{SAT} (V_6) increased from .305 volts to 1.08 Volts. Investigating
			45	BV_9 decreased from 5.85 volts to .451 volts. Investigating

TABLE 2 (Cont.)

SUMMARY OF FAILURES - Vendor B

LIFE TEST

DATA POINT	Total Number of Samples	Number of Failures	Device Number	Remarks
3000 Hour Life	40	1	19	I_3 increased from 4.80 na to 492.6 na. Device annealed and returned to test.
6000 Hour Life	40	1	30	BV_9 decreased from 31.30 volts to 13.59 volts. No failure analysis performed. Device returned to test.
7000 Hour Life	40	1	8	V_{SAT} increased from .239 volts to 1.87 volts.
8000 Hour Life	39	2	19	BV_8 decreased from 27.10 volts to 16.24 volts.
				BV_9 decreased from 28.30 volts to 15.24 volts
			30	BV_9 decreased from 31.30 volts to 14.19 volts.
9000 Hour Life	37	1	9	V_{SAT} increased from .256 volts to 20.36 volts
10,000 Hour Life	36	0		

TABLE 2 (Cont.)

SUMMARY OF FAILURES - Vendor C

LIFE TEST

DATA POINT	Total Number of Samples	Number of Failures	Device Number	Remarks
1000 Hour Life	40	1	31	I_7 increased from 2.7 na to 109.5 ua.
6000 Hour Life	39	1	24	V_{SAT} decreased from .265 volts to .2354 volts. Device returned to test.
7000 Hour Life	39	0		
8000 Hour Life	39	1	43	BV_7 decreased from 18.80 volts to .720 volts.
9000 Hour Life	38	0		
10,000 Hour Life	38	1	13	BV_9 decreased from 19.10 volts to .195 volts.

TABLE 2 (Cont.)

SUMMARY OF FAILURES - Vendor E

Life Test

DATA POINT	Total Number of Samples	Number of Failures	Device Number	Remarks
250 Hour Life	20	1	24	Output transistor leakage current increased from 750-800 na to 2 ma.
500 Hour Life	19	0		
1000 Hour Life	19	0		
2000 Hour Life	19	0		
3000 Hour Life	19	0		
4000 Hour Life	19	0		
5000 Hour Life	19	0		
6000 Hour Life	19	0		

2.0 DISCUSSION

DTL NAND/NOR GATES, Integrated Circuits procurred from three manufacturers are being used in this study. The data presented in Table 3 represents test results gathered from two life test groups. One group has completed 10,000 hours and the other group has completed 6000 hours of operation. The number of completed hours are total test hours accumulated on each device with the exception of those devices removed from test for detail failure analysis. The operating life test will continue to 30 June 1967.

The gates are exposed to an ambient temperature of +125°C. The gates are switched from "0" to "1" state at a 1 megacycle pulse repetition rate using parallel switching. Each gate is loaded to simulate its maximum fan-out with a resistive-capacitive load. All unused input diodes are reverse biased by being connected to the V_{CC} 4.0 volt supply. The net effect is to study both the dynamic and reverse characteristics of these logic elements.

Results of the life test to date are summarized in Table 3 showing: Description of Failure, Electrical Indicators, Discrepancies Observed, Frequency of Occurrence, and Possible Screening Tests that could be considered in the future.

TABLE 3

INVESTIGATION OF INTEGRATED CIRCUIT DISCREPANCIES
WHICH OCCURRED DURING LIFE TEST

DESCRIPTION OF FAILURE	ELECTRICAL INDICATORS	DISCREPANCIES OBSERVED	FREQUENCY OF OCCURRENCE	POSSIBLE SCREENING TEST
Input diode shorted (catastrophic)	Low breakdown voltage	Bubbles in metallization Bubbles in oxide	5	Visual inspection prior to sealing package, high temperature storage 250 hour
		Flake suspended between two internal leads		Visual inspection prior to sealing package, vibration and x-ray
		Chipping of oxide around the outer edge of emitter diffusions		Does not appear to be a failure mechanism
		Black intermetallic formation on metallization over input diode		High temperature storage with bias for 250 hours
Input diode breakdown voltage (degradation)	High resistive characteristic of input diode	Black intermetallic formation around gold bonds on aluminum pads	7	High temperature storage with bias for 250 hours
		Black intermetallic formation growth just beginning		
Input diode leakage current (degradation)	Leakage current increased greater than one order of magnitude	Superficial scratches in metallization and oxide	7	Visual inspection prior to sealing package
		Black intermetallic formation		High temperature storage with bias for 250 hours
Transistor output saturation voltage open (catastrophic)	Very high saturation voltage (open circuit voltage)	Black intermetallic formation spotted over entire metallized areas	3	High temperature storage with bias for 250 hours. Burn-in test for 500 hours at an elevated ambient temperature
Transistor output saturation voltage (degradation)	Increase in saturation Voltage greater than 10%	Black intermetallic formation Superficial scratches	2	High temperature storage with bias for 250 hours Burn-in test for 500 hours at an elevated ambient temperature

3.0 RESULTS

The test results, to date, indicate that failure mechanisms or modes for integrated circuits are similar to those experienced with switching type diodes and small-signal planar/passivated transistors. The most common defects were surface contamination and scratches.

An operating life test which allows simultaneous static (dc) and dynamic operation of the integrated circuit has definite merit. The static operation provides well defined leakage current parameter degradation criteria. The dynamic operation stresses the entire integrated circuit and enables the establishment of degradation criteria for the gain and saturation parameters in an addition to the dc leakage current.

Observations from the data indicate that the input diodes being driven by the signal source (0 - 4 volts) were the predominant failure areas. This type of life testing more closely simulates the actual device application.

Possible screening tests to isolate those discrepancies identified in Table 3 are listed as follows:

1. Visual inspection prior to sealing package
2. Vibration
3. X-Ray
4. High temperature storage with bias
5. Operating life with temperature, stressing both the dynamic and reverse characteristics of the logic elements.

The test conditions and rejection criteria for the above mentioned tests are shown in Table 4.

TABLE 4

POSSIBLE SCREENING FOR ISOLATING DEFECTS
IN INTEGRATED CIRCUITS

TEST	CONDITIONS	REJECTION CRITERIA
Microscope Inspection	200x binocular inspection of unsealed integrated circuits	Detection of visible surface defects and bonding defects
High Temperature Storage with Bias	Reverse bias circuit and substrate with rated voltage for 250 hours at +150°C	High leakage parameter deviations from predetermined criteria
Operating Life (Burn-in)	Dynamic operation (100Kc minimum) at +125°C for 500 hours	Leakage parameter and output parameter deviations from predetermined criteria
X-Ray	Two views perpendicular about longitudinal axis. Resolution to allow detection of a particle .001 inch	Inadequate internal clearance, evidence of foreign particles. X-Rays viewed at a magnification 20X power minimum
Vibration	55 cps, 0.060 inch double amplitude 2 hours in X or Y axis. Monitor output of devices under test	Discontinuity greater than 10 μsec.