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CIRCUIT CONSIDERATIONS FOR DC TO DC CONVERSION ABOVE 10 KHZ

by

G. Ernest Rodriguez

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Goddard Space Flight Center
Greenbelt, Maryland

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SUMMARY

Various circuits have been developed for DC to DC conversion in the frequency range of 400 HZ to 10 KHZ. Conversion above 10 KHZ has usually been accomplished at the expense of efficiency. Power losses of several circuits are discussed and a method for optimizing the feedback loop of the "two transformer oscillator" for operation above 10 KHZ is formulated. The method is used in the design of a converter at 25 KHZ, and preliminary results are presented. Selection of the transformer core material is based on displayed hysteresis loops during circuit operation of two core materials.

CIRCUIT CONSIDERATIONS FOR DC TO DC CONVERSION ABOVE 10 KHZ

INTRODUCTION

Static conversion of DC to DC has been a prime requirement in the overall design of scientific satellites in order to provide the necessary voltage levels required by the complex experiments and instruments on board. Particular interest is placed on the individual efficiency of each converter, as it places a constraint on the overall power required by the spacecraft. Along with efficiency, performance, and reliability, the inevitable restriction on size and weight soon becomes a problem.

Choosing a high frequency of operation for the converter enables the designer to meet the requirement of small size and weight. During the past two years, transistor manufacturers have increased the operating frequency capability of silicon power transistors to the point where the designer is no longer faced with the problem of choosing a good transistor for high frequency operation.

Circuit Variations

Several circuits developed for DC to DC conversion have become standard. The magnetic coupled multi-vibrator, Figure 1, is one such circuit.[1,2] This circuit was later improved by Jensen[3], Figure 2, and since then there have been several variations, Figure 3. Most of these circuits operate satisfactorily in the frequency range of 400 HZ to 10 KHZ, but in the frequency range of 10 KHZ to 100 KHZ efficiency and performance become questionable. Therefore, for a converter to operate in this high frequency range, careful consideration of circuitry and circuit design is necessary.

If the circuit of Figure 1 is designed to operate in the frequency range of 10 KHZ to 100 KHZ, a considerable amount of power is dissipated in the transistors. This power dissipated in the transistors can be expressed as:

$$P_d \cong f\,(V_{ce\ sat}\, I_{avg}\, t_{cond} + E_{bb}\, I'_{avg}\, t_{sw}) \qquad (A)$$

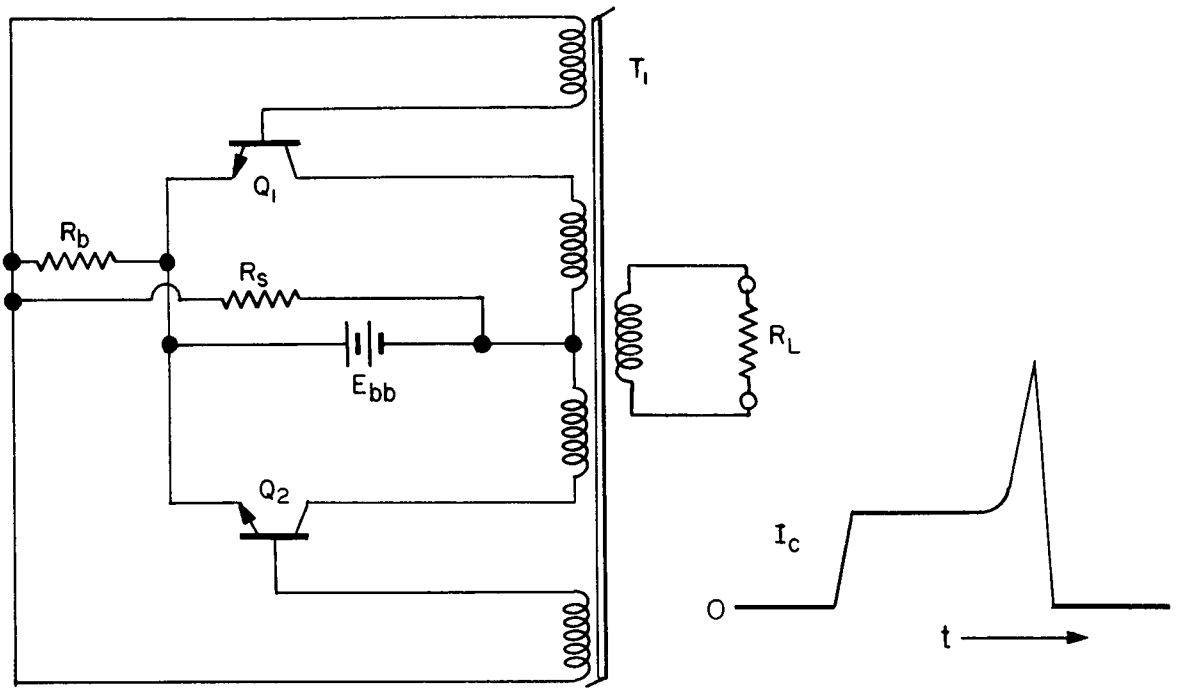


Figure 1–Basic Magnetic–coupled Multivibrator

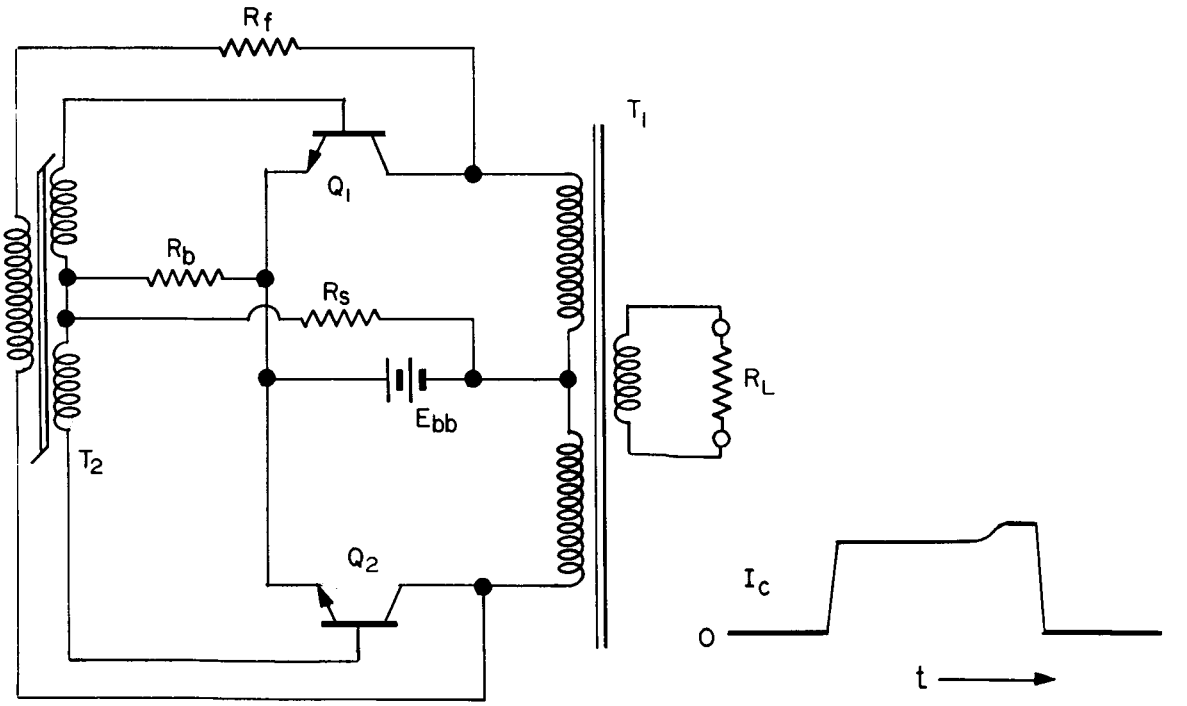


Figure 2–Improved Magnetic–coupled Multivibrator

where

t_{sw} = total time for switching (t_{rise} and t_{fall})

t_{cond} = $1/2f - t_{sw}$

f = frequency of operation

I_{avg} = average collector current during t_{cond}

I'_{avg} = average collector current during t_{sw}

$V_{ce\ sat}$ = collector emitter voltage drop of transistor

E_{bb} = power source voltage level.

From this it is evident that transistor dissipation becomes objectionable when t_{sw} approaches T/2, but particularly when the collector current is rapidly increasing with time prior to switching, as is the case for the circuit of Figure 1. This increase of current is necessary for the operation of the circuit and is a result of the transformer T_1 demanding more magnetizing current upon reaching saturation. The value of current which can flow at this time is dependent on the h_{fe}, storage time of the transistor, and the available base drive. In most circuit designs of this type, the value of this current maximum is some factor between 1 to 2 times the maximum load current and in some cases up to ten times the maximum load current. Consequently, the efficiency of this circuit would be very low in the high frequency range of 10 KHZ to 100 KHZ.

The switching of conduction between the two transistors (in the circuit of Figure 2) is accomplished by reducing the base drive to the transistors. This lowers the value of I'_{avg} and I_{avg} in the expression for P_d, (A) and consequently reduces the power dissipated in the transistors. If the transformer T_1 is designed in such a way that the flux excursion is some fraction of the maximum flux capacity of the core, then the power dissipated in it will be less than the power dissipated in T_1 of Figure 1. (Assuming the same core material and size.) If the component parameters are such that the circuit is in complete symmetry, then the hysteresis loop of T_1 will be a minor loop centered around its axis of symmetry. However, this is usually not the case, as the symmetry of the circuit is upset by variations in transistor parameters. When this occurs, the hysteresis loop is no longer centered around its axis of symmetry, but close to one end of saturation. Provisions must, therefore, be incorporated to insure circuit symmetry as much as possible.

The circuit in Figure 3(a) is sometimes used in applications requiring a fixed frequency independent of E_{bb}. Here the frequency is dependent primarily on the LC product. The design of the circuit necessitates a base current well in excess of that required for saturation of Q_1 and Q_2. As a result,

the storage time of the transistors is increased to such a magnitude that in order to remove the excess stored charges, a large reverse base current is required. This current must flow through the base-emitter junction of the opposite transistor, rendering it conductive, and since both transistors are conductive a large current surge is drained from the supply. This current surge occurs every time the transistors switch states, and represents power dissipation directly proportional to frequency.

The circuit in Figure 3(b) employs a current transformer in the feedback loop. Here the base drive is proportional to the load current, and the frequency of operation is determined by the core properties and the voltage induced in the feedback winding. Usually this voltage is equal to the base-emitter voltage of the transistor plus a diode voltage, and consequently circuit symmetry is greatly unbalanced by variations in V_{be} between Q_1 and Q_2. As the load current is reduced, the base current is proportionately reduced and a condition arises where the circuit goes into a much higher frequency of operation. Provisions to prevent this from occurring and provisions for maintaining circuit symmetry are necessary for proper operation of this circuit at high frequency.

If the inductance L_1 of the circuit in Figure 3(a) is replaced by a resistor (as in Figure 3(c)), the frequency of operation is determined by the RC product, load, and transistor parameters. The maximum base current which can flow at the beginning of each half cycle is limited by the series resistance and rapidly decays until the transistor can no longer remain in conduction. Stored charges are reduced considerably in this circuit, (which results in good switching), but circuit symmetry is very poor.

Efficiency Considerations

A breakdown of the power losses common to the various circuits described would be:

(a) transformer losses

(b) rectifier and filter losses

(c) transistor losses

(d) feedback power losses

The losses incurred by items (a) and (b) are somewhat fixed by the characteristics of the materials and components used and can be made a minimum by careful selection. Transistor losses (c) and losses in the feedback loop (d), however, depend largely on the type of circuit and the design procedure.

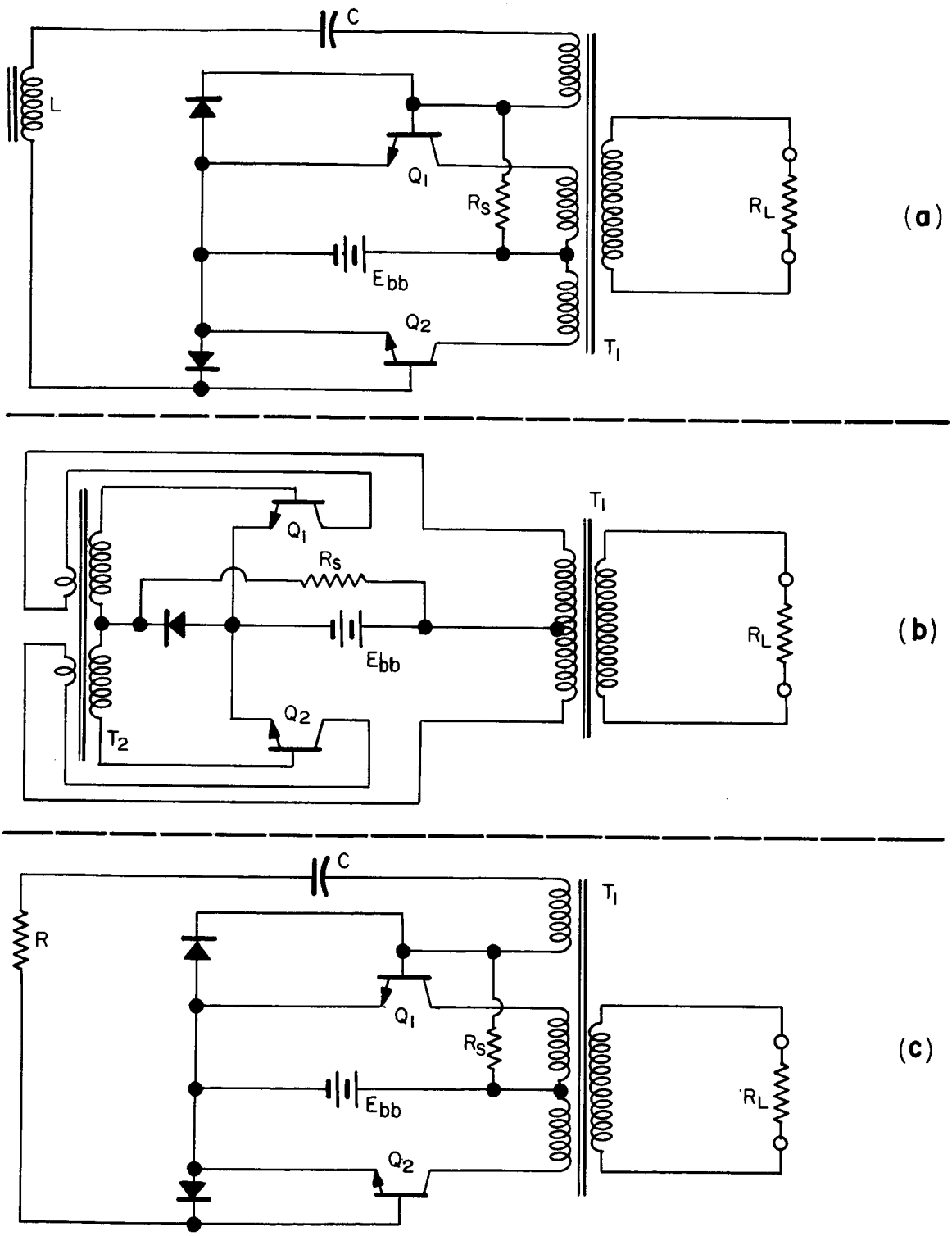


Figure 3–Variations of Square Wave Oscillators

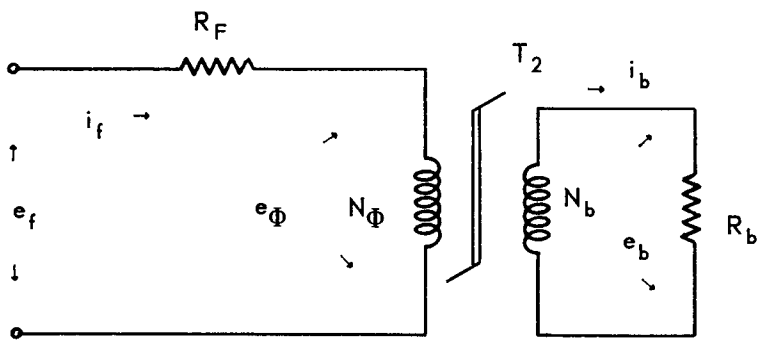
Circuit Selection

The designer is left with a favorable choice of circuit techniques for the lower operating frequency, but must consider carefully the choice of circuit for the higher operating frequency. The basic two-transformer oscillator as shown in Figure 2 offers a good choice for high frequency operation when considering stability from no load to full load, efficiency, and circuit symmetry.

Optimizing the Feedback Loop

Attempting to design the two-transformer oscillator for high frequency operation readily leads to the question of the value of Rf, Figure 2. This value of Rf greatly affects the feedback power losses and thus must be optimized for high efficiency.

For the circuit of Figure 2, the feedback loop can be considered as a simplified equivalent circuit.



where:

e_f = feedback voltage from oscillator

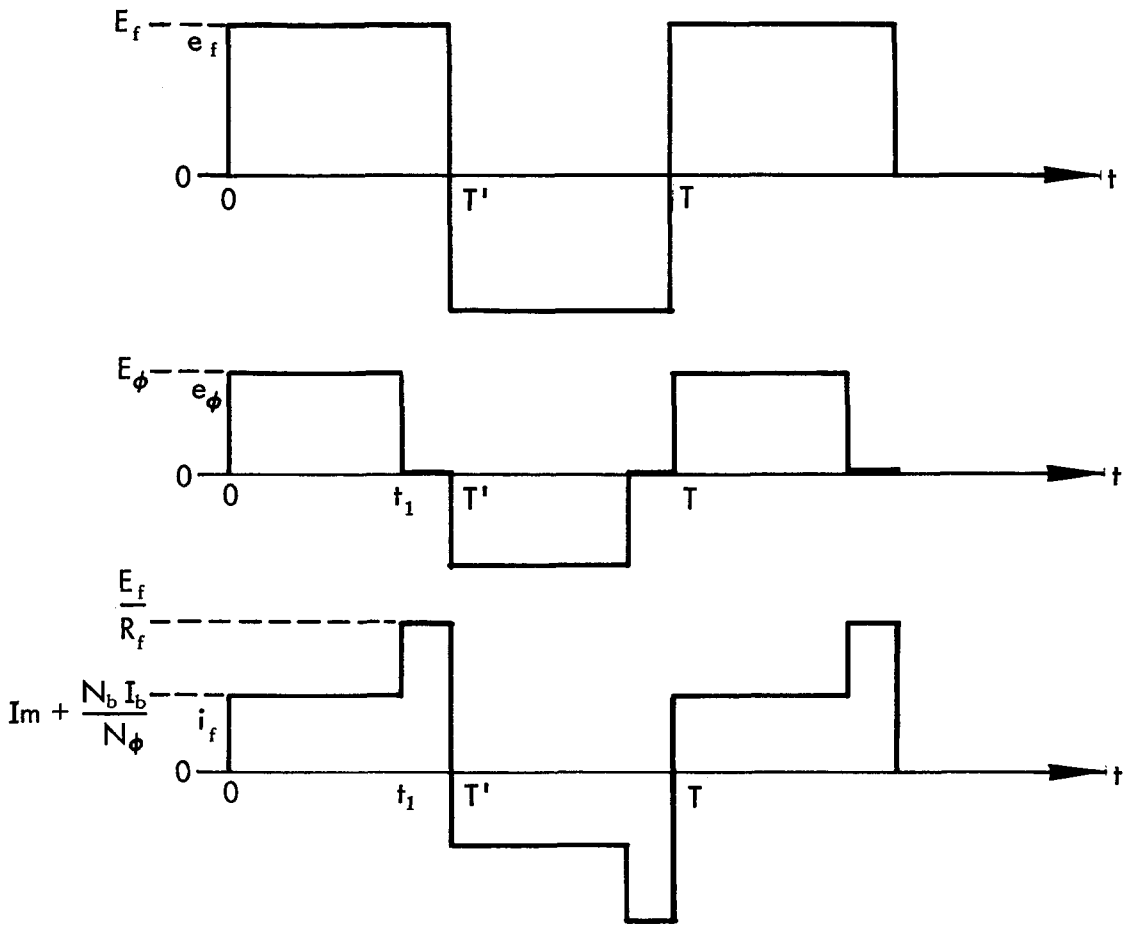
R_f = feedback resistor

T_2 = saturating square-loop transformer

R_b = equivalent resistance of base circuit

e_b = necessary base drive voltage.

The voltage and current waveforms for the circuit are assumed to be square waves, or:



For the circuit and the associated waveforms, the power dissipated can be expressed as:

$$P_{df} = \frac{1}{T'} \int_0^{t_1} e_f \, i_f \, dt + \frac{1}{T'} \int_{t_1}^{T'} \frac{e_f^2}{R_f} \, dt \qquad (1)$$

this expression reduces to:

$$P_{df} = \frac{1}{T'}\left[E_f\left(I_m + \frac{N_b}{N_\phi} I_b\right) t\right]_0^{t_1} + \frac{1}{T'}\left[\frac{E_f^2}{R_f} t\right]_{t_1}^{T'} \quad (2)$$

where: 0 to t_1 represents the time transformer T_2 takes to saturate from one saturation flux level to the other saturation flux level.

t_1 to T' represents the time after transformer T_2 saturates to the time the oscillator changes states, or approximately the storage time of the transistor, t_s.

T' represents one-half of the period.

E_f is the magnitude of the square wave voltage e_f, I_m is the magnitude of the magnetizing current of transformer T_2, I_b is the magnitude of the base current necessary for the switching transistors, and N_b/N_ϕ is the turns ratio of the secondary winding and primary winding of T_2.

With these assumptions and definitions, then:

$$P_{df} = \frac{1}{T'}\left[E_f\left(I_m + \frac{N_b}{N_\phi} I_b\right)(T' - t_s)\right] + \frac{1}{T'} \frac{E_f^2}{R_f} t_s \quad (3)$$

the value of R_f can be found by considering:

$$E_f = \left(I_m + \frac{N_b}{N_\phi} I_b\right) R_f + E_\phi$$

or

$$R_f = \frac{E_f - E_\phi}{\left(I_m + \frac{N_b}{N_\phi} I_b\right)} \quad (4)$$

Defining a_ϕ as a ratio such that:

$$\alpha_\phi = \frac{E_\phi}{E_f} \tag{5}$$

then substituting for E_ϕ, equation (4) reduces to:

$$R_f = \frac{E_f\left(1 - \alpha_\phi\right)}{I_m + \frac{N_b}{N_\phi} I_b} \tag{6}$$

and substitution of (6) in (3) yields:

$$P_{df} = \frac{E_f\left(I_m + \frac{N_b}{N_\phi} I_b\right)}{T'} \left[T' - t_s + \frac{t_s}{1 - \alpha_\phi}\right] \tag{7}$$

Since

$$\frac{N_b}{N_\phi} = \frac{E_b}{E_\phi} = \frac{E_b}{\alpha_\phi E_f} \tag{8}$$

then

$$\left(I_m + \frac{N_b}{N_\phi} I_b\right) = I_m + \frac{P_b}{\alpha_\phi E_f} \tag{9}$$

where P_b is the necessary power in the base circuit, or, $P_b = E_b I_b$. Using this new term, equation (7) becomes:

$$P_{df} = \left(E_f I_m + \frac{P_b}{\alpha_\phi}\right)\left[\frac{T' - t_s}{T'} + \frac{t_s}{T'\left(1 - \alpha_\phi\right)}\right] \tag{10}$$

Introducing a new term, x, such that $t_s = xT'$, then equation 10 becomes:

$$P_{df} = \left(E_f I_m + \frac{P_b}{\alpha_\phi}\right)\left[(1 - x) + \frac{x}{1 - \alpha_\phi}\right] \tag{11}$$

the magnitude of I_m is related to the core properties of transformer T_2, and is:

$$I_m = \frac{.4\pi H_c \ell_m}{N_\phi} \tag{12}$$

where: H_c is the coercive force of T_2 at the operating frequency

ℓ_m is the mean magnetic path length in centimeters

N_ϕ, however, is related to E_ϕ by:

$$E_\phi = N_\phi \frac{d\phi}{dt} \times 10^{-8}$$

From this a relation for N_ϕ can be found to be:

$$N_\phi = \frac{E_\phi T'(1 - x)\ 10^8}{\phi_c} \tag{13}$$

where ϕ_c is the flux capacity of transformer T_2. Thus Equation (12) can be expressed as:

$$I_m = \frac{.4\pi H_c \ell_m \phi_c \times 10^{-8}}{\alpha_\phi E_f T'(1 - x)} \tag{14}$$

Substituting Equation (14) in (11) and simplifying will yield:

$$P_{df} = P_b(1 + n)\left[\frac{1 - \alpha_\phi (1 - x)}{\alpha_\phi (1 - \alpha_\phi)}\right] \tag{15}$$

where:

$$n = \frac{P_c}{P_b} = \frac{E_\phi I_m}{P_b} = \frac{1.6\pi \ell_m A_c B_m H_c f \times 10^{-8}}{P_b (1 - x)} \qquad (16)$$

and:

P_c = effective core loss

A_c = effective Core Cross-Sectional area

B_m = maximum flux-density saturation level

$\phi_c = 2B_m A_c$

f = desired operating frequency.

Equation (15) expresses the power dissipated in the feedback loop, and is independent of the magnitude of the feedback voltage, E_f, but is a function of P_b, n, α_ϕ and x. As originally defined, x is a function of the storage time of the switching transistors and the frequency of operation, or, $x = t_s/T' = 2t_s f$, consequently it becomes important at the higher frequencies. The designer is left with a choice of α_ϕ between 0 and 1, and either zero or 1 is never used because for either case the circuit would not function as intended. By taking the partial derivative of P_{df} with respect to α_ϕ and equating it to zero, an extreme value of P_{df} can be found. The roots of

$$\frac{\partial P_{df}}{\partial \alpha_\phi} = 0$$

are found to be:

$$\alpha_{\phi_1} = \frac{1 + \sqrt{x}}{1 - x} \quad \text{and} \quad \alpha_{\phi_2} = \frac{1 - \sqrt{x}}{1 - x} \qquad (17)$$

α_{ϕ_1} is an extraneous root because for any value of x between 0 and 1, $\alpha_{\phi_1} > 1$, thus the only real root is α_{ϕ_2}. The value of α_{ϕ_2} will range from 1/2 to 1 for values of x ranging from 0 to 1, and it can be shown that for any value of α_{ϕ_2} in this range, the $\partial^2 P_{df}/\partial \alpha_\phi^2$ will be positive, and hence the extreme value of P_{df} will be a minimum.

Equation (17) for α_{ϕ_2} may be used to determine what value of α_ϕ will result in minimum power consumption by the feedback loop. It is interesting to note that n is directly proportional to frequency, effective core volume, and the area

of the hysterysis loop. These factors should be kept in mind when selecting the core material for T_2, as they will affect the value of n.

Usually E_f is chosen as the voltage from collector to collector, but it can be obtained from any convenient secondary winding on T_1. A low value of E_f will result in a small number of turns and thus T_2 will be easier to wind.

The value of R_f can be determined from:

$$R_f = \frac{E_f^2}{P_b} \frac{\alpha_\phi (1 - \alpha_\phi)}{(1 + n)} \tag{18}$$

where E_f is in volts and P_b in watts.

n can be calculated from the core properties which are known once the core material and size is chosen for T_2. This in turn can be determined by choosing the core size from the following relation:

$$\phi_c W_A = \frac{5P_b (1 - x) \times 10^{11}}{f} \tag{19}$$

where: $\phi_c W_A$ is the product of window area of the core and its flux capacity, and is a measure of the core-size. (A winding factor of .133 and a current rating of 750 cir mils/amp was used to obtain equation (19).)

Once the core-size for T_2 has been selected, N_ϕ can be calculated by:

$$N_\phi = \frac{\alpha_\phi E_f (1 - x) \times 10^8}{2f \phi_c} \tag{20}$$

Since the calculations of α_ϕ and P_{df} involve x, or the storage time, it is necessary to measure the storage time of the transistor under the same conditions it will see in the final circuit configuration.

Selection of Transformer Material

The basis of operation for the circuits of Figures 2 and 3 rely on the operation of the main transformer to be a non-saturating mode. This condition will only occur if the flux excursion as seen by the transformer during each half cycle is identically the same as the other half, otherwise the transformer will be biased towards saturation in either direction, depending on circuit symmetry. The characteristics of the core material will determine the tendancy for the transformer to saturate during the latter portion of a half cycle.

High frequency operation readily indicates that eddy current losses become important, and, therefore, must be considered in the selection of core material. Ferrite cores offer low eddy current losses, but hysteresis losses sometimes become objectionable. Highly orientated core material, such as Round Permalloy 80, tape wound cores of 1 mil to 1/8 mil, offer lower hysteresis losses, but their squareness is somewhat undesirable for the type of circuit requiring non-saturating operation.

Design of a 25 KHZ DC to DC Converter

The circuit as shown in Figure 4 was designed for a power level of eight watts at an input level of 15 volts, and at an operating frequency of 25 KHZ.

The feedback loop was designed by the procedure as follows:

1. Calculate P_b:

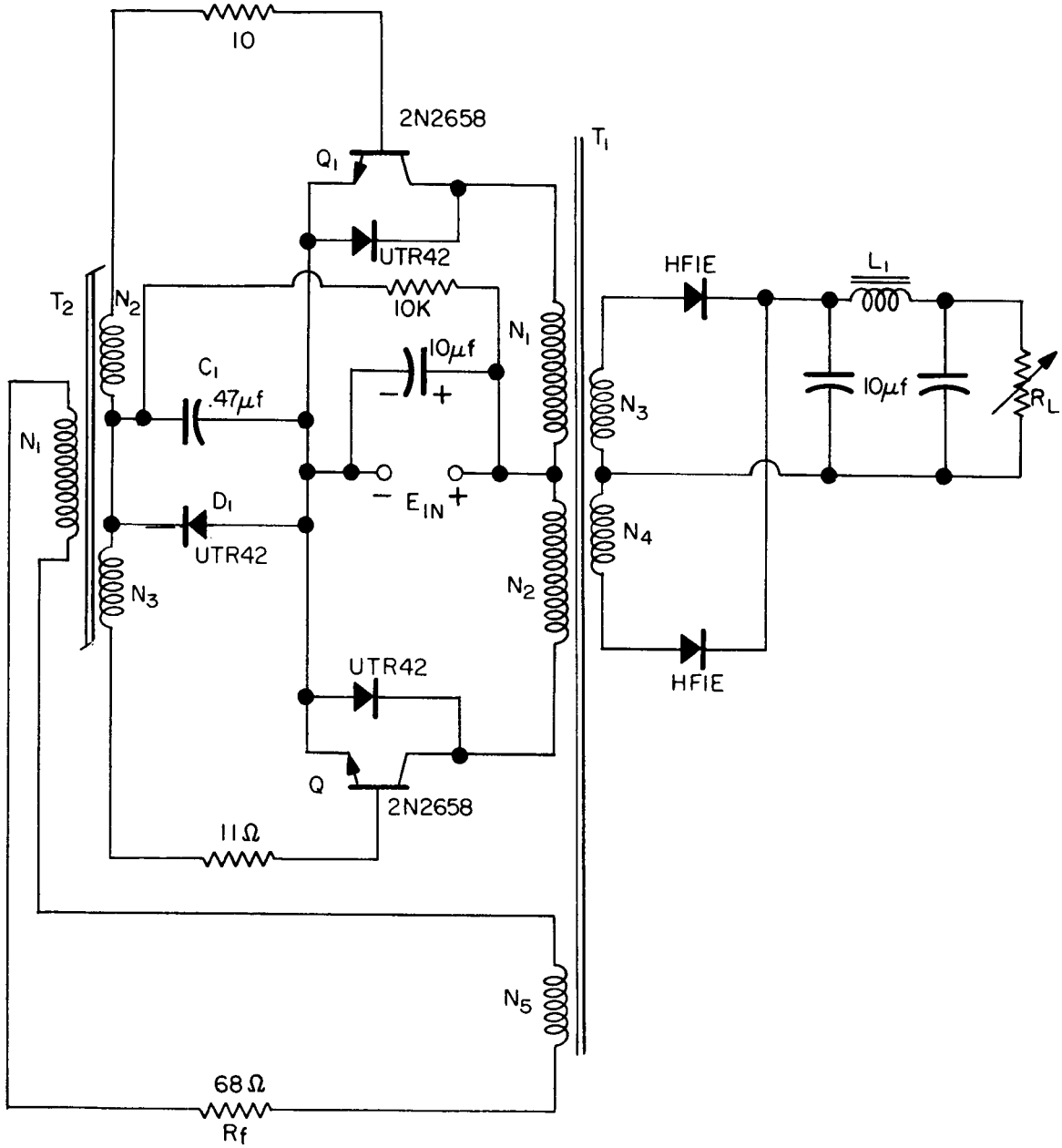
$$P_b = E_b I_b$$

and

$$I_b = \frac{I_{c\ max}}{10} = \left(\frac{P_0}{.8}\right)\left(\frac{1}{E_{in}}\right)\left(\frac{1}{10}\right)$$

where

P_0 = Maximum power output
.8 = approximate overall efficiency
10 = Drive factor for good saturation



T_2 = MAG. INC. 80609-1/8 D
N_1 = 213 TURNS
$N_2 = N_3$ = 106 TURNS
T_1 = INDIANA GENERAL CF-114-03
$N_1 = N_2 = N_3 = N_4$ = 40 TURNS
N_5 = 20 TURNS

E_{IN} = 15 VOLTS

Figure 4–GDC to DC Converter at 25 KHZ

$$E_b = V_{be} + I_b R_b + V_d \approx 2.7 \text{ volts}$$

thus, $P_b = 0.18$ watts.

2. Calculate x:

$$x = 2f\, t_s = (2)(25)(4) \times 10^{-3} = 0.2$$

3. Calculate α_ϕ :

$$\alpha_\phi = \frac{1 - \sqrt{x}}{1 - x} = \frac{1 - \sqrt{.2}}{.8} = 0.691$$

4. Choose core size and material for T_2:

$$W_a \phi_c = \frac{5P_b(1 - x) \times 10^{11}}{f} = \left(\frac{5}{25}\right) \frac{(.18)(.8) \times 10^8}{} = 3.6 \times 10^6$$

Select Core No. 80609 - 1/8D {Mag. Inc.}

$$\phi = 60, \quad \ell = 4.2 \text{ c.m.}$$

5. Calculate n:

$$n = \frac{1.6\pi \ell_m A_c B_m H_c f \times 10^{-8}}{P_b (1 - x)}$$

$$n = \frac{(1.6)(3.14)(4.2)(30)(.15)(25) \times 10^{-5}}{(.18)(.8)} \approx 0.166$$

6. Calculate N_ϕ:

$$N_\phi = \frac{\alpha_\phi E_f (1 - x) \times 10^8}{2f \phi_c}$$

$$N_\phi = \frac{(.691)(7.5)(.8) \times 10^8}{(2)(25)(60)} = 138 \text{ turns}$$

7. Calculate N_b :

$$N_b = \frac{E_b}{E_\phi} \times N_\phi = \frac{(138)(2.7)}{(.691)(7.5)} = 72 \text{ turns.}$$

8. Calculate R_f :

$$R_f = \frac{E_f^2}{P_b} \frac{\alpha_\phi (1 - \alpha_\phi)}{(1 + n)}$$

$$R_f = \frac{(7.5)^2}{(.18)} \frac{(.691)(.309)}{1.166} = 57\ \Omega$$

9. Calculate R_b:

$$R_b = \frac{E_b - V_d - V_{be}}{I_b} = \frac{1.1v}{67 \text{ ma}} \cong 16\ \Omega$$

The power dissipated in the feedback loop, calculated by using Equation (13) and actual values of x, α_ϕ was 0.38 watts, which compares to 0.35 watts measured by the $e\Phi$ and $i\Phi$ photographs of Figure 12.

The circuit in Figure 4 is a modification to that in Figure 2. The modification mainly consists of replacing R_b with a diode and capacitor in parallel, plus the addition of a resistor in each leg of the base drive for the transistors. The diode presents a high impedance to the starting current and, therefore, increases the necessary resistance required for starting; it also presents a high impedance for reverse base current which is required to remove the stored charges in the conducting transistor prior to switching. Consequently, the opposite transistor presents the only path for this reverse current and this would tend to render it conductive. However, capacitor C_1 presents a low impedance path for the required reverse base current and remains charged in the polarity so that the opposite transistor cannot be rendered conductive until the stored charges are removed from the conducting transistor. The resistors in the base lead provide

the necessary adjustment to obtain the best circuit symmetry with the available transistors and associated parameters. The two diodes connected across the collector to emitter of each transistor reduce transient high speed voltage spikes induced during switching to some degree, but do not eliminate them. The diodes were found to exhibit a small degree of inductance prior to conduction, thereby reducing their ability to present a load to the voltage spike.

Selection of the transformer core material necessitated a comparison of the B-H loops for two core materials; ferramic material 03 as manufactured by Indiana General Co., and square permalloy 80, as manufactured by Magnetics, Inc. both of toroidal configuration. The Hysteresis loop of each core material was displayed on an oscilloscope during circuit operation by the technique as shown in Figure 5.

A current probe was used by arranging all the current carrying wires of the transformer in such a way that they cancel out and leave only the magnetizing current to produce a voltage signal proportional to the magnetizing force. This was used for horizontal deflection, and a simple R-C integrator was used for vertical deflection to represent the flux-density excursion. The resultant display is not very accurate, but sufficies to give a fair overall picture of the general shape. Two cases were considered;

1. Effect of load changes
2. Effect of circuit symmetry.

For load changes, a comparison of Figure 6 with Figure 7 indicates that the ferramic core material offers better stability of the B-H loop than the round permalloy 80.

A comparison of Figure 8 with Figure 9 also indicates that the ferramic core material offers better stability for circuit symmetry.

Remarks

Efficiency of the converter was measured under the following conditions:

E_o	P_{out}	E_{in}	P_{in}	N_f
14.93 v	0	15.0	0.6	0
13.86 v	3.6 w	14.97	4.5	80%
13.60 v	8.15 w	14.93	9.56	85%

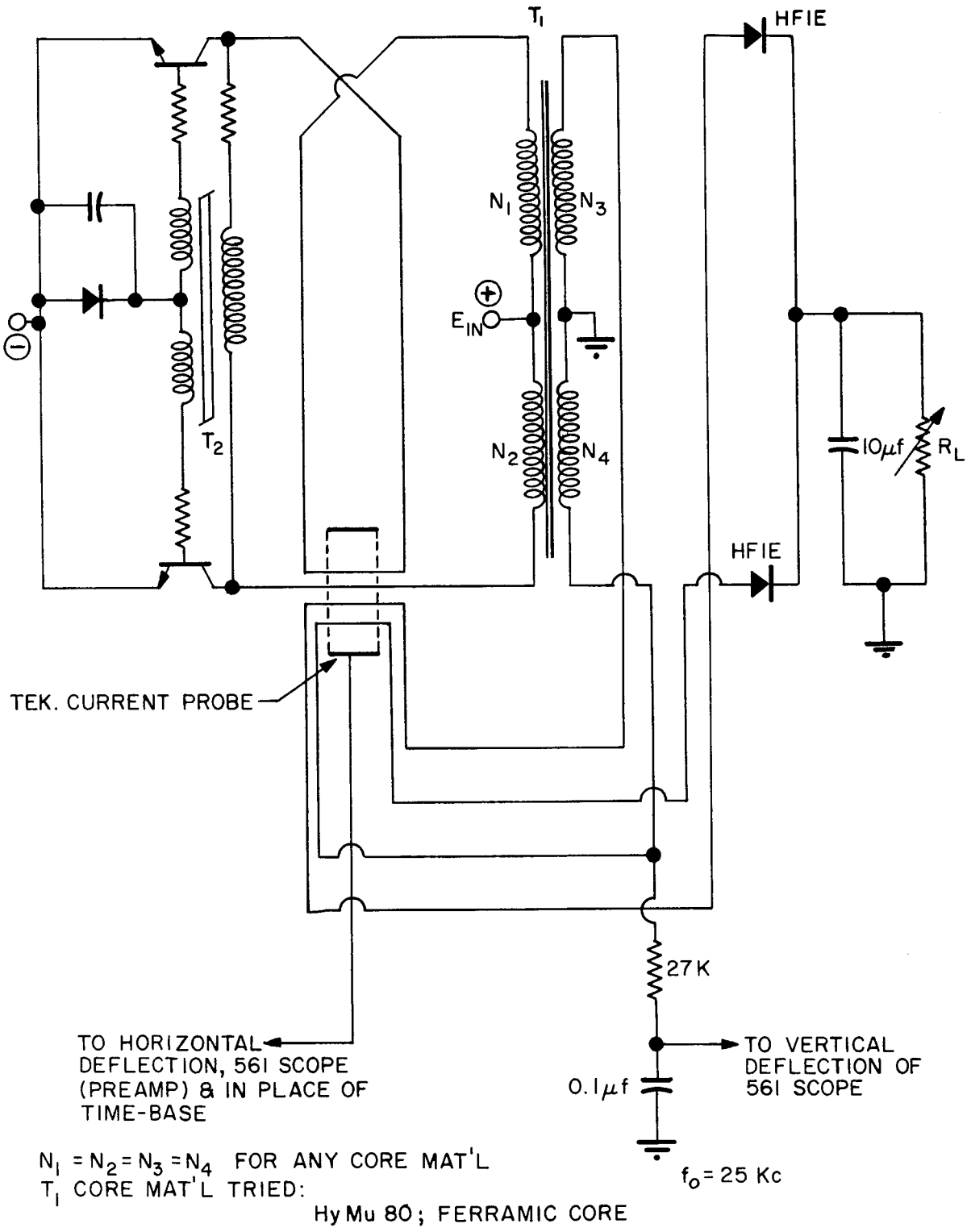
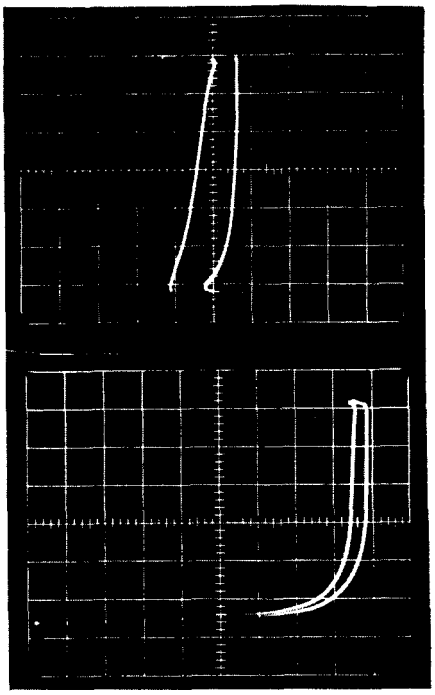


Figure 5–Measurement Technique for Displaying Hysteresis



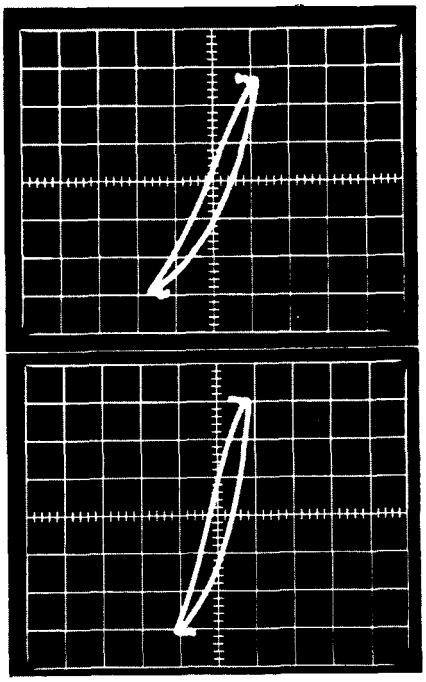
(a)

Converter at no load, horizontal deflections is 20 ma/cm

(b)

Converter at full load, horizontal deflection is 100 ma/cm

Figure 6–In-Circuit Hysteresis Loop, Square Permalloy 80.



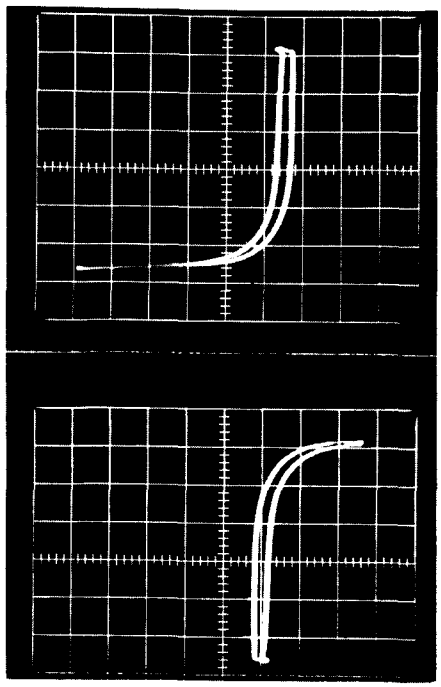
(a)

Converter at no load, horizontal deflection is 50 ma/cm

(b)

Converter at full load, horizontal deflection is 50 ma/cm

Figure 7–In-Circuit Hysteresis Loop, Ferramie 03 Core Material.



(a)

Circuit symmetry unbalanced
by changing base resistor
1 ohm

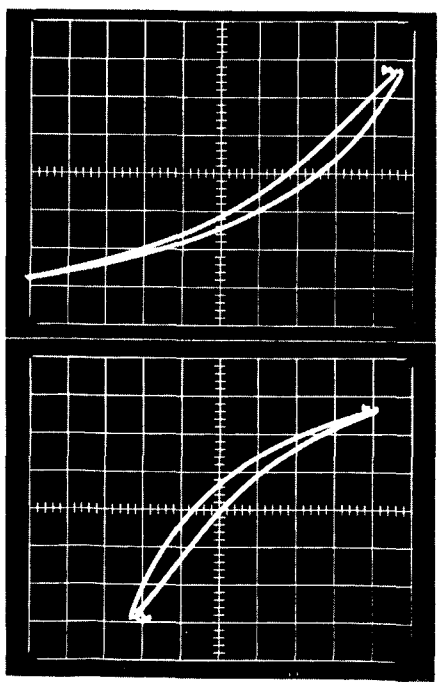
Horizontal deflection 100 ma/cm

(b)

Circuit symmetry unbalanced
by changing base resistor
of opposite side by 1 ohm

Horizontal deflection 100 ma/cm

Figure 8–In-Circuit Hysteresis Loop, Square Permalloy 80 Core Material.



(a)

Circuit symmetry unbalanced
by changing base resistor
one ohm

Horizontal deflection is 50 ma/cm

(b)

Circuit symmetry unbalanced
by changing base resistor
of opposite side by one ohm

Horizontal deflection is 50 ma/cm

Figure 9–In-Circuit Hysteresis Loop, Ferramie 03 Core Material.

Photographs of various waveforms of the circuit were taken and are shown in Figures 10-13.

The procedure outlined for designing the feedback loop proved to be very useful and the approximations used checked favorably with the experimental results. The procedure also applies to lower frequency operation but is not as important as for the higher frequency range.

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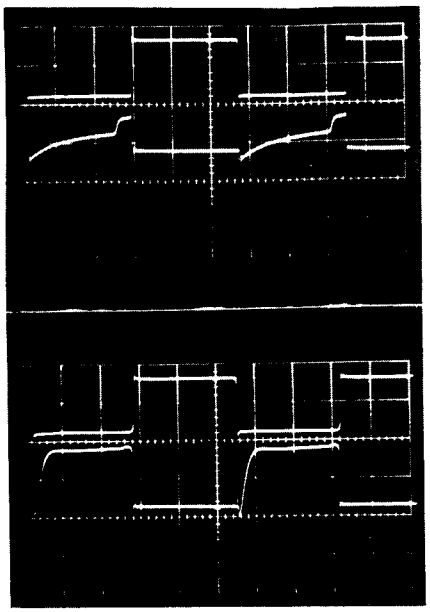


(a) NO LOAD

← V_{ce} = 20 v/cm

← I_c = 50 ma/cm

10 μs/cm

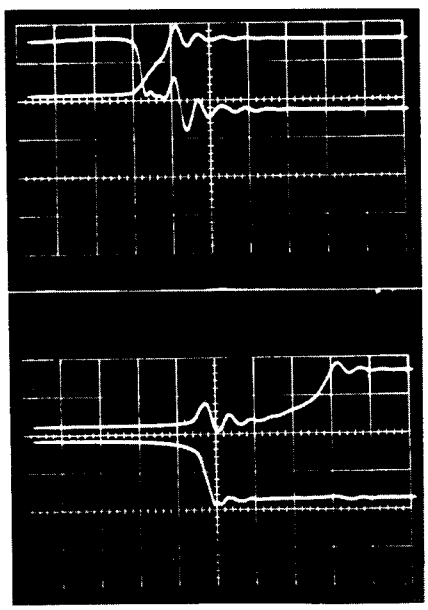
(b) FULL LOAD

← V_{ce} = 20 v/cm

← I_c = 500 ma/cm

10 μs/cm

Figure 10–Switching Characteristics of V_{ce} and I_c.



(a) NO LOAD

← V_{ce} = 20 v/cm

← I_c = 50 ma/cm

.2 μs/cm

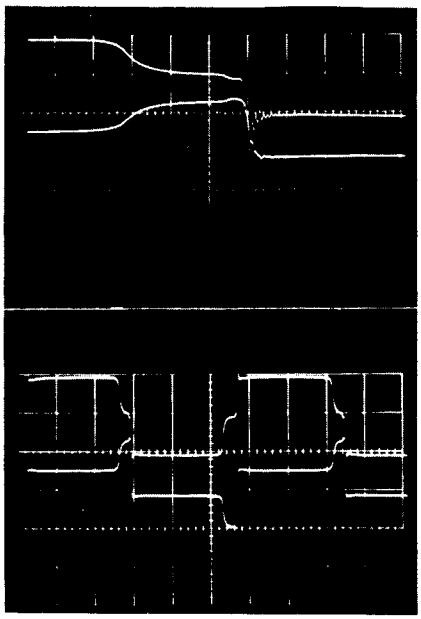
(b) FULL LOAD

← V_{ce} = 20 v/cm

← I_c = 500 ma/cm

.2 μs/cm

Figure 11–Expanded Portion of Switching Characteristics of Vce and I_c.



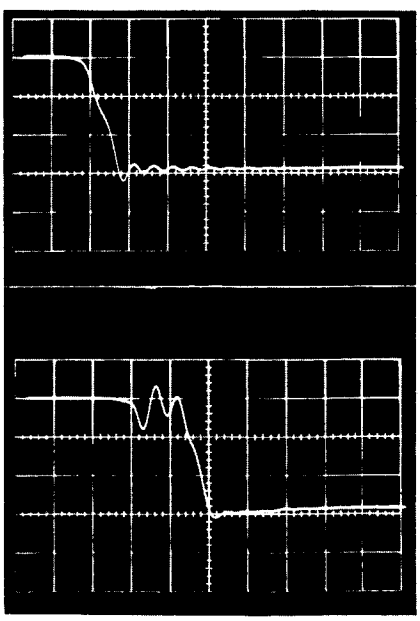
(a)

$e\Phi$ at 5 v/cm
$I\Phi$ at .1 a/cm
1 μ sec/cm

(b)

$e\Phi$ at 5 v/cm
$I\Phi$ at .1 a/cm
10 μ s/cm

Figure 12–Feedback Loop Currents and Voltage Characteristics.



(a) NO LOAD

V_{ce} at 10 v/cm
.2 μs/cm.
Q_1

(b) FULL LOAD

V_{ce} at 10 v/cm
.2 μs/cm
Q_1

Figure 13–Variations of V_{ce} for No Load and Full Load.