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4 QUARTERLY TECHNICAL REPORT

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FOREWORD

This report covers work performed for the Jet Propulsion Laboratory, California Institute of Technology (under JPL ~~Contract~~ 951079) which is sponsored by the National Aeronautics and Space Administration (under NASA Contract NAS7-100). Although the contract starting date was August 17, 1966, work was delayed until September 15, 1966 at the request of the Jet Propulsion Laboratory.

CONTENTS

ILLUSTRATIONS

Section 1
PROGRAM OBJECTIVE AND SPECIFICATIONS

1.1 OBJECTIVE

The objective of this program is to design, fabricate, and test a subsystem consisting of an eight-pole commutator, an associated shift register, and control logic that will meet the functional, electrical, and environmental requirements defined in JPL Specification GMN-50524-DSN-A. The latest state-of-the-art developments in MOS technology are to be applied wherever possible.

1.2 FUNCTIONAL REQUIREMENTS

JPL Specification GMN-50524-DSN-A is enclosed in the Appendix. The following statement is quoted from the specification:

> "Functional requirements: The commutator shall function so that it switches sequentially each of eight analog voltage inputs to a common output line as illustrated in Fig. 1. A quaded deck switch shall be provided for the control of the analog voltage output. The commutator shall contain a second set of eight switches for multiplexing variable-resistance sensors (see Fig. 2). Certain logic functions shall be provided to control the operation of the shift register and the deck switch. Figure 1 illustrates the complete functional representation of the required logic with the following exception. If the shift register is designed with a logical delay between clock line activation (logic "1") and the activation of any stage output, an equivalent delay shall be provided in line X. This is necessary in order for the deck switch to be activated and deactivated in phase with the analog switches."

Section 2

PROGRAM DEFINITION

The steps listed below define the program which will be followed in order to develop and manufacture the required hardware.

1. Preliminary Study
2. Design
   - Block Diagram
   - Schematic Diagram
   - Logic Diagram
   - Timing Diagram
3. Breadboard Verification of Design
4. Development of Environmental Test Plan
5. Drafting - Logic Diagram and Schematic Diagram
6. Production of MOS Composite
7. Production of Masks
8. Evaluation Run - Pilot Line
9. Testing of Evaluation Wafers
10. Final Run - Pre-Production Line
11. Testing of Production Wafers

Section 3
STATUS REPORT

During the preliminary study, a worst-case voltage analysis of the subsystem revealed that devices manufactured by the process, which has been standard at the Philco-Ford Corporation facility, would not withstand the applied voltages if the subsystem were faulted as specified by section 3.5.1.7 of the JPL specification. A change in the Philco-Ford Corporation manufacturing process has been made which allows production of devices with the required breakdown voltage.

3.1 PRELIMINARY STUDY

During the preliminary study, three alternative implementations of the shift register (section 1.1) were considered:

- three-stage counter and decoder
- static shift register
- dynamic shift register

3.1.1 Three-Stage Counter and Decoder

A counter would require only three stages; however, the decoding of eight states would be required. The large number of interconnections required precluded use of this implementation.

3.1.2 Static Shift Register

A static shift register, such as that illustrated in Fig. 3-1, requires 19 active devices per stage. This is a relatively high device count when compared to the seven devices per stage required by the dynamic shift register.

3.1.3 Dynamic Shift Register

In contrast to the static shift register, which requires only one clock input, the dynamic shift register illustrated in Fig. 3-2 requires three clock inputs. The dynamic shift register, however, requires fewer active devices per stage and fewer crossovers than the static shift register. The simplicity of this implementation has resulted in a higher manufacturing yield than any other implementation.

3.2 DESIGN

The design phase is currently underway. The schematic diagram, block diagram, and logic diagram will be completed and the design-verification breadboard will be constructed during December and January.

Figure 3-3 shows the schematic and timing diagrams of the three-phase clock generator to be incorporated into the commutator.

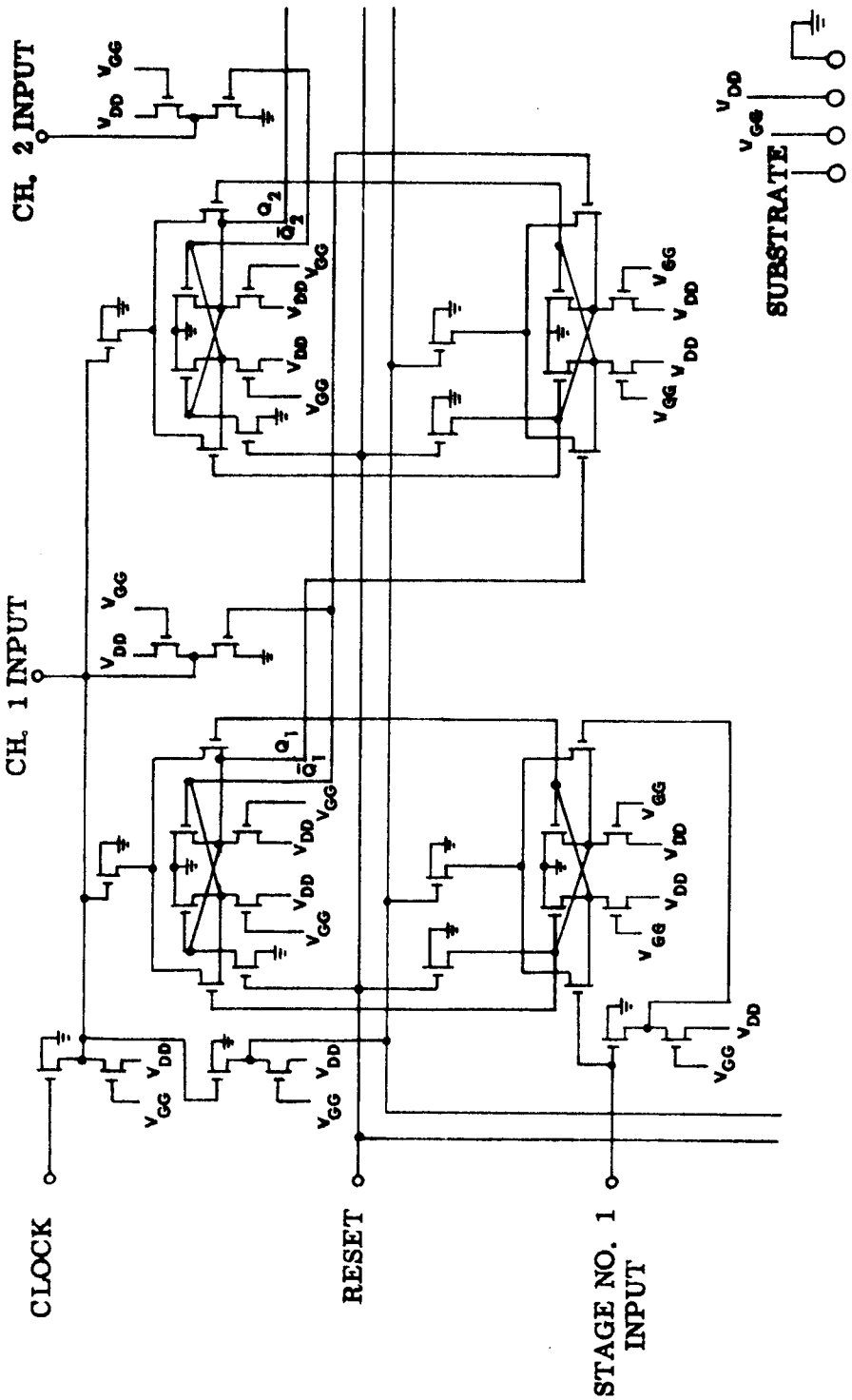

Fig. 3-1 Schematic Diagram of Static Shift Register

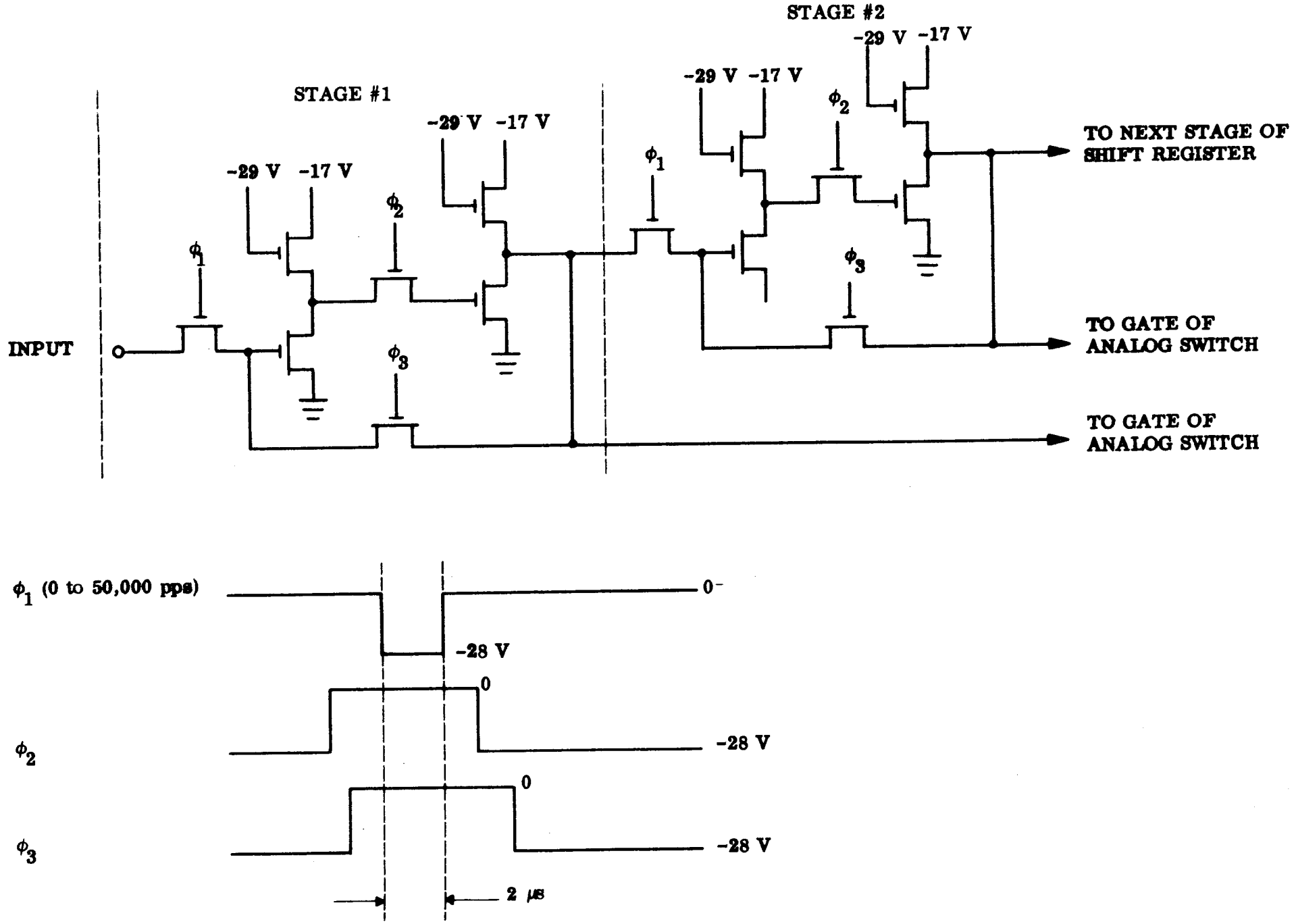

Fig. 3-2 Schematic Diagram and Timing of Dynamic Shift Register

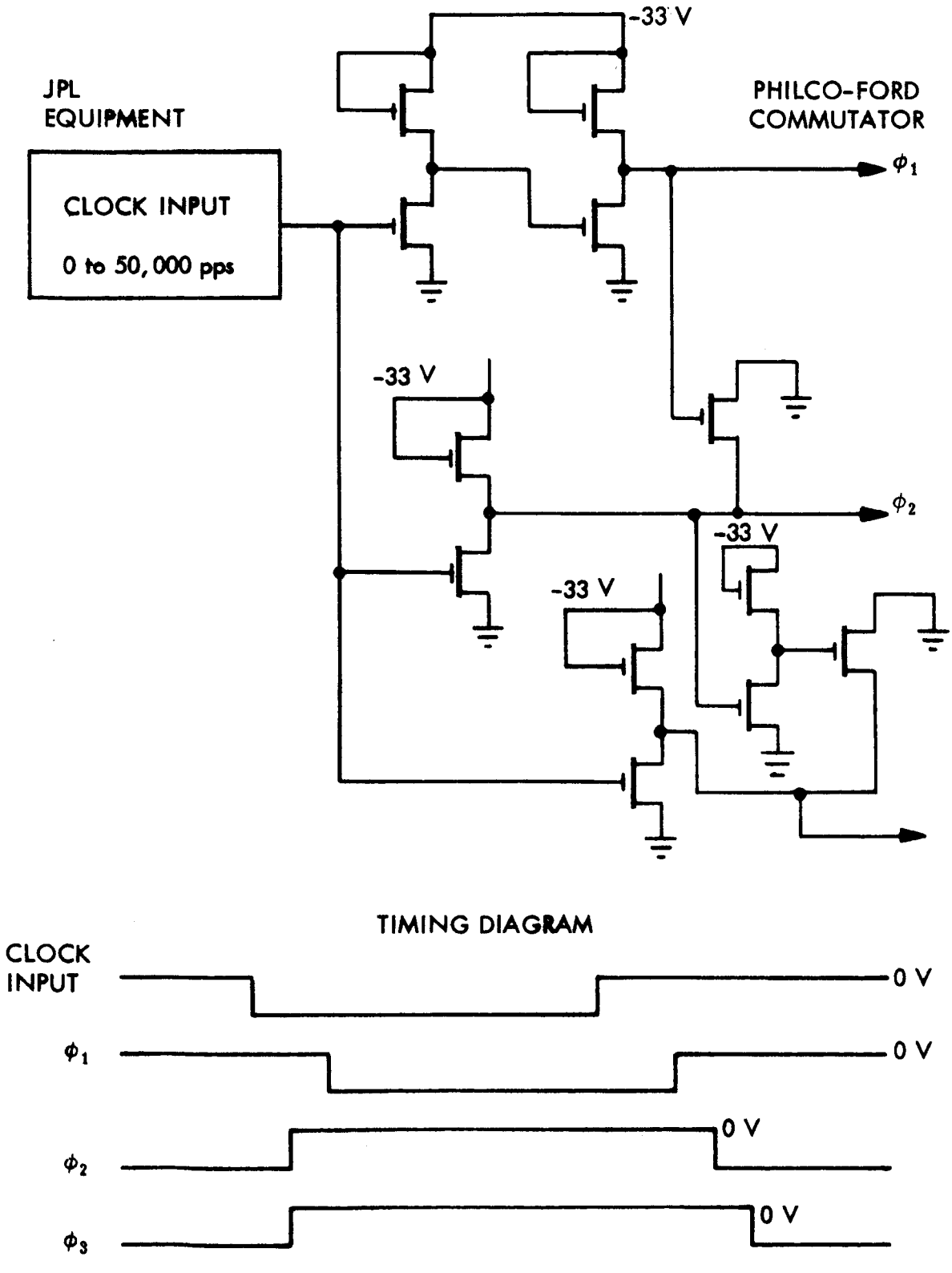

Fig. 3-3 Schematic Diagram of Three-Phase Clock

Section 4
TECHNICAL PROBLEMS

The only technical problem encountered concerned the capability of Philco-Ford Corporation to produce a commutator with a layer of oxide insulation to withstand the specified worst-case voltages. Current experiments indicate that a considerable margin of safety with respect to device breakdown voltage will be available in the devices to be built under this contract. Essentially, the desired effect has been achieved merely by lengthening the time period during which the oxide layer is deposited without changing any other steps in the Philco-Ford Corporation manufacturing process. Substantiating evidence is currently being gathered and evaluated.

Section 5
WORK PLAN FOR THE NEXT QUARTER

During the next quarter, steps 3 through 6 of the program defined in Section 2 will be started and steps 2, 3 and 5 should be completed.

APPENDIX

JPL SPECIFICATION
GMN-50524-DSN-A

JET PROPULSION LABORATORY
CALIFORNIA INSTITUTE OF TECHNOLOGY
PASADENA, CALIFORNIA

JPL SPEC GMN-50524-DSN-A

DATE: 5 April 1966

DESIGN SPECIFICATION
SPACECRAFT FLIGHT EQUIPMENT
TELEMETRY SUBSYSTEM
INTEGRATED CIRCUIT COMMUTATOR

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A		5-4-66	

REV	AMEND	DATE	AUTHORITY

CONTENTS

CONTENTS (cont)

ILLUSTRATIONS

TABLES

1. SCOPE

1.1 This specification describes the electrical, environmental, and quality assurance requirements for a silicon Integrated Circuit (IC) Commutator, using solid state analog switches operating on the Field-Effect principle. The commutator is to be clocked in sequence at any rate from dc to 50,000 pulses per second (pps). The requirements contained herein are minimum, and should reflect worst case hardware. Microminiaturized techniques are to be used in an effort to reduce size, weight, and power consumption, but still maintain high performance and reliability.

2. APPLICABLE DOCUMENTS

Not applicable.

3. REQUIREMENTS

3.1 Materials, parts and processes. Materials, parts, and processes used in the design, fabrication, and assembly of the items covered by this specification shall conform to the applicable documents specified herein. The contractor's selection shall assure the highest uniform quality and condition of items; such selection shall be subject to the approval of JPL. The use of magnetic materials is not preferred, but will be allowed.

3.2 Request for deviations. In the event that this specification does not cover all areas of design that the supplier must consider, JPL shall be informed in writing of the supplier's design goal. The supplier shall await JPL's direction in the matter.

3.3 Interchangeability. All parts having the same part number shall be directly and completely interchangeable with respect to installation and function.

3.4 Design requirements.

3.4.1 Design objective. The commutator shall be designed for optimum operation in accordance with the following priority list:

a. Reliability. Reliability is considered to be of prime importance, and can be achieved only by careful and thorough analysis, design, development, fabrication, and testing.
b. Noise immunity.
c. Minimum power consumption.
d. Packaging density expressed as number of circuits per flatpack.

3.4.2 Functional requirements. The commutator shall function so that it switches sequentially each of eight analog voltage inputs to a common output line as illustrated in Figure 1. A quaded deck switch shall be provided for control of the analog voltage output. The commutator shall contain a second set of eight switches for multiplexing variable resistance sensors (see Figure 2). Certain logic functions shall be provided to control the operation of the shift register and the deck switch. Figure 1 illustrates the complete functional representation of the required logic with the following exception. If the shift register is designed with a logical delay between clock line activation (logic "1") and the activation of any stage output, an equivalent delay shall be provided in line X. This is necessary in order for the deck switch to be activated and deactivated in phase with the analog switches.

3.4.2.1 Control functions. The function of the three control inputs are:

a. Deck switch control input:

logical 0 = deck switch deactivated at all times
logical 1 = deck switch activated when the deck control flip-flop is in the "set" condition.

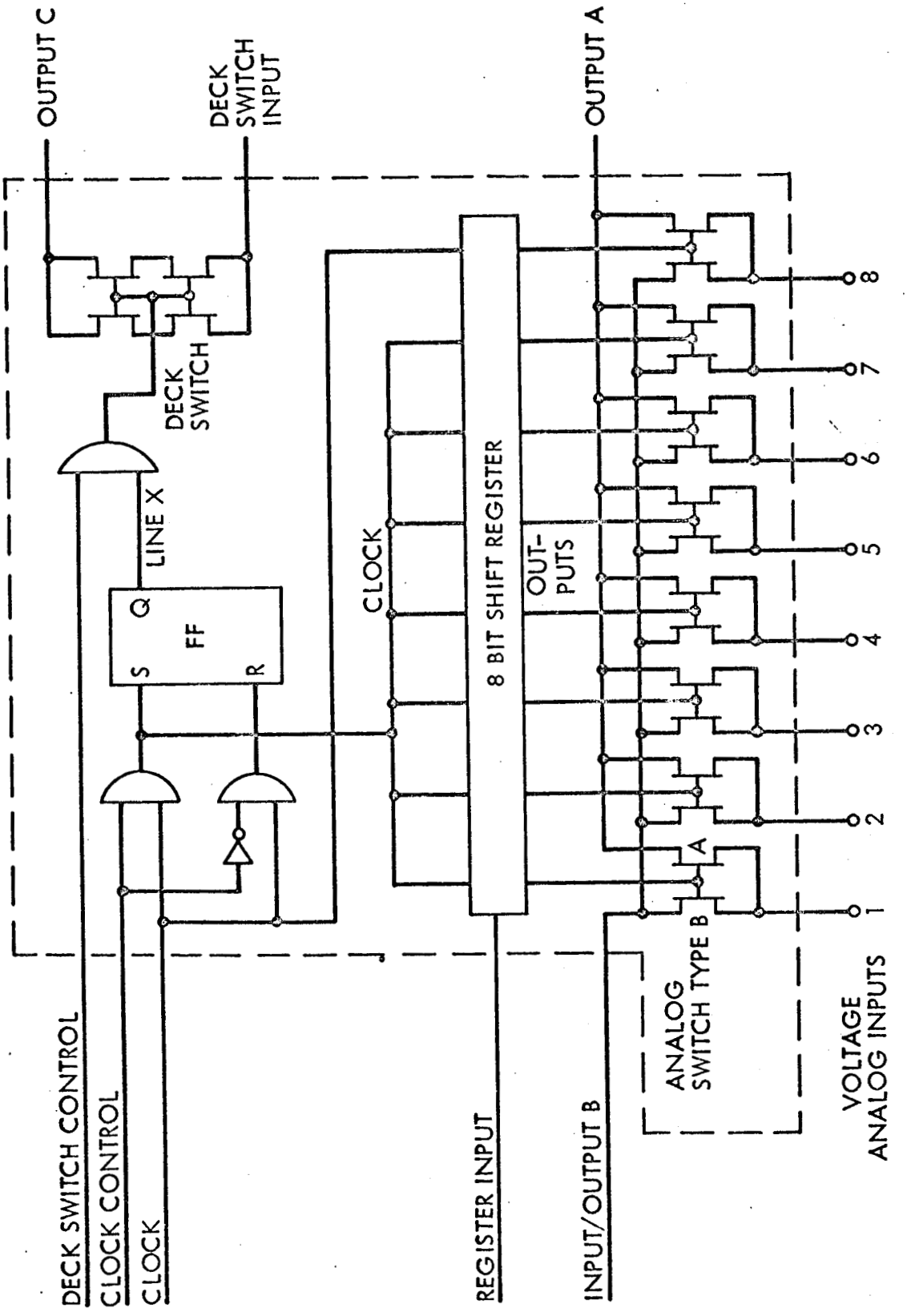

Figure 1. Commutator Functional Block Diagram

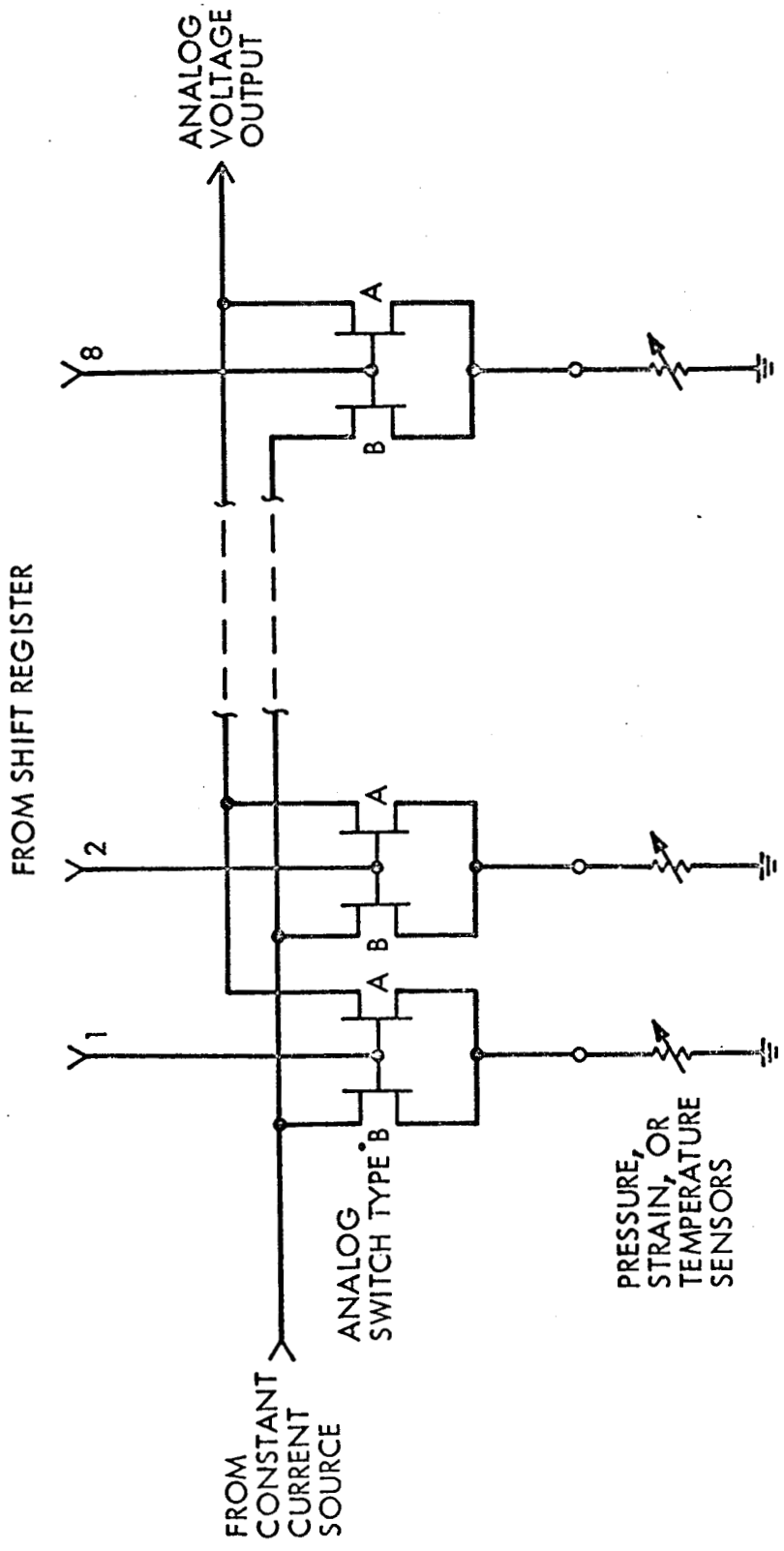

Figure 2. Variable Resistance Sensor Multiplexing

b. Clock control input:

logical 0 = clock input blocked from the first seven stages of the shift register.
logical 1 = clock input connected to the first seven stages of the shift register.

c. Shift register input:

logical 0 = a logical 0 will appear at the output of the first shift register stage during the next clock cycle.
logical 1 = a logical 1 will appear at the output of the first shift register stage during the next clock cycle.

3.4.2.2 Shift register functions. When a logical "1" is applied to the shift register input it shall be transferred to the output of the first register stage during the first succeeding gated clock cycle. When a logical "1" appears at the output of the first stage, the pair of analog switches connected to that stage shall be activiated. The logical "1" shall be transferred along the register one stage per clock cycle. In normal operation the "1" is removed from the register input after the first clock cycle. The transfer of the single "1" state along the register shall result in the analog switch pairs being activated, one at a time, in direct sequence. The register shall be open ended so that after the single "1" state is shifted out of the eighth stage, the register will contain all "0" states and remain that way on successive clock cycles until a logical "1" is once more applied to the input.

3.5 Performance and product characteristics. The commutator shall meet all requirements of this section.

3.5.1 Analog and deck switch requirements.

3.5.1.1 Impedance (switch open). The dc impedance across each analog switch and across each series-parallel deck switch shall be greater than 1000 megohms when deactivated or open.

3.5.1.2 Leakage current. The leakage currents measured at outputs A and B shall be less than 40 nanoamperes each, when all sixteen analog switches are open with their inputs at +5 volts, and all power supplies connected to the commutator. The leakage current at output C shall be less than 5 nanoamperes when the deck switch is open, with +5 volts on the deck switch input and all power supplies connected to the commutator.

3.5.1.3 Impedance (switch closed). The dc impedance across each switch, when activated, shall be 2000 ohms ±50 percent for analog types A and B, and 1000 ohms ±50 percent for the deck switch. The impedances shall be measured with the signal currents specified in 3.5.1.6.

3.5.1.4 Source resistance. The commutator shall meet the requirements of this specification when the analog voltage signal inputs, 1 through 8, are supplied from a source resistance that is from less than 1 ohm up to 2500 ohms.

3.5.1.5 Load impedance. The commutator shall be designed to operate with a load impedance at output A, AB (A and B connected together) or C of 1 to 10 megohms in parallel with 10 picofarads.

3.5.1.6 Input signal. The signal voltage at the eight analog inputs shall be 0 to ±5 volts. The source to drain signal current shall be 0 to ±5 microamperes in the type A analog and deck swtiches, and 0 to 1.5 milliamperes in the type B analog switches.

3.5.1.7 Fault voltage. The analog switches shall not be damaged when any voltage from +8 to -8 is applied to any of the analog inputs. The source resistance of the fault voltage shall be less than 1 ohm.

3.5.1.8 Fault current. The analog switches shall be capable of carrying, without damage, the fault current generated when all analog switch pairs are simultaneously activated, and a voltage differential of 5 volts is at the inputs. For example, the input of one switch pair might be at ±5 volts and the inputs of the other seven switch pairs at 0 volts. A source resistance of less than 1 ohm shall be assumed.

Note: This shall not apply if the commutator is designed to avoid the possibility of more than one analog switch pair being simultaneously activated at power turn-on.

3.5.2 Commutator requirements.

3.5.2.1 Signal error. Commutator signal error is defined as the difference between the input analog voltage (Ei) and the resultant output analog voltage, for any input, when the commutator is in operation. Table I defines four operational configurations for the commutator. In all configurations the input voltage is applied to the analog voltage input terminals and the designated output measurement point is loaded with a 1 megohm resistor and 10 picofarads capacitance in parallel. Under the power supply and temperature variations specified herein, the error measured in the various configurations shall not exceed the values given in Table I. The error measurement shall be made with the commutator operating at a clock rate of 50,000 pps. The output (or error) voltage shall reach a stable, steady state level within 10 microseconds after it crosses the 10 percent amplitude point, as shown in Figure 3. The output (or error) voltage shall be read at the 10 microseconds point. When a measurement is being made on one analog switch, or switch pair, all other input terminals shall be connected to the worst case voltage level for the input range.

Table I. Maximum Commutator Error

Config-uration	Connections From	Connections To	Input Range 0 to ±250 mvdc	Input Range ±250 mvdc to ±5 vdc	Error at Output
I	-	-	±1.0 mvdc	±0.4% of Ei	A
II	Output A	Output B	±0.5 mvdc	±0.2% of Ei	AB
III	Deck Switch Input	Output A	±1.5 mvdc	±0.6% of Ei	C
IV	Deck Switch Input	Outputs A & B	±1.0 mvdc	±0.4% of Ei	C

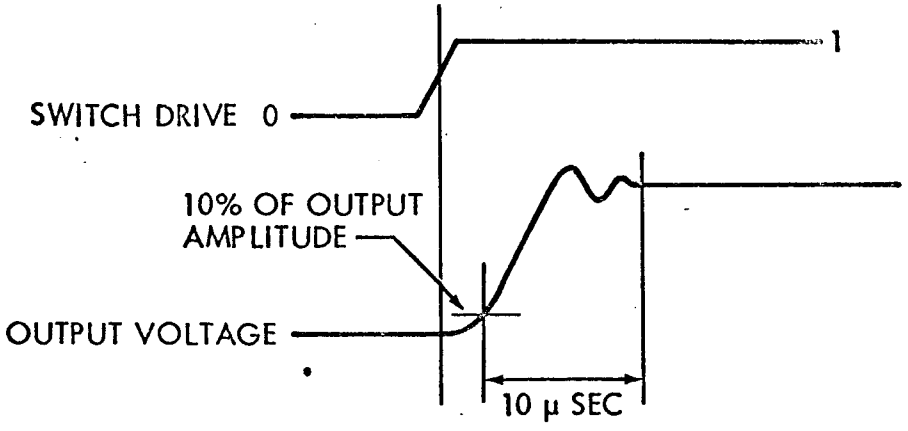

Figure 3. Output Waveform in Error Measurement

3.5.2.2 Power. Power requirements shall be in accordance with the following criteria.

a. Power consumption. Under all temperature conditions and power supply variations specified herein, the power consumption of the commutator shall be less than 75 milliwatts.

b. Power supply voltages. The nominal power supply voltages shall be defined by the contractor and are subject to JPL approval.

c. Static voltage regulation. The commutator shall meet all requirements of this specification when operated from power sources which have a static voltage regulation (variations less than 1 cps) of ±10 percent.

d. Turn-on sequence. Random power or logic turn-on sequence shall not damage the commutator.

e. Overvoltage. The commutator shall not be damaged by an overvoltage 50 percent greater than the nominal value on any one power source or overvoltages simultaneously on all power supplies 25 percent greater than the nominal value.

3.5.2.3 Switch overlap time. Switch overlap time is defined as the period of time when two adjacent analog switch pairs are simultaneously activated. Switch overlap time between any adjacent switches shall not exceed one microsecond when the commutator is operated under any combination of conditions specified herein.

3.5.2.4 Control and timing signals. The commutator shall operate from the digital control signals specified in 3.4.2.1 and a clock signal. The logic voltage levels of these signals shall be defined by the contractor, subject to JPL approval, and shall be the same for all four signals.

3.5.2.4.1 Clock signal. The clock signal shall be 0 to 50,000 pps with a minimum pulse width of 2 microseconds.

3.5.2.5 Noise margins. The commutator shall not malfunction under the following noise conditions:

a. Power line noise.

Frequency - 1 to 100,000 cps.

Amplitude - ±10 percent of the nominal power supply voltage superimposed on the actual voltage within its static regulation limits.

b. Control and timing signal noise.

Frequency - 1 to 100,000 cps.

Amplitude - shall be specified by the contractor, subject to JPL approval.

3.6 Fabrication, packaging and marking requirements.

3.6.1 Fabrication. All elements of the commutator, shown in Figure 1, shall be fabricated on a single silicon chip.

3.6.2 Packaging. Each commutator chip shall be packaged in a flatpack that is a standard item for the contractor. The contractor's choice of package shall be subject to JPL approval.

3.6.2.1 Flatpack leads. The flatpack leads shall be solderable and weldable. The lead spacing shall be 0.050 inch. All leads shall be able to withstand a two ounce pull for a period of five minutes without damage to the lead or the commutator. The commutator shall not become damaged when the leads are immersed in molden 60/40 solder (without flux) at a temperature of 230 ±5°C, for 15 seconds. The leads shall be immersed to within 0.020 inch of the body of the flatpack.

3.6.2.2 Flatpack markings. All commutator flatpacks shall be marked with the contractor's symbol, part number, serial number, and manufacturing date code. The markings shall be legible after prolonged exposure to the maximum temperature specified herein.

3.6.2.3 Hermetic seal. Each commutator flatpack shall be hermetically sealed to pass the following tests.

a. Gross leak test. Each commutator flatpack shall be submerged in a pyrex beaker of ethelene glycol at 100°C, for at least 15 seconds. The flatpack has failed the test if any bubbles emanate from the flatpack case.

b. Small leak test. Each commutator flatpack shall be subjected to helium gas at a pressure of 60 psig, and maintained at this pressure for 4 hours ±30 minutes. Upon removal from the pressurized helium, the flatpack shall then be allowed to stabilize for one hour in helium gas at one atmosphere. The flatpack shall then be air-washed and subjected to a Vecco leak test within 30 minutes after removal from the helium.

If the flatpack has been out of the helium atmosphere more than 30 minutes, but less than 3 hours, it shall be repressurized in helium at 60 psig, for one hour before testing. If a period of 3 hours is exceeded before testing, the test shall be aborted, and started again. The flatpack has failed the test if the leak rate is in excess of 5×10^{-7} cc of helium per second.

3.7 Environmental requirements. Each commutator shall be designed, fabricated, and packaged to operate within the requirements of this specification during or after the following environmental tests.

3.7.1 Temperature.

3.7.1.1 Operating temperature. Each commutator shall operate properly with case temperatures in the range of -25 to +85°C.

3.7.1.2 Storage temperature. The commutators shall not be damaged by storage temperatures in the range of -55°C to +150°C.

3.7.1.3 Nonoperational thermal shock. The commutator (nonoperating) shall be subjected to 10 cycles of thermal shock. Each cycle shall consist of 15 minutes at -65°C, 5 minutes at +25°C, 15 minutes at +160°C, and 5 minutes at +25°C, in immediate succession.

3.7.2 Acceleration.

3.7.2.1 Nonoperational constant acceleration. The commutator flat-packs shall be subjected to a constant acceleration of 20,000 g's for one minute in each of three mutually perpendicular planes.

3.7.2.2 Nonoperational shock. The commutator shall be capable of withstanding five, 0.2 millisecond, 3000 g shocks in each of three mutually perpendicular planes (total of 15 impacts).

3.7.2.3 Operational vibration. The commutator shall operate properly while being subjected to a 20 g rms sinusoidal vibration sweep from 20 to 2000 cps and back to 20 cps, during a five minute period, in each of three mutually perpendicular directions.

3.7.3 Space radiation. The commutator shall be designed to operate properly (taking into account present knowledge of radiation effects) while being subjected to the following radiation environment:

a. Time integrated (equivalent to one year in space) proton flux of 5.0×10^{10} protons/cm^2 ($E > 30$ Mev).
b. Peak electron flux of 1.0×10^{9} electrons/cm^2/second ($E > 0.5$ Mev).

4. QUALITY ASSURANCE PROVISIONS

4.1 Contractor inspection. The contractor shall perform the receiving, in-process and final inspections necessary to assure that the commutators conform to all the requirements of applicable specifications.

4.2 Test methods. Tests shall be performed in accordance with the methods specified in the applicable statement of work.

5. PREPARATION OF DELIVERY

5.1 Preparation for delivery shall be as specified in the contract or procurement instrument.

6. NOTES

Not applicable.