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SQUARING COUNTER** 4

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FINAL REPORT

**INTEGRATED TUNNEL-DIODE/TRANSISTOR
SQUARING COUNTER**

Contract NAS-9657

FOREWORD

This technical report is the final report on NASA contract NAS-9657, entitled "Development of Tunnel Diode Packaging Interconnection and Readout Techniques." The work was administered by the Goddard Space Flight Center, Greenbelt, Maryland. Mr. D. H. Schaefer was the Technical Officer for NASA.

The contract was conducted by the RCA Applied Research department in Camden, New Jersey, under the direction of J. A. Brustman, Manager, Computer Advanced Product Research, and N. S. Parks, Leader, Fabrication and Memory Techniques. The development on the contract was performed by H. R. Kaupp, R. E. Herr, F. V. Henuset, H. C. Nichols, F. Fowler, T. R. Mayhew, J. J. Surina, and A. W. Gellert. The report was written by H. R. Kaupp. 90

SUMMARY

Tunnel diode circuits can operate at frequencies over 10 MHz while dissipating less than 1 milliwatt of power. To demonstrate the advantages of hybrid tunnel-diode/transistor integrated circuits in spacecraft, a squaring counter system was built. The system performs the sum of squares operation on bursts of pulses appearing at the input.

The basic counting is performed by Chow type tunnel diode circuits. Output circuits amplify the tunnel diode logic levels of 400 mV up to 4 V, for compatibility with circuits outside the system. An important feature of this system is active delay circuits which provide 80 nanoseconds of delay with no degradation of risetime.

The circuits are packaged in 0.35 inch high TO-5 cans (0.35 inch in diameter). The circuit modules are soldered on two multilayer printed circuit boards having two signal wiring planes, two ground planes and three power supply planes. The entire system of 27 circuit modules is housed in a 3 inch x 3 inch x 1.5 inch aluminum box, which is constructed to keep out undesirable signals.

The individual counters are capable of running at 17 MHz, and the system can receive inputs at a 4-MHz rate. The power dissipation of the entire system is less than 15 mW.

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Section I

INTRODUCTION

Tunnel diodes and transistors used together in digital circuits provide advantages not obtained by either device alone. Of primary importance is the ability to obtain high-speed operation at low power levels with reasonable component and power supply tolerances. These attributes are especially attractive for spacecraft application, where power dissipation is a principal concern, but where high speed computation can reduce the amount of data that must be transmitted back to earth.

On the other hand, the use of tunnel diodes, which have signal swings of less than 0.5 volt, introduces problems. The circuits must be relatively insensitive to noise and able to communicate with transistor circuits having much larger signal swings.

This project was initiated to develop microelectronic packaging techniques for hybrid transistor/tunnel-diode integrated circuits. In particular the goals were:

- 1) To package the Chow-type tunnel diode counter as modified by Bush² in a TO-5 can. This counter should be capable of operating at 15-MHz rates and should dissipate less than 1 mW of power.
- 2) To develop a buffer, or output, circuit which will simultaneously isolate the counter from external noise signals, while amplifying the tunnel diode signal to levels compatible with transistor logic circuits.
- 3) To develop packaging techniques that will ensure proper functioning of the small signal circuits in a noisy environment.
- 4) To build a suitable system to demonstrate the circuits and packaging techniques.

To accomplish these objectives a squaring counter system was built. The system gives the square in binary of the number of pulses received at the count input within a given period of time. This square is automatically added to the sum of the squares obtained previously.

The system utilizes 10 counter stages, which are capable of counting at a 17-MHz rate. The system can receive pulses at a 4-MHz rate. The total power dissipation for the system, which is composed of 27 circuit modules, is less than 15 milliwatts.

Section II

SYSTEM CONSIDERATIONS

First, the basic operation of the system will be described. Then the mathematical basis for how this operation is accomplished will be discussed. Finally the equations will be derived that describe the system timing.

A. BASIC OPERATION

The system is shown in Fig. 1. Counter stages T_1 through T_4 compose the linear counter; they contain, in binary form, the total number of pulses received at count input A. Counter stages T_{11} , T_{12} and T_5 through T_8 make up the square, or output, counter. This counter contains, in binary form, the sum of the squares of previous groups of input pulses. The number of pulses in a group are determined by the interval between linear resets.

For example, assume all counter stages are reset to zero. Now if four pulses are received at input A, the linear counter contains binary 4 ($T_3 = "1"$; $T_1, T_2, T_4 = "0"$) and the square counter will contain 16 ($T_7 = "1"$; all others = "0").

Now if linear reset signal RL is applied, the linear counter will be reset to zero, but the squaring counter will still contain 16. Suppose that now three pulses are received at input A. The linear counter will contain 3 and the squaring counter contain $16 + 8 = 24$. But the square of 3 is 9, not 8! Now an additional function of linear reset signal RL will be seen; it must add one to the squaring counter when the number squared is odd.

For an odd number of pulses at the input, the RL signal (acting through G4) triggers T_{11} , the least significant bit of the squaring counter. If one were interested

only in approximate squares (to within one binary digit) G_4 , T_{12} and T_{11} could be eliminated. Of course in this case the counter outputs would indicate that the sum of a long string of ones squared was zero, when in fact it might be approaching infinity.

Before the detailed working of the system is discussed, it will be well to examine the mathematical basis for assembling the system as it is in Fig. 1.

B. SQUARING A BINARY NUMBER

The general representation of a binary number, x , is

$$x = a_0 2^0 + a_1 2^1 + a_2 2^2 + a_3 2^3 + \dots a_n 2^n \quad (1)$$

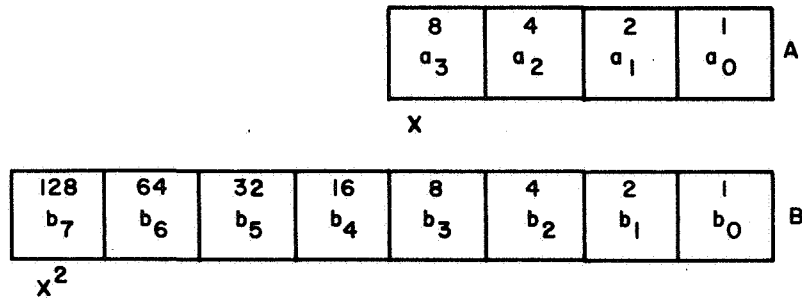
Squaring and reducing Eq. (1) yields

$$\begin{aligned} x^2 = & (a_0 a_0) 2^0 + (a_0 a_1 + a_1 a_0) 2^1 + (a_0 a_2 + a_1 a_1 + a_2 a_0) 2^2 \\ & + (a_0 a_3 + a_1 a_2 + a_2 a_1 + a_3 a_0) 2^3 + (a_1 a_3 + a_3 a_1) 2^4 + (a_2 a_3 + a_3 a_2) 2^5 + \dots \end{aligned} \quad (2)$$

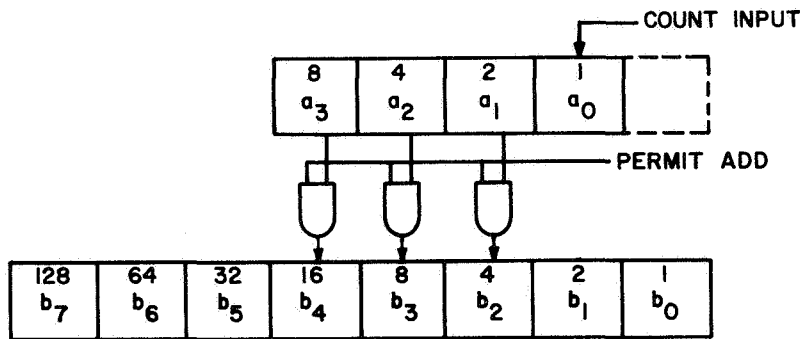
There are two points of note in Eq. (2). First, the 2^0 term of x^2 is identical to that of x . Second the 2^1 term of x^2 is absent, or always zero. Consequently, the first two bits of the x^2 register need not exist for the squaring operation. For summing the squares, however, the first two bits are required.

Now the logical construction of the squaring counter will be discussed. Consider a counter-register, A, containing x and another counter register B containing x^2 , as shown in Fig. 2(a). If 1 is added to the contents of the A register, the B register must now contain

$$(x + 1)^2 = x^2 + 2x + 1. \quad (3)$$



(a) The A register contains x ; the B register contains x^2 .



(b) The B register being triggered by the A register such that $2x$ is added to x^2 .

Fig. 2. Squaring a binary number.

But the B register already contains x^2 ; consequently, it is simply necessary to add the quantity $2x + 1$ to it. To multiply a binary number by 2 it is only necessary to shift the number one digit to the left. Consequently, to add $2x$ to x^2 , a_1 triggers b_2 , a_2 triggers b_3 , and a_3 triggers b_4 , as shown in Fig. 2(b). Since the b_1 bit is always zero, as indicated in Eq. (2), a_0 does not trigger b_1 . Also from Eq. 2, the b_0 bit is identical to a_0 . Therefore if only the square were required, rather than the sum of squares, the B counter register would not need bits b_0 or b_1 .

Before discussing the sum of squares operation, it will be well to go through the squaring procedure. In Fig. 2b the "permit add" signal, in conjunction with the AND gates, allows the A register to settle down before the B register is triggered. For this discussion assume that the b_1 and b_0 bits are inoperative and let the a_0 bit serve for the least significant bit of both counters. The successive changes in the register states in response to the count input are shown in Fig. 3.

NUMBER OF COUNT INPUT PULSES	a_3 8	a_2 4	a_1 2	a_0 1	OUTPUT x^2	b_7 128	b_6 64	b_5 32	b_4 16	b_3 8	b_2 4	b_1 2	b_0 EQUALS a_0 1
x													
0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	1	1	0	0	0	0	0	0	0	1
2	0	0	1	0	4	0	0	0	0	0	1	0	0
3	0	0	1	1	9	0	0	0	0	1	0	0	1
4	0	1	0	0	16	0	0	0	1	0	0	0	0
5	0	1	0	1	25	0	0	0	1	1	0	0	1
6	0	1	1	0	36	0	0	1	0	0	1	0	0
7	0	1	1	1	49	0	0	1	1	0	0	0	1
8	1	0	0	0	64	0	1	0	0	0	0	0	0

Fig. 3. Successive counter states in response to count input pulses.

In conjunction with Fig. 3, it can be seen that the counter of Fig. 3(b) works as follows:

Step 1. A count input is applied.

Step 2. The linear counter, A, counts up by 1. Counter A now contains $x+1$ and counter B contains x^2+1 , since the a_0 bit serves for both a_0 and b_0 (more precisely, the B register contains x^2 if $x+1$ is even and contains x^2+1 if $x+1$ is odd).

Step 3. The "permit add" signal is applied to the AND gates.

If $a_1 = "1"$, b_2 is triggered, thereby adding 4 to the B register.

Likewise, if $a_2 = "1"$, b_3 is triggered, adding 8 to B.

Similarly, if $a_3 = "1"$, b_4 is triggered, adding 16 to B.

Figure 3 shows that a case of particular interest occurs at the seventh count. a_1 is "1", causing b_2 to trigger from "1" to "0". This change causes b_2 to trigger b_3 in a linear fashion; however, b_3 is also triggered by a_3 . Thus b_3 goes from "0" to "1" to "0" on the same count input. In addition, b_3 changing from "1" to "0" generates a carry which causes b_4 to change state. Finally, b_4 generates a carry to trigger b_5 in linear fashion. Thus in this case counter stage b_3 is called upon to trigger twice within one circuit delay. Counters can not be re-triggered in such a short time. This required counter recovery time is the reason the delay modules are used in the system (Fig. 1).

To obtain the sum of squares, stages b_1 and b_0 must be used. But b_1 and b_0 can not be allowed to count while the squaring is being done, because (as seen from Fig. 3) the b_1 bit must always be zero during the squaring operation. Consequently, b_0 is triggered only when the squaring operation is complete. From the diagram of the finished system in Fig. 1 it is seen that this finalizing of the squaring operation is accomplished by the linear reset signal, RL. If a_0 is a "1", the linear reset signal causes b_0 to trigger just before the A counter is reset to "0". The inherent delay in the reset circuit, R_1 , allows the a_0 stage to be interrogated before it is reset.

The b_0 bit then triggers the b_1 bit in a linear manner. Consequently, b_2 is triggered via b_1 only upon application of the linear reset signal, RL, which occurs after the squaring operation is completed. Note that if the RL signal is repeatedly applied after a single count input ($1^2 + 1^2 + 1^2 \dots$), the B register will count up in a linear manner.

C. SYSTEM TIMING

1. Critical Timing Parameters

As previously noted, the counter stages must have sufficient time to recover between trigger pulses. This requirement leads to the use of delay circuits in association with those stages (T_5 , T_6 and T_7 in Fig. 1) which are triggered from two sources. The critical timing occurs during the squaring operation and involves the following circuits and their timing parameters. (Subscript "i" denotes the general circuit.)

a. Counter Circuit

- T_i : triggered response time, or logic delay time. (Time increment from when T_{i-1} goes from "1" to "0" until T_i changes logic level.)
- R_i : Recovery time of counter circuit (minimum time between successive trigger pulses).

b. Delay Circuit

- D_i : Time delay of delay circuit.

c. Gate Circuit

This circuit has no logic delay. That is, the response time of T_6 is the same whether it is triggered from T_5 or the output of D_3 . This fact will be apparent when the circuit operation is discussed in a later section. However, the gate does require recovery time:

- G_{Ri} : For gate 2 ($i=2$) the delay between the time T_3 changes state and the time the count pulse can arrive at the output of D_3 . (This time is quite significant when T_3 goes from "0" to "1".)

2. Derivation of Equations

Now the time delays of the delay circuits will be determined. Consideration of the logic diagram in Fig. 1 shows the critical timing relationships of the system to be:

- | | |
|--|---|
| (4) $D_1 > T_1 + T_2 + G_{R1}$ | G_1 is ready to receive the count pulse after T_2 changes state. |
| (5) $D_1 + D_3 > T_1 + T_2 + T_3 + G_{R2}$ | G_2 is ready to receive the count pulse after T_3 changes state. |
| (6) $D_1 + D_3 + D_5 > T_1 + T_2 + T_3 + T_4 + G_{R3}$ | G_3 is ready to receive the count pulse after T_4 changes state. |
| (7) $D_1 + D_3 > D_1 + T_5 + R_6$ | T_6 is triggered via T_2 and T_5 ; then, after T_6 recovers, T_3 triggers T_6 . |
| (8) $D_1 + D_3 + D_5 > D_1 + T_5 + T_6 + R_7$ | T_7 is triggered via T_2 , T_5 and T_6 ; then, after T_7 recovers, T_4 triggers T_7 . |
| (9) $D_3 > T_5 + R_6$ | T_6 recovers from being triggered by T_5 via T_2 before being triggered by T_3 . |
| (10) $D_5 > T_6 + R_7$ | T_7 recovers from being triggered by T_6 via T_3 before being triggered by T_4 . |

Now the above relationships will be reduced to determine the limiting values of the delays. All T_i 's are equal, all G_{Ri} 's are equal, and all R_i 's are equal.

Inserting Eq. (4) into Eq. (5) yields

$$D_3 > T_3 \quad (11)$$

which is superseded by Eq. (9).

Inserting Eq. (5) into Eq. (6) yields

$$D_5 > T_4 \quad (12)$$

which is superseded by Eq. (10).

Simply canceling D_1 from each side of Eq. (7) yields

$$D_3 > T_5 + R_6 \quad (13)$$

which is identical to Eq. (9).

Consequently, it is necessary to enforce relations (4), (9) and (10). These relations can be changed to equalities by using tolerances, or limiting values.

$$D_{1min} = 2 T_{imax} + G_{Rmax} \quad (14)$$

$$D_{3min} = T_{imax} + R_{max} \quad (15)$$

$$D_{5min} = T_{imax} + R_{max} \quad (16)$$

Now the limitations on the count input repetition rate will be considered. Since the count inputs can occur at random, it is really the minimum time between successive count inputs, τ_{min} , that is of interest.

$$\tau_{min} = D_{1max} - 2T_{imin} \quad (17)$$

$$\tau_{min} = D_{1max} + D_{3max} - 3T_{imin} \quad (18)$$

$$\tau_{min} = D_{1max} + D_{3max} + D_{5max} - 4T_{imin} \quad (19)$$

Equations (17) to (19) require the (n)th count pulse to trigger the appropriate gate before the (n+1)th count pulse changes the respective gate input. For example, the output of T_4 should not be changed by the next count input until the present count input has had the opportunity to trigger T_7 by way of D_5 .

There are three more equations which prevent stages T_6 and T_7 from being triggered by the (n+1)st pulse before they have recovered from being triggered by the (n)th pulse. These equations are:

$$\tau_{\min} = D_{1\max} + D_{3\max} + R_{\max} - D_{1\min} - T_{1\min} \quad (20)$$

$$\tau_{\min} = D_{1\max} + D_{3\max} + D_{5\max} + R_{\max} - D_{1\min} - D_{3\min} - T_{1\min} \quad (21)$$

$$\tau_{\min} = D_{1\max} + D_{3\max} + D_{5\max} + R_{\max} - D_{1\min} - 2 T_{1\min} \quad (22)$$

Equation (22) prevents T_7 from being triggered by the (n+1)st pulse via D_1 , T_5 and T_6 before it has recovered from being triggered by the (n)th pulse via D_1 , D_3 and D_5 .

There is a seeming paradox in Eqs. (20) and (21) in that delays are allowed to be maximum and minimum in the same equation. This phenomenon can occur because the delay circuits are active and depend on the amplitude and width of the input pulse; consequently, it is necessary to allow for the worst case difference in shape between pulses (n) and (n+1).

Now Eqs. (17) through (22) will be examined to determine $\tau_{\min}$, the absolute minimum time between successive count inputs. (The maximum value of $\tau_{\min}$) Eq. (17) is redundant with respect to Eq. (18) if

$$D_{1\max} + D_{3\max} - 3T_{1\min} > D_{1\max} - 2T_{1\min}$$

Reducing this expression yields

$$D_{3\max} > T_{1\min} \quad (23)$$

Relation (23) is shown to be true by the condition established in Eq. (11). Consequently, Eq. (17) is redundant.

Equation (18) is redundant with respect to Eq. (19) if

$$D_{5\max} > T_{i\min} \quad (24)$$

This relation is true by Eq. (12). Consequently, Eqs. (17) and (18) are redundant with respect to Eq. (19).

Equation (20) is redundant with respect to Eq. (21) if

$$D_{5\max} > D_{3\min} \quad (25)$$

This relationship is true, since from Eqs. (15) and (16), D_5 and D_3 are nominally equal. Equation (21) is redundant with respect to Eq. (22) if

$$D_{3\min} > T_{i\min} \quad (26)$$

As before, this relation is true by Eq. (5).

Thus, either Eq. (19) or Eq. (22) determines the minimum allowable value of $\tau_{\min}$, and Eqs. (17), (18), (20) and (21) are redundant. Equation (19) is redundant with respect to Eq. (22) if

$$R_{\max} + 2T_{\min} > D_{1\min} \quad (27)$$

Substituting Eq. (14) into relation (27) yields

$$R_{\max} > 2(T_{i\max} - T_{i\min}) + G_{R\max} \quad (28)$$

If the inequality in relation 28 is correct, Eq. (22) determines $\tau_{\min}$; and if the inequality is incorrect, Eq. (19) determines $\tau_{\min}$.

With the above analysis, the delay circuit propagation times can be determined. From a preliminary circuit breadboard of the Chow counter circuit, the following timing parameters were selected:

$$T_i = 10 \text{ ns} \pm 5 \text{ ns}$$

$$R_{\max} = 65 \text{ ns}$$

$$G_{R\max} = 50 \text{ ns}$$

$$\text{Delay circuit variation} = \pm 10 \text{ ns}$$

Inserting these parameters into Eqs. (14), (15) and (16) yields

$$D_{1\min} = (2 \times 15) + 50 = 80 \text{ ns}$$

$$D_{3\min} = 15 + 65 = 80 \text{ ns}$$

$$D_{5\min} = 15 + 65 = 80 \text{ ns}$$

Since the variation in the delay is $\pm 10 \text{ ns}$, all the delay circuits have a nominal propagation delay of 90 ns.

The minimum time between input pulses is determined from Eqs. (19) and (22).

From Eq. (19)

$$\tau_{\min} = (3 \times 100) - (4 \times 5) = 280 \text{ ns}$$

From Eq. (22)

$$\tau_{\min} = (3 \times 100) + 65 - 80 - (2 \times 5) = 275 \text{ ns}$$

The largest value of $\tau_{\min}$ is most restrictive; thus, with a minimum allowable interval between input pulses of 280 ns, the maximum worst case repetition rate is 3.57 MHz.

Inserting nominal timing parameters into Eqs. (18) and (19) yields a minimum allowable input pulse interval of 230 ns, which corresponds to a maximum nominal repetition rate of 4.35 MHz.

Section III

CIRCUITS

Operation of the system circuits will now be discussed. The fiducial state of the system was chosen to be 0 volts to concur with the switching action of the counter stage. In a binary counter a carry occurs when the output of the counter changes from logical "1" to "0". The Chow type counter triggers on a positive going signal. Consequently, the high voltage levels, 0.4 V for the tunnel diode signals and 4 V for the input-output signals, are designated logical "0"; and the low voltage levels, essentially 0 volts for both the tunnel diode signals and the input-output signals, are designated logical "1".

Before discussing the details of each circuit, a brief exposition on the circuit interrelationships is in order. The circuit schematic of the block of logic D_3 , G_2 and T_6 (Fig. 1) is typical; this schematic is shown in Fig. 4. The delay circuit ensures that the linear counter stage (T_3) has settled down and the gate circuit (G_2) has recovered before the count input, via D_1 , appears at the gate circuit. In a like manner the delay circuit ensures that T_6 is recovered from being triggered by T_5 before it can be triggered by way of G_2 .

From Fig. 4 it can be shown that the logic circuit, G_2 , has no propagation delay with respect to the squaring counter stage, T_6 . With the output of T_3 at 0.4 V (logical "0"), all the current flows through Q_1 and the input from D_3 has no effect. Consequently, a logical "0" at T_3 inhibits the action of gate G_2 and prevents T_6 from being triggered via D_3 . On the other hand, if the T_3 output is at 0 volts, a positive voltage pulse will cause Q_2 to saturate, thereby producing a sharp negative pulse at the collector. It can be seen that the collectors of Q_2 (in the gate) and Q_3 (in the counter stage) are connected to form the wired OR function. Thus

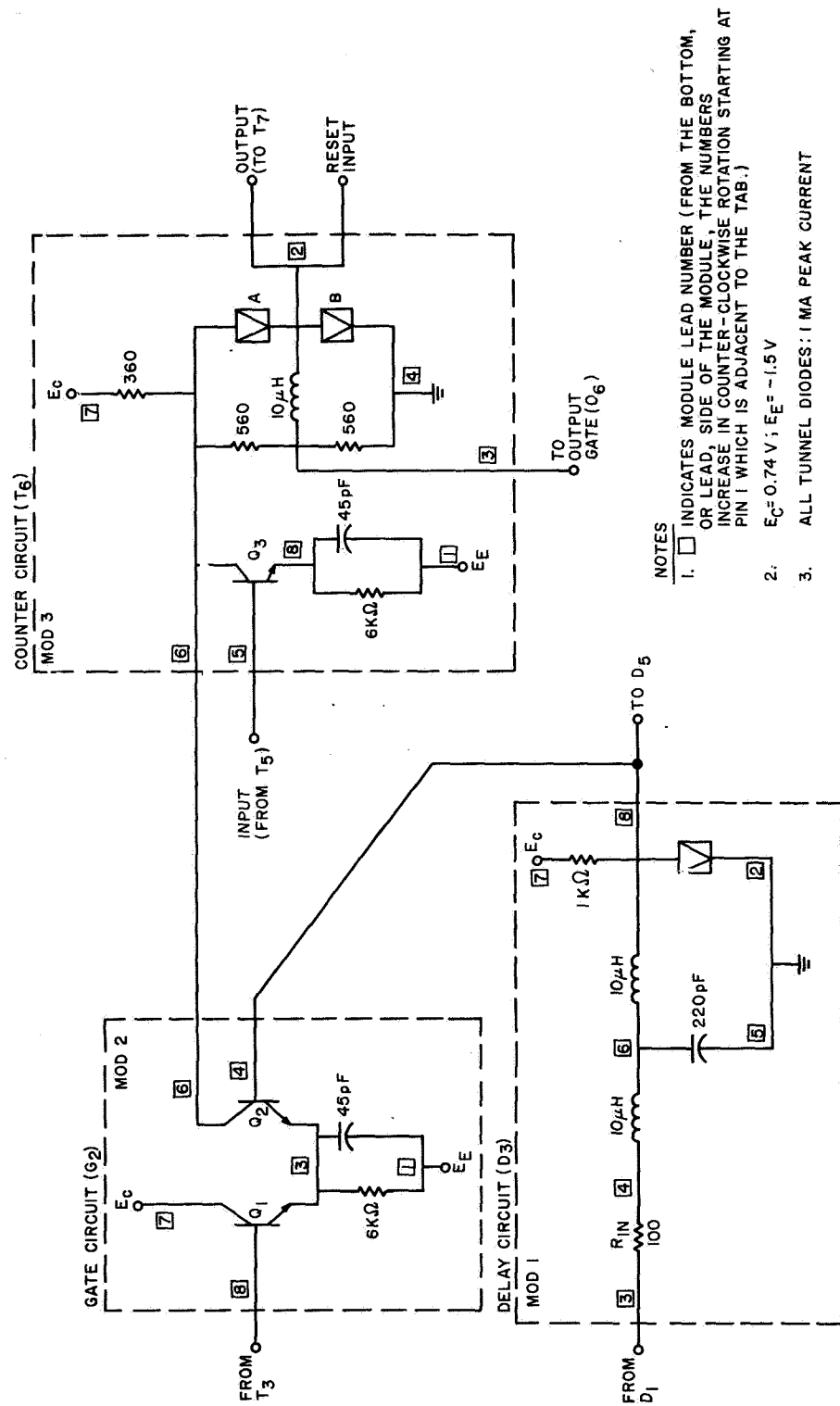


Fig. 4. Schematic of circuits as typically interconnected in the system shown in Fig. 1.

with T_3 in the low voltage state, the counter stage T_6 can be triggered via the gate in the same amount of time as it is triggered by the input from T_5 .

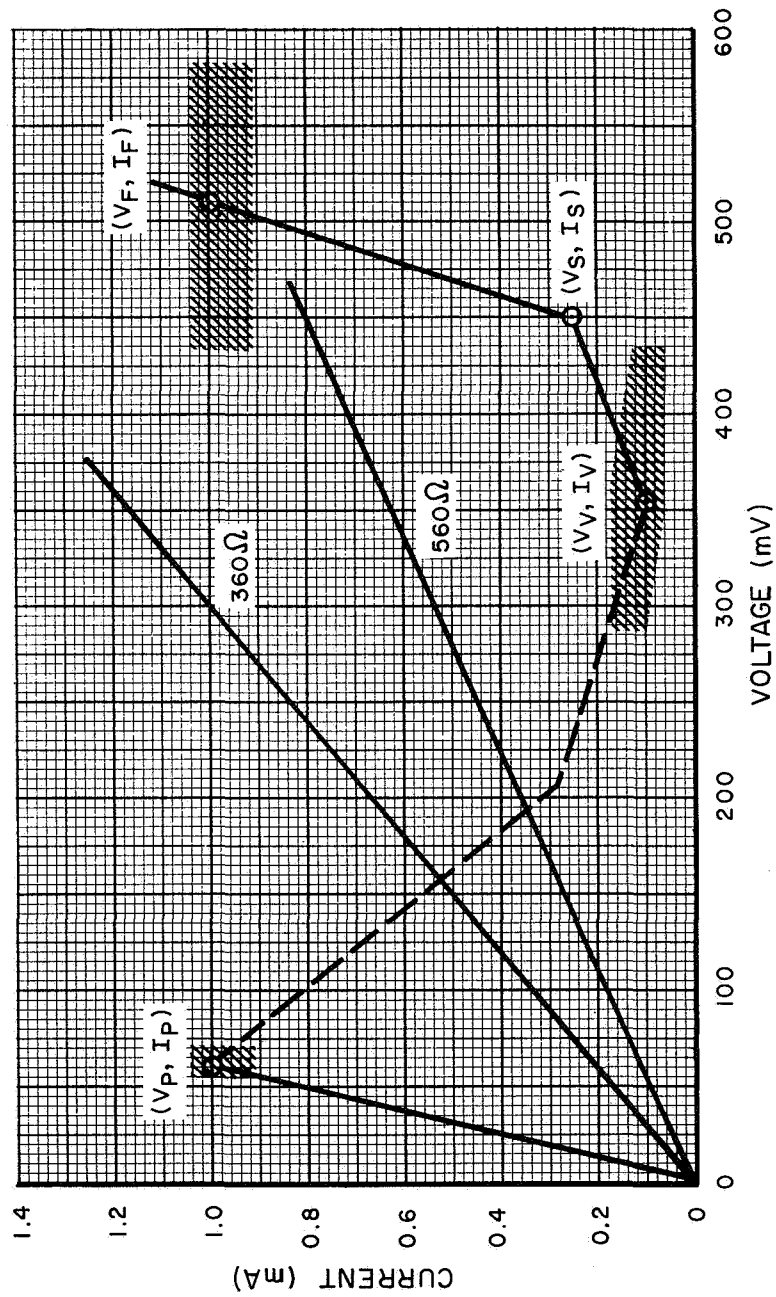
The transistors in the gate circuit must be matched to ensure proper operation with the relatively small tunnel diode logic levels. Matching the base-emitter voltages for emitter currents of 0.2 mA to within 100 mV is adequate. However, to guarantee proper operation in the event that the characteristics age and vary differently with temperature, a variation of only 20 mV at room temperature was allowed.

A. COUNTER CIRCUIT

The counter circuit is the basic Chow counter¹ with the modification in the coupling as introduced by Bush.² An additional circuit modification was added by RCA. The output gate is driven from pin 3 rather than the conventional circuit output of pin 2. Then during switching, the capacitive loading of the output gate is decoupled from the tunnel diodes by the inductor. Consequently, the tunnel diodes switch faster, and higher counting rates can be achieved.

The tunnel diodes are 1N3713's, which have a 1 mA peak current (± 2.5 percent) and less than 5 pF of junction capacitance. A linearized version of the tunnel diode characteristic, with tolerances indicated, is shown in Fig. 5. The transistor in the coupling stage is a 2N709.

The static operating points of the Chow circuit are shown graphically in Fig. 6. The characteristic passing through point (0, 0) is that of tunnel diode B (Fig. 4) in parallel with the adjacent 560-ohm resistor. The characteristic passing through the point (660, 0) is the parallel combination of tunnel diode A and its 560-ohm resistor in series with the parallel combination of the 360-ohm resistor to the 0.74 volt source and the transistor, Q_3 , which is essentially a current source. Note that there are two values of current for Q_3 : 0.1 mA when the transistor base (pin 5) is low (40 mV) and 0.15 mA when it is high (360 mV).



NOTE: A STRAIGHT LINE APPROXIMATION IS USED HERE. THE POINTS TYPICALLY SPECIFIED BY THE MANUFACTURER ARE USED. THE ADDITIONAL POINT IN THE NEGATIVE RESISTANCE REGION WAS OBTAINED FROM THE VALLEY POINTS OF DIODES IN PARALLEL WITH A 560Ω RESISTOR. THE SHADED AREAS INDICATE THE MAXIMUM VARIATION IN THE SPECIFIED POINTS OVER THE TEMPERATURE RANGE $+70$ TO -20°C . (A REALISTIC VOLTAGE TEMPERATURE COEFFICIENT FOR V_F & V_V IS $-0.9\text{ mV}/^\circ\text{C}$). THE RESISTORS USED IN THE CIRCUIT ARE ALSO SHOWN HERE TO FACILITATE GRAPHICAL ANALYSIS.

Fig. 5. Tunnel diode characteristic.

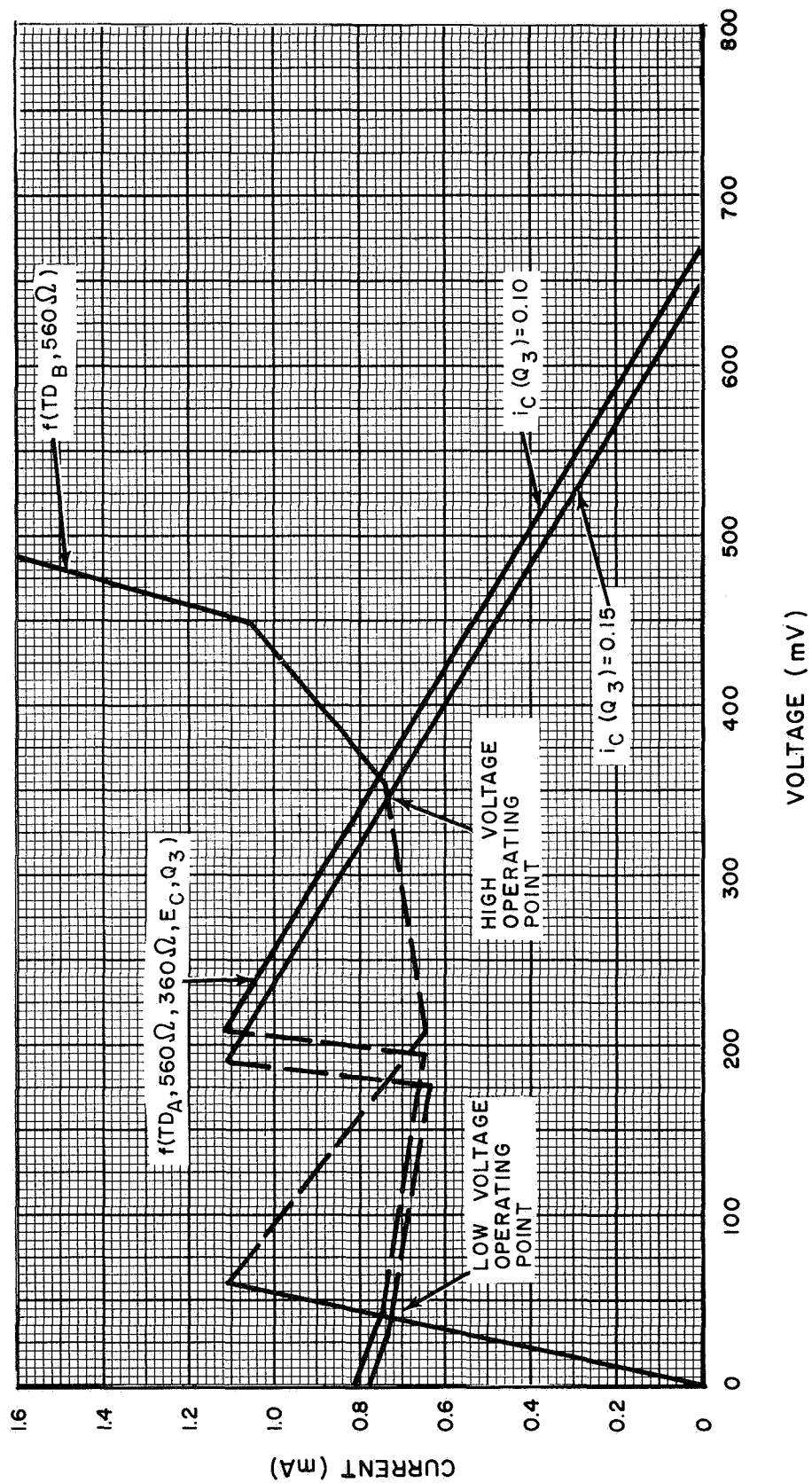


Fig. 6. Graphical representation of counter stage of Fig. 4 in steady state.

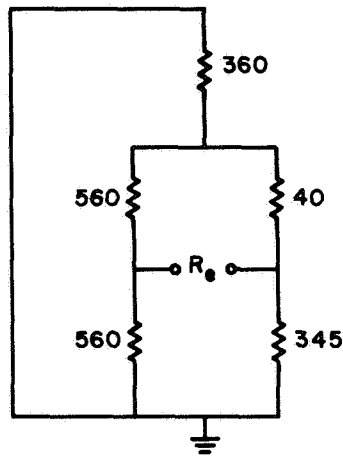
The counting operation of the circuit will now be discussed. Basically, the circuit counts because the current stored in the inductor is in such a direction that the operating point (Fig. 6) switches each time the peaks of the characteristics are crossed. The peaks of the characteristics are made to cross by reducing the combined voltage across the tunnel diodes (point 6 of the counter schematic) to zero. For example, let the output, pin 2, be at 40 mV. As seen from Fig. 5 with the output at 40 mV and a total voltage across the diodes of 360 mV, most of the current flows through the top 560-ohm resistor and tunnel diode B. Consequently, the direction of the current in the inductor is into the junction of the diodes, pin 2. When the voltage at point 6 is shorted to ground (by saturating Q_3), the characteristics of Fig. 6 will intersect near zero. The current in the inductor adds to the characteristic at the right in Fig. 6, making its peak much greater than that of the left characteristic. When the voltage across the diodes is allowed to increase, the characteristics are drawn apart. But the peak of the right characteristic is much higher than that of the left characteristic; consequently, the left characteristic reaches its negative resistance region first and is switched to its high voltage state. In this manner the circuit changes state each time a negative pulse appears at the collector of Q_3 . The pulse need not make the voltage across the diodes equal to zero; it is necessary only that the operating point be reduced to less than the voltage at the peak of the left characteristic of Fig. 6 for a sufficient period of time.

1. Inductive Time Constant

It is critical to the circuit operation that enough current is left in the inductor to switch the circuit to the proper state when the voltage across the diodes is increasing and the peaks of the characteristics cross. Consequently, to ensure proper operation the inductive time constant must be large relative to the width of the trigger pulse at the collector of Q_3 .

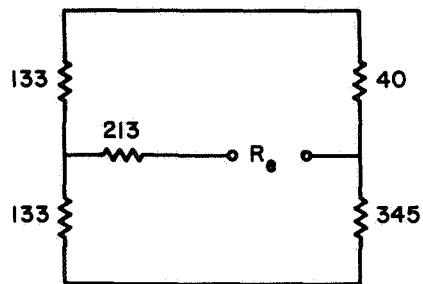
A close approximation to the inductive time constant can be determined by computing the equivalent resistance, R_e , in the circuit of Fig. 7. Here the tunnel diode switching transition time is assumed small with respect to the inductive time constant. This assumption must be true if the circuit is to operate. It has also been assumed that during the transient one tunnel diode will be in its low voltage region and the other tunnel diode will be in its low voltage region half the time and in its high voltage region the other half of the time. Thus a low voltage region resistance of 40 ohms was used for the top diode and the average of the 40 and 650-ohm resistances was used for the lower diode. Based on the schematics in Fig. 7, the equivalent resistance, R_e , is 340 ohms. It should be noted that the assumed resistance value for the switching tunnel diode is not critical in the calculation of R_e . If the low region resistance of 40 ohms was used alone, the equivalent resistance would be 300 ohms; had the high voltage region resistance of 650 ohms been used alone, the equivalent resistance would be 354 ohms. Both of these values are within 10 percent of the 340 ohm value used. Thus with the 10-mH inductor of Fig. 4 the inductive time constant is

$$\tau_L = \frac{L}{R_e} = \frac{10 \times 10^{-6}}{340} = 29.4 \text{ ns} \quad (29)$$



(a)

AS TAKEN FROM FIG. 4.



(b)

AFTER Δ -Y TRANSFORMATION

Fig. 7. Circuit for determining equivalent resistance used in computing inductive time constant.

This value of τ_L is in close agreement with an equivalent value determined from an oscilloscope photo of a breadboard version of the circuit.

It is important that the inductor is given enough time to recover before it is triggered again; thus the inductive time constant is a critical factor in the maximum counter repetition rate. The waveform of the inductor current is plotted in Fig. 8. A repetition period of 60 ns (16.7 MHz) was used in this analysis to ensure that the counter would run at the desired rate of 15 MHz. The steady state current values are ± 0.52 for the computed waveform (determined from Figs. 5 and 6) and ± 0.59 for the experimental waveform. Recall that the reset, or trigger, pulse must be rising and greater than approximately 125 millivolts before the current in the inductor passes through zero, for proper counter operation. Ten percent of the tunnel diode peak current, or 0.1 mA, is a reasonable value to ensure proper switching; therefore, the first trigger pulse should be less than 15 ns for the computed waveform and 19 ns for the experimental waveform, as seen from Fig. 8. However, a second trigger pulse occurring 60 ns after the first must be less than 11 ns for the computed waveform and less than 13 ns for the experimental waveform, if there is to be enough current remaining in the inductor to ensure proper circuit switching. To use a wider pulse width it would be necessary to increase the inductive time constant; however, the maximum repetition rate would then be reduced.

2. Capacitive Time Constant

The other important time factor in the counter circuit is the 45 pF capacitor in the emitter branch of Q_3 . Q_3 , the 6 kilohm resistor and the 45 pF capacitor make up the coupling circuit of the counter.

The input signal to Q_3 comes from another counter stage; consequently, the amplitude of this pulse is on the order of 400 mV. The transistor is always in the on state. When the input is low (0 volt), the collector current is approximately 0.1 mA; and when the input is higher (0.4 volt), the current is 0.15 mA. When a fast

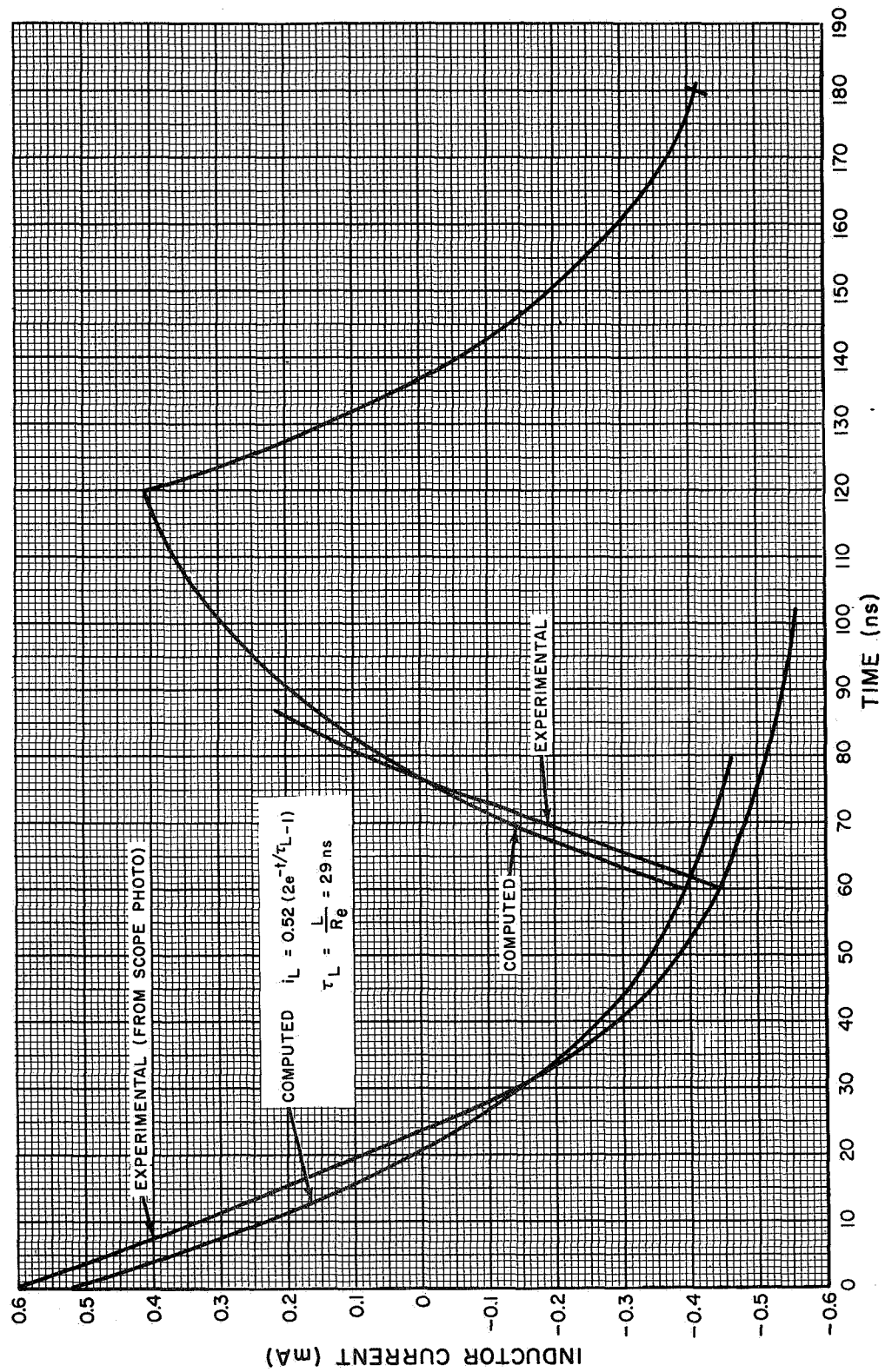


Fig. 8. Experimental and computed waveforms of inductor current showing need for narrow trigger pulse and repetition rate limitations.

rising input pulse is applied to the base of Q_3 , the emitter is retarded from rising by the capacitor; consequently, the transistor goes deep into saturation in order to supply enough charging current to the capacitor. When Q_3 saturates, its collector drops sharply toward the emitter voltage level, thereby supplying the negative pulse to reset the tunnel diodes. Since the transistor is saturated, it can quickly charge the capacitor, and the collector voltage returns to its steady state 400 mV level. This operation of the coupling circuit is indicated in the waveforms of Fig. 9. These waveforms are the collector, emitter and base voltages as taken from a breadboarded Chow counter stage. The output of the counter stage is not shown in Fig. 9 because it follows the collector waveform very closely, thereby causing confusion.

When the input to the counter stage returns to 0 volt the base-emitter diode falls below 0.7 volt; and because the emitter cannot follow, Q_3 cuts off. The emitter falls relatively slowly, its time constant being determined by the 6 kilohm resistor and the 45 pF capacitor. This time constant is

$$\tau_e = RC = 6 \times 10^3 \times 45 \times 10^{-12} = 2.70 \times 10^{-7} \text{ second.} \quad (30)$$

The low steady state value for the emitter is -0.7 volt. However, the emitter falls toward the -1.5 volt supply until the emitter-base diode of the transistor becomes forward biased.

There are two important considerations with regard to the coupling circuit. First, the capacitor must be large enough so that the negative voltage spike in the collector waveform comes close enough to ground to reset the tunnel diodes; and second, when the input goes low, the emitter must fall enough that when the next pulse input occurs the transistor can be resaturated. Both of these requirements can be treated from a charge point of view.

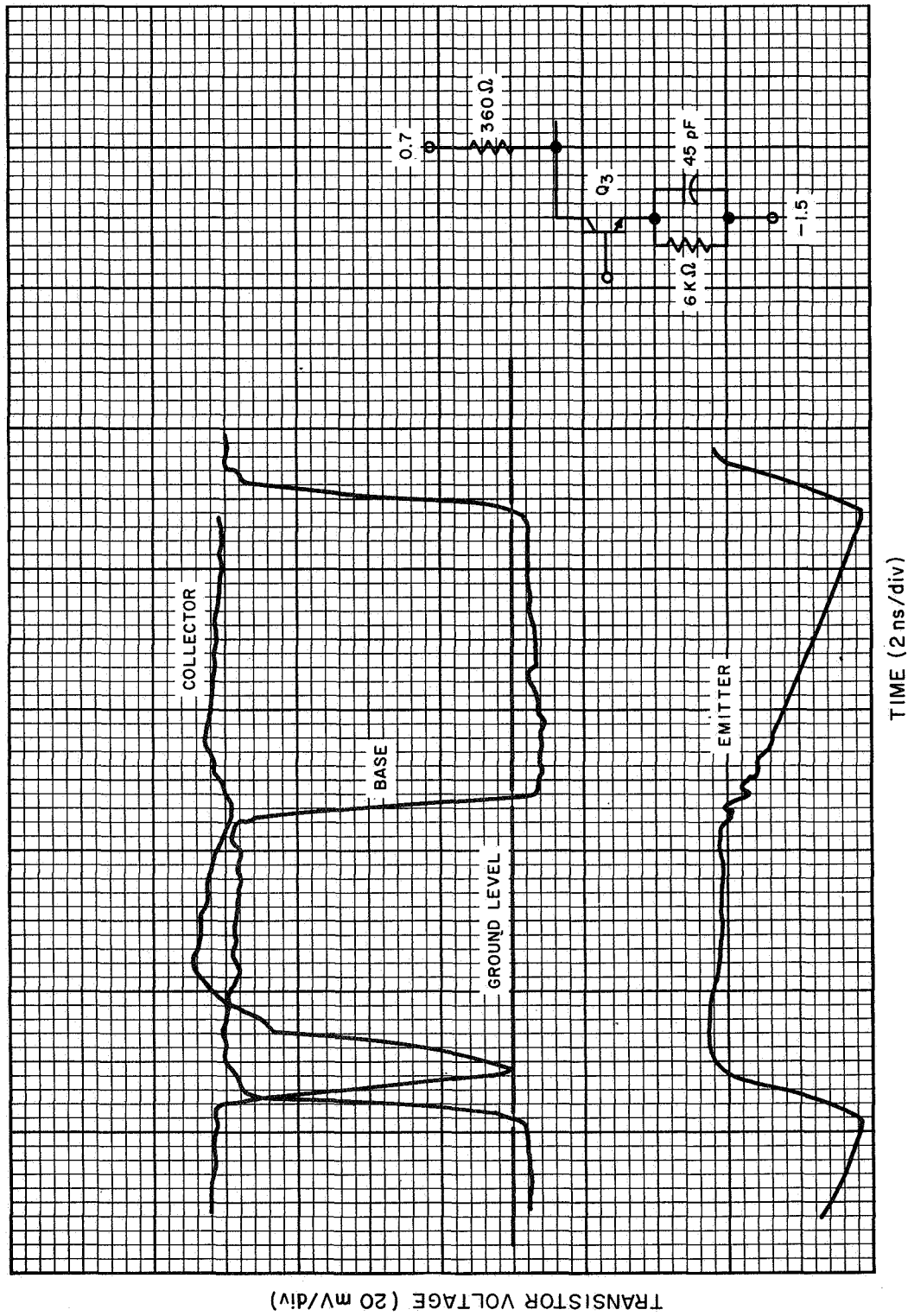


Fig. 9. Waveforms of counter coupling network transistor.

The collector current necessary to bring the collector voltage down to zero is, from Fig. 9.

$$i = \frac{0.400}{360} = 1.1 \text{ mA} \quad (31)$$

The change in capacitor charge needed to get 1.1 mA with the narrow spike required is the area under the collector current waveform. The shape of the waveform is the same as that for the collector voltage indicated in Fig. 9. Consequently the charge is

$$\Delta Q = \frac{i_{\max} \Delta t}{2} \quad (32)$$

where $i_{\max}$ is the maximum current of the collector waveform and Δt the pulse width at its base. Then for a 12 ns, 1.1 mA pulse, the required charge is

$$\Delta Q = \frac{1.1 \times 10^{-3} \times 12 \times 10^{-9}}{2} = 6.6 \text{ picocoulombs} \quad (33)$$

The emitter voltage rise necessary to get this charge is

$$\Delta V = \frac{\Delta Q}{C} = \frac{6.6 \times 10^{-12}}{45 \times 10^{-12}} = 0.147 \text{ volt} \quad (34)$$

Thus when the input goes low, enough time must be allowed for the emitter to fall 147 mV before the next input pulse arrives. This recovery time, as can be seen from the schematic in Fig. 9, is

$$t_r = -RC \ln \left(1 - \frac{\Delta V}{E_E - E_1} \right) \quad (35)$$

where RC is the time constant discussed above, E_E is the supply voltage (-1.5 volts in Fig. 9) and E_1 is the steady state emitter voltage when the input is high (-0.27 volt in Fig. 9). With the values cited, the recovery time is

$$t_r = -6 \times 10^3 \times 45 \times 10^{-12} \ln \left(1 - \frac{(-.147)}{(-1.5) - (-.27)} \right) \quad (36)$$

$$t_r = 34.4 \text{ ns.}$$

From the waveform observed in Fig. 9, 34.4 ns after the input goes low the emitter has fallen 170 mV, which is 23 mV farther than predicted. Consequently, the result is in error by less than 15 percent.

If the maximum required input repetition rate is 15-MHz, the emitter has sufficient time to recover. A 15-MHz repetition rate yields a period between pulses of 67 nanoseconds; thus, if 35 nanoseconds are allowed for the capacitor recovery time, the pulse width at the counter input must be less than 32 ns. Consequently, the repetition rate of the counter stages is limited by the inductive recovery time, which was seen to be on the order of 60 ns.

3. Power Dissipation

The power dissipation in the counter stage can best be analyzed in three parts: the basic counter, the coupling circuit, and the 360-ohm resistor.

The power dissipation in the basic counter can be determined from the graphical representation in Fig. 6. Here it is shown that the total voltage drop across the tunnel diode pair is

$$V_6 = 0.040 + 0.360 = 0.400 \text{ volt} \quad (37)$$

and the steady state current is 0.75 mA. Consequently, the power dissipation in the basic counter is

$$P_{BC} = 0.75 \times 10^{-3} \times 0.400 = 0.300 \text{ mW.}$$

To determine the power dissipation in the coupling stage, the current drain of the 6 kilohm resistor must be found (Fig. 9). While the base of Q_3 swings between 0 and 0.4 volt, the emitter swings between -0.7 and -0.3 volt, for the typical base-emitter drop of 0.7 volt. Consequently, the average emitter voltage is -0.5 volt. Thus the average steady state current in the 6 kilohm resistor is

$$i_{\text{coup}} = \frac{1.5 - 0.5}{6 \times 10^3} = 0.167 \text{ mA}$$

Consequently, the average power dissipated in the coupling circuit is

$$P_{\text{coup}} = (1.5 + 0.4) 0.167 \times 10^{-3} = 0.317 \text{ mW}$$

The power dissipated in the 360-ohm resistor is

$$P_{360} = \frac{(0.7-0.4)^2}{360} = 0.25 \text{ mW}$$

The total nominal power dissipation in the counter stage is*

$$\begin{aligned} P_{\text{total}} &= P_{\text{BC}} + P_{\text{coup}} + P_{360} \\ &= 0.3 + 0.317 + 0.25 \\ &= 0.867 \text{ mW} \end{aligned}$$

B. GATE CIRCUIT

As can be seen from Fig. 4, the gate circuit is identical to the counter input stage, except that its action can be inhibited by the input at the base of transistor Q_1 . Consequently, as with the counter stage, the gate circuit recovery time is given by Eq. 35. With the gate circuit, however, the recovery time applies to either input. Thus, when the input from T_3 goes negative, the capacitive recovery time must be waited before the gate can receive an input via the delay circuit D_3 .

* There is a small additional component of power dissipated in the 360-ohm resistor where a gate circuit is phantom ORed to the counter stage. The average current drained from the counter stage by the gate circuit is

$$i_{\text{GC}} = \left(\frac{1}{2}\right) \left(\frac{1}{2}\right) \frac{(1.5-0.7)}{6 \times 10^3} = 0.033 \text{ mA}$$

Consequently, the power dissipation in the 360-ohm resistor due to the average gate circuit current drain is only $0.033 \times 10^{-3} \times 0.4 = 13.2 \text{ } \mu\text{W}$.

As can be seen from Fig. 4, the current drain of the gate circuit is the same as that of the counter coupling circuit, namely 0.167 mA. Consequently, the power dissipation in the gate circuit is

$$P_{\text{gate}} = 0.167 \times 10^{-3} (1.5 + 0.7) = 0.367 \text{ mW}$$

C. RESET CIRCUIT

The function of the reset circuit is to force the counter stages to the high voltage state (logical "0"). It accomplishes this by supplying 0.5 mA to the tunnel diode junction of the counter (pin 2). The effect of this reset current on the counter is best seen in the graphical representation of Fig. 6. The 0.5 mA reset current adds directly to the right hand characteristic (the one containing TD_A), causing the only operating point to be at about 440 mV. As the reset current diminishes to zero, the operating point slides down the characteristic containing TD_B to the steady state high voltage operating point.

The approximate steady state operating points of the reset circuit are shown in the schematic on Fig. 10. Here the voltage values are determined with the high counter output voltage because this case provides the smallest reset current. Of course, if the counter is in the high voltage state it is already reset. The typical reset current is about 0.8 mA. The typical power dissipation of this circuit is 12 mW with the input pulse at 4 volts, and 0 mW when the input pulse is at 0 volt.

Since the duty cycle of the reset pulse is extremely low, the power dissipation of the reset circuit is negligible. A pulse width of 20 ns is more than adequate for the reset pulse. With a typical count input rate of 4 MHz and an average count of at least 4, the linear reset repetition rate will be 1 MHz. Consequently, the average duty cycle of the linear reset pulse will be no more than 2 percent. Thus the power dissipation of the linear reset gate will be typically less than 0.24 mW. The repetition rate of the system reset pulse will be at least an order of magnitude less, yielding a correspondingly lower power dissipation for the system reset gates.

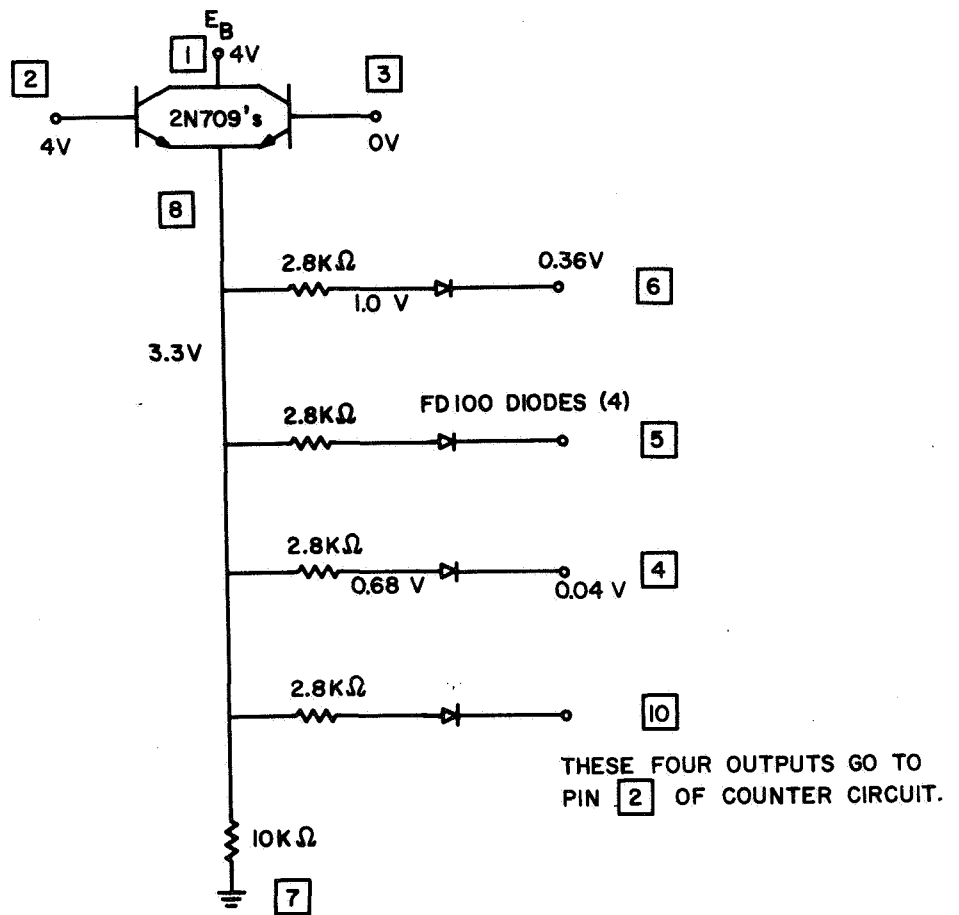


Fig. 10. Reset circuit with typical steady state operating voltages.

Switching waveforms of reset action are shown in Fig. 11. These waveforms were observed during system operation at counter stage T_1 , upon application of the linear reset pulse. The reset delay is less than 4 ns, measured between the 50 percent signal amplitude points; and the entire resetting action takes less than 10 ns. It was also observed that a reset pulse less than 5 ns wide at the base would reset the counter. The counter circuit can be reset less than 10 ns after it has been set.

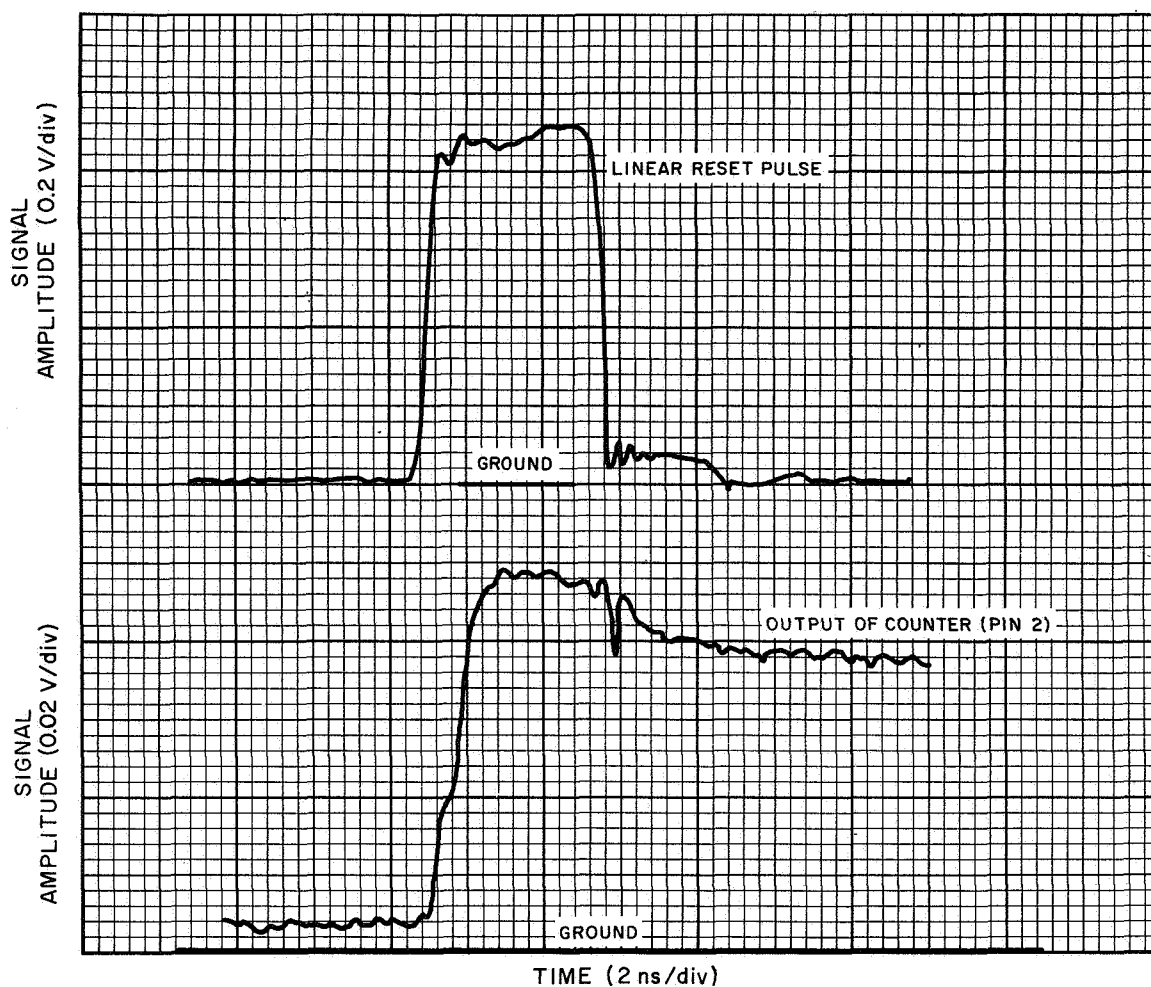


Fig. 11. Resetting counter stage T_1 with a linear reset pulse.

D. OUTPUT CIRCUIT

One of the focal points of this development program was the output circuit. The output circuit must make tunnel diode signal swings compatible with transistor signal swings, while providing the tunnel diode circuits with good isolation from external noise. Most present day medium speed logic circuits (other than Current Mode Logic) have signal swings on the order of 3 to 5 volts. For the present system, voltage levels of 0 and 4 volts were chosen for the output gate. As will be seen, however, the output gate can easily provide other signal swings.

Amplification of the 350 mV tunnel diode swing can best be accomplished by a circuit of the current steering type such as shown in Fig. 12. The circuit must fulfill two requirements: 1) when the input is high (0.35 to 0.4 volt), Q_2 should draw negligible current so that the output voltage, V_O , is approximately equal to E_B ; 2) when the input is low (0 to 0.05 volt), Q_2 must draw enough current such that the output voltage is approximately zero. In order to meet the second requirement while maintaining low power dissipation and relatively loose tolerances, it is necessary that transistors Q_2 and Q_4 operate in the saturated mode under some conditions. It is also necessary that the low voltage output level be negative by a fraction of a volt to ensure that, under all conditions, it is never greater than 0.4 volt (an arbitrary but reasonable limit). In general, however, it is not objectionable

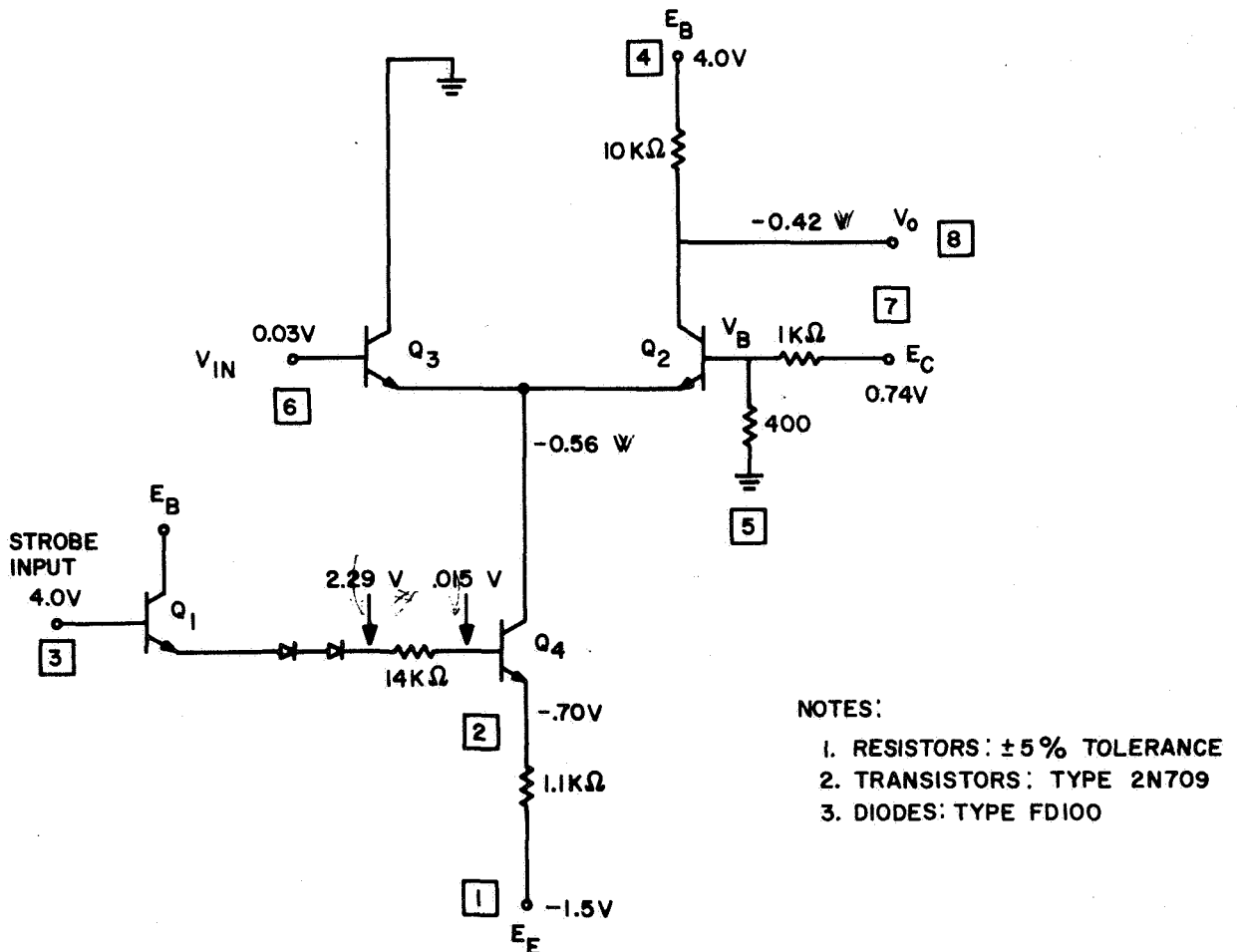


Fig. 12. Output circuit schematic with typical steady state operating voltages for the strobe input high (4 V) and the input voltage low (40 mV).

to allow the low logic level to swing below zero; on the contrary, it has the desirable effect of increasing circuit noise immunity. If it is required that this voltage stay closer to 0 volt, a clamping diode, with anode returned to the E_C supply voltage, can be inserted into the circuit.

In order to minimize power dissipation, the current source is turned off except when the contents of the counter are being read via the output circuit. The circuit is enabled by the strobe input at the base of transistor Q_1 . If the strobe input is at 0 volt (logical "1"), the base emitter junction of Q_4 is reverse biased and there is negligible current flow in the circuit. When the strobe input is high (logical "0"), the 1.1 kilohm current source is turned on, and the logic state of the counter stage attached to the input, V_{in} , can be read at the output, V_o .

Initially 1.5 kilohms instead of 1.1 kilohms were used for the value of the resistor attached to the emitter of Q_4 , in an effort to minimize power. Under worst case conditions, however, the 1.5 kilohm value of resistance allowed the low value of the output voltage to approach 1.5 volts. Unfortunately, the TO-5 circuit modules were assembled with 1.5 kilohm resistors; however, it is an easy matter to parallel these resistors (pins 1 and 2) with 3.9 kilohm resistors to obtain the desired value of 1.1 kilohms. A 3.9 kilohm resistor was added to output gate 08 (Fig. 1) in the system. Table I gives a comparison between the output levels of gates 05 and 08 in the working system for worst case power supply voltages and temperature range. It is seen that there is little difference between worst case high levels, as seen in case 6. However, for the worst case low levels, 05 has the prohibitive value of 1.45 volts while 08 has a value of 0.133 volt (case 8).

TABLE I. VOLTAGE LEVELS OF OUTPUT GATES 05 AND 08 UNDER NOMINAL AND WORST CASE CONDITIONS

CASE NO.	TEMP. (°C)	E_C (volts)	E_E (volts)	E_B (volts)	OUTPUT LEVELS (volts)			
					High		Low	
					05	08	05	08
1	25	0.74	-1.5	4.0	3.77	3.99	-0.123	-0.371
2	25	0.66	-1.35	4.4	4.12	4.36	1.35	-0.044
3	25	0.82	-1.65	3.6	3.42	3.60	-0.371	-0.436
4	70	0.74	-1.5	4.0	3.73	3.89	-0.207	-0.309
5	70	0.66	-1.35	4.4	4.06	4.26	+1.04	-0.194
6	70	0.82	-1.65	3.6	3.37	3.47	-0.299	-0.361
7	-20	0.74	-1.5	4.0	3.79	4.02	-0.179	-0.432
8	-20	0.66	-1.35	4.4	4.15	4.41	+1.45	+0.133
9	-20	0.82	-1.65	3.6	3.38	3.57	-0.462	-0.528

NOTE: The current source resistor of 05 is 1.5 kilohms and that of 08 is 1.1 kilohms.

The transient response of output circuit 05, as it functions in the system, is shown in Fig. 13. Here the strobe input is at its high level and the circuit is on; then the counter stage, T_5 , changes to its high voltage level. The exponential time constant of the circuit (the time for an exponential signal to reach 63 percent of its maximum value) is about 100 ns. The time response to a negative signal is essentially the same. Note in Fig. 13 that the voltage amplification is more than 10 to 1.

Figure 14 shows the output circuit response to a strobe input pulse when the computer is quiescent. It can be seen that the strobe pulse must be at least 100 ns wide to correctly interrogate the counter.

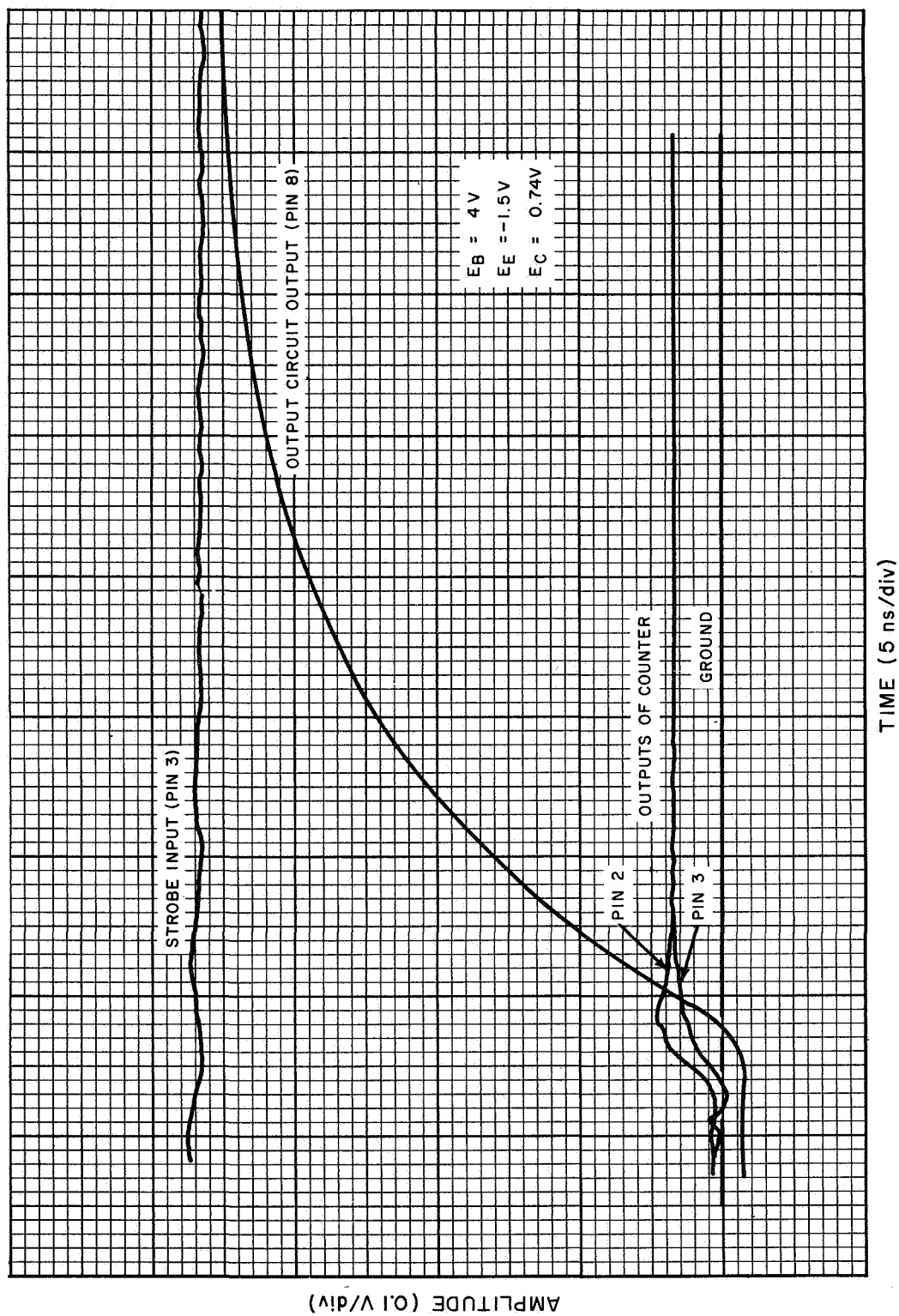


Fig. 13. Response of output circuit (gate 05 in system) to change in counter state.

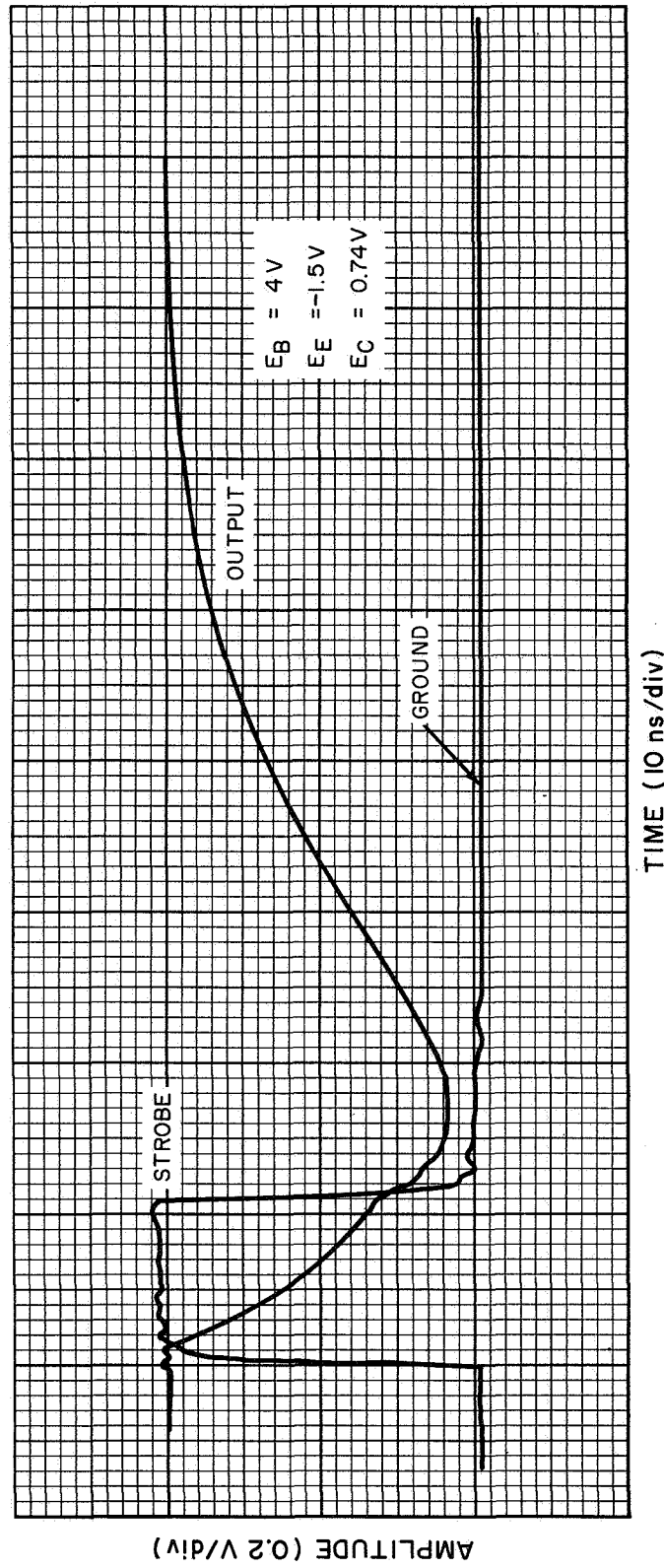


Fig. 14. Output gate response to strobe pulse (counter quiescent).

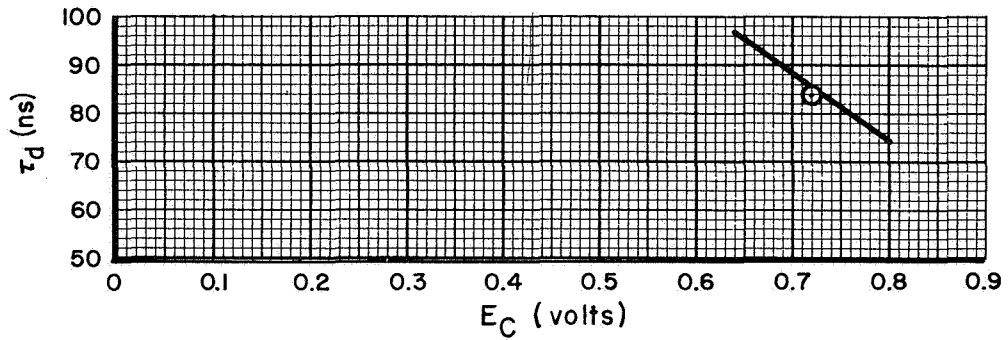
The power dissipation of the output circuit will be negligible since it is active for only short periods of time. From Fig. 12 it can be seen that the maximum power is dissipated when the count input is low, and this power dissipation is less than 4 mW (approximate calculation, based on voltage extremes and current in the 1.1 kilohm resistor).

E. DELAY CIRCUIT

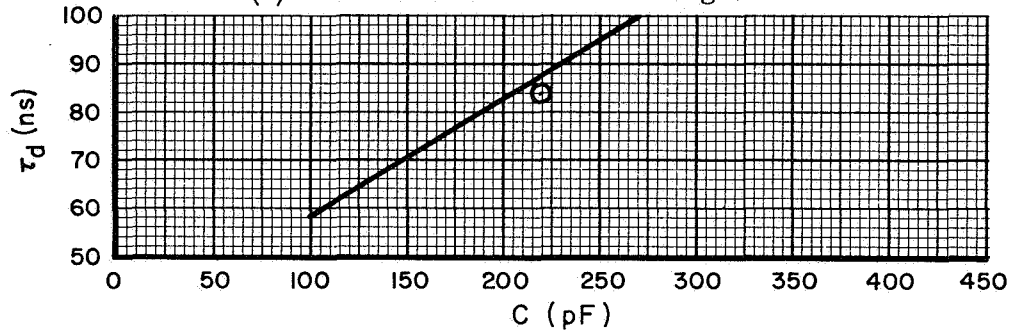
The delay circuit presented the most difficult development problem in the system. A total delay of about 250 ns is required through the delay modules D_1 , D_3 and D_5 in Fig. 1. The risetime of the signal at the output of these delay modules must be fast enough to trigger the counter stage via the gate circuit, as indicated in the schematic of Fig. 4. In addition, the delay must be packaged in a TO-5 type can (0.35 inch diameter by 0.35 inch high). The circuit must also be capable of running at the system repetition rate, which is on the order of 5 megahertz.

The delay circuit of Fig. 4 meets these requirements. Essentially the circuit is composed of a single T-section of a lumped delay line followed by a monostable tunnel diode stage. The purpose of the T-section, composed of two 10 μ H inductors and a 220 pF capacitor, is to provide a slow risetime. The combination of the 1 kilohm resistor and the 0.74 volt supply voltage causes the tunnel diode to be biased in its low voltage region at about 0.7 mA. Thus, when the current out of the T-section is greater than 0.3 mA, the tunnel diode switches to its high stage. Since the circuit is monostable, the output pulse returns to approximately 0 volt. Thus, the delay and slow risetime of the T-section contribute the delay, and the signal risetime is regenerated by the fast switching of the tunnel diode.

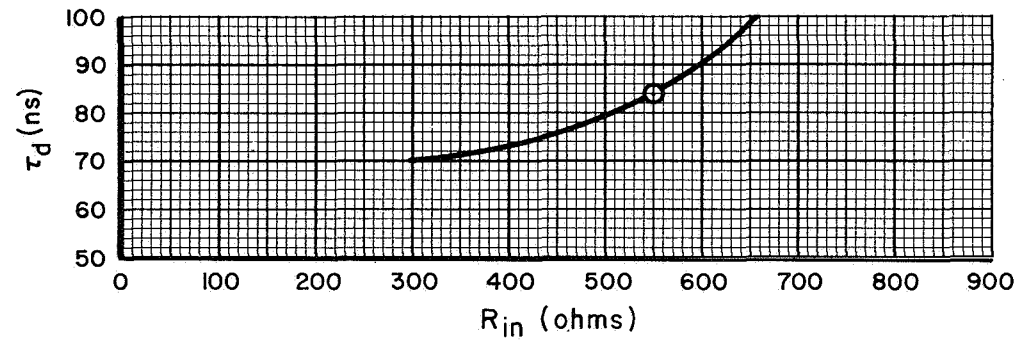
Insight into the sensitivity of the delay time to other circuit parameters, is given in Fig. 15. The parameters considered are bias voltage, E_C ; T-section capacitance; input resistance, R_{in} ; and the driving pulse amplitude and width. Here a single unloaded delay circuit was driven with a 3 ns risetime pulse. The nominal circuit



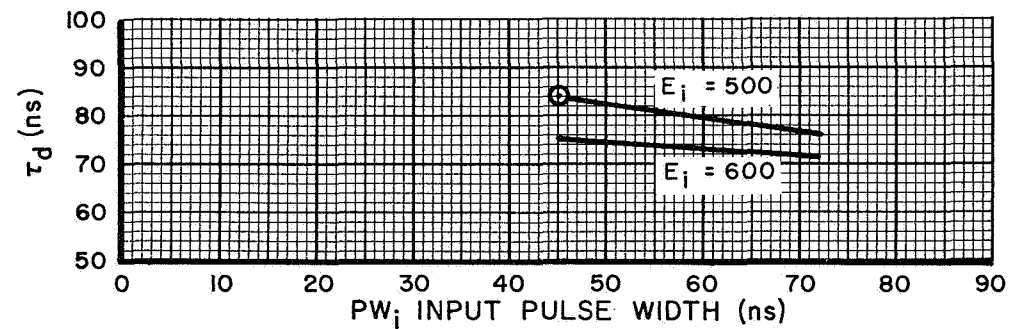
(a) Variation versus bias voltage.



(b) Variation versus T-section capacitance.



(c) Variation versus input resistance.



(d) Variation versus input pulse width and amplitude.

NOTE: Reference run: $R_{in} = 550$ ohms, $E_C = 0.72$, $C = 220$ pF, $PW_i = 47$ ns.

Fig. 15. Variation in delay module propagation time.

parameters were $E_C = 0.72$ volt, $C = 220$ pF and $R_{in} = 550$ ohms. The input pulse was nominally 47 ns wide and 0.5 volt in amplitude. As seen in Fig. 15, these nominal parameters yield a delay of 84 ns. The nominal output amplitude was 450 mV and it changed less than 50 mV for all the variations shown in Fig. 15. The risetime of the delayed pulse was less than 10 ns for all parameter variations.

From Fig. 15(a) it is seen that the delay decreases with increasing bias voltage. This trend is to be expected; as the bias increases, the tunnel diode is biased closer to its peak. Consequently, less input current is required to switch the tunnel diode.

In Fig. 15(b) it is seen that the delay increases as the capacitance of the T-section is increased. Since increased capacitance retards the rise of the input signal, this trend is expected.

An increase in input resistance attenuates the input signal, thereby requiring more time for the input signal to reach the threshold of the current tunnel diode (see Fig. 15(c)).

From Fig. 15(d), an increase in input pulse amplitude allows the threshold of the tunnel diode to be reached sooner, thereby causing a decrease in propagation delay. However, an increase in input pulse width has little effect on delay time.

It is of interest that the delay is a linear function of T-section capacitance. A capacitance of 100 pF yields a delay of 58 ns, while a capacitance of 270 pF yields a delay of 100 ns. On the other hand, the effect on delay of the series resistance is nonlinear; the delay falls off very gradually as the resistance is decreased below 400 ohms. This nonlinearity of delay with R_{in} turned out to be important when the delay modules were operated in the system.

It was found that the system repetition rate was limited by the delay circuits. However, by decreasing R_{in} from 550 ohms to 100 ohms, the recovery time of the delay circuits was vastly improved, thereby making it possible to reach a

repetition rate of 2 MHz in the breadboarded system. This increase in repetition rate was achieved with only a small decrease in circuit delay because of the non-linearity of delay as a function of R_{in} .

Waveforms of the delay circuits operating in the final system are shown in Fig. 16. By making some changes in the circuits of the system, a repetition rate of 4 MHz was achieved. The changes enhanced the repetition rate and maximized the allowable variation in the supply voltage, E_C . The changes, which were made on the circuit board, are 1) short out R_{in} in D_3 , 2) shunt the 220 pF capacitor in D_1 and D_3 with 240 ohms, 3) shunt the output of D_5 with 1.1 kilohms. These modifications improved the recovery time of the delay circuits.

The variation in delays from the nominal case of Fig. 16, were observed for changes in bias voltage, count-input pulse width, and count-input pulse amplitude. These results appear in Table II. The delay times are most sensitive to changes in bias voltage, the relationship being approximately one to one. A 10 percent change in bias voltage causes about a 10 percent change in total delay. The delay is less sensitive to changes in the count-input characteristics. A 40 percent range in pulse amplitude yields a 15 percent range in delay time, while a range of 48 percent in pulse width yields a delay range of only 13 percent. Of course the ranges of variation in delay are changed somewhat when different nominal conditions are selected.

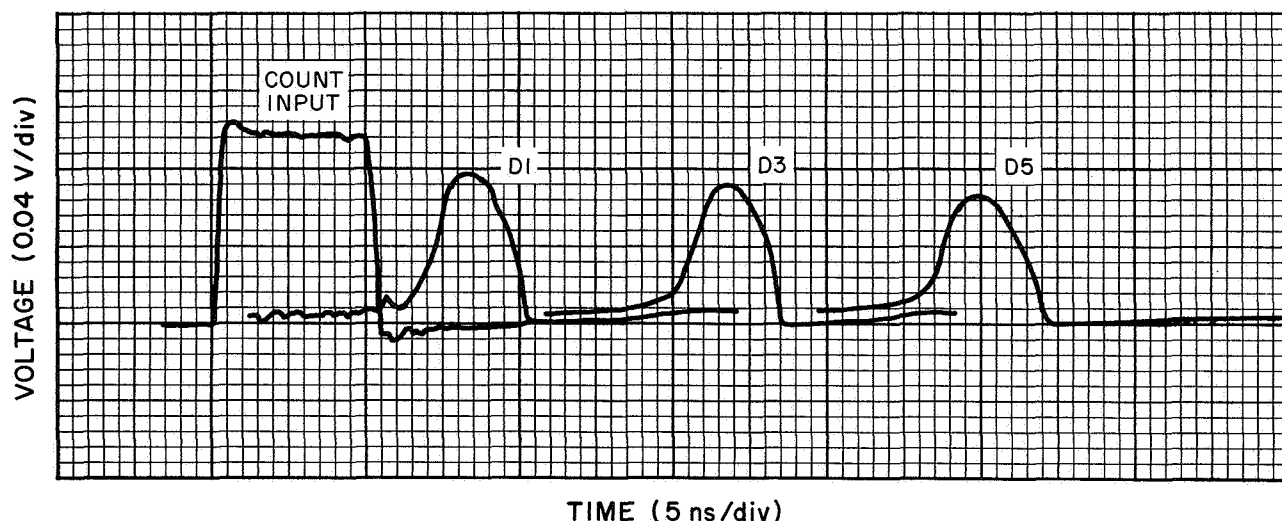


Fig. 16. Waveforms of delay circuits operating in the system shown in Fig. 1.

TABLE II. RANGE OF DELAYS IN SYSTEM AS A FUNCTION OF BIAS VOLTAGE E_C AND COUNT INPUT PULSE WIDTH AND AMPLITUDE

INPUT PULSE		BIAS VOLTAGE E_C (volts)	INDIVIDUAL DELAY TIMES (ns)			TOTAL DELAY (ns)	DEVIATION IN TOTAL DELAY FROM NOMINAL (percent)
Width (ns)	Amplitude (volts)		D_1	D_2	D_3		
50	480	0.74	71	84	82	237	---
50	480	0.67	76	90	98	264	+11.4
50	480	0.85	62	76	70	208	-12.2
50	400	0.74	81	90	88	259	+ 9.7
50	600	0.74	66	78	80	224	- 5.5
38	480	0.74	78	93	88	259	+ 9.7
62	480	0.74	72	78	80	230	- 3.0

NOTE: Time measurements made at 200 mV level.

For all the variations expressed in Table II the voltage amplitudes of the delay modules varied less than 40 mV, except for the count-input pulse width of 38 ns, where the amplitude of D_5 decreased 70 mV. The amplitude of D_5 can be increased by increasing the externally inserted load resistor from its present value of 1.1 kilohms. The risetimes of the delay pulses changed very little for the variations of Table II.

Section IV

PACKAGING

A. CIRCUIT MODULES

All circuits in the system are packaged on TO-5 headers, which are 0.35 inch in diameter. Photographs of the counter stage are shown in several stages of development in Fig. 17. At the left, from bottom to top, are the inductor, a wafer containing the two tunnel diodes, and another wafer containing the transistor, resistors and capacitor. In the middle is the TO-5 header and its cover. Note that the leads stick up through the header; these projecting leads are used to interconnect and hold the wafers in place. The rest of the circuit modules are packaged in the same manner.

The delay module also has two wafers, one for the tunnel diode and one for the resistors and capacitor. However, this module has two coils, making it the most densely packaged module. The logic gate utilizes a single wafer. The reset circuits and the output circuits require two wafers each to house their components.

All modules except the reset gate have eight leads. The reset gate required nine leads to interconnect the two wafers; consequently, a 10 lead TO-5 header was used.

Because of the inductor size, the counter and delay modules were packaged in 0.35 inch high cans, while the other three module types utilize a 0.25 inch high can.

In addition to the modules fabricated in TO-5 cans for use in the system, two working units of the counter circuit were built in a flat package. This flatpack, which is a 0.4 inch square by 0.1 inch thick, is shown with the breadboarded counter module in Fig. 18.

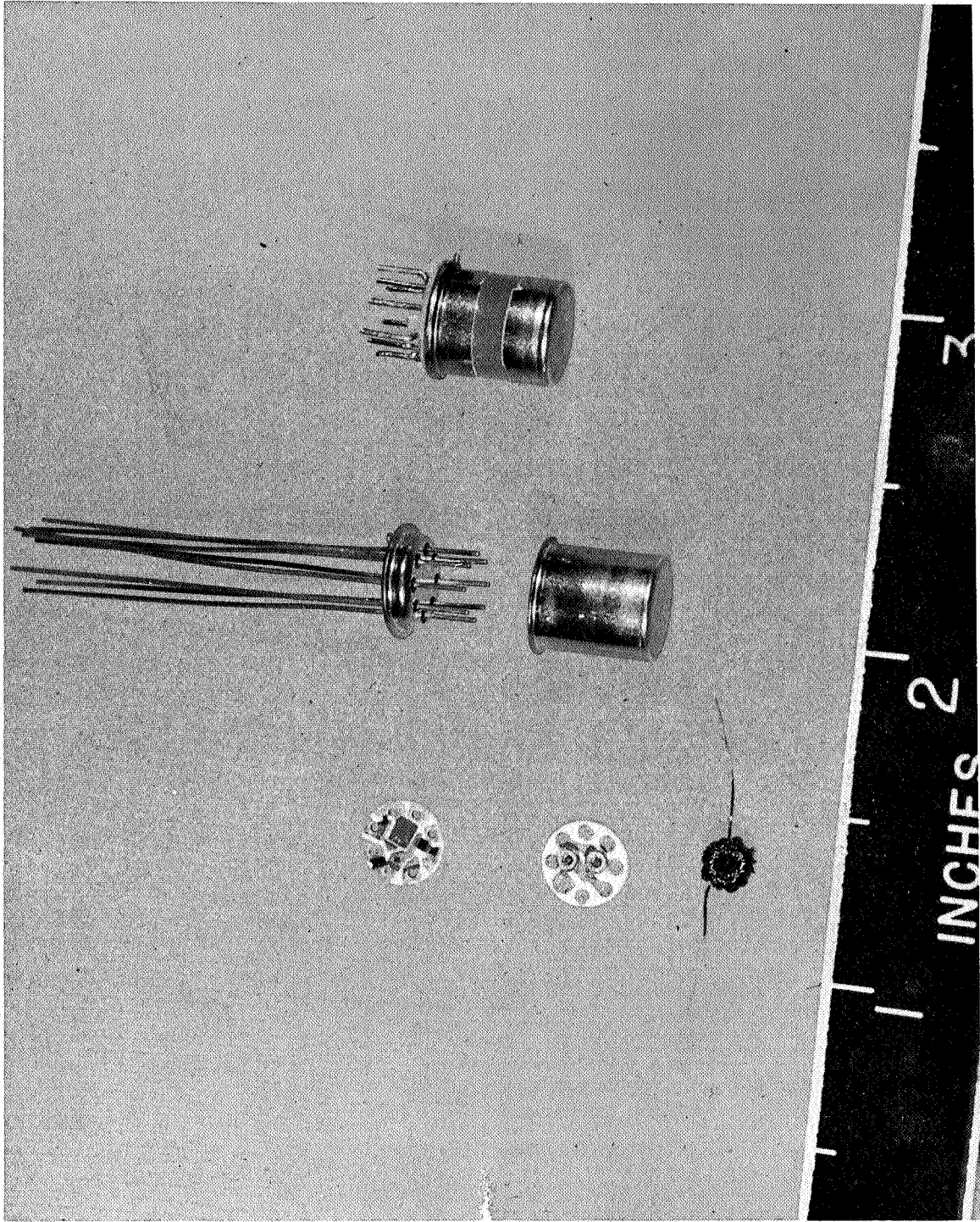


Fig. 17. Counter module construction

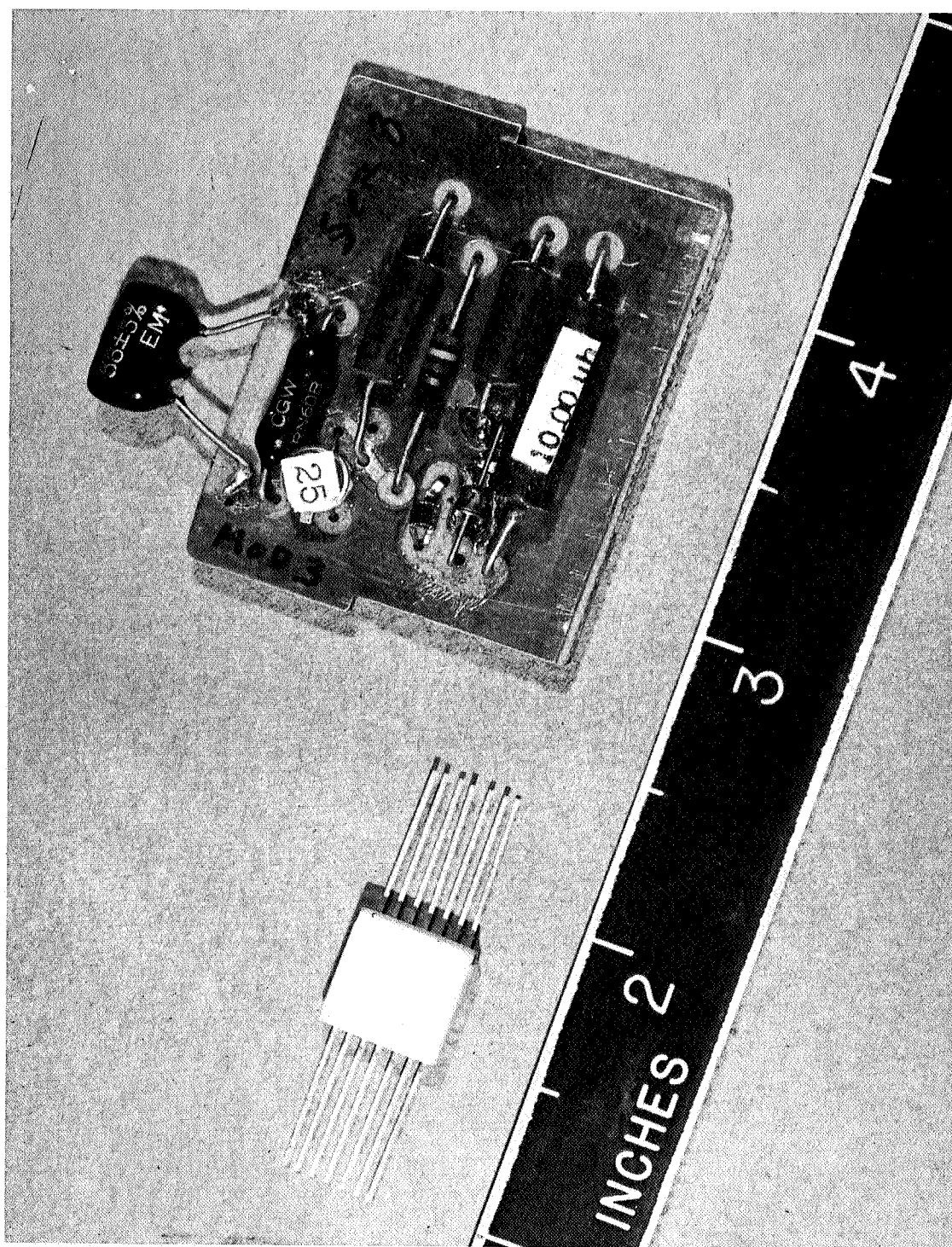


Fig. 18. Breadboarded counter stage and flatpack version.

B. MULTILAYER BOARDS

Printed circuit boards are used to interconnect the circuit modules. These boards have seven layers: the two surface layers are used for signal interconnections, the next two layers are ground planes, and the middle three layers are power supply buses. The signal lines are 0.0014 inch thick while the five internal layers are 0.0028 inch thick.

The fiberglass-epoxy dielectric material is 0.004 inch thick in the internal layers. These layers are made thin to form a distributed capacitor which aids in the dynamic regulation of the power supply voltages. On the other hand, the signal lines are separated from their respective ground planes by 0.0021 inch thick fiberglass-epoxy, in order to minimize the capacitance of the signal interconnections.

The signal lines are 0.010 inch wide, which, with the fiberglass-epoxy dielectric constant of 5, leads to a capacitance of about 1.7 pF/inch. Signal and power supply connections are brought to both board surfaces by plating the holes used for the module leads.

The overall board thickness is limited by the ability to make reliable plated through holes. The ratio of board thickness to hole diameter is about four to one, within the present state of the art.

C. SYSTEM ASSEMBLY

The assembled system is shown in Fig. 19. The module leads are inserted through the board and soldered in place. Lead breakout of the modules is modified to a square pattern to allow room on the board for the shoulders of the plated through holes and to enable the printed wiring to pass between the pins. This modification is accomplished by a plastic standoff which can be seen on the modules in Fig. 19. In addition, the standoff prevents the signal lines from shorting to the module case and keeps moisture from being trapped between the board and the module.

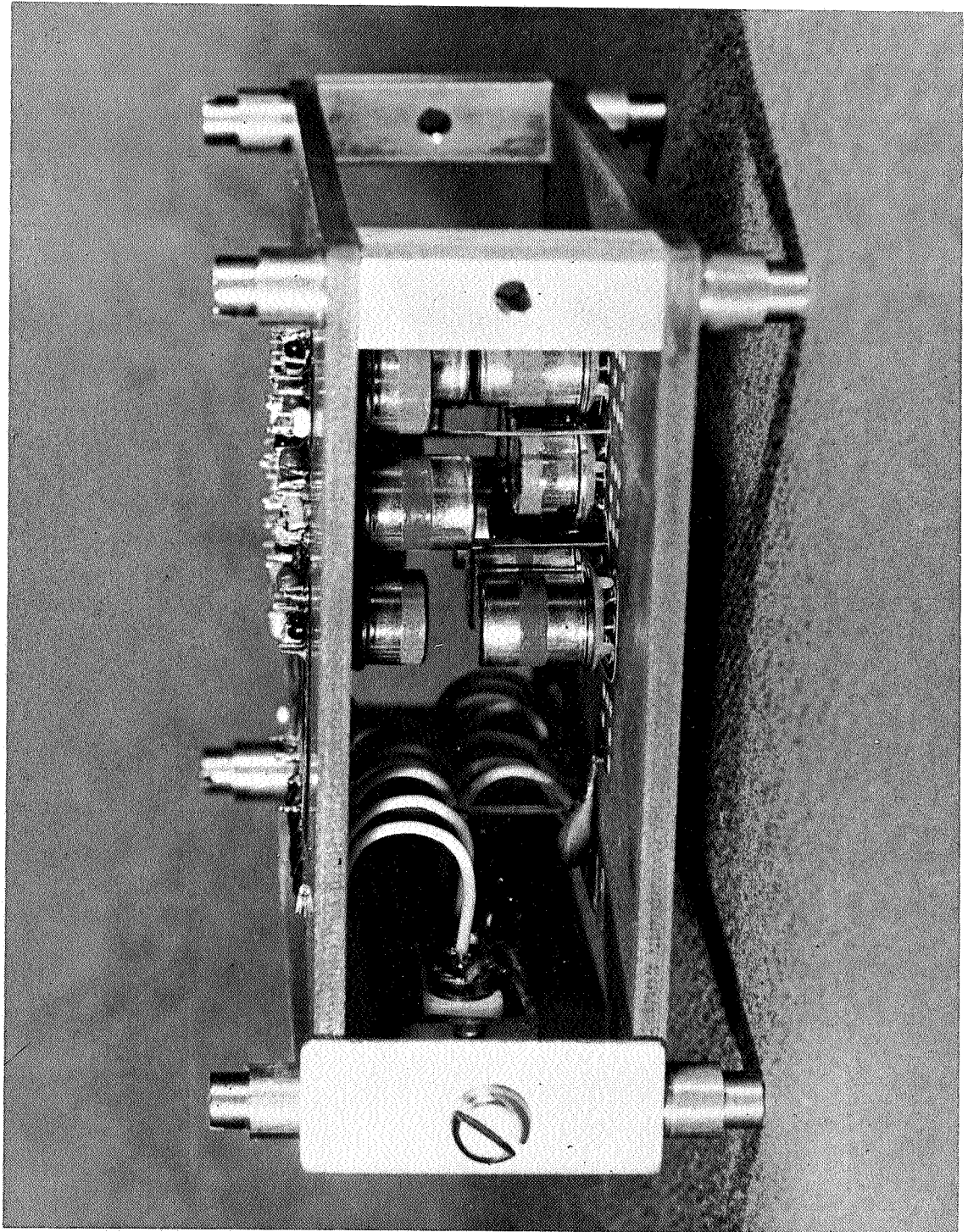


Fig. 19. Assembled squaring counter system.

Modules are placed so as to keep interconnection lengths short in order to minimize crosstalk and line capacitance. The wiring diagram of the system is shown in Figs. 20 through 23. Partitioning the logic modules between the two boards was made in a manner that minimizes the number of connections between boards. From the logic diagram of Fig. 1, it is seen that a natural place to divide the system is at the output of the gate circuits. By dividing the system at this point, 13 modules go on the top board, 14 modules go on the bottom board and there are only four connections between the boards. Connections between the boards are made by direct wires as can be seen in Fig. 19. These intra-board connection lengths are minimized by placing the gate modules within one module position over their respective counter stages. Placing the modules in this manner not only keeps the interconnections short, but also minimizes wiring crossovers on the boards.

In order to reduce the effects of crosstalk, lines carrying the 400 mV tunnel diode signals are placed on the module side of the boards and the 4 volt input-output signals are placed on the outside of the boards. Since the smaller signal levels are placed on the inside of the board, they are shielded from external noise by the ground planes inside the boards.

Although the count input signal need only be on the order of 0.5 volt, a 4 volt signal was used. The 4 volt signal is then attenuated by a voltage divider, as can be seen in Fig. 20(a). This high-level count input was used so that all input signals to the system would be 4 volts, thereby preventing damage to the first counter stage or delay circuit by mixing up the input cables.

The connector used to join the squaring counter with the outside world was purchased from the I. T. T. Cannon Electric Co. (their part number DCM17W5). This connector has 12 conventional pin type terminals and 5 coaxial type terminals. The bias voltages and system outputs utilize the conventional pins, while the system reset, linear reset, strobe and count-input signals utilize the coaxial terminals. The remaining coaxial fitting is used by the highest order output gate, 08, thereby enabling the system to be dynamically checked in a noise environment.

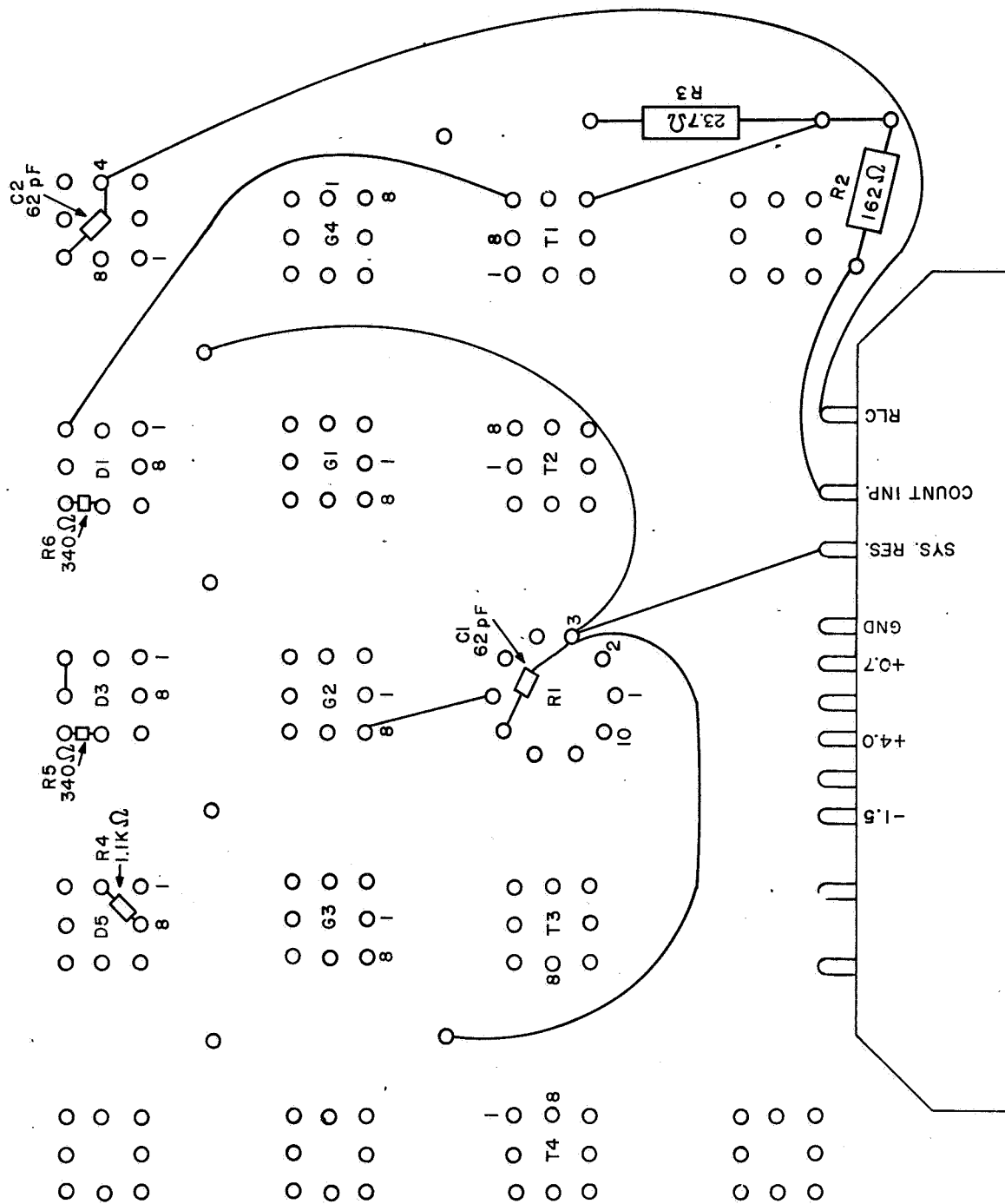


Fig. 20. System wiring diagram, top of upper board, outer side.

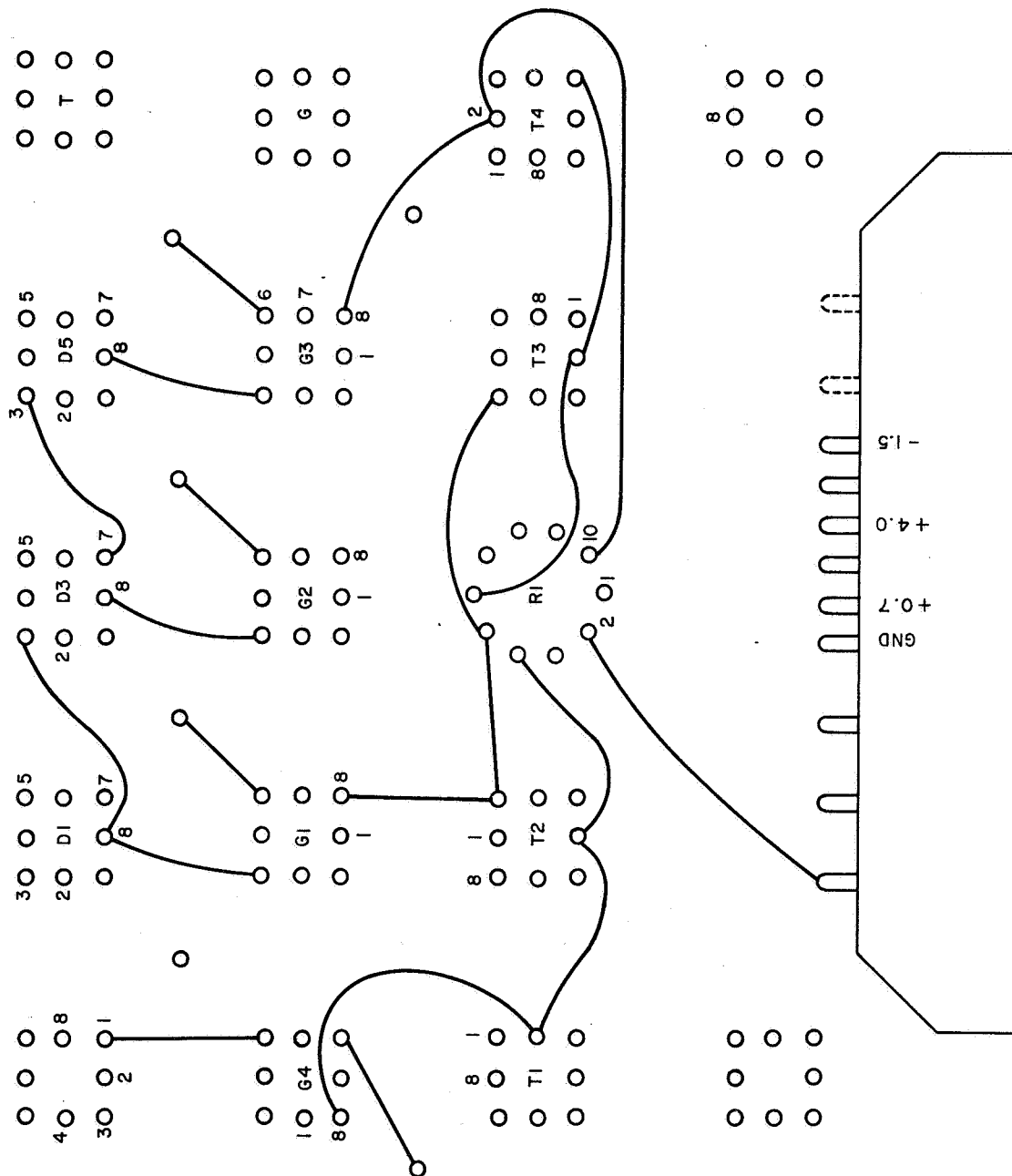


Fig. 21. System wiring diagram, bottom of upper board, module side.

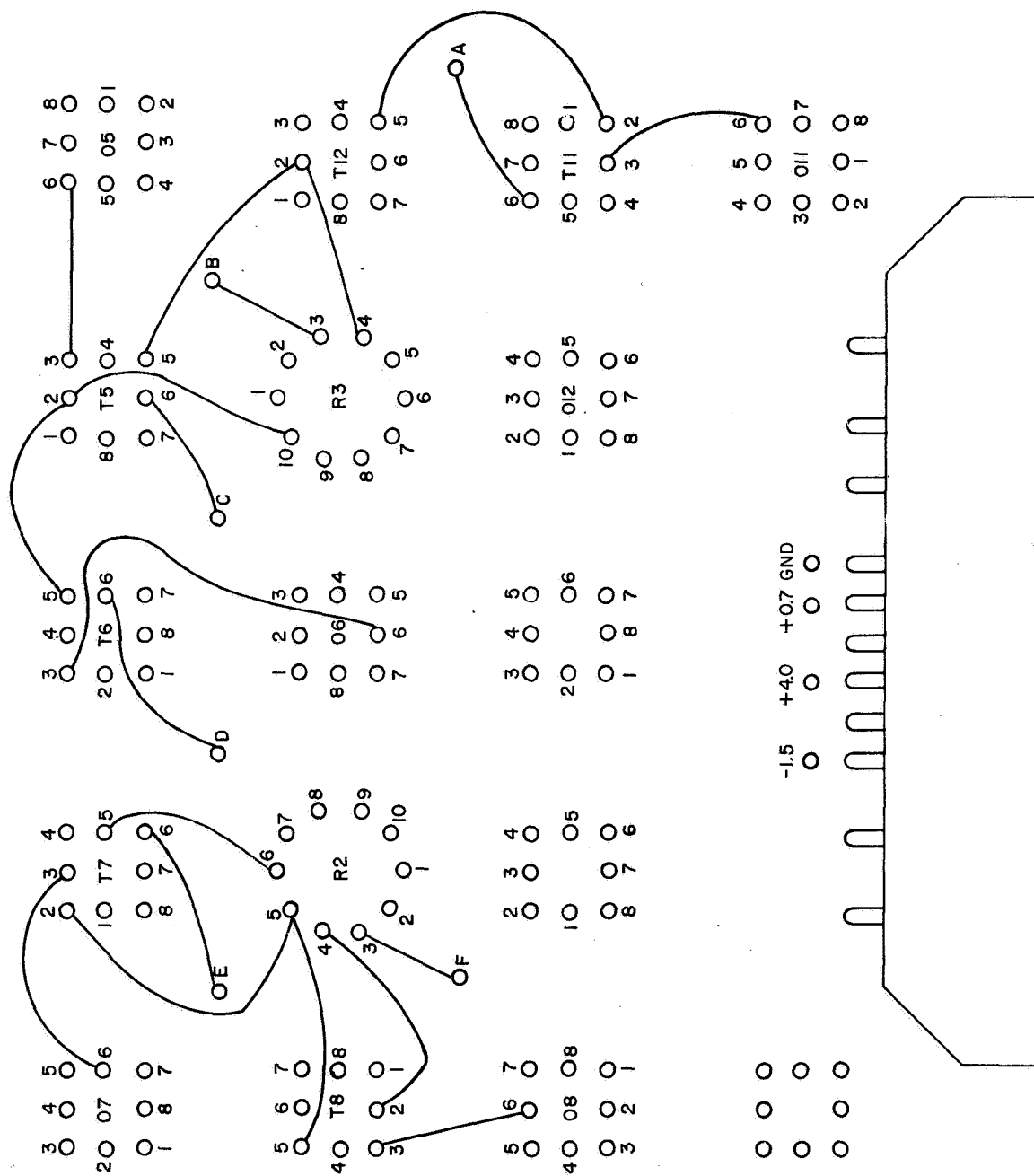


Fig. 22. System wiring diagram, top of lower board, module side.

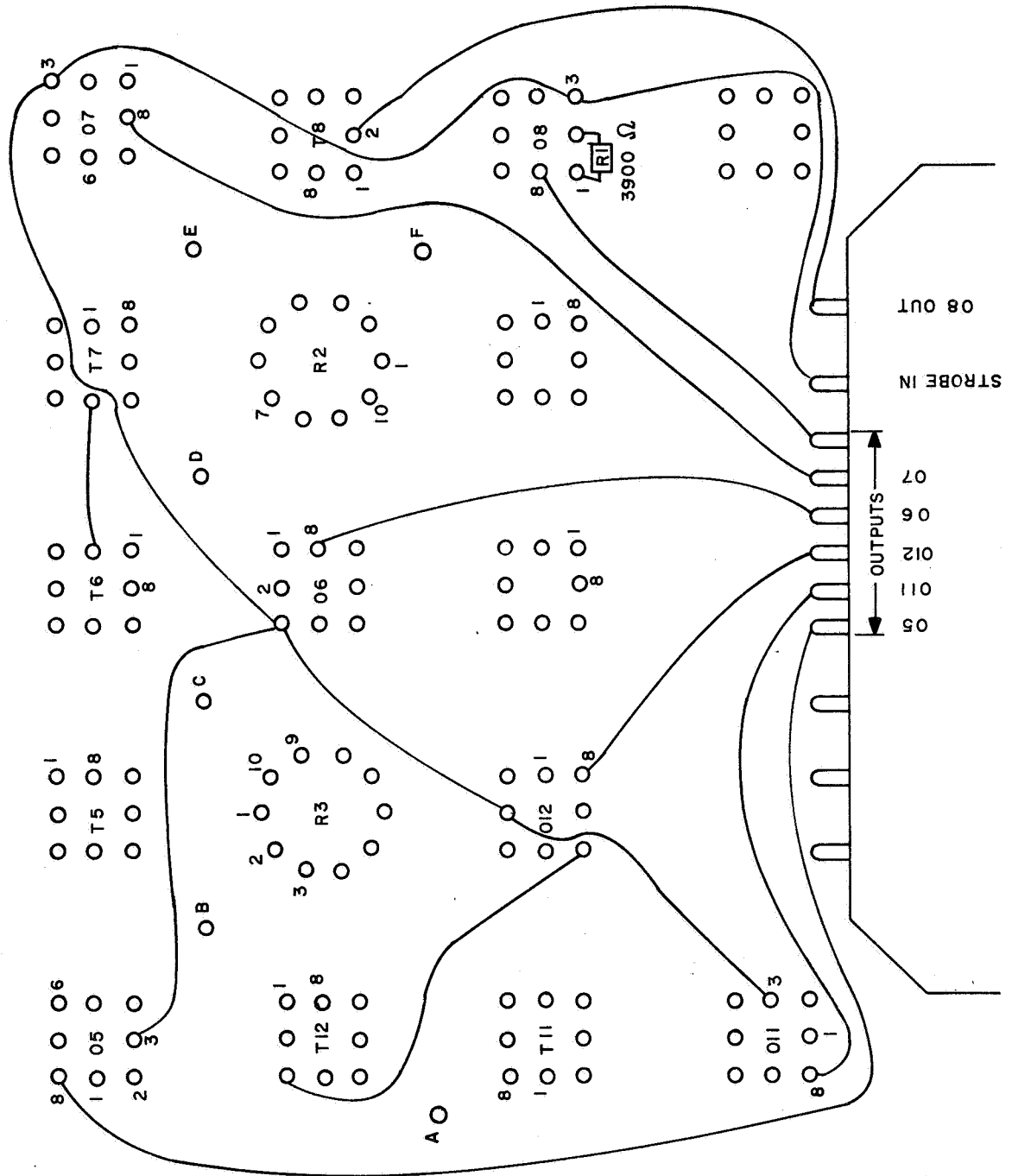


Fig. 23. System wiring diagram, bottom of lower board, outer side.

The bias voltages are bypassed at the connector with $0.1 \mu\text{f}$ (25 V) capacitors. Additional bypassing of $0.1 \mu\text{f}$ (3 V) is provided on the boards for the -1.5 V and +0.7 V supplies.

Connections between the connector and the boards are made with 1 inch long jumpers which are composed of seven strands of 0.008 inch wire. These wires allow the connector to be pushed back between the two boards (Fig. 19) so that the connector and boards can be removed intact from the shielding enclosure seen in Fig. 24.

This aluminum enclosure is made with two removable lids, thereby making all circuit points readily available for testing and troubleshooting. These lids have a double edge which are inlaid with RF gasketing to ensure good shielding. Consequently, the system is housed in a well-shielded, easily accessible package.

D. CONNECTING TO THE SYSTEM

In order to monitor the states of the system, the output gates were connected to lamps by way of external lamp driving circuits. To keep extraneous signals from entering the system via the lamp driver lines (which are about 5 ft long) bypass capacitors of $0.1 \mu\text{f}$ were placed on the connector that mates with the system. The bias voltage supply lines were also bypassed in a like manner. Dynamic inputs to the system were brought into the mating connector on coaxial cable. To house these capacitors a brass box was attached to the mating part of the system connector. A sketch of this connector-box assembly is shown in Fig. 25. The miniature coax connector is attached to the side of the box so that output circuit 08 can be monitored without a bypass capacitor; consequently, the system noise response can be studied when the system is running in the dynamic mode.

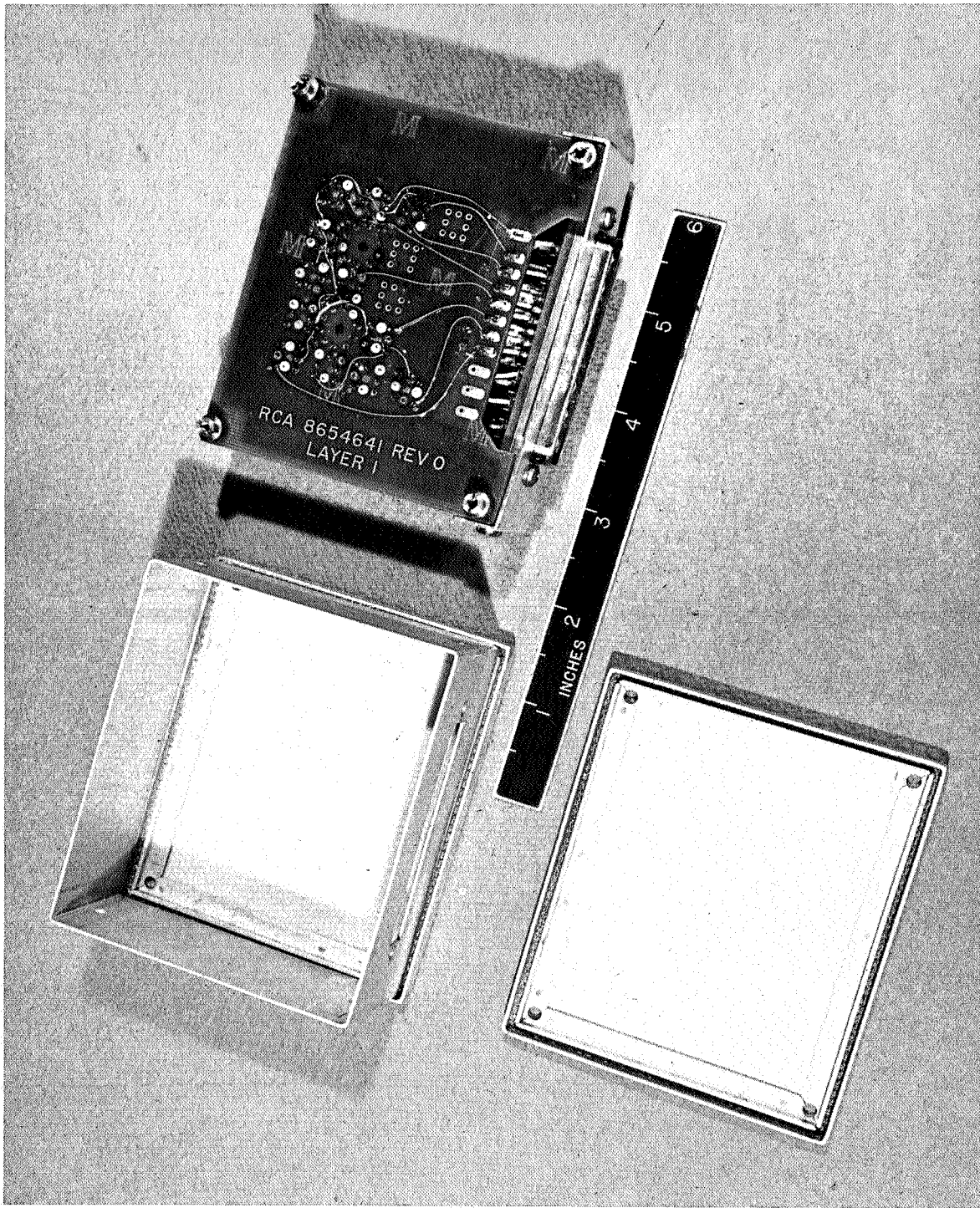


Fig. 24. Assembled system and shielding enclosure.

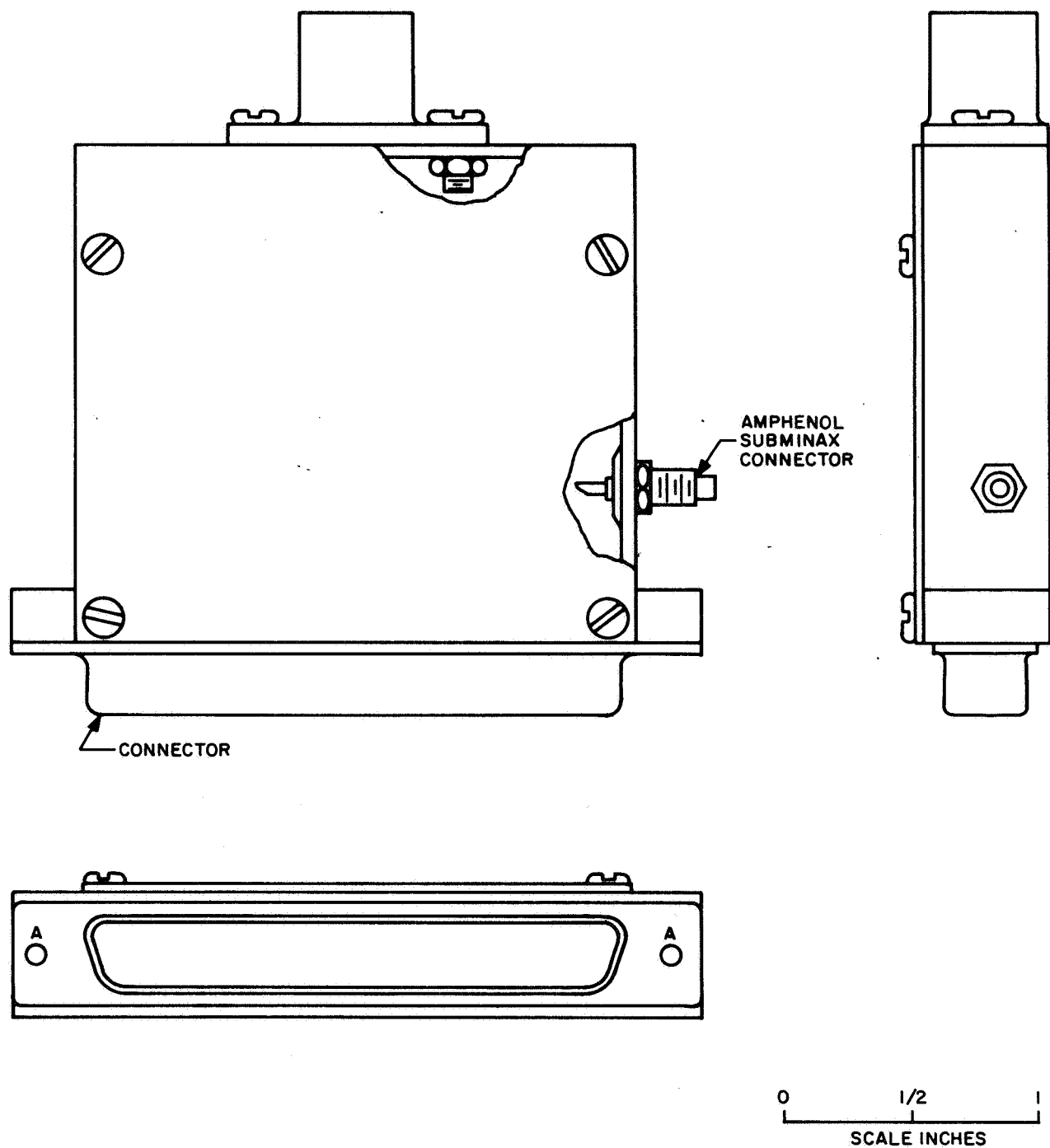


Fig. 25. Connector-box assembly for attaching to squaring counter system.

Section V

MEASUREMENTS OF SYSTEM OPERATION

A. NOISE SUSCEPTIBILITY

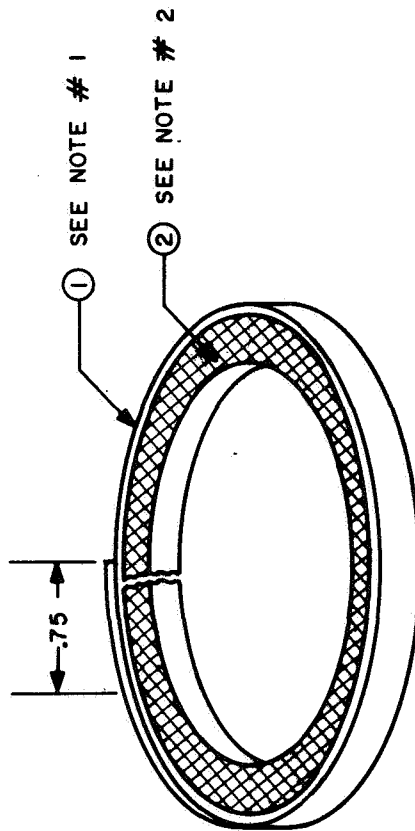
The system was checked for its immunity to noise by switching neon lights and a solder gun in direct physical contact with the system enclosure. Although these devices may be technically unaesthetic, they are excellent noise generators.

It was found that switching the soldering gun when in direct contact with either the system box or the connector box would not produce an error in the counter. However, by switching the gun and moving it simultaneously in contact with the system and connector boxes, the system would trigger while in the static, or non-counting, mode.

The weak link in the noise immunity chain was found to be the commercial connector. The effects of noise were completely eliminated by using a "washer" to cover this connector. This washer, shown in Fig. 26, makes tight contact to both boxes. A better connector might make this washer unnecessary.

B. SYSTEM REPETITION RATES

The system runs at a repetition rate of 4 MHz over the temperature range of -20°C to $+70^{\circ}\text{C}$. The linear counter stages T_1 through T_4 will function properly for an input signal of 17.3 MHz. This 17.3-MHz rate was observed with the oscilloscope probe on the output of T_4 . If the probe, with its capacitance of 2.6 pF, is placed on the output of T_1 , the input count frequency must be reduced to 15.6 MHz for T_1 to function properly. Consequently, an additional load capacitance of 2.6 pF in the counter stage reduces the operating frequency by 1.7 MHz.



NOTES:

1. LAP ENDS .75" AS SHOWN, AND SOFT SOLDER JOINT, THEN APPLY FINISH.

2. PLACE ITEM # ② INTO ITEM # ① AS SHOWN, AFTER FINISHING ITEM # ①

① MATERIAL: PHOSPHOR BRONZE STRIP 1.005" THK X.20" WIDE X 6.55" LONG

FINISH: BRIGHT DIP FOR COPPER AND COPPER ALLOYS (AFTER JOINING)

② MATERIAL: FORMED RFI GASKET, # 10117, 6.38" LG. PURCHASE FROM: TECHNICAL WIRE PRODUCTS, INC. CRANFORD, N.J.

Fig. 26. RFI washer, which completely encloses the commercial connector and makes tight forced contact to the system and connector boxes.

The effective operating frequency of the squaring counter stage T_6 is shown to be 17.3 MHz in Fig. 27. Here counter stage T_6 is triggered first by way of T_5 and then by the count input pulse via delay circuit D_3 . The resulting pair of triggering pulses appear across the tunnel diodes of counter stage T_6 . The time delay between these two pulses is 58 ns, which gives an effective repetition rate of 17.3 MHz. In Fig. 27, the result of this double trigger pulse is to switch counter stage T_6 from the "0" state to the "1" state and then back to the "0" state. Thus when the counter reaches steady state, stage T_6 has returned to its original state; but, in addition, a carry has been generated to change the state of counter stage T_7 .

C. BIAS VOLTAGE VARIATIONS

The counter circuits are most sensitive to voltage variations when the system is running. Thus the "1"/"0" pattern of the final counter stage, T_8 , was observed on an oscilloscope while bias variations were made. When this pattern deviated from the correct pattern, with the system receiving a continuous stream of count-input pulses, the system is said to fail. These correct "1"/"0" patterns are given for each counter stage in the system, in Fig. 28.

Because variations of the 4 V supply, E_B , had little effect on system operation, this supply was held constant during tests. The effects of worst case 10 percent variations in bias supply voltages, E_B , E_C and E_E , on the output circuit have already been discussed in conjunction with Table I.

The range of the E_C supply voltage is shown over the temperature -20°C to $+70^\circ\text{C}$ in Table III. Here the range of E_C for which the system functioned properly is recorded with E_B held constant at 4 V and E_E at ± 10 percent in addition to its nominal value of -1.5 volts. The E_C bias range variation with temperature is graphically shown in Fig. 29 for E_E at its nominal value. From Fig. 29 it is seen that the optimum value of E_C is 0.72 V. This value decreases $0.57 \text{ mV}/^\circ\text{C}$. For a nominal E_C value of 0.72 volt, the voltage range over which the system will function at -20°C is 18.7 percent; at

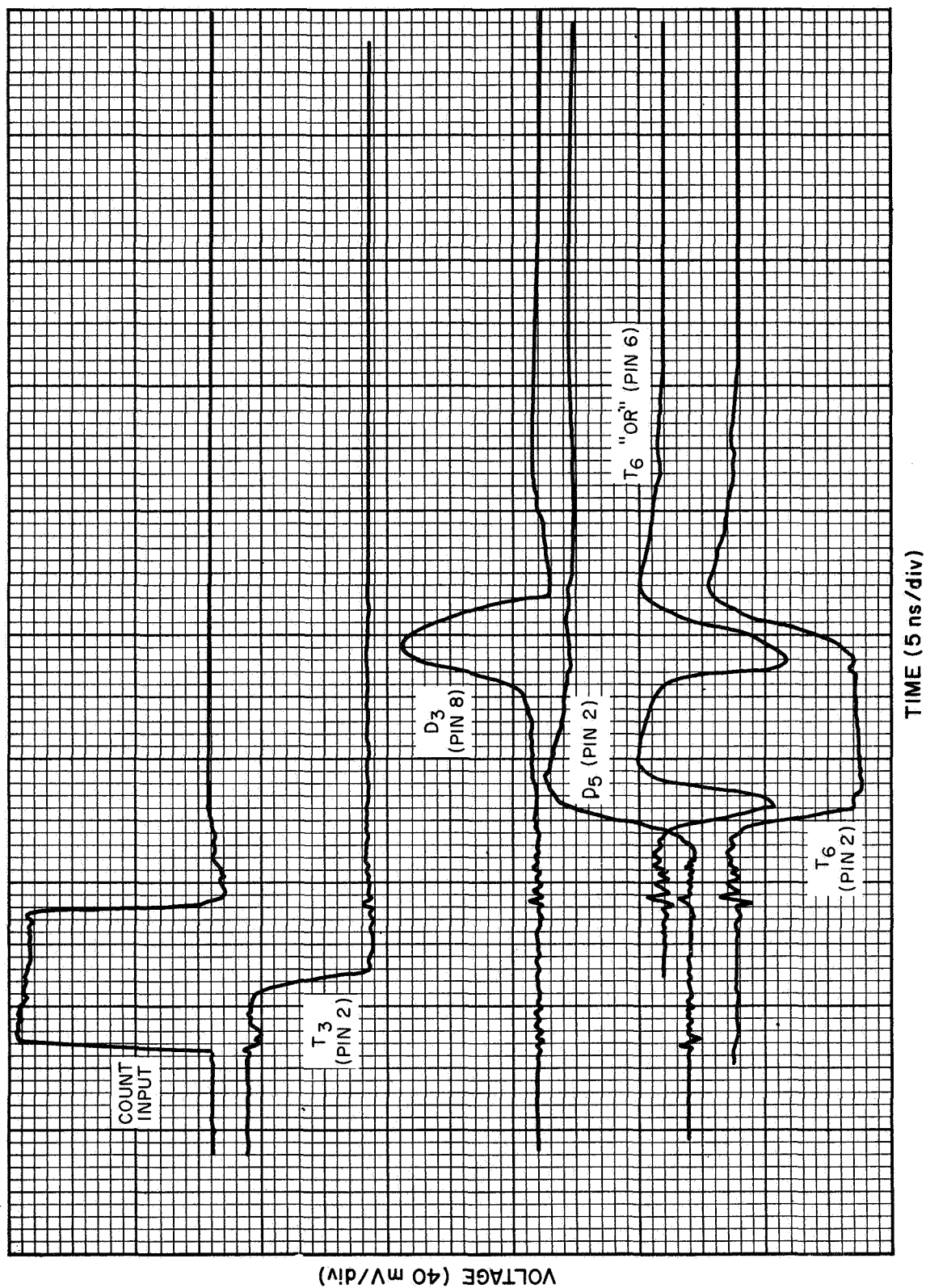
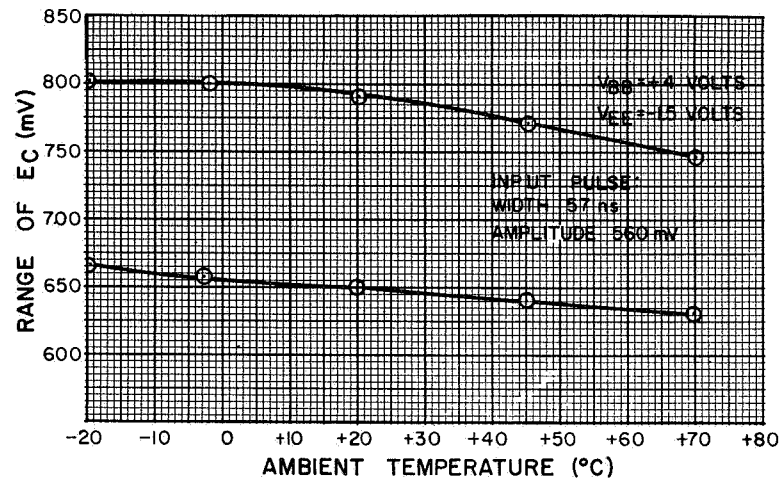


Fig. 27. Waveforms showing effective repetition rate of 17.3 MHz for squaring counter stage T₆.

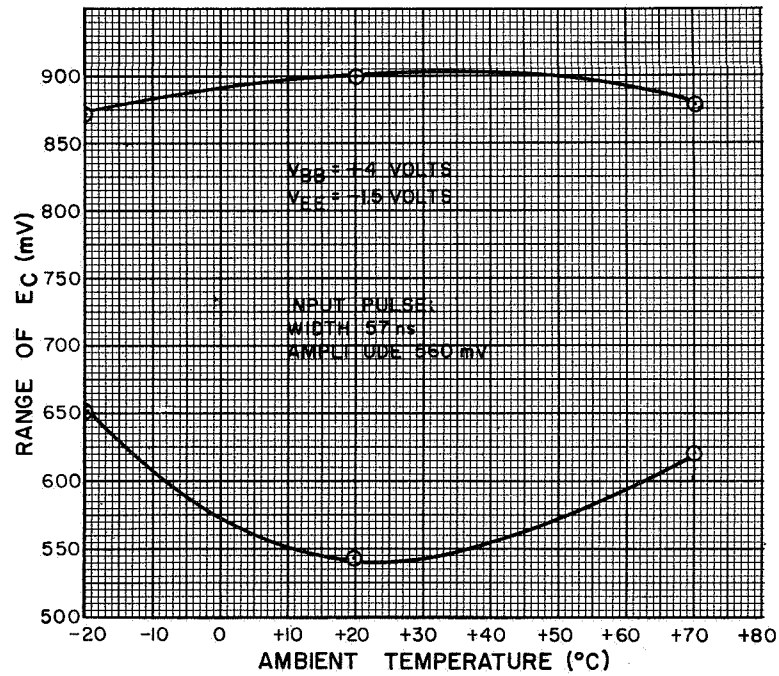
Time →		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
2^0	T_1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
2^1	T_2	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
2^2	T_3	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	0	0
2^3	T_4	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2^2	T_5	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0
2^3	T_6	0	0	0	1	0	1	0	0	0	0	1	0	1	0	0	0	0	0	0	1	0	1	0	1	0	0	0	0	0	0	0	0
2^4	T_7	0	0	0	0	1	1	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1	1	0	0
2^5	T_8	0	0	0	0	0	0	1	1	0	0	1	1	0	1	0	1	1	1	1	1	1	1	0	0	1	1	0	0	1	0	1	0

Notes: Carry producing intermediate states shown displaced.
Bar denotes period of counters.

Fig. 28. Free running patterns of system.



(a) Dynamic function.



(b) Static function.

Fig. 29. Variation in range of E_C as a function of temperature for which the system will properly function.

+20°C it is 19.4 percent; and at +70°C it is 16.7 percent. Consequently, the bias range narrows slightly with increasing temperature. Also shown in Fig. 29 is the E_C range over which the system is statically operable. As to be expected, this static range is much wider than the dynamic range. At room temperature the E_C voltage can go as low as 0.54 V and as high as 0.9 V before the system fails in the static mode.

As mentioned previously, the limitations on the E_C voltage supply are imposed by the delay circuits. To show the range of E_C when the Chow circuits are functioning as conventional counters, the linear counter (composed of stages T_1 through T_4) was observed. The bias range of the linear counters is about twice that of the squaring counter system, as can be seen in Table IV.

TABLE III. BIAS VOLTAGE VARIATIONS OF SQUARING COUNTER SYSTEM AS A FUNCTION OF TEMPERATURE

TEMP. (°C)	E _E MIN. (V)	RANGE OF E _C (V)	E _E NOM. (V)	RANGE OF E _C (V)	E _E MAX. (V)	RANGE OF E _C (V)
-20	-1.65	0.675-0.800	-1.5	0.665-0.800	-1.35	0.665-0.81
-3	-1.65	0.675-0.800	-1.5	0.655-0.800	-1.35	0.655-0.785
+20	-1.65	0.670-0.790	-1.5	0.650-0.790	-1.35	0.650-0.790
+45	-1.65	0.660-0.755	-1.5	0.640-0.770	-1.35	0.620-0.760
+70	-1.65	0.650-0.730	-1.5	0.630-0.745	-1.35	0.610-0.740

Note: E_B constant at 4 V; count-input repetition rate = 2 MHz.

TABLE IV. BIAS VOLTAGE VARIATION FOR LINEAR COUNTER AT ROOM TEMPERATURE

E _E MIN. (V)	RANGE OF E _C (V)	E _E NOM. (V)	RANGE OF E _C (V)	E _E MAX. (V)	RANGE OF E _C (V)
-1.65	0.635-0.900	-1.5	0.60-0.90	-1.35	0.595-0.900

Note: E_B = 4 V; count-input repetition rate = 2 MHz; temperature = 20°C.

Section VI

CONCLUSIONS

The tunnel-diode/transistor hybrid circuits function reliably and well. When careful attention is given to packaging details, tunnel diode circuits can be made impervious to noise.

The delay circuits decrease the system repetition rate by about 1 MHz and limit the tolerance of the 0.7 volt supply to about ± 8 percent. These limitations are not serious, considering that a delay of 80 ns is packaged on a TO-5 header with negligible signal degradation. Then, too, the delay circuit could be improved with the aid of a computer analysis.

It should be stated here that the TO-5 header is superior to the flat package for housing these circuits. This is primarily due to the size of the inductors and the ability to interconnect component wafers with the output lead risers of the TO-5 header.

All the objectives of the development program were met. The system functions properly over a temperature range of -20 to $+70^{\circ}\text{C}$ and is unaffected by noise. The counter circuits run at 17 MHz with a power dissipation of 0.9 mW and have a very wide tolerance to power supply variations. The output circuit provides the tunnel diode circuits with an excellent interface to other type logic circuits.

Where counting and shifting circuits that have speeds greater than 1 MHz and minimum power dissipation are required, tunnel-diode/transistor hybrid circuits are excellent.

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2. Bush, E. G. , "A tunnel-diode counter for satellite applications," NASA Technical Note D-1337, June 1962.