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Final Report
for
Nimbus Design Study
(30 December 1966)

Contract No.: NAS5-3787

Prepared by
Radiation Incorporated
Melbourne, Florida
for
Goddard Space Flight Center
Greenbelt, Maryland

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ABSTRACT

This report describes the efforts involved in determining the feasibility of modifying the present Nimbus PCM Telemetry Subsystem to provide new capabilities and improve present features with as little disturbance to the existing configuration as possible. The new capabilities included the addition of digital channel processing, satellite time as a telemetered parameter, and synchronization of the PCM unit with the spacecraft clock. Improvement of present capabilities included investigation of an analog gate having a higher breakdown voltage, a different sync word, improved switching functions, and investigation of recording a split phase RZ signal for a better signal to noise ratio. Necessary modifications to the associated Acceptance Test Equipment to accommodate the recommended changes were studied and reported. A new breakthrough in multiplexing analog data utilizing metallic oxide Semiconductor Field Effect Transistors is described.

The report concludes that the new system capabilities and the improvements upon the present system features are both feasible and desirable.

The recommendation is made to incorporate these items into the present system.

The Ground Equipment Study concerned the investigation of the feasibility of modifying the NIMBUS PCM Ground Station for compatibility with the data format changes as proposed in the Airborne Equipment section and provide data processing capability to improve overall system performance.

Synchronization with a new data format, decommutation, additions required to process increased data content capabilities, record and display of digital channels, and Time Code data covered a major portion of the scope of the study. Type of signal modulation was investigated to determine if improved S/N performance could be obtained with feasible, economical modification of the existing Ground Station. Test circuits were breadboarded, and a portion of the NIMBUS Ground Station was modified to obtain analysis data and demonstrate feasibility of proposed modifications.

The results of the study showed minor modifications of the Ground Station required for the new format, fairly extensive modification to one assembly to accommodate split phase signal modulation for maximum increase in S/N performance. Detailed modifications to Ground Station Simulator are shown and appear feasible and practical for adequate testing compatibility with proposed system changes.

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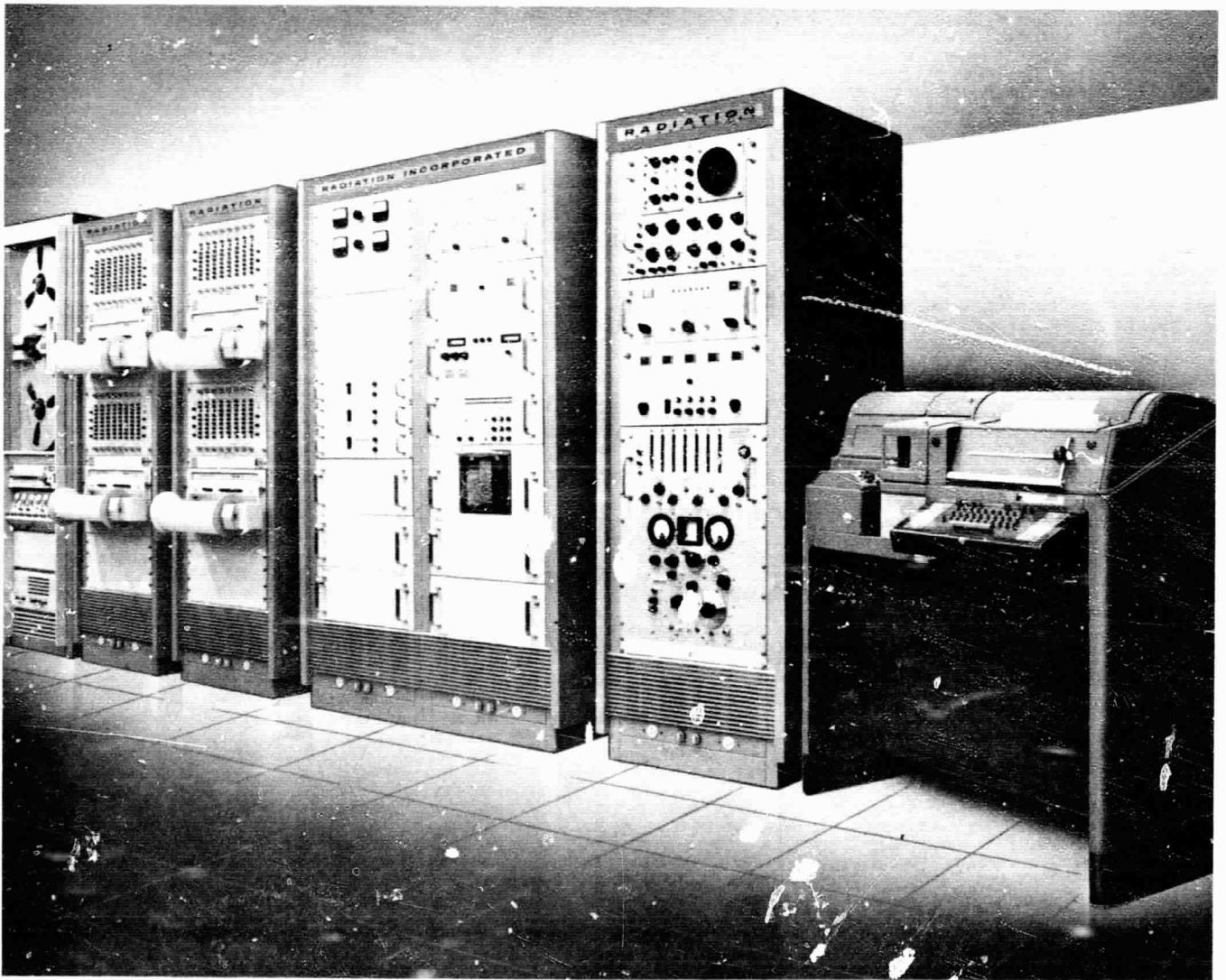
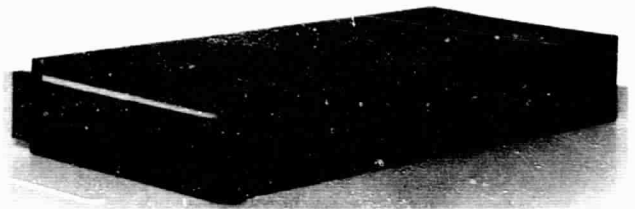
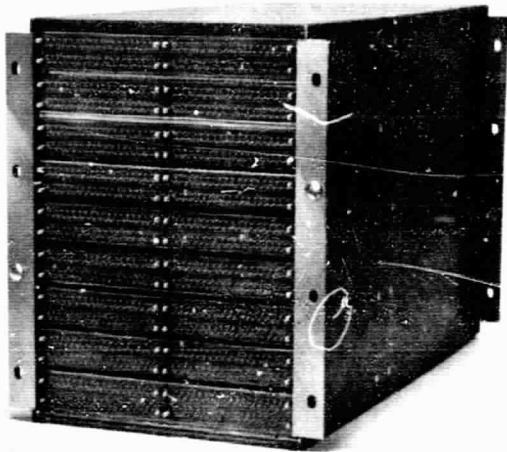
SECTION I

INTRODUCTION AND DISCUSSION

1. INTRODUCTION AND DISCUSSION

1.1 INTRODUCTION. - In order to provide new, and improve present, capabilities of the Nimbus Telemetry System a study was launched to determine the feasibility of modifying the existing system. The present Nimbus Telemetry System is a communications link between the Satellite and the ground station utilizing a 136 mc A. M. modulated carrier. The information transmitted and received consists of converted analog data with sync added in order to obtain intelligent interpretation of data, and command control signals. This report evaluates the results of the study and sets forth specific recommendations which will result in improvements to the existing system within reasonable economic limits. For the purposes of this study, separation is maintained between the Airborne and Ground equipments because of their relative independence except that Airborne equipment modifications initiated compatible Ground equipment changes. In all areas where functional changes concerned the complete system there was coordination in expanding ideas to insure system compatibility. It should be noted here that an important phase of the study involved microelectronic design which is covered in paragraph 1.6.5 and Section 2.

1.1.1 Airborne. - The major objectives of the Airborne Equipments Design study are tabulated in Table 1. The new capabilities are of importance in that analog is now supplemented with digital capability and Time Code insertion is of paramount importance. In addition, an objective of the study included



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Figure 1. Major Study Design Equipment, Nimbus System

determination of the effects of the modifications on existing Acceptance Test Equipment. A breadboard model was demonstrated successfully to prove the Multicoder for which one breadboard was constructed.

Table 1. Major Objectives of Airborne Design Study

New Capabilities	Improved Capabilities
a. Provide digital multiplexing.	a. Better PCM synchronization words generation and format.
b. Provide satellite time in PCM output format as a telemetered parameter.	b. Utilization of a split phase signal for Unit A output for better signal to noise ratio.
c. Provide synchronization of the PCM with Satellite clock.	c. Increased reliability and operating life in other areas.

1.1.2 Ground. - Objectives of Study Program concerning the Ground Station are practical design changes and minimum additions to the existing system enabling a modified ground station to accept and process data in proposed new format and using split phase signal modulation for A data.

1.2 SCOPE. - The Airborne scope of the study included performance to all objectives, building the required breadboards following design analysis, and this final report. The breadboard model sufficed to fulfill the objectives without extensive disturbance of the present hardware. The Ground equipment portion of the study encompassed modification of part of a Nimbus Ground Station to demonstrate the feasibility of accepting and processing the new type data in addition to providing indication that the Airborne objectives were attained. Necessary illustrations and procedures to support the study are included. The mechanics of the modifications are discussed where applicable, but detailed assembly

drawings are beyond the scope of this report. Some units such as the Beacon Transmitter and Tape Transport Unit are mentioned briefly in order to integrate the Study Design.

1.3 PRESENT AIRBORNE EQUIPMENT. - The present Nimbus Telemetry PCM Subsystem monitors test point signals at strategic locations within other subsystems of the Satellite. Figure 2 illustrates the present subsystem with its associated Input Test Equipment. The subsystem consists of the four components listed below:

- a. PCM Multicoder; so designated because it contains complete multiplexing and coding units in a single enclosure.
- b. Telemetry Electronics Equipment (TME).
- c. Tape Transport Unit; used for recording Unit A data from the Multicoder and playback on command from the Ground Station.
- d. Beacon Transmitter; provides the telemetry link to the Ground Station.

1.3.1 Unit A PCM. - This part of the Multicoder accepts analog input signals in the range of 0 to -6.4 volts from 542 analog channels and converts the analog to an equivalent seven bit binary code. The output signal is in NRZ serial format which is fed to the TME unit. Each output word at a bit rate of 500 cps consists of eight bits of which bit one is the sync bit. The sync bit is always a zero except in word one to every subframe in which it is a one. There are 64 words in each subframe and 16 subframes comprise a frame. Thirty-two of the words in each subframe are sampled at a rate of 1 sps and are called prime channels. The remaining 32 words are sampled at a rate of 1/16 sps and are called subcommutated channels. The prime channels in turn are divided into 30 analog channels and two channels of sync

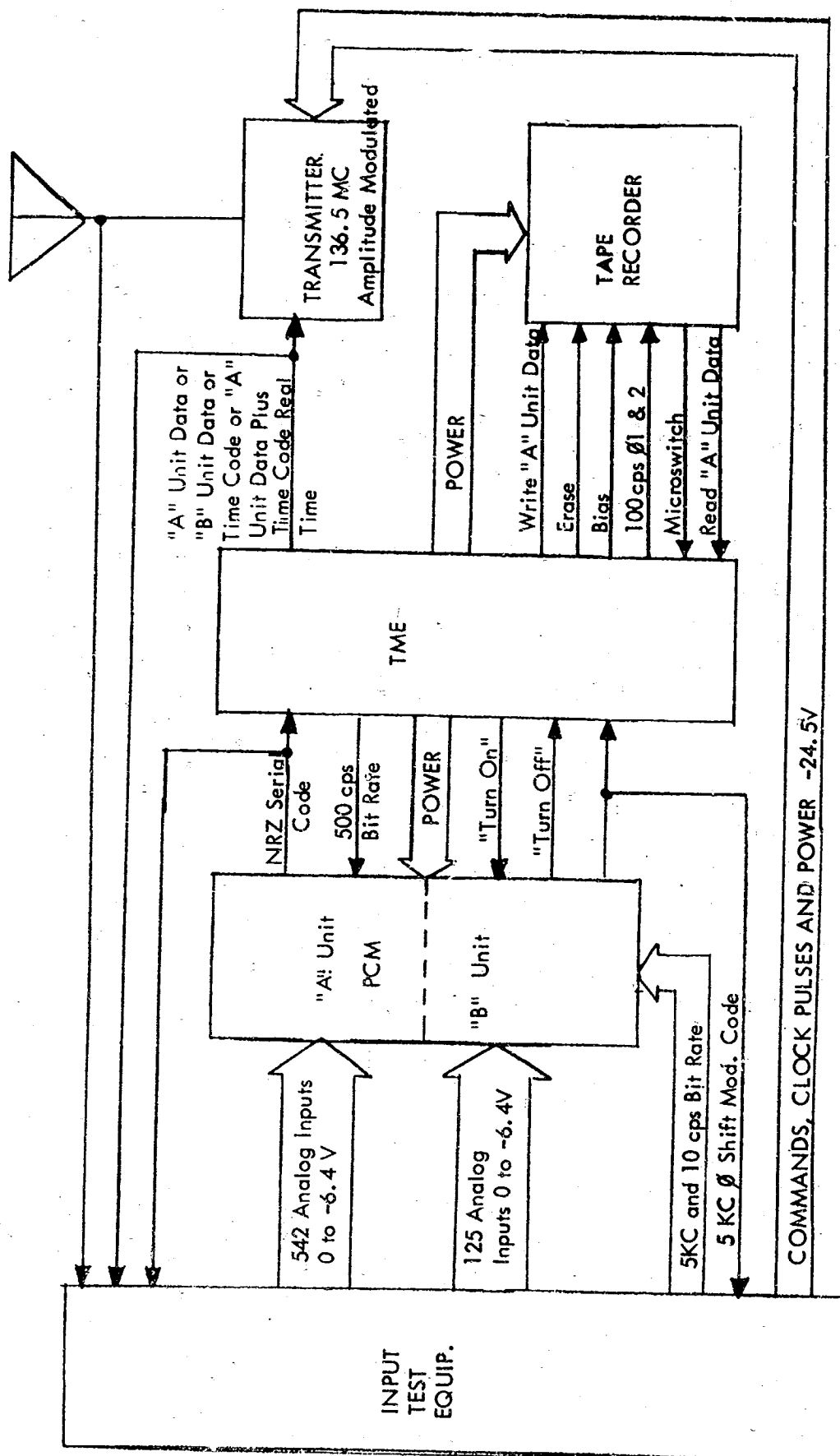


Figure 2. Present Nimbus PCM Subsystem, Test Connected

and subframe identification. The second word is used for sync with four "0" bits and subframe count of 0 to 15 for the remaining four bits. Data channel capability, therefore, amounts to 512 subcommutated channels and 30 prime channels for a total of 542 (exclusive of sync data). Normally Unit A has precedence over Unit B so that if Unit A's coder should fail the coder from Unit B would be switched in with a subsequent disabling of Unit B.

1.3.2 Unit B PCM. - This part of the Multicoder operates only on command, and then it cycles through its program of 128 words consisting of analog and three sync channels. Then it automatically turns off with no power usage until commanded to turn on again. Output data consists of seven bit binary code for analog as part of an eight bit word at a serial output bit rate of 10 cps. This results in 1024 bits per frame of 128 words for a maximum single channel capability sampling rate of one sample per 1.76 minutes. All output words from Unit B occur at the same sampling rate unless the inputs are supercommutated or subcommutated external to the Multicoder. The one output signal from Unit B is a 5 kc carrier which is phase-modulated by NRZ code at a 10 cps rate. A "1" bit shifts the carrier phase 180° while a "0" bit has no effect on the carrier.

1.3.3 Telemetry Electronics. - The Telemetry Electronics contains switching relays which are activated by commands from the satellite Master Clock. Functions performed by this switching are switching of the modulation input to the transmitter, power and RECORD-PLAYBACK mode switching of the tape transport, and emergency clock operation switching. The transmitter modulation switching selects one of four possible inputs. These inputs are stored, Unit A PCM data from the tape recorder, Time

Code data from the Master Clock, Unit A PCM data in real time combined with Time Code data, and Unit B PCM data in real time. The RECORD-PLAYBACK switching controls power to the tape transport unit and connects the tape transport head to the RECORD or PLAYBACK amplifier in the telemetry electronics as required. The emergency clock is switched on the event of Master Clock failure and provides the 500 cps bit rate and two-phase 100 cps required for operation of Unit A PCM and the Tape Transport unit. The Telemetry Electronics also contains the Unit A modulator which converts the NRZ code from the PCM to a gated sine wave signal in which a 500 cps sine wave represents a "0" in the serial code. This gated sine wave signal is then stored in the magnetic tape of the Tape Transport unit. Upon PLAYBACK command the stored data is read out through the playback amplifier in the Telemetry Electronics at 30 times the record speed and routed to the modulator input of the telemetry transmitter which transmits the data to the ground receiver station.

- 1.3.4 Input Test Equipment. - The input test equipment simulates the master clock, analog transducers and monitors the outputs of the PCM. One rack of equipment is used to check the operation of the PCM while another rack of equipment is used to check the TME. The test equipment for the PCM provides the input analog voltages (variable in 1 millivolt increments from 00.000 volts to minus 10.000 volts) and monitors operation of the selected channel to see if it performs to the required accuracy. More detailed information on the above described units is available in their respective "Handbook of Instructions" which are listed in the report bibliography as references 1, 2, 3 and 4.

1.4 DESIGN STUDY PCM SYSTEM. - The present Nimbus PCM systems are capable of processing only analog and sync data. It would be desirable to add a digital multiplexer to the PCM since it is inefficient to code a relay closing (digital device) with an analog to digital converter (ADC) where seven bit times are used. Because the Unit A data is stored on tape (at such times as the satellite is out of the telemetry link communications range) and read out at a later time, it would also be desirable to multiplex a Time Code into the output serial data for Time correlation purposes. This addition of digital and Time Code channels would improve the present system and at the same time permit sync words to be programmed bit by bit instead of word by word.

1.4.1 The existing Unit A of the Multicoder was modified so that the output format now contains Time Code and digital channel data in addition to analog and sync data. Table 2 comparison evaluates the existing and the modified systems. A block diagram of the modified Multicoder (figure 3) may be compared to the existing system (figure 2), and it is observed that the Input Test Equipment, TME, Transmitter, and Tape Recorder remain unchanged. The two additional blocks represent constructed breadboards for Unit A and the simulated additional inputs of the Input Test Equipment. The analog portion of the Multicoder remains unchanged except for an inhibit during digital channel processing and a change in the subframe word length from 64 to 62.5 in order to sync the Multicoder with the Time Code frame of once per second.

Table 2. Present Versus Study Nimbus Unit A PCM Channel Capability

Signal Identification	Present Nimbus Words Used	Study Nimbus Words Used
Sync and identification	2*	2.5*
Prime analog	30	22
Subcommutated analog	512	470
Time Code	0	6
Prime Digital	0	8 (56 bi-level)
Subcommutated digital	0	3 (21 bi-level)
Pulse digital with storage	0	1 (7 pulse inputs)
Words per frame	64	62.5
* Present Nimbus system contains sync words in which the bits are either all "ones's" or all "zero's". The Study Nimbus system sync words are selectable by bits in any combination.		

- 1.4.2 The PCM breadboard (figure 4) contains all the necessary modifications to the existing Unit A to incorporate Time Code and digital channel capability (table 3). Figure 5 illustrates the make-up of the breadboard chassis.
- 1.4.3 Input Impedance. - The PCM input impedance will be kept as large as possible to reduce input current requirements to a minimum for the input signal sources. The source impedance should be as low as is practical in order to keep signal source output voltage drop to a minimum.
- 1.4.4 New Input Signal Specifications. - These are tabulated in (table 4). In comparison with other similar PCM systems these values are typical, and normal circuit

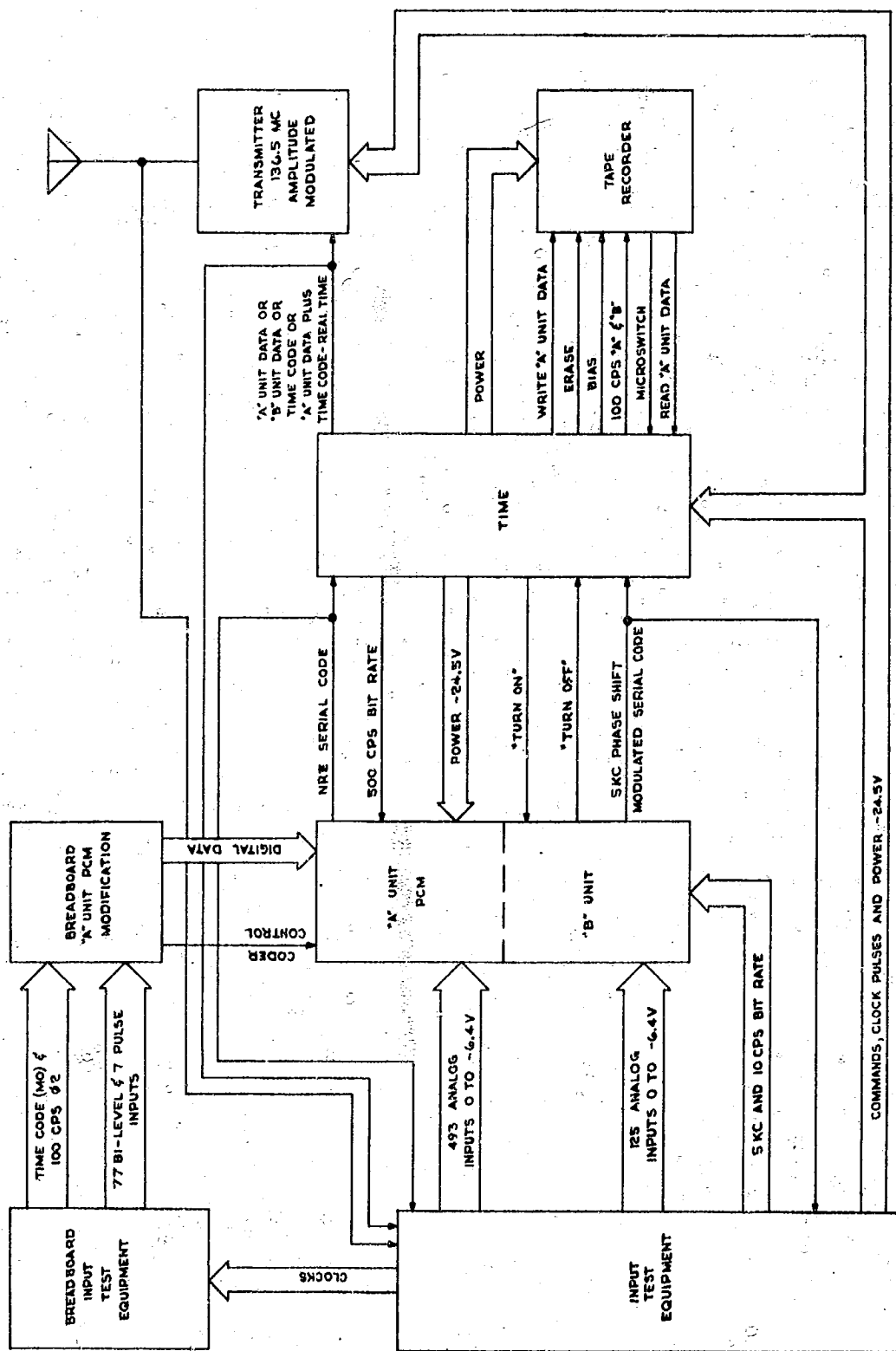


Figure 3. Study Nimbus PCM Subsystem Block Diagram, Test Connected

Table 3. Multi-coder Unit A Output Format for Nimbus "B" System (Sheet 1 of 16)

Subframe #1

<u>Time Slot</u>	<u>Matrix</u>	<u>Channel</u>	<u>Time Slot</u>	<u>Matrix</u>	<u>Channel</u>
1	P1	Sync #1	33	P17	1A11
2	P2	Sync #2 & ID	34	P18	1A12
3	A1	1/16A1	35	A9	1/16A12
4	B1	Units Sec.	36	B9	Ten Hours
5	P3	1D1	37	P19	1D5
6	P4	1A1	38	P20	1A13
7	A2	1/16A2	39	A10	1/16A13
8	B2	1/16A3	40	B10	1/16A14
9	P5	1A2	41	P21	1A14
10	P6	1A3	42	P22	1A15
11	A3	1/16A4	43	A11	1/16A15
12	B3	Tens Sec.	44	B11	1/16A16
13	P7	1D2	45	P23	1D6
14	P8	1A4	46	P24	1A16
15	A4	1/16A5	47	A12	1/16A17
16	B4	1/16A6	48	B12	1/16A18
17	P9	1A5	49	P25	1A17
18	P10	1A6	50	P26	1A18
19	A5	Units Min	51	A13	1/16A19
20	B5	1/16A7	52	B13	1/16A20
21	P11	1D3	53	P27	1D7
22	P12	1A7	54	P28	1A19
23	A6	Tens Min.	55	A14	1/16A21
24	B6	1/16A8	56	B14	1/16A22
25	P13	1A8	57	P29	1A20
26	P14	1A9	58	P30	1A21
27	A7	1/16A9	59	A15	1/16A23
28	B7	1/16A10	60	B15	1/16A24
29	P15	1D4	61	P31	1D8
30	P16	1A10	62	P32	1A22
31	A8	Unit Hours	63	A16	Sync #3
32	B8	1/16A11			

Table 3. Multi-coder Unit A Output Format for Nimbus "B" System (Sheet 2 of 16)

Subframe #2

<u>Time Slot</u>	<u>Matrix</u>	<u>Channel</u>	<u>Time Slot</u>	<u>Matrix</u>	<u>Channel</u>
64	P1	Sync #1	96	P17	1A11
65	P2	Sync #2 & 1D	97	P18	1A12
66	A17	1/16A25	98	A25	1/16A37
67	B17	1/16D1	99	B25	1/16A38
68	P3	1D1	100	P19	1D5
69	P4	1A1	101	P20	1A13
70	A18	1/16A26	102	A26	1/16A39
71	B18	1/16A27	103	B26	1/16A40
72	P5	1A2	104	P21	1A14
73	P6	1A3	105	P22	1A15
74	A19	1/16A28	106	A27	1/16A41
75	B19	1/16D2	107	B27	1/16A42
76	P7	1D2	108	P23	1D6
77	P8	1A4	109	P24	1A16
78	A20	1/16A29	110	A28	1/16A43
79	B20	1/16A30	111	B28	1/16A44
80	P9	1A5	112	P25	1A17
81	P10	1A6	113	P26	1A18
82	A21	1/16D3	114	A29	1/16A45
83	B21	1/16A31	115	B29	1/16A46
84	P11	1D3	116	P27	1D7
85	P12	1A7	117	P28	1A19
86	A22	1/16D4 Storage	118	A30	1/16A47
87	B22	1/16A32	119	B30	1/16A48
88	P13	1A8	120	P29	1A20
89	P14	1A9	121	P30	1A21
90	A23	1/16A33	122	A31	1/16A49
91	B23	1/16A34	123	B31	1/16A50
92	P15	1D4	124	P31	1D8
93	P16	1A10	125	P32	1A22
94	A24	1/16A35	126	A32	Sync #3
95	B24	1/16A36			

Table 3. Multi-coder Unit A Output Format for Nimbus "B" System (Sheet 3 of 16)

Subframe #3

<u>Time Slot</u>	<u>Matrix</u>	<u>Channel</u>	<u>Time Slot</u>	<u>Matrix</u>	<u>Channel</u>
127	P1	Sync #1	159	P17	1A11
128	P2	Sync #2 & ID	160	P18	1A12
129	A33	1/16A51	161	A41	1/16A67
130	B33	1/16A52	162	B41	1/16A68
131	P3	ID1	163	P19	ID5
132	P4	1A1	164	P20	1A13
133	A34	1/16A53	165	A42	1/16A69
134	B34	1/16A54	166	B42	1/16A70
135	P5	1A2	167	P21	1A14
136	P6	1A3	168	P22	1A15
137	A35	1/16A55	169	A43	1/16A71
138	B35	1/16A56	170	B43	1/16A72
139	P7	ID2	171	P23	ID6
140	P8	1A4	172	P24	1A16
141	A36	1/16A57	173	A44	1/16A73
142	B36	1/16A58	174	B44	1/16A74
143	P9	1A5	175	P25	1A17
144	P10	1A6	176	P26	1A18
145	A37	1/16A59	177	A45	1/16A75
146	B37	1/16A60	178	B45	1/16A76
147	P11	ID3	179	P27	ID7
148	P12	1A7	180	P28	1A19
149	A38	1/16A61	181	A46	1/16A77
150	B38	1/16A62	182	B46	1/16A78
151	P13	1A8	183	P29	1A20
152	P14	1A9	184	P30	1A21
153	A39	1/16A63	185	A47	1/16A79
154	B39	1/16A64	186	B47	1/16A80
155	P15	ID4	187	P31	ID8
156	P16	1A10	188	P32	1A22
157	A40	1/16A65	189	A48	Sync #3
158	B40	1/16A66			

Table 3. Multi-coder Unit A Output Format for Nimbus "B" System (Sheet 4 of 16)

Subframe #4

Time Slot	Matrix	Channel	Time Slot	Matrix	Channel
190	P1	Sync #1	222	P17	1A11
191	P2	Sync #2 & ID	223	P18	1A12
192	A49	1/16A81	224	A57	1/16A97
193	B49	1/16A82	225	B57	1/16A98
194	P3	ID1	226	P19	ID5
195	P4	1A1	227	P20	1A13
196	A50	1/16A83	228	A58	1/16A99
197	B50	1/16A84	229	B58	1/16A100
198	P5	1A2	230	P21	1A14
199	P6	1A3	231	P22	1A15
200	A51	1/16A85	232	A59	1/16A101
201	B51	1/16A86	233	B59	1/16A102
202	P7	ID2	234	P23	ID6
203	P8	1A4	235	P24	1A16
204	A52	1/16A87	236	A60	1/16A103
205	B52	1/16A88	237	B60	1/16A104
206	P9	1A5	238	P25	1A17
207	P10	1A6	239	P26	1A18
208	A53	1/16A89	240	A61	1/16A105
209	B53	1/16A90	241	B61	1/16A106
210	P11	ID3	242	P27	ID7
211	P12	1A7	243	P28	1A19
212	A54	1/16A91	244	A62	1/16A107
213	B54	1/16A92	245	B62	1/16A108
214	P13	1A8	246	P29	1A20
215	P14	1A9	247	P30	1A21
216	A55	1/16A93	248	A63	1/16A109
217	B55	1/16A94	249	B63	1/16A110
218	P15	ID4	250	P31	ID8
219	P16	1A10	251	P32	1A22
220	A56	1/16A95	252	A64	Sync #3
221	B56	1/16A96			

Table 3. Multi-coder Unit A Output Format for Nimbus "B" System (Sheet 5 of 16)

Subframe #5

Time Slot	Matrix	Channel	Time Slot	Matrix	Channel
253	P1	Sync #1	285	P17	1A11
254	P2	Sync #2 & ID	286	P18	1A12
255	A65	1/16A111	287	A73	1/16A127
256	B65	1/16A112	288	B73	1/16A128
257	P3	ID1	289	P19	ID5
258	P4	1A1	290	P20	1A13
259	A66	1/16A113	291	A74	1/16A129
260	B66	1/16A114	292	B74	1/16A130
261	P5	1A2	293	P21	1A14
262	P6	1A3	294	P22	1A15
263	A67	1/16A115	295	A75	1/16A131
264	B67	1/16A116	296	B75	1/16A132
265	P7	ID2	297	P23	ID6
266	P8	1A4	298	P24	1A16
267	A68	1/16A117	299	A76	1/16A133
268	B68	1/16A118	300	B76	1/16A134
269	P9	1A5	301	P25	1A17
270	P10	1A6	302	P26	1A18
271	A69	1/16A119	303	A77	1/16A135
272	B69	1/16A120	304	B77	1/16A136
273	P11	ID3	305	P27	ID7
274	P12	1A7	306	P28	1A19
275	A70	1/16A121	307	A78	1/16A137
276	B70	1/16A122	308	B78	1/16A138
277	P13	1A8	309	P29	1A20
278	P14	1A9	310	P30	1A21
279	A71	1/16A123	311	A79	1/16A139
280	B71	1/16A124	312	B79	1/16A140
281	P15	ID4	313	P31	ID8
282	P16	1A10	314	P32	1A22
283	A72	1/16A125	315	A80	Sync #3
284	B72	1/16A126			

Table 3. Multi-coder Unit A Output Format for Nimbus "B" System (Sheet 6 of 16)

Subframe #6					
Time Slot	Matrix	Channel	Time Slot	Matrix	Channel
316	P1	Sync #1	348	P17	1A11
317	P2	Sync #2 & ID	349	P18	1A12
318	A81	1/16A141	350	A89	1/16A157
319	B81	1/16A142	351	B89	1/16A158
320	P3	ID1	352	P19	ID5
321	P4	1A1	353	P20	1A13
322	A82	1/16A143	354	A90	1/16A159
323	B82	1/16A144	355	B90	1/16A160
324	P5	1A2	356	P21	1A14
325	P6	1A3	357	P22	1A15
326	A83	1/16A145	358	A91	1/16A161
327	B83	1/16A146	359	B91	1/16A162
328	P7	ID2	360	P23	ID6
329	P8	1A4	361	P24	1A16
330	A84	1/16A147	362	A92	1/16A163
331	B84	1/16A148	363	B92	1/16A164
332	P9	1A5	364	P25	1A17
333	P10	1A6	365	P26	1A18
334	A85	1/16A149	366	A93	1/16A165
335	B85	1/16A150	367	B93	1/16A166
336	P11	ID3	368	P27	ID7
337	P12	1A7	369	P28	1A19
338	A86	1/16A151	370	A94	1/16A167
339	B86	1/16A152	371	B94	1/16A168
340	P13	1A8	372	P29	1A20
341	P14	1A9	373	P30	1A21
342	A87	1/16A153	374	A95	1/16A169
343	B87	1/16A154	375	B95	1/16A170
344	P15	ID4	376	P31	ID3
345	P16	1A10	377	P32	1A22
346	A88	1/16A155	378	A96	Sync #3
347	B88	1/16A156			

Table 3. Multi-coder Unit A Output Format for Nimbus "B" System (Sheet 7 of 16)

Subframe #7

Time Slot	Matrix	Channel	Time Slot	Matrix	Channel
379	P1	Sync #1	411	P17	1A11
380	P2	Sync #2 & ID	412	P18	1A12
381	A97	1/16A171	413	A105	1/16A187
382	B97	1/16A172	414	B105	1/16A188
383	P3	1D1	415	P19	1D5
384	P4	1A1	416	P20	1A13
385	A98	1/16A173	417	A106	1/16A189
386	B98	1/16A174	418	B106	1/16A190
387	P5	1A2	419	P21	1A14
388	P6	1A3	420	P22	1A15
389	A99	1/16A175	421	A107	1/16A191
390	B99	1/16A176	422	B107	1/16A192
391	P7	1D2	423	P23	1D6
392	P8	1A4	424	P24	1A16
393	A100	1/16A177	425	A108	1/16A193
394	B100	1/16A178	426	B108	1/16A194
395	P9	1A5	427	P25	1A17
396	P10	1A6	428	P26	1A18
397	A101	1/16A179	429	A109	1/16A195
398	B101	1/16A180	430	B109	1/16A196
399	P11	1D3	431	P27	1D7
400	P12	1A7	432	P28	1A19
401	A102	1/16A181	433	A110	1/16A197
402	B102	1/16A182	434	B110	1/16A198
403	P13	1A8	435	P29	1A20
404	P14	1A9	436	P30	1A21
405	A103	1/16A183	437	A111	1/16A199
406	B103	1/16A184	438	B111	1/16A200
407	P15	1D4	439	P31	1D8
408	P16	1A10	440	P32	1A22
409	A104	1/16A185	441	A112	Sync #3
410	B104	1/16A186			

Table 3. Multi-coder Unit A Output Format for Nimbus "B" System (Sheet 8 of 16)
Subframe #8

Time Slot	Matrix	Channel	Time Slot	Matrix	Channel
442	P1	Sync #1	474	P17	1A11
443	P2	Sync #2 & ID	475	P18	1A12
444	A113	1/16A201	476	A121	1/16A217
445	B113	1/16A202	477	B121	1/16A218
446	P3	1D1	478	P19	1D5
447	P4	1A1	479	P20	1A13
448	A114	1/16A203	480	A122	1/16A219
449	B114	1/16A204	481	B122	1/16A220
450	P5	1A2	482	P21	1A14
451	P6	1A3	483	P22	1A15
452	A115	1/16A205	484	A123	1/16A221
453	B115	1/16A206	485	B123	1/16A222
454	P7	1D2	486	P23	1D6
455	P8	1A4	487	P24	1A16
456	A116	1/16A207	488	A124	1/16A223
457	B116	1/16A208	489	B124	1/16A224
458	P9	1A5	490	P25	1A17
459	P10	1A6	491	P26	1A18
460	A117	1/16A209	492	A125	1/16A225
461	B117	1/16A210	493	B125	1/16A226
462	P11	1D3	494	P27	1D7
463	P12	1A7	495	P28	1A19
464	A118	1/16A211	496	A126	1/16A227
465	B118	1/16A212	497	B126	1/16A228
466	P13	1A8	498	P29	1A20
467	P14	1A9	499	P30	1A21
468	A119	1/16A213	500	A127	1/16A229
469	B119	1/16A214	501	B127	1/16A230
470	P15	1D4	502	P31	1D8
471	P16	1A10	503	P32	1A22
472	A120	1/16A215	504	A128	Sync #3
473	B120	1/16A216			

Table 3. Multi-coder Unit A Output Format for Nimbus "B" System (Sheet 9 of 16)

Subframe #9

Time Slot	Matrix	Channel	Time Slot	Matrix	Channel
505	P1	Sync #1	537	P17	1A11
506	P2	Sync #2 & ID	538	P18	1A12
507	A129	1/16A231	539	A137	1/16A247
508	B129	1/16A232	540	B137	1/16A248
509	P3	1D1	541	P19	1D5
510	4	1A1	542	P20	1A13
511	A130	1/16A233	543	A138	1/16A249
512	B130	1/16A234	544	B138	1/16A250
513	P5	1A2	545	P21	1A14
514	P6	1A3	546	P22	1A15
515	A131	1/16A235	547	A139	1/16A251
516	B131	1/16A236	548	B139	1/16A252
517	P7	1D2	549	P23	1D6
518	P8	1A4	550	P24	1A16
519	A132	1/16A237	551	A140	1/16A253
520	B132	1/16A238	552	B140	1/16A254
521	P9	1A5	553	P25	1A17
522	P10	1A6	554	P26	1A18
523	A133	1/16A239	555	A141	1/16A255
524	B133	1/16A240	556	B141	1/16A256
525	P11	1D3	557	P27	1D7
526	P12	1A7	558	P28	1A19
527	A134	1/16A241	559	A142	1/16A257
528	B134	1/16A242	560	B142	1/16A258
529	P13	1A8	561	P29	1A20
530	P14	1A9	562	P30	1A21
531	A135	1/16A243	563	A143	1/16A259
532	B135	1/16A244	564	B143	1/16A260
533	P15	1D4	565	P31	1D8
534	P16	1A10	566	P32	1A22
535	A136	1/16A245	567	A144	Sync #3
536	B136	1/16A246			

Table 3. Multi-coder Unit A Output Format for Nimbus "B" System (Sheet 10 of 16)

Subframe #10

Time Slot	Matrix	Channel	Time Slot	Matrix	Channel
568	P1	Sync #1	600	P17	1A11
569	P2	Sync #2 & ID	601	P18	1A12
570	A145	1/16A261	602	A153	1/16A277
571	B145	1/16A262	603	B153	1/16A278
572	P3	1D1	604	P19	1D5
573	P4	1A1	605	P20	1A13
574	A146	1/16A263	606	A154	1/16A279
575	B146	1/16A264	607	B154	1/16A280
576	P5	1A2	608	P21	1A14
577	P6	1A3	609	P22	1A15
578	A147	1/16A265	610	A155	1/16A281
579	B147	1/16A266	611	B155	1/16A282
580	P7	1D2	612	P23	1D6
581	P8	1A4	613	P24	1A16
582	A148	1/16A267	614	A156	1/16A283
583	B148	1/16A268	615	B156	1/16A284
584	P9	1A5	616	P25	1A17
585	P10	1A6	617	P26	1A18
586	A149	1/16A269	618	A157	1/16A285
587	B149	1/16A270	619	B157	1/16A286
588	P11	1D3	620	P27	1D7
589	P12	1A7	621	P28	1A19
590	A150	1/16A271	622	A158	1/16A287
591	A150	1/16A272	623	B158	1/16A288
592	P13	1A8	624	P29	1A20
593	P14	1A9	625	P30	1A21
594	A151	1/16A273	626	A159	1/16A289
595	B151	1/16A274	627	B159	1/16A290
596	P15	1D4	628	P31	1D8
597	P16	1A10	629	P32	1A22
598	A152	1/16A275	630	A160	Sync #3
599	B152	1/16A276			

Table 3. Multi-coder Unit A Output Format for Nimbus "B" System (Sheet 11 of 16)

Subframe #11

Time Slot	Matrix	Channel	Time Slot	Matrix	Channel
631	P1	Sync #1	663	P17	1A11
632	P2	Sync #2 & ID	664	P18	1A12
633	A161	1/16A291	665	A169	1/16A307
634	B161	1/16A292	666	B169	1/16A308
635	P3	1D1	667	P19	1D5
636	P4	1A1	668	P20	1A13
637	A162	1/16A293	669	A170	1/16A309
638	B162	1/16A294	670	B170	1/16A310
639	P5	1A2	671	P21	1A14
640	P6	1A3	672	P22	1A15
641	A163	1/16A295	673	A171	1/16A311
642	B163	1/16A296	674	B171	1/16A312
643	P7	1D2	675	P23	1D6
644	P8	1A4	676	P24	1A16
645	A164	1/16A297	677	A172	1/16A313
646	B164	1/16A298	678	B172	1/16A314
647	P9	1A5	679	P25	1A17
648	P10	1A6	680	P26	1A18
649	A165	1/16A299	681	A173	1/16A315
650	B165	1/16A300	682	B173	1/16A316
651	P11	1D3	683	P27	1D7
652	P12	1A7	684	P28	1A19
653	A166	1/16A301	685	A174	1/16A317
654	B166	1/16A302	686	B174	1/16A318
655	P13	1A8	687	P29	1A20
656	P14	1A9	688	P30	1A21
657	A167	1/16A303	689	A175	1/16A319
658	B167	1/16A304	690	B175	1/16A320
659	P15	1D4	691	P31	1D8
660	P16	1A10	692	P32	1A22
661	A168	1/16A305	693	A176	Sync #3
662	B168	1/16A306			

Table 3. Multi-coder Unit A Output Format for Nimbus "B" System (Sheet 12 of 16)

Subframe #12

Time Slot	Matrix	Channel	Time Slot	Matrix	Channel
694	P1	Sync #1	726	P17	1A11
695	P2	Sync #2 & ID	727	P18	1A12
696	A177	1/16A321	728	A185	1/16A337
697	B177	1/16A322	729	B185	1/16A338
698	P3	1D1	730	P19	1D5
699	P4	1A1	731	P20	1A13
700	A178	1/16A323	732	A186	1/16A339
701	B178	1/16A324	733	B186	1/16A340
702	P5	1A2	734	P21	1A14
703	P6	1A3	735	P22	1A15
704	A179	1/16A325	736	A187	1/16A341
705	B179	1/16A326	737	B187	1/16A342
706	P7	1D2	738	P23	1D6
707	P8	1A4	739	P24	1A16
708	A180	1/16A327	740	A188	1/16A343
709	B180	1/16A328	741	B188	1/16A344
710	P9	1A5	742	P25	1A17
711	P10	1A6	743	P26	1A18
712	A181	1/16A329	744	A189	1/16A345
713	B181	1/16A330	745	B189	1/16A346
714	P11	1D3	746	P27	1D7
715	P12	1A7	747	P28	1A19
716	A182	1/16A331	748	A190	1/16A347
717	B182	1/16A332	749	B190	1/16A348
718	P13	1A8	750	P29	1A20
719	P14	1A9	751	P30	1A21
720	A183	1/16A333	752	A191	1/16A349
721	B183	1/16A334	753	B191	1/16A350
722	P15	1D4	754	P31	1D8
723	P16	1A10	755	P32	1A22
724	A184	1/16A335	756	A192	Sync #3
725	B184	1/16A336			

Table 3. Multi-coder Unit A Output Format for Nimbus "B" System (Sheet 13 of 16)

Subframe #13

Time Slot	Matrix	Channel	Time Slot	Matrix	Channel
757	P1	Sync #1	789	P17	1A11
758	P2	Sync #2 & ID	790	P18	1A12
759	A193	1/16A351	791	A201	1/16A367
760	B193	1/16A352	792	B201	1/16A368
761	P3	ID1	793	P19	ID5
762	P4	1A1	794	P20	1A13
763	A194	1/16A353	795	A202	1/16A369
764	B194	1/16A354	796	B202	1/16A370
765	P5	1A2	797	P21	1A14
766	P6	1A3	798	P22	1A15
767	A195	1/16A355	799	A203	1/16A371
768	B195	1/16A356	800	B203	1/16A372
769	P7	ID2	801	P23	ID6
770	P8	1A4	802	P24	1A16
771	A196	1/16A357	803	A204	1/16A373
772	B196	1/16A358	804	B204	1/16A374
773	P9	1A5	805	P25	1A17
774	P10	1A6	806	P26	1A18
775	A197	1/16A359	807	A205	1/16A375
776	B197	1/16A360	808	B205	1/16A376
777	P11	ID3	809	P27	ID7
778	P12	1A7	810	P28	1A19
779	A198	1/16A361	811	A206	1/16A377
780	B198	1/16A362	812	B206	1/16A378
781	P13	1A8	813	P29	1A20
782	P14	1A9	814	P30	1A21
783	A199	1/16A363	815	A207	1/16A379
784	B199	1/16A364	816	B207	1/16A380
785	P15	ID4	817	P31	ID8
786	P16	1A10	818	P32	1A22
787	A200	1/16A365	819	A208	Sync #3
788	B200	1/16A366			

Table 3. Multi-coder Unit A Output Format for Nimbus "B" System (Sheet 14 of 16)

Subframe #14

Time Slot	Matrix	Channel	Time Slot	Matrix	Channel
820	P1	Sync #1	852	P17	1A11
821	P2	Sync #2 & ID	853	P18	1A12
822	A209	1/16A381	854	A217	1/16A397
823	B209	1/16A382	855	B217	1/16A398
824	P3	1D1	856	P19	1D5
825	P4	1A1	857	P20	1A13
826	A210	1/16A383	858	A218	1/16A399
827	B210	1/16A384	859	B218	1/16A400
828	P5	1A2	860	P21	1A14
829	P6	1A3	861	P22	1A15
830	A211	1/16A385	862	A219	1/16A401
831	B211	1/16A386	863	B219	1/16A402
832	P7	1D2	864	P23	1D6
833	P8	1A4	865	P24	1A16
834	A212	1/16A387	866	A220	1/16A403
835	B212	1/16A388	867	B220	1/16A404
836	P9	1A5	868	P25	1A17
837	P10	1A6	869	P26	1A18
838	A213	1/16A389	870	A221	1/16A405
839	B213	1/16A390	871	B221	1/16A406
840	P11	1D3	872	P27	1D7
841	P12	1A7	873	P28	1A19
842	A214	1/16A391	874	A222	1/16A407
843	A214	1/16A391	875	B222	1/16A408
844	P13	1A8	876	P29	1A20
845	P14	1A9	877	P30	1A21
846	A215	1/16A393	878	A223	1/16A409
847	B215	1/16A394	879	B223	1/16A410
848	P15	1D4	880	P31	1D8
849	P16	1A10	881	P32	1A22
850	A216	1/16A395	882	A224	Sync #3
851	B216	1/16A396			

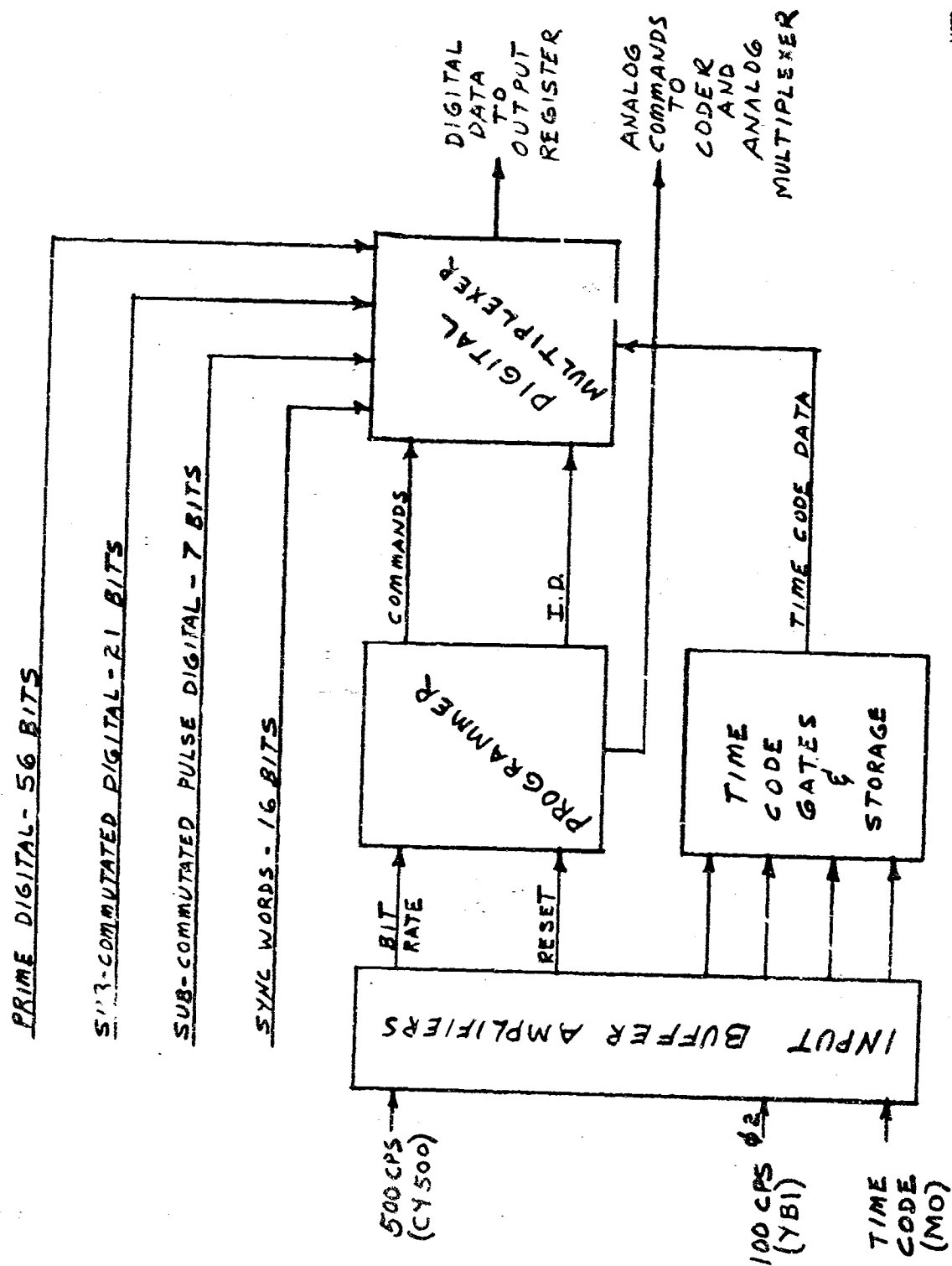
Table 3. Multi-coder Unit A Output Format for Nimbus "B" System (Sheet 15 of 16)

Subframe #15

Time Slot	Matrix	Channel	Time Slot	Matrix	Channel
883	P1	Sync #1	915	P17	1A11
884	P2	Sync #2 & ID	916	P18	1A12
885	A225	1/16A411	917	A233	1/16A427
886	B225	1/16A412	918	B233	1/16A428
887	P3	1D1	919	P19	1D5
888	P4	1A1	920	P20	1A13
889	A226	1/16A413	921	A234	1/16A429
890	B226	1/16A414	922	B234	1/16A430
891	P5	1A2	923	P21	1A14
892	P6	1A3	924	P22	1A15
893	A227	1/16A415	925	A235	1/16A431
894	B227	1/16A416	926	B235	1/16A432
895	P7	1D2	927	P23	1D6
896	P8	1A4	928	P24	1A16
897	A228	1/16A417	929	A236	1/16A433
898	B228	1/16A418	930	B236	1/16A434
899	P9	1A5	931	P25	1A17
900	P10	1A6	932	P26	1A18
901	A229	1/16A419	933	A237	1/16A435
902	B229	1/16A420	934	B237	1/16A436
903	P11	1D3	935	P27	1D7
904	P12	1A7	936	P28	1A19
905	A230	1/16A421	937	A238	1/16A437
906	B230	1/16A422	938	B238	1/16A438
907	P13	1A8	939	P29	1A20
908	P14	1A9	940	P30	1A21
909	A231	1/16A423	941	A239	1/16A439
910	B231	1/16A424	942	B239	1/16A440
911	P15	1D4	943	P31	1D8
912	P16	1A10	944	P32	1A22
913	A232	1/16A425	945	A240	Sync #3
914	B232	1/16A426			

Table 3. Multi-coder Unit A Output Format for Nimbus "B" System (Sheet 16 of 16)

Subframe #16					
Time Slot	Matrix	Channel	Time Slot	Matrix	Channel
946	P1	Sync #1	978	P17	1A11
947	P2	Sync #2 & ID	979	P18	1A12
948	A241	1/16A441	980	A249	1/16A457
949	B241	1/16A442	981	B249	1/16A458
950	P3	ID1	982	P19	ID5
951	P4	1A1	983	P20	1A13
952	A242	1/16A443	984	A250	1/16A459
953	B242	1/16A444	985	B250	1/16A460
954	P5	1A2	986	P21	1A14
955	P6	1A3	987	P22	1A15
956	A243	1/16A445	988	A251	1/16A461
957	B243	1/16A446	989	B251	1/16A462
958	P7	ID2	990	P23	ID6
959	P8	1A4	991	P24	1A16
960	A244	1/16A447	992	A252	1/16A463
961	B244	1/16A448	993	B252	1/16A464
962	P9	1A5	994	P25	1A17
963	P10	1A6	995	P26	1A18
964	A245	1/16A449	996	A253	1/16A465
965	B245	1/16A450	997	B253	1/16A466
966	P11	ID3	998	P27	ID7
967	P12	1A7	999	P28	1A19
968	A246	1/16A451	1000	A254	1/16A467
969	B246	1/16A452	1001	B254	1/16A468
970	P13	1A8	1002	P29	1A20
971	P14	1A9	1003	P30	1A21
972	A247	1/16A453	1004	A255	1/16A469
973	B247	1/16A454	1005	B255	1/16A470
974	P15	ID4	1006	P31	ID8
975	P16	1A10	1007	P32	1A22
976	A248	1/16A455	1008	A256	Sync #3
977	B248	1/16A456			



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Figure 4. Simplified Block Diagram of Unit A PCM Breadboard

A 1	8:1 Counter
A 2	62.5:1 Counter
A 3	16:1 Counter
A 4	1 CPS Reset & Coder Control
A 5	Programmer
A 6	Programmer
A 7	Programmer
A 8	Programmer
A 9	Digital Multiplexer Strobe Command and Driver
A10	Digital Multiplexer Gates
A11	Digital Multiplexer Gates
A12	Digital Multiplexer Gates
A13	Digital Multiplexer Gates
A14	Digital Multiplexer Gates
A15	Digital Multiplexer Gates
A16	Digital Multiplexer Gates
A17	Digital Multiplexer Gates
A18	Core Drivers
A19	Bias Amplifier and I. D. Buffer
A20	Storage Bistables and Reset
A21	Time Code Storage Shift Register, Shift Driver, and Time Code Buffer
A22	Time Code Storage
A23	1 CPS Reset, Time Code Buffer

Figure 5. Nimbus PCM Breadboard Chassis (Front View)

designs are flexible enough to accept these values ($\pm 50\%$), or greater, depending on the parameter varied. However, all these specifications are tentative and the table should be studied to correct unrealistic values. If these assumed values differ by a very large percentage, then trouble may be encountered in design. The input circuits may become more complex; power dissipation and physical size requirements may increase.

Table 4. Nimbus Study System Input Signal Specifications

Circuit	Source Impedance (Ohms)	Volts	Up-Level Milliamps. Max.	Volts	Down-Level Milliamps. Max.
Analog Channel	3,300	0		-6.4	
Digital Bi-level	1,000	0 to -1.0	1.5	-5 to -24	0.01
Digital Pulse*	1,000	0 to -1.0	0.01	-5.50 -24	1.0
Pulse Width Time Code	(MO) 2,700	0 to -0.2	0.01	-1 to 5.4	1.0
500 cps Bit Rat (CY 500)	2,900	0 to -0.2	0.01	-1 to -5.8	1.0
100 cps Clock (YBI)**	300	0 to 2.5	0.01	-20 to -24	0.5

* PW = 250 ms

T_r 10 ms

T_r 10 ms

** Nimbus
"A" or "C"
Clock

1.5 MULTICODER REQUIREMENTS. - Stringent requirements were followed in the modification.

These requirements precluded changing the physical dimensioning of the present package and coder redundancy features. Existing circuits were to be either unchanged or changed a minimum amount; power increase was to be held to less than 1.5 watts, and the modifications were to be compatible with both A and C Nimbus Master Clocks. To insure reliability, worst case conditions were assumed for the design approach. Temperature environment for the circuits was limited to the range of -10°C to $+65^{\circ}\text{C}$. Component parameters were conservatively rated to allow an adequate safety margin. In most cases, breakdown voltages for derated transistor junctions were derated 50% from the maximum ratings. Where the breakdown voltages were exceeded at the V_{BE} junction in circuits having large negative voltages, diodes were inserted in series to prevent reverse current flow. In calculating the base current and derated value for h_{FE} was assumed to insure adequate drive. Worse case characteristics of the transistor parameters V_{BE} , V_{CESAT} , I_{CBO} , C_{ob} , and C_{ib} were used along with worse case tolerance limits of the passive elements in determining the final component values. A typical example of worse case design equations for a simple inverter and equivalent step function is shown in figure 6. One trade off encountered in using a worse case design technique is that of increased power consumption. However, the final increase was only approximately 15 % of the allotted power, justifying the worse case design approach.

1.5.1 Synchronization and Programming. - All of the clock inputs to the PCM plus the Time Code are connected through input level adjusting buffer amplifiers. The 500 cps bit rate and the detected 1 cps Time Code control the counters in the programmer. The counters still function as before in respect to the analog multiplexer except that

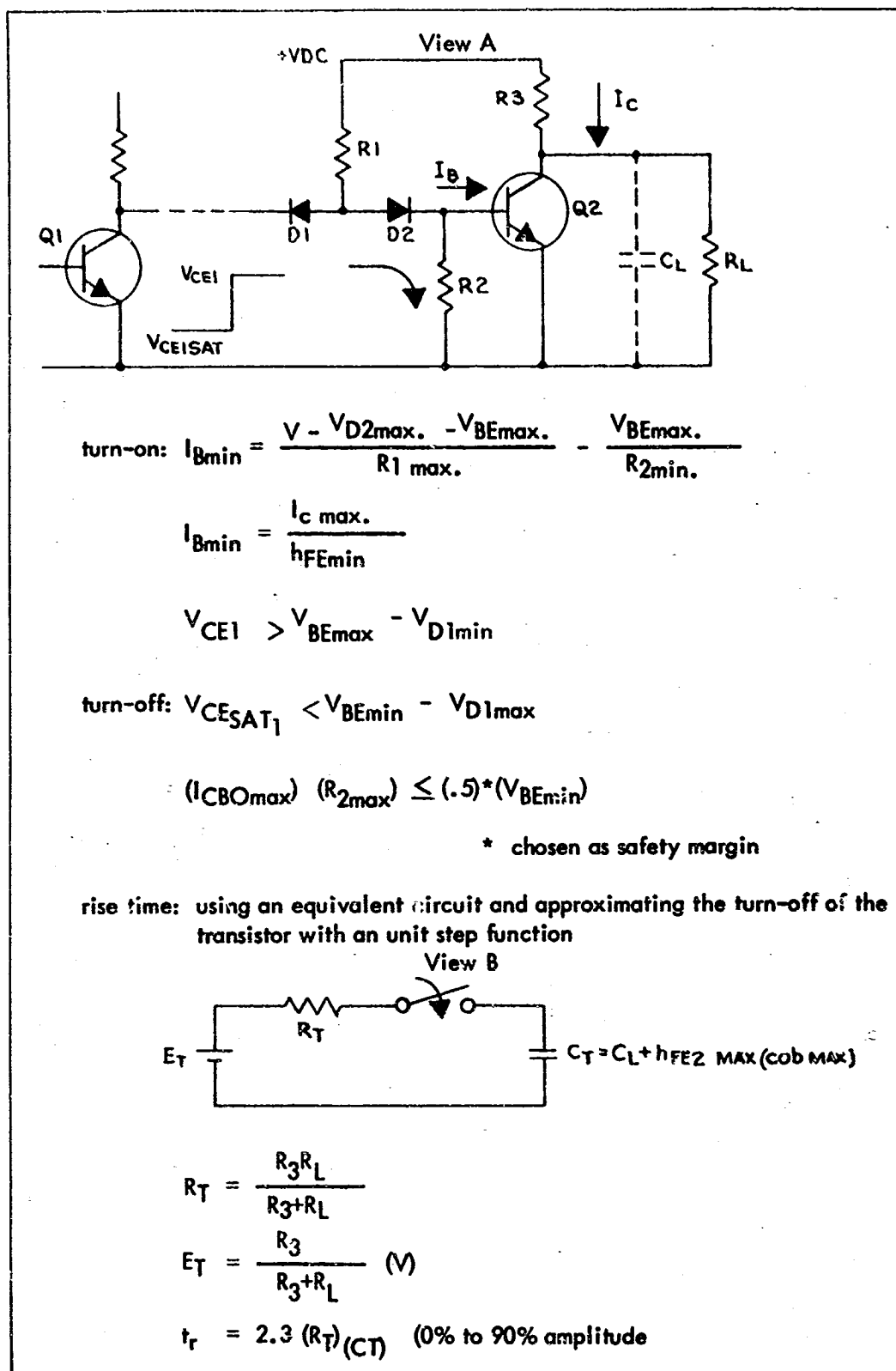


Figure 6. Circuits to Illustrate Worst Case Design Approach

one analog control circuit is added to control the coder. Diode matrices are added to control the digital multiplexer functions. By these means the programmer controls Unit A of the Multicoder.

1.5.2 Time Code Insertion. - Two new control signals have been added to Unit A PCM to place the free-running Time Code in the output PCM format. These signals, 100 cps $\phi 2$ and the pulse width modulated Time Code, are connected through buffer amplifiers into the Time Code control circuitry where the Time Code is accumulated four bits at a time and stored until the programmer reads the four bits through the digital multiplexer into the shift register. The Time Code storage register is automatically cleared before new data is stored. Thus the input Time Code storage circuits are completely independent of the PCM programmer, and it is up to the programmer to strobe the Time Code digital multiplexer gate at the proper time to place the Time Code bits in the output Register before new Time Code data is stored.

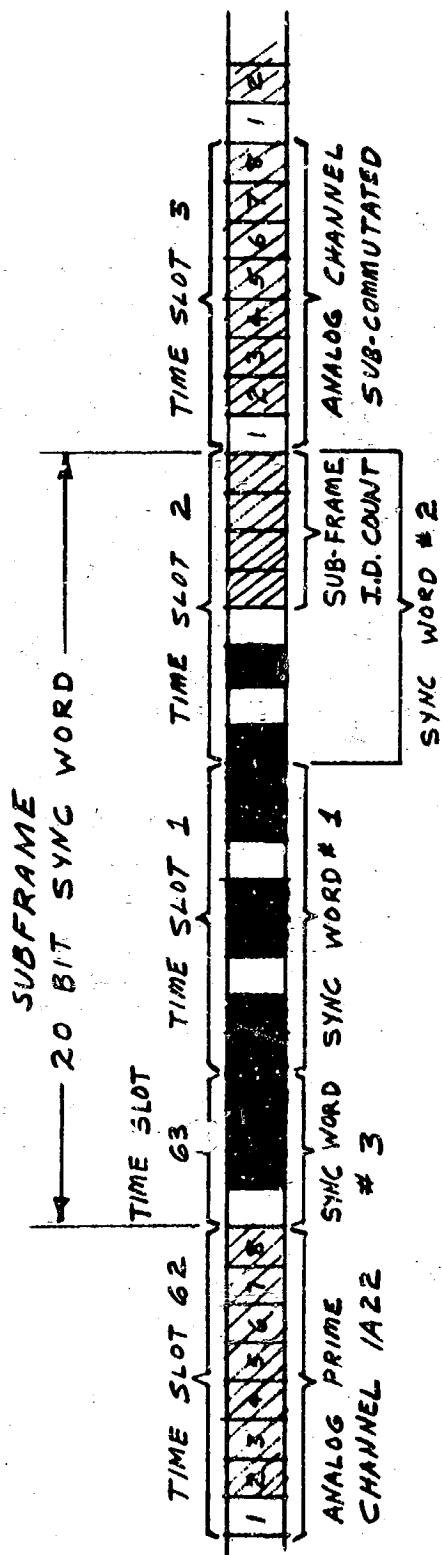
1.5.3 Digital Channels. - The digital multiplexer controls one set of SET windings in the output register and both the "A" and "B" coders still control individual sets of SET windings in the output register. Therefore the output register set windings still function as an OR gate with the new digital multiplexing capability completely independent of the analog multiplexers as long as both do not feed their set windings at the same time. To control this possibility and to prevent it from happening, another OR gate is located in the programmer so that whenever any digital word occurs it prevents the coder power switch from turning on. This control is located at the output of the word rate counter and controls the word rate regardless of which

coder is being used. If the word rate square wave is turned off, the coder power switch will not turn on and the coder will not allow current to flow in its output register set windings. The digital multiplexer contains the following 16 digital gate circuits.

- a. 8 gates for prime digital data
- b. 3 gates for subcommutated digital data.
- c. 1 gate for subcommutated pulse digital data.
- d. 1 gate for the Time Code.
- e. 3 gates for sync and subframe identification.

1.5.4 Sync Word. - The present sync word contains 16 bits with the first eight bits being all "1's", the next 4 bits being "0's" and the last four bits being the subframe identification count from the programmer's 16:1 counter. The Study Nimbus PCM will have 20 bits of subframe sync as shown in (figure 7). The first 16 bits can be selected to any combination of "1's" and "0's" by hard wiring the sync word digital multiplexer word gate inputs to Power Supply Command for a "0" and -24.5V for a "1". The optimum code combination for synchronizing the Nimbus ground station was determined and is shown in figure 7 since 8 adjacent "1's" do not occur as a sync word, a new sync word detector will have to be placed in the PCM Test Set to provide proper decommutation. This can be a simple serial 16 bit shift register that resets the test set to word 1.5 upon coincidence of the sync word in the register.

1.6 MULTICODER BREADBOARD CONSTRUCTION. - With the Multicoder requirements firmed (paragraph 1.5), detailed design of the circuits was initiated with the selection of



- NOTES:
1. SUB-FRAME SYNC WORD CONTAINS 20 BITS.
 2. FIRST 16 BITS ARE FIXED IN THE DIGITAL MULTIPLEXER TO THE CODE 0111-11011011-1010.
 3. LAST 4 BITS ARE SUB-FRAME I.D. COUNT AND THE CODE SEQUENCES FROM 0000 THRU 1111.
 4. ABOVE FILLED BITS (■) ARE "ONES"
 5. ABOVE UN-FILLED BITS (□) ARE "ZEROS"
 6. ABOVE BITS (■) CAN BE EITHER "ONES" OR "ZEROS"

Figure 7. Subframe Sync Word

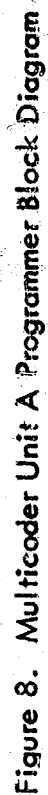
components and defining the design assumptions. In most cases the general design approach was already established because the logic design had been previously decided. Updating design and construction techniques as much as practical for this study, the digital word gates of the digital multiplexer utilized microelectronic circuits. The following paragraphs describe the logic design, component selection, and all detailed analysis data required to construct the breadboard.

1.6.1 Multicoder Component Selection. - The design of the circuits for the Nimbus Study was based on component selection conforming to certain worst case design parameters. In respect to transistor selection, these are tabulated in table 5 and parameters not defined are in accordance with manufacturer's specifications for similar devices. All transistors are assumed to have V_{BE} 0.8V at -10°C , V_{BE} 0.4V at 65°C and V_{CE} saturated -0.3V maximum at 65°C . The diode type used for all applications is the RAD 100613 similar to 1N916. This device has been used extensively in recent PCM systems and has an excellent reliability record. Worst case design voltage across the diode was set at 0.7V maximum at -10°C and 1 ma and at 0.4V minimum at 65°C and 0.5 ma. Other parameters are reflected in specification sheet. The resistors and capacitors used in the new circuitry are from the RAD 106115 series and the RAD 104228 series respectively. The first series designates the Allen Bradley carbon composition resistors, and the second series the Vitronman ceramic VK 20 CW type. As before, these components have excellent reliability records on previous spacecraft telemetry.

Table 5. Worst Case Design Parameters for Transistor Components

Specification	Parameters	
RAD 100817 NPN similar to 2N718A	$h_{FE} = 10 \text{ min at } -10^{\circ}\text{C}$ $I_C = 1 \text{ ma}$	$I_{CBO} = 160 \text{ na max. at } 65^{\circ}\text{C}$ $V_{CB} = 60\text{V}$
RAD 100823 NPN similar to 2N930	$h_{FE} = 40 \text{ min at } -10^{\circ}\text{C}$ $I_C = 1 \text{ ma}$	$I_{CBO} = 160 \text{ na max. at } 65^{\circ}\text{C}$ $V_{CB} = 45\text{V}$
RAD 100667 NPN similar to 2N753	$h_{FE} = 20 \text{ min at } -10^{\circ}\text{C}$ $I_C = 1 \text{ ma}$	$I_{CBO} = 160 \text{ na max. at } 65^{\circ}\text{C}$ $V_{CB} = 15\text{V}$
RAD 100422 PNP similar to 2N2412	$h_{FE} = 10 \text{ min at } -10^{\circ}\text{C}$ $I_C = 1 \text{ ma}$	$I_{CBO} = 160 \text{ na at } 65^{\circ}\text{C}$ $V_{CB} = -30\text{V}$
RAD 102258 PNP similar to 2N2412	$h_{FE} = 20 \text{ min at } -10^{\circ}\text{C}$ $I_C = 1 \text{ ma}$	$I_{CBO} = 160 \text{ na at } 65^{\circ}\text{C}$ $V_{CB} = -25\text{V}$

1.4.2 Programmer. - (See figure 8.) The programmer is still connected in the same manner to the analog multiplexer because the analog register and matrices operation is unchanged. For this reason, the digital multiplexer circuits alone are shown in the block diagram. All of the programmer blocks represent new circuitry except for the three counter blocks. The counters already exist in the present Nimbus system but have been modified somewhat. Additional outputs to the digital matrices are required from all three counters and external reset circuits have been added to the bit and word counter. The subframe counter controls the reset to the digital multiplexer input pulse (event storage bistables.) A 1 cps clock pulse is fed into the 62.5:1 word counter detector circuit to provide sync in the PCM output format.



This sync enables the system to properly multiplex Time Code data with analog and digital data. Note on the block diagram that the digital multiplexer data is independent (paragraph 1.5.3) of the analog coder used to code the "A" Unit Analog Multiplexer.

1.6.2.1 Since the Output Shift Register operates like a three input "OR" gate, it was quite easy to add to digital multiplexer capabilities, without affecting the existing analog capability except as to the quantity of inputs. The output register windings used for Units A and B coders have not been changed. The winding used for the subframe identification count has been reconnected to control all digital words including digital bilevel data, Time Code, sync words, identification count, and bit sync. Thus, the programmer has new diode matrices to generate the commands for controlling the digital multiplexer and Time Code storage. Buffer amplifiers have been added where necessary to generate the proper logic levels for system operation from the external clock commands.

1.6.2.2 The word counter now counts 62.5:1 and then resets itself to Word 1 as shown in (figure 9) (sheet 3) instead of counting 64:1. The five "1's" in the serial pulse width modulated Time Code train are detected and also reset the 62.5:1 word counter once every second. If the Time Code input is operating properly, the programmer will be externally synchronized and the Time Code will be correctly placed in the output format. If Time Code is lost, the programmer will still operate at 62.5 words per second

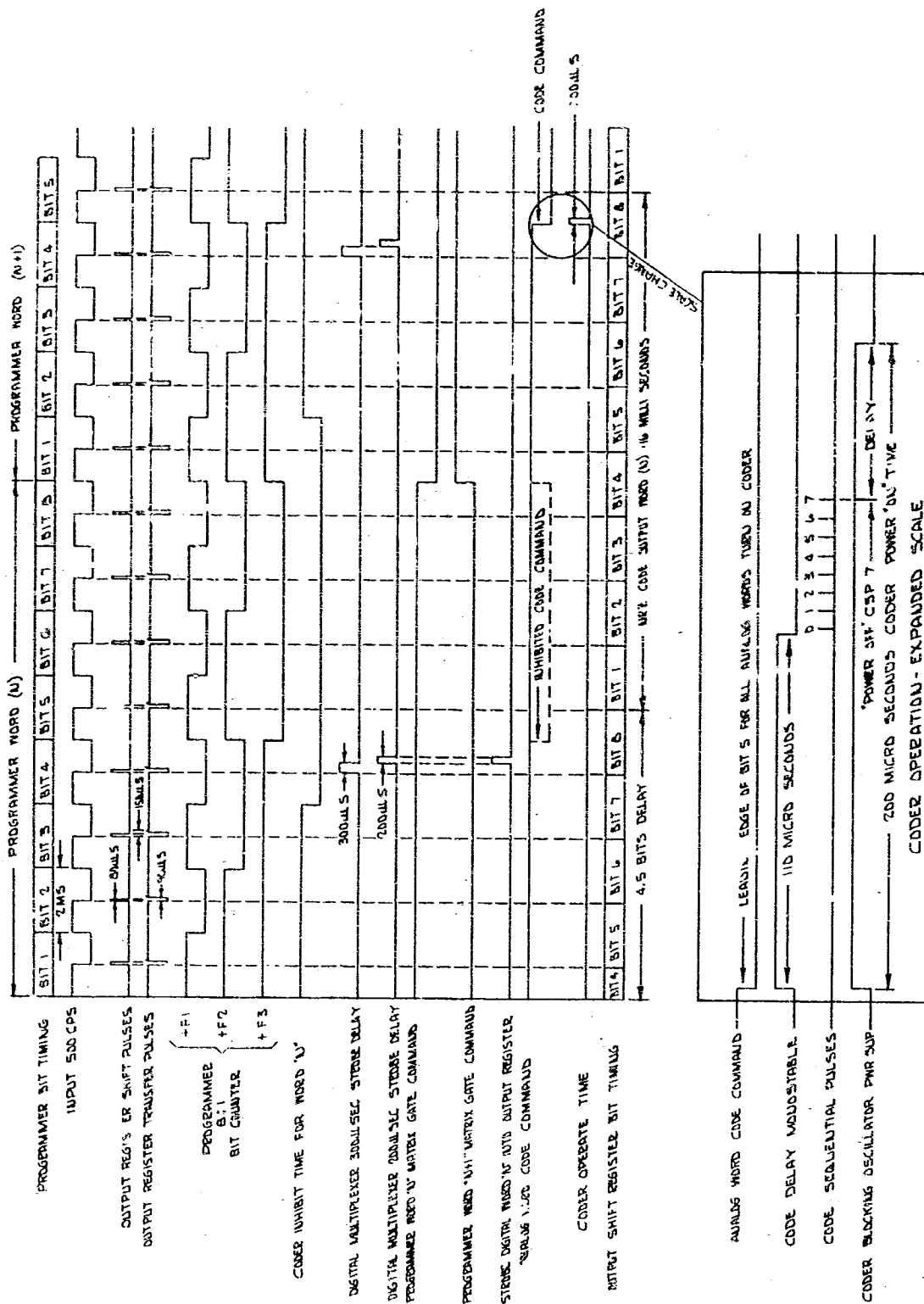


Figure 9. Programmer Timing Diagram (Sheet 2 of 3)

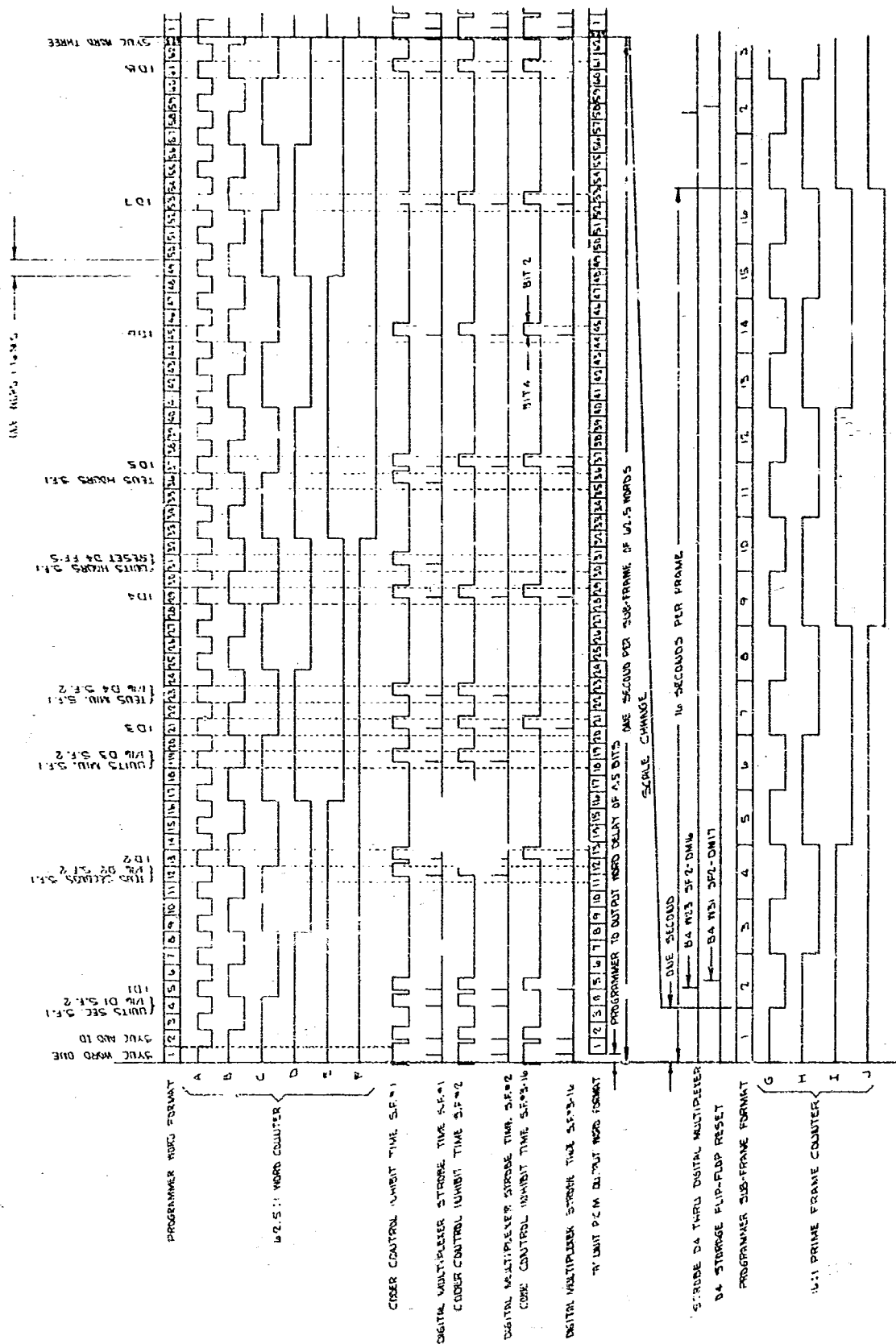
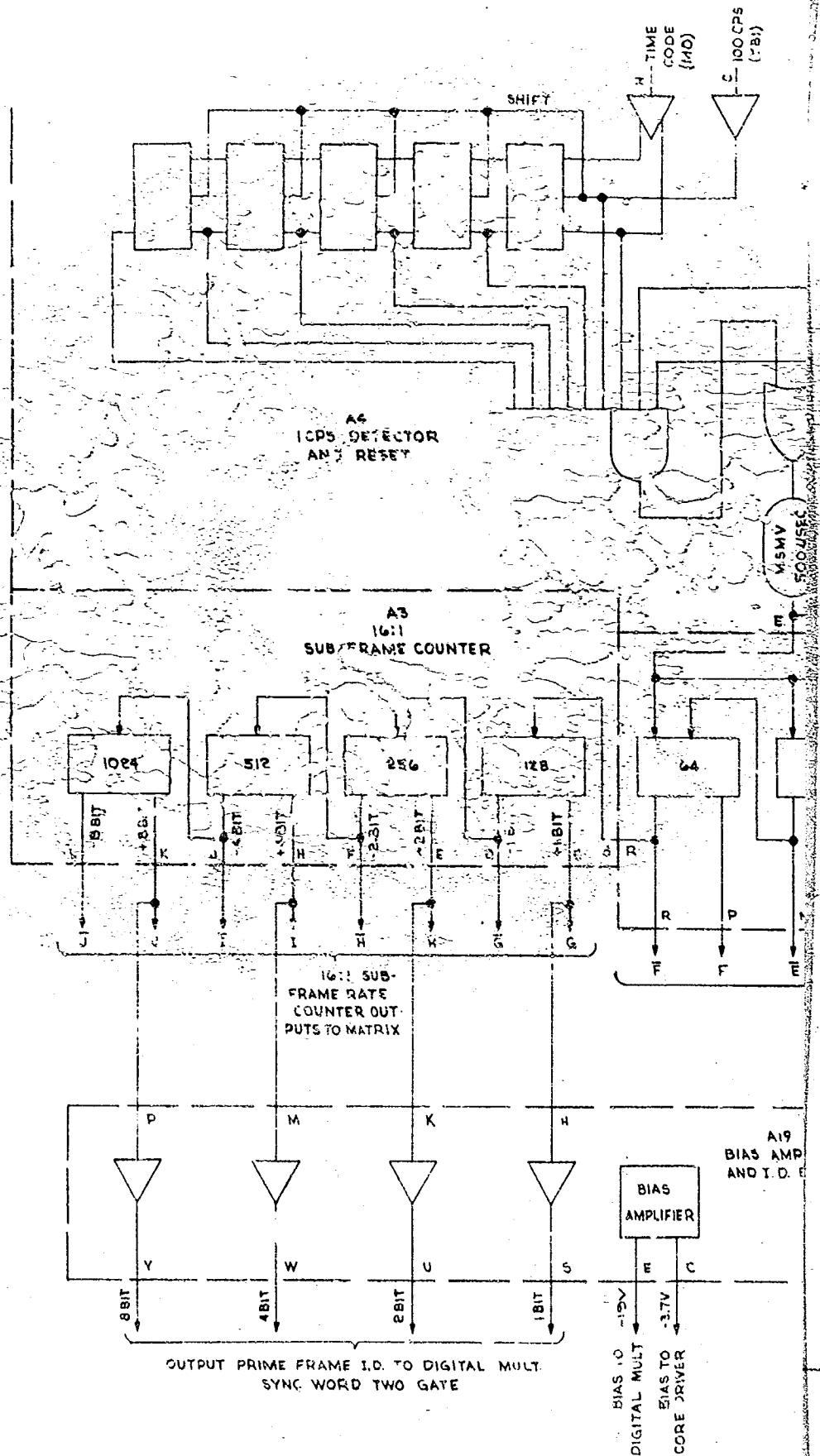


Figure 9. Programmer Timing Diagram (Sheet 3 of 3)

per subframe, but the Time Code appearing in the output format will be either all "0's" or will consist of random "1's" and "0's" depending upon the mode of failure. Both the word counter and the subframe 16:1 counter are connected to diode matrices to generate the proper output commands for each of the input digital words, Time Code words, and sync words. These matrices will produce the digital time slots out of the total frame length of 63×16 or 1008 total time slots. To reduce the total power required by these commands the output matrices do not conduct current until the power strobe appears for 200 microseconds. This pulse applies ground to the output matrix "AND" gates and allows current to flow into the output circuit if all inputs to the "AND" gate are positive. This power strobe is produced by the 8:1 bit counter and the 500 cps bit rate so that the command appears during the second half of bit 8 of all words. Thus, the strobe appears and sets the output register just after the eight bit of the preceding word has been read out and just before reading out bit one of the next word. Since the coder is not used for digital transfer, the coder is automatically inhibited during digital gating. The inhibit circuit word rate output is connected to Unit A and B relay so that the new digital circuits will operate properly with either Unit A or Unit B coder. Using this method, more reliability is achieved by preventing intermix of analog and digital data. In addition, the total average power is minimized.

1.6.2.3 The storage bistables for the seven bits, necessary for the 250 millisecond transient data are reset by the subcommutated word matrix every 16 seconds. The 7 bits of data appear in word 23 (time slot 86) of Subframe 2 and then the storage is reset during the time of word 31. If the readout command occurs just prior to the set data from the inputs, the data will not be lost upon resetting the storage flip-flops because after the reset command occurs there still remains a minimum of 120 milliseconds of set data time. Therefore, no data will be lost since the SET commands are approximately twice the width of time that separates the readout command and reset command. Also it is possible that a "one" bit can be read out in two successive samples because of this overlap if the set command occurs just prior to readout and overlaps the reset command. The normal output data from these flip-flops will be zeros except for a "1" bit (2 maximum) for every input transition which may occur only once per day. Level changing amplifiers were added between the 16:1 Subframe counter and the subframe identification inputs to the digital multiplexer. This was required because the input voltage levels of the digital multiplexer for logic "0" and "1" are zero volts and minus five volts while the counters are -24 volts and -12 volts for corresponding "0" and "1" logic.

1.6.2.4 Figures 10, 11 and 12 illustrate the logic involved in the programmer. The 8:1 bit counter was slightly modified so that all outputs of the three flip-flops are now available for external matrix timing. The input 500 cps bit rate signal, the inversion of the 500 cps is used to generate the



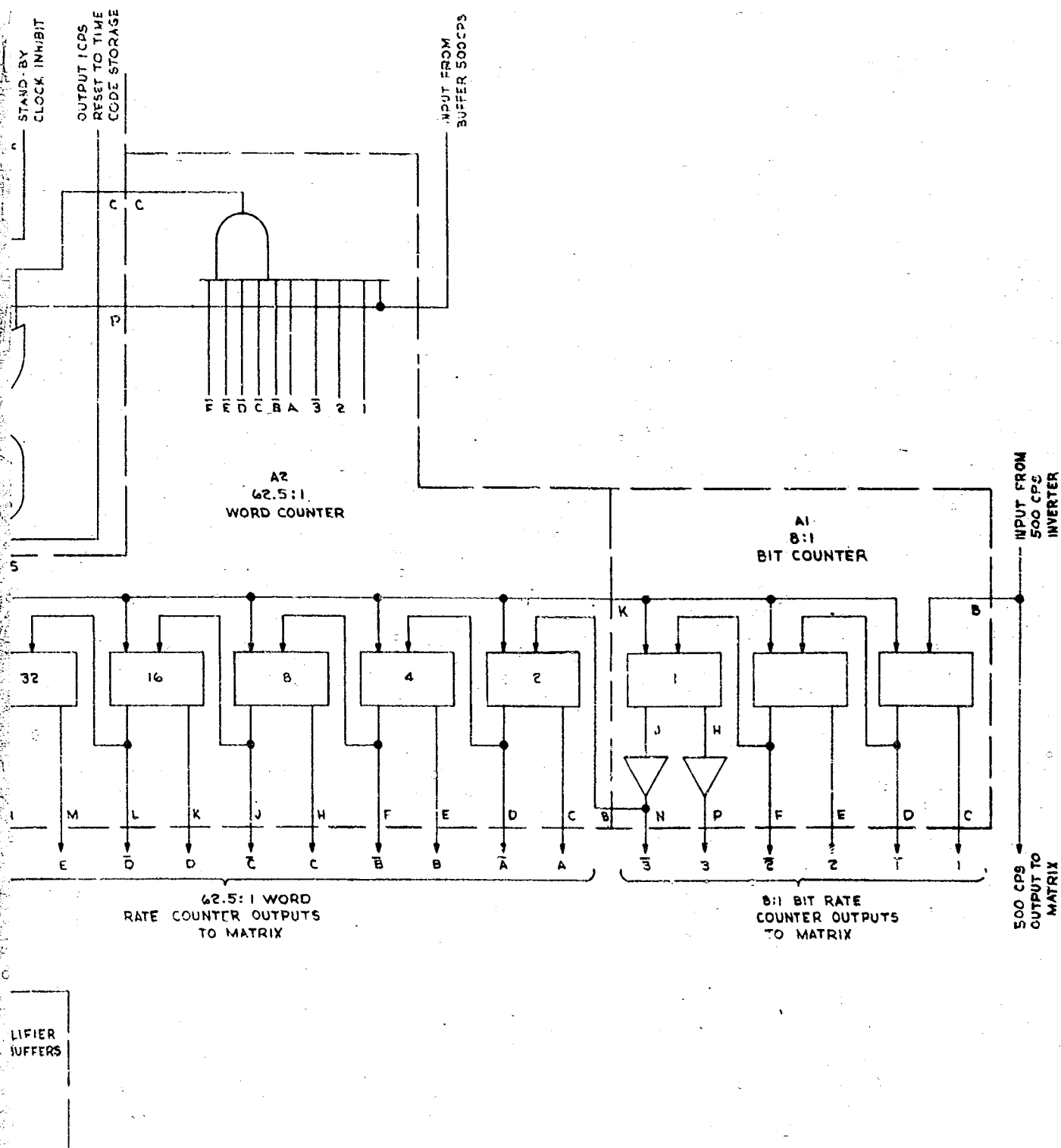


Figure 10. Programmer Counters Logic Diagram



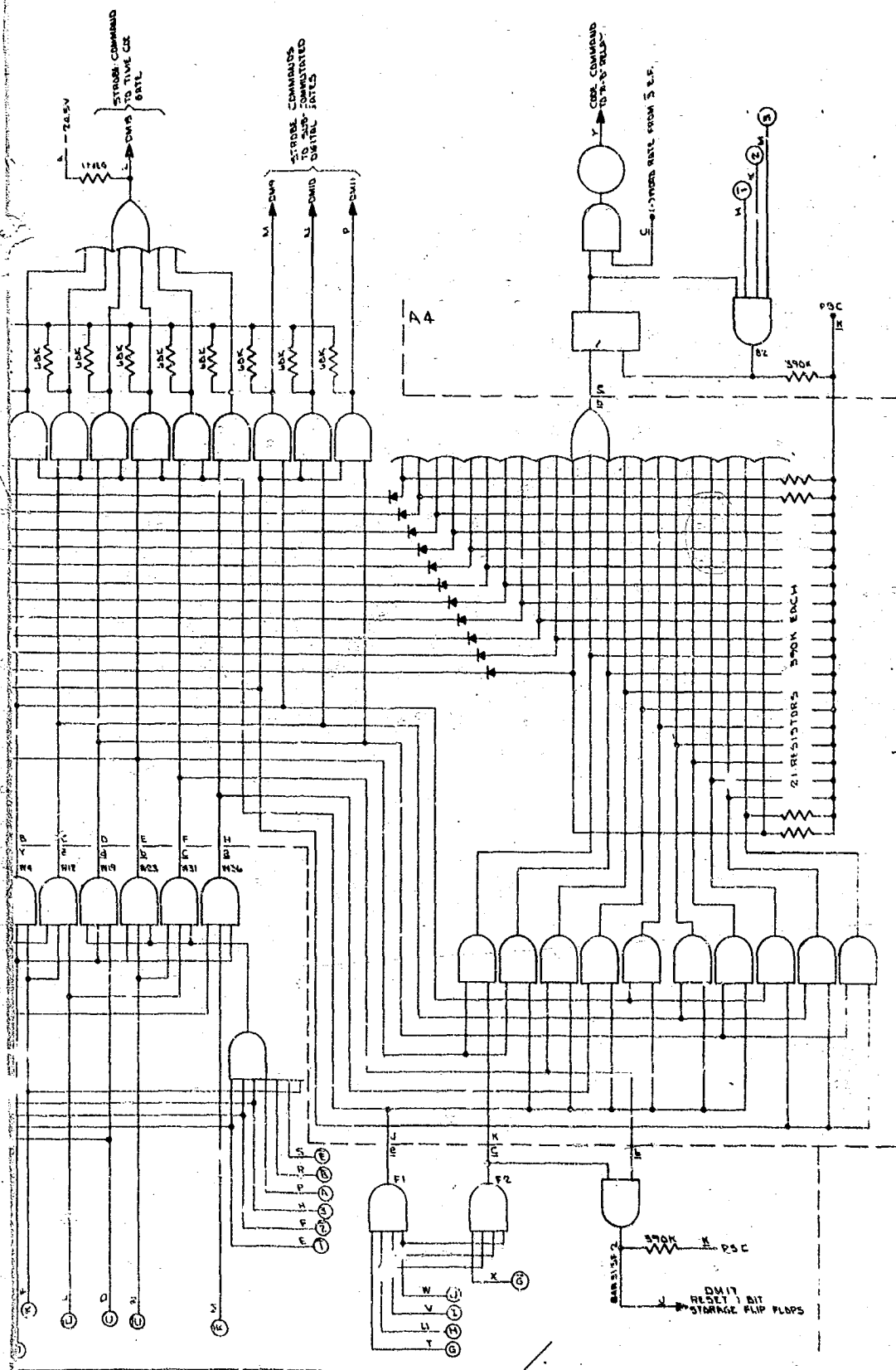


Figure 11. Programmer Command Matrix Logic Diagram

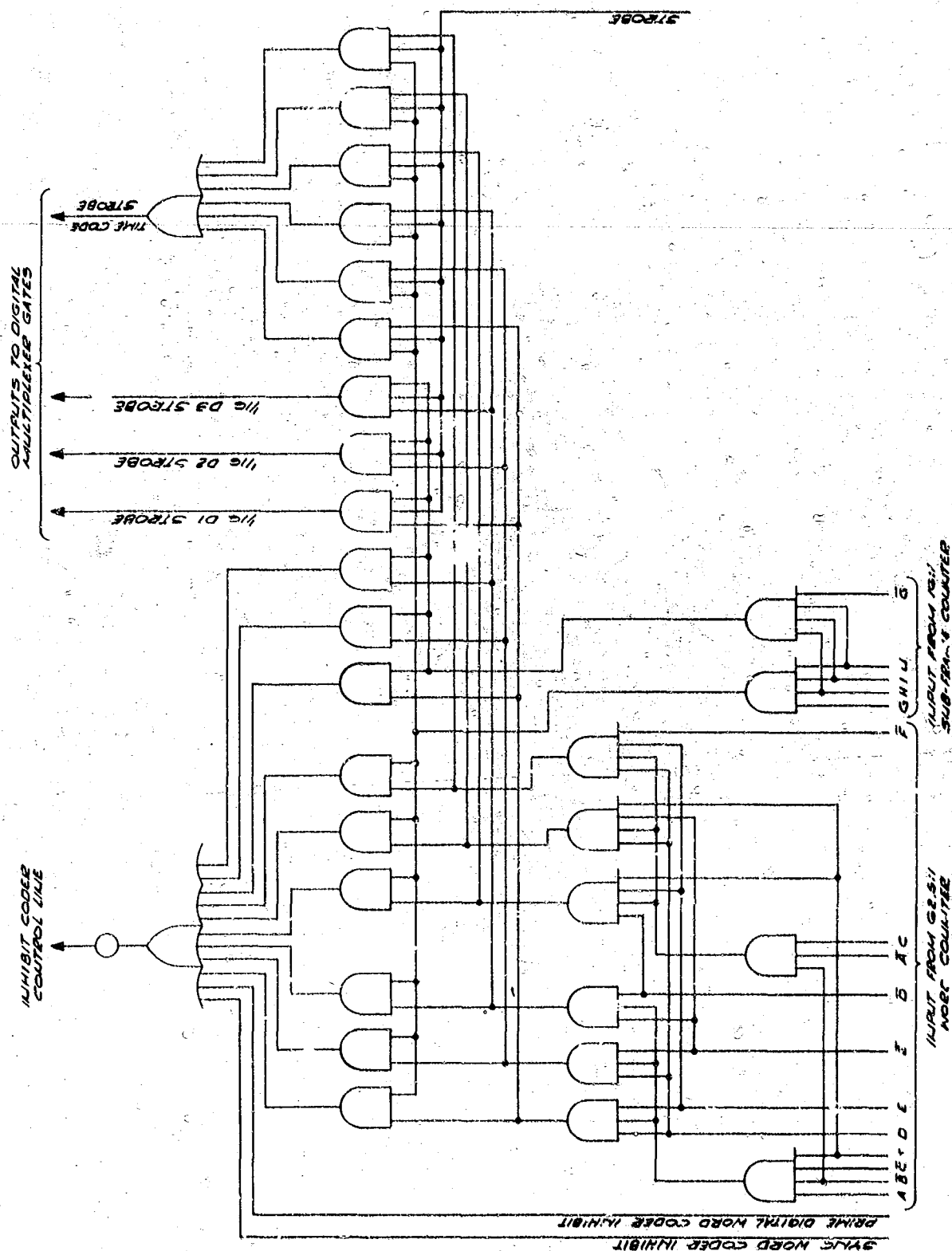


Figure 12. Programmer Time Code and Subcommutated Digital Word Matrix

output register shift and transfer commands. The timing of these commands with respect to the programmer bit times is shown in figure 9.

Since the counter and the output register operate from negative going transitions, the programmer bits and output bits have a minimum separation of one half bit or one millisecond. The word rate emitter followers are still used to control the analog multiplexer.

- 1.6.2.5 The 64:1 word counter (A2) has been changed to a 62.5:1 word counter by adding a detector type reset gate. This reset gate detects word 63 and then the 500 cps and bit counter inputs produce the first half of bit 5 so that the output from this gate is a one millisecond pulse occurring during the first half of Bit 5, Word 63 (B5W63). Reference to the timing diagram (figure 9) shows this reset pulse after it goes through a 500 microsecond monostable flip-flop. This pulse also resets the 10:1 counter located in the Time Code storage circuits. However, in the event the Time Code is lost, the resetting or synchronizing of the Time Code 10:1 counter by the programmer will result in the loss of Time Code. Thus, the resetting of the 10:1 counter is only necessary when the Time Code 5 "ones" are detected to produce the external 1 cps reset for the 62.5:1 word counter at which time the 10:1 counter must be synchronous with the programmer and Time Code. The method of detecting the 5 Time Code "ones" to produce a 1 cps reset was selected because it is independent of the 10 cps and 1 cps clock pulses which are phased differently in the Nimbus "C" Clock, from

what they were in the Nimbus "A" Clock. Thus, the PCM can be used with either the Nimbus "A" Clock or the Nimbus "C" Clock because the only signals that must maintain close phasing are the 500 cps, 100 cps, and Time Code, and these signals are coherent in both clocks.

- 1.6.2.6 The 16:1 subframe counter (A3) operates the same way as in the present system except that both phases of all four flip-flops are now connected to external pins on the modules. The output plus sides are connected to the level changing identification buffer amplifier (A19) so that a "1" level changes from -22V to -19 volts and a "0" level changes from -12V to 0 volts. With the connections shown in figure 10, all counter outputs are plus (-12 volt level) so that all outputs from the buffers are plus (0 volt level) and binary 0000 is read out as the identification subframe count.
- 1.6.2.7 Figure 10 also shows the 5 stage shift register (A4) that will store the 5 sequential Time Code "ones" when they appear in the code train. The outputs of these 5 flip-flops are connected to an "AND" gate along with Time Code inverted, 500 cps, and 100 cps $\phi 2$ to produce the reset pulse shown in figure 9. This reset pulse is also coupled to the 500 microsecond monostable and resets both the 62.5:1 word counter and the 10:1 Time Code counter, so that the PCM becomes synchronous with the Time Code train.
- 1.6.2.8 The bias amplifier (A19) shown develops -19 volts and -4 volts so that the programmer can control the output register and digital multiplexer. Since

there are several diode gate energy gaps separating the counter flip-flops from the digital multiplexer gate driver and since the input digital gates have a "0" level that may range from 0 to -1V, and since the power supply contains only 0V and -24.5 volts, the bias amplifier was added so that proper control of "turn-off" can be maintained by the counters. The -19 volts provides the emitter return for the digital multiplexer gate driver such that -22 volts from the counters will hold the gate "off". The -4 volts provides the emitter return for the output register core driver. An input data logical "0" (0 to -1 volt) will hold the driver in the "off" state.

- 1.6.2.9 The entire programmer matrix (figure 11), shows all of the digital multiplexer bilevel gate commands, Time Code gate command, sync word gate commands, the reset command to the 7 bit digital pulse data storage register and the code command to the Unit A and B coder relay. The breadboard card A9 contains the 500 cps inverter and the digital multiplexer power strobe generator. The 500 cps inverter is used to trigger the counter stage so that the counter changes in state occur during the positive transition of the input 500 cps clock (CY 500). Thus, all the counters are completely through changing state before the output shift register shifts and transfer commands occur. For general information, the coder operation is also shown on an expanded scale. The programmer timing with respect to the output shift register timing shows a 4.5 bit delay with all of the digital words being strobed into the output register during the time of programmer

bit 4, and with all of the analog words being set into the output register at the beginning of the programmer bit 5.

1.6.2.10 Breadboard card A5 contains the gates that generate the three sync word strobe commands for words 1, 2 and 62.5. These three commands, called DM12, 13 and 14 respectively, are directly connected to the digital multiplexer gate driver transistors. Because the coder must be inhibited during digital words, the first operation is to gate out the digital word times first which are used to inhibit the coder and are also connected to the output gates. The output strobe switch applies power supply common to the output gates 68 K resistors during the last half of bit 4 of words 1, 2 and 62.5. When the resistors are returned to power supply common by the power switch, and when the inputs to the diodes are in their upper level, the resistors will allow current to flow into the digital multiplexer driver transistors bases, allowing them to turn on for 200 usec. Thus, the digital multiplexer duty cycle is on for 200 microseconds and off for 16 milliseconds giving a minimum power reduction of 80:1. The exact power ratios can be determined over a subframe or over prime frame by referring to the timing diagram (figure 9). The digital commands are shown for subframes 1, 2 and 3 through 16 giving an "ON/OFF ratio of:

$17 \times 200/10^6$ or 294:1 for subframe 1,
 $15 \times 200/10^6$ or 333:1 for subframe 2,
 $11 \times 200/10^6$ or 454:1 for subframes 3 through 16.

Thus, the total power reduction ratio averaged over 16 complete frames is 16×10^6 or 432:1. This means that averaged out over a period of time the entire digital multiplexer dissipates 1/432 of the peak power dissipated by any digital gate.

1.6.2.11 Breadboard card A6 contains the gates that generate the eight prime digital word strobe commands for words 5, 13, 21, 29, 37, 45, 53, and 62 of every subframe. These word commands are also gated out first to inhibit the coder and then to allow the 200 usec power strobe to turn on the digital gate during the time the sync word commands, which is at the rate of one sample per second. The eight digital words are referred to as 1D1 through 1D8 and are shown along with the other digital words (figure 9). The strobe commands to the digital multiplexer gates are called DM1 through DM8.

1.6.2.12 Breadboard card A7 contains the gates which generate six word time slots 4, 12, 19, 23, 31, and 36 used for the Time Code and subcommutated digital channels. To simplify the programmer and to make it more flexible, the six time slots used in subframe 1 for the Time Code can be used in subframes 2 through 16 to generate subcommutated digital channels, each channel having 7 digital data inputs. Only the output gates must be added to increase the subcommutated digital channel capability. The six time slots in subframes 2 through 16 can therefore be used to generate commands for 6×15 or 90 subcommutated digital words. In the PCM Study System,

only four subcommutated digital words are provided. They are readout as words 4, 12, 19 and 23 of subframe 2. With this method two more digital words can be added by adding two more digital multiplexer gate circuits and by adding 10 diodes and 4 resistors to the programmer. In addition, since the subframe is also necessary to generate the commands, every group of 6 subcommutated digital words added will also add four more diodes to generate the subframe command. Also on this card is the two millisecond reset command for the seven bit storage register used for the seven pulsed digital inputs. This reset occurs at B4W31 SF 2 and the command is called DM 17. This reset command and the set command, DM 16 are both shown on the timing diagram (figure 9).

- 1.6.2.13 Breadboard card A8 contains all of the output subcommutated digital word commands (three subcommutated bilevel words, one subcommutated pulsed digital word, and one command line for all six Time Code words) plus the inhibit command to the coder gating flip-flop. The subcommutated digital gates operate the same as the prime digital gates and the sync word gates except they are also gated with the proper subframe count which reduces the sampling rate to one sample every 16 seconds. The twenty input "OR" gate shown has separate diode "AND" gates on all of its input lines. Thus, the Time Code slots show 10 each 2 input "AND'S" and the sync and prime digital word time slots show isolating diodes, so that the coder inhibit "OR" gate will be isolated from the Time Code "OR" gate and from the

digital word commands. Using this type of coder inhibit circuit permits the programmer digital word capability to be increased or decreased without affecting the circuit design.

1.6.2.14 Breadboard card A4 contains the coder inhibit flip-flop that is used to inhibit the word rate square wave command to the "A-B" coder relay. The coder operates on the negative going transition of the word rate. Should an inhibit occur, the entire negative alternation of the word rate square wave is removed so that the output to the relay remains in the upper level during all digital word times. Figure 9 shows the coder inhibit times for all 62.5 words in all 16 subframes. The timing for subframes 1, 2, and 3 are different from each other as shown. Subframes 4 through 16 are timed the same as subframe 3.

1.6.3 Digital Multiplexer Logic. - The block diagram (figure 13) shows a total of 16 digital gate circuits. Logically these are identical except that the 16th gate is preceded by a seven bit storage register. Eight gates are used for prime digital words, three for subcommutated bilevel digital words, one for a subcommutated pulse digital word, three for sync words, and one gate for the Time Code. Each bit is binary weighted in conformance with the output register format with "OR" gating using isolation diode coupling. The logic diagram (figure 14) makes this self-evident. Negative true logic is used with the inputs accepting a 0 to -1 volt range for logic "0" and -5 to -24 volt range for logic "1". The function of the 16th gate is not readily apparent. These circuits sample 250 millisecond nominal transient input data pulses which normally occur in a non-synchronous manner at a rate of up to

NOTES:

ONLY FOUR BITS OF TIME CODE ARE USED,
THE REMAINING THREE BITS ARE ZEROS

INPUT DATA FROM TRANSDUCERS AND COMMANDS FROM PROGRAMMER

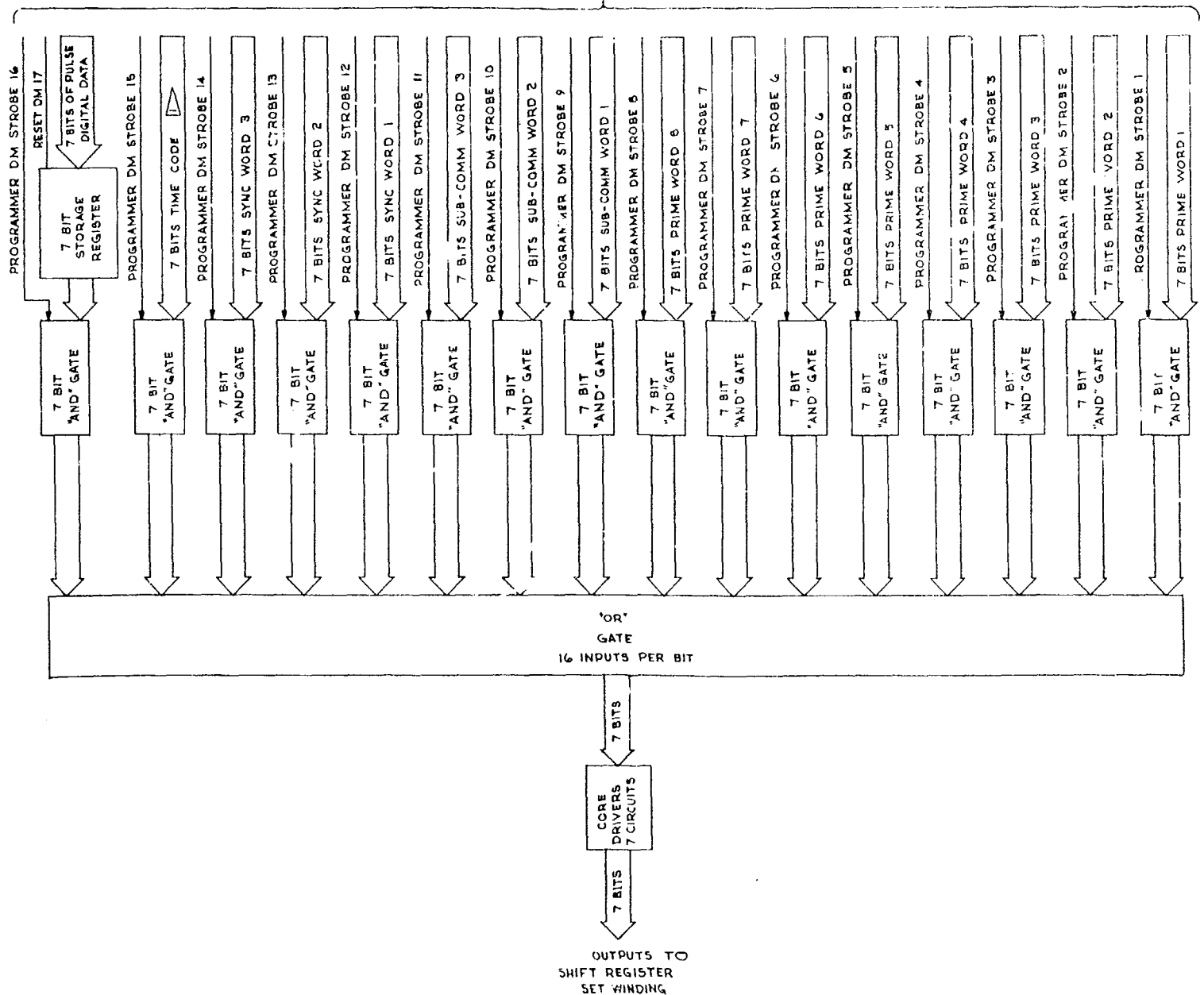
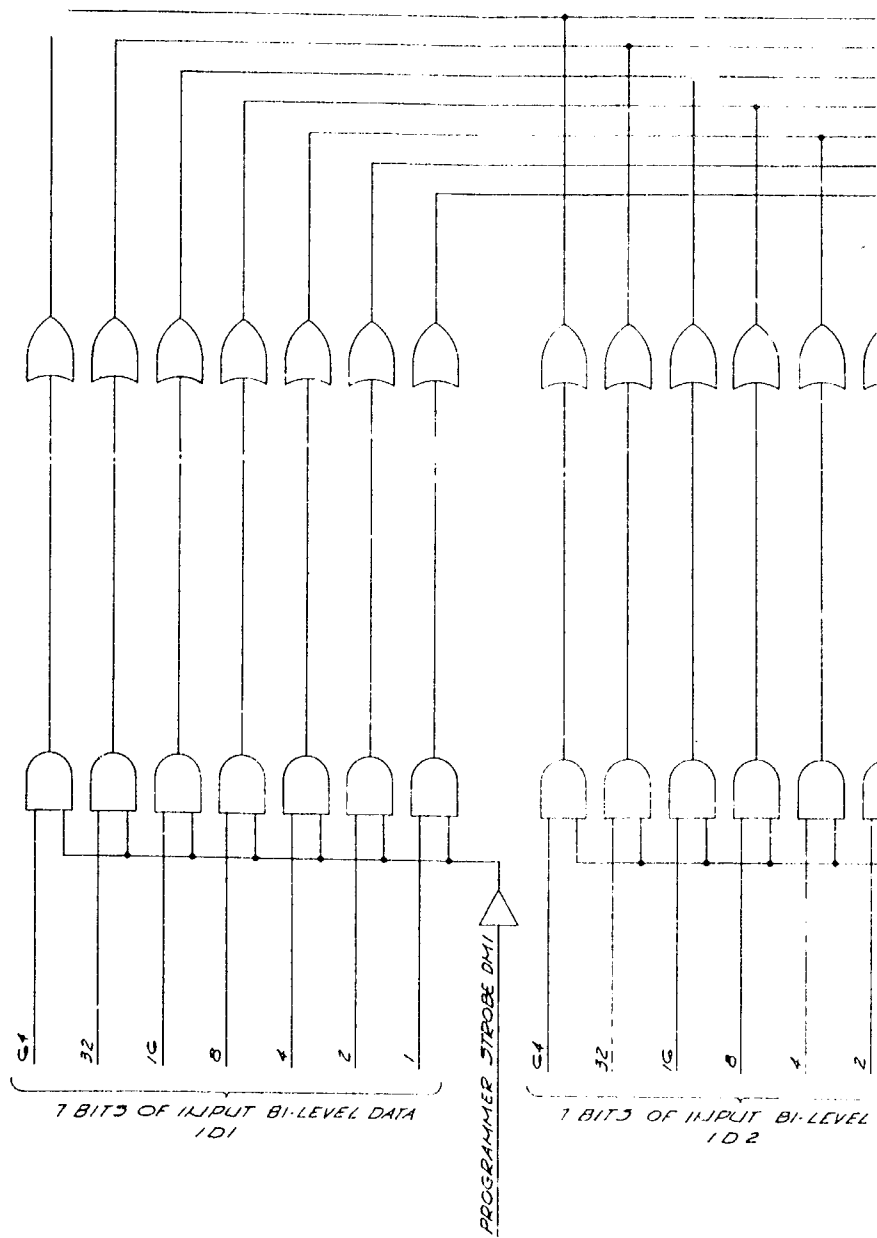


Figure 13. Digital Multiplexer Gates Block Diagram



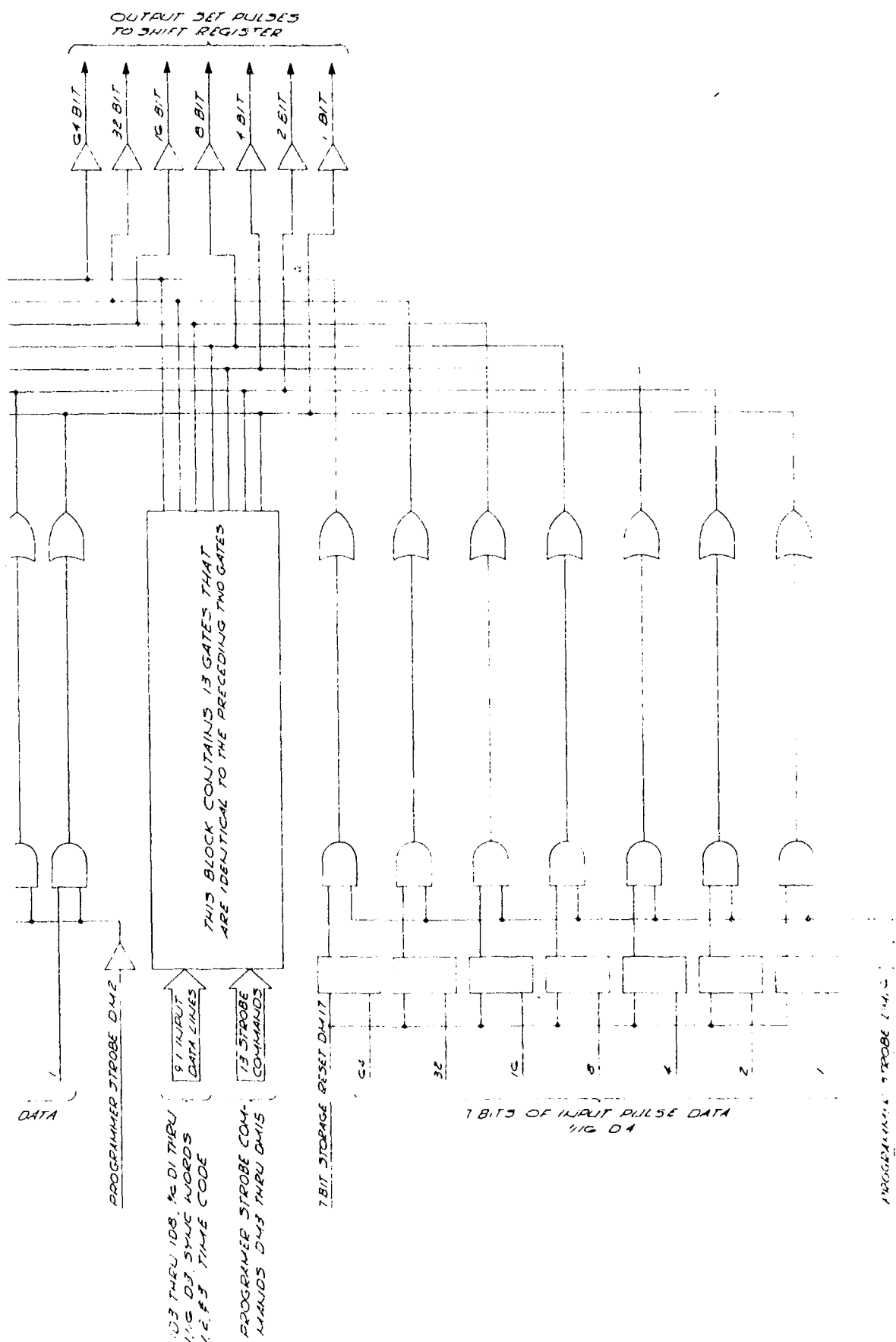


Figure 14. Digital Multiplexer Logic Diagram

one pulse per day. These pulses are stored and shifted out at the frame rate. The power strobe which acts as the enable for each AND gate is of 200 μ sec time duration effectively turns on the power for the digital multiplexer. In the absence of a power strobe there is no power dissipated (see paragraph 1.6.2.10 for mathematical analysis). The output of all gates are OR gated. To prevent crosstalk, or maintain channel isolation, into the seven core drivers, only one gate can be turned on during a time interval.

1.6.3.1. The A and B coders are each connected directly to its respective output shift register SET windings which are identical to the digital multiplexer SET windings. The output shift register operates as a three input OR gate, but only one input can be applied at any one time. The two coders are presently interlocked with relays in such a manner that only one coder will operate at any one time with Unit A multiplexer.

1.6.3.2 The coders in the Study System are now electronically interlocked with the digital multiplexer also. Word counts from the word counters are continuously monitored. Should the next time slot in the output format be a digital word, it is detected by the programmer, and the coder is inhibited. (All digital operations are performed during the time of bit 4 of that word). The detected digital word turns on the coder inhibit circuit at the beginning of bit 4 so that the negative edge of the word rate, which occurs at the beginning of bit 5, will be inhibited to prevent the coder from turning on. The complete prime frame waveforms for the coder inhibit circuits are shown

in figure 9. The digital multiplexer strobe pulses shown occur approximately 1.3 milliseconds after the coder is inhibited. The actual logical command sequence is as follows:

- a. The shift register reads out bit 8 of the preceeding word - analog or digital (except for word 62.5).
- b. The digital word is detected in the programmer matrix and turns on the coder inhibit flip-flop.
- c. The digital word is strobed through the digital multiplexer into the output register.
- d. The coder command does not occur because of the inhibit flip-flop.
- e. The next shift pulse occurs to read out bit 1 of the seven bit digital word stored in the output register.

i.6.4 Digital Multiplexer Detailed Analysis. - The schematic diagram (figure 15) represent the circuit properly only if it is fabricated with discrete components. The digital multiplexer in the Study System initially contained this type of circuit. All of the diodes are 1N916s, the resistors are $27K \pm 5\%$ and the transistors are 2N918s. The component values very nearly approximate their equivalent counter parts in the micro-integrated circuit gate, as the 27K resistors minus 10% for tolerance, temperature, and aging is 24.3K and the integrated circuit 30K (resistor values have since been increased to 45K) resistors minus 20% for tolerance, temperature, and aging is 24K. These low values simulate the worst case conditions at the lowest temperature extreme of $-10^{\circ}C$, as they require a maximum current when the transistor h_{FE} is at its

- NOTES
1. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE 47K, 2.5% TOL, 1/4W.
 2. UNLESS OTHERWISE SPECIFIED, ALL DIODES ARE 100G13, ALL TRANSISTORS ARE 100B18.
 3. PARTIAL REF DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION PREFIX WITH UNIT NO. OR SUBASSY DESIGNATION.

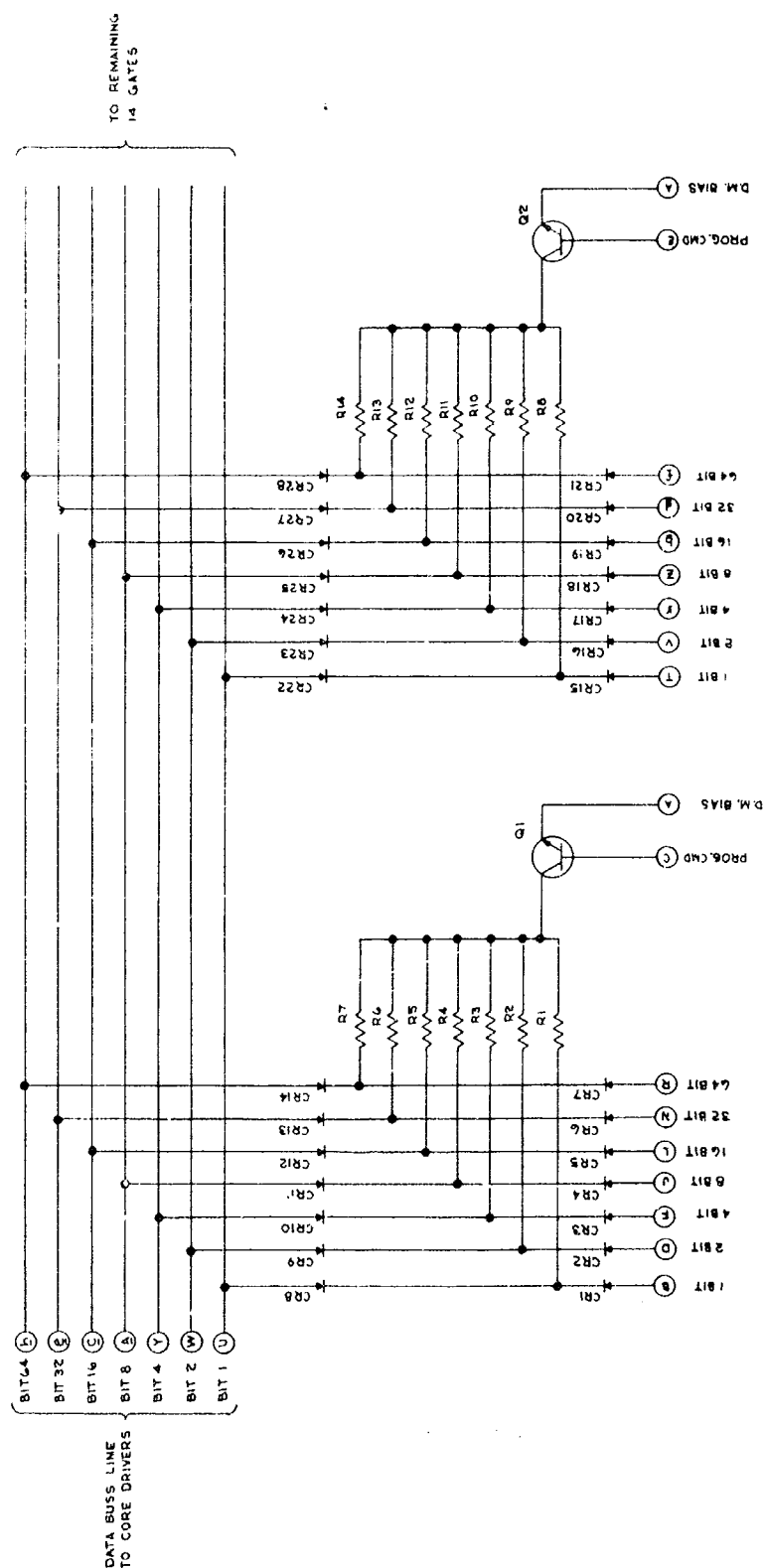


Figure 15. Digital Multiplexer Gates A10 through A17 Schematic Diagram

minimum. Thus, with these conditions the programmer matrix power strobe resistors must pass maximum base current to Q1. The value of the strobe resistor is 68K, which assumes the resistor can increase by 10% to 74.8K and still pass enough base current to properly operate the digital word gate.

1.6.4.1 The detailed interface schematic diagram of one bit of the digital word gate is shown in (figure 16). This circuit shows an assumed impedance of 1K for either a logical "0" or a logical "1", and this input 1K resistance is applied by a $V_{CE\text{SAT}}$ energy gap of a PNP (Q1) for a "0" and an NPN (Q2) for a "1". The output core driver interface shows a grounded resistor (R3) and a PNP (Q3) emitter returned to -3.6V bias, which will allow current to flow through R3 until the voltage developed across it exceeds -4.3V which will turn on the transistor. The programmer transistors Q4 and Q5 represent the circuits that turn on the gate driver transistor Q6. As shown on the drawing when current flows through Q4, R5, 3 diodes, and Q5 to -22 volts, which holds Q6 off as there is one volt reverse bias across the base-emitter junction. When Q5 turns off, the current from Q4 will flow through R5 and into the base of Q6 which turns Q6 on and clamps the base junction to -18.3 volts. Q4 is held on by the power strobe command for 200 microseconds.

1.6.4.2 All of the voltages and currents shown in figure 16 reflect normal conditions where the resistor values are exact, diode $V_{fD} = 0.6$ volts, transistor $V_{BE\text{SAT}} = 0.7$ volts and transistor $V_{CE\text{SAT}} = 0.2$ volts. These are

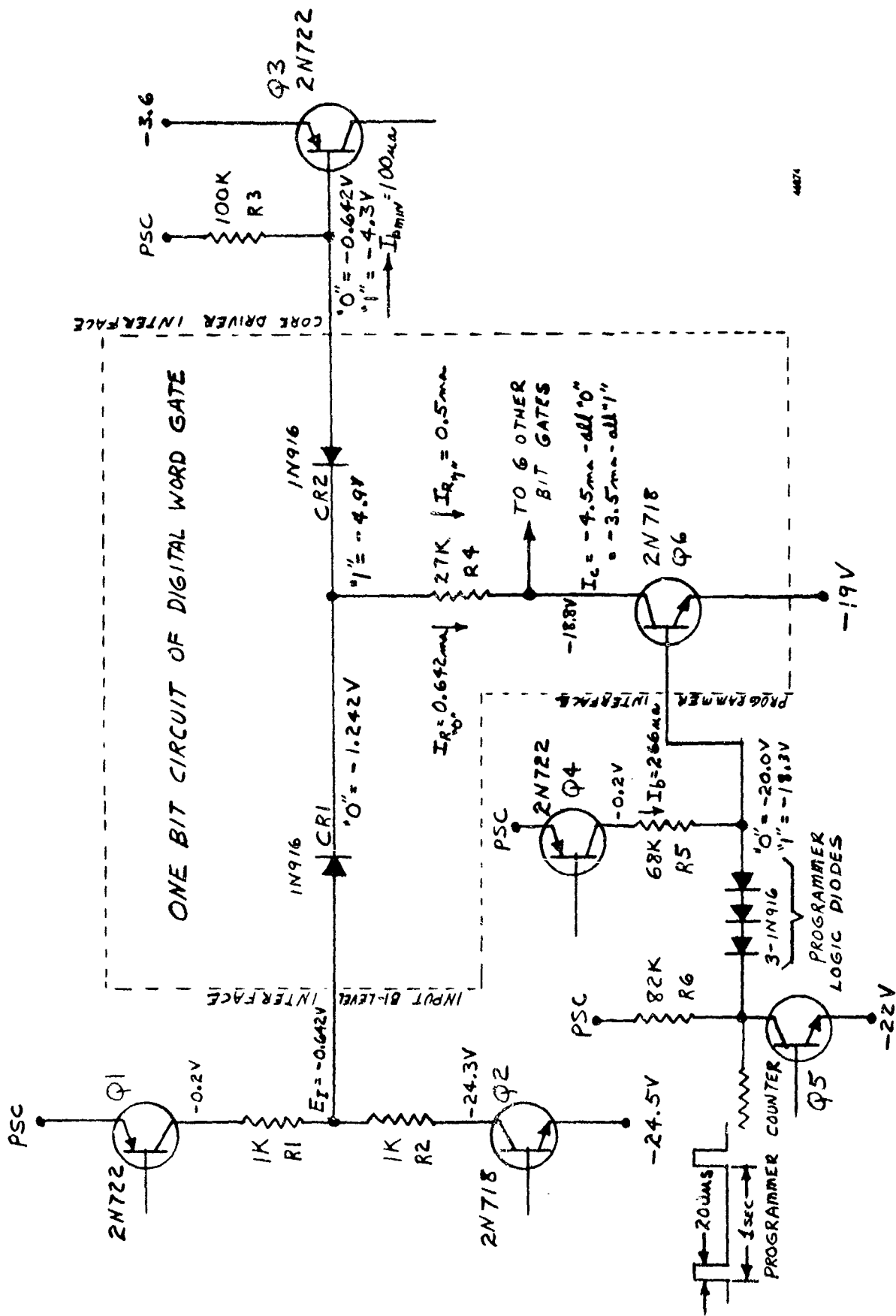


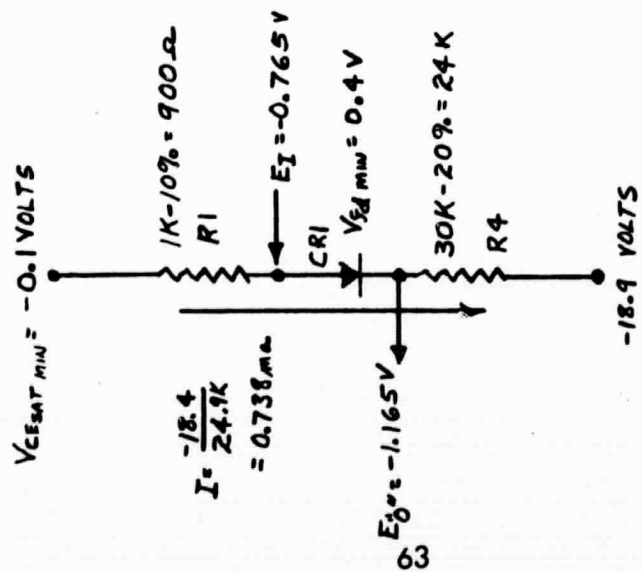
Figure 16. A One Bit Interface Schematic Diagram

the same semiconductor values as the ones listed in the circuit design section of this report. The -24.5 volts shown is the battery voltage, the -22 volts shown is the PCM system voltage at the output of the line filter. The -19 volts and -3.6 volts comes from the digital multiplexer bias amplifier circuit.

- 1.6.4.3 The maximum current flows through Q6 when the maximum voltage is developed across the seven R4's in parallel; all seven R's and R1's have minimum resistance; all 7 diode V_{fd} 's (CR1) are minimum; and when $V_{CE\text{SAT}}$ is minimum for Q6 and all seven Q1's. Figure 17A shows these parameters which cause a maximum Q6 collector current. The input voltage at the system data interface is -0.765V and the required maximum current from the programmer is $I_{C/B}$ or $5.17/20 = 259$ microamps. However, if the programmer 68K resistor increases 10% to 74.8K and if Q6 $V_{BE\text{SAT}}$ increases to 0.9V, the maximum current 240 microamps which requires a Q6 current gain of $5.17/0.24 = 21.6$. Since all of these factors will not occur simultaneously, this circuit will work properly down to -10°C, at which time the drive becomes marginal if all of the discussed parameters approach their worst case value. The 68K resistors were not decreased to the next lowest resistor value of 62K, because of the additional loading placed on the counter flip-flops. The counters would have to be redesigned to increase their load capability and the power increase of one stage would be multiplied by the total number of stages (13), which

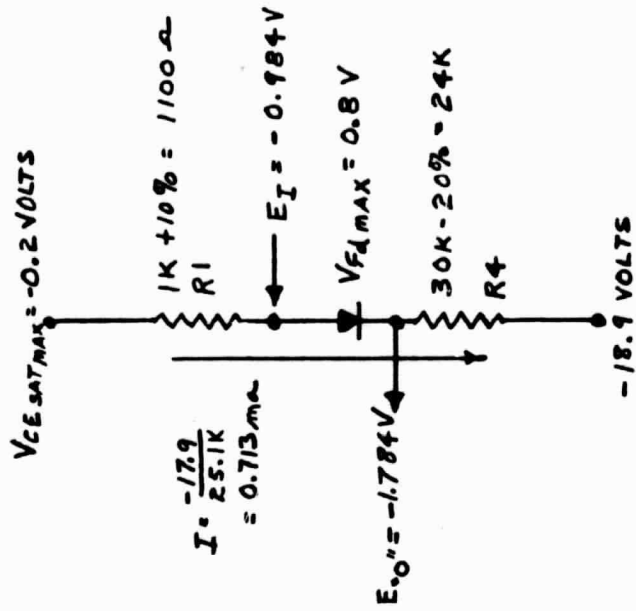
of course, is not necessary as the -10°C margin is 35°C below the normal environmental temperature, and 5°C below the specified minimum.

- 1.6.4.4 The maximum allowable interface input voltage for a logical zero is shown in figure 17B. This value occurs when the input transistor $V_{\text{CE SAT}}$, input resistor $R1$, and input diode V_{fd} are maximums and when the gate resistor $R4$ and gate transistor $V_{\text{CE SAT}}$ are minimums. Thus, the voltage developed by the divider at the interface is -0.984 volts which resulted in the 0 to -1 volt specification with 1K source impedance.
- 1.6.4.5 The maximum source impedance that can be used reliably is calculated as shown in (figure 18). The core driver bias is adjusted to -3.6 ± 0.5 volts which gives the minimum -3.1 volts shown. If the $V_{\text{BE SAT}}$ minimum 0.5V then the base emitter junction forward bias point borderline is -3.6 volts, and if V_{fd} of CR2 is 0.4 volts, then the internal gate voltage at the junction of CR1 , CR2 , and $R4$ is -4.0 volts. Since a known voltage is across $R4$, the current is established as -0.62 ma. Also since the voltage of CR1 is a maximum of 0.8V , the voltage across $R1$ is known and since the current is known, $R1$ is calculated as a maximum of 4.3K . This value for $R1$ is not 100% correct as calculated because all of the assumptions are not exactly 100% correct and all of the conditions will probably not occur at the same time. 4.3K would probably work sufficiently well with discrete component digital gates, but could present problems if used with the integrated circuit digital gates unless the values of $R1$ through $R7$ are increased.



THUS $I_{C MAX Q6} = 7 \times 0.738 \text{ mA}$
 $= 5.17 \text{ mA}$

(A) TO DETERMINE $I_{C MAX Q6}$



(B) TO DETERMINE $E_{I MAX}$ FOR LOGICAL "0"

Figure 17. Equivalent Circuits Worst Case

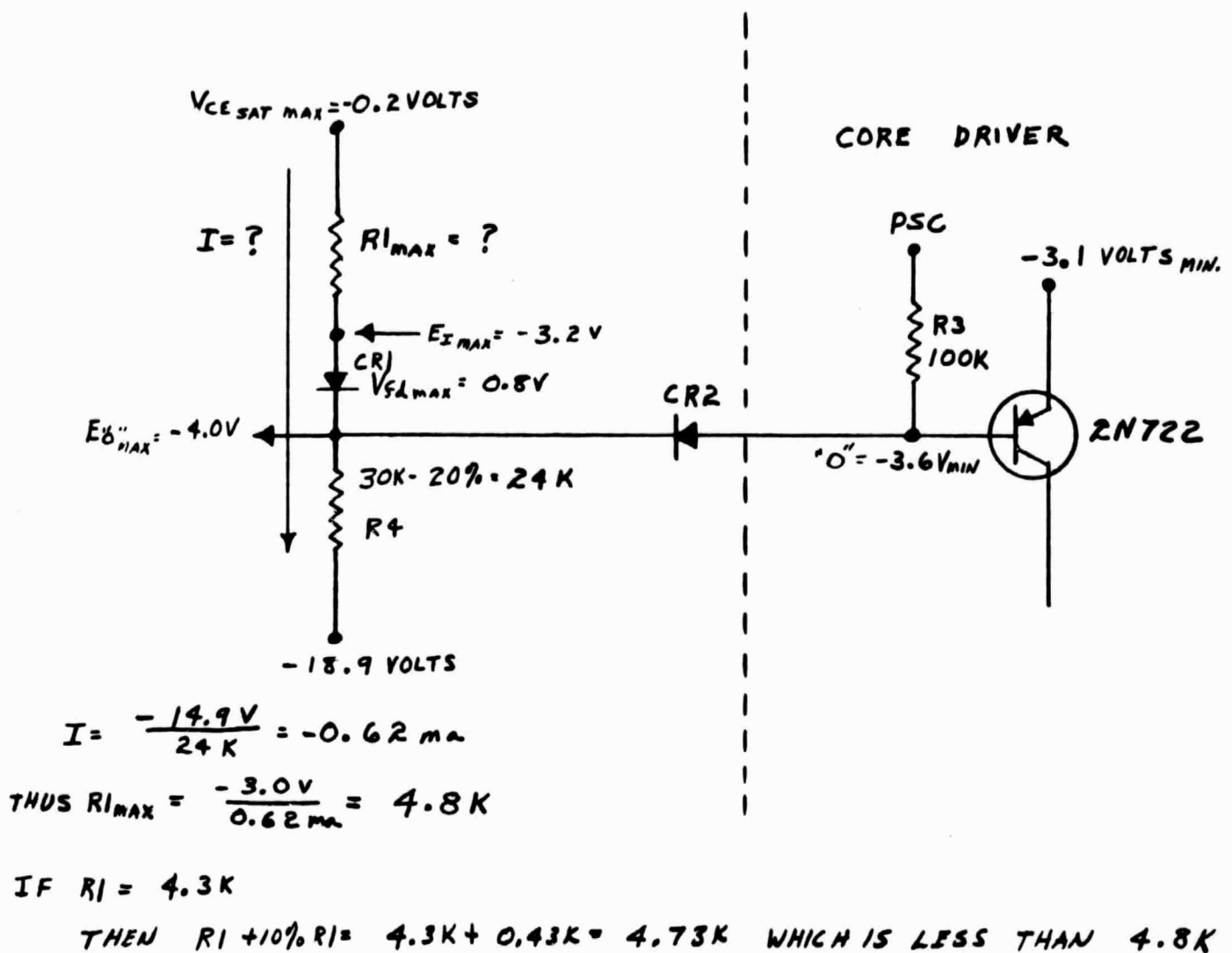


Figure 18. Equivalent Circuit for Maximum Interface Voltage for "0"

1.6.5 Microelectronic Digital Word Gate. - There are 16 digital multiplexer word gates as shown by the block diagram of figure 13. The Nimbus PCM Study Program provides all 16 of these gates in the new micro-package integrated circuit design concept. Since each small flat-pack only contains 14 leads and one complete digital word gate requires 16 leads, only one-half of a digital gate is placed in each package. Thus, the PCM Study System will contain 16 digital word gates contained inside 32 micro flat-packs with each flat-pack measuring 0.125 x 0.25 x 0.035 inches. The integrated circuit digital multiplexer operates exactly like its discrete component equivalent, except the circuit design specifications and equivalent circuits are different. In the integrated circuit digital gate stray capacities and parasitic elements are no longer negligible, and some new parasitics are generated which do not exist with discrete components. Since this generally degrades circuit operation, work is progressing to eliminate these parasitics from the fabricated circuit chips. Presently the greatest disadvantage of the micro circuit techniques (with respect to the Nimbus Study digital gate) is the inability to fabricate seven high resistance resistors on one chip along with the necessary 14 diodes and driver transistor. For example, note that the core driver transistor Q3 requires a minimum base current of 100 micro amps. This current could be supplied by a R4 value of $(-18.8V) - (-4.9V) / 0.1 \text{ ma} = 139 \text{ K}$ which means the integrated circuit 30 K resistor is approximately 1/5 the discrete component value. However, it is not practical at this time to make the integrated digital gate resistors much larger than 30 K. Although subsequently the value of the gate resistor has been increased to $45 \text{ K} \pm 10\%$ at 25°C . Work is progressing on increasing the practical value of resistance to 100 K.

1.6.5.1 The following specifications were first written 3 June 1964, corrected at a design review meeting on 12 June 1964 and updated 25 September 1964. See Appendix II for final specifications.

a. Temperature Test Range for Proper Operation of Circuit: -10° to 25°C

b. Transistors - Switching Circuit:

(1) Forward base-collector voltage drop - 0.7V max at 1 ma and 25°C

(2) Forward base-emitter voltage V_{BE} min = 0.16V at 1 ma and 75°C

V_{BE} max = 1.1V at 1 ma and -20°C

(3) Saturated collector-emitter voltage $V_{CE\text{SAT}}$ min = 0.2V at 1 ma and -20°C

$V_{CE\text{SAT}}$ max = 1.0V at 10 ma

and $+75^{\circ}\text{C}$

Leakage current I_{CBO} max = 10 nanoamps at 20V and 25°C

Peak reverse voltage base collector = 40 volts at 25°C

Maximum forward collector current $-I_C$ max = 10 ma at 25°C

Minimum forward collector current $-I_C$ min = 1 ma at 25°C

DC current gain HFE min = 20 at 1 ma and -20°C

HFE max = 200 at 1 ma and $+75^{\circ}\text{C}$

c. Diodes

Forward base-collector voltage drop = 0.7 volts max at 1 ma and 25°C

Reverse voltage base-collector = 40 volts max at 25°C

Peak leakage current = 200 nanoamps at 24V and 55°C.

Forward current maximum = 10 ma at 25°C

d. Resistors

Capacity per 1000 ohms at "N" isolation region = 2 pf max

Capacity of "N" region to "P" substrate = 10 pf max

All "N" regions per 10 K section must be floating with respect to the other "N" regions.

The parasitic PNP beta from the resistor to substrate is a maximum of 0.01 at 25°C.

Nominal resistance is $45 \pm 10\%$ at 25°C.

The temperature coefficient of resistance is 0.3% per °C max.

Maximum tolerance is $\pm 20\%$ from -10°C to + 65°C.

e. Capacitors - Stray Parasitic

$$C = 2 C_o \frac{(V2 + 1 - V1 + 1)}{V2 - V1} \text{ farads} \quad (\text{Equation 1.0})$$

where C = equivalent capacity

C_o = zero - volt capacity

$V1$ = minimum voltage across C_o

$V2$ = maximum voltage across C_o

and values for C_o are $C_{ob} = 9 \text{ pf max.}$

$C_{ib} = 6 \text{ pf max.}$

Collector of PNP to "P" substrate = 9 pf max.

"P" resistor material to "N" isolation region = 2 pf/K ohm max.

1.6.5.2 The equivalent schematic diagram (figure 19) shows the discrete component gate of (figure 15) converted to the integrated circuit schematic. On the Nimbus Program this schematic diagram is implemented by two of the micro chips with each chip containing 4 bit gates. Thus, 8 bit gates are present but only 7 are used. Since discussions on the circuits in (figure 19) would be complicated by the size of the drawing and since all 7 bit gates operate identically, only one bit gate will be discussed in (figure 20). The stray parasitic capacitors on the input diode, CR7, and output diode, CR14, have been added for circuit considerations, but are considered to be negligible in comparison with the operating speed of the Nimbus PCM. Capacitor C_{bo} is approximately nine picofarads and C_{eb} is approximately six picofarads. Since the diodes CR7 and CR14 are actually implemented by NPN transistors used with open emitter circuits, the C_{eb} is effectively not in the circuit, and the C_{bc} value of nine picofarads is only in the circuit until the base-collector junction is forward biased. The RC time of C_{bc} has a maximum of only $9 \times 10^{-12} \times (1K + 30K) = 279 \times 10^{-9}$ seconds or $RC = 0.279$ microseconds. This RC time is affected by the stray input capacity (which is unspecified), C4 capacity, and the stray capacities associated with R1 and Q1 which are considerably larger than C_{bc} so that with respect to the entire gate circuit C_{bc} becomes negligible. Thus, the actual gate reduces to the circuit shown in figure 19 wherein stray capacities C_{eb} and C_{bc} of diodes CR7 and CR14 are negligible.

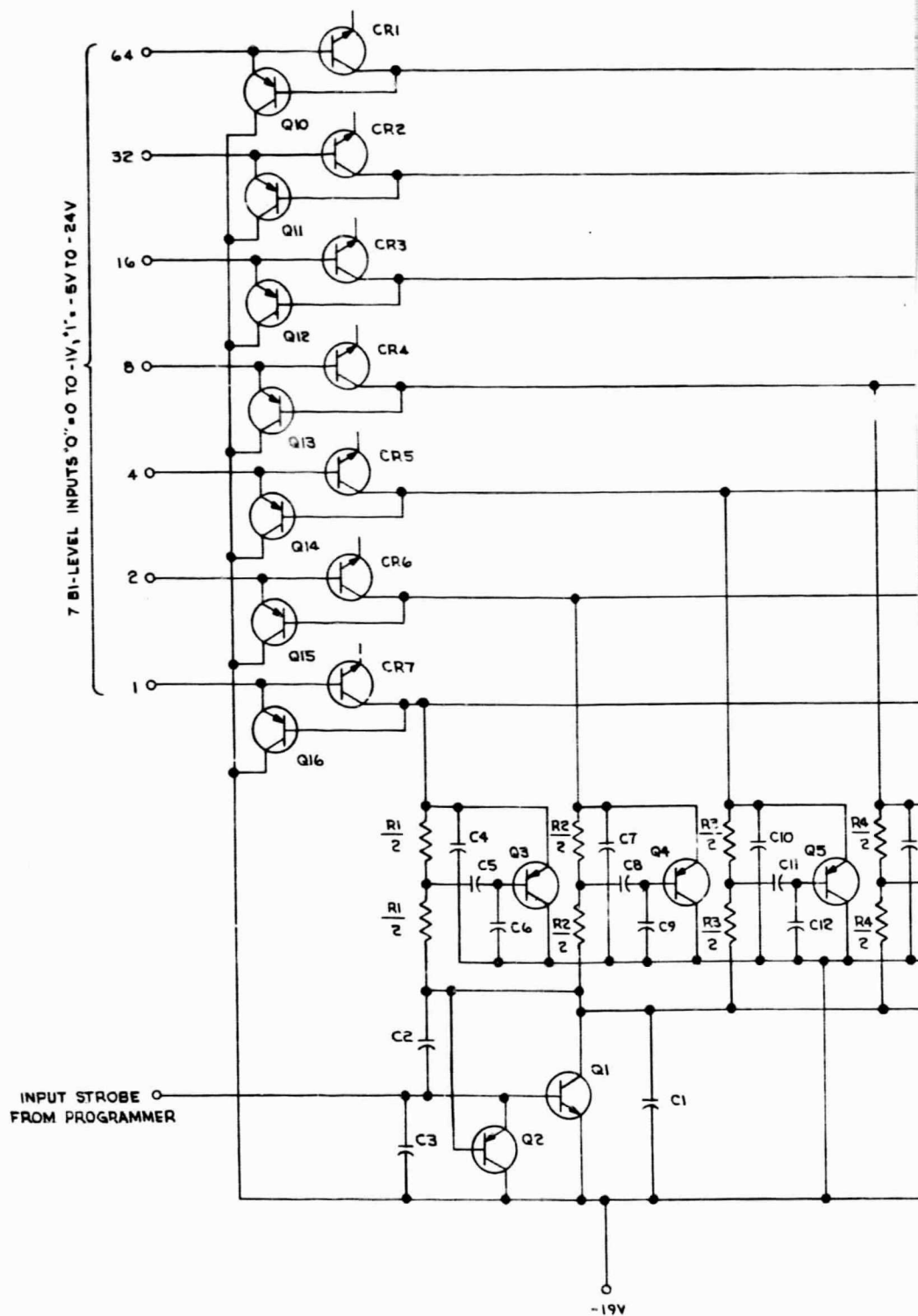
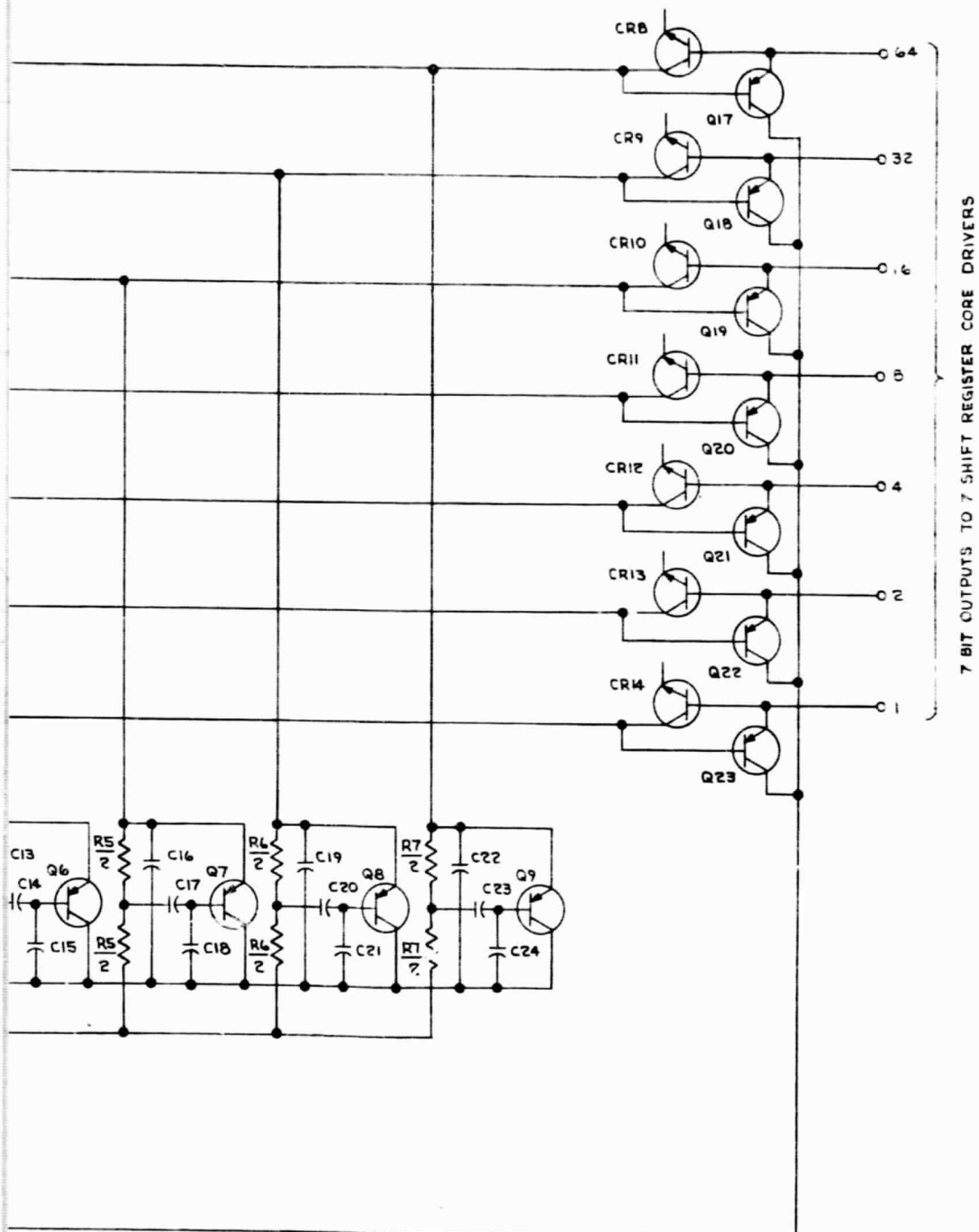


Figure 19. Microelectronic E



Equivalent Circuit Seven Bit Digital Word Gate Schematic Diagram



Figure 20. Microelectronic Equivalent Circuit One Bit Digital Word Gate Schematic Diagram

1.6.5.3 Figure 20 shows four undesirable PNP transistors Q2, Q3, Q16, and Q23 which are formed by the process of fabricating NPN transistors on a "P" substrate material (figure 21, View A). If these undesirable transistors possess a current gain of 0.01 or greater, operation of the gate will be materially degraded. For example, Q16 emitter is the anode (base) of CR7 and Q16 base is the cathode (collector) of CR7. Any input signal current becomes PNP base current and the collector of the PNP is effectively connected to the substrate and -19 vdc. The transistor Beta times this base current will flow directly from the input bilevel line to the substrate with the current completely bypassing R1 (figure 21, View B). Effectively, R1 becomes smaller by the amount of the stray PNP Beta.

$$I_{in} = \frac{-19 - (-V_{ce \text{ Sat } Q1}) - (-E_{in})}{R1 + R1 (\text{PNP Beta})} \quad (\text{Equation 2})$$

$$R1 (\text{effective}) = \frac{R1}{1 + \text{Beta stray}} \quad (\text{Equation 3})$$

Therefore, if Q16 has a Beta of 0.1, R1 is bypassed by 10R1 with an effective decrease of 10%. With the normal range of tolerance already $\pm 20\%$ it is evident that all stray PNP Betas should be held to 0.01 or less. This maximum Beta will hold R1 decrease to 1% and the undesirable PNP transistors can be removed from the circuit.

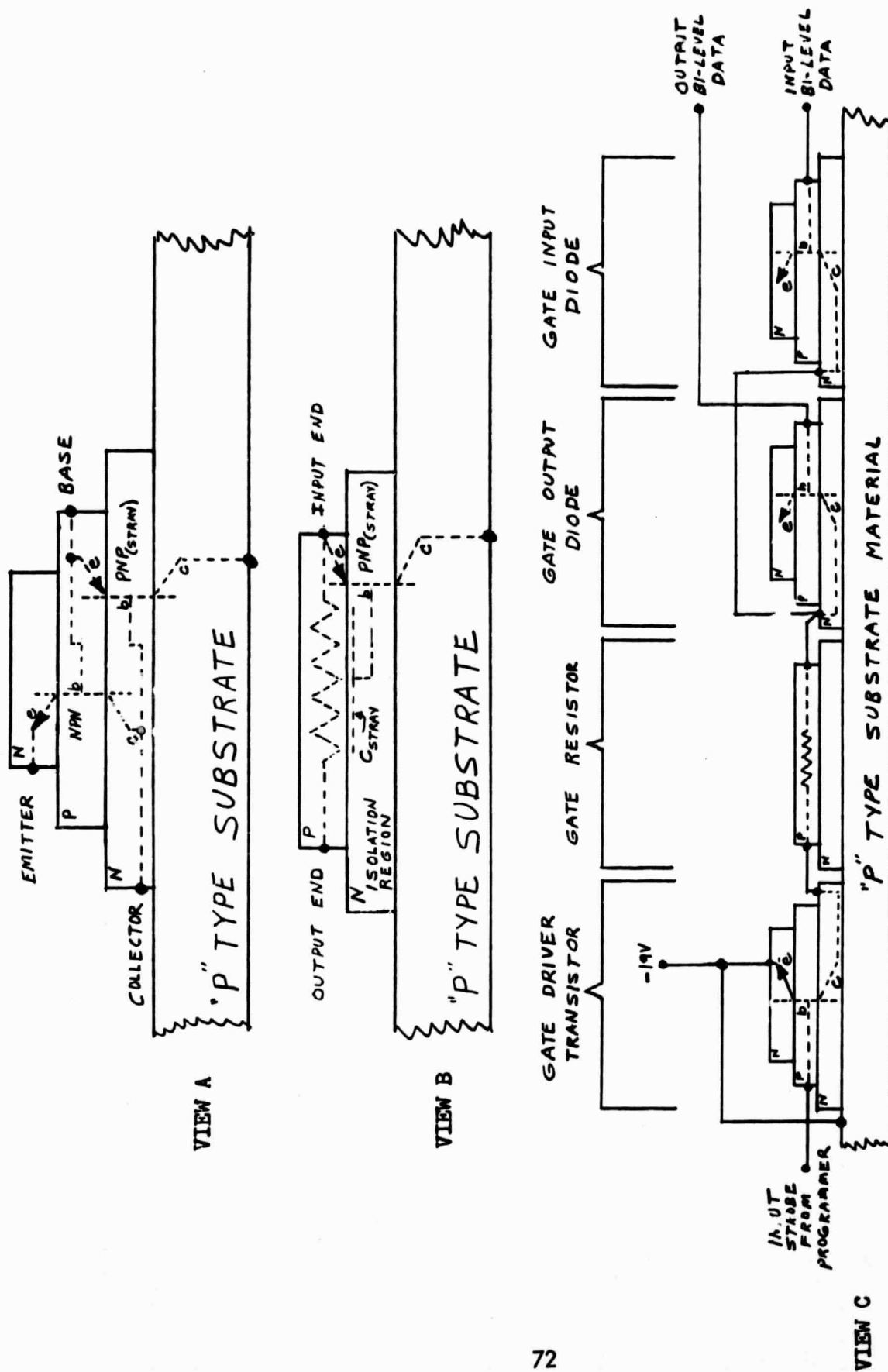


Figure 21. Physical Layout of Integrated Circuit Transistors and Resistors

- 1.6.5.4 View C shows the physical layout (one bit wiring) of the gate integrated components, showing the common substrate "P" material which prevents perfect isolation of all the individual components. Note how all the stray capacities and PN junctions are formed because of the physical properties and proximity of the various materials used in the diffusion process. The capacities are dependent on the area and thickness of the material, but since junctions are formed the capacities are also dependent on the junction voltages. Equation 1 show this. Figure 22 shows a simplified one bit gate with the voltages across the capacitors to determine the values of C1 through C6. The voltages for Q1 are taken from the assumed specifications. Since an input "0" logic places the greatest voltage across R1, the junction of the two resistors which make up R1 contains a voltage half way between -1.24 and -18 volts equal to -9.62 volts. The following parameters were calculated from the capacitor equation:
- a. C1 (collector to substrate capacity of Q1) has a zero volt capacity of 10 pf but an effective capacity of 3.48 pf.
 - b. C2 (collector to base capacity of Q1) has a zero volt capacity of nine pf but an effective capacity of 3.59 pf.
 - c. C3 (Base to emitter capacity of Q1) has a zero volt capacity of six pf but an effective capacity of 8.28 pf.
 - d. C4 (Collector to substrate capacity of CR7 plus CR14 with each having 10 pf) has a zero capacity of 20 pf but an effective capacity of 4.81 pf.

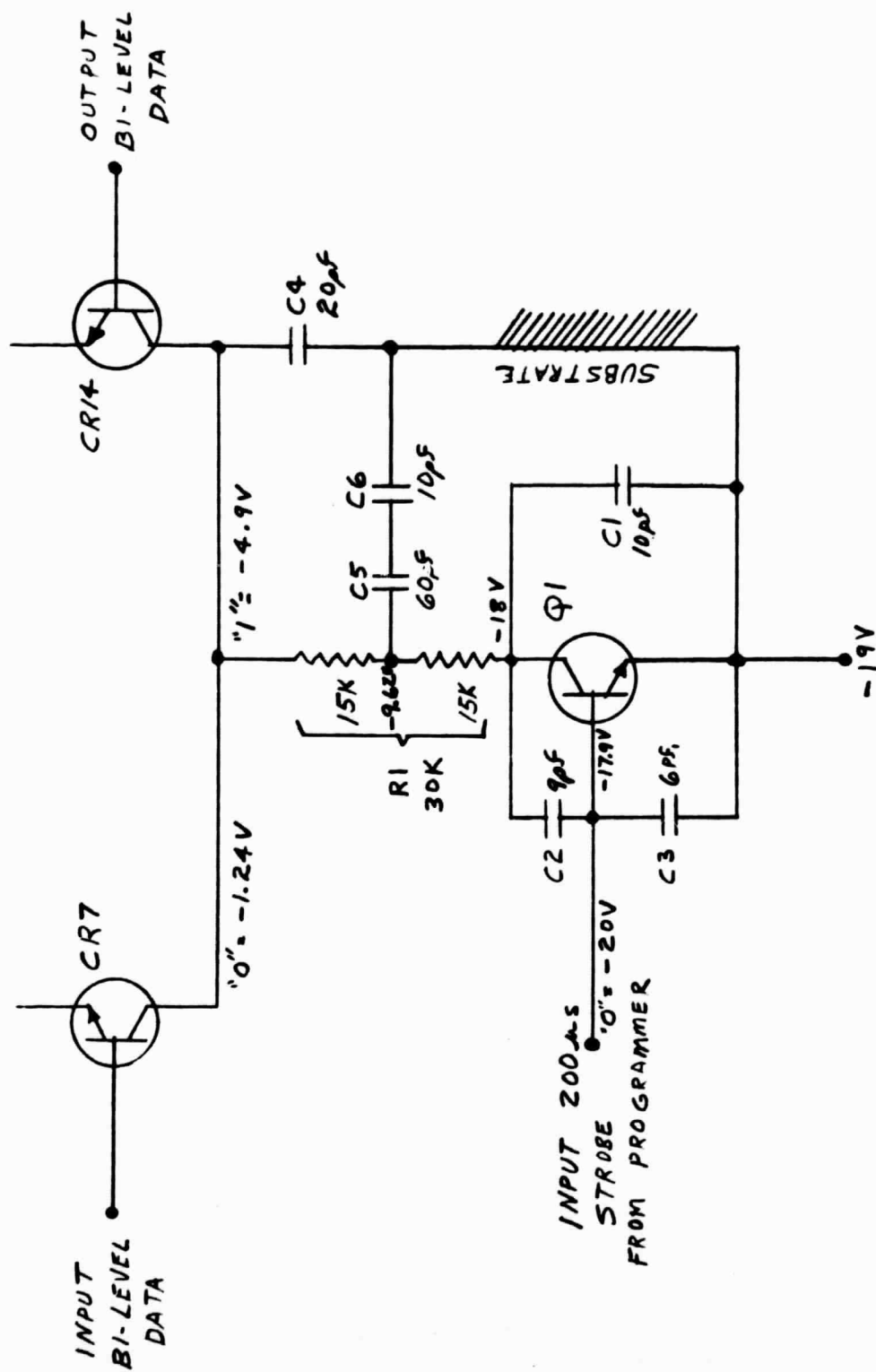


Figure 22. Simplified One Bit Gate Equivalent Circuit Schematic Diagram

- e. $C5 + C6 - C5$ is the capacity of R1 to the "N" isolation region, and C6 is the capacity of the "N" isolation region to the substrate. With Q3 eliminated, C5 and C6 are in series, and the total zero volt capacity is 8.57 pf and effective capacity is 2.27 pf.

As noted above the calculated capacities are very small, and all of the RC time constants involved, using these capacitors, are less than one usec. Any time constants which are less than one usec become negligible since the only command affected by the transient response is the programmer command to the gate driver which has a rise and fall time of approximately four usec. Only stray C5 cap- is critical. Assuming a Q3 gain of greater than 0.01, C5 would be multiplied by this gain and the junction of CR7, CR14, and R1 would be pulled negative to -9.62 volts. This is because C5 and Q3 would short the top half of R1 for the first few usec of every sample command until C5 is charged. If the junction of CR7, CR14, and R1 is held more negative than -4.9 volts for eight usec or longer, it is possible to read a false "1" into the output register when the input is a "0". However, with the nominal Q3 Beta assumed, the equivalent circuit is reduced to the circuit shown in figure 15.

- 1.6.6 Time Code Storage Blocks and Logic Analysis. - The block diagram (figure 23) circuits use two commands from the Nimbus "A" or "C" clock to convert the RZ serial pulse width modulated Time Code to an NRZ output code. The Time Code train is coded BCD at the input to the PCM, and is a BCD code at the output of the PCM.

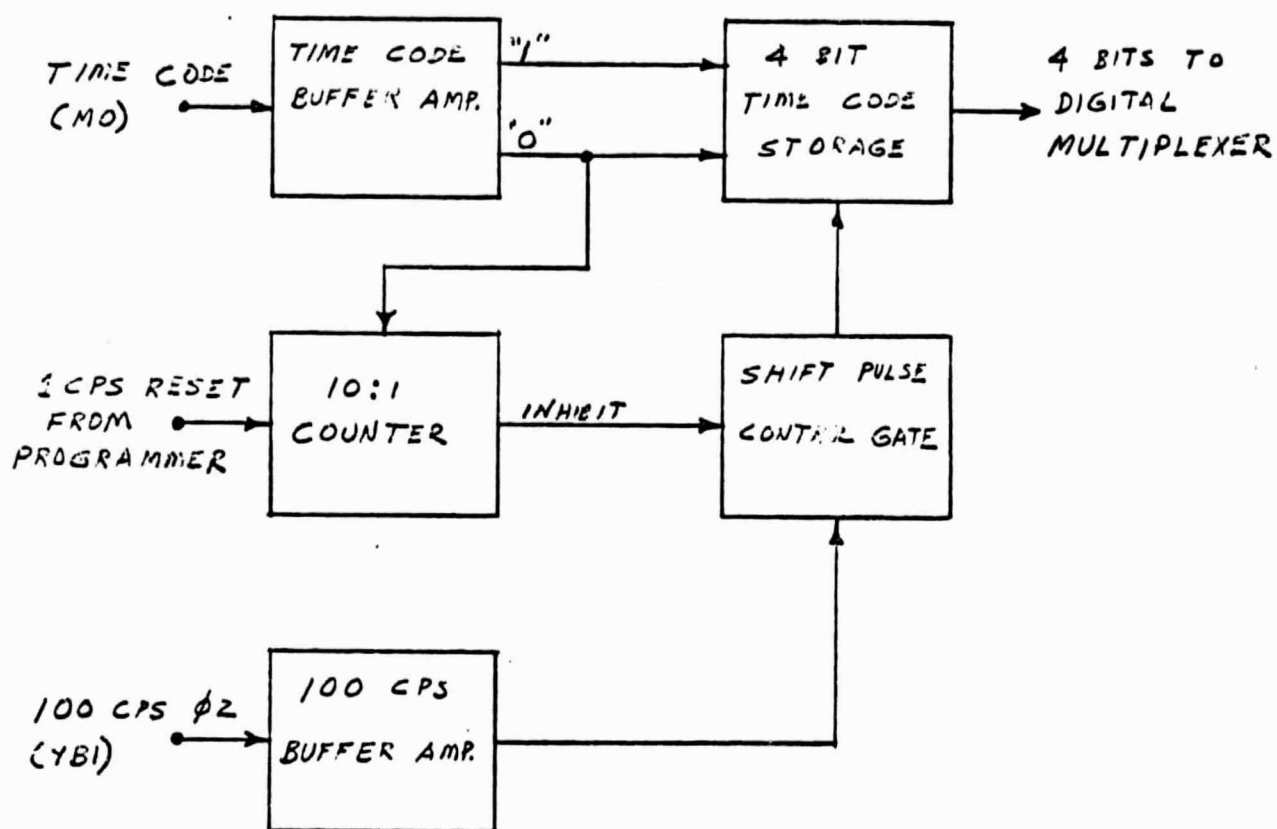


Figure 23. Time Code Storage Block Diagram

- 1.6.6.1 The 10:1 counter is externally synchronized by the programmer at the same time the programmer counters are synchronized by the Time Code detected 1 cps reset pulse. Thus, the 10:1 counter is in phase with the Time Code and counts the "0's" as they occur. During the first five counts of the 10:1 counter, all four Time Code bits of a word are shifted into the four stage shift register by the 100 cps $\div 2$, then the last flip-flop in the 10:1 counter inhibits the shift pulses so that they do not pass through the control gate. The four stages of the shift register are directly connected to a digital multiplexer word gate. The Time Code is fed into the output register when the digital word gate is strobed by the programmer.
- 1.6.6.2 Strobing of the digital multiplexer is entirely independent of the Time Code storage circuits, as the Time Code storage circuits will automatically store the next group of four Time Code bits regardless of what the programmer does. Since the programmer is synchronous with the Time Code circuits, the programmer provides a digital multiplexer strobe pulse during the time interval that the shift pulse control gate is inhibited by the 10:1 counter. This strobe pulse does not occur at the same time in every Time Code group (with respect to the beginning of the interval gap) as the Time Code can only be readout into subcommutated time slot. The Time Code word requires 100 milliseconds at the input to the PCM and is reduced to 16 milliseconds at the output of the PCM.

1.6.6.3 Because the Time Code word rate and PCM word rate are not compatible with respect to each other, the output Time Code words are unevenly spaced in the PCM format with respect to each other. The input Time Code occurs at a much slower rate than the PCM output words, and a storage device must be used to accumulate and store the Time Code until the time occurs to place it in the output format. The Time Code consists of four bits of data for every Time Code train 10 bit word, therefore, a minimum of four bits of storage is required. If all six Time Code words (units and tens of seconds, units and tens of minutes, units and tens of hours) were stored and readout into adjacent output PCM words, 22 bits of storage would be required, therefore, only four bits of storage was selected to minimize the hardware. A Time Code synchronous 10:1 counter is used to gate the four Time Code data bits into the storage register. This counter is made synchronous with the Time Code when the programmer detects the Time Code five "1's" and resets the 10:1 counter.

1.6.6.4 The logic diagram of (figure 24) shows the Time Code logic. The timing diagrams of (figure 9 and 25) show that the 10 bit positions of any Time Code word occupies 10 milliseconds of time each. If a "0" is present, only the first two milliseconds are used, if a "1" is present, only the first six milliseconds are used. The last four milliseconds are never used. Since the "1" and the "0" pulses begin at the same time with respect to the bit position, there is always a pulse transition at the beginning of each

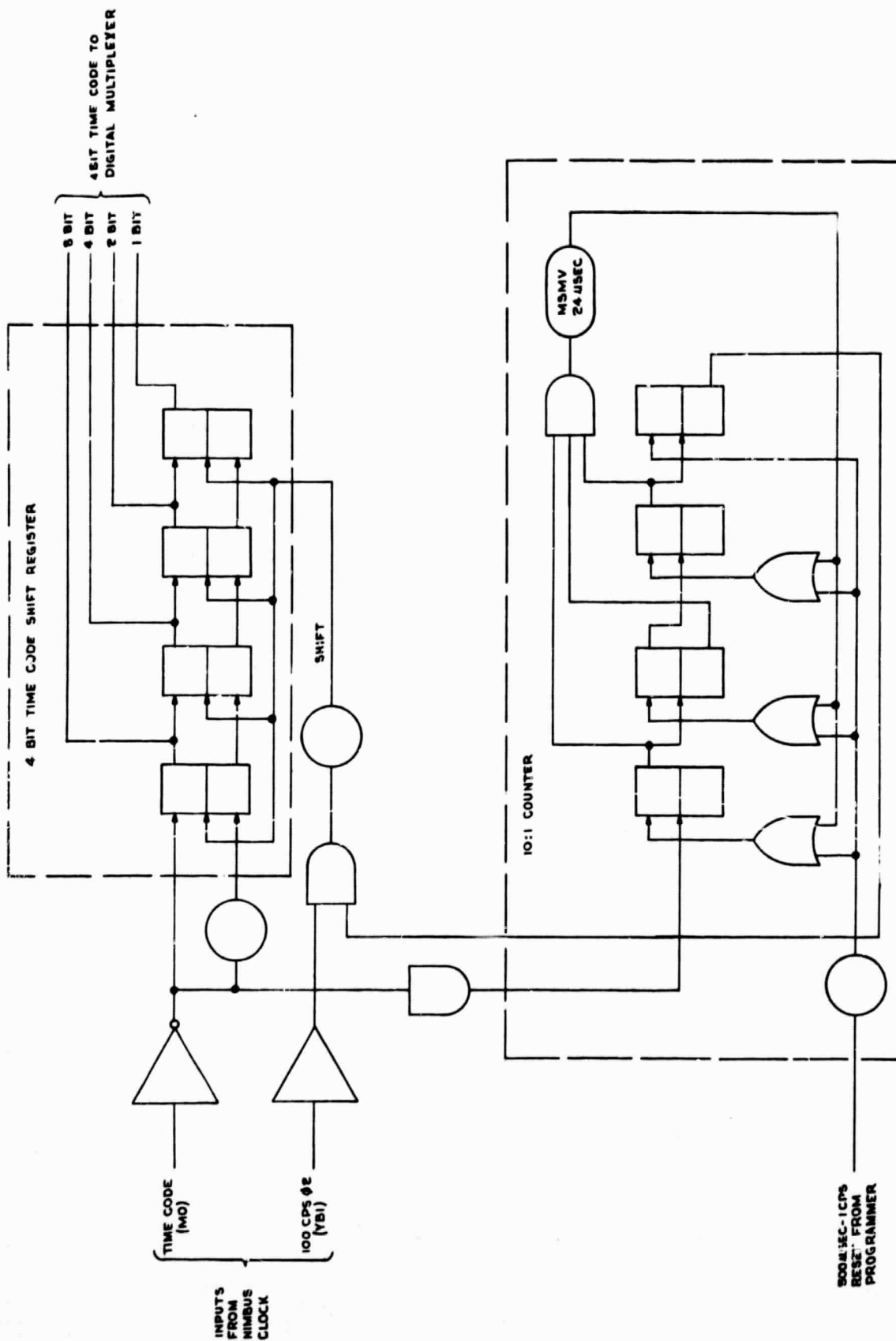


Figure 24. Time Code Storage Logic Diagram

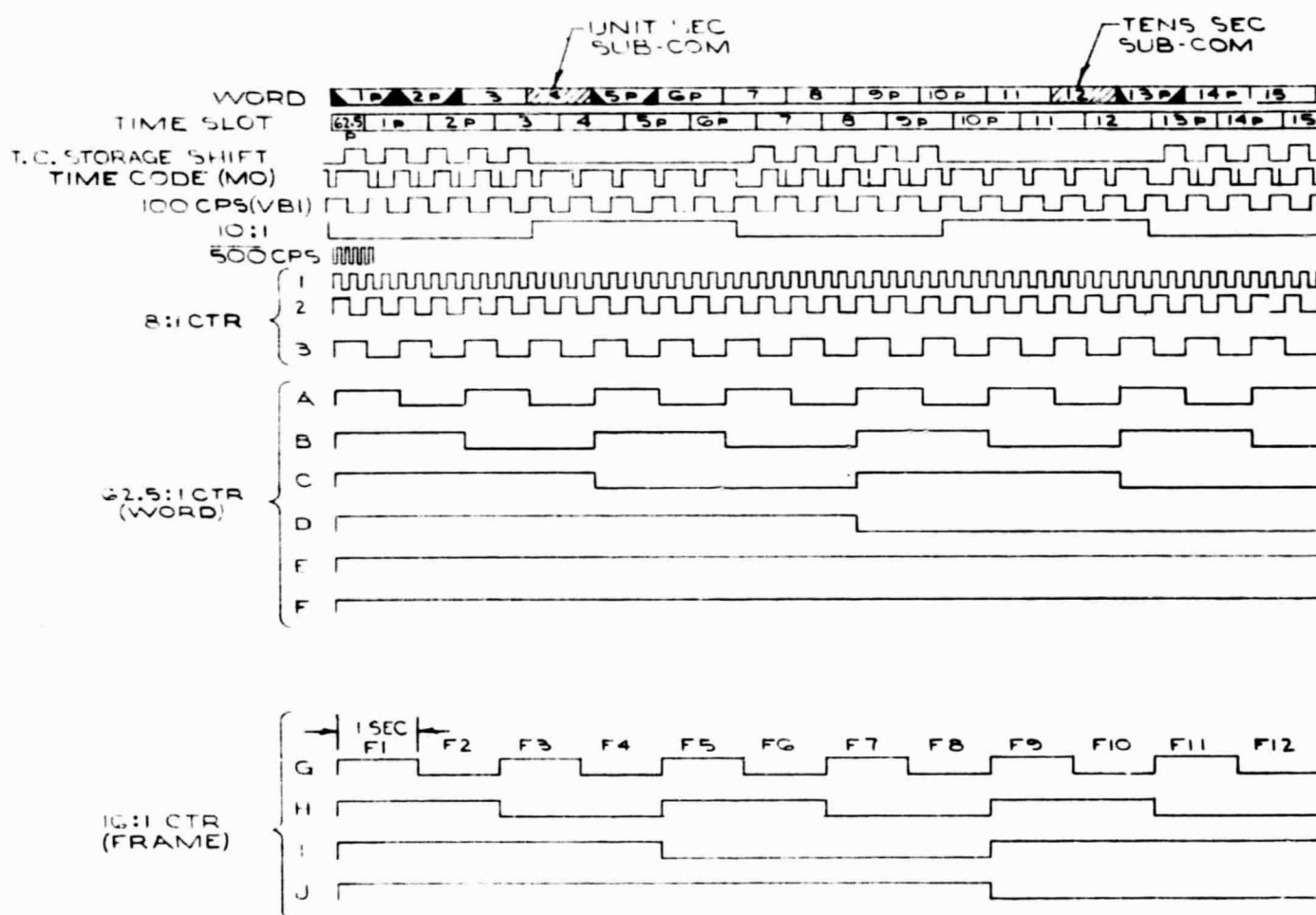
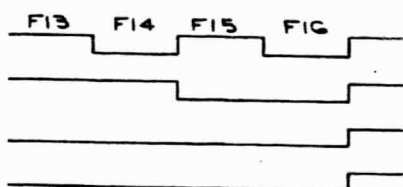
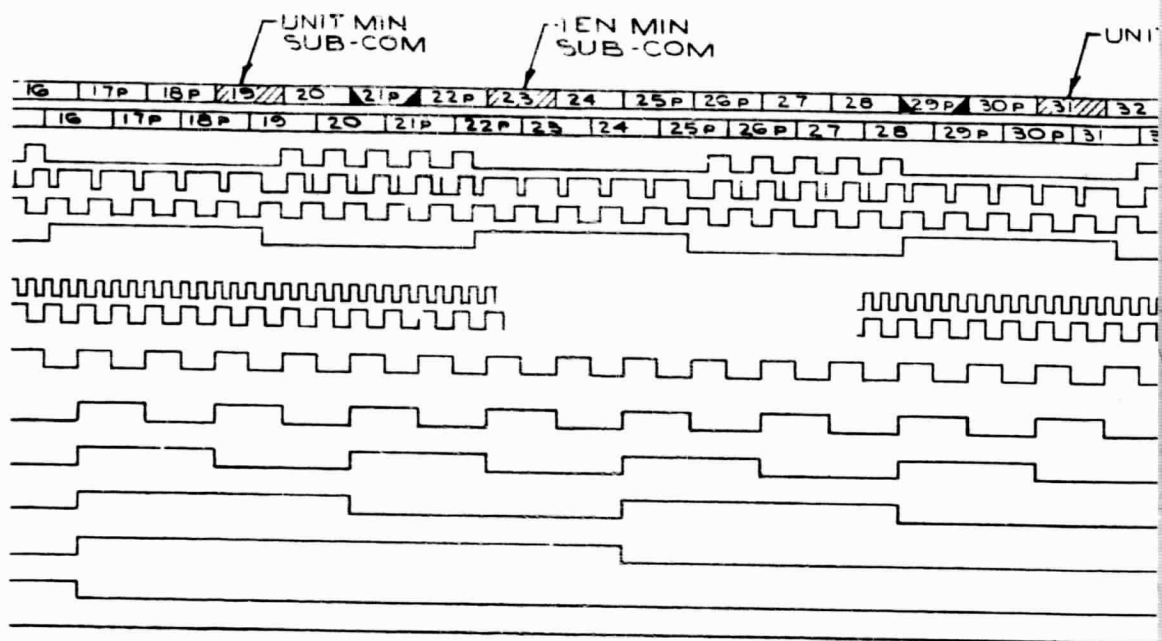
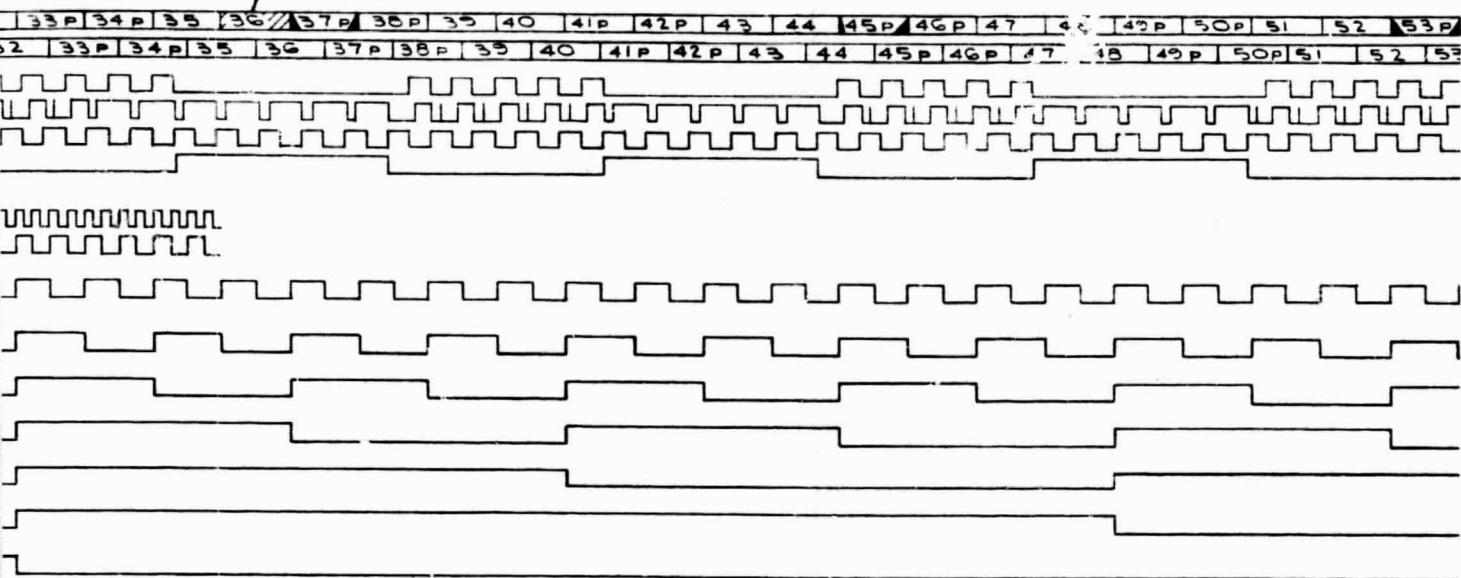


Figure 25. Time Code Storage Timing Diagram (Sheet 1 of 2)

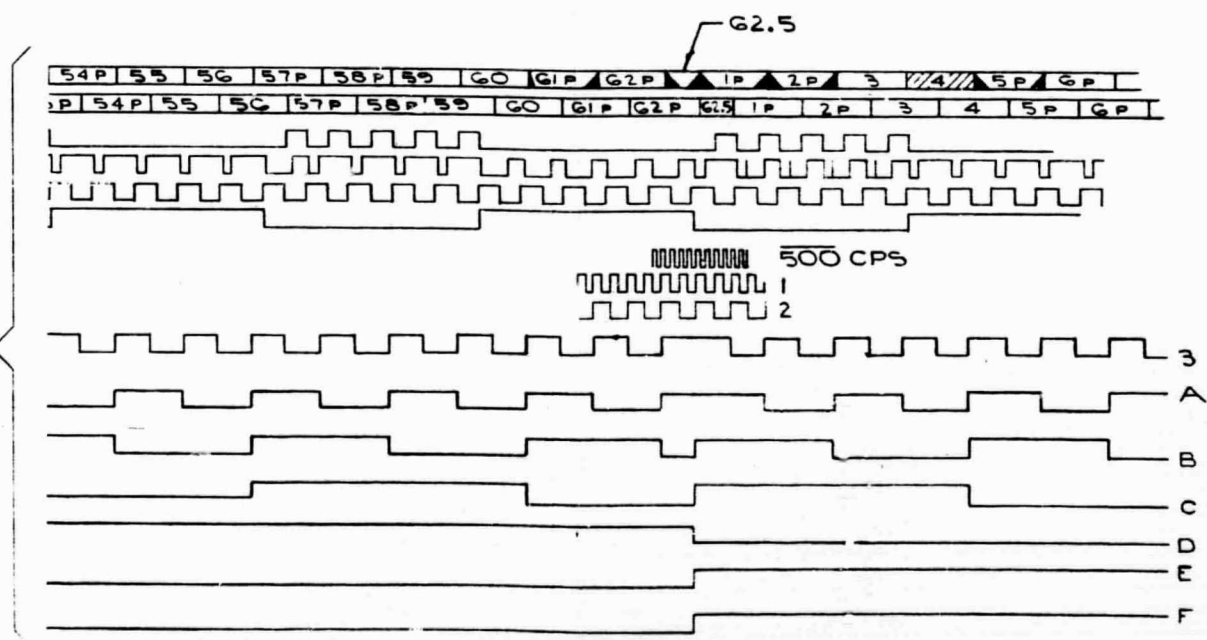


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bit time. This transition is used to trigger the 10:1 counter. The first bit position in each group of 10 bits is not used for the Time Code data, but bit positions 2, 3, 4, and 5 contain Time Code bits 1, 2, 4, and 8 respectively. The last five bit positions do not contain Time Code data which allows the programmer 50 milliseconds (approximately three PCM words) of time in which to read the stored Time Code word through the digital multiplexer before the Time Code changes. The 10:1 counter allows the 100 cps $\phi 2$ to shift the Time Code data serially into the input shift register during the first five bit positions and inhibits the next five shift pulses to give the programmer time to readout the four bits stored. The Time Codes "1's" occur during the fall time of 100 cps $\phi 2$, so that the negative 100 cps transient is used to strobe the "1's" into the shift register. This strobe pulse occurs 2.5 milliseconds after the "0" pulse disappears and 1.5 milliseconds before the "1" pulse disappears, therefore, it is centered properly for reliable gating of any "1's" that appear. This timing is the same for the Nimbus "A" and "C" clocks.

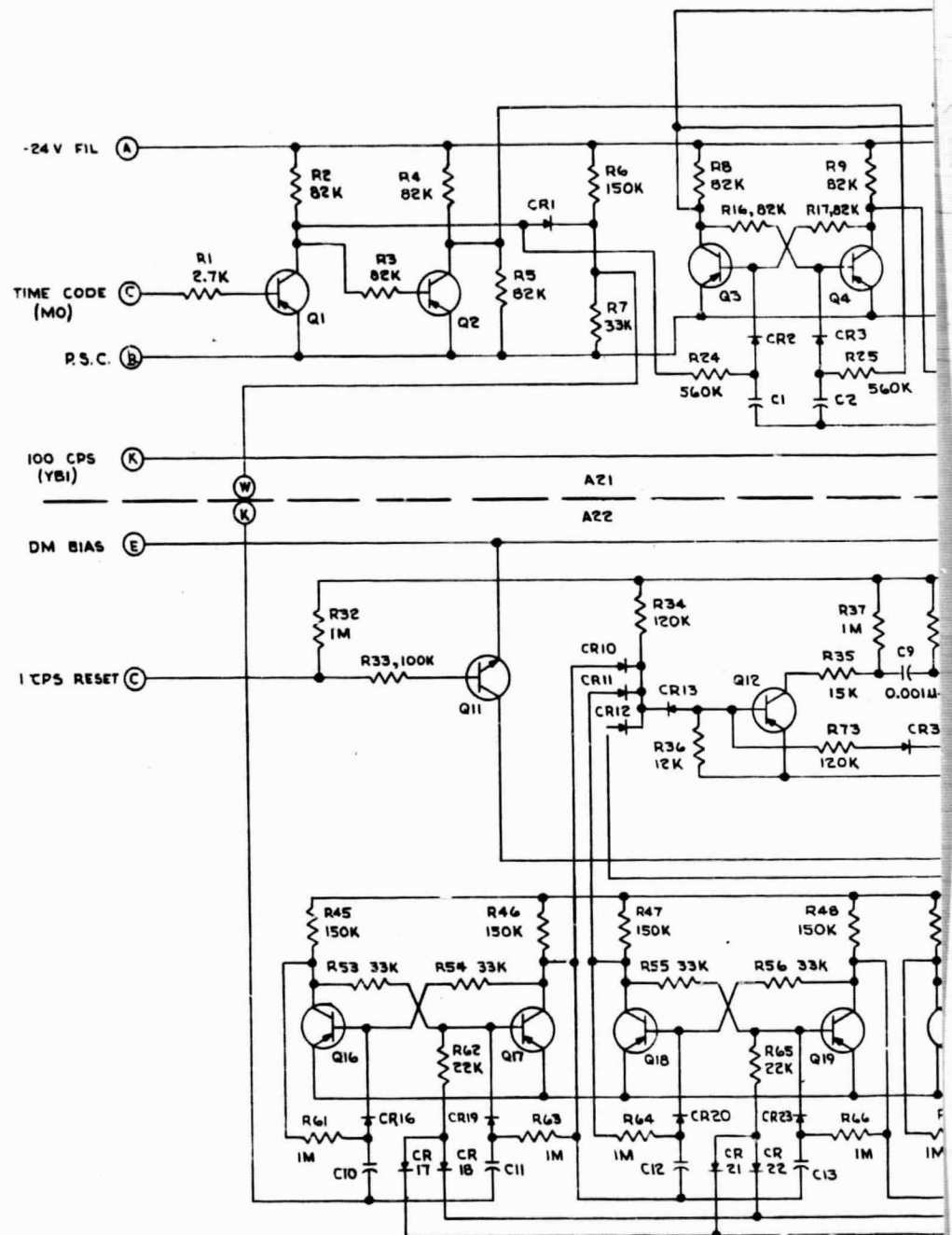
- 1.6.6.5 A Time Code buffer amplifier is used to change the input DC level to make it compatible with the system logic levels and also places a minimum load on the clock line (MO). The amplifier is connected to an inverter so that the input Time Code data and its complement can be fed to the first stage of the shift register to provide the proper input data for shifting the data serially. The amplifier is also connected to the 10:1

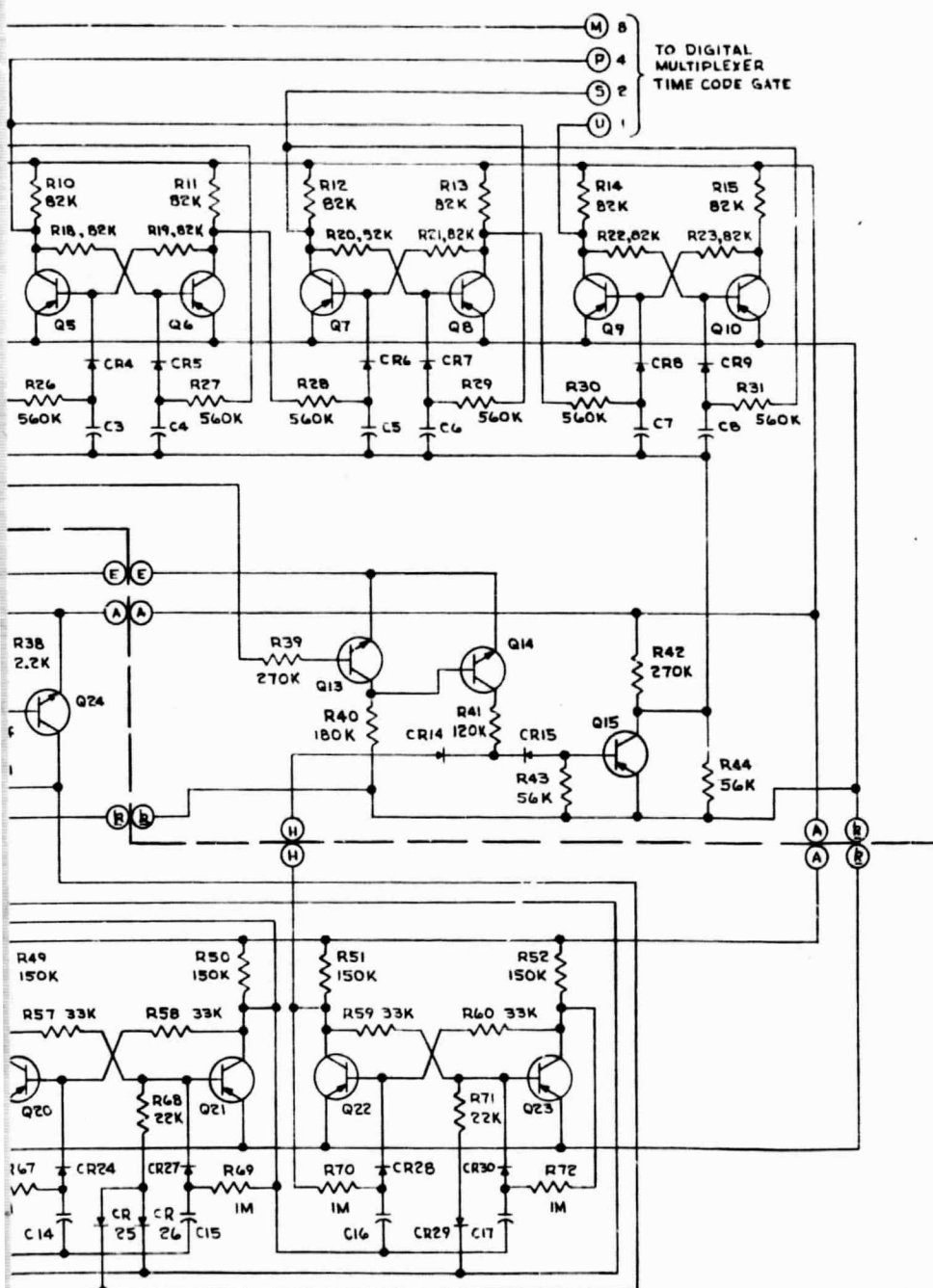
counter through an isolating diode gate. The 100 cps $\phi 2$ buffer amplifier is connected to an "AND" gate that is controlled by the last stage of the 10:1 counter. This "AND" gate is enabled for the first five bits of every Time Code 10 bit group and allows the 100 cps signal to feed into the inverter. The inverter output then becomes the five shift pulses to the four bit storage register.

- 1.6.6.6 The 10:1 counter uses a monostable for feedback reset to insure that all counters are reset every time because an "AND" gate detects the 5:1 count which would make it possible to reset one stage feeding the "AND" gate and remove the reset pulse before the other two stages are reset. An inverter on the reset line from the programmer is used to correct the polarity of the 1 cps reset pulse as the programmer counters contain NPN's and the 10:1 counter contains PNP's.

- 1.6.7 Time Code Storage Detailed Analysis. - The Time Code storage circuitry is shown in figure 26. The function of this circuitry is to accept the serial Time Code data having the form of a pulse width modulated signal, store the data until it can be inserted into the output format, and convert the serial data into a four bit parallel data word with logic levels compatible to the digital multiplexer gate.

- 1.6.7.1 The circuitry consists of the Time Code buffer Q1 and Q2 and the four stage shift register Q3 through Q10 on A21 with 1 cps reset buffer Q11, the 5:1 count detect gate and reset monostable CR10, CR11, CR12, Q12, and Q24, the shift driver Q13, Q14, and Q15, and the four stage 10:1





NOTES:

1. TRANSISTORS: Q1 THRU Q10, Q15, Q16 THRU Q23 ARE 102258; Q11, Q14, Q24 ARE 100818; Q12 IS 100422, & Q13 IS RAD 100667.
2. UNLESS OTHERWISE SPECIFIED ALL DIODES ARE 100G13.
3. CAPACITORS: C1 THRU C8 ARE 820 PF, C10 THRU C17 ARE 150 PF.
4. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS, $\pm 5\%$ TOL, $\frac{1}{4}$ W. CAPACITANCE VALUES ARE IN PICOFARADS, $\pm 10\%$ TOL, 200V.
5. PARTIAL REF DESIGNATIONS ARE SHOWN, FOR COMPLETE DESIGNATION PREFIX WITH UNIT NO. OR SUBASSY DESIGNATION.

Figure 26. Time Code Storage A21 and A22 Schematic Diagram

counter Q16 through Q23 on A22. The Time Code signal is buffered and fed into the shift register. The signal is also fed down to the 10:1 counter which consists of a 5:1 counter (first three stages) and a 2:1 counter. The output of the last stage of the 10:1 counter feeds an inhibit AND gate in the shift driver. The shift driver also accepts the 100 cps (YB1) signal. The purpose of the 10:1 counter is to provide storage time in the shift register by shifting in only the sync bit and the four data bits of the ten bit Time Code word. The counter enables the shift driver thereby providing five shift pulses to the register. These five pulses shift out previously stored data and the sync bit, and load the four bits of Time Code into the four stages. At this time the counter inhibits the shift driver and the shift register remains loaded with Time Code data. During the inhibit time, the data is transferred through a digital multiplexer gate into the output format. The next change of state of the 10:1 counter output occurs and the stored data is shifted out and replaced by the next Time Code data word. The 1 cps reset driver provides synchronization between the Time Code and PCM output format. The AND gate and monostable detect the five count and reset the first three stages of the counter giving the 5:1 counter section.

- 1.6.7.2 The Time Code buffer is a two stage device providing both an inverted and a non-inverted steering output to the shift register. The input Time Code signal swings from 0V to -1V. The two steering outputs swing from 0V - 0.3V to -11V $\pm$ 1V and have an output impedance of approximately

40K. The outputs were designed to match the shift register stages to give uniform transfer characteristics. An inverted Time Code signal is also fed to the 10:1 counter. This output is diode decoupled to allow a source impedance and level similar to those of the counter stages. The output amplitude for this signal is limited to about 4V so that the counter transistors will not exhibit base-emitter junction breakdown.

- 1.6.7.3 The shift register is similar to that of the 1 cps reset circuitry (paragraph 1.6.8) except for the PNP transistors. The PNP type was chosen since it is directly compatible with the digital multiplexer gate and has a simpler buffer input than an NPN shift register. As in the 1 cps reset shift register, the stages are of the saturating type using direct coupled transfer through the steering resistors. Positive triggering of the bistables is accomplished by differentiator circuits with diode coupling to the bases of the transistors. The steering levels are 0V -0.3V (transfer of binary "1") and -11 $\pm$ 1V (transfer of binary "0"). The differentiated spike is approximately 4V in amplitude. The output logic levels to the digital multiplexer are 0V -0.3V (binary "0") and -11V $\pm$ 1V (binary "1").
- 1.6.7.4 The PNP configuration for the 10:1 counter was used so that the existing Time Code buffer could be utilized. The stages of the counter are typical saturating bistables. Triggering of the bistables is by the differentiators connected to the bases through the coupling diodes. The 5:1 feedback reset and the 1 cps reset circuits trigger one side of the bistables through

the OR gate diodes and the 22K base resistors. The transistors are triggered by being turned on instead of off as with the normal feed forward triggering. The output levels of the counters are 0V -0.3V and -4V $\pm$ 0.5V. The swing is limited to approximately 4V in order to keep the base-emitter junctions from breaking down.

- 1.6.7.5 The 5:1 feedback reset monostable is triggered by the three input AND gate. The monostable configuration is unorthodox due to the level requirements of the input gate and the reset line. Normally, both the PNP and NPN transistors are off. When the AND is enabled, the PNP saturates supplying a surge of current through the timing capacitor C9 thereby saturating the NPN output stage. The positive feedback, necessary in any monostable circuit, is supplied through R73 and CR31 and keeps the PNP saturated for the duration of the output pulse. The output is a negative pulse swing from 0V to -22V. The width of the pulse is determined by the duration of the current surge through the capacitor where:

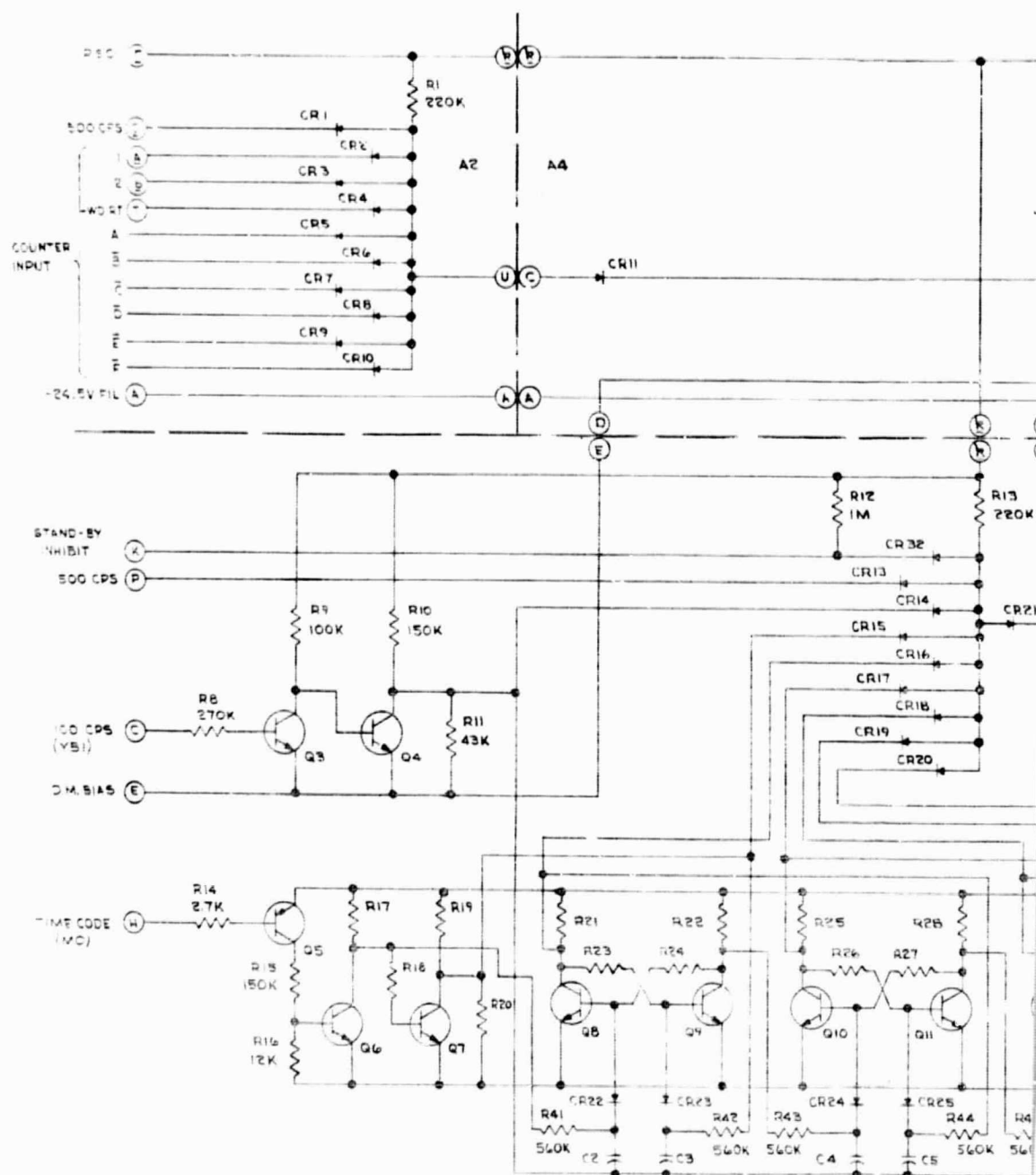
$$1 \approx \frac{22V}{R_{35}} \left(e - \frac{t}{R_{35} C_9} \right).$$

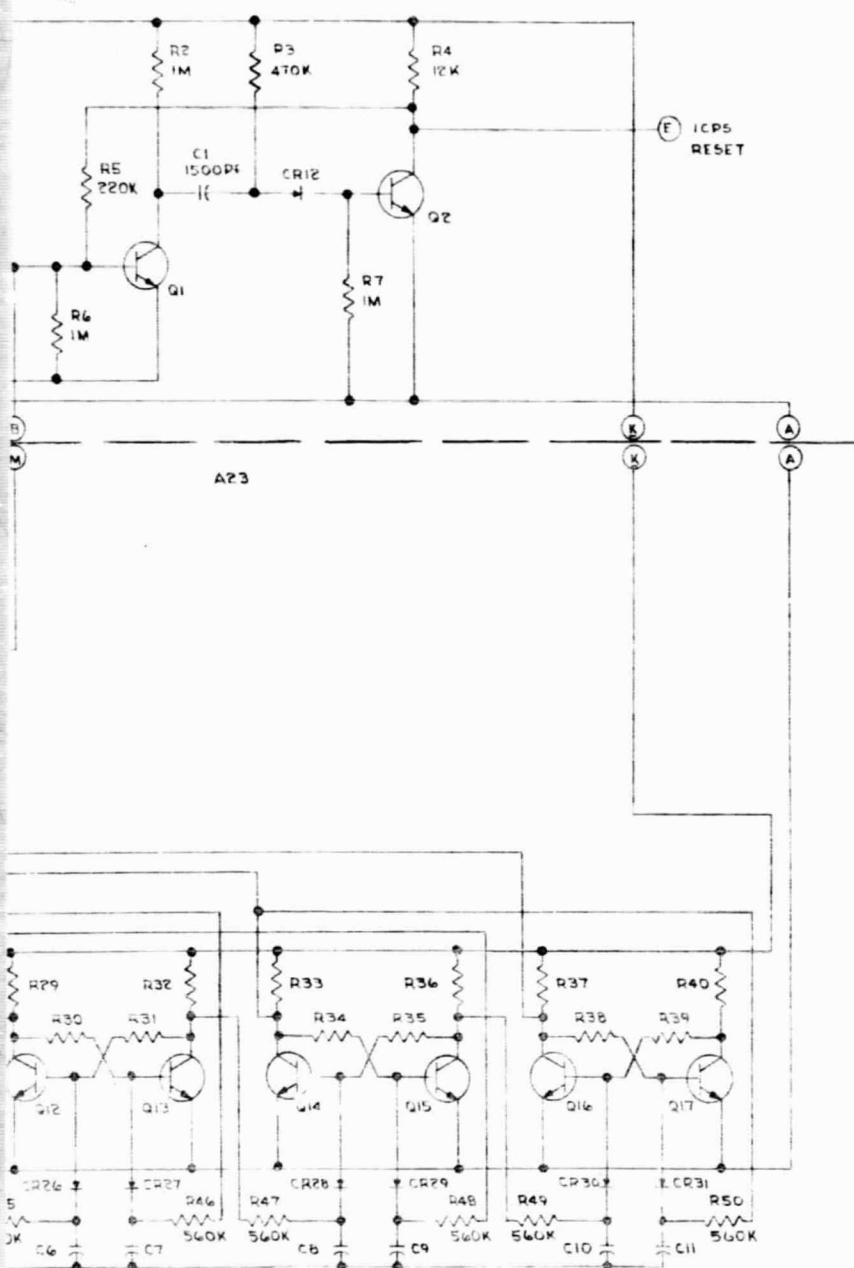
The 1 cps reset driver is a simple one stage inverter used to synchronize the 10:1 counter with the PCM format.

1.6.7.6 The shift driver consists of a two stage non-inverting buffer for the 100 cps (YB1) signal, a diode inhibit AND gate and the PNP output driver. The 100 cps input signal swings from $-1.5V \pm 1V$ to $-23V \pm 1.5V$ with a 270 ohm source impedance. The buffer output acts as a strobe to the inhibit AND gate resistor R41. When the gate is enabled, the PNP stage is saturated and when inhibited, the PNP transistor is off. The output shift pulse level is limited to $3.8V \pm 0.5V$ to prevent base-emitter breakdown of the transistors in the storage shift register. The output impedance of the shift driver was designed to discharge the shift line capacitance in 1 ms. The 1 ms insures ample discharge in view of the five ms shift pulse width and 10 ms shift pulse period.

1.6.8 The one cps Reset circuitry is shown in (figure 27). The circuitry provides a one cps synchronous reset pulse obtained from the satellite master clock. In addition, a 62.5:1 count detector supplies a one cps reset timing in the event of a failure in the satellite master clock to maintain the one second format. The one cps reset allows the PCM to operate synchronously with the master clock. The configuration was developed from the necessity of using both the Nimbus A and C clocks. Although both clocks have one cps signals, they have different phasing. To obtain a design capable of using both clocks only the Time Code signal (MO) and the 100 cps signal (YB1) were utilized. These two signals do not change phasing with the two clocks. The one cps reset is obtained by detecting the unique Time Code sync word

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NOTES:

1. RESISTORS R17 THRU R40 ARE 82K.
2. DIODES ARE RAD 100G13.
3. TRANSISTORS: Q2, Q3, Q4, Q6 THRU Q17 ARE RAD 100G67; Q1 IS RAD 100B18, Q5 IS RAD 100422.
4. UNLESS OTHERWISE SPECIFIED RESISTANCE VALUES ARE IN OHMS, 5% TOL, 1/4 W. ALL CAPACITORS ARE 820 PICO FARADS.
5. PARTIAL REF DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NO. OR SUBASSY DESIGNATION.

Figure 27. One CPS Reset A2, A4, and A23 Schematic Diagram

with the five stage shift register and nine input AND gate (A23). The output of the AND gate triggers the reset monostable through an OR gate. The 62.5:1 count detector is a 10 input diode AND gate (A2) which also connects through the OR gate to the monostable. Coincidence of reset from both gates is achieved by using the 500 cps signal as a common input. The reset monostable (A4) is triggered by the one cps pulse from the OR gate. The monostable was designed to provide a 500 us reset pulse. This width was chosen to guarantee reset even though some counters may be slow in response, and to allow for the effect of propagation delay through the counter string. Time Code data is read into the shift register in serial form by the Time Code buffer. The buffer accepts a -1V signal and provides two outputs to the steering resistors of the first shift register stage. Using this input method, all stages are the same and more uniform shifting action is achieved. The shift driver converts the 100 cps signal into an acceptable shift pulse. The phasing of the 100 cps signal is such that the shift transition always occurs within the logic "1" data time of the pulse width modulated Time Code. This phasing is unique to both clocks thereby permitting both to be compatible with the reset circuitry. The shift register is a typical transistor bistable configuration. All stages are saturating stages using direct coupled transfer through the steering resistors. Negative triggering of the bistables is accomplished by differentiator circuits with diode coupling to the bases of the transistors. The steering levels are $-22V \pm 1V$ (transfer of binary "1") and $-11V \pm 1V$ (transfer of binary "0"). The differentiated spike is approximately

4V in amplitude. Use of an NPN shift register was dictated by the logic levels of the present Nimbus PCM counters which feed the 62.5:1 detect gate. The Time Code buffer Q5, Q6, and Q7 provides both an inverted and a non-inverted steering output to the shift register. The input signal switches from 0V to -1V minimum, thereby necessitating the PNP stage. The two NPN transistors have output levels and output resistances identical to those of the bistable stages giving uniform transfer characteristics to the shift register. The 100 cps shift driver Q3 and Q4 is a two stage non-inverting device. The input signal swings from an upper level of $-1.5V$ $\pm 1.5V$. The two transistors are therefore referenced to the digital multiplexer bias $19V \pm 1V$ to insure at least a 1.5V back bias turn-off voltage. The output impedance was designed for a one msec rise time to insure the charging of the shift line capacitance within the five ms half cycle period of the square wave. The output level is limited to a 4.2V swing so as not to break down the base-emitter junctions of the shift register transistors. The monostable A4 provides the 500 us reset. It is triggered by a positive pulse causing Q1 to saturate. The input trigger pulse from the one cps detect gate is one msec wide although the 62.5:1 count detect gate can have a pulse width of only a few microseconds. The diode, CR12, is in series with the base to prevent the breakdown of the base-emitter junction of Q2. Incorporating the diode in the base leg, rather than the emitter leg allows the output level to go as close to -24V filtered as possible otherwise there would be difficulty in turning off the NPN transistors connected to the reset bus unless they were referenced to the digital multiplexer bias. The reset bus load is approximately 13K giving a 10V output level.

1.6.9 Storage Bistables. - The storage bistables (figure 28) functions as a storage device for transient bilevel digital data. Random input data is in the form of 250 msec pulses switching from 0 to -5 volts. The bistables are conventional saturating flip-flops designed on the basis of minimum power dissipation. The large collector resistance tends to slow transition time, but no critical timing problem exists with a 250 msec set pulse and a two msec reset pulse. The output is taken off the RESET side and with negative true logic this results in a one ma saturation current to the digital multiplexer for logic "0" at a voltage level of 0 to 0.3 volt. Binary "1" resulting from SET data is approximately -5 volts. The two msec RESET pulse is obtained from the programmer through an inverting driver.

1.7.0 Identification Format Buffers. - The buffers (figure 29) provide frame identification bits of Word two of the output format. These buffers are used to transform the programmer 16:1 count outputs to logic levels compatible to the digital multiplexer gate. The configuration selected has the features of minimum power consumption and loading of the counter stages. The input NPN stage operates class A in the off modes while the output PNP stage is in the saturated off modes. High input impedance is achieved with the 56K emitter resistors resulting in an input impedance of $(h_{FE}) (56K)$. The 270K collector resistors provide leakage current paths as well as decreasing the fall time. The output logic levels from the buffers are 0V - 0.3V (binary 0) and $19 \pm 1V$ (binary 1).

- NOTES:
1. PARTIAL REF DES ARE SHOWN. FOR COMPLETE DES PREFIX WITH UNIT NO. OR SUB-ASSY DES.
 2. UNLESS OTHERWISE SPECIFIED RESISTANCE ARE IN OHMS $\pm 5\%$ TOLERANCE, $\frac{1}{4}$ WATT.
 3. UNLESS OTHERWISE SPECIFIED, ALL DIODES ARE RAD 100G43, TRANSISTORS Q2 THRU Q15 ARE RAD 100422, Q1 IS RAD 100B18.

LAST NO. CHART	
LAST NO. UNUSED	
CR2	
R43	
Q15	

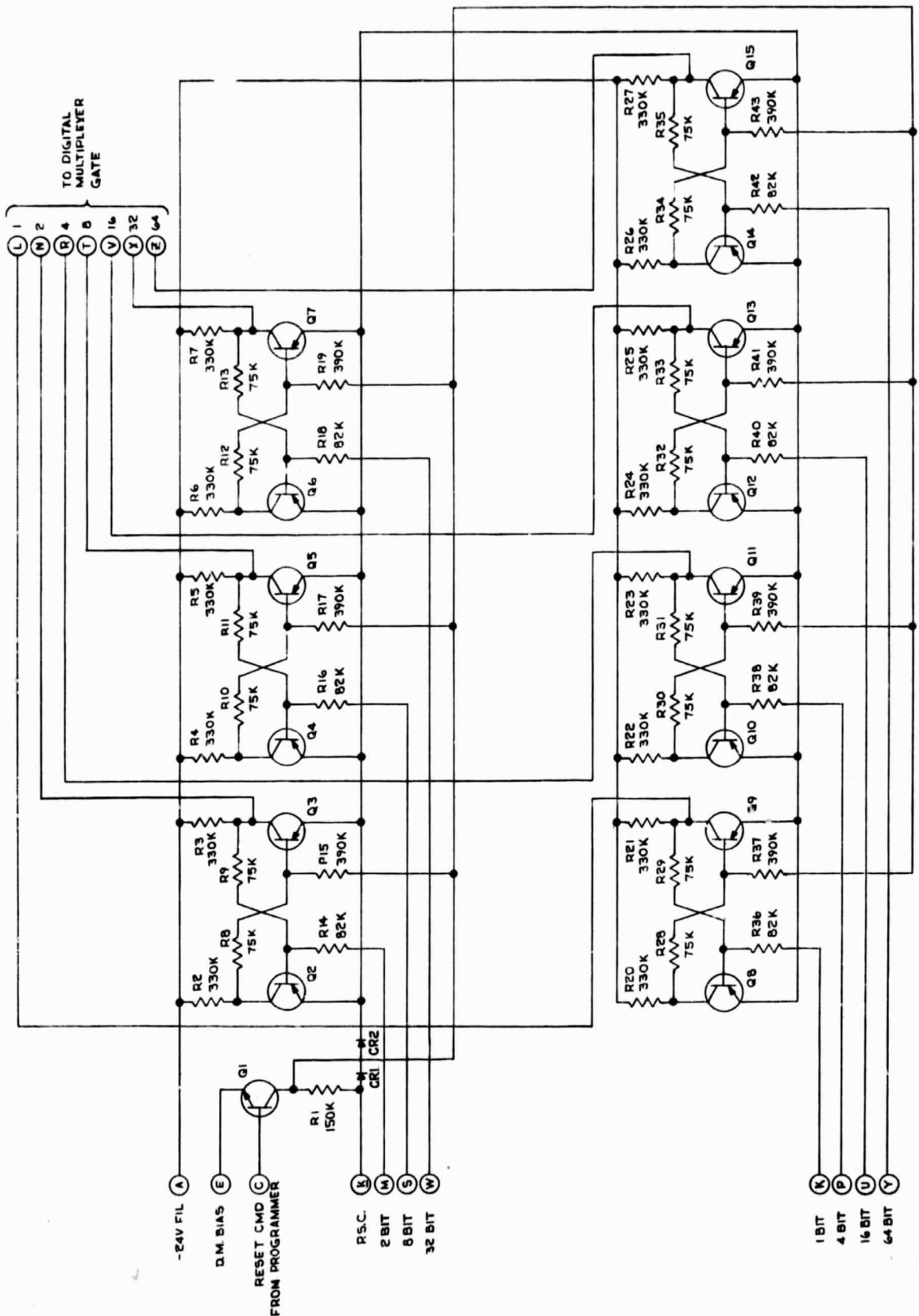
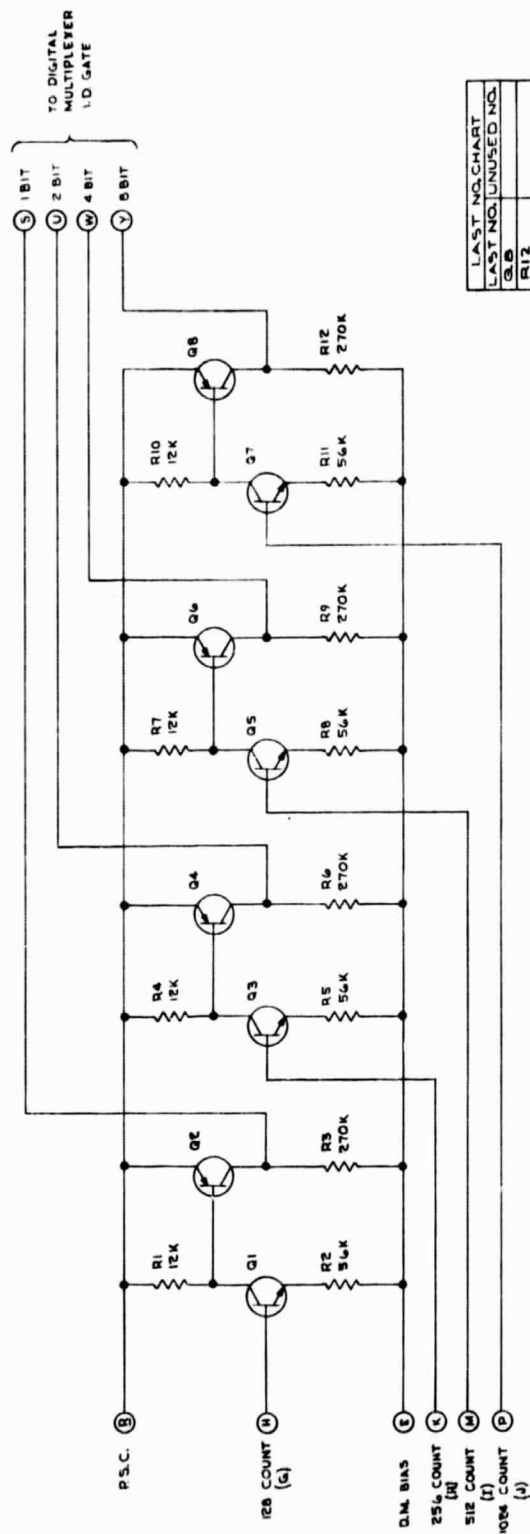


Figure 28. Transient Data Storage Schematic Diagram

- NOTES:
1. TRANSISTORS Q1, Q3, Q5, Q7 ARE 100B16; Q2, Q4, Q6, Q8 ARE 100-422.
 2. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS, 5% TOL, 1/4 W.
 3. PARTIAL REF. DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION PREFIX WITH UNIT NO. OR SUBASSY DESIGNATION.



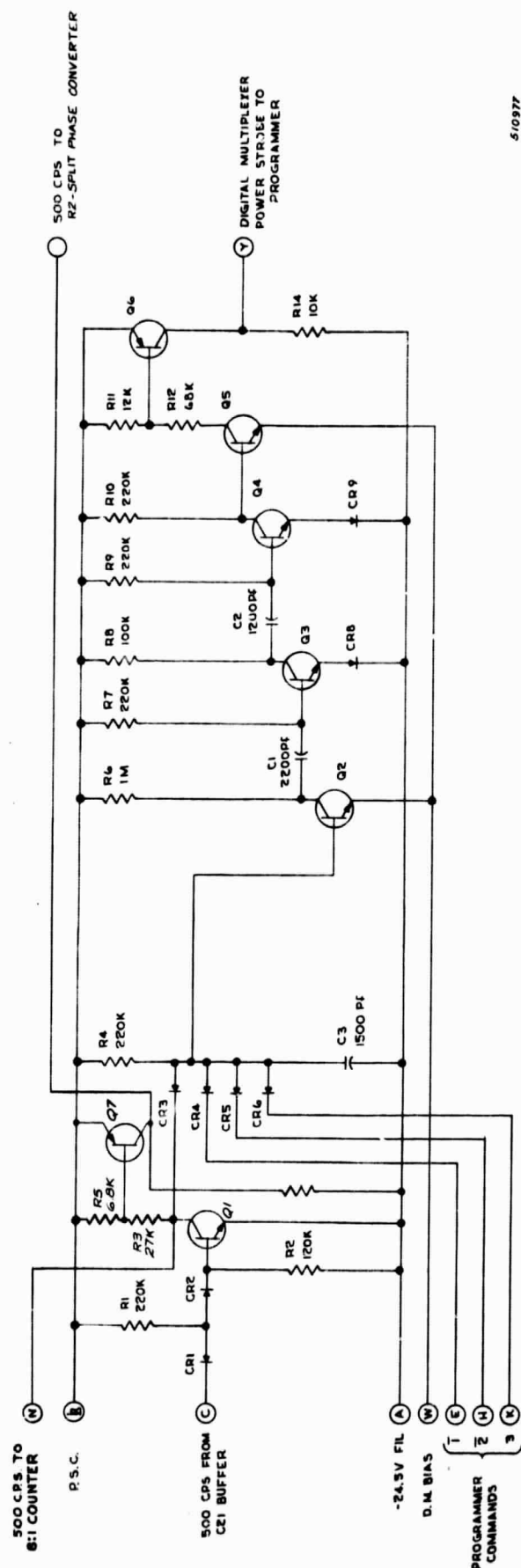
LAST NO. CHART	
LAST NO. UNUSED NO.	
G. 9	
R. 12	

Figure 29. Identification Format Buffers

1.7.1 Digital Multiplexer Power Strobe. - The digital multiplexer power strobe (figure 30)

functions as a delayed pulse to the matrix gates controlling the digital multiplexer. The delay of approximately 300 us prevents storing data in the output shift register while other data is being shifted and transferred. The strobe to the matrix gate resistors decreases the power consumption while reducing the number of diodes in the matrix. The circuitry consists of a 500 cps buffer, a four input AND gate-inverter, a 300 us delay half shot, a 200 us strobe half shot and a strobe buffer. The AND gate-inverter and buffer provide a one msec trigger pulse to the half shot during bit four of the programmer word. The inverter also provides a 500 cps square wave signal to the counter string. The 300 us delay half shot C1, R7, R8, Q2, and CR8 allows the strobe to always occur after the shift and transfer pulses. The delay provides a 150 usec safety factor between the trailing edge of the transfer pulse and the beginning of the strobe pulse. The pulse width is determined by the R_7C_1 time constant and is not particularly critical other than being greater than the shift and transfer pulse widths. Diode CR8 prevents current from flowing in the reverse direction should the base-emitter junction of Q3 break down. The 200 us strobe half shot C2, R9, R10, Q4, and CR9 is identical to the delay half shot except different component values are used to obtain the reduced pulse width. The strobe buffer Q5, Q6, R11, R12, R14, is a two stage non-inverting driver with both transistors normally off. When the half shot output goes positive both transistors saturate. The output is then clamped to power supply common through

- NOTES:
1. PARTIAL REF DES ARE SHOWN. FOR COMPLETE DES PREFIX WITH UNIT NO. OR SUB ASSY DES.
 2. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS $\pm 5\%$ TOLERANCE, $\frac{1}{4}$ WATT, CAPACITANCE VALUES ARE EXPRESSED IN PICOFARADS.
 3. UNLESS OTHERWISE SPECIFIED, ALL DIODES ARE RAD 100G13, TRANSISTORS Q1 THRU Q5 ARE RAD 100B17, Q6 IS RAD 100A22, Q7 IS RAD 100A22.



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Q6. The output is common to all the matrix gate resistors supplying current to the digital multiplexer. Selection of 200 μ s for the strobe width was based on providing sufficient time to charge the stray capacitance in the programmer and gate drivers, and to allow adequate time to set the shift register cores. The strobe buffer, being essentially a power driver, was designed using the complementary scheme to conserve power by keeping both stages off during the non-strobe time. Since the duty cycle is 1.25% this approach effects a considerable power savings.

1.7.2 Coder Control. - The coder control circuit (figure 31) provides the inhibited code command to the encoder power supply. By preventing power from being applied to the encoder, digital words can be inserted into the format in place of the inhibited analog words. The circuit used to prevent activating the pulse power supply consists of a bistable, AND gate, and inverter. The pulsed supply is triggered by the negative transition of the word rate signal. The method of inhibiting was, therefore, designed to prevent any unwanted negative transitions from reaching the power supply. By setting the flip-flop during the negative half cycle of the (-) word rate input, the AND gate command is clamped to the digital multiplexer bias thereby keeping the inverter transistor off. If the flip-flop is in the reset state, the bistable input to the AND gate is positive and the transition from the negative half cycle to the positive half cycle of word rate causes the inverter transistor to saturate and activate the pulsed power supply. The bistable and inverter are referenced to the digital multiplexer bias since they are commanded from the matrix and the (-) word rate buffer. The bistable is direct coupled to accept the

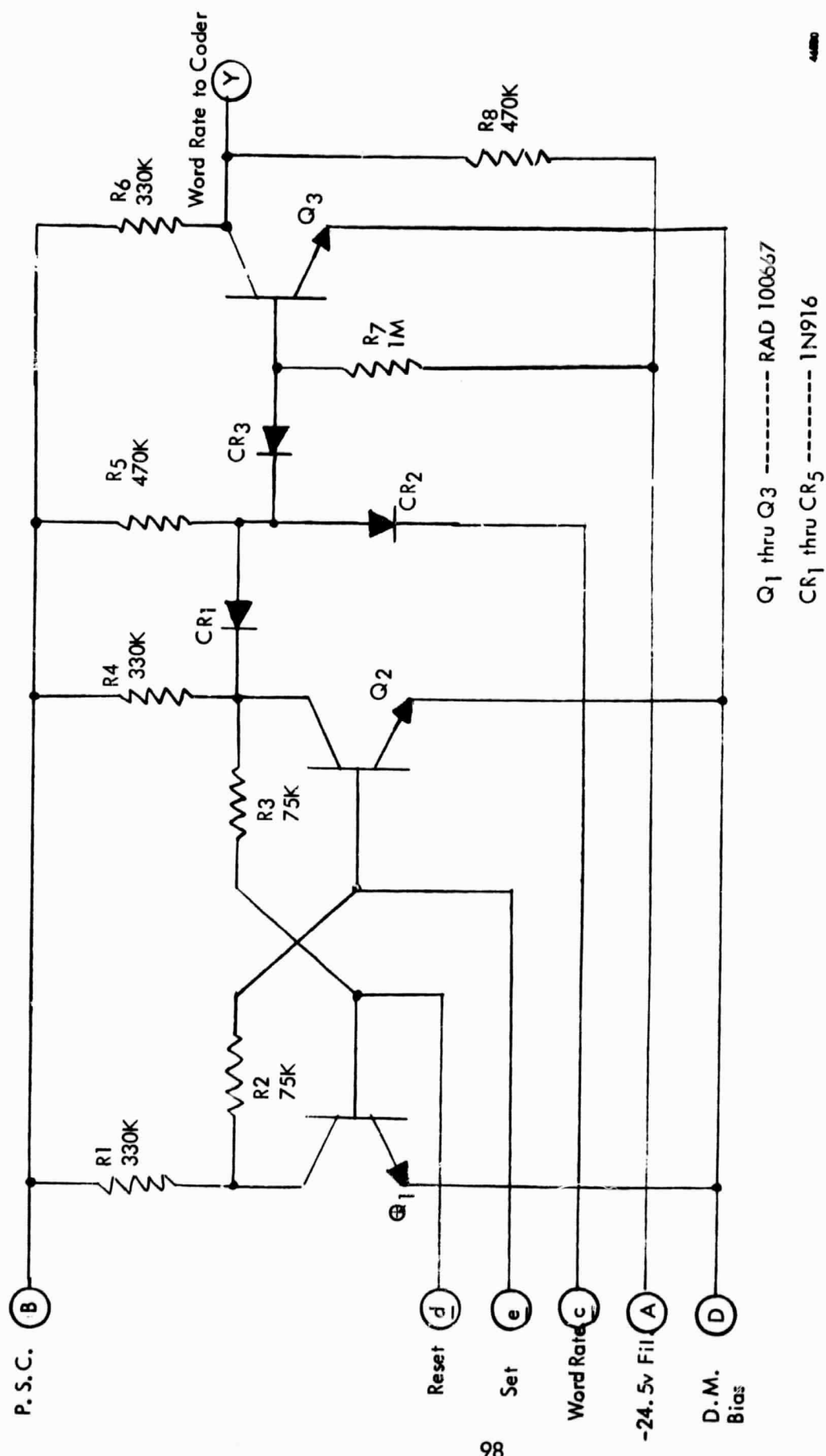


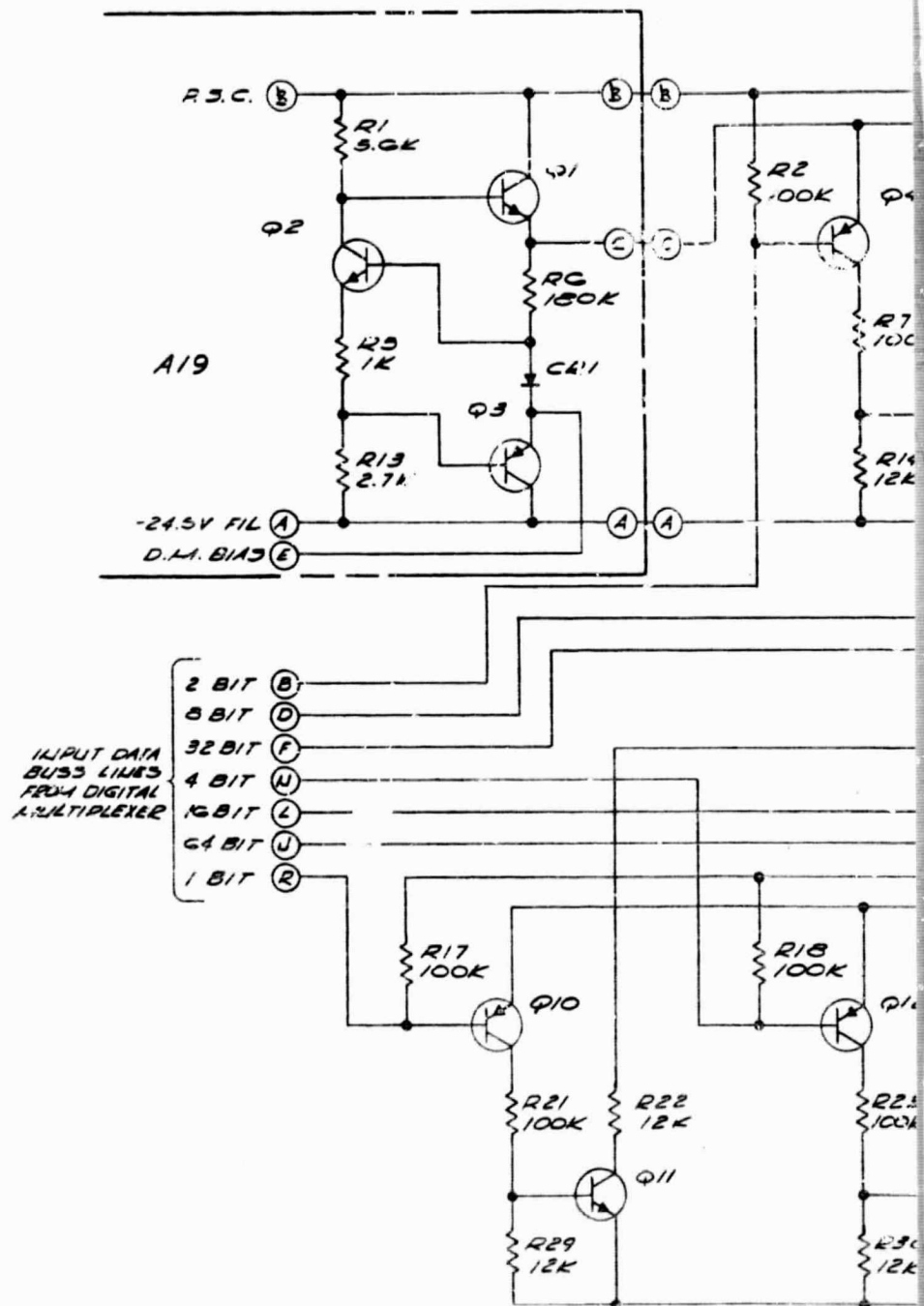
Figure 31. Coder Control Schematic Diagram

two msec set and reset pulses directly from diode matrix gates. The inverter output is clamped on the up level by the resistive voltage divider R6 and R8 in order to maintain the same trigger amplitude used in the present system.

1.7.3 Bias Amplifier. - The bias amplifier (A19, figure 32), provides a reference bias voltage to the seven core drivers and a second bias level to the digital multiplexer gates and other circuits.

1.7.3.1 The reference bias voltage is used in the core drivers to allow detection between binary "1" and "0" of the digital data. The reference level is adjusted such that a binary "0" will never turn on the PNP input stage due to the emitter always being at a more negative potential in respect to the "0" input level at the base. A binary 1 will always turn on the PNP stage because the reference level is more than the "1" level to the base. The second bias level designated the digital multiplexer bias provides a positive voltage in reference to the -24V filtered line. The positive voltage is necessary when using diode - resistor logic to allow turn off of the transistors driven from the matrix gates. In the present programmer scheme a maximum of three diodes energy gaps plus $V_{CE SAT}$ of the counter transistor must be compensated to permit logic operation.

1.7.3.2 The configuration selected to obtain the two bias levels has several unique features. It is basically two emitter followers and a constant current source. The current source consists of Q2, Q3, R5, and CR1. The constant current is pulled through resistor R1 to provide the reference



NOTES:

1. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS, $\pm 5\%$ TOL., $\frac{1}{4}$ W.
2. UNLESS OTHERWISE SPECIFIED, Q4, Q6, Q8, Q10, Q12, Q14, Q16 ARE 100422, Q1, Q2, Q5, Q7, Q9, Q11, Q13, Q15, Q17 ARE 100823, Q3 IS 102258, Q1 IS 100613.
3. PARTIAL REF DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NO. OR SUBASSY DESIGNATION.

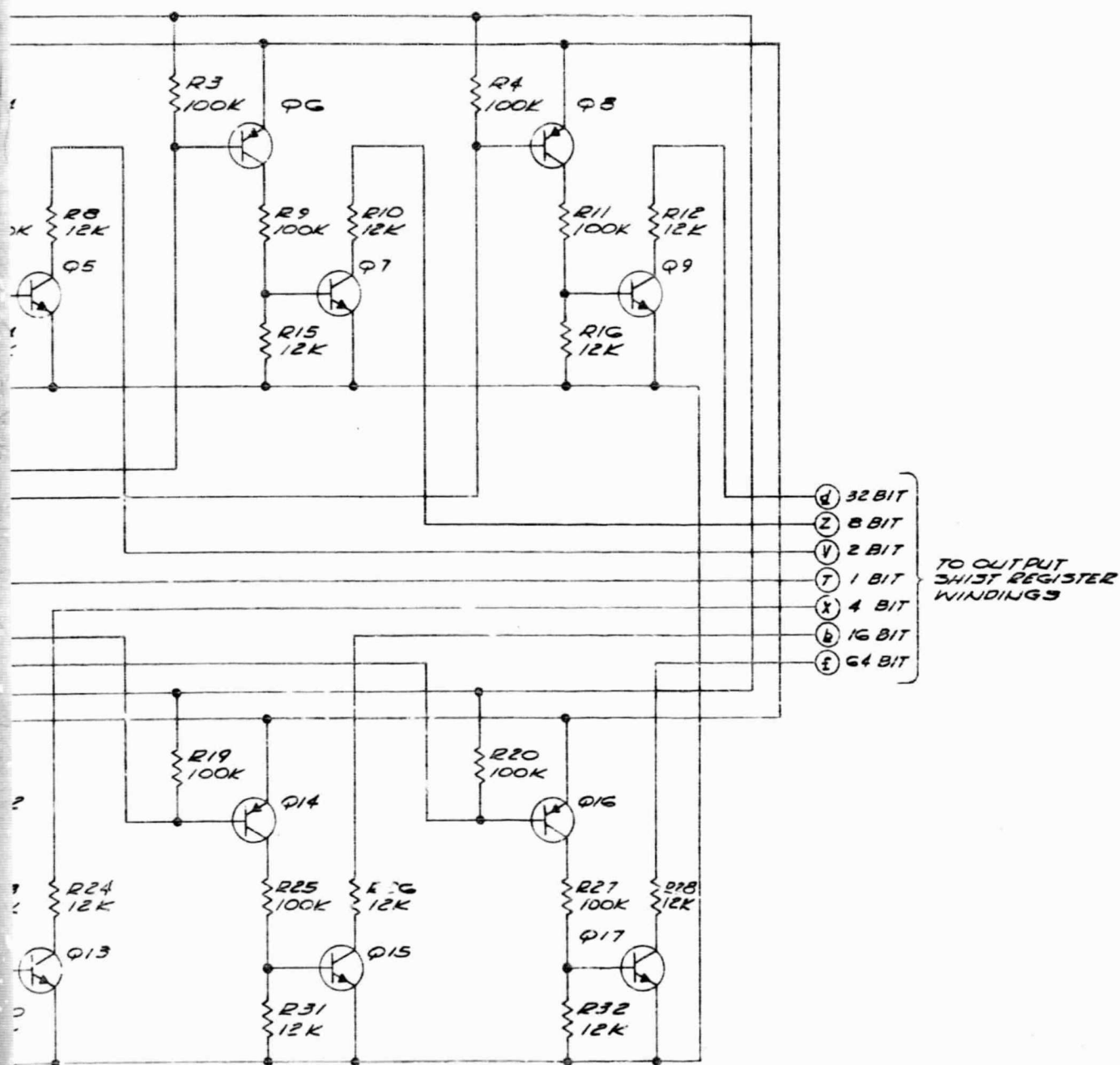


Figure 32. Bias Amplifier and Core Drivers Schematic Diagram

bias voltage which is buffered by the emitter follower Q1. The same current also flows through R13 to develop the digital multiplexer bias voltage which is likewise buffered by the emitter follower Q3. The circuit can be easily adjusted for different levels by changing the resistor values of R1, R5, and R13. In addition to providing two adjustable levels with a minimum of components the circuit has acceptable temperature and load stability without the use of zener diodes or differential feedback amplifiers. The reference bias voltage is described by the equation:

$$E = -V_{BE1} - R_1 \left(\frac{V_{BE3} + V_{CR1} - V_{BE2}}{R_5} \right)$$

$$E = -V_{BE1} - \frac{R_1}{R_5} (V_{CR1})$$

This voltage (E) has a positive temperature coefficient of:

$$\frac{(R_1 + 1)}{(R_5)} (1.8) \text{ mv}/^{\circ}\text{C}$$

and a dynamic output impedance of:

$$\frac{E}{I_o} = \frac{R_1}{h_{FE1}}$$

The digital multiplexer bias voltage is described by the equation:

$$E' = -24.5V (\text{Fil.}) + R_{13} \left(\frac{V_{BE3} + V_{CR1} - V_{BE2}}{R_5} \right) + V_{BE3}$$

$$E' \approx -22 + \frac{R_{13}}{R_5} (V_{CR1}) + V_{BE3}$$

The voltage (E') has a negative temperature coefficient of approximately:

$$\frac{(R_{13} + 1)}{(R_5)} (1.8) \text{ mv}/^{\circ}\text{C}$$

and a dynamic output impedance of:

$$\frac{E}{I'_o} = \frac{R_{13}}{h_{FE3}}$$

The above equations are approximations since the following assumptions were applied:

$$V_{BE1} = V_{BE3}$$

$$V_{BE1} = V_{BE3} \quad (\text{temperature and load})$$

$$I_c \gg I_{B1}$$

$$I_c \gg I_{B3}$$

where I_c - constant current

$$I_{B1} = \text{base current of Q1}$$

$$I_{B3} = \text{base current of Q3}$$

$$h_{FE} \gg 1$$

1.7.4 Core Drivers. The seven core drivers (figure 32) replace the present modules C20 and C17 for driving the sync windings of the output shift register. The sync windings can then be used to insert all the digital data into the output format. The core drivers are similar to the previous drivers except for the PNP input stage required by the logic levels. As explained in the bias amplifier section, the core driver detects the logic differences by biasing the emitter of the input such that a "0" never turns on the PNP transistor and a "1" always turns on the transistor. A two stage configuration was chosen for the driver primarily because of the high leakage currents of the 2N722 and proven results with the previous drivers. The leakage of the 2N722 was felt to be high enough to possibly set the core using a one stage arrangement with the core winding as a collector load instead of the second stage. Another factor is the noise that would be put on the reference bias line since two ma set current is used. By using the two stage scheme the set current is supplied by the output NPN and does not affect the bias. The previous Nimbus drivers also used this arrangement (NPN core drivers) thereby allowing a minimum change to the package with this modification. In the quiescent mode both transistors are off with the base of the input stage back biased to 0V for noise immunity. When a "1" is read into the driver from the digital multiplexer gate, the PNP input saturates supplying base current to the NPN output. The output stage also saturates drawing approximately two ma through the 12K collector resistor and the shift register winding. The winding is tied to power supply common to complete the collector circuit loop.

1.7.5 Programmer Counters. The three stage 8:1 counter (figure 33) and the ten stage multiplexer synchronizer (figure 34) provide the basic timing signals to the programmer matrix and to the analog multiplexer for generating the desired PCM format.

1.7.5.1 The design of the counter stages consisted of modifying the existing stages by changing the components and by adding circuits to provide reset. In the original configuration the counter stages were not identical. To insure more uniform characteristics it was decided to make the new counter string from one basic bistable design. Since the counter outputs now feed diode matrix gates, it is important that transition times and delays of the stages be consistent, otherwise the possibility of generating noise spikes in the gates is increased. The addition of the reset inputs to the first six stages in figure 34 is to provide the 62.5 word format. Since the 8:1 counter already had reset inputs it was only necessary to change the value of the input resistor from 220K to 100K. The last four stages of the multiplexer synchronizer are not reset since they only serve to count the 16 frames of the output format.

1.7.5.2 The modifications made to the existing Nimbus PCM Synchronizer Counter design were the changing of all transistors to RAD 100667, all collector and base cross-over resistors to 82K, all steering resistors to 560K, all diodes to RAD 100613, and all trigger capacitors to 390 pf. The configuration was also modified by eliminating the 220K base-emitter resistors

LAST NO CHART	LAST NO UNWIND
Q8	Q8
R30	R18
C6	CR12

NOTES:

1. PARTIAL RUF DES ARE SHOWN. FOR COMPLETE DES PREFIX WITH UNIT NO. OR SUB ASSY DES.
2. UNLESS OTHERWISE SPECIFIED RESISTANCE VALUES ARE IN OHMS, 15% TOLERANCE, 1/4 WATT, CAPACITANCE VALUES ARE 390 PICOFRADS.
3. UNLESS OTHERWISE SPECIFIED, ALL DIODES ARE RAD 100G13, TRANSISTORS Q1 AND Q2 ARE RAD 100422, Q3 THRU Q8 ARE RAD 100607.

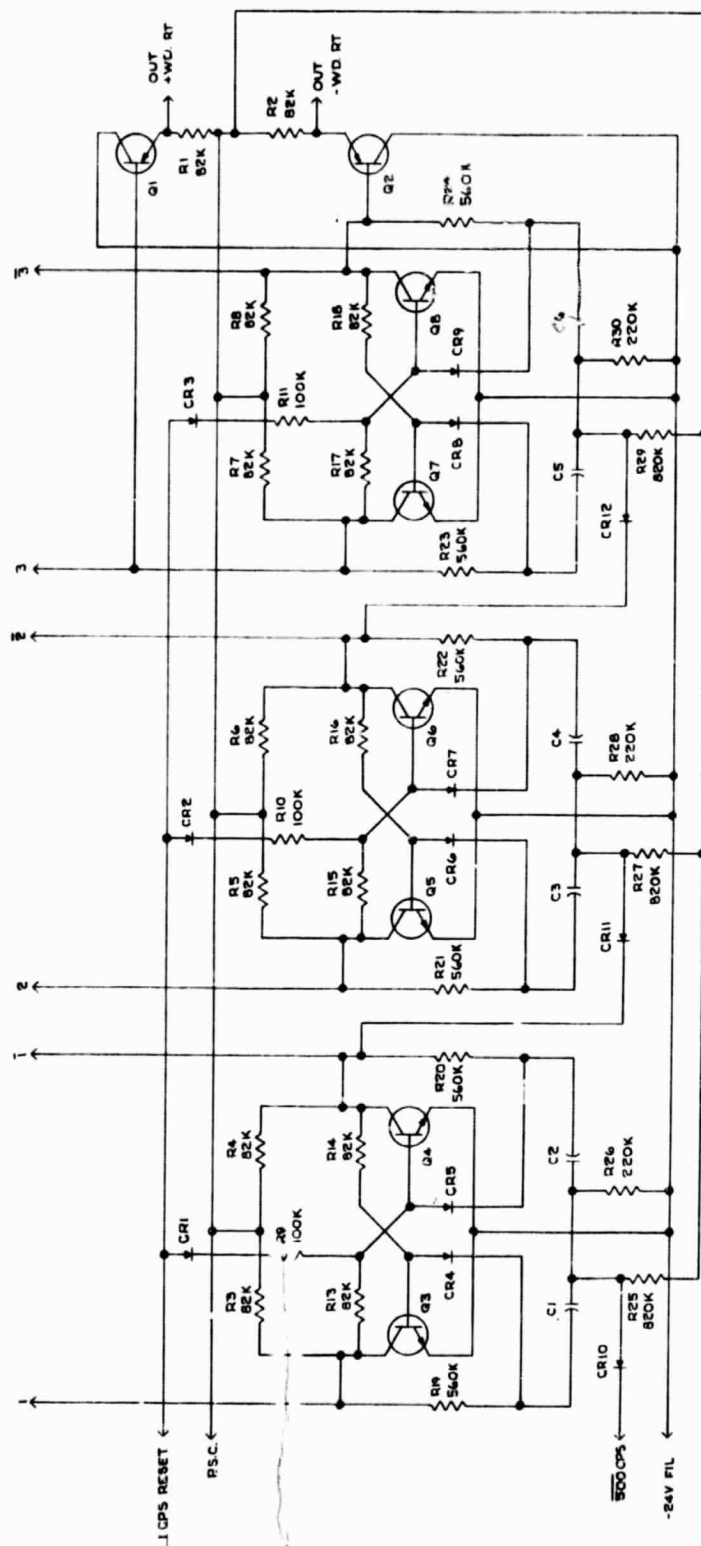
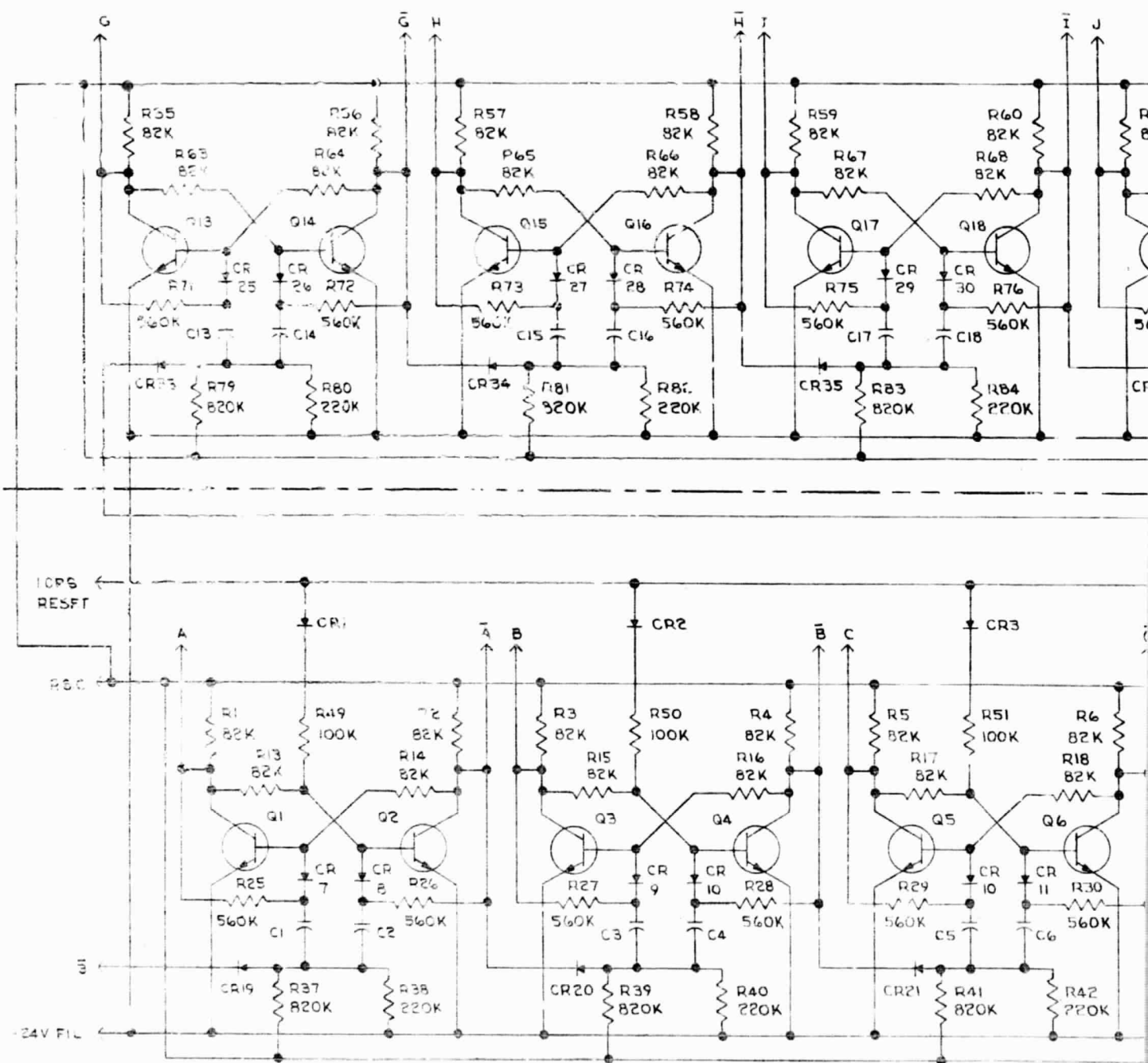


Figure 33. Programmer 8:1 Counter Schematic Diagram

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NOTES:

1. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS $\pm$ 5% TOLERANCE, 1/4 WATT
2. UNLESS OTHERWISE SPECIFIED, DIODES ARE RAD 100613,
TRANSISTORS Q1 THRU Q20 ARE RAD 100667.
CAPACITORS C1 THRU C20 ARE 390PF.
3. PARTIAL REF DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NO. OR SUBASSY DESIGNATION.

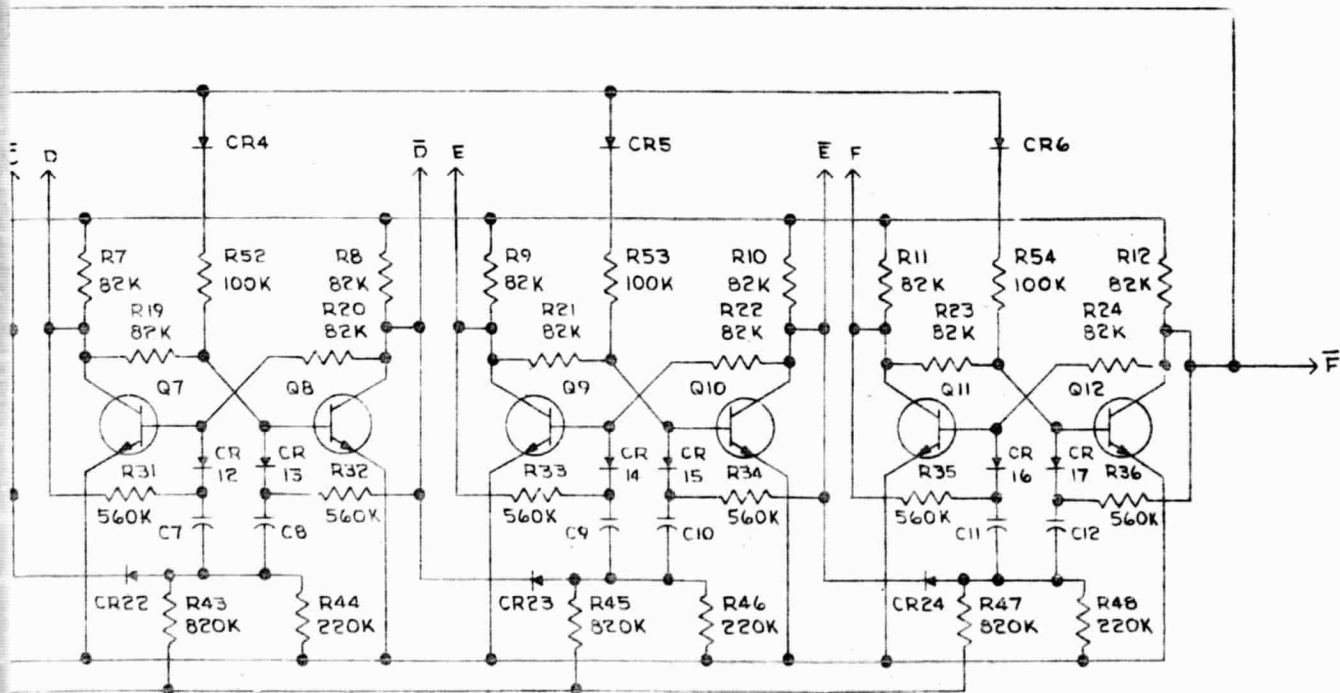
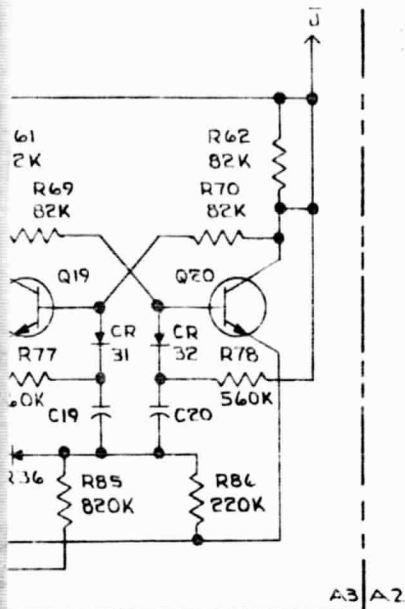


Figure 34. Unit A Multiplexer Synchronizer A2 and A3 Schematic Diagram

since the I_{CBO} leakage of the RAD 100667 units is sufficiently small. The speed up capacitors in the 8:1 counter were removed as unnecessary to the operation of the circuits in view of the faster transistors. In some stages, a resistor was in series with the feed forward lead. This resistor was removed and all stages were coupled through diode isolation circuits. The two reasons for coupling forward by this method was to allow dropping the voltage swing on the trigger capacitor from 11V to 4V and to isolate the collectors from the capacitive load of the trigger circuits. The four volts swing will not breakdown the base-emitter junctions, thereby increasing the reliability of the circuit.

1.7.6 Additional Multicoder Modification Requirements for Digital Inputs Compatibility.

A number of other modifications on the multicoder itself were required for compatibility with the digital inputs. These are listed below and described in succeeding paragraphs:

- a. Matrix drivers.
- b. Shift register.
- c. Sync word generation.
- d. Unit A programmer.
- e. Word rate counter.

1.7.6.1 The matrix drivers were modified to make the analog multiplexer matrix row drivers compatible with the 62.5 word subframe. Row 16 drivers in both the A and B matrices are in the SET condition at the time the

synchronizer counts are reset by the one cps subframe reset pulse. The result of this is that row 16 is read out at the same time as row one of the next subframe. Since row 16 of these matrices is not used in the 62.5 word subframe, the condition was corrected by terminating the "D" and "E" register shift pulses at the end of row 15. The following procedure was used:

- a. A connecting ribbon was welded from pin 7 of T2 to pin 8 of T2 on the M36 module (D501249) used in the "D" register.
- b. A connecting ribbon was welded from pin 7 of T2 to pin 8 of T2 on the M16 module (D50144) used in the "E" register.

1.7.6.2 The shift register was modified to provide a means of inserting the data from the digital multiplexer core drivers into the output shift register of the present A to D converter. In order to accomplish this, the present subframe gate modules C17 and C20 were removed from card 5B and the shift register core windings previously used for subframe identification were used for setting the digital data into the register. The printed circuitry on card 5B was changed to connect C26-26 to #2, C25-7 and 20 to power supply common. Except for the connections listed below, all other connections remain unchanged. Printed circuitry for modules C17 and C20 is no longer required.

NOTE

No. 1, C25 is the C25 which formerly had pin 31 connected to C17-11.

<u>Shift Register</u>	<u>Core Drivers</u>
#1, C25-31	1 bit output
#1, C25-18	2 bit output
#1, C25-5	4 bit output
#2, C25-31	8 bit output
#2, C25-18	16 bit output
#2, C25-5	32 bit output
C26-24	64 bit output

1.7.6.3 The sync word generation circuit was modified to provide a means of inserting a logic "1" bit into the 128 bit core of the output shift register during multiplexer time slot 2 for purposes of generating the Nimbus B frame sync word. This is accomplished by replacing Module M8 in the "C" register with an M31 module and connecting the coder command output from M31-4 to the coder command output from M31-4 in the "B" register. This will insert a "1" bit for the first two words of each sub-frame. The procedure follows:

a. Remove module M8 on card 9A and replace it with an M31 module.

(Pin layout is the same for both modules.)

b. Remove the wire on the internal harness from P2Y-17 to P19Y-31 and install a wire from P2Y-17 to P19Y-28.

1.7.6.4 Unit A programmer is modified to provide synchronizer counts to the digital multiplexer section from the counters presently used in the analog synchronizer and to provide a reset line to the counters in order to synchronize the counts to the one cps rate of the master clock. The count outputs from the synchronizer to the analog multiplexer will remain the same, i. e., both sides of the 2, 4, 64, 512, and 1024 counts. In addition to these counts, the digital multiplexer will require both sides of the 8, 16, 32, 128, and 256 counts. A new printed circuit layout of card 10B is required to provide the following connections in addition to the present connections.

a. A common reset line from the internal connector (either P35G or P36G) to modules M23, M24, M25, and M26. This line will also be routed to the 8:1 counter on coder card 5B.

b. Six additional leads are required from P35G or P36G to M24 in order to bring out both sides of the 8, 16, and 32 counts.

c. Modules M23, M24, M25, and M26 will require new assembly drawings in accordance with new schematic drawings.

1.7.6.5 The word rate counter circuit is modified to bring out both sides of all counts in the 8:1 counter in the Unit A coder for use by the digital multiplexer to

provide a method for inserting an inverter stage between the bit rate amplifier module and the 8:1 counter, and to provide a coder control line from the digital programmer to the coder turn-on line. The procedure follows:

- a. Relay out modules C1 and C2 on card 5B to provide outputs from all counts per schematic diagram.
- b. Relay out card 5B to bring out all counts from 8:1 counter to the internal harness on P19Y or P20Y. Relay out card 5B to provide connection from internal harness to junction of C21-8 and C22-7. This is output to bit rate inverter.
- c. Relay out card 5B to bring out C1-4 to internal harness. Connection from C21-7 to C1-4 is to be eliminated. This is to provide inverted bit rate to the 8:1 counter.
- d. Remove wire on internal harness between P20Y-4 and P24Y-35. Word rate from coder control circuit in digital multiplexer will be connected to P24Y-35.

1.7 TELEMETRY ELECTRONICS. - The TIME is modified to provide a reset inhibit voltage to the multicoder unit in the event of a Master Clock failure. Under normal operating conditions, the multicoder programmer will be reset by a pulse developed from the time code frame sync word. For emergency operation, the Standby Clock will be activated to provide the 500 cps bit rate and an inhibit voltage to the time code reset gate. The synchronizer will then be reset by the 62.5 word count from the synchronizer counters.

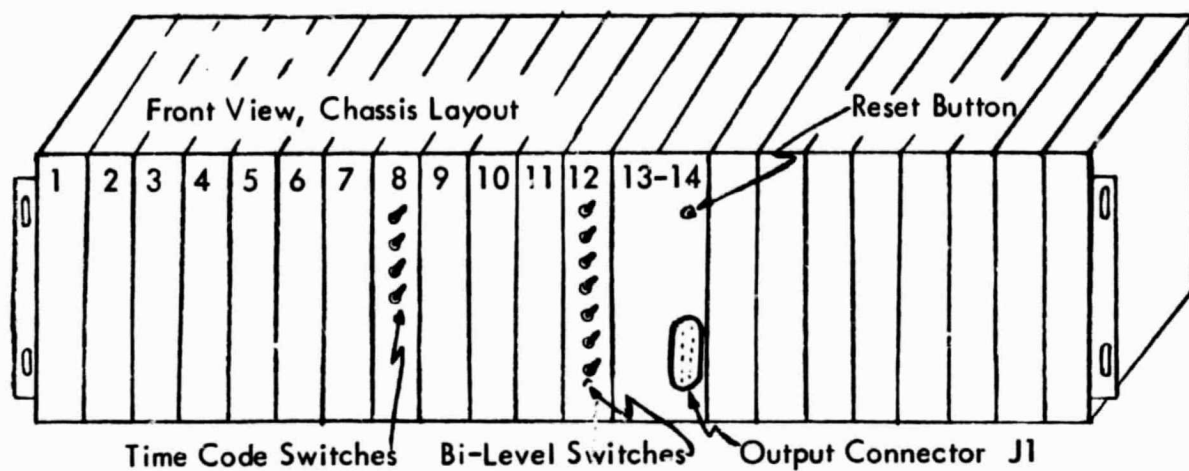
- a. Add a jumper on the TME internal harness from P2-6 to P4-2.
- b. Connect a wire on the external harness from P3-36 to multicode reset inhibit input.

1.8 BREADBOARD FOR INPUT TEST EQUIPMENT. - The Time Code and Digital Simulator has two principal purposes; first, to provide signals to simulate the pulse width modulated time code signal and the 100 cps square wave from the Nimbus Spacecraft Clock, and second, to provide simulated transducer inputs to the digital bi-level channels and the digital transient data storage channels.

1.8.1 Operation and Interface. - (See Figures 35, 36, 37, and 38) Logic functions to provide proper timing of the simulated clock signals are provided by standard logic cards of the same type that are used in the PCM Test Set, RAD 600436. Drawings and circuit descriptions of these cards can be found in Section 5 of the Radiation Incorporated Nimbus PCM Test Set Instruction Manual.

1.8.1.1 Cards #1, #2, and #3 are standard logic bistable cards, RAD 1290-26.

They provide the synchronizing counts for gating out the Time Code train. Card #1 is connected as a 10:1 counter and counts down the 1kc from the PCM Test Set to 100 cps. Outputs of this counter are used to provide synchronization of the 100 cps square wave YA1 output and the 2 millisecond "0" bit of the Time Code which occur at the 100 cps rate. Card #2 is a 10:1 counter which counts the 100 cps down to the 10 cps Time Code word rate. Outputs from this card are used to gate the Time Code data bits into the Time Code output stage. These bits, which occur as the first, second, third,

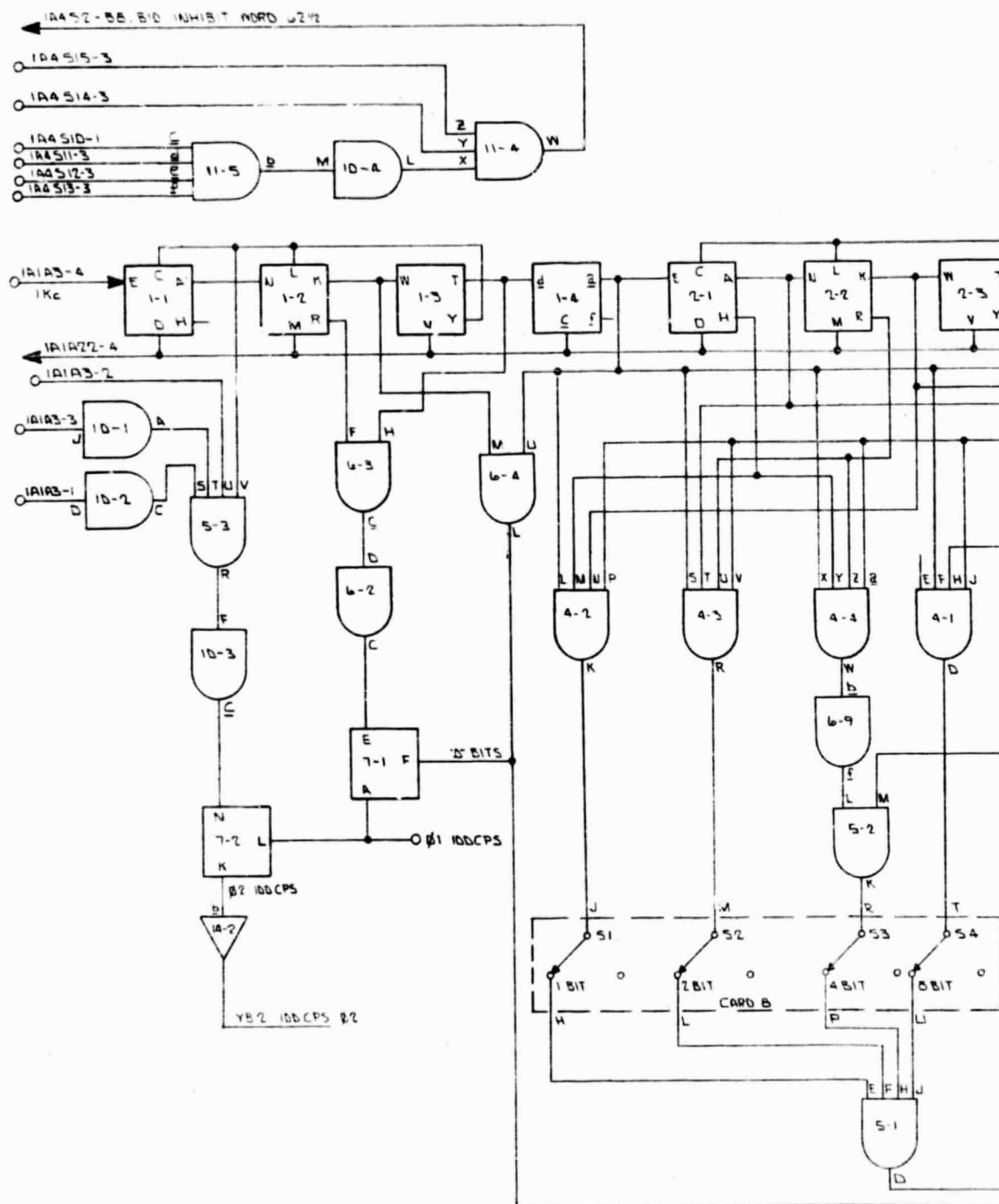


Card	RAT Number	FUNCTION
1	1297-26	Bistable Multivibrator
2	1297-26	Bistable Multivibrator
3	1297-26	Bistable Multivibrator
4	1297-46	Four-Input NOR
5	1297-46	Four-Input NOR
6	1297-30	Two-Input NOR
7	1297-26	Bistable Multivibrator
8	-----	Time Code Bit Switch Card
9	1297-25	Monostable Multivibrator
10	1297-30	Two-Input NOR
11	1297-46	Four-Input NOR
12	-----	Bi-Level Simulator Switch Card
13		
14	-----	Output Amplifier Card

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Figure 35. Time Code and Digital Simulator Chassis and Card Assembly

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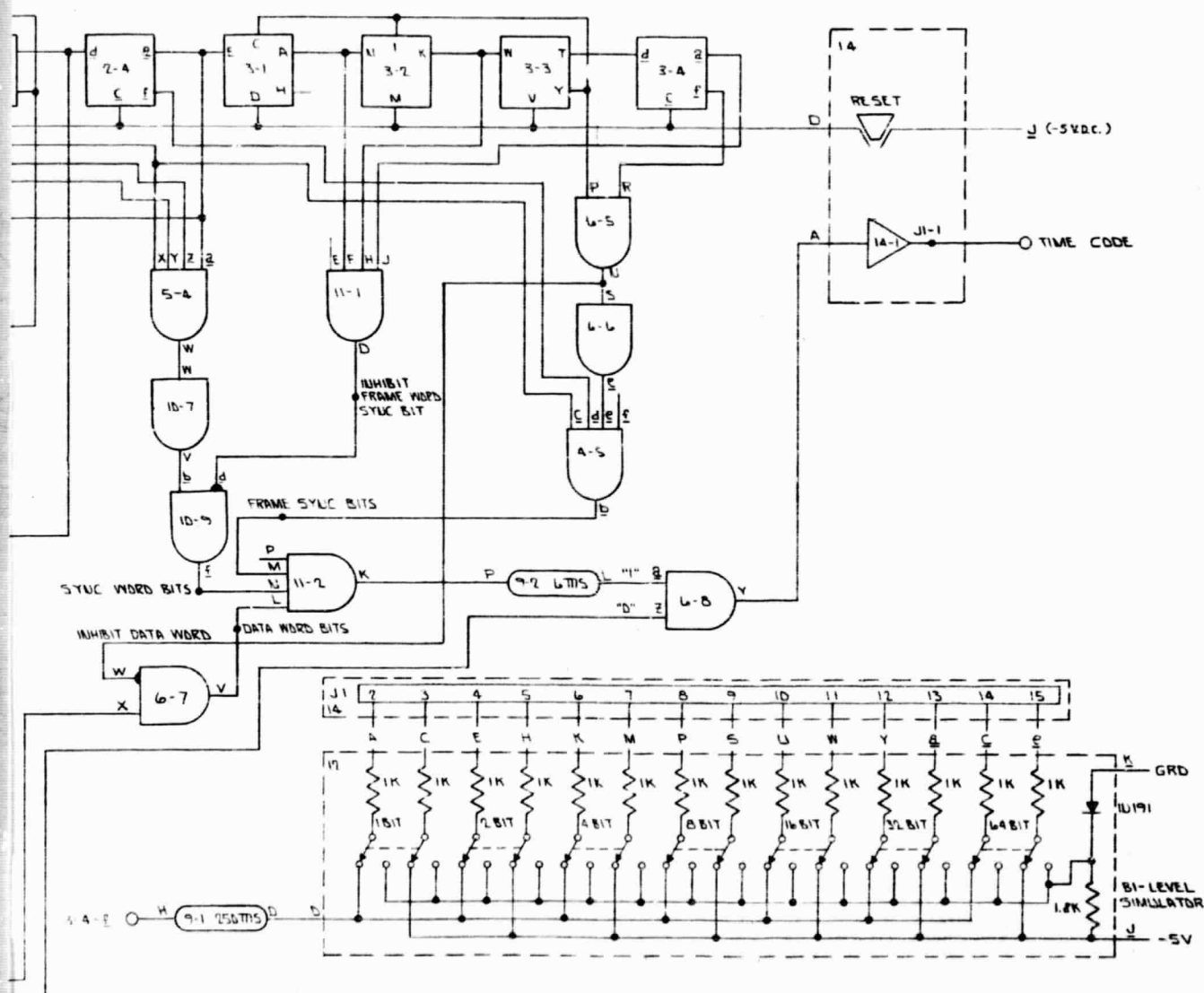


Figure 36. Time Code and Digital Simulator Logic Diagram

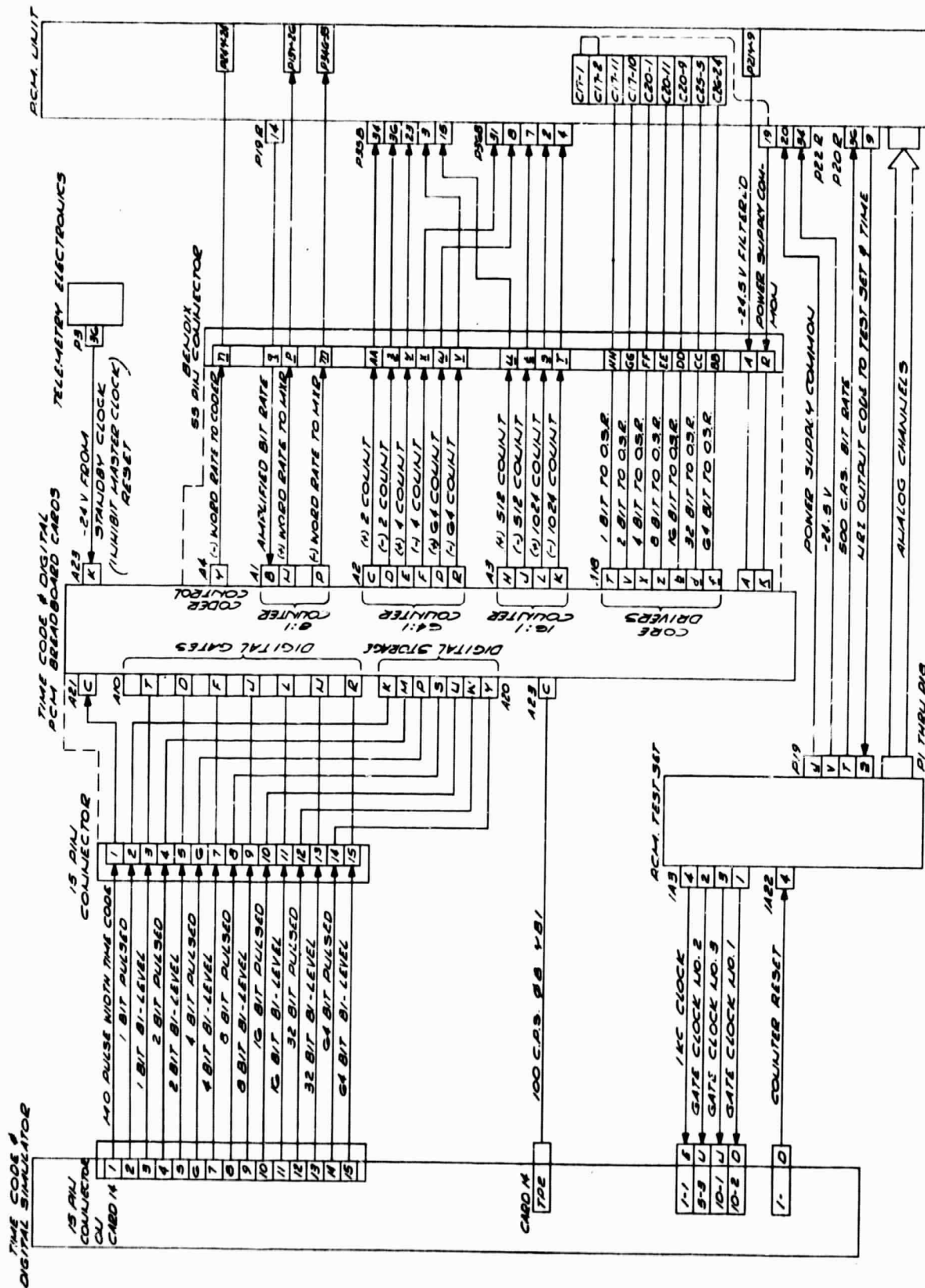


FIGURE 051

Figure 38. Interconnection Cabling Diagram for Checkout Test

and fourth bit of each word, except the frame sync word, can be selected by means of four toggle switches on card #3 to provide either a 2 millisecond "0" bit or a 6 millisecond "1" bit. The tenth bit of each word is always gated as a "1" bit except for the word following the frame sync word.

1.8.1.2 Card #3 is a 10:1 counter which counts the 10 cps down to the 1 cps frame rate. The outputs of this counter together with the word rate counter provide the timing to gate out the frame sync word which consists of "1" bits in the fifth through ninth bit positions of the frame sync word. A 6 millisecond word sync bit is provided prior to the occurrence of each time code data word following frame sync. A 2 millisecond word sync bit occurs prior to time code data word one.

1.8.1.3 The selected "1" bit gating pulses are used to drive a monostable which provides the necessary 6 millisecond "1" bit pulse width. The outputs of the "0" bit generator, card 6-4, and the "1" bit generator, card 9-2, are then fed into a NOR gate. The output of the NOR gate, 6-8, is then a continuous train of 2 millisecond "0" bit pulses at 10 millisecond intervals except during those times when the 6 milliseconds "1" bit pulses are gated in to override the "0" bits.

1.8.1.4 The 100 cps YB1 is phase shifted 90° with respect to YA1 by means of timing counts from the Radiation PCM Test Set. The 100 cps YB1 output amplifier is a single stage amplifier with a complementary emitter follower

output built on card #14. This circuit amplifies the 100 cps YBI signal to provide a positive level of 0 volts and a negative level of -23V.

1.8.1.5 The time code output amplifier provides a no load output of -5 volts during bit time and 0 volts for the no bit level. The bit level is reduced to -0.8 volt with a 600 ohm load.

1.8.1.6 The reset button on card #14 provides a reset voltage to the counter stages in the test equipment and the counters in the PCM Test Set to insure that the 500 cps bit rate from the PCM Test Set is in phase with the test equipment outputs.

1.8.1.7 The digital transducer outputs to the PCM are simulated by means of 7 dpdt toggle switches. The bilevel switch contacts are tied back to -5 volts in the up position through one K ohms to simulate a "1" bit and tied back to -1 volt in the down position through 1.2K ohms to simulate a "0" bit.

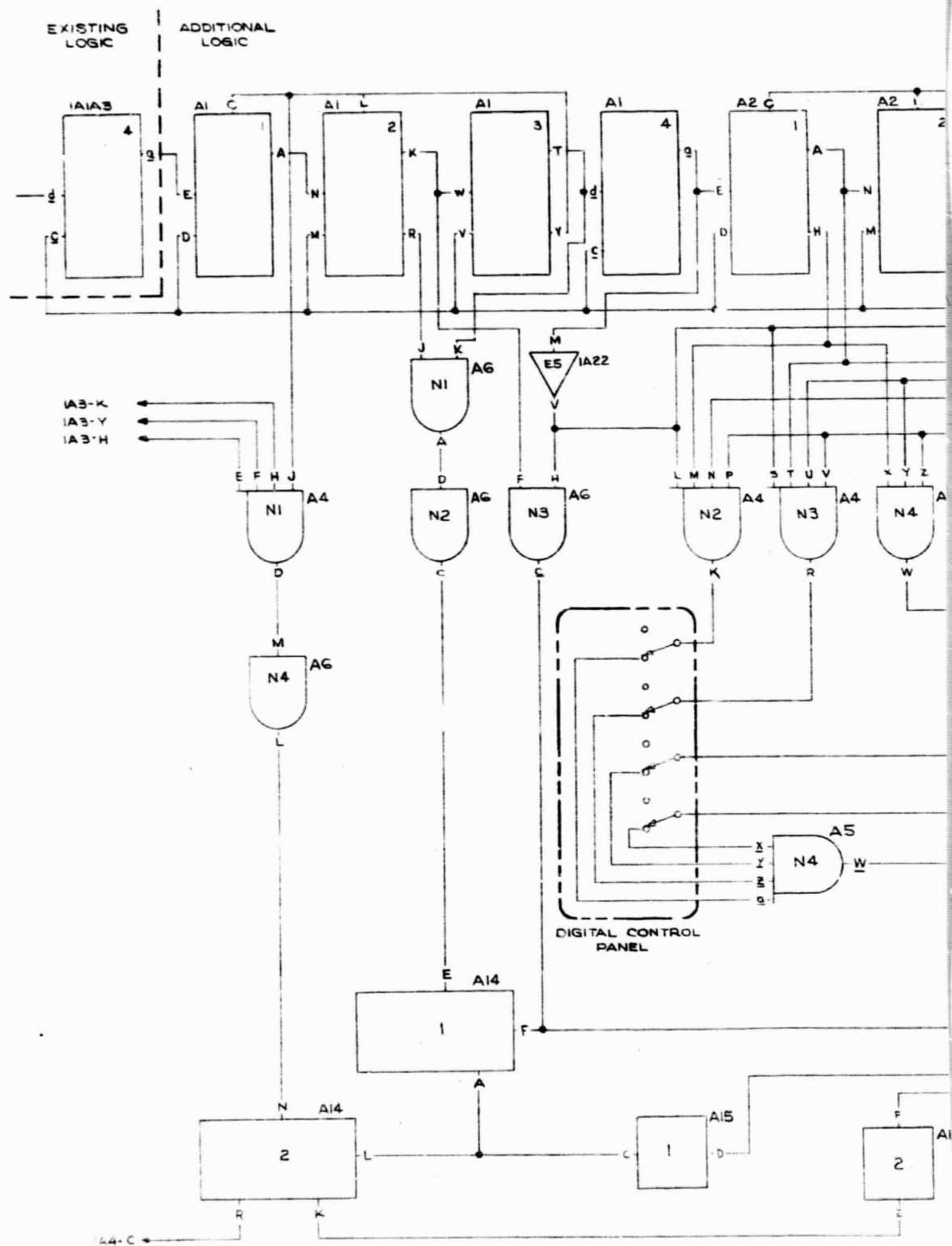
1.8.1.8 The transient data transducers are simulated by the other pole on the same switches which provide the bilevel inputs. In the UP position, this pole is tied back to the output of a 250 millisecond monostable which is activated once per second. During the ON time of the 250 millisecond monostable, a -5 volt level through a 1.0K resistor is provided through the switch to the PCM transient data storage circuits. In the DOWN position, the switch is tied to -1 volt through the 1.0K resistor. The top switch on both the time code and digital simulator cards corresponds to the least significant bit of the data word. In checking the PCM unit,

the four time code switches should not be placed in the "1" position at the same time as this results in an erroneous data word which corresponds to the time code frame sync word of five "1" bits.

- 1.9 ACCEPTANCE TEST EQUIPMENT.- The multi-coder modifications result in additional modification requirements in the Acceptance Test Equipment without changing its compatibility in respect to the existing Nimbus "A" multi-coder. Briefly, these requirements are:
- a. The addition of logic to provide a simulated Master Clock output to the multi-coder of the time code train signal (MO) and the phase B 100 cps signal (YB1).
 - b. The addition of signals to simulate the digital bilevel and digital transient data inputs to the multi-coder.
 - c. The addition of logic to recognize the new 16-bit sync word pattern.
 - d. The addition of logic to inhibit voltage comparison on the readout of the time code word 63 which is now part of the sync word.
 - e. Simultaneous display and error detection of the six time code words.

1.9.1 Simulated Master Clock Logic. -The simulated Master Clock logic is shown in figure 39. Cards A1, A2, A3 and A4 are standard logic bistable counter cards and are used to provide the synchronizing counts for gating out the time code word train. Card A1 is connected as a 10:1 counter and counts down the 1 kc from the PCM Test to 100 cps. Outputs of this counter are used to gate the time code data bits into the time code words. These data bits which occur as the first, second, third, and fourth bit of each word, except the frame sync word can be selected by means of four toggle switches, which will be located on the test set digital

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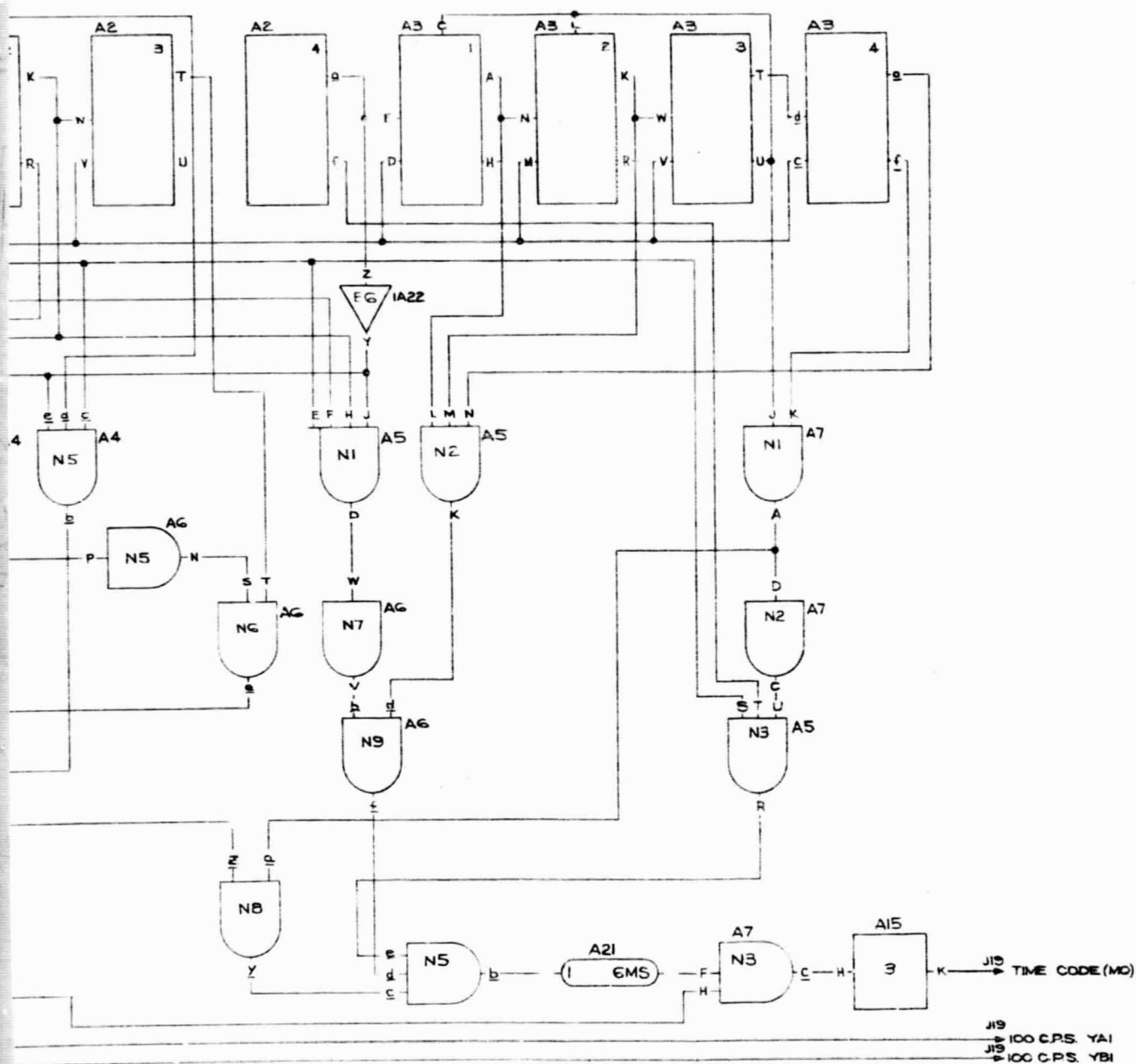


Figure 39. Test Set Clock Simulator I Logic Diagram

control panel, to provide either a 2 millisecond "0" bit or a 6 millisecond "1" bit. The tenth bit of each word is always gated as a "1" bit except for the frame sync word. Card A3 is a 10:1 counter which counts the 100 cps down to the cps time code frame rate. The outputs of this counter provide the timing to gate out the frame sync word, which consists of a "1" bit in the fifth through ninth bit positions of the frame sync word. The selected "1" bit gating pulses are used to drive a monostable that provides the necessary 6-millisecond "1" bit pulse width. The outputs of the "0" bit and "1" bit generators, cards A6-3 and A5-5 respectively, are then fed to a NOR gate. The output of the NOR gate, A7-3 is a continuous train of two millisecond intervals except during those times that a six millisecond "1" bit pulse is gated in, to override the "0" bit. The output of this Time Code train is fed to an amplifier driver on card A15. This amplifier simulates the output impedance characteristics of the Master Clock Time Code output circuit and provides a no load output level of -5 volts during bit time and 0 volts for the no bit level. The 100 cps $\phi 2$ (YB-1) is phase shifted 90° with respect to $\phi 1$ by means of timing counts from the test set counters. The 100 cps amplifiers are single-stage amplifiers with a complimentary emitter follower output. This circuit provides a positive signal level of 0 volts and a negative level of -23 volts. Signal coherency of the simulated clock outputs is shown in figure 37. The Time Code data word (figure 39) would appear in the Time Code word train in all slots. In order to provide a different word for each of the Time Code data slots readout in the Multi-coder, it is necessary to provide additional logic (figure 40). The

NOTE
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN, FOR COMPLETE DESIGNATION PREFIX WITH UNIT NO. OR SUB-ASSEMBLY DESIGNATION.

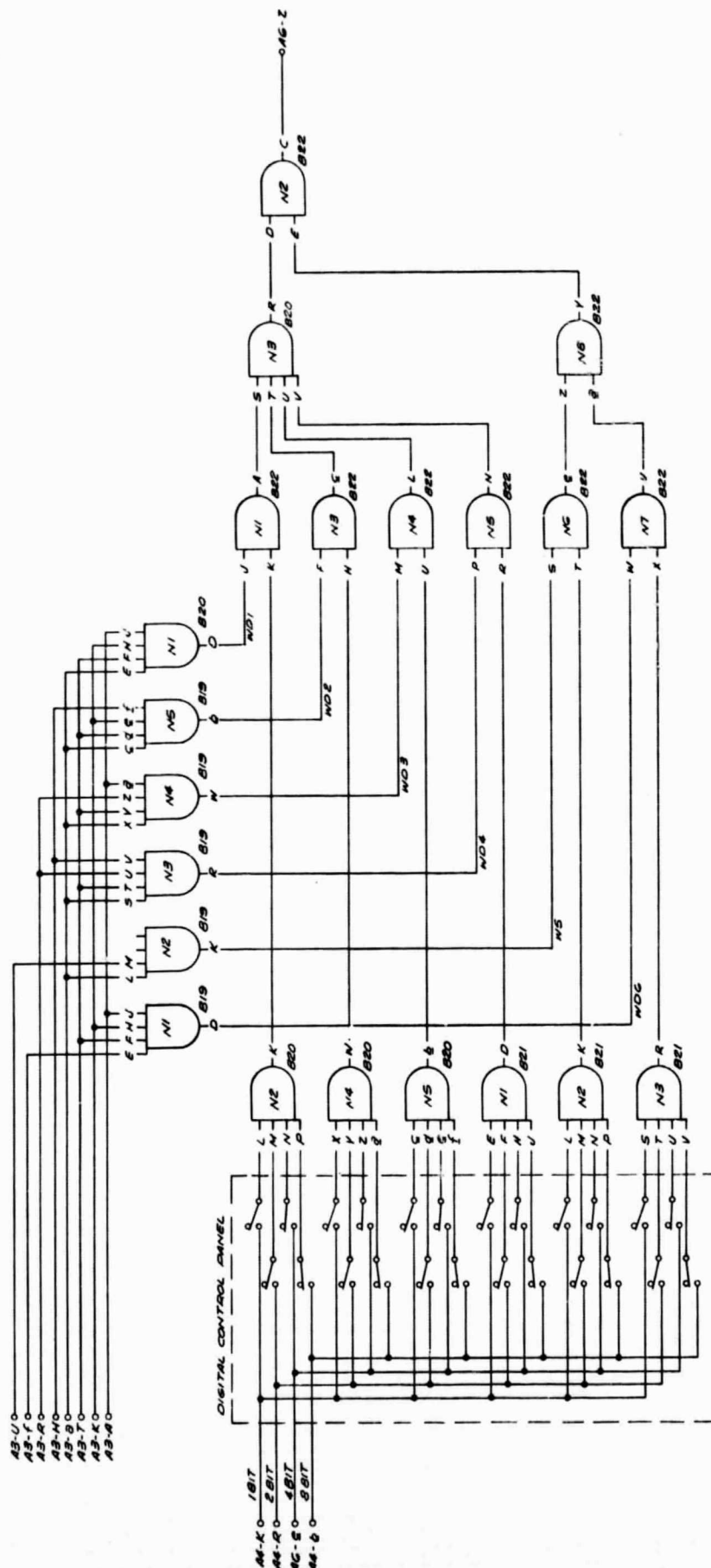
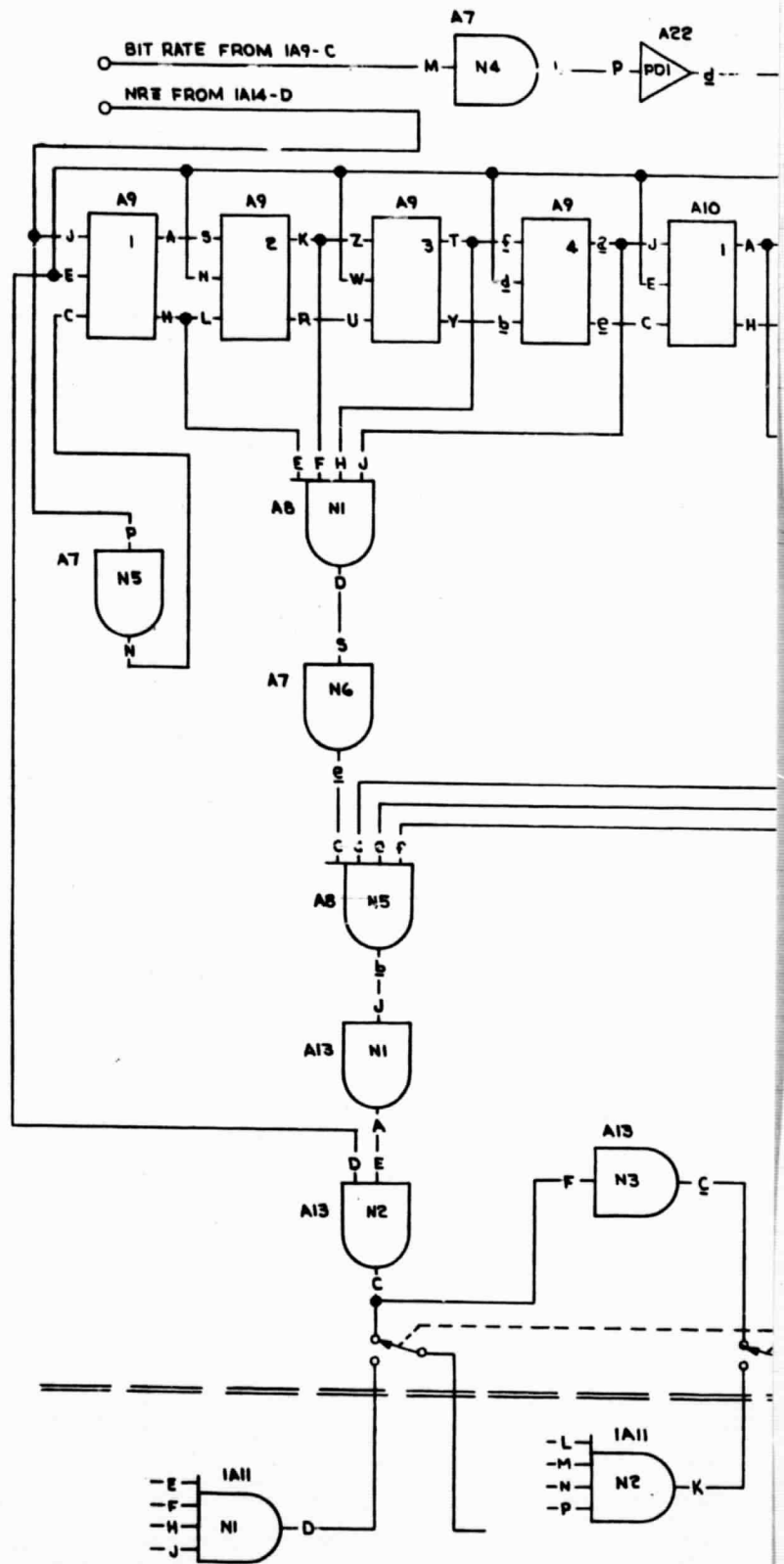


Figure 40. Test Set Clock Simulator II Logic Diagram

timing pulses for the first four bits in each word are gated into six sets of switches. Each set consists of four switches corresponding to the four data bits. When a switch is closed, the data bit will be OR gated with the other data bits in the set. This output is then AND gated with one of the six Time Code word slots. The six word slots and their selected data bits are then OR gated into the Time Code word train through gate A6-N8 as shown in figure 39.

1.9.1.1 The 16-bit sync word recognition logic is shown in figure 41. Cards A9, A10, A11, A12 are connected as a 16-bit shift register. The steering inputs of the shift register are the NRZ and inverted NRZ code from the PCM multicoder. The NRZ code is shifted into the register at the 500 cps bit rate which is coherent with the 500 cps used to generate the NRZ code. When the unique sync pattern is shifted into the register, an output sync pulse is generated by virtue of the NOR gating arrangement connected to the appropriate output sides of the register stages. When the SYNC WORD SELECT switch on the digital control panel is in the 16-bit position, this pulse is used in place of the 8-bit sync pulse to reset the test set logic to the start of the frame. The word rate counter in the test set is now reset to the one-half word position because sync recognition now occurs at the half word point of Word 2 instead of at the end of Word 1 utilized in the Nimbus "A" 8-bit sync recognition pattern.



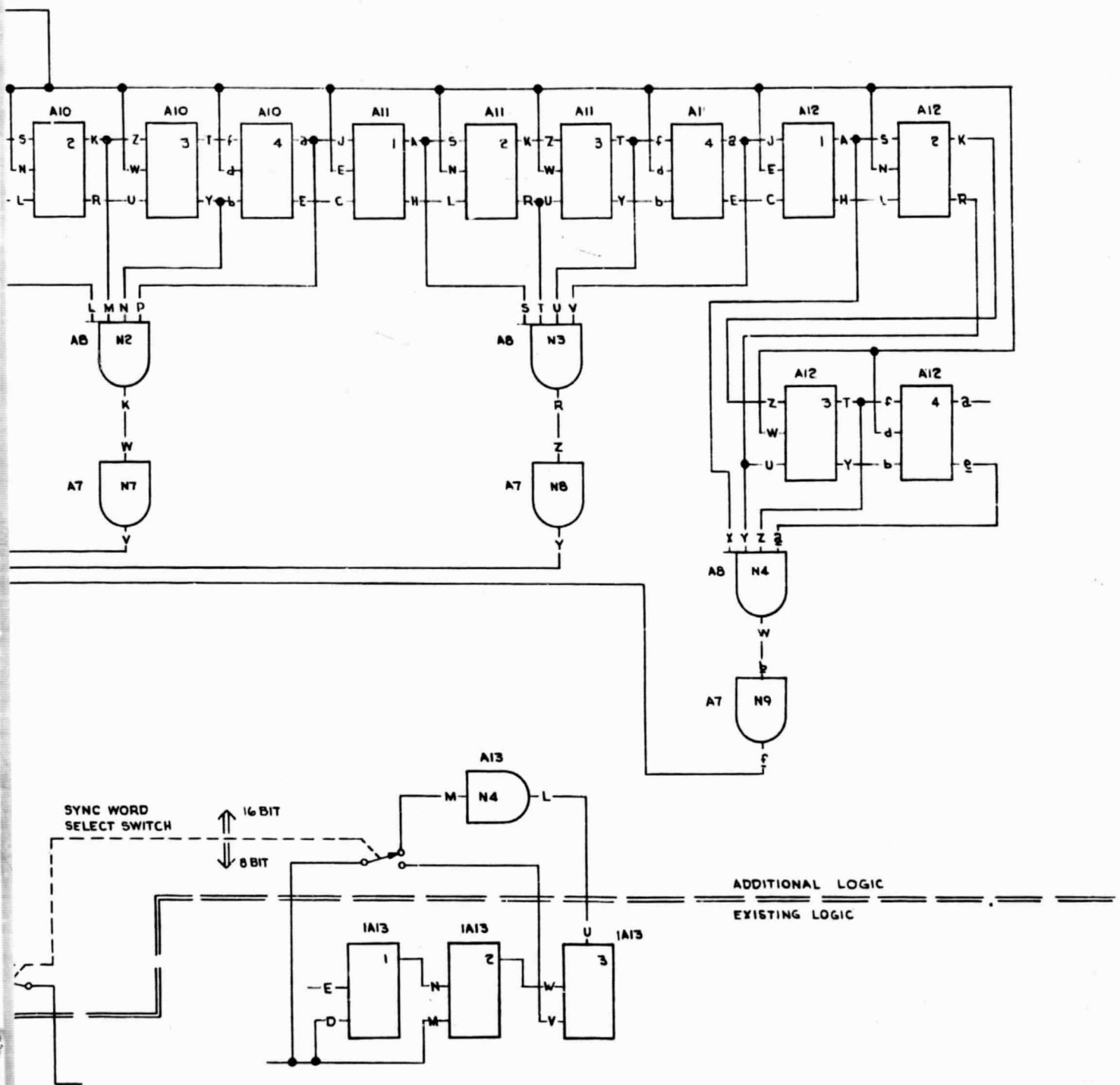


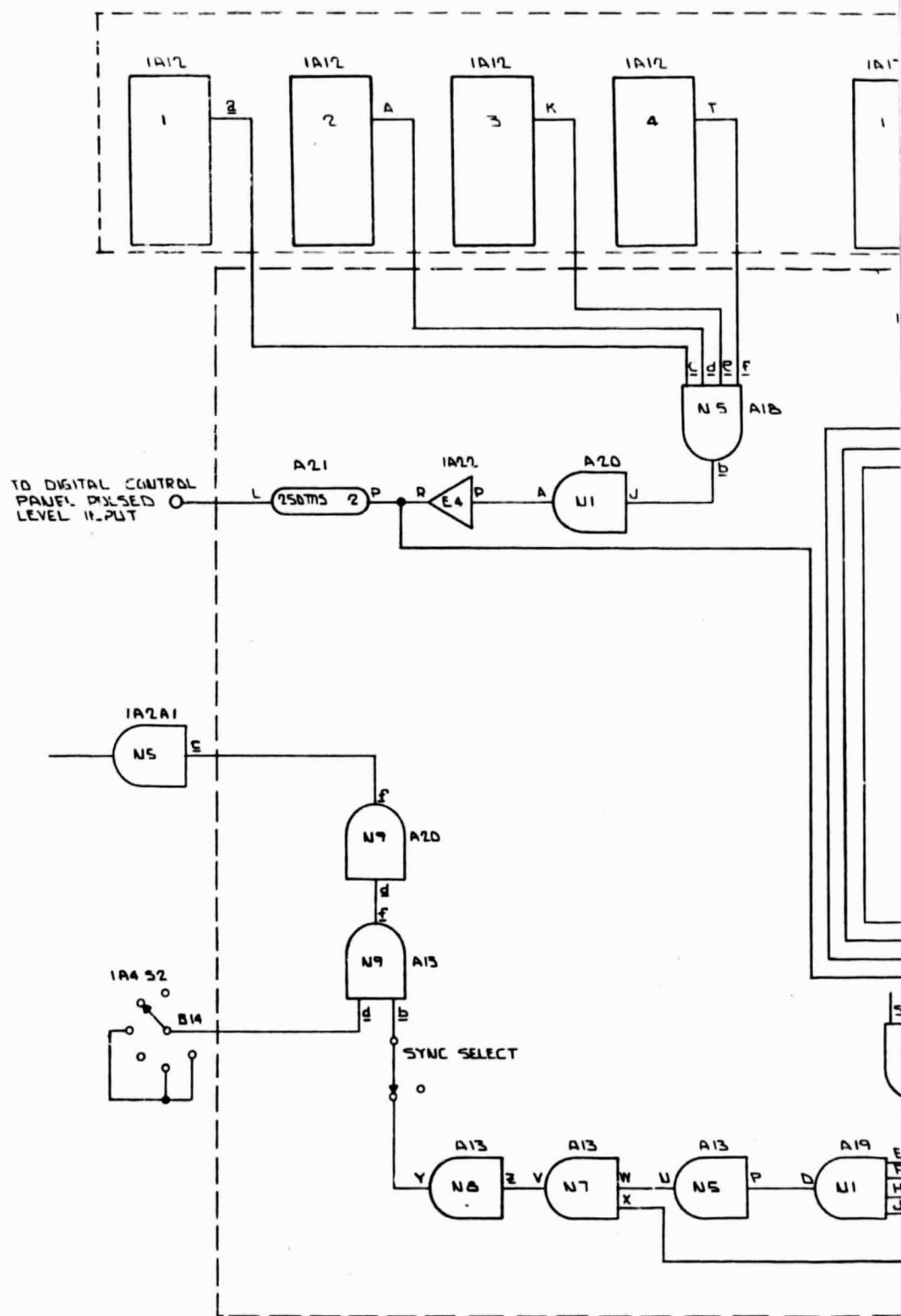
Figure 41. Test Set Sync Recognition Logic Diagram

1.9.1.2 The logic diagram of the word inhibit circuitry is shown in (figure 42).

The Counts from the test set time slot and subframe counter cards 1A12, 1A17, 1A18 are used to drive a NOR gate arrangement which selects the six Time Code time slots in subframe one and time slot 63 in all subframes. During these time slot periods, a voltage level is produced at the output of card A13-8 which can be used to inhibit the test set voltage comparison circuit. In the 16-bit position of the SYNC WORD SELECT switch, this inhibit voltage is OR gated with the normal inhibit voltages from 1A4S2.

1.9.1.3 The digital control panel interconnection diagram is shown in (figure 43).

The SYNC WORD SELECT switch controls the selection of the 8-bit or 16-bit subframe sync word and in the 16-bit position also connects in the Time Code word inhibit circuitry. The SYNC WORD SELECT switch will be placed in the 16-bit position only for checkout of the input A of Nimbus "B". The TIME CODE SIMULATOR switches provide the means of selecting the data bits to be inserted into the Time Code word train. It should be remembered that all four bits should not be placed in the "1" position at the same time as this is not a true Time Code word and results in the generation of false sync words. The DIGITAL SIMULATOR switches provide the means of selecting the signal level to the input of the digital channels. The switches correspond to the bit weight position of the channels in the digital word. One pole of each switch is used for the bilevel channels



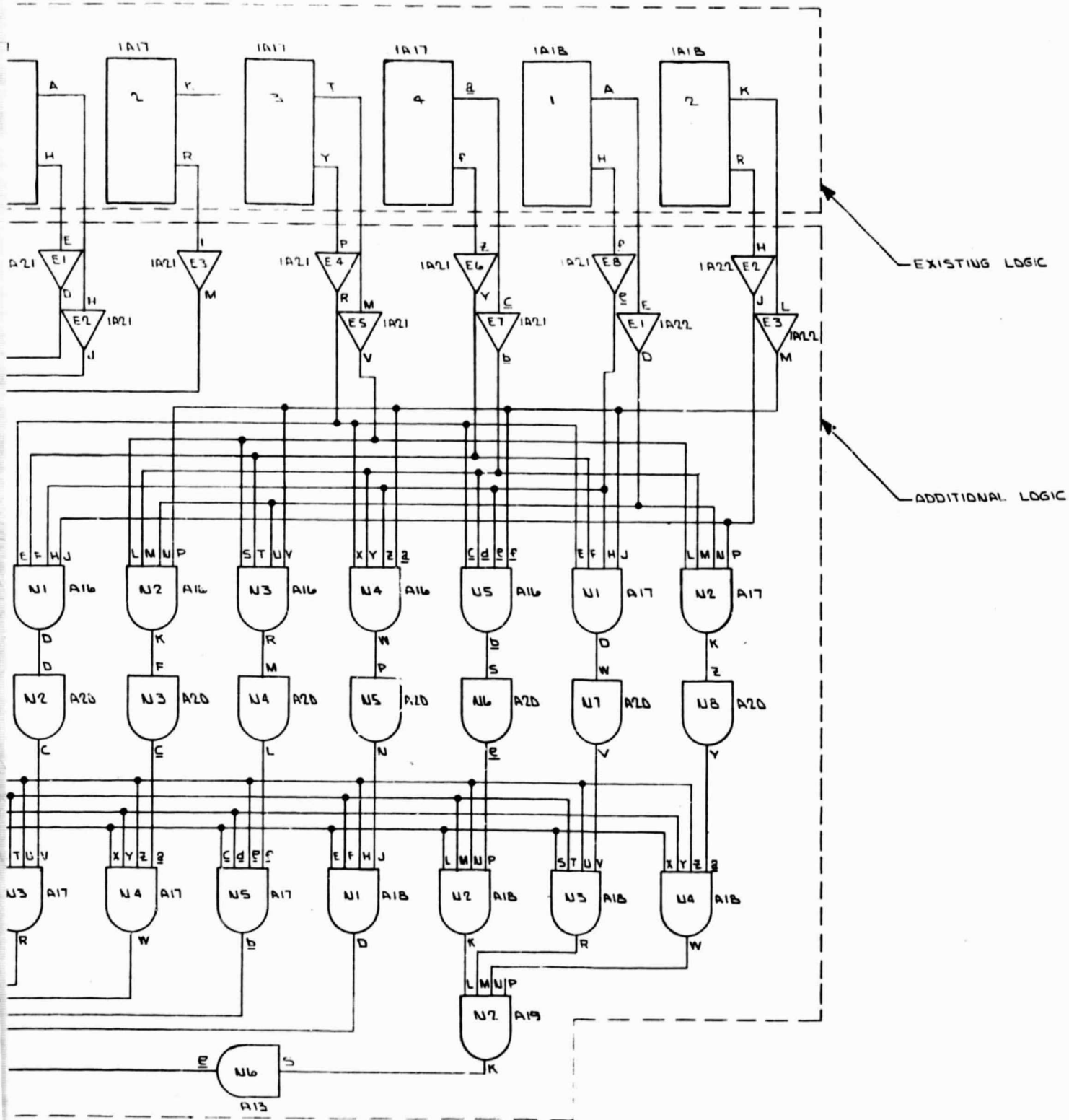
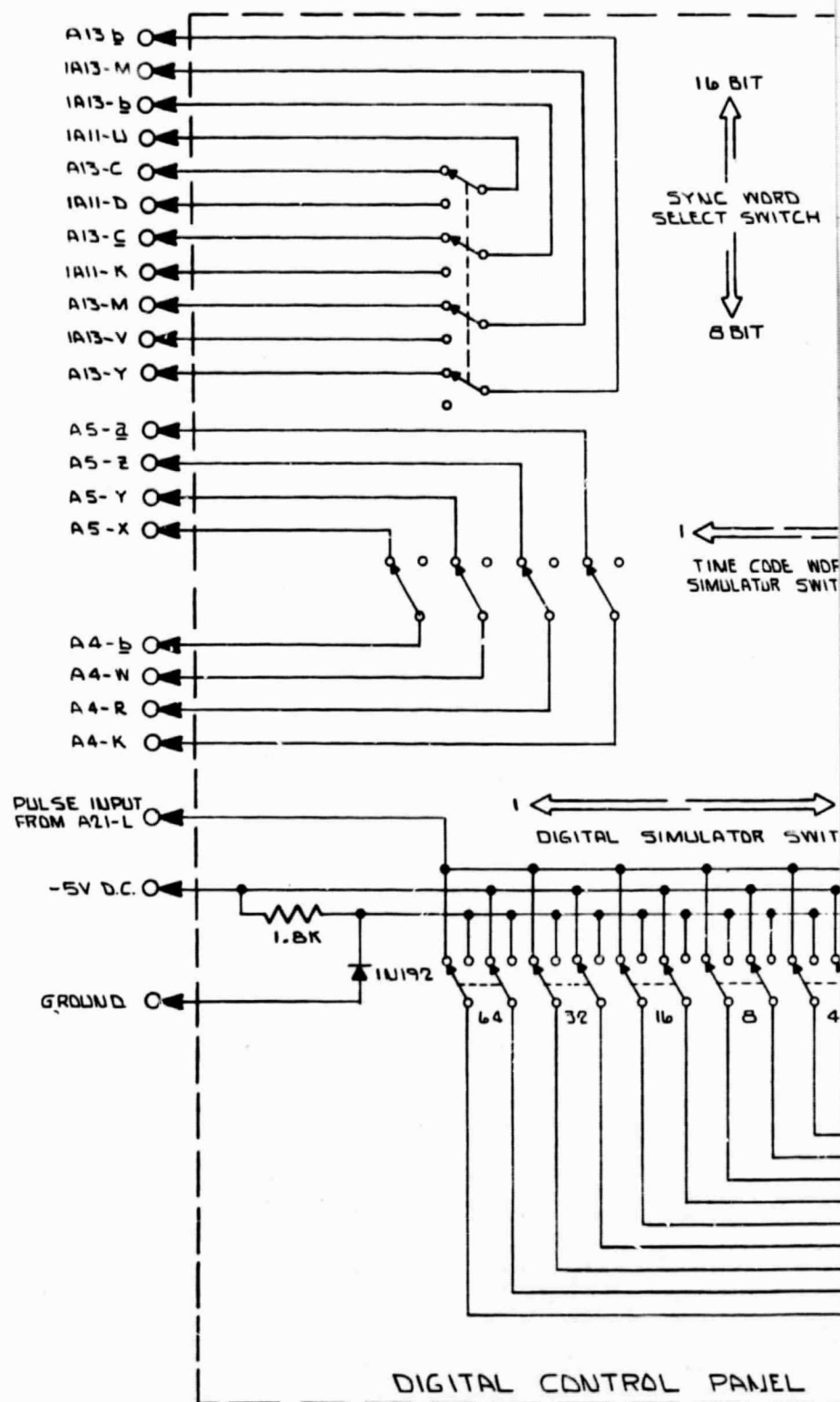


Figure 42. Test Set Time Code Inhibit Logic Diagram



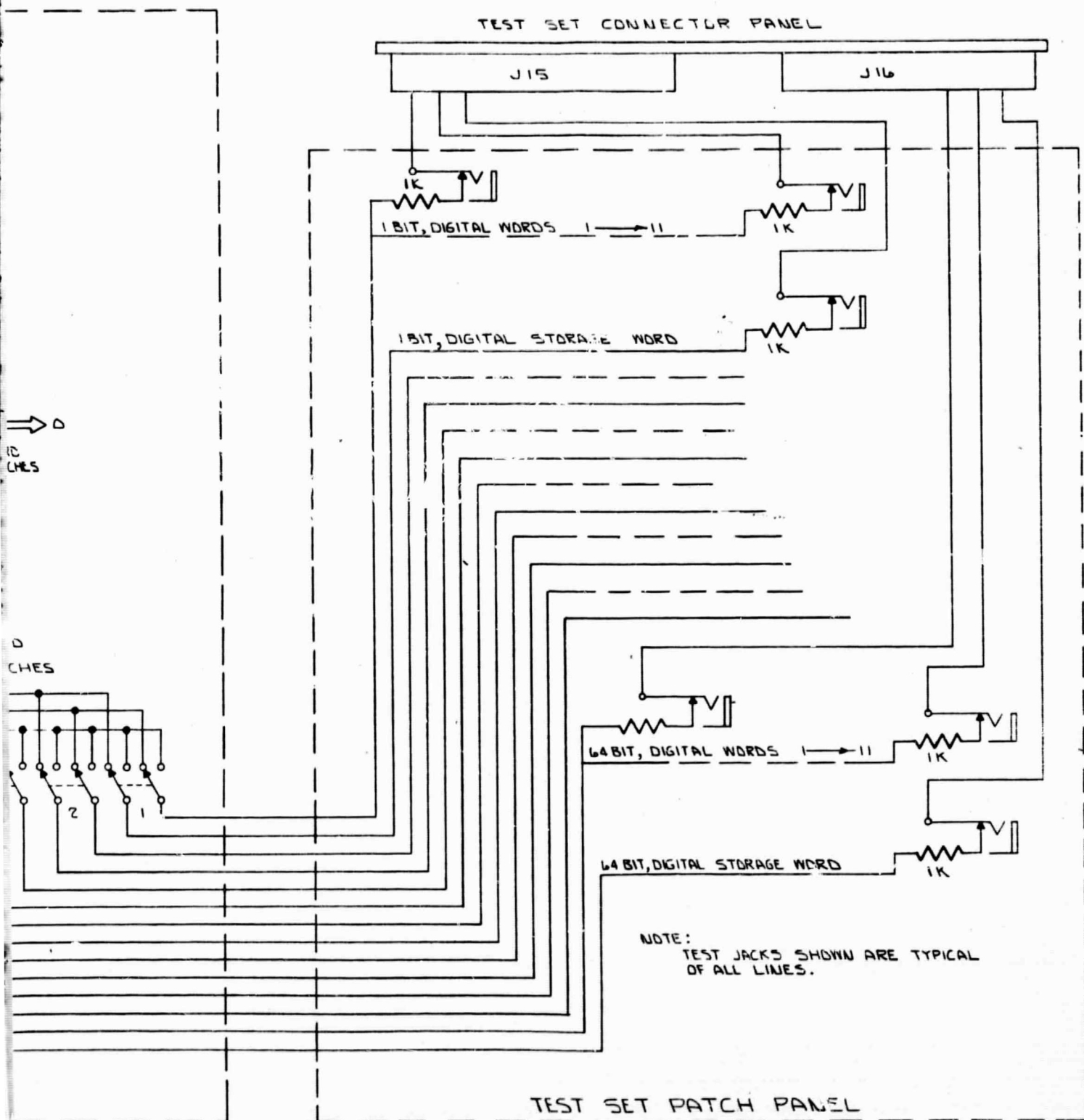


Figure 43. Interconnection Cabling Functional Diagram for Digital Control Panel

and the other pole is used for the transient data storage channels. In the "0" level of the switch position, the voltage level output is a worst case condition of -1 volt. In the "1" level of the switch position, the voltage level output is a worst case condition of -5 volts. The output of these switches is connected to the appropriate Multicoder digital channel through a 1K resistor and the normally closed contacts of a test jack on the test set patch panel.

- 1.9.1.4 The logic for simultaneously displaying and detecting errors in the six Time Code words is shown in (figure 44). The first four bits of the test set voltage code storage bistables are connected to six sets of AND gates with each set consisting of four gates corresponding to the four voltage code bits. Each of the six sets is gated with one of the Time Code words. When a particular Time Code word slot occurs it gates the four data bits, which are in the voltage code storage, into a Time Code storage bistable. The Time Code storage bistable will then light an indicator lamp if it is storing a "1". All six Time Code words will be read into storage during subfram 1. At the start of subfram 2, the particular side of the storage bistables, as selected by the twenty-four toggle switches, will be interrogated. These switches will be in the same configuration as the switches which generate the simulated Time Code word train. If the readout of the Time Code words does not match the simulated word train selection, then an error signal is generated which will be used to drive

NOTES:
1. PARTIAL REF DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NO. OR SUBASSY DESIGNATION.

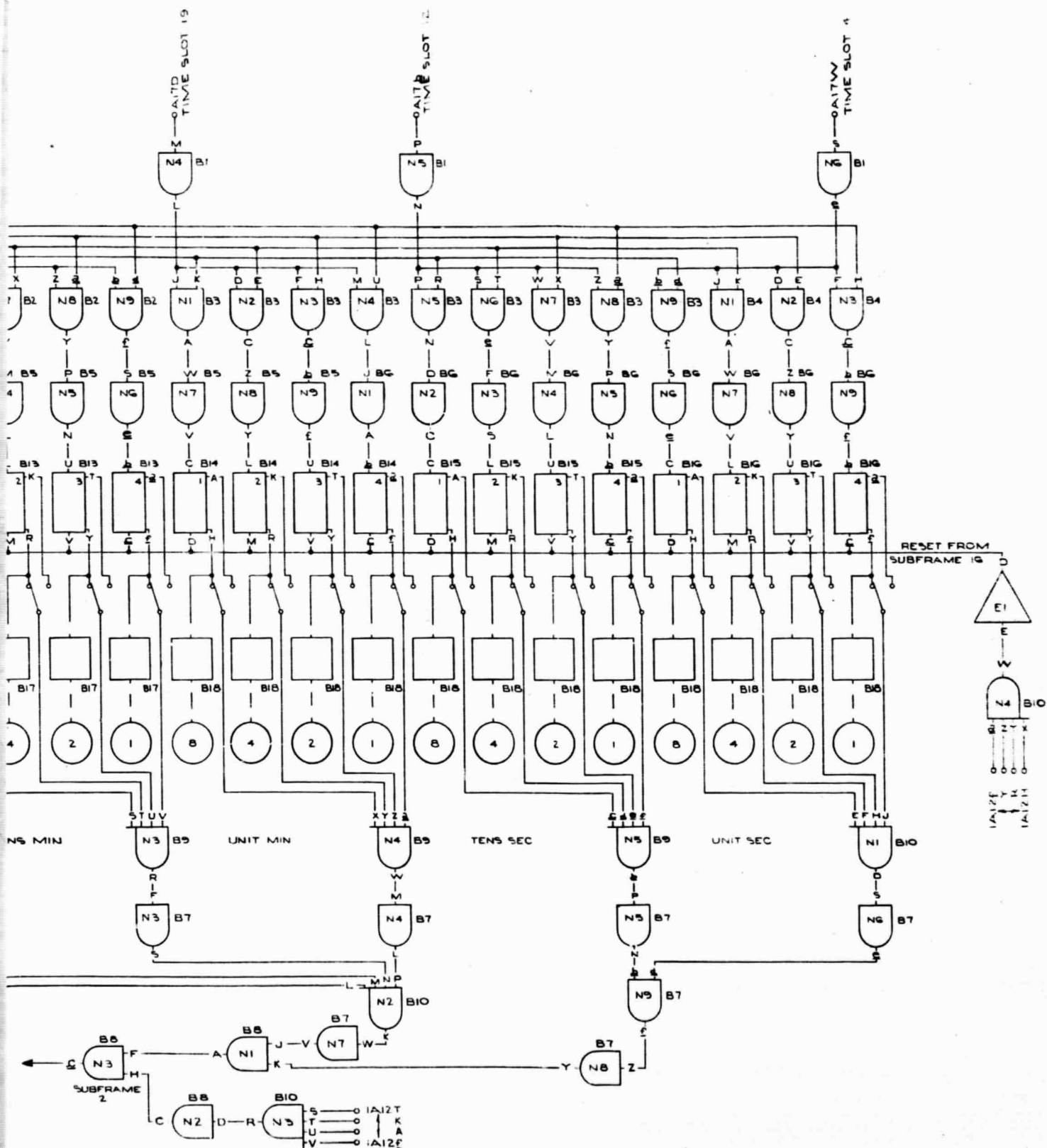


Figure 44. Test Set Time Code Display Logic Diagram

a magnetic relay type counter. During subframe 16, the storage and readout will be reset and ready to read in the next six Time Code words which will occur in subframe one.

- 1.9.2 Additional Power Requirements. - Because the addition of the forty-seven logic cards, the two negative five volt supplies in the PCM test set are no longer adequate. These supplies are KEPCO Mod SC-18-2M. The recommended replacement is KEPCO Mod CK8-5M which has the same external dimensions as the SC 18-2M. A mounting panel KEPCO Mod RM 4 will be required for mounting the new supplies.

1.9.3 Hardware Requirements. -

- 1.9.3.1 The logic additions to the test set will require 47 logic cards and two card chassis. The card chassis will be mounted in the available space above the two chassis now installed in the test set. The card breakdown is listed below:

Quantity	Type	Assembly Drawing
1 each	Power Driver	D1297-44
4 each	Shift Register	D1297-27
10 each	Bistable Multivibrator	D1297-26
12 each	Four Input NOR	D1297-31
13 each	Two Input NOR	D1297-48
2 each	Emitter Follower	D1297-28
1 each	Monostable Multivibrator	D1297-25
1 each	Special Amplifier	To be Drawn

Quantity	Type	Assembly Drawing
1 each	Logic Card Chassis	D600462
2 each	Offset Network	To be Drawn

1.9.3.2 The digital control panel will consist of an aluminum plate on which will be mounted the DIGITAL SIMULATOR switches, the TIME CODE switches and the SYNC WORD SELECT switch. The present test set patch panel will have 2.75 inches removed from its bottom edge and the digital control panel will be mounted in this space. The test jacks for the "B" unit multiplexer will be moved up on the patch panel to the unused "B" matrix test jacks. The required hardware for this panel is listed below:

<u>Quantity</u>	<u>Description</u>
7 each	Switch, D.P.D.T. miniature toggle
48 each	Switch, S.P.D.T. miniature toggle
1 each	Switch, 4-P.D.T. toggle
1 each	Diode 1N192
1 each	Resistor, 1.8 K, 1/4 w
1 each	Aluminum Panel 19 x 2.75 x 0.125

1.9.4 Harness Requirements. - A new harness is required to connect the test set digital outputs into the PCM Multicoder. The harness will require three Bendix type PT 06CE-22-55P(SR) connectors and approximately one thousand feet of #24 stranded wire.

1.9.5 System Test Set Modification Requirement.— The 62.5 word subframe and 16 bit sync word require addition logic (Figure 45) in the System Test Set in order to provide compatible simulated PCM output. Word 62.5, Word 1, and Word 2 are gated from the subframe counter bistables in the test set and are AND gated with the appropriate word bits from the word count bistables to generate the sync word 0 1 1 1 1 1 0 1 1 1 0 1 0. This RZ sync word is then gated to the NRZ output bistable 3A7A4-4 from the "0" gate B6-N8 and the "1" gate B6-N9. Bistable 3A7A4A-3, which has been set at the start of Word 62.5 by gate B6-N2 output, inhibits data word output to the NRZ bistable during sync word time. Positive transition of gate B6-N1 at the end of Word 2 is used to reset the inhibit bistable and enable the data word output. Negative transition from gate B5-N8 at the end of Word 62.5 is used to reset the subframe counters. The additional logic requires four each 4 NOR logic and two each 2 NOR logic cards which can be accommodated in the present logic card rack.

1.10 RELIABILITY.— The reliability effort consisted of a study to determine recurring problem areas prevalent in the previous Nimbus PCM Telemetry System (Ref 14, Section 4) and to assess the reliability of the modified system. The reliability estimates reflect the latest data on component failure rates (Ref 14, Section 4).

1.10.1 Numerical Assessment of Subsystem Reliability.— A detailed evaluation of the reliability of the PCM Study Subsystem modifications using discrete components has been made, resulting in a probability of successful operation (P_s) for a six months life and allowing no loss of data of 0.7946. Assuming a minimum failure

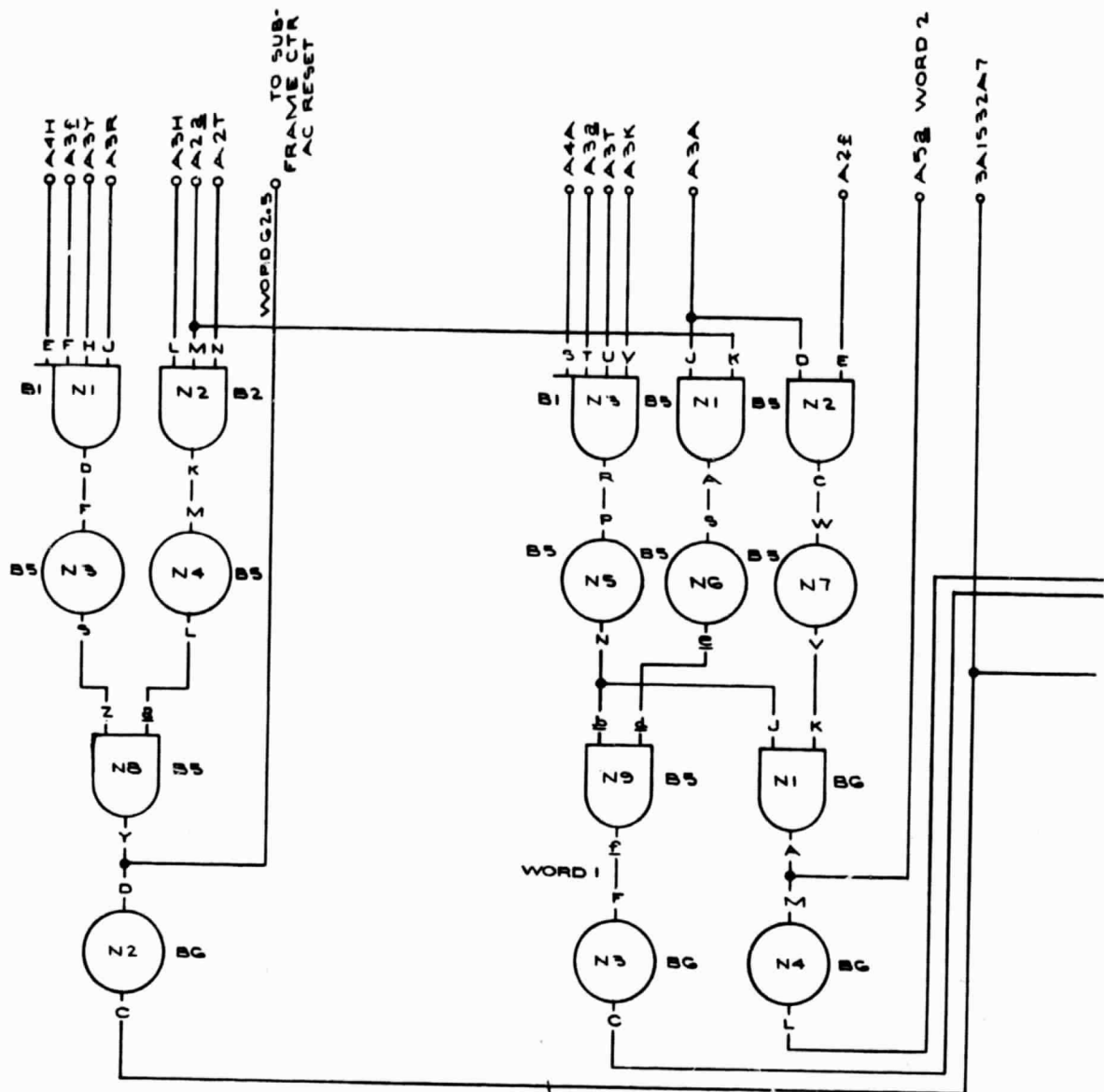


Figure 45. System Test Set Additions Logic Diagram (Sheet 1 of 2)

NOTES:
1. PARTIAL REF DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NO. OR SUBASSY DESIGNATION.

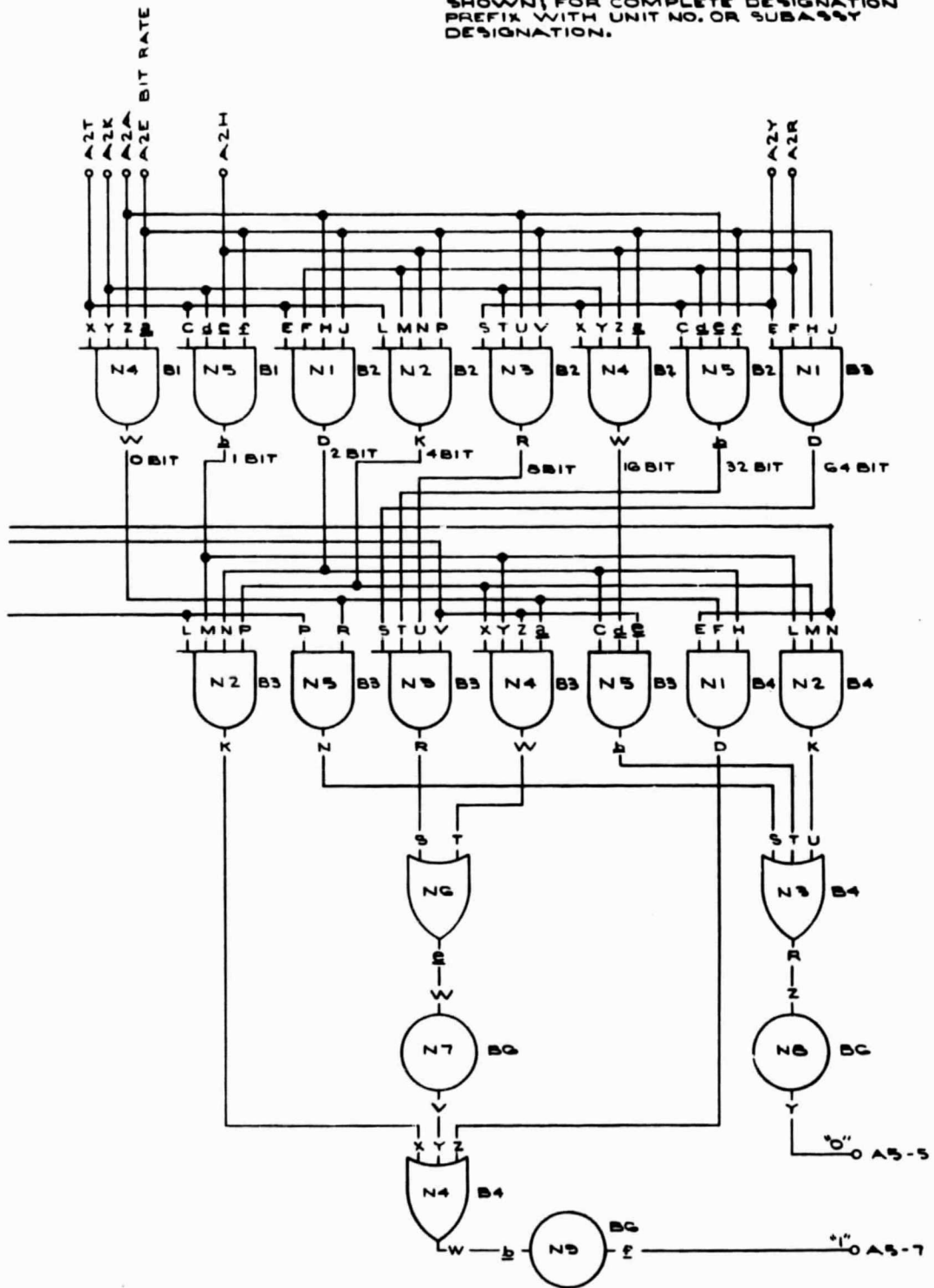


Figure 45. System Test Set Additions Logic Diagram (Sheet 2 of 2)

rate improvement of 2:1 using integrated circuits for the digital multiplexer gates increases the P_s to 0.8394.

1.10.2 Reliability Mathematics. - The underlying distribution to describe the failure pattern of any piece, part, circuit or subassembly is assured to be exponential when used in a single mode, nonredundant application.

Probability of success:

$$P_i = e^{-\lambda_i t}$$

Where:

P_i = probability of success of circuit

λ_i = failure rate of circuit

t = time of mission

The reliability model for failure-free operation is simply the product of the zero-failure probabilities of all blocks.

$$P_s = \prod_{i=1}^H P_i$$

$$i = A$$

$$= P_A P_B P_C \dots P_H$$

Where

$$P_i = e^{-\lambda_i t}$$

1.10.3 Failure Rate Considerations. - The failure rates for semi-conductors (ref 13, Section 4) are considered somewhat pessimistic in view of the fact that the high-temperature operating burn-in which all semi-conductors on the Nimbus Program are being subjected will improve their inherent reliability, but no

means of measuring this improvement is readily available. Because of this, the semiconductor failure rates do not reflect any improvement in reliability gain with the bake program.

- 1.10.4 Analysis Work Sheets. - Appendix IV contains the Reliability Calculation Form work sheets. These work sheets give the results of stress analyses performed on all circuits in the system, and the assigned failure rate for the calculated stress level.
- 1.10.5 Reliability Block Diagram. - (See Figure 46.) The block diagram gives the apportionment of the overall subsystem reliability for each functional circuit block and is currently applicable for the PCM study modifications.
- 1.10.6 Failure Effects Analysis. - The following paragraphs present a failure effects analysis of the Nimbus Study System modifications. This analysis was made utilizing the logic and timing diagrams presently available. The failure effects analysis considers failures at the circuit level, and in some cases, higher levels of assembly as in the case of the programmer counters. Each circuit or block is assumed to fail in turn, with the consequences of the failure on the mission capability then determined. For analysis, the study system circuits and assemblies have been grouped as follows:
 - a. Programmer Counters
 - b. 1 CPS Reset Circuit
 - c. Bias Amplifier
 - d. I. D. Buffers

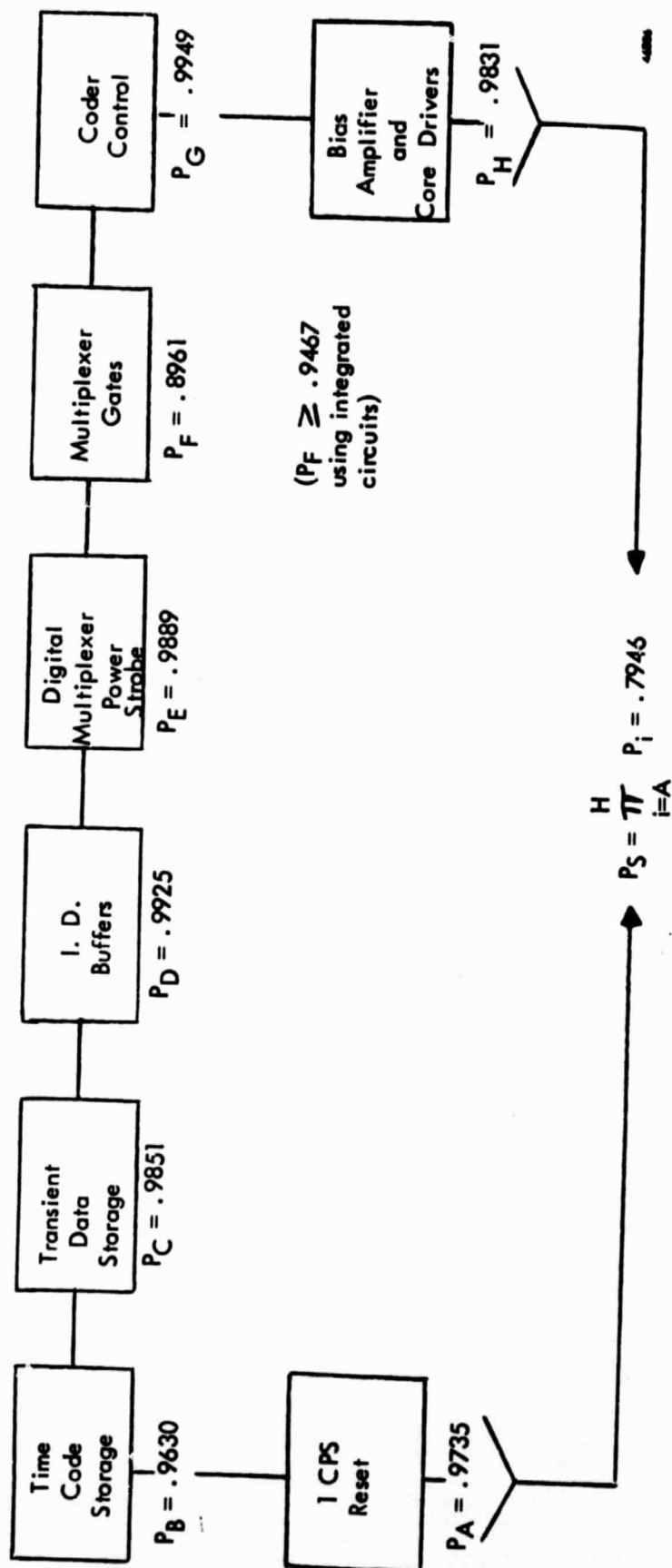


Figure 46. Reliability Block Diagram

- e. Programmer Command Matrix
- f. Coder Control
- g. Digital Multiplexer
- h. Time Code Storage

1.10.6.1 The first stage of the counter string accepts an inverted 500 cps trigger originating from the Nimbus clock. The first three stages perform an 8:1 count for bit rate, the next six stages comprise a 62.5:1 counter (with reset) for word count, and the last four stages comprise a 16:1 counter for subframe count. A failure in any stage of the 8:1 or 62.5:1 counters will cause the loss of enabling commands for the placement of all digital data into the output format. Also, a counter failure would result in the loss of all analog data. For the 16:1 counter, three failure modes have been considered. Any of the three failure modes would introduce error in the frame identification word.

- a. A subframe 1 "lock-up" failure would affect Words 4, 12, 19, 23, 31, and 36 of 62.5 of F2-16 of the digital data, and all sub-commutated analog data. The six word Time Code would appear in all frames (F1-16), Words 4, 12, 19, 23, 31, and 36 of 62.5. The total data loss would include all subcommutated analog data (coder being continuously inhibited and no commands to the analog matrices), the three subcommutated digital words, and the

subcommutated digital storage word (the loss of the reset pulse for the storage flip-flops during $W \frac{31}{62.5} F2$ would be of small importance since the word strobe, $W \frac{23}{62.5} F2$, would not occur).

- b. Subframe 2, "lock-up" failure would affect words 4, 12, 19, 23, 31, and 36 of 62.5, F1, F3-16, of the digital data, and all subcommutated analog data. The total loss would include all subcommutated analog data (coder is inhibited) and the six time code digital words. In F1, four of the six time code words would be replaced by the three subcommutated digital words and the subcommutated storage word. The other two word slots, $W \frac{31, 36}{62.5} F1$, reserved for two subcommutated analog words, would be vacant (loss of commands and coder inhibit).
- c. A subframe 3 - 16, "lock-up" malfunction will cause the loss of all digital data in words 4, 12, 19, 23, 31, and 36 of 62.5, F1, 2, and all analog subcommutated data.

1.10.6.2 There are two 1 CPS detect circuits used to reset the six stage counter to provide a 62.5:1 count. They are 62.5 word detector and 1 CPS detector. The 62.5 word detector is an AND gate. It detects word 63 ($A, \bar{B}, \bar{C}, \bar{D}, \bar{E}, \bar{F}$), bit five (1,2,3), and is gated with the 500 cps input from the clock to provide a reset pulse at the beginning of bit 5, word 63. This pulse drives a monostable multivibrator which gives a

500 μ s reset pulse. A failure in this circuit could affect the count. An open diode could cause a false reset and a shorted diode would load the counter. The 1 CPS detector is a five stage storage register which detects the five "ones" that occur in the time code each second and provides a 1 CPS pulse. This pulse is OR'ed with the 62.5:1 word detector pulse to provide synchronization of the counter with real time. A failure in this circuit could affect the count (Q6 shorted C-E in the time code buffer) and the count will probably be asynchronous with real time.

1.10.6.3 This amplifier provides bias to the core drivers and digital multiplexer. A failure will cause the loss of all digital data.

1.10.6.4 This circuitry buffers the output of the four stages in the 16:1 counter. This output is in the form of a frame I.D. word (4 bits, W2/62.5, F1-16). A failure would cause the loss of the frame identification word.

1.10.6.5 The most adverse failure mode would be that which would continuously inhibit the coder, resulting in the loss of all analog data. The digital failure modes are discussed below:

a. A9. A failure in this portion could cause the loss of all digital data as a result of power strobe loss.

b. A5. A failure here could cause the loss of the three digital sync words, W $\frac{1,2,62.5}{62.5}$, F1-16.

c. A6. A failure here could cause the loss of all prime digital data,

$$W \frac{5, 13, 21, 29, 37, 45, 53, 61}{62.5}, F1-16.$$

d. A7. A failure here could cause the loss of the time code,

$$W \frac{4, 12, 19, 23, 31, 36}{62.5} F1, \text{ the three subcommutated digital words,}$$

$$W \frac{4, 12, 19}{62.5} F2, \text{ and the subcommutated digital storage word,}$$

$$W23/62.5 F2.$$

e. A8. A failure here could have the same effect as in the A6 circuit

with an additional failure possibility in the coder inhibit OR gate.

A failure in this gate could cause either the coder to be inhibited continuously or the result could be a no-inhibit condition causing degradation of all digital data by analog superposition.

1.10.6.6 A failure here could cause the loss of, or continuous presence of, coder inhibit. In the former case, the result would be the loss of all analog data. The latter would result in the degradation of all digital data caused by analog superposition.

1.10.6.7 In the following analysis, a digital multiplexer gate is analyzed on a piecepart level.

a. Driver Transistor. The most adverse failure mode would be a short of the driver transistor. This would enable the digital gate continuously. The effect would be that all data would be degraded

by superposition on the 7 bit bus to the core drivers. An open mode failure would cause the loss of only one digital word.

- b. Gate Resistors. An open or shorted resistor would cause the loss of one bit in the digital word in question.
- c. Input Diode. A shorted input diode would cause the degradation of one bit in all data as a result of superposition on the common bus. An open input diode would cause a continuous "one" to be read for one bit in the digital word in question.
- d. Output Diode. An open output diode would cause the loss of one bit in the digital word. A shorted diode would result in a loss of isolation and degradation of the digital word in question.

1.10.6.8 The time code storage consists of a 10:1 counter and a four stage shift register. The 10:1 counter provides the shift pulses required to enter each time code word into the register for presentation to the digital multiplexer. A failure in this counter would result in the loss of the time code words. The four stage register stores the four bit time code prior to sampling. After the code is read out through the digital multiplexer, a new time code word is shifted in. A failure in the storage register would result in the loss of the time code words.

1.10.7 Parts Selection. - The additional components required for the Nimbus Study Program were selected from similar qualified and acceptable units used in the original system where possible and from those components already qualified to

pertinent specification on other Telemetry Systems at Radiation. Every effort has been made to use the minimum practicable number each generic part type. A review of the parts list for the original Nimbus PCM design was undertaken to determine the revisions necessary for future systems using discrete components, with the following results:

- a. The 2N495 transistor, Radiation Specification 100354-1 (manufacturer Philco) was used extensively. Since Philco no longer produces transistors, it is suggested that the 2N2187 (manufacturer Sprague) be considered as a replacement.
- b. The T2209 transistor, Radiation Specification 100330-1 (matched pair of 2N862 transistors manufactured by Philco) is used as a gating switch pair. This transistor can be obtained from Sprague as a matched pair or a redesign could be undertaken to use the 3N74 integrated chopper in future systems, which would increase reliability and improve performance.

1.10.8 Failure History.— A program for recording Nimbus PCM module and system failures was implemented in September 1961, and was in operation throughout the three prototype and five flight systems. Corrective action performed on the flight systems eliminated several problem areas that occurred during tests of the prototype systems. Every effort should be made to eliminate all of the recurring problem areas on future Nimbus Systems. The following paragraphs describe the major contributing factors that have caused system malfunctions along with the corrective action that has been implemented.

1.10.8.1 In respect to design, repeated timing malfunctions during high temperature tests of the prototype systems were the result of leakage current triggering the flip-flops in the Synchronizer Circuits. All of the synchronizer stages of Unit A and Unit B were redesigned. The nature of the redesign was to increase the operating current of each stage, thereby obviating the effects of leakage. No further problems resulted from this circuit during tests of the flight models. A similar problem occurred during high temperature tests of the flight systems. Erroneous bits were generated in the Output Shift Register caused by the leakage current from one leg of the AND gate (2N1711 transistor) through the set windings. A design change was made to lower the value of the base resistor and to increase the bias voltage. Several tests were conducted to prove the reliability of the changed circuit and all tests proved to be successful. However, since the core winding is used as a collector load for the other side of the AND gate (2N722 transistor), a further redesign has been undertaken (figure 32) during this study program to preclude any possibility of the 2N722 leakage current setting the core winding on future systems.

1.10.8.2 During vibration tests of the prototype systems, several instances of module pin breakage occurred. It was discovered that uneven pressure was distributed across the module surfaces, when compressed in a system configuration, creating tension on some of the module pins.

The tension is increased with the additional stress of vibration, causing the pins to break. It was also discovered that in some instances the module top or bottom planes were not parallel to the printed circuit boards, on which it was mounted, due to variation in module height or improper potting. As a result of the following corrective actions, no further failures of this nature were encountered in the flight systems.

- a. All modules were cemented to the printed circuit board.
- b. Increased emphasis by inspection to ensure that all modules are mounted flat to the board.
- c. Greater control of the module potting process to ensure proper curing time and temperature.
- d. Eliminate crimping of pins when soldered to the board.
- e. Eliminate the use of weak component leads as module pins.

1.10.8.3 Numerous-system malfunctions prior to Acceptance testing and several during Acceptance testing were attributed to defective pulse transformers. The primary problems have been squareness ratio degradation, open windings and winding-to-core-to-winding shorts. The original transformers used on the prototype systems were manufactured by Radiation using Arnold cores. After several system malfunctions caused by transformer core squareness ratio degradation, a thorough investigation was made and the Radiation manufactured units were replaced with units manufactured by Sprague using Dynacore cores.

The transformer squareness ration degradation mode of failure was substantially reduced during tests of the flight systems. The cause of the open winding was discovered to be the result of the terminal wires not soldered internal to the Sprague transformer package. Items of this nature should be controlled by inspection during manufacture at the vendors facility. The specification control drawings for these transformers include a polarity test of the windings to be performed on all production units after each has been subjected to thermal shock tests. This test should detect open winding defects that may occur due to a fault in the inspection procedure. The most frequent mode of a failure with the Sprague transformers was due to internal shorting. In almost every instance, this was found to be caused by a short from winding to winding through the stainless steel core bobbin. After considerable investigation, including trips to the vendors facility, it was concluded that the wire insulation was degraded during winding operations by the pitted bobbins and that the stainless steel bobbin was not properly insulated. The specification control drawing was revised to specify that the bobbin must be free of pits and burrs when viewed at 100 magnification and it now specifies a double coat of varnish on the core, followed by an insulation resistance test prior to assembly. The vendor is also required to conduct a dielectric strength test plus an insulation resistance test of the completed

transformer, following the non-destructive thermal shock tests on each of the production units. The specification control drawings for the pulse transformers have been upgraded to ensure that the above defects are controlled by the vendor. Tests were conducted on a sample size of transformers manufactured by Sprague to the revised specification. Twenty (20) units were vibrated to the levels specified in MIL-T-21038B (General Specification for Low Power Pulse Transformers dated 11 January 1962). No open or shorts were detected after vibration. Nineteen (19) units were tested to destruction in order to measure the dielectric withstanding voltage. The average dielectric strength of the improved transformers is over 60% higher than the previous design. This higher dielectric strength means that the insulation life is extended and that the probability of winding to winding shorts are greatly minimized.

- 1.10.8.4 Workmanship in welding operations is a contributing factor to module malfunctions. This problem received considerable study and has been alleviated by specifying weldable lead requirements in all part specification control drawings, by checking the lead material on each component to ensure proper weld and pressure settings for optimum weld strength, and by implementing a more rigid weld inspection procedure. The modules also receive individual vibration tests to further detect weak welds prior to being placed in a system. Subsequent in-house projects

have experienced very few weld problems since the institution of this corrective action.

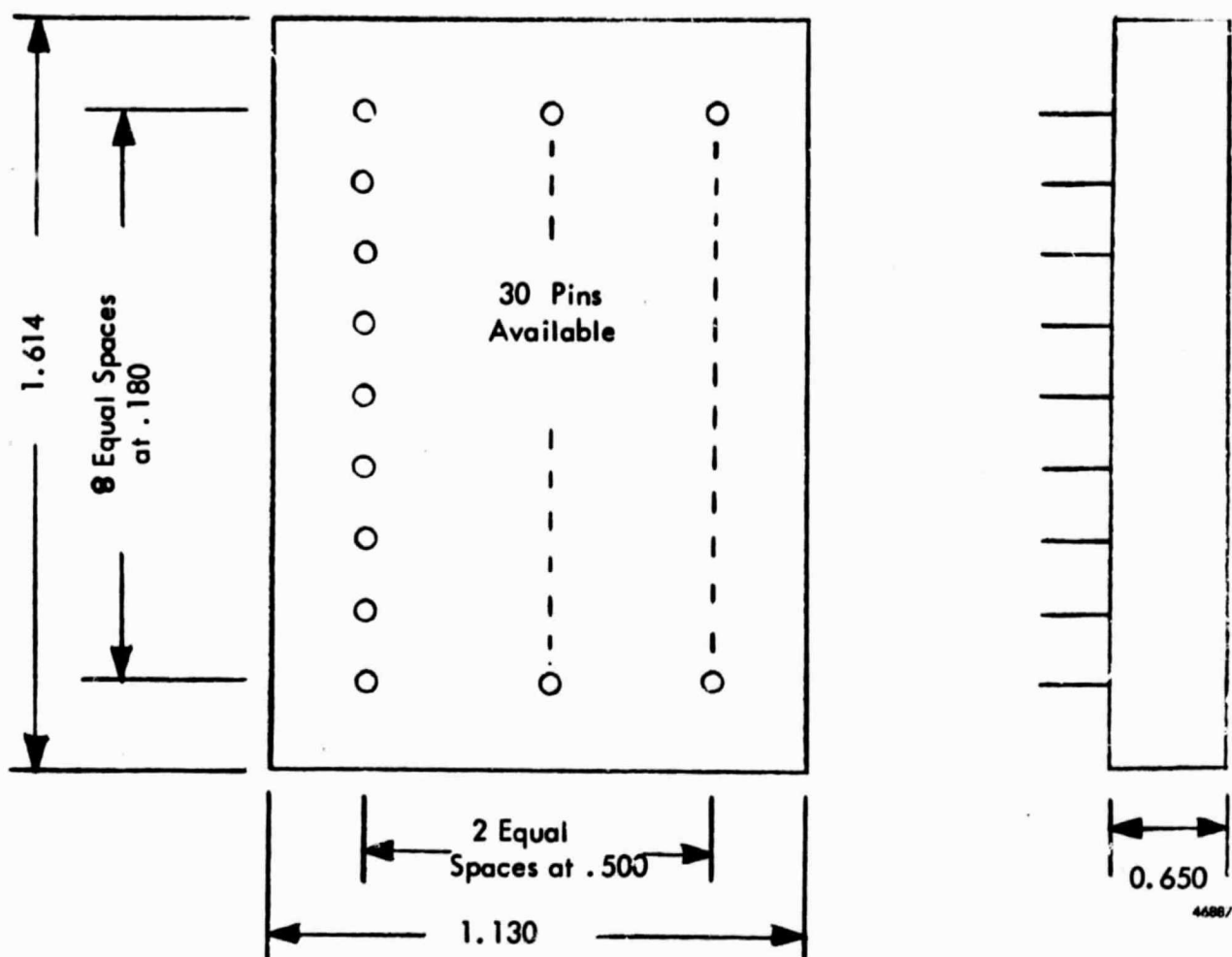
1.11 MECHANICAL. - Results of the investigation into repackaging the Airborne equipment to include the modifications show that these modifications can be adequately incorporated into the present system with relatively little disruption of the existing hardware. Part of the small stack of cards, trays 10, 16, 17, and 18 must be relayed to accomodate the new digital circuits. Additionally, one card in the large stack, 5B, will require minor changes to the printed circuitry to reflect the changes in the 8:1 counter and to permit sync and digital data functions into the output shift register. New card layouts are necessary only where module changes have been made. Thus the size and quantity of printed circuit cards remain unchanged. No problems are anticipated in fabrication and assembly.

1.11.1 Packaging Requirements. - The integrated circuits, supplied in flat packages, are to be mounted to small cards (referred to as "carrier cards"). These carrier cards are epoxy laminate cards with printed circuitry on each side. Their size is approximately 1.71 x .50 x .035 inches. The integrated circuit packages are placed flat against the surface of these cards, and the leads are either welded or soldered directly to the appropriate printed wiring. Each carrier card accommodates two integrated circuit package. Interconnection lead wires are attached, and the carrier cards are epoxy coated for protective purposes. The next higher assembly is achieved by positioning four completed carrier cards into a holding fixture so that the cards are all parallel and equally spaced with each other. Sheets of mylar with welded module wiring patterns printed on them,

which have been previously punched for location over the protruding leads, are located in place. The interconnections between the leads are then made by welding nickel ribbon to them as is done in the standard cordwood modules.

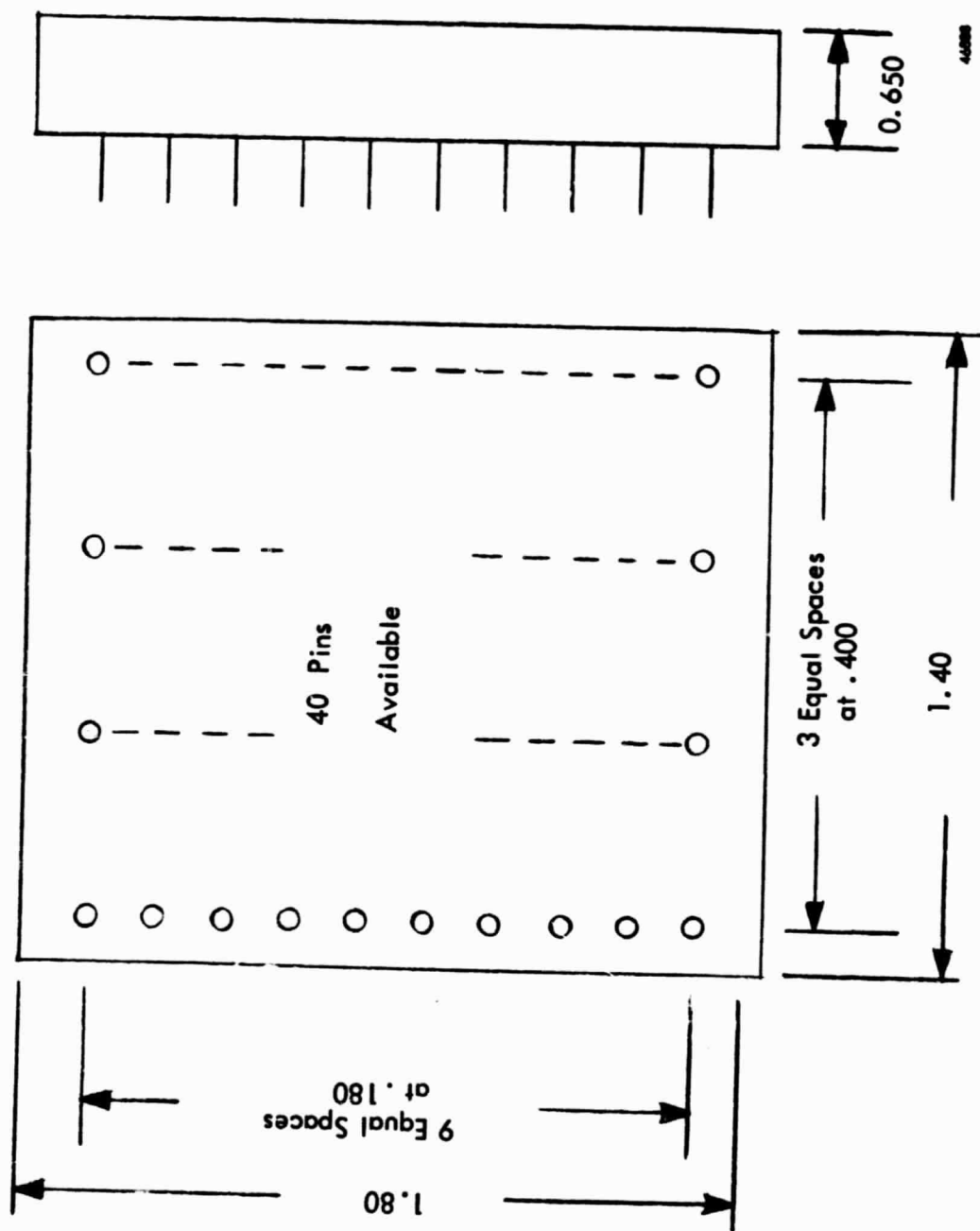
1.11.2 Packaging Concept. - The packaging concept remains unchanged. Welded cordwood modules similar to those currently in use will be fabricated. Both the cordwood and integrated circuit welded modules will be foamed with urethane rigid foam. No changes in system response to any of the induced environments should occur. New module configurations are illustrated in figures 47 and 48. Two new molds are required in order to foam the modules because of the new module sizes, and one existing mold will require pin pattern modifications because of module relayout. Table 6 tabulates module utilization. The present type and quantity of connectors will be maintained. In line with the present system, two-sided circuitry with plated-through holes will be used. All affected cards, eight per system, will require relayout which, in turn, necessitates eight new masters. Repositioning will require four new drill templates (table 7). To satisfy pin requirements, the printed circuitry will conform to the following criteria:

- a. Conductor Width 0.020 inch
- b. Land Width 0.080 inch
- c. Hole Size 0.035 inch
- d. Circuit Spacing 0.020 inch min.



NOTE:
All dimensions in inches.

Figure 47. Typical Module



NOTE:
All Dimensions in Inches.

Figure 48. "Carrier" Card Module

Table 6. Module Utilization Summary

New Module Designation	Old Module Replaced	Module Contents	Qty. Per System	Location Tray Card		Pins Utilized Per Module
D-1	C-17	Bias Amp & 3 Core Drivers	1	5	B	10
D-2	C-20	4 Core Drivers	1	5	B	11
D-3	C-1	Word Rate Counter	1	5	B	Present & 3
D-4	C-2	Word Rate Counter	1	5	B	Present & 2
D-5	M-23	8:1 Count Sync	1	10	B	10
	M-24					
D-6	M-25	1/2-65:1 Count Sync	2	10	B	11
D-7	M-26	16:1 Count Sync	1	10	B	11
D-8		Dig. Mpxr Gates	4	18	A&B	40
D-9		Trans. Data Storage	1	18	B	11
D-10		Trans. Data Storage	1	18	B	10
D-11		Programmer	1	17	A/B	18
D-12		Programmer	1	17	A/B	20
D-13		Programmer	1	17	A/B	19
D-14		Programmer	1	17	A/B	20
D-15		Programmer	1	17	A/B	18
D-16		Programmer	1	17	A/B	27
D-17		Programmer	1	17	A/B	26
D-18		Coder Control	1	16	A/B	7
D-19		1 CPS Reset	1	16	A/B	9
D-20		1 CPS Reset	1	16	A/B	27
D-21		Time Code Strobe	2	16	A/B	8
D-22		Time Code Strobe	1	16	A/B	15
D-23		I. D. Buffer	1	16	A/B	10
D-24		Dig. Mpxr Pwr Strobe	1	17	A/B	9

Table 7 Printed Circuit Card Utilization

Card Designation	Card Relay out Card Number	Card Designation	Pins Utilized Internal	Connector Pair External
Coder	501292-52	5-B	*	*
Sync	501292-48	10-B	30	---
Miscellaneous	501292-49	16-A	*	10
Miscellaneous	501292-50	16-B	*	---
Programmer	501292-49	17-A	40	---
Programmer	501292-50	17-B	40	---
Dig Mpxr	501292-49	18-A	30	49
Dig Mpxr	501292-50	18-B	30	56

* Exact quantity not determined at present time, but is well under the maximum allowable of 74 pins per card.

1.12 DESIGN PROOF TESTING. - Testing of the modified system was only made to the extent necessary to prove the feasibility of the new design modifications. Testing was divided into three categories which included a design feasibility test, design evaluation test, and a series of mechanical tests. The design feasibility and evaluation tests were repeated under typical temperature variations. In addition, a breadboard demonstration model was operationally tested to conclude the testing program.

1.12.1 Electrical Testing. -

1.12.1.1 The design feasibility test involved operating the system with the new format. Insertion of Time Code and digital data into the format along with synchronizing the system to the master clock at a 1 cps rate was achieved. All digital and analog channels were checked to establish the successful completion of the objective of the study program. Checking the channels was accomplished by using a modified PCM test to compare the value of the output code with a preselected value.

1.12.1.2 The design evaluation test consisted of measuring various parameters to confirm circuit performance. Included in these measurements were pulse widths, rise and fall times, and amplitudes of the switching circuits; voltages and noise levels of the two bias lines; transient characteristics of the counters and shift register stages; and in general any parameter considered indicative of proper circuit operation. The evaluation test was not intended to be a formalized, rigorous, electrical test of each individual circuit as would be expected in a prototype

breadboard, but rather, it was intended to be a test of the inherent good in the feasibility model.

1.12.1.3 The temperature test involved cycling the breadboard modifications between -10°C and 65°C . Certain parameters were measured, where deemed necessary, to establish temperature characteristics for a circuit. Those circuits were the digital multiplexer strobe, the 1 cps reset, and the bias amplifier. In addition, all channels were checked with the test equipment for correct code. To find the limits of operation the temperature extremes were increased to 50°C and 85°C with no failure in the system operation. No critical adjustments were required even under repeated operation at temperature extremes. Power requirements increased by only 220 milliwatts.

1.12.2 Mechanical Testing.—Vibration tests were conducted on the microelectronic integrated digital gate module chips to determine the effect of sinusoidal and random vibrations at the Nimbus specification levels and with a high G shaped input to simulate the effect of structural packaging on the chips. Two module chips were mounted back to back on an epoxy-fiberglass card. The card was then clamped between 80 durometer rubber attached to a cubical vibration fixture (figure 49, View A).

The modules, operating in Nimbus PCM circuitry, were monitored by project personnel using a nimbus PCM simulator. The vibration test procedure was conducted in accordance with the qualification section of NASA Nimbus specification dated December 1962 and the anticipated maximum vibration that the micro

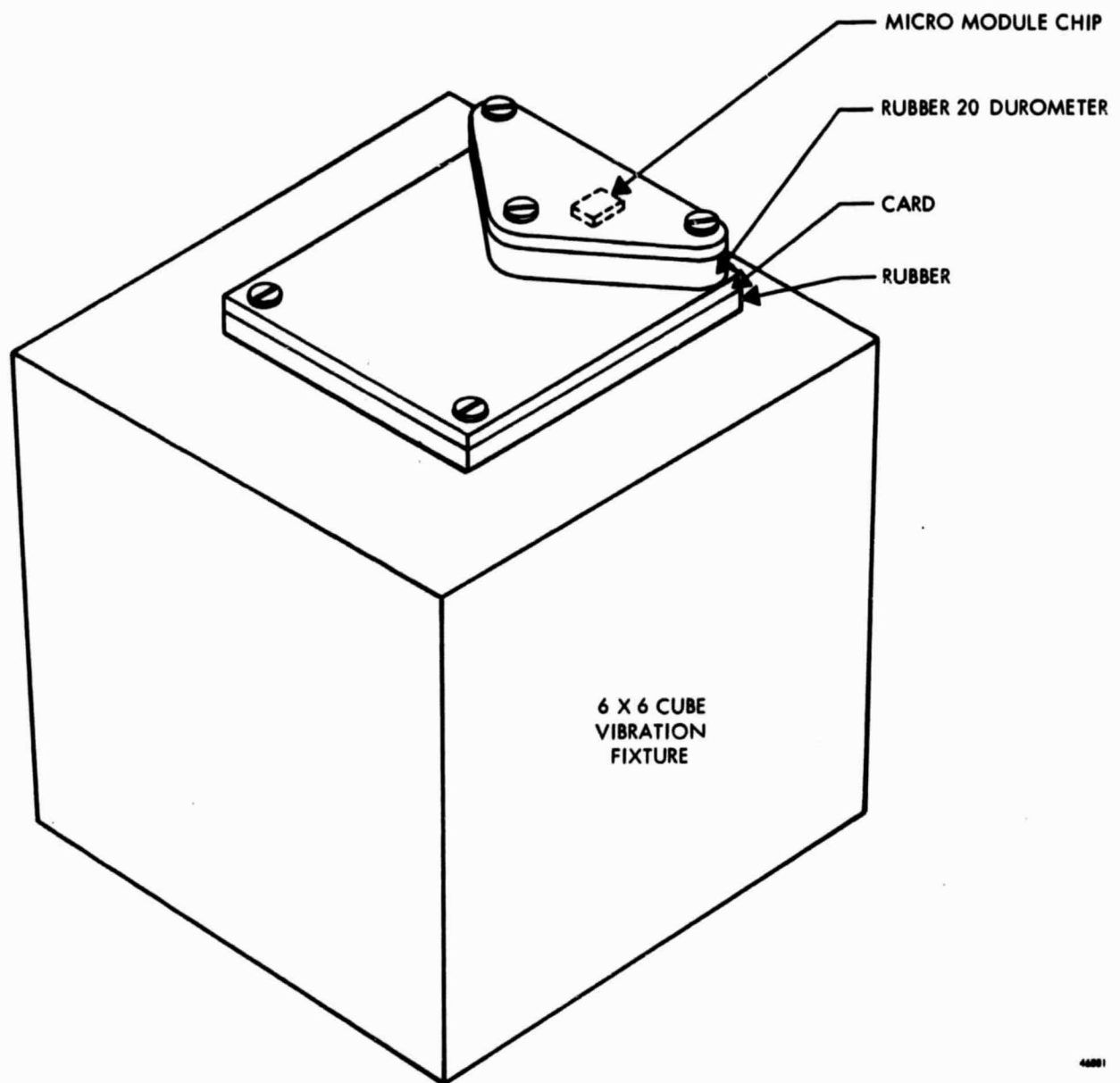


Figure 49. Vibration Tests (Sheet 1 of 3)

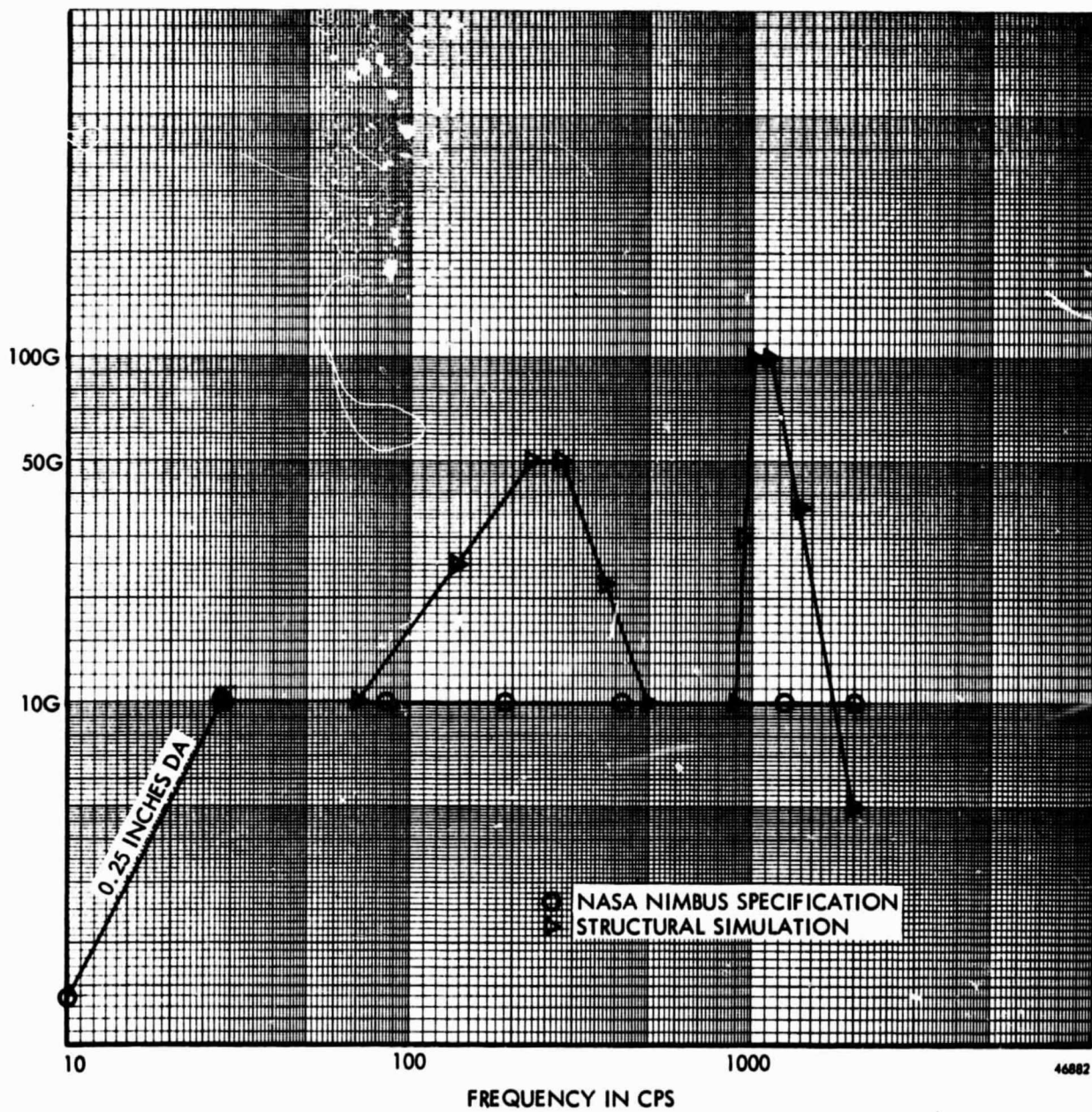


Figure 49. Vibration Tests (Sheet 2 of 3)

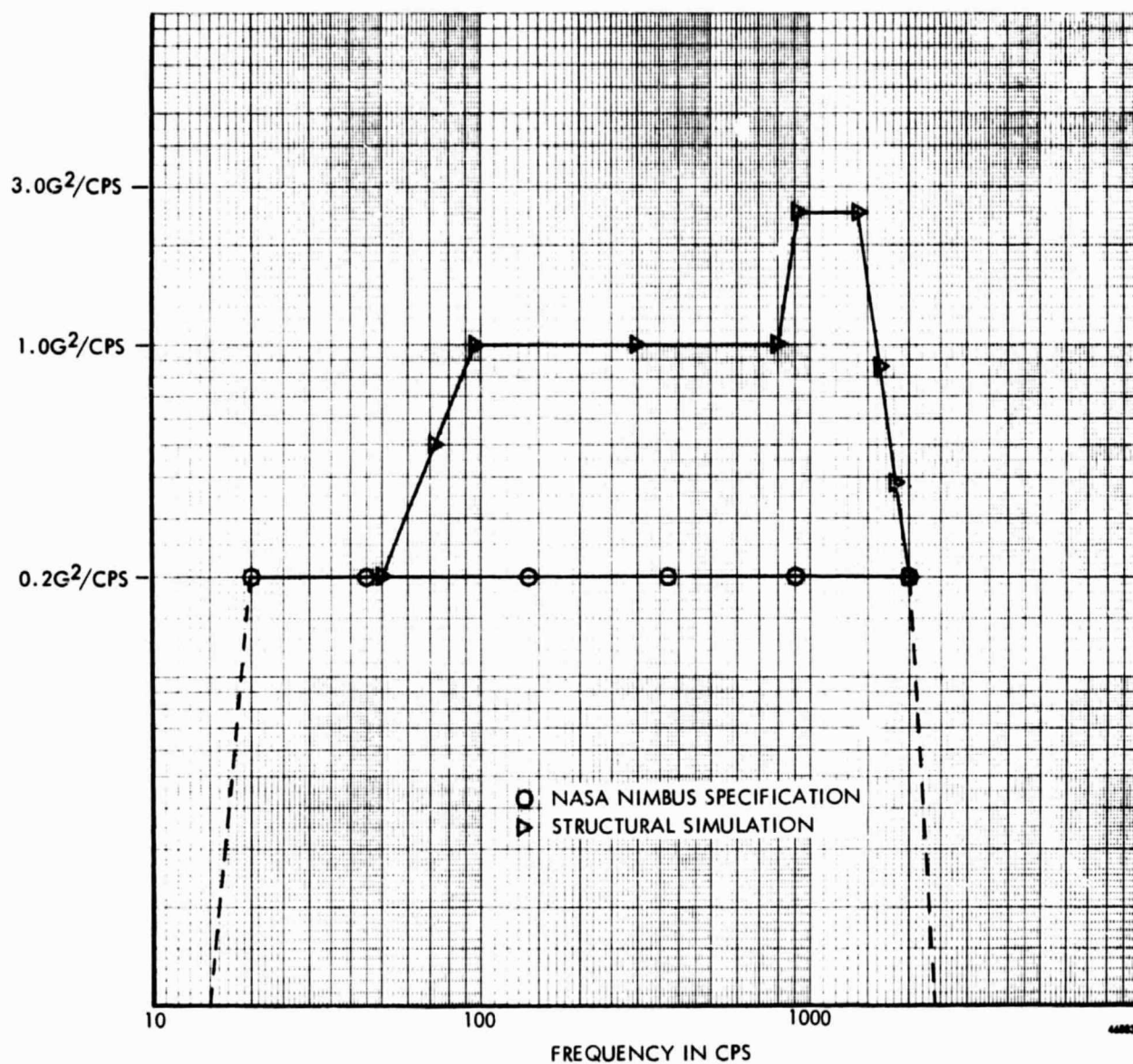


Figure 49. Vibration Tests (Sheet 3 of 3)

module would be subjected to in the typical Nimbus package. These tests were performed along each of the three major mutually perpendicular axes of the chips, serial numbers 2, 7, 16 and 17 as follows:

- a. Test I - Sinusoidal vibration at 10 g peak, limited to 0.25 in D.A. was applied from 5 cps to 2 KCS with a sweep rate of 2 minutes per octave (approximately 17 minutes).
- b. Test II - Random vibration with a power spectral density level of 0.2 g^2/cps over the 20 to 2000 cps band (20 g RMS) was applied for four minutes in each axis.
- c. Test III - Sinusoidal vibration in accordance with the structural simulation curve shown in View B was applied. Axes and sweep rate were the same as Test I.
- d. Test IV - A random vibration input spectrum in accordance with the structural simulation curve in view C was applied. Axes and exposure times were the same as those of Test II.

The samples were vibrated along three axes at Nimbus specification levels (Test I and II) and then along three axes at higher levels (Tests III and IV). No apparent electrical or mechanical degradation resulted from these tests.

1.12.3 Breadboard System Demonstration. - The breadboard model was demonstrated to verify operational capability of the modified PCM system in accordance with the design objectives and compatibility of the outputs with the Ground Station. A test tape format (Appendix VII) was used. The breadboard circuit cards, a modified Multicoder and TME, a Nimbus A Master Clock, and a Nimbus Airborne Tape Transport unit were connected as a system. Unit A output of this system was then recorded utilizing a MINCOM tape unit. This tape was played back into a modified Ground Station where evaluation of Time Code, Digital

Channels, Analog Channels, and Sync was made. Stored Unit A and real time data were recorded using both the gated sine wave and split phase (M) type of codes.

1.13 OTHER AIRBORNE CONSIDERATIONS. - Two further studies were made, one of which dealt with modifications for increased reliability, and the other concerned a modification in the method of modulation. Paragraph 1.13.5 describes the modification for increased reliability. The modulation study is analyzed in the following Paragraphs through Paragraph 1.13.4.

The feasibility of using an NRZ or split phase signal with the Nimbus tape recorder was studied (Reference 9, Paragraph 2, Section 4). The purpose of this study was to obtain a method of recording and playback of Unit A data which would yield a better signal to noise (S/N) than sine wave gating. The extensive modifications to other equipments required for NRZ modulation ruled out this method in favor of split phase modulation. At present the code consists of a 500 cps sine wave which is gated on and off by the NRZ code from the PCM Multicoder. Each sine wave cycle which is gated on corresponds to a "0" in the NRZ code. Because of differentiation introduced by the record-playback head, it was decided to gate the sine wave at the 90° point rather than the zero crossover so that the reproduced signal will more closely resemble a sine wave. As shown in (figure 50) the reproduced signal with code train of 00110011 has an overshoot component caused by differentiation of the fast rise time at the gating points on the input signal. It will also be noted that the first sine wave in a series has a lower amplitude than the succeeding sine waves. These distortions result in a waveform which has poor signal to noise characteristics.



Figure 50. Sine Wave Gating Illustrating Overshoot

In Technical Report No. 8 prepared by the Radiation Advanced Communications Group, a recommendation was made to record the NRZ signal from the PCM unit directly. The playback signal, which is differentiated by the record-playback process, indicated that a gain of 7 db in the signal to noise ratio could be expected from the NRZ modulation as compared to the gated sine wave modulation. A breadboard experiment was made to determine the feasibility of the record and playback technique discussed above. The results of the experiment indicated that the present Nimbus tape transport could be used for this method. Results of the experiment and waveform illustrations are included in the Technical Report Number 8. Selection of the type of code to be used in this study was arrived at by consideration of the NRZ method described above; a split phase digital method and feasibility of decreasing the distortion of the present gated sine wave method.

The NRZ method of modulation, while considered to have the optimum signal to noise ratio, had two undesirable properties for overall system operation. The first of these is that the beacon transmitter would have to be redesigned to accommodate dc coupling of the modulation signal (Appendix VI). The second is that the ground station synchronizer would have difficulty in maintaining sync in the event of a large number of data words containing all 0's (since there would be no transitions in the modulation signal during this period). Some method of decreasing the distortion of the present sine wave signal might prove to be the easiest modification to perform, but it was felt that the anticipated gain in signal to noise ratio was not sufficient to warrant concentrating on this particular

method (Appendix VII). The split phase method offers an increase in signal to noise ratio approaching that of an NRZ signal and can be ac coupled to the transmitter. It also offers the advantage of having at least one amplitude transition for each bit time and would also eliminate the requirement for the "A" unit modulator in the Telemetry Electronics. A split phase MARK code that changes phase for each "0" in the code was selected as requiring the fewest changes in the ground station logic. A diagram of the various code wave forms is shown in figure 51.

1.13.1 Circuit Design.-The technical effort on improving the characteristics of the Nimbus tape recorder system was divided into four major categories; recording technique, playback technique, system modification and test equipment modifications. The present Nimbus system uses an analog recording technique whereby the data signal is added to an ac bias signal. This type of recording permits the signal to be stored on tape with less distortion than other methods and is the most commonly used recording technique with sinusoidal or audio type signals. However, when a square wave signal is fed to the Nimbus recorder, the resulting playback is responsive only to the transitions of the recorded signal. Due to this fact and because there were other advantages to be gained, a digital recording method was employed for the modified recorder system. The digital recording is accomplished by saturating the magnetic tape to either the negative or the positive extremes for every data transition. The play back signal is similar to that obtained by the analog recording method. The use of digital recording with the split phase M signal offers several advantages. The new record amplifier is

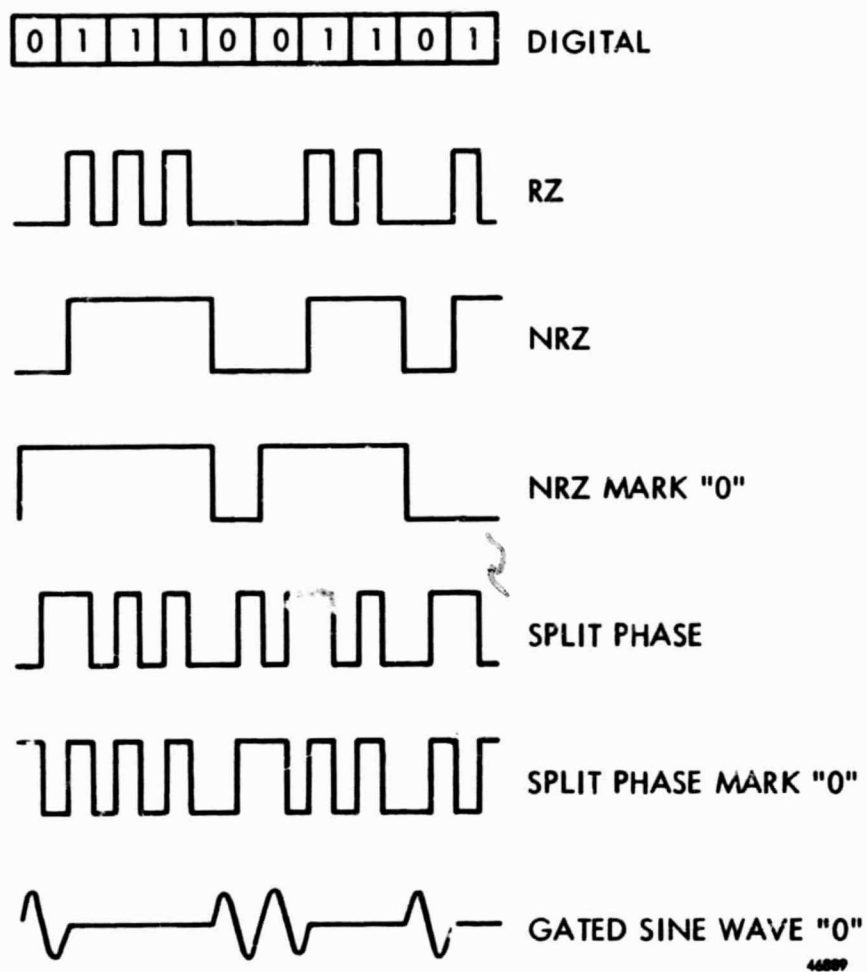


Figure 31. Digital Codes

smaller in size requiring only one module, whereas the present method uses a module for the record amplifier and a module for the bias oscillator. The operation of the digital record amplifier is less critical than the analog arrangement, which requires a select at test component and a gain adjustment potentiometer. Aside from the improvement in circuit performance using the digital recording method it is possible to obtain improved signal and noise characteristics. A maximum playback signal is recovered from the tape because the recorded signal causes the tape to swing from negative saturation to positive saturation. Furthermore, noise is reduced since the tape is held in saturation at all times, except for the data transitions. Noise can be superimposed on the signal only by being of sufficient amplitude to bring the tape out of saturation. The analog method is susceptible however, to noise being superimposed on the signal since the recording range is within the linear range of the tape magnetization curve. The analog record amplifier is also more susceptible to noise on the input due to Class A operation and a high input impedance. On the other hand, the digital record amplifier uses large signal swings from a buffered flip-flop to saturate the input stages. The saturating stages require more input noise energy than the analog stage before recording noise on the tape.

- 1.13.2 Record Amplifier (See Figure 52).—Transistors Q1 and Q2 act as gates for the current sources Q4 and Q3 respectively. When Q1 saturates it supplies base drive to the current source Q4. The current source pulls the record current through the gate (Q1) and the record winding. Diode CR2 prevents gate Q1

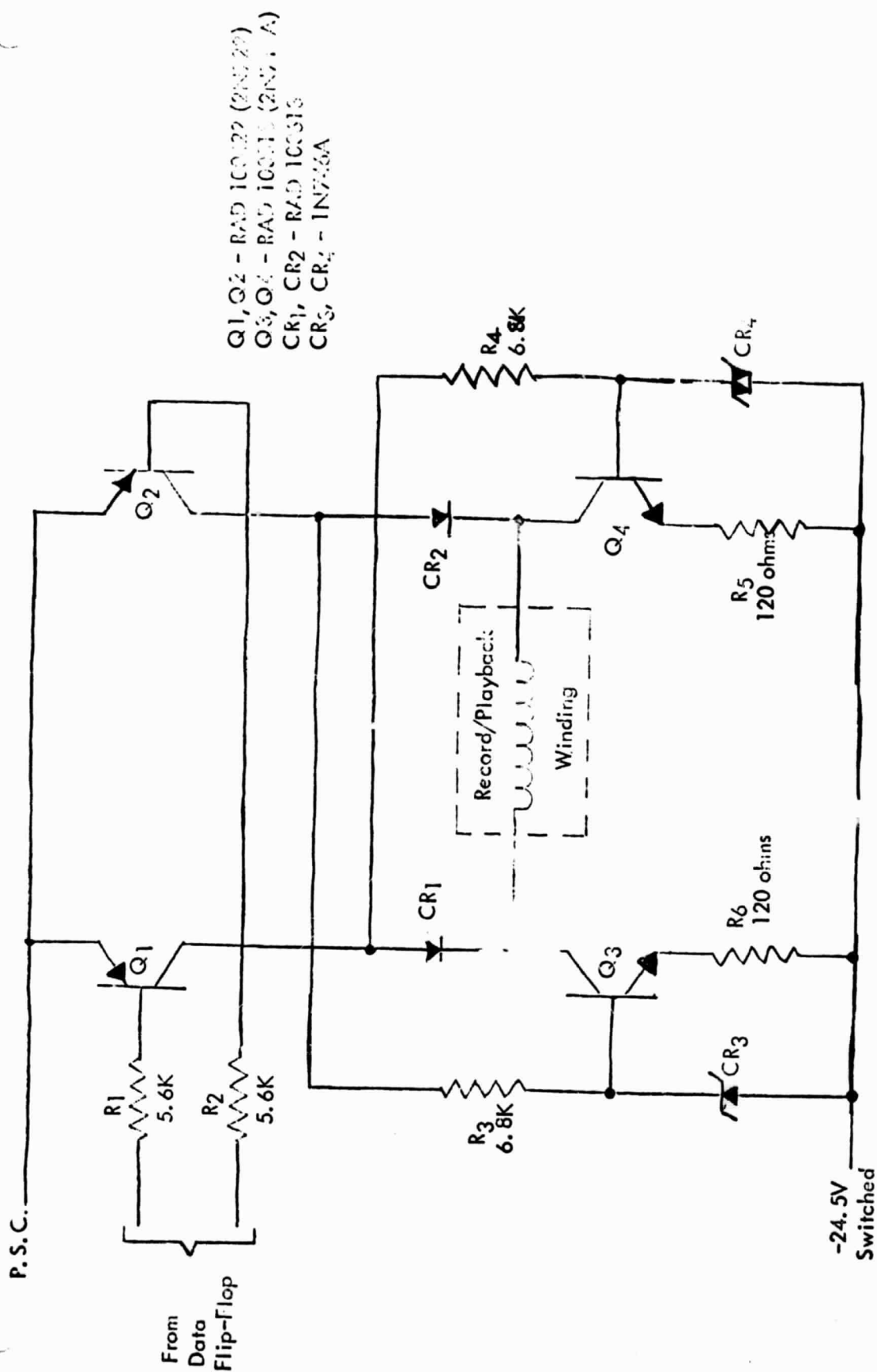


Figure 52. Nimbus Record Amplifier

from also supplying base drive to current source Q3. To reverse the polarity of the record current the gate transistor Q1 turns off and the other gate transistor Q2 saturates. The same sequence of events follows as before with the record current being pulled through the winding in the opposite direction by current source Q3. The record current necessary to saturate the tape was found from experimentation to be around 12 ma. To insure that tape saturation does occur R5 and R6 were calculated to give about 20 ma of record current from each current source. The current sources are temperature stabilized by the use of 1N746A zener diodes (CR3, CR4) which have a negative temperature coefficient close to that of the base emitter junctions of Q3 and Q4.

- 1.13.3 Playback Amplifier (See Figure 53).— Because of the recorder characteristics, the playback signal cannot be used directly off the playback head. The square wave is effectively differentiated by the playback action where E_{out} of the winding is proportional to $\frac{d\phi}{dt}$. Furthermore, the playback winding acts as a low pass filter resulting in different amplitude pulses for the two fundamental frequencies of the split phase M signal. To offset the limitations of the recorder when using the digital signal, a high gain, frequency compensated amplifier was used to drive a pulse shaping circuit. The end result is a square wave split phase M signal identical to the recorded signal except for the 30 times increase in bit rate frequency. The playback signal from the recorder winding is fed differentially into the input amplification stage. The differential input eliminates most of the low frequency common mode noise

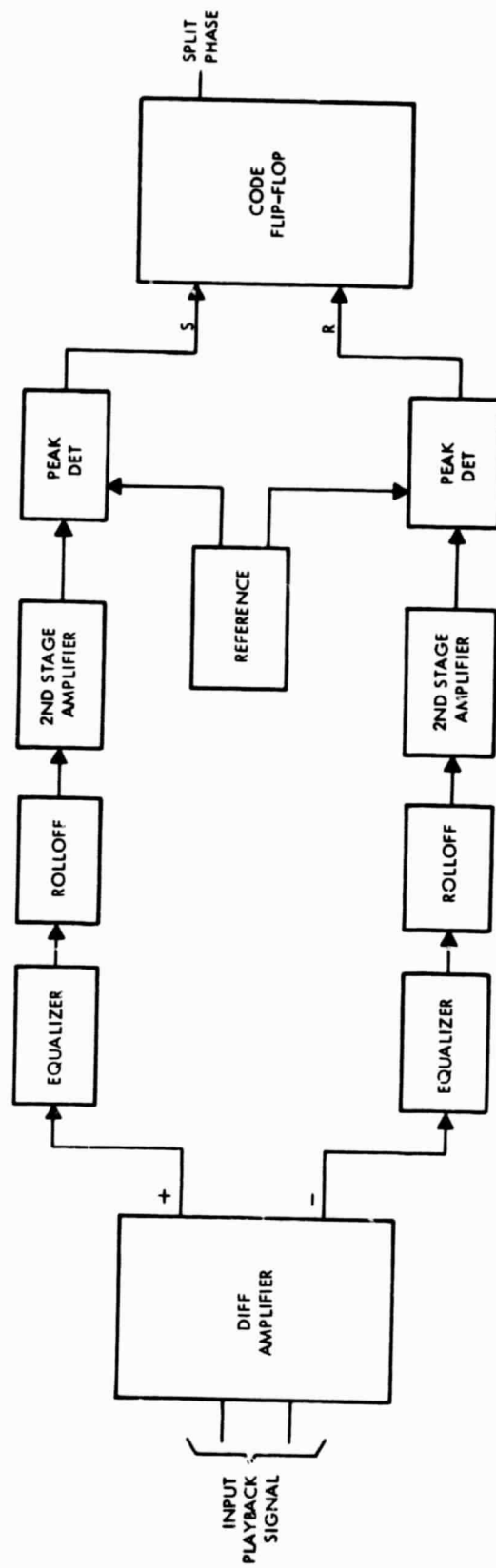
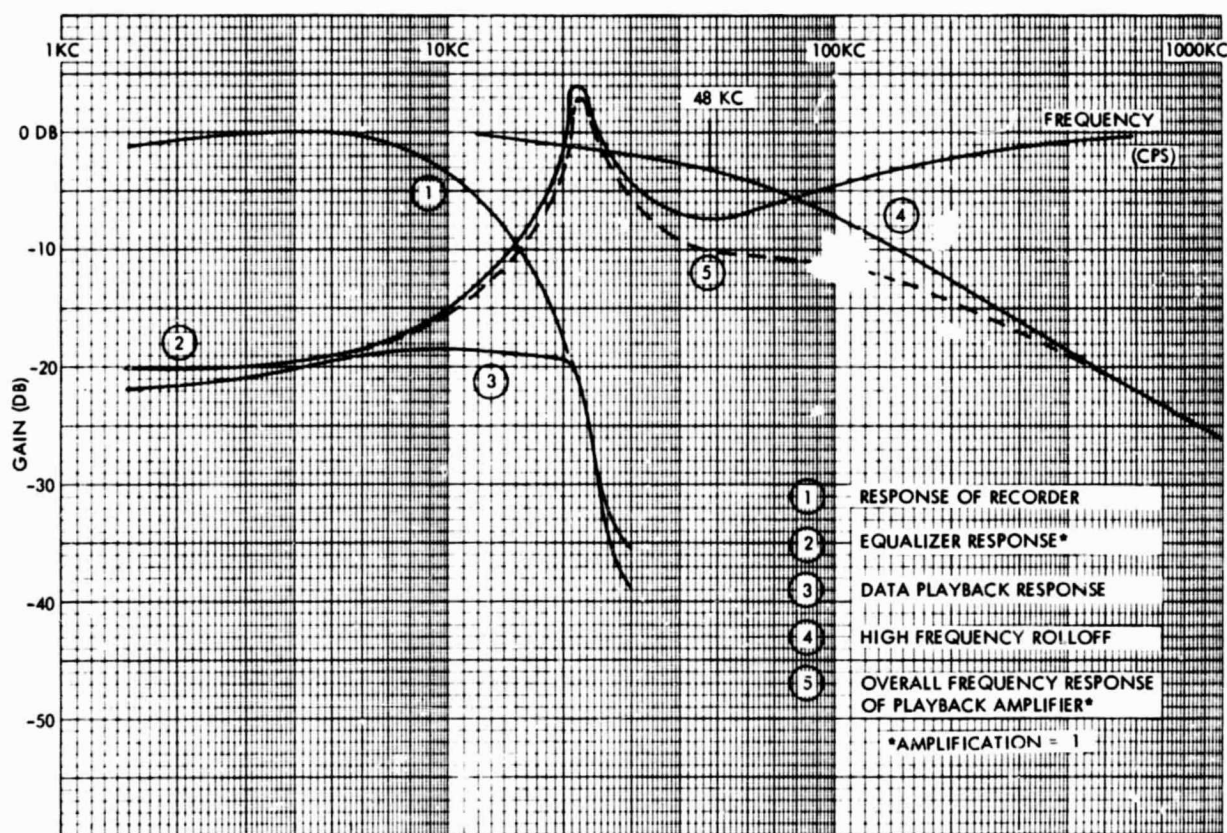


Figure 53. Nimbus Playback Amplifier Block Diagram

coming from the recorder drive motor. The output of the amplification stage is double ended to give a positive signal and a negative signal. These two signals are fed into the equalization networks. The purpose of the equalization network is to compensate for the frequency characteristics of the playback head. The recorder playback response curve 1 (figure 54) is shown to have poor response at the data fundamental frequencies of 7.5kc and 15 kc. The response of the equalization network, (figure 54) curve 2, improves the response characteristics so that the playback is ± 0.5 db between 5kc and 20kc. The playback response is shown in curve 3. The output of the equalizer was observed to have high frequency noise riding on the signal and occasional high peak impulse noise spikes. Because the method of pulse shaping involved differentiating, the presence of noise on the signal was highly undesirable. Therefore, a high frequency RC roll-off circuit was inserted between the equalizer and the second amplification stage. The second amplification stage provides the gain to increase the equalized signal to about 6v pp. It consists of a single stage amplifier having a high input impedance and a constant gain over the frequency and temperature ranges encountered in the system. The signal from the second amplification stage is fed to the peak detecting circuitry where it is clipped at about four volts and differentiated. The clipping reference is a simple voltage divider which is used to bias the differentiator so that only the positive peaks of the signal will be differentiated. The differentiator output crosses a zero reference at the peak of the input signal, since the slope of the signal is zero at the peak. The output has a



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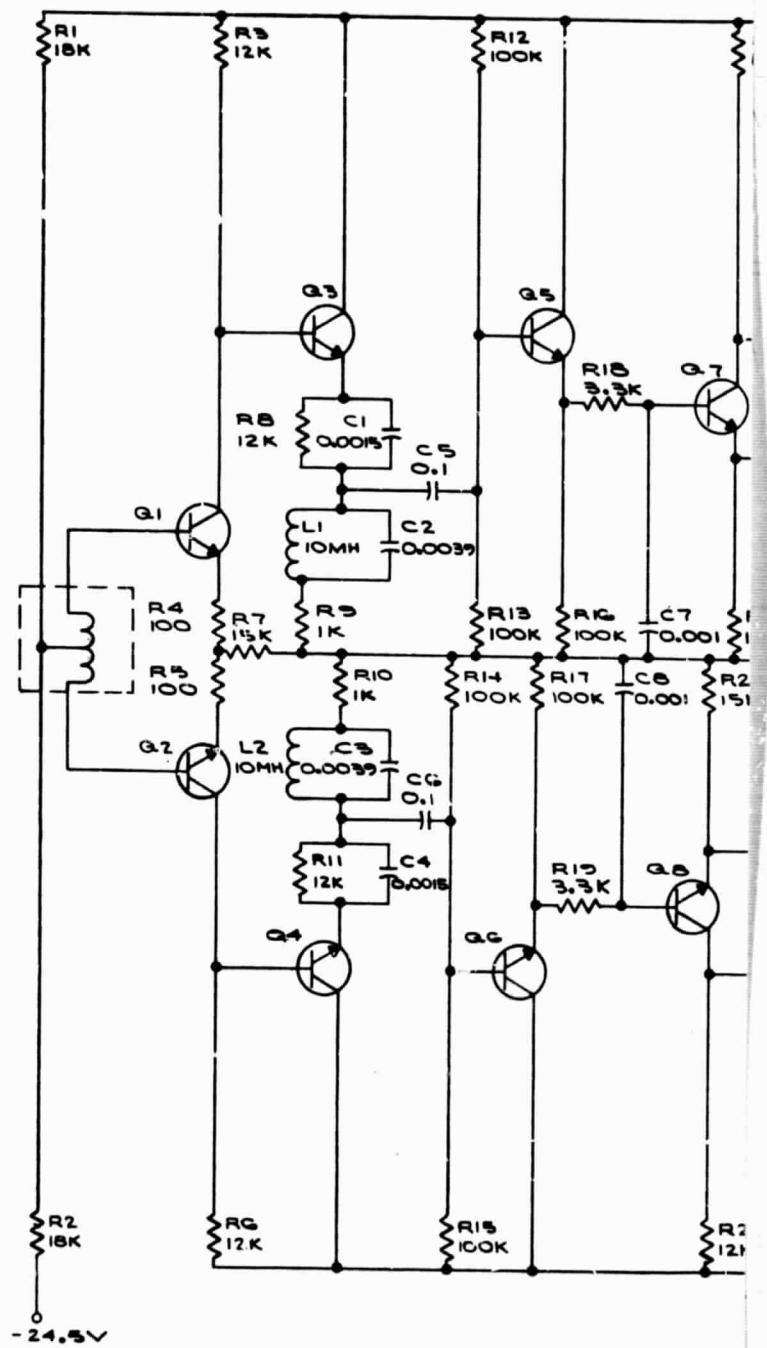
Figure 54. Nimbus Recorder Frequency Characteristics

positive slope at the zero because of inverting action of the differentiator crossing and this slope is used to trigger the code flip-flop. Because both the positive and negative phases of the signal are compensated and differentiated, a positive trigger pulse is obtained for every peak of the playback signal. The positive peak of the playback signal causes the flip-flop to be set and the negative peak of the playback signal causes the flip-flop to be reset. In this manner the split phase mark code is regenerated from the recorded data. Since the playback amplifier reconstructs the recorded signal using peak detection, it is compatible with any other type of recorded bilevel code such as NRZ or RZ type code.

1.13.3.1 The functional blocks of the amplifier (figure 53) are correlated with the schematic diagram (figure 55) as follows:

- a. Differential input amplifier stage is Q1 and Q2 circuits.
- b. Positive and negative equalization stages are Q3 and Q4 circuits.
- c. Positive and negative rolloff stages are Q5 and Q6 circuits.
- d. Positive and negative output amplifier stages are Q7 and Q8 circuits.
- e. Positive and negative peak detectors are Q9 and Q10 circuits.
- f. Clipping reference level are Q11 and Q12 circuits.
- g. Output code flip-flop is Q13-A14.

1.13.3.2 The differential input amplifier Q1 and Q2 was utilized primarily to eliminate common mode recorder noise from the playback signal. Since the signal from the recorder is fairly low level, ranging from



NOTES:

1. PARTIAL REF DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NO. OR SUBASSY DESIGNATION.
2. UNLESS OTHERWISE SPECIFIED, RES VALUES ARE IN OHMS, $\pm 5\%$ TOL, $\frac{1}{4}$ W. CAPACITANCE VALUES ARE IN MICROFARADS.
3. UNLESS OTHERWISE SPECIFIED, Q1 THRU Q10 ARE 100B23 (2N230), Q11 & Q12 ARE 100G07, L1 THRU L4 ARE ALADOIN 22-10S.

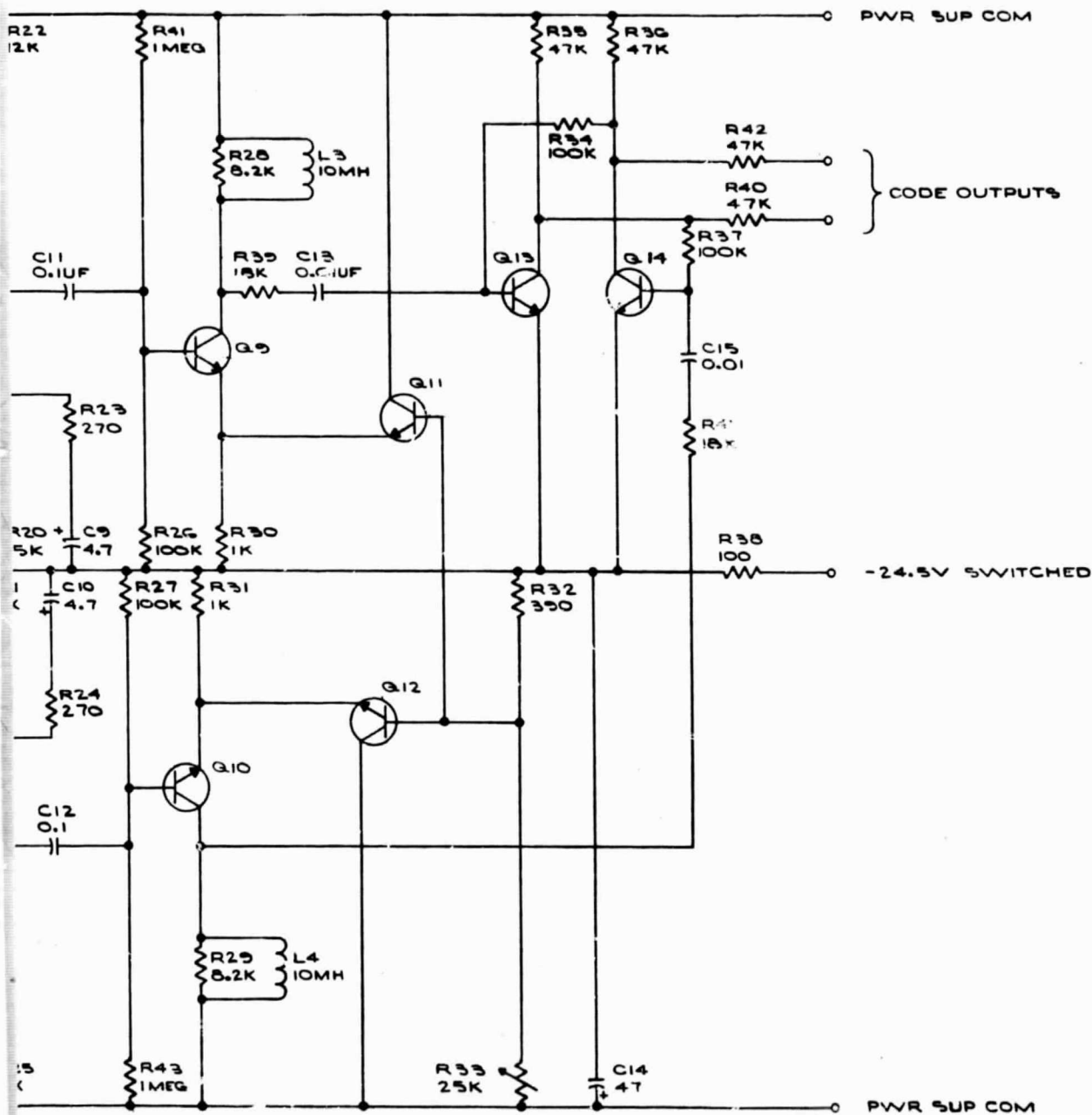


Figure 55. Nimbus Playback Amplifier Schematic Diagram

46mv at 4.5kc to about 0.8 mv at 30kc, the differential input must also have sufficient gain to drive the equalization networks. Otherwise, the attenuation characteristic of the equalizers would reduce the signal level down close to the high frequency noise level and would make the high frequency roll off less effective. By using high gain transistors (2N930) for the differential amplifier, a circuit gain of approximately 50 is obtained. The input impedance of the amplifier is about 20k. Bias current to the bases is supplied by the voltage divider R1 and R2 through the playback winding. This arrangement gives a common mode bias current and helps maintain balance between the two input stages. The output of the differential amplifier is double-ended, providing positive and negative signals to the two equalization circuits.

- 1.13.3.3 The two equalization circuits, Q3 and Q4, are used to improve the poor frequency response of the recorder. The equalizers are identical, one being for the positive output signal of the differential amplifier and the other for the negative output signal. The equalizer circuit consists of an emitter follower input, and an R-L-C network. The emitter follower prevents the equalizer from loading the input amplifier and also acts as a low impedance driving source to the R-L-C network. The frequency response of the recorder before equalization is shown in figure 56. This curve was obtained by recording a square wave signal and measuring the playback signal. Figure 56 also shows

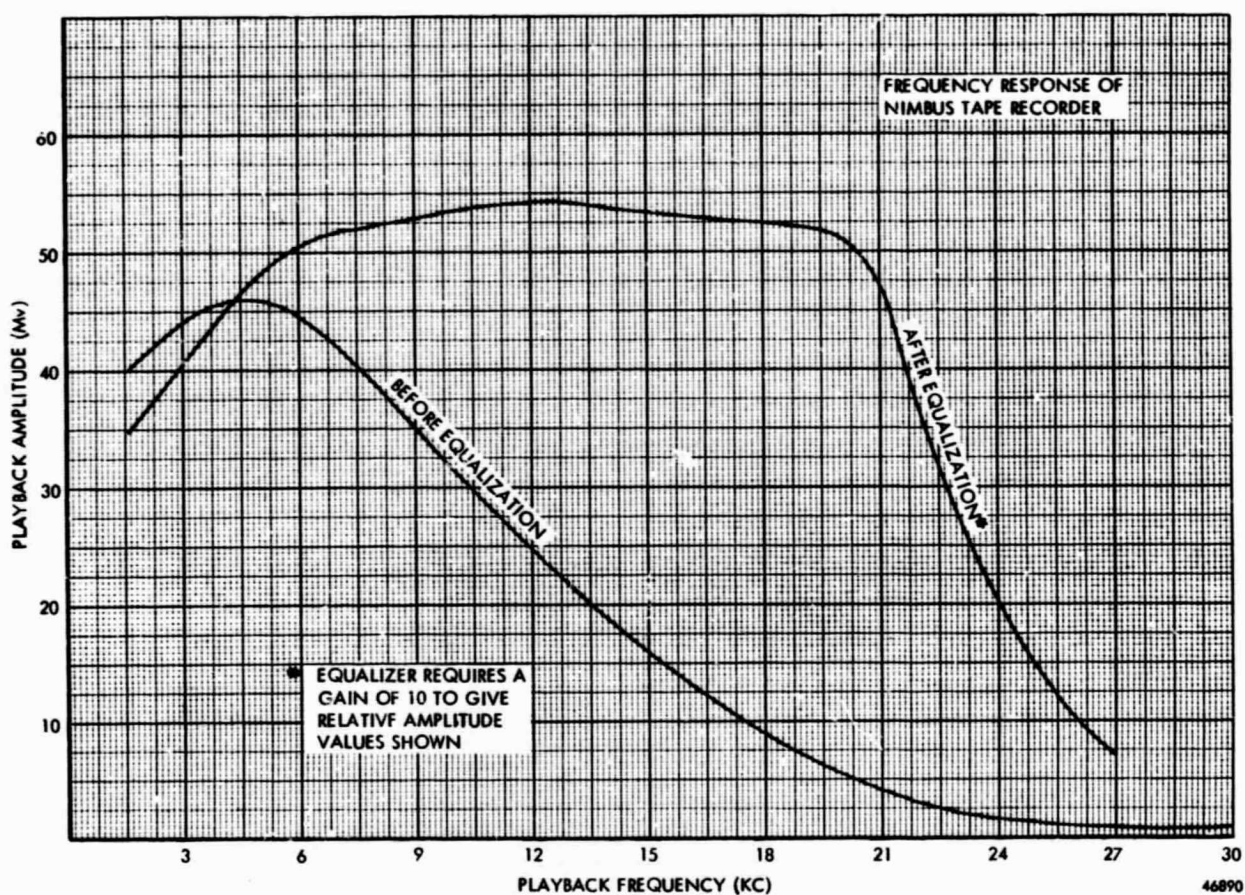


Figure 56. Nimbus Playback Frequency Response

the results of the equalization. This curve was obtained by using an input sinusoidal signal having a response identical to that of the playback signal. The relative amplitudes shown require an amplification of 10 for the equalizer. The actual response of the R-L-C equalizer networks is shown in figure 54, curve 2. Curve 3 of the figure is the overall response of the playback signal after equalization expressed in decibels. The R-L-C network has two major frequency characteristics. The R8, C1 impedance begins a 6 db/octave decrease at the corner frequency of 8.8kc and the L1, C2 circuit resonates at about 22kc. At the lower frequencies the equalizer output voltage is attenuated by the ratio of R8 and R9 plus the impedance of the L1, C2 circuit. As the frequency increases, the shunting effect of C1 causes the impedance ratio of R8, C1 to R9+ L1, C2 to be less attenuating. Increasing the frequency higher, the L1, C2 circuit begins approaching resonance, and its impedance becomes very large which further decreases the attenuation. Passing through the resonant frequency for the tank circuit the output signal approaches the input, since both C1 and C2 act as low impedance shunts and the network is approximately a 1 k load across a driving source. The output signals of the equalizers are fed to the high frequency roll-off circuits.

- 1.13.3.4 The roll-off circuits Q5 and Q6 consist of ac-coupled emitter followers with RC networks coupling to the second amplification stages. As with

the equalization networks, the emitter follower inputs prevent loading the equalizers with the RC roll-off circuits and also provide low impedance driving sources for the roll-off circuits. AC coupling of the emitter followers was necessary, since the dc level of the equalizer outputs is about 1.5 v above the -24.5 v switched level. The RC circuit of R18 and C7 has a 6 db/octave attenuation with a corner break frequency of 48kc. A plot of this circuit's characteristics is shown in figure 54, curve 4. The combined frequency response for the equalization and roll-off circuits is shown in figure 54, curve 5. By using the 48kc break, high frequency noise on the playback signal is effectively suppressed without degrading the data response characteristics.

- 1.13.3.5 The second amplification stages Q7 and Q8 are fed directly from the roll-off circuits. They obtain dc bias from the emitter followers Q5 and Q6 through the resistors R18 and R19. The gain of the amplifiers is about 35 which provides outputs of approximately 6 v pp. The outputs of the amplifiers are ac-coupled to the peak detection circuits through C11 and C12.
- 1.13.3.6 The peak detection circuits and the code output flip-flop reconstruct a square wave split phase mark code train from the playback signal. The peak detection circuitry consists of the two differentiators Q9 and Q10 and the two emitter follower reference outputs Q11 and Q12. The input signals from the second amplification stages are referenced to

about 2.4 v above the -24.5 v level by the 10 to 100k voltage divider. The emitters of the differentiators are biased to a reference voltage so that the peaks of the playback signal can be clipped. This reference voltage is established by the 390 ohm resistor R32 and the 25k pot R33 and is buffered by Q11 and Q12. The clipping level is varied with the pot so that a 2 v peak is clipped from the incoming signal. The output of the differentiator is $E_o = \frac{di}{dt}$ where $i = ER$ and where E is the clipped playback signal and R is the 1k value emitter resistors of the differentiators. The output then becomes $E_o = LR \frac{dE}{dt} = K \frac{dE}{dt}$. With a sinusoidal signal, the true peak is characterized by having a zero slope so that $\frac{dE}{dt} = 0$ at the peak. The differentiator outputs are fed into the flip-flop, Q13 and Q14, to generate the split phase mark code train. Because the differentiator outputs are inverted, the zero crossover $\frac{dE}{dt} = 0$ has a positive slope and the outputs are directly ac-coupled to the flip-flop through C13 and C15. Since the flip-flop is not a true zero crossing detector, it does contribute to the unequal pulse widths obtained. However, most of the pulse width distortion is due to the phase shift encounter in the playback signal and for this reason more sophisticated zero crossing detectors were not used. The output of the code flip-flop is fed into the combining networks through one of the 47k resistors. A simple RC filter R38 and C14 is used to reduce 100 cycle noise on the -24.5 v switched line.

1.13.4 System Change Requirements. - Several changes in the NIMBUS system other than the record and playback amplifiers were required. These changes included deletion of several existing modules, modification of the Time Code amplifier and the combining network and replacing the RZ-NRZ converter with an RZ to split phase converter. A block diagram of the present and proposed record-playback system (figure 57) shows the only required change to the Multicoder unit is replacement of the RZ-NRZ converter module by an RZ to split phase converter module.

The changes to the Telemetry Electronics includes the elimination of the four- unit A modulator modules and the replacement of the record and playback circuitry modules by a digital type record amplifier and a playback amplifier which will restore the differentiated playback signal to a square wave split phase type of signal. The A real-time signal will be combined with the 10kc Time Code signal in the same manner as that of the gated sinusoid signal and will require only minor changes to the Time Code amplifier circuitry. The Time Code Amplifier module 112, which amplifies the combined 10kc Time Code and unit A real-time signals, requires an increase in the size of the coupling capacitors in order to prevent differentiation of the split phase real-time signal. The changes required are an increase in size of C2 to .47uf and increase in size of C3 to 10 uf.

The combining network module 18 requires a reduction in the size of bypass capacitor C1 from .001uf to 100pf in order to prevent excessive integration of the high frequency components of the split phase output signal.

The RZ to Split Phase Converter (figure 58) converts the RZ output from the output

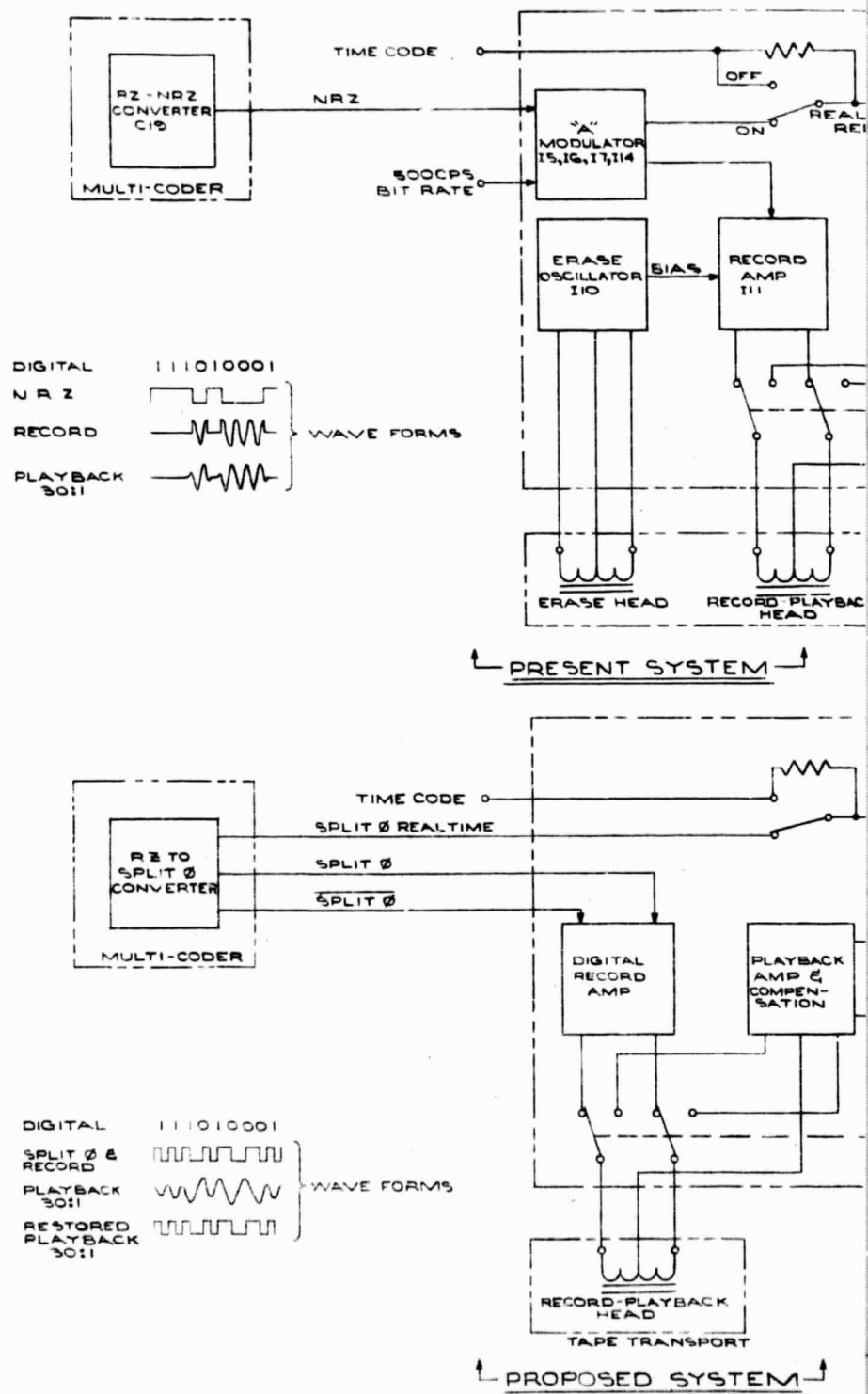
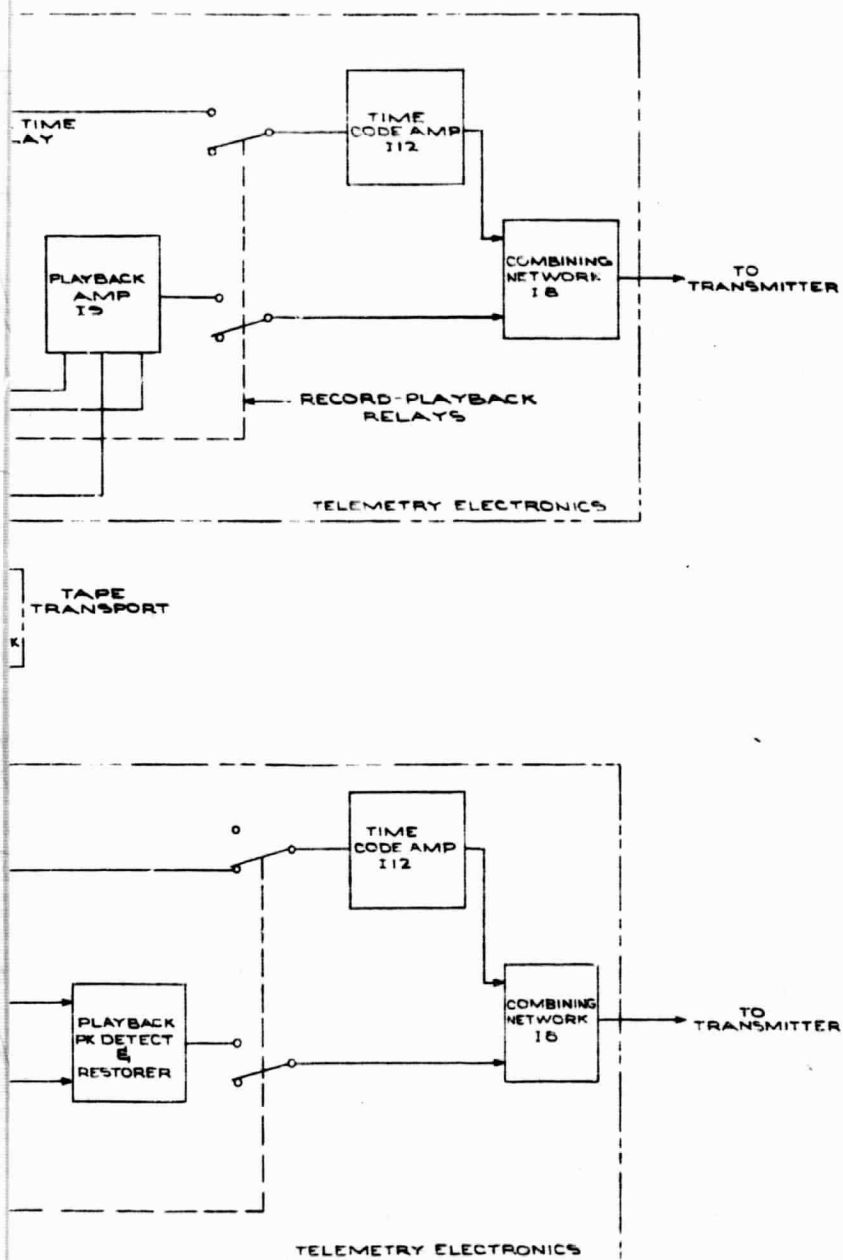


Figure 57. Present and proposed systems.



NOTES:

1. PARTIAL REF DES ARE SHOWN FOR COMPLETE DES PREFIX WITH UNIT NO. OR SUB ASSY DES.
2. UNLESS OTHERWISE SPECIFIED RESISTANCE VALUES ARE IN OHMS $\pm 5\%$ TOLERANCE, $\frac{1}{2}$ WATT CAPACITANCE VALUES ARE EXPRESSED IN PICOFARADS
3. UNLESS OTHERWISE SPECIFIED DIODE CR1:CR3 ARE RAD 104E39, CR3 IS RAD 101E56, CR4 THRU CR7 ARE IN791, TRANSISTORS Q1 THRU Q7 ARE RAD 100422, Q8 IS RAD 100318.

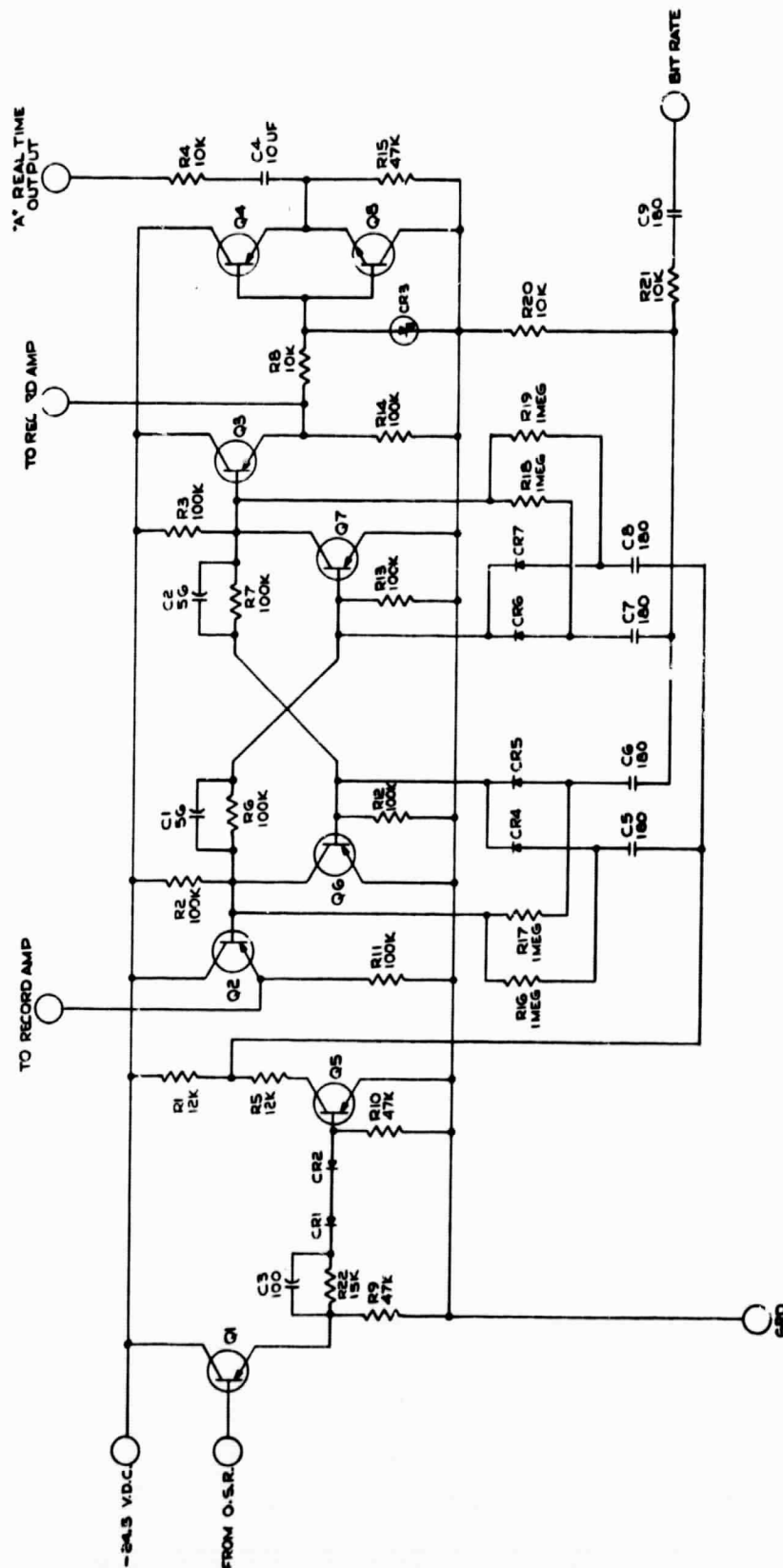


Figure 58. RZ to Split Phase Converter Schematic Diagram

shift register to a 500 cps square wave which effectively reverses phase on a "0" output from the output shift register. The outputs from this module are used to drive the digital record amplifier and the "A" real-time input to the Time Code amplifier. The circuitry used is a modification of C18, the RZ to NRZ converter used in the B Unit. Two signals are Or gated to the count input of a bistable counter circuit. The bit rate input causes a change in state for each positive transition of the 500 cps bit rate. The output shift register input, which is 180 degrees out of phase with the 500 cps bit rate, will cause another change of state for each "1" in the digital output code. The output of the bistable then appears as a 500 cps square wave. If there is no output from the output shift register, which is a "0" condition, the bistable will not change state at this time, and it will appear that the 500 cps output of the bistable has shifted phase. A series of "0"s from the output shift register will appear as a 250 cps square wave. Emitter follower circuits are employed to provide the drive current for the record amplifier from each side of the bistable. A complementary emitter follower circuit is utilized to provide the real-time output to the Telemetry Electronics where it is combined with the 10kc Time Code signal. The negative level of the real-time output is zener-clamped at a negative 6.8 volts.

1.13.4.1 The new record/playback system will require changes in both the PCM package and in the TME packaging. The changes to the Multicoder unit will require a new module assembly for the RZ to split phase converter module. The module size and shape will be identical to the

C19 module which it replaces. The printed circuitry of card 5B will require modification in order to bring out two additional lines to the external harness connector from the converter module. The changes to the Multicoder unit will require new module assemblies for the record amplifier and the playback amplifier. The record amplifier module will be accommodated in the same standard size module as the one being replaced. The new playback will require two standard size modules in place of the single one previously used. There is adequate space for the installation of this extra module since the A unit modulator modules and the erase oscillator module are being removed. The printed circuitry of the Telemetry Electronics module card will require a new layout to accommodate the new record and playback module assemblies. The relay card will not require changes as the switching functions remain the same. The harness assembly between the Multicoder and the Telemetry Electronics will require two additional wires for the two additional outputs from the converter module. The harness assembly between the Telemetry Electronics and the Tape Transport can remain unchanged although there is no longer a requirement for the three leads to the erase head.

1.13.4.2 Test equipment modifications were required for both the PCM Test Set and the TME Test Set. In order for the PCM Test Set to be compatible with the split phase M code output of the PCM multicoder, the logic circuit additions shown in figure 59 are required. The logic operation is to gate bit rate with the split phase and inverted split phase from the PCM unit. These outputs from gates 2A18-3 and 2A18-8 are used to set and reset bistable 2A20-2. The resultant output from 2A20-2 is an NRZ mark code with a transition occurring for each "0" in the code train. The mark code and inverted mark code are then differentiated to produce a negative pulse for each transition in the code. These pulses are OR gated to the input of a 15 μ s monostable which fires and produces a pulse which sets the NRZ output bistable 2A20-1 to the "0" level, and inhibits the differentiated bit rate input to the set "1" side of the bistable. The output of 2A20-1 is now an NRZ code, compatible with the present test set, and can be directed to the normal test set NRZ input circuitry.

The standard ground card circuits required for the PCM Test modification are listed below:

1 each 2 NOR card

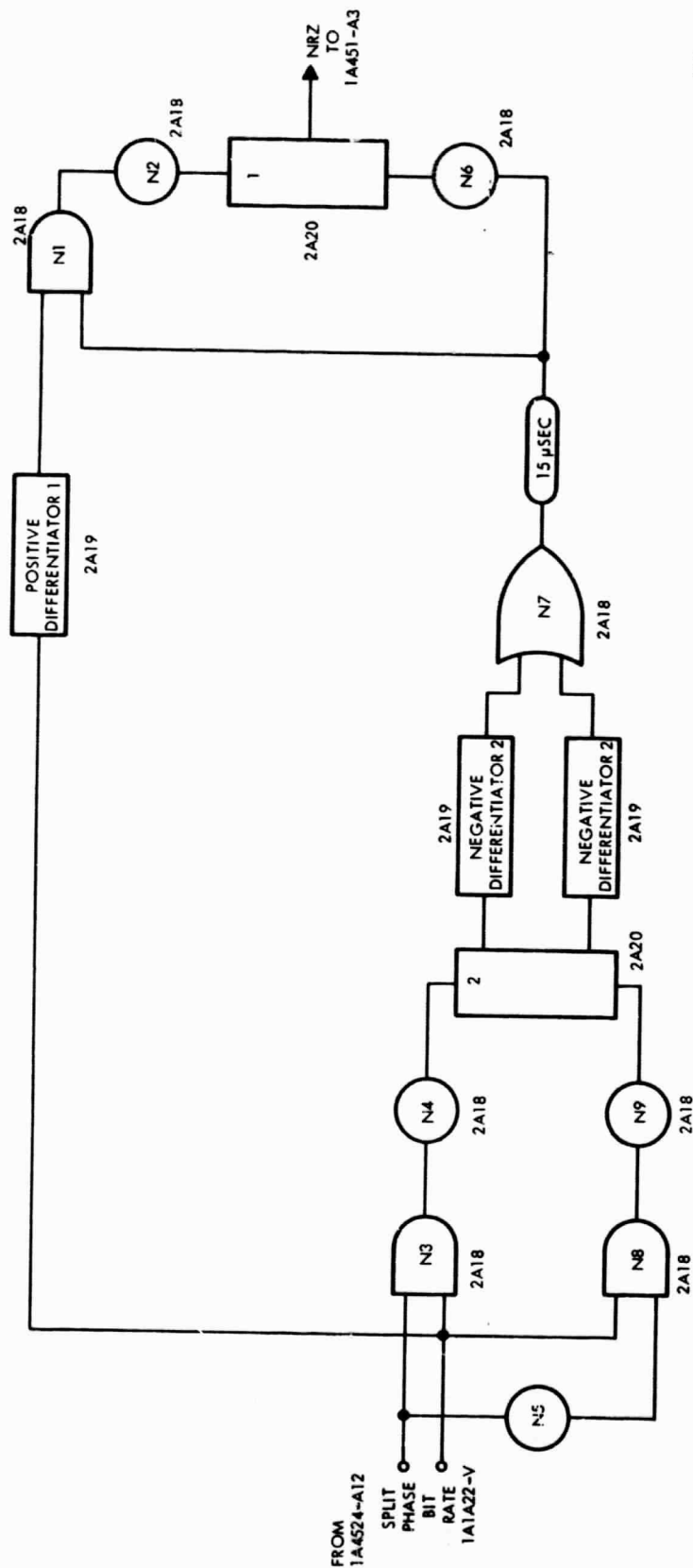
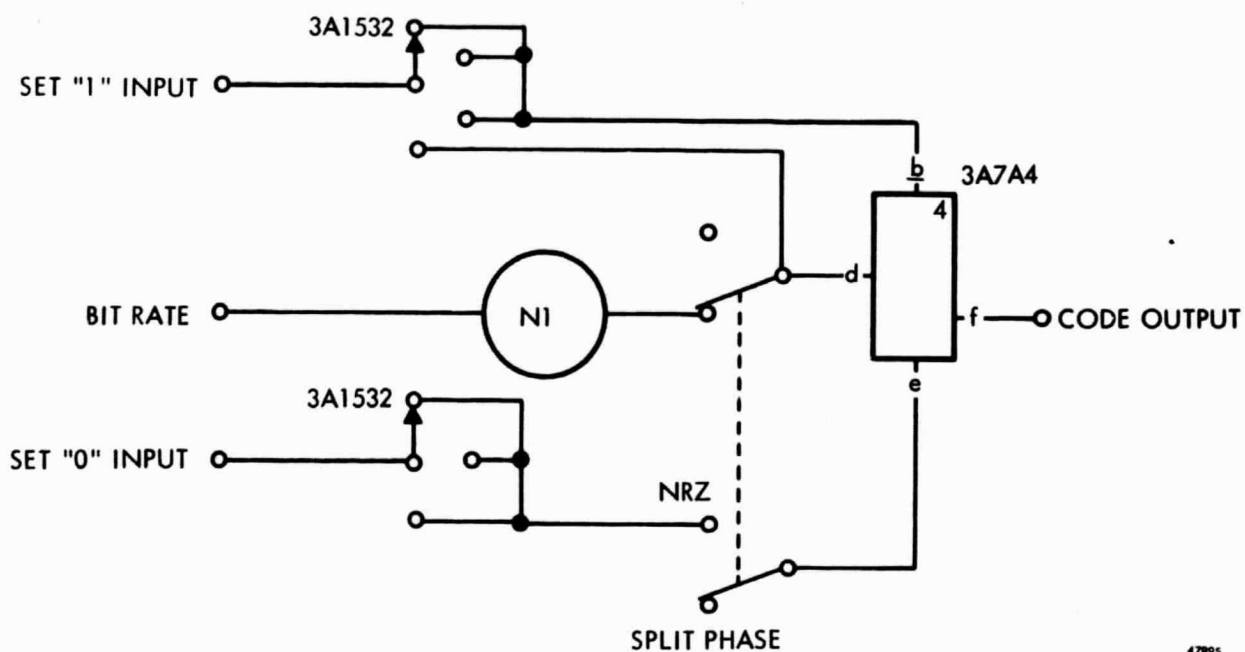


Figure 59. PCM Test Set Logic Additions Split Phase to NRZ Conversion

1 each Differentiator Card

2 each Bistable Multivibrator Card

In order for the TME test set functions to be compatible with the split phase M data PCM output, there are three areas where modification are required. The three areas are "A" unit data detector logic, the simulated PCM word train logic, and the simulated 15 KC playback circuitry. Since the A unit data is now in split phase M code form, it will no longer be necessary to use the data detector logic which formerly converted the gated sine wave to an NRZ signal. This wiring modification is shown in figure 60. The circuit design of the "A" Real Time detector card 3A7A14-7 will be modified to remove the 10 KC Time Code component and put out a split phase square wave signal which can be directly processed by the PCM test set. To provide a simulated PCM split phase M code output, the logic changes shown in figure 61 are required. The "0" set input to the code bistable 3A7A4-4 would be switched out and a count input from inverted bit rate would be switched in. Switch 3A1532 in figure 60 is the OPERATION switch shown in the A Real Time position. Since the playback signal is now a split phase M code, the 15 KC modulator card 3A7A22-2 is no longer required and the output of the split phase converter 3A7A4-4 can be used directly to provide the



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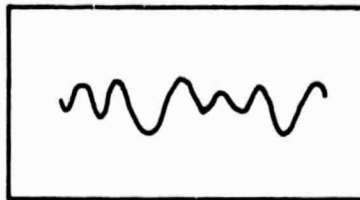
Figure 61. System Test Set Split Phase Output Modification

the simulated playback signal to the dummy recorder head in the test set. This signal will be differentiated by the dummy head to provide a signal similar to that which is provided from the tape transport unit. The only additional materials required to modify the TME test set is a 6-pole double throw wafer switch.

- 1.13.4.3 Testing of the new circuitry included design feasibility testing and design evaluation testing. The design feasibility testing involved operating the new circuits in conjunction with the rest of the system. The purpose of this test was to prove that the method chosen to implement the new record-playback technique had been successful. Various codes ranging from full scale to zero scale were recorded and played back using the new circuits. Having established the satisfactory reconstruction of the playback signal to the split phase M code train, master tapes were made of the system outputs for verifying compatibility with the ground station modifications. Design evaluation testing consisted in making measurements of various parameters to confirm the circuit performance. Temperature measurements were made with the temperature varied from -35°C to $+85^{\circ}\text{C}$, as a safety factor, although the design range was -10°C to $+65^{\circ}\text{C}$. Measurements were made of the gain stability of the stages in the playback

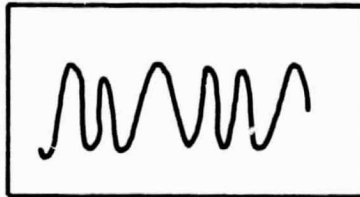
amplifier and of the stability of the record current in the record amplifier. Within the circuit operational range of -10°C to $+65^{\circ}\text{C}$ the gain of the differential input stage increased 14%, the gain of the equalizer varied +28% to -6% from the nominal gain at 25°C , and the gain of the second amplification stage varied +5.1% to -1.7% from the nominal gain at 25°C . The combined effect of the gain drifts of these different stages was an output signal of $5.9\text{V} \pm 0.3\text{V}$, -0.1V or a 0.4V variation in the clipped signal. Although the clipped signal is only 2V the 0.4V variation does not degrade the differentiated output. The code flip-flop performed satisfactorily throughout the design range. The record current varied $\pm 0.5\text{ ma}$ from the two current sources. The peak to peak record current of 37 ma at 25°C represents 18.5 ma from each current source. Figure 62 illustrates typical circuit operation.

- 1.13.5 Modifications for Increased Reliability. - Some work was performed in other areas of the PCM subsystem for increased reliability through modifications which resulted in specific recommendations. This work included modification of Unit B Activate Command circuit, TME Standby Clock modification, and Relay Driver Wiring modification to the TME interconnection cabling.



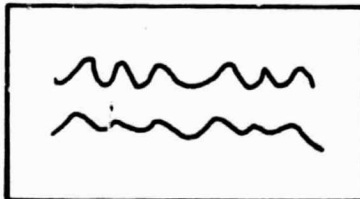
View A

View A shows the output of the differential amplifier. The effect of poor frequency response is evident by the amplitude variation when data changes from "1" to "0".



View B

View B is the output of the second amplification stage after equalization. Slight irregularities in the waveform are due to clipping action of the peak detecting circuits. Improvement in amplitude response is apparent.



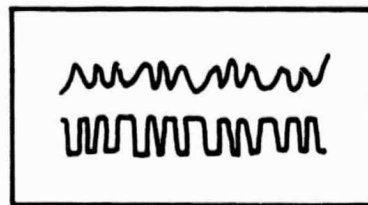
View C

View C shows the equalized output (top waveform) and the unequalized output to illustrate the phase shift of the playback amplifier.

Figure 62. Typical Waveforms (Sheet 1 of 2)

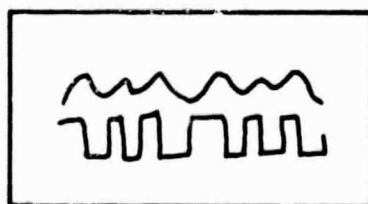


View D



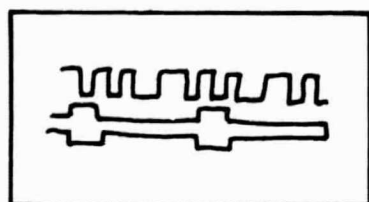
View E

Views D and E show reconstructed split-phase - M, code-train phasing in reference to unequalized and equalized playback signals, respectively.



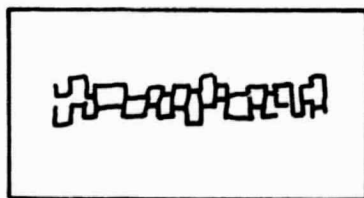
View F

View F also shows reconstructed split-phase data and unequalized playback signal.



View G

View G shows A unit real-time data and time-code signal before addition in the time-code amplifier.



View H

View H is the summation signal of A unit real-time data and time-code from the combining network.

Figure 62. Typical Waveforms (Sheet 2 of 2)

1.13.5.1 It would be advantageous to modify the present Unit B Activate Command circuit (figure 63) to that illustrated in figure 64. During spacecraft integration tests at General Electric Test Facility it was found that noise transients on the command matrix lines to the PCM B unit were activating the B Unit synchronizer reset monostables. On one PCM unit it was also found that the 24 volt amplitude of the command pulse, (originally specified as 12 volts,) was causing premature turn-off of the reset monostable. To correct this problem it was decided to place an isolating relay and filter network between the Unit B command lines and the Unit B command inputs. The added relay and filter components were installed on a special bracket in the Telemetry Electronics as it was not desirable to re-layout the multicode unit to accommodate these components due to cost and time limitations. The purpose of this modification is to relocate the relay in the multicode unit and to eliminate the monostable in the synchronizer reset circuit. The hold in type of relay, which is now located in the Telemetry Electronics, would be placed in a standard 1.64" x 1.13" x .65" foam module and installed on card 4A of the multicode in the space now occupied by a dummy module.

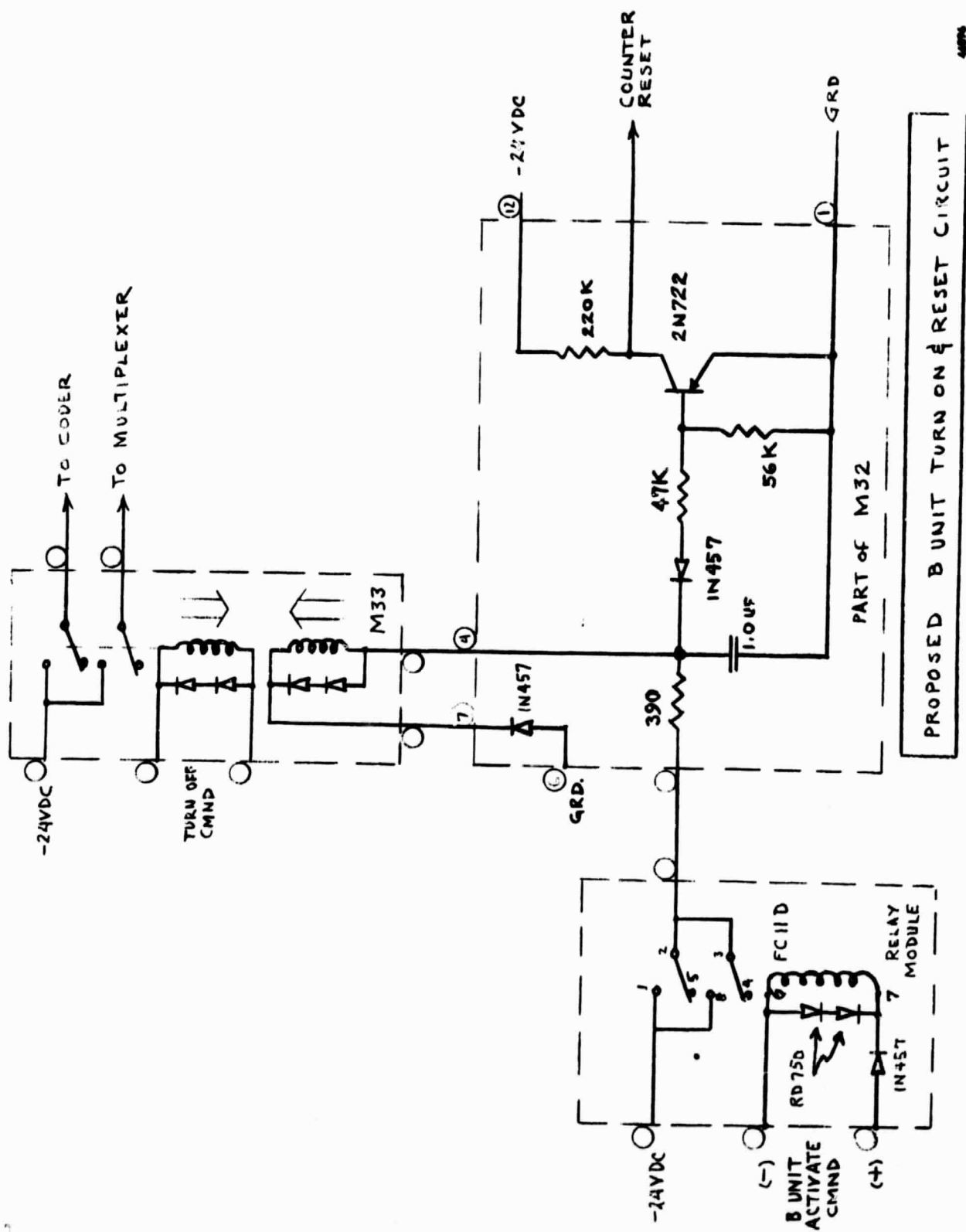


Figure 63. Proposed Unit B Turn On and Reset Circuit

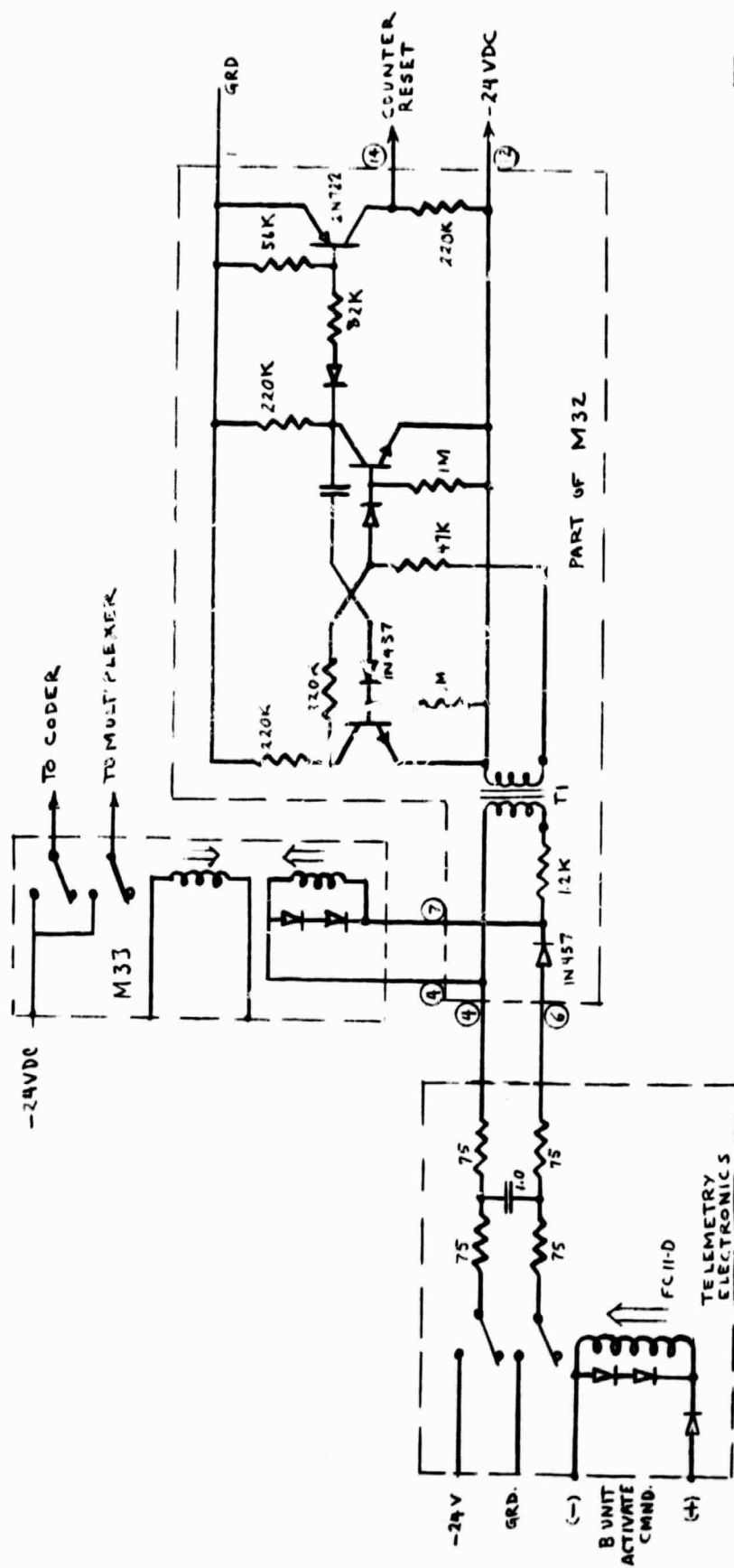


Figure 64. Present Unit B Turn On and Reset Circuit

The -24 volts dc output from the relay contacts would then be routed to a modified M32 module on card 1B. Since the clock matrix command holds in the commanded relay for 60 ± 10 msec, it is not necessary to use a monostable circuit to generate the reset pulse width, as it is only necessary that the reset pulse be wide enough to insure its presence when power is applied to the Unit B Multicoder from the Power-on relay in module M33. Closure time of the Power-on relay is approximately four milliseconds after the closure of the hold-in relay; from this, it appears that a reset pulse width of 10 milliseconds or greater would provide adequate overlap. In the proposed circuit Unit B Activate command energizes the hold-in relay which applies the filtered -24 dc through a 390 ohm resistor to the 460 ohm coil of the latching relay in module M33 and to the base of the reset driver transistor in module M32. The reset driver turns on, which drives the reset line to ground level in approximately 70 microseconds and maintains this level for the duration of the command pulse. The latching relay contacts close approximately four milliseconds after the start of the reset pulse and applies power to the Unit B coder and multiplexer. The 390 ohm resistor and 1.0 μ capacitor provide filtering of -24 volt dc

to maintain the voltage across the latching relay winding at -12 volt dc during any transients which might occur due to contact bounce of the hold-in relay. Present configuration requires manufacture of a special bracket for mounting of the relay and filter components in the Telemetry Electronics as well as interconnection wiring between the Telemetry Electronics and Multicoder units. The advantages of this modification are that it will consolidate the required hardware for the Unit B Command in the Multicoder unit and increase reliability by deletion of the monostable in the reset circuit. The deletion of the monostable will reduce circuit requirements by fifteen components as listed below:

1 Pulse Transformer	2 Diodes
2 Transistors	9 Resistors
1 Capacitor	

The required changes to the Multicoder unit will consist of changes to the printed circuit layout of cards 1B and 4A addition of relay module to card 4A; assembly modification of module M32, and changes to the internal and external harnesses. The change to card 4A will consist of providing for installation of the relay module including input lines from the external connector and an output line to the internal

connector. Module M32 assembly will be changed to eliminate the monostable circuit. The change to the external harness will delete the command lines between the Telemetry Electronics and Multicoder units and provide the matrix command lines to the external connector on card 4A.

1.13.5.2 The Standby Clock modification provides short circuited current limiting protection for the output transistors in the 100 cps outputs of the TME Standby Clock to the Tape Transport motors. A 120 ohm resistor in series with each output line would limit maximum current to 200 ma and eliminate repair costs caused by accidental short circuiting to ground. The modification substitutes a 120 ohm resistor from pin 4 to the junction of Q13 and Q14 emitters, and from pin 3 to the junction of Q3 and Q5 in place of the present connecting ribbons on module 1-4 (501523).

1.13.5.3 The purpose of this modification is to simplify external harness wiring to the Telemetry Electronics. At present, pin 1 of module 1-15 (501524) is connected to the -24.5 volt line through a jumper wire in the external harness. Since -24.5 volts is already routed into the module via pin 8 it would be a simple module assembly change to connect pin 1 inside the module to the -24-volt line. This change

would eliminate the external harness jumper from J1-6, 8 to J4 by substituting on 1-15 (D501524) a welded ribbon from pin 1 to (+) side of CR-9.

1.14 AIRBORNE EQUIPMENT CONCLUSIONS.- No significant problem areas exist to nullify the feasibility of modifying the NIMBUS "B" in accordance with the modifications described in this report. The breadboard demonstration model, using test tapes verified the new and improved capabilities in respect to inclusion of Time Code and digital multiplexing in the output format along with synchronization of the PCM with the spacecraft clock. The study objectives were achieved 100%. A microelectronic analog multiplexer utilizing MOSFET units (See Section 2) is feasible and offers significant size and reliability advantages over the present multiplexer at slightly increased power requirements. Conclusions are summarized in paragraphs 1.14.1 and 1.14.2.

- 1.14.1 a. Modified Multicoder Power Requirements - Power increase over the existing multicoder is less than 250 milliwatts.
- b. New Packaging - External dimensioning will not change. Two new molds required, and one mold modified for fabrication purposes. Some card relay out, but no great problem in fitting the modifications within the present package.
- c. Weight - No significant effect because space currently filled with dummy modules will be occupied by modified circuits.

- d. Reliability - Defining a successful operation as no loss of data channels, and using discrete components, operational probability for six months is 0.7946. Cross strapping the PCM inputs will increase this reliability. Part failure rate improvement will also add to reliability. Decreasing the part failure rate by a factor of 10 would increase probability to 0.9779 for six months operation. This can be achieved by specifications equivalent to the Minuteman program. System reliability would be improved by consolidation of the "Unit B Activate Command" circuitry, relocating some external wiring of the TME inside the unit would contribute some added reliability.

1.14.2 NRZ and Split Phase Study -

- a. It is feasible to replace the present gated sine wave code with split phase code for Unit A. In respect to economy it is a better alternative than NRZ code originally proposed and capability has been demonstrated by breadboard circuits.
- b. Split phase code circuits can be accommodated in the present TME package with a net reduction of four modules because of elimination of Unit A modulator requirement.
- c. TME power consumption by split phase modifications will increase approximately 250 milliwatts.
- d. It is feasible to transmit the split phase signal using the present Hughes transmitter. It is also feasible to transmit Unit A real time

data in the form of split phase M signal using the Hughes transmitter.

- e. With satisfactory performance of the system over the temperature range and with no supply voltage changes greater than ± 0.5 volts the only apparent fault of the new system is the phase distortion of the playback signal. This distortion results in slightly asymmetrical pulse widths of the reconstructed split phase M signal. Improvement in the phase distortion would require a new record-playback head for the recorder to avoid further complicating the playback amplifier. The ultimate decision in this instance depends primarily upon the compatibility of the distorted signal with the ground station equipment.

1.15 AIRBORNE EQUIPMENT RECOMMENDATIONS. - It is recommended that the

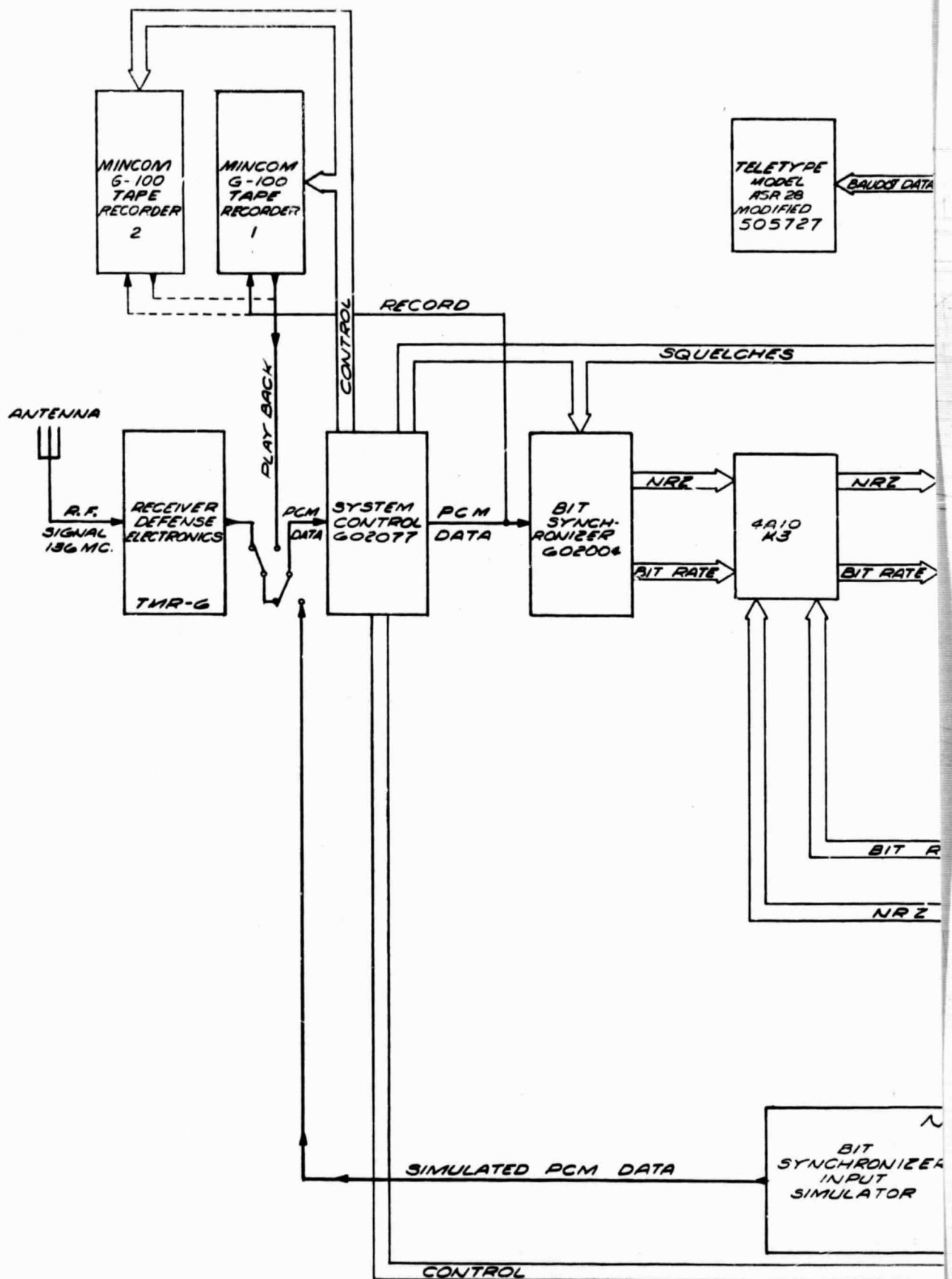
Unit A Multicoder modifications be accepted in total based on minimum cost impact, measured parameters, and test tape evaluation. Further:

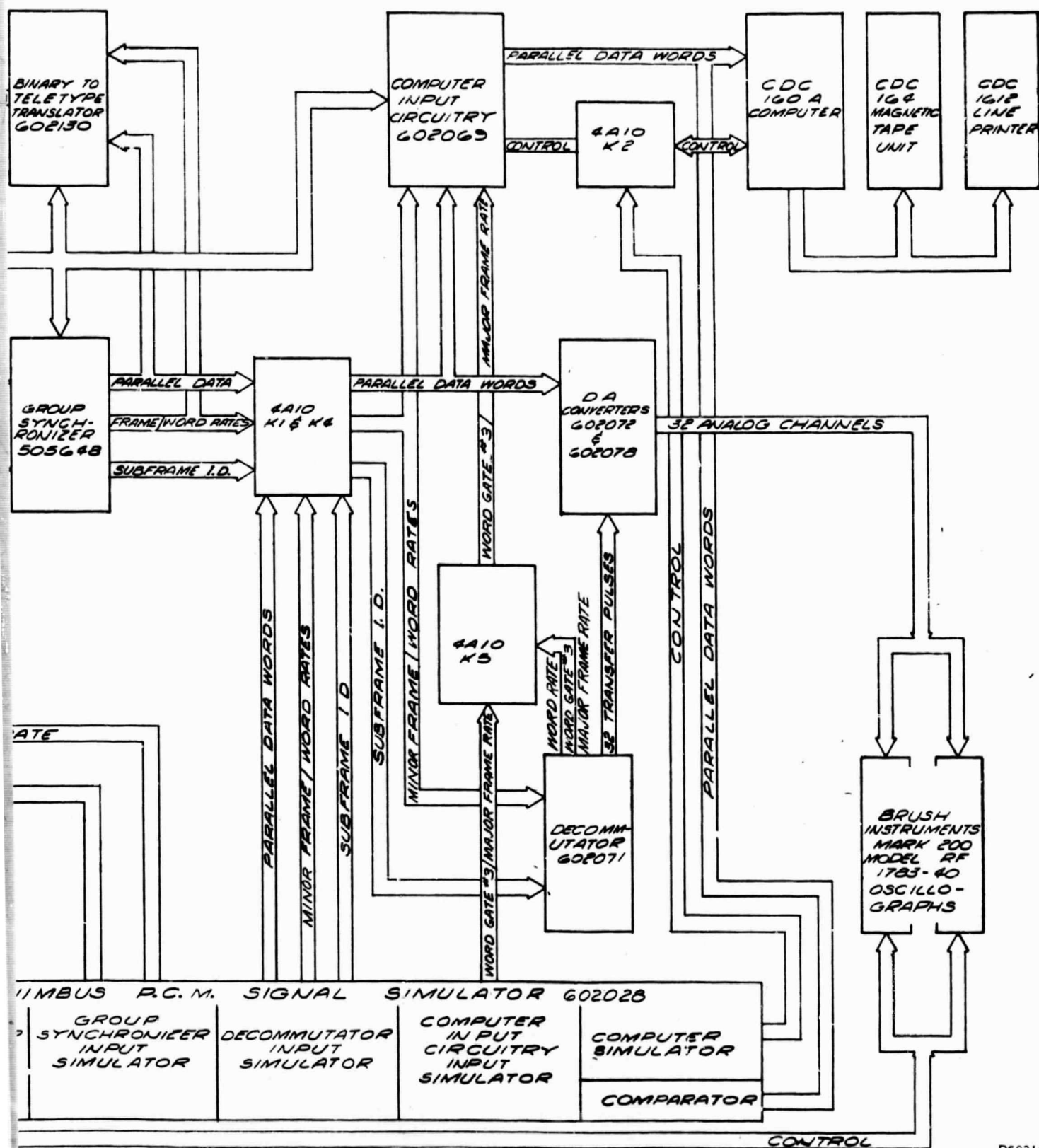
- a. The analog gate transistors should be replaced by PINCH units or the gates be replaced by MOSFET gates and integrated circuit drivers.
- b. Unit A output should utilize a split phase (M) code if the present gated sine wave signal is considered inadequate.
- c. The "Unit B Activate Command" modification circuitry and the minor TME circuit modifications previously described be made.
- d. Unit B output should be covered as an area of study.

Presently this output is a phase modulated 5 Kc sine wave. By using the split phase M code output, as employed by the A unit, it may be possible to improve transmission characteristics as well as effect a saving in circuits in both the airborne and the ground station.

1.16 GROUND EQUIPMENT. - Figure 1 illustrates the NIMBUS PCM Ground Station.

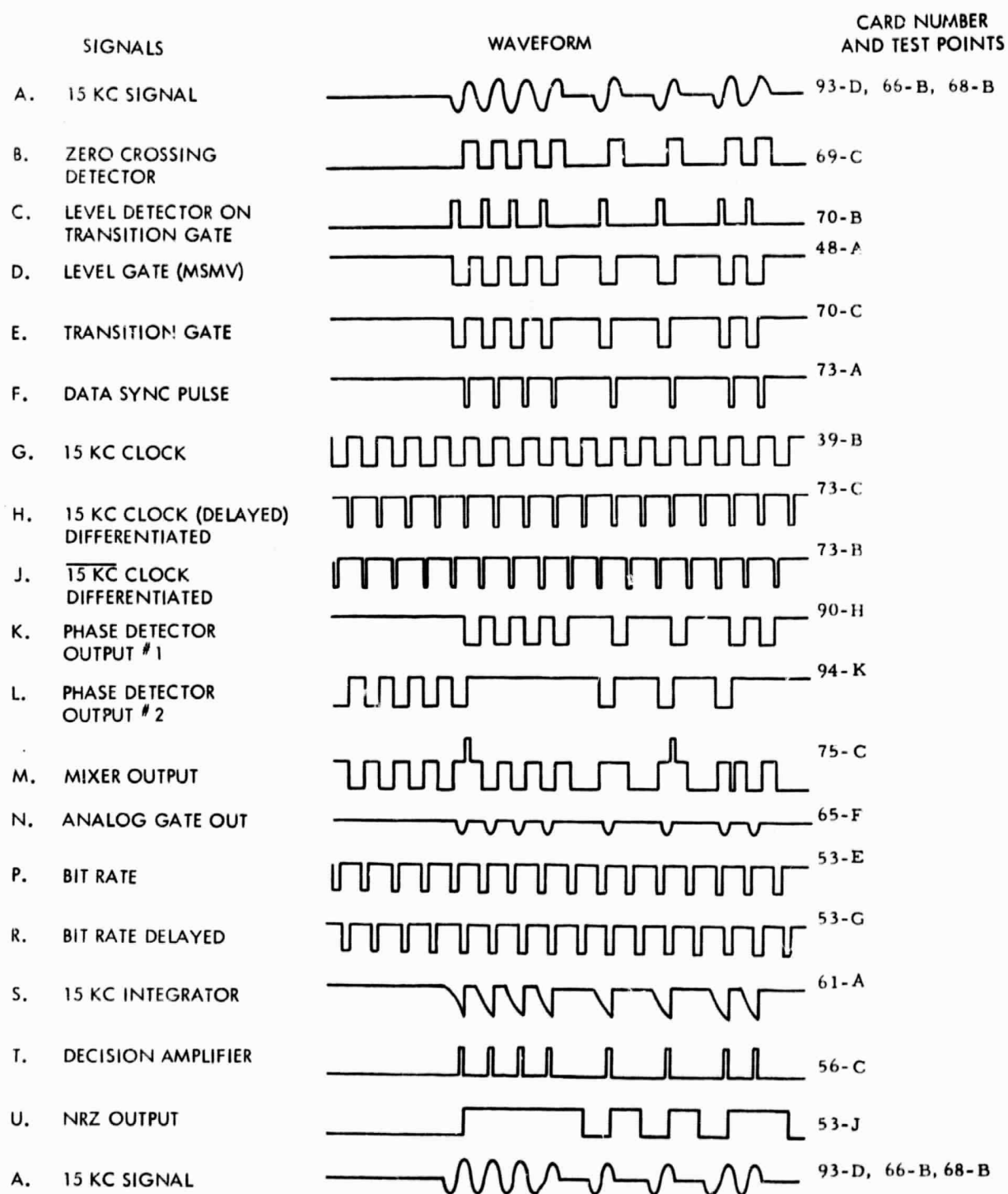
The NIMBUS Instruction Manual (Reference 15, Section 3) should be referred to for detailed theory of operation of the Ground Station. Essentially an RF signal from the airborne telemetry system is received by the Ground Station (figure 65) and routed through the system receiver, or a video signal is received from a remote receiver. Magnetic tape records the video signal for later playback and processing. Real time processing routes the video signal to the System Control Assembly where squelch circuits detect and indicate whether serial data is a real or stored, or B data. The video data is routed to the Bit Synchronizer where the system bit rate timing is synchronized with incoming data and a decision is made on each bit defining it as "1" or "0". The present NIMBUS data output signal is of the gated-sine-wave type with a "0" represented as one complete cycle of a sine wave and a "1" as the absence of a signal for a bit interval (waveform A, figure 66). The output of the Bit Synchronizer is serial NRZ data (waveform U) and synchronized bit rate. This signal is routed to the Group Synchronizer where the data is converted to parallel 7 bit data words and further system timing synchronized with detected frame and word sync, enabling the remainder of the system to decommutate the data and route it through patch panel selection to digital-to-analog converters. The resulting output is then displayed on traces of Brush Analog Recorders. A computer input circuit assembly also provides interface logic for the general purpose computer (supplied with the station) to process the data in accordance with a selected programming. Two separate areas of the study program were of major concern to the Ground Station, processing data in the new format and handling of a split phase modulated signal in place of the gated sine wave type.





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Figure 65. System Block Diagram



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Figure 66. Bit Synchronizer Timing Diagram

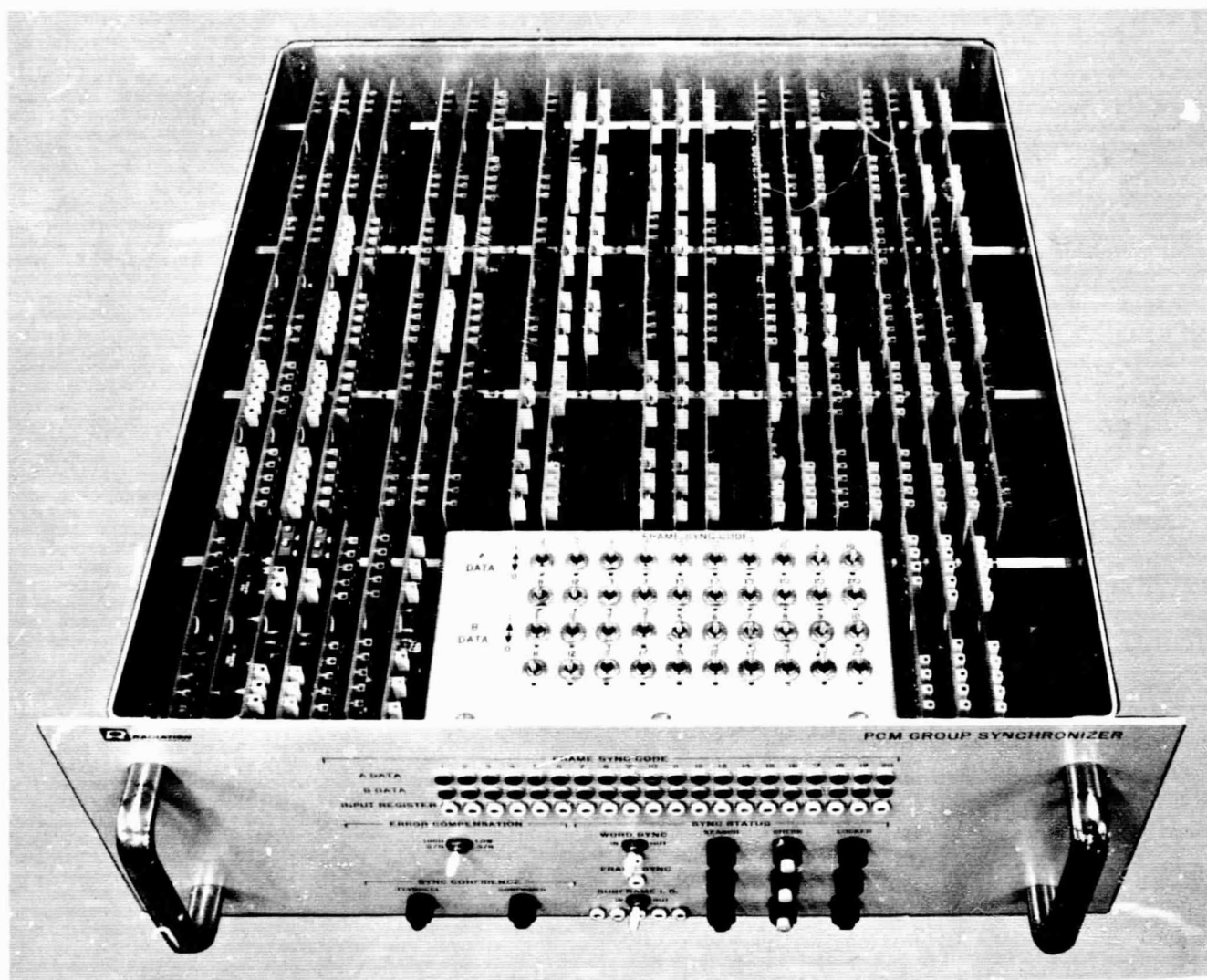
Processing data in the new format required changes to the Group Synchronizer assembly and additional decommutation capability. The use of the split phase modulated signal concerned treatment of the video signal in the Control Assembly and Bit Synchronizer. Thus, the study and subsequent testing concentrated on these areas as separate items.

1.16.1 Areas of Change. - The new format would contain $62\frac{1}{2}$ words per subframe with each word consisting of eight bits including one bit of sync. The information content in respect to the Group Synchronizer was a two word frame sync code, followed by a $\frac{1}{2}$ word (four bits) subframe identification and then 60 normal words. Thus, the counter must be changed for flywheeling and checking at the $62\frac{1}{2}$ word frame length. The frame sync code recognition logic would be seeking correlation on a 4-bit longer and more uniquely coded pattern. There would be no change to the remaining logic except for the different timing relation at the start of a frame, thus fulfilling minimum modification requirement.

1.16.2 Provisions for Feasibility Demonstration. - For testing and the feasibility study demonstration, a signal simulator was breadboarded which provided both types of the video signal and the serial NRZ signal in the new format. Arrangement was also made with airborne equipment study group to supply magnetic tapes. made from its study test set up providing a video signal in the new date format. Both gated sine wave and split phase modulation types tapes would be made. The modification to update an existing NIMBUS Ground Station was being performed at Radiation during the study program period. Schedules were so

arranged that portions of the system would be available for practical performance testing and demonstrating the feasibility of proposed changes.

- 1.16.3 Recommended Decommutation Approach. - As part of the study program, the necessary decommutation for the added digital channels and time code words in the new format was investigated. Methods and detailed logic were proposed. One method studied was the addition of an independent separate Digital decommutator to the system with a minimum of interfaces and system changes. A second approach was to modify and add to existing system required decommutation logic to provide required expansion.
- 1.16.4 Digital Channels and Time Code Recording. - The print-out of the digital channels using an "event" type recorder and similar recording of time code data is proposed. Detailed interface and packaging requirements will be discussed later in this report as part of the proposed digital decommutation output. No demonstration or hardware testing was proposed in this area of recording and display.
- 1.16.5 Split Phase Modulation. - The ability of the Ground Station to handle a split phase modulated subcarrier signal was studied as a separate problem. The problems of the gated sine wave modulation have been discussed in previous portions of this report (paragraph 1.13). The objectives of the ground equipment study in this area were to determine how to modify the Ground Station to accept and process split phase modulated signals and what economically feasible advantages could be expected. Essentially this involved modification



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Figure 67. Group Synchronizer Assembly

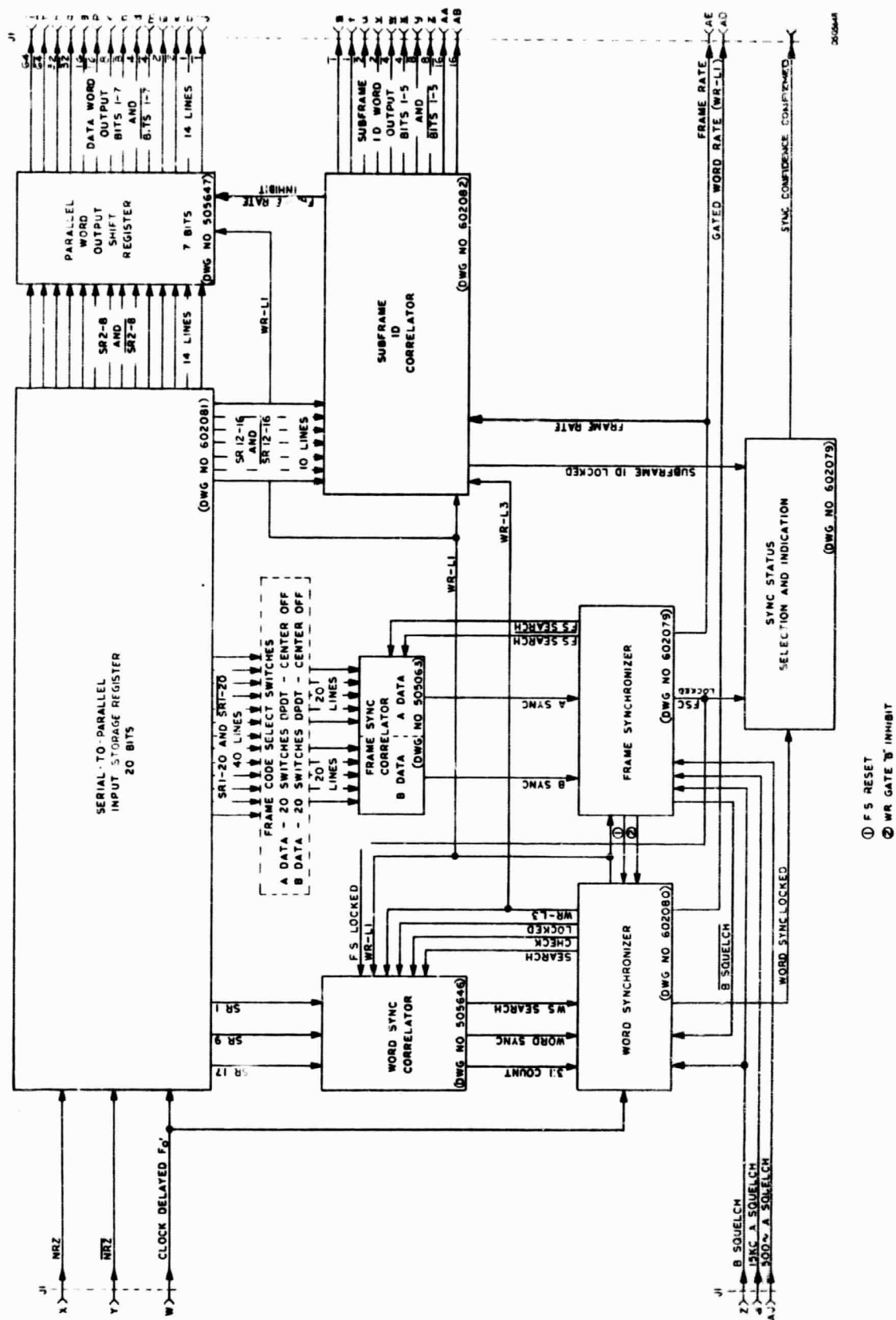


Figure 68 Group Synchronizer (Over-all Block Diagram)

Table 8. Group Synchronizer Input Content at Word Count Intervals

INPUT SHIFT REGISTER		TO SFID INPUT REGISTER																TO OSR								1
		20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2						
EXISTING "A" FORMAT																										
WORD COUNT	0	FRAME RATE AND READ SFID	X	X	X	WR O	S _{FID} I _D	S _{FID} I _D	S _{FID} I _D	S _{FID} I _D	SFID FC O	FC O	FC O	FC O	FC I	FC I	FC I	FC I	FC I	FC I	FC I	FC I	FC I	FC I	FC I	
	1		X	X	X	WR O	X	X	X	X	X	X	WR O	S _{FID} I _D	S _{FID} I _D	S _{FID} I _D	S _{FID} I _D	SFID FC O	FC O	FC O	FC O	FC O	FC O	FC O		
	2		X	X	X	WR O	X	X	X	X	X	X	WR O	X	X	X	X	X	X	X	X	X	X	WR O		
	3		X	X	X	WR O	X	X	X	X	X	X	WR O	X	X	X	X	X	X	X	X	X	X	WR O		
	↓																									
	63		SFID FC O	FC O	FC O	FC O	FC I	FC I	FC I	FC I	FC I	FC I	FC I	X	X	X	X	X	X	X	X	X	X	WR O		
	0		X	X	X	WR O	S _{FID} I _D	S _{FID} I _D	S _{FID} I _D	S _{FID} I _D	SFID FC O	FC O	FC O	FC O	FC I	FC I	FC I	FC I	FC I	FC I	FC I	FC I	FC I	FC I		

INPUT SHIFT REGISTER		TO SFID INPUT REGISTER																TO OSR								1
		20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2						
NEW "A" FORMAT																										
WORD COUNT	0	FRAME RATE AND READ SFID	S _{FID} I _D	S _{FID} I _D	S _{FID} I _D	S _{FID} I _D	SFID FC O	FC I	FC I	FC I	FC I	FC I	FC O	FC I	FC I	FC O	FC I	FC I	FC I	FC I	FC I	FC O	FC I	FC O		
	1		X	X	X	WR O	S _{FID} I _D	S _{FID} I _D	S _{FID} I _D	S _{FID} I _D	SFID FC O	FC I	FC I	FC I	FC I	FC I	FC I	FC I	FC I	FC I	FC O	FC I	FC I			
	2		X	X	X	WR O	X	X	X	X	X	X	WR O	S _{FID} I _D	S _{FID} I _D	S _{FID} I _D	S _{FID} I _D	SFID FC O	FC I	FC I	FC I	FC I	FC I			
	3		X	X	X	WR O	X	X	X	X	X	X	WR O	X	X	X	X	X	X	X	X	X	WR O			
	4		X	X	X	WR O	X	X	X	X	X	X	WR O	X	X	X	X	X	X	X	X	X	WR O			
	↓																									
	62		FC I	FC I	FC O	FC I	FC I	FC O	FC I	FC I	FC I	FC I	FC O	X	X	X	X	X	X	X	X	X	WR O			
	(63) 0		S _{FID} I _D	S _{FID} I _D	S _{FID} I _D	S _{FID} I _D	SFID FC O	FC I	FC I	FC I	FC I	FC I	FC O	FC I	FC I	FC O	FC I	FC I	FC I	FC I	FC O	FC I	FC O			
	1		X	X	X	WR O	S _{FID} I _D	S _{FID} I _D	S _{FID} I _D	S _{FID} I _D	SFID FC O	FC I	FC I	FC I	FC I	FC I	FC O	FC I	FC I	FC O	FC I	FC I	FC I			

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and comparative performance checks on the Bit Synchronizer assembly. It is recognized that the squelch circuits also receive the video signal and may require minor modification for optimum performance with the split-phase signal with the only difference being the frequency sensitive squelch circuit will be seeing a nearly square wave input instead of the present sine-wave. The continuity of waveform in split phase modulation will enhance the performance by eliminating the sensitivity of squelches to data content, i.e.; fixed word of all "1's", on all channels with gated-sine-wave modulation has minimum signal content of one cycle per eight-bit intervals. Split- phase modulation will provide continuous full cycle square waves, reversing phase for "0's". This gives a worst-case condition for all zeros where the signal waveform looks like a $1/2$ bit rate square wave. Much testing and documentation had already been performed on the present NIMBUS Bit Synchronizer and thus a basis for comparison was easily established. Signal-to-noise (S/N) performance using one type of modulation versus the other was the prime measurement for comparative performance indication. Extreme care was taken to use the same test set up and instrumentation with emphasis on comparative results rather than absolute S/N performance measurement techniques. Tests were carefully documented, precision test equipment was used and valid techniques were followed giving results which were close to the expected. The study involved building breadboard logic and modifying an existing NIMBUS Bit Synchronizer for tests and final demonstration. An additional approach was employed taking test data and demonstrating the use of Radiation Incorporated's,

Universal Bit Synchronizer in place of the NIMBUS Bit Synchronizer in the NIMBUS System.

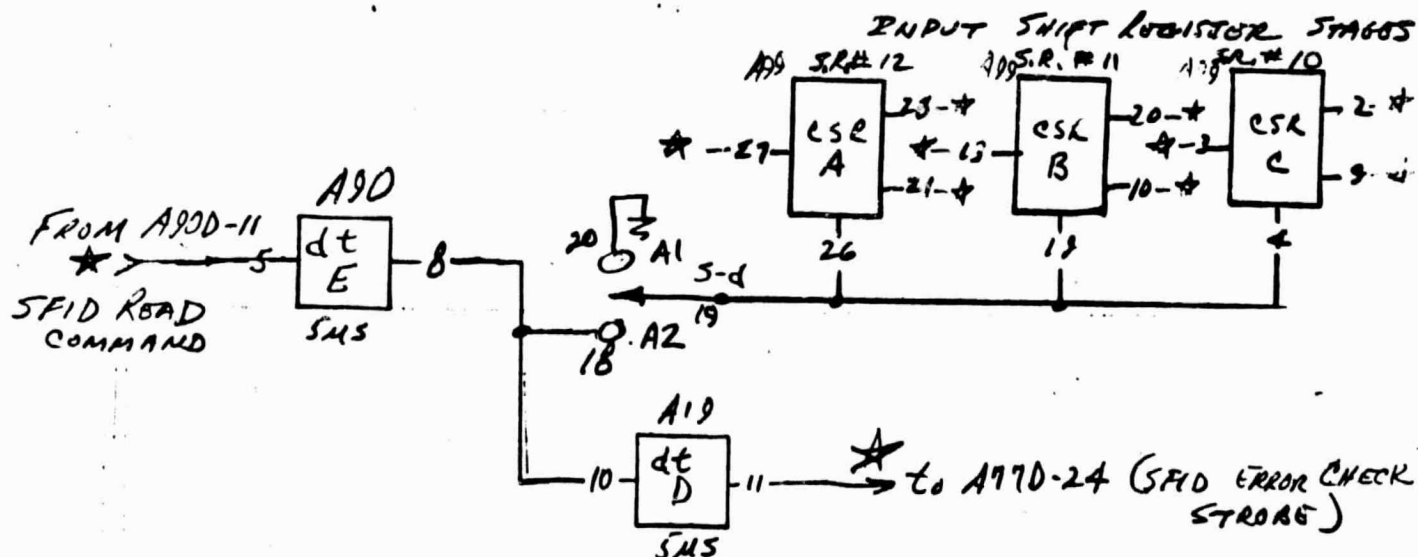
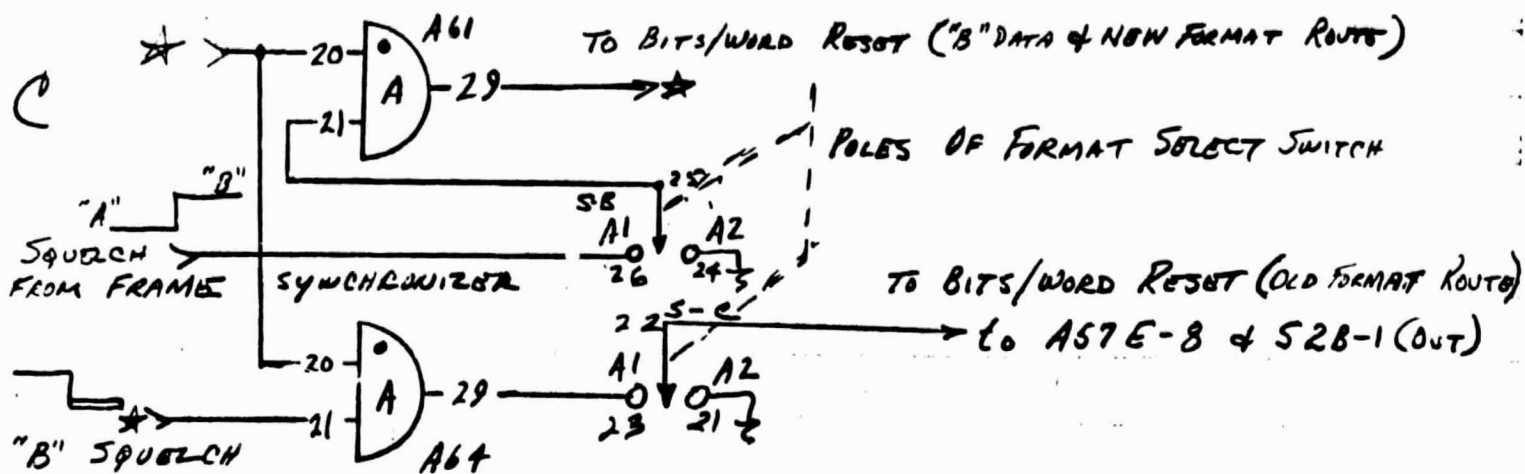
1.17 MODIFICATION OF GROUP SYNCHRONIZER ASSEMBLY. - Figure 67 is a photograph of this assembly. Figure 68 illustrates the Group Synchronizer as a block diagram. The modification of the Group Synchronizer, enabling synchronization with the new format, was accomplished by adding a format select switch (6 PDT) with appropriate wiring and logic changes which permitted operational checks to be made in the existing format and ability to switch to proposed new format for further checks. Details of the changes involved in this study can be followed by noting the sequence of data through the input register of the Group Synchronizer; first in the existing format and then in required sequence for the new format.

1.17.1 Table 8 indicates the differences in the existing and the new format as it appears in the input register and further the progression of data bits (left to right) at various word count intervals. In the existing format, frame sync recognition occurs when the correct pattern (eight "1's" and four "0's" occurs in the register in stages numbered 1 through 12. The word counter is reset to zero by frame sync defining word count zero (0-63 count sequence). Read-out of subframe identification (SFID) is also initiated at this time, reading broadside from the input register stages 12 through 16 (4 bits plus last 0 bit of frame sync code, FC, enabling future expansion to 32 subframe count). Finally, at word count zero time the output shift register (OSR) is set and held at all "0's".

1.17.2 Word count 1 occurs 8 bits later and data has shifted to the right 8 stages. Data in stages 2 through 8 for readout to the OSR is SFID information plus "0" bits of the frame sync code, and can be decommutated as Word 1. After another 8 bits of data has shifted into the register, word count 2 occurs with stages 2 through 8 containing the 7 data bits of Word 2 as a readout to the OSR. The data continues in serially at bit rate as described to a word count of 63, at which time the last data word of that subframe is in stages 2 through 8 and read out to the OSR. The frame sync code pattern is again entering the register, and after another 8 bits it is in correct position for correlation. This occurs at a word count of zero which defines frame rate and SFID read outs as previously described.

1.17.3 Now looking at the new format and following the same sequence of data through the input register, the differences and required logic changes can be seen. When the frame sync code (now 16 bits) is in stages 1 through 6, it will be detected. This requires only a change in the present 16 frame code select switches from the eight "1's", four "0's", four bit switches at center-off position to the selected Barker code. Two poles of the format select switch are used to route the detected frame sync code signal in the present path for existing format, but in new format position to reset the bit counter to a four count (0-7 sequence). See figure 69 (view C) for wiring change required. This in effect sets the word count to 0 plus 1/2 word. This necessitated routing of the frame sync during search signal to OR gate into the frame rate line A30B since frame rate generation depended on the bit counter also being zero (not four bits or 1/2 word ahead). By this means





* Denotes Added Logic Stage
 Denotes Existing Signal Routing

Figure 69. Group Synchronizer Wiring Changes
 (Sheet 2 of 2)

frame rate would now be generated at every word count zero time. The OSR is held at all "0's" at word count zero. However, the SFID cannot be read at this time as was done before, because stages 12 through 16 do not contain SFID data. We need to initiate "SFID Read" after four more bits of data are shifted in the register and this is done since the bit counter was set to a four count at word count zero and will be indexed by bit rate to a zero count after four more bits. The existing SFID Read logic holds the word count zero indication looking for WR-L1 (bits-per-word count zero) to generate the SFID Read command. Thus, four bit intervals after word count zero, stages 12 through 16 contain the SFID data and is read to the SFID register. Also the word counter is indexed to Word 1 count.

- 1.17.4 Next it is necessary to reset a portion of the input register after the frame sync pattern has passed its correlation check in order to reconstruct a full seven bit data word for the SFID four bit word. By routing a delayed SFID Read (figure 69, View D) from A90E through a pole of the format select switch to reset input register stages 10, 11 and 12 to "0" we are now ready at word count 2 to read-out the correct SFID data with the three most significant bits as "0's" and SFID information (0-15 count) in the four least significant bit positions.
- 1.17.5 The OSR needs to be inhibited for both word count zero and word count 1, since word count 2 is the first time valid data is in proper stages for readout. The existing logic accomplishes this since the OSR inhibit is initiated by frame rate and continues until next WRL-3 (bit count 2) occurs. Thus the reset of the

bit counter to 1/2 word ahead by frame rate enables the inhibit signal to last from word count zero (frame rate time) through word count 1 (at next WR-L1 and two more bit intervals (next WR-L3). On the existing format the same logic only inhibits the OSR for word count zero and a word count 1 time correct SFID data is read.

- 1.17.6 An additional timing change that existing logic accomplishes in the same fashion is the gated word rate signal to the rest of the system. On A data operation, WR-L1 is routed out as word rate. The reset of the bit counter 1/2 word ahead deletes one WR-L1. The decommutator counts this word rate relating it to proper words. In the existing format it relates the first word rate received at frame rate as associated with frame synch code, the second received as associated with SFID word and the third one denotes the first data word and so on. Therefore, the new format must send only one word rate for word count zero and word count 1 and the second word rate at word count 2. The present logic will do this since it deletes the word rate (WR-L1) at the word count zero time but not any other word count time by the advanced reset change.
- 1.17.7 After SFID data is read out of the OSR (word count 2 or decommutator Word 1 time) and eight more data bits enter the input register, the first data word of the new format is in position for read out to the OSR. Thus, data sequence and decommutation is the same as per the existing format for the 60 data words after SFID. Data Words are available at same patch panel selection as before.

1.17.8 In the new format the subframe ends after the 60th data word and it is necessary to start the word count over at this time. This was accomplished by making the word counter an asymmetrical counter counting 64 counts with 63 inputs. Feed back was routed from the 32 count stage (figure 69, View B) to add one count. Thus the word counter starts with a zero count through 32 adding one at this time so the 33rd input produces a 34 count and on to a 63 count with 62 inputs and reset to zero (or 64 count) on the 63rd input. This enables the word counter to flywheel and check for frame synch by the same method as with existing format.

1.18 MODIFIED BARKER FRAME SYNC CODE. - (See Ref. 16, 17, and 18 Section 3). In choosing a 16 bit frame sync code for the new format, a Barker code word was considered. An n-bit frame sync pattern should be selected under the criterion that probability of displacement of the pattern by ± 1 bit be minimized, at the same time restricting the probability of pattern displacement by 2 to (n-1) bits below a prescribed maximum. The IRIG Telemetry Standards Document suggests a 11-bit plus complement 11-bit code word and deleting latter bits of the complement for prescribed length of code word. The 11-bit Barker word suggested was 11100010010. However, this was later revised to a 31-bit synchronization pattern under PCM Standards as follows:

0101011010100101101001101010111

Extensive coverage of sync patterns is available in the references. In the NIMBUS format it is evident for maximum uniqueness that the word sync pattern be excluded such that a worst-case data pattern with word sync would still give an Error indication. Also initially a requirement was considered stipulating the first bit of the frame sync

code be a "0" bit to be compatible with the generation of the word sync bit of the 63rd word. The new format deletes the last 12 bits of the 512 bit frame length and adds the remaining first 4 bits (0 word sync plus 3 data bits) of the 63rd word to the frame sync code. By this means a 11-bit Barker word plus the first 5 bits of its complement was modified to exclude the word sync pattern. Plotting of various deviations from this pattern versus error information as pattern appeared slipped to either side of the correct correlated position was done to obtain a satisfactory unique code pattern for the NIMBUS format (table 9). Further work could be done in this area for the NIMBUS format, but the Ground Station possesses the flexibility of selecting switch positions for correlation of any pattern.

1.19 PROCESSING OF DIGITAL CHANNELS AND TIME CODE. - To process the expanded data capability of the new format requires additional decommutation. Eight prime and four subcommutated analog channels of the existing format have been designated to contain 1-bit (on/off functions) digital information channels. The Time Code data is located in six subcommutated channels. Logic design was studied to sort and provide routing to recorder and display for 84 single channels plus the Time Code. One approach was to provide an independent digital decommutator assembly requiring a minimum of inputs from the system and capable of being packaged with its recording and display at the system or remote. A second approach proposed adding another logic drawer to the present system sharing timing and patching that is available.

Table 9A. Deviation Checks from Modified Sync Pattern

FRAME SYNC PATTERN																				Slip Left	Errors					
0	x	x	x	x	0	1	1	1	1	1	0	1	1	0	1	1	1	0	1	0	x	x	x	0	0	
x	x	x	x	x	0	1	1	1	1	1	0	1	1	0	1	1	1	0	1	0	x	x	x	x	1	8
x	x	x	0	1	1	1	1	1	0	1	1	0	1	1	1	0	1	0	x	x	x	x	x	2	6	
x	x	0	1	1	1	1	1	0	1	1	0	1	1	1	0	1	0	x	x	x	x	x	x	3	5	
x	0	1	1	1	1	1	0	1	1	0	1	1	1	0	1	0	x	x	x	x	x	x	x	4	5	
0	1	1	1	1	1	0	1	1	0	1	1	1	0	1	0	x	x	x	x	x	x	x	0	5	7	
1	1	1	1	1	0	1	1	0	1	1	1	0	1	0	x	x	x	x	x	x	x	0	x	6	3	
1	1	1	1	0	1	1	0	1	1	1	0	1	0	x	x	x	x	x	x	x	0	x	x	7	3	
1	1	1	0	1	1	0	1	1	1	0	1	0	x	x	x	x	x	x	x	0	x	x	x	8	5	
1	1	0	1	1	0	1	1	1	0	1	0	x	x	x	x	x	x	x	0	x	x	x	x	9	2	
1	0	1	1	0	1	1	1	0	1	0	x	x	x	x	x	x	x	0	x	x	x	x	x	10	3	
0	1	1	0	1	1	1	0	1	0	x	x	x	x	x	x	x	0	x	x	x	x	x	x	11	4	
1	1	0	1	1	1	0	1	0	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	12	4	
1	0	1	1	1	0	1	0	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	0	13	2	
0	1	1	1	0	1	0	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	0	x	14	2	
1	1	1	0	1	0	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	0	x	x	15	1	
1	1	0	1	0	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	0	x	x	x	16	1	
x	x	x	x	x	x	0	x	x	x	x	x	x	0	x	x	x	x	x	x	x	0	x	x	} WORST CASE CODE PATTERN	1	
x	x	x	x	x	0	x	x	x	x	x	x	0	x	x	x	x	x	x	x	0	x	x	1			
x	x	x	0	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	0	x	x	x	1			
x	x	x	x	x	x	0	x	x	x	x	x	x	0	x	x	x	x	x	x	0	x	x	1			

WORST
CASE
CODE
PATTERN

FRAME SYNC PATTERN																							Slip Right	Errors	
0	x	x	x	x	0	1	1	1	1	1	0	1	1	0	1	1	1	0	1	0	x	x	x	0	0
x	0	x	x	x	x	0	1	1	1	1	1	0	1	1	0	1	1	1	0	1	0	x	x	1	8
x	x	0	x	x	x	x	0	1	1	1	1	1	0	1	1	0	1	1	1	0	1	0	x	2	6
x	x	x	0	x	x	x	x	0	1	1	1	1	1	0	1	1	0	1	1	1	0	1	0	3	5
x	x	x	x	0	x	x	x	x	0	1	1	1	1	1	0	1	1	0	1	1	1	0	1	4	5
x	x	x	x	x	0	x	x	x	x	0	1	1	1	1	1	0	1	1	0	1	1	1	0	5	7
x	x	x	x	x	x	0	x	x	x	x	0	1	1	1	1	1	0	1	1	0	1	1	1	6	4
x	x	x	x	x	x	x	0	x	x	x	x	0	1	1	1	1	1	0	1	1	0	1	1	7	4
0	x	x	x	x	x	x	x	0	x	x	x	x	0	1	1	1	1	1	0	1	1	0	1	8	6
x	0	x	x	x	x	x	x	x	0	x	x	x	x	0	1	1	1	1	1	0	1	1	0	9	2
x	x	0	x	x	x	x	x	x	x	0	x	x	x	x	0	1	1	1	1	1	0	1	1	10	4
x	x	x	0	x	x	x	x	x	x	x	0	x	x	x	x	0	1	1	1	1	1	0	1	11	3
x	x	x	x	0	x	x	x	x	x	x	x	0	x	x	x	x	0	1	1	1	1	1	0	12	4
x	x	x	x	x	0	x	x	x	x	x	x	x	0	x	x	x	x	0	1	1	1	1	1	13	2
x	x	x	x	x	x	0	x	x	x	x	x	x	x	0	x	x	x	x	0	1	1	1	1	14	3
x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	0	x	x	x	x	0	1	1	1	15	2
0	x	x	x	x	x	x	x	0	x	x	x	x	x	x	0	x	x	x	x	0	x	x	x	16	2

Error Check For 0101110110111110 Frame Sync Pattern

- NIMBUS PCM GROUND STATION
- "A" FORMAT MODIFICATION
- SUBFRAME LENGTH
- 62-1/2, 8-BIT WORDS
- 01111011011010 → DIRECTION ENTRY TO INPUT SHIFT REGISTER
- FRAME SYNC CODE
- 1/2 WORD (4 BITS), WORD NO 2-1/2
- SUBFRAME ID
- 60 - 8-BIT WORDS: WORDS NO 3-1/2 THROUGH NO 62-1/2; 0 WORD SYNC PLUS 7 DATA BITS
- DATA

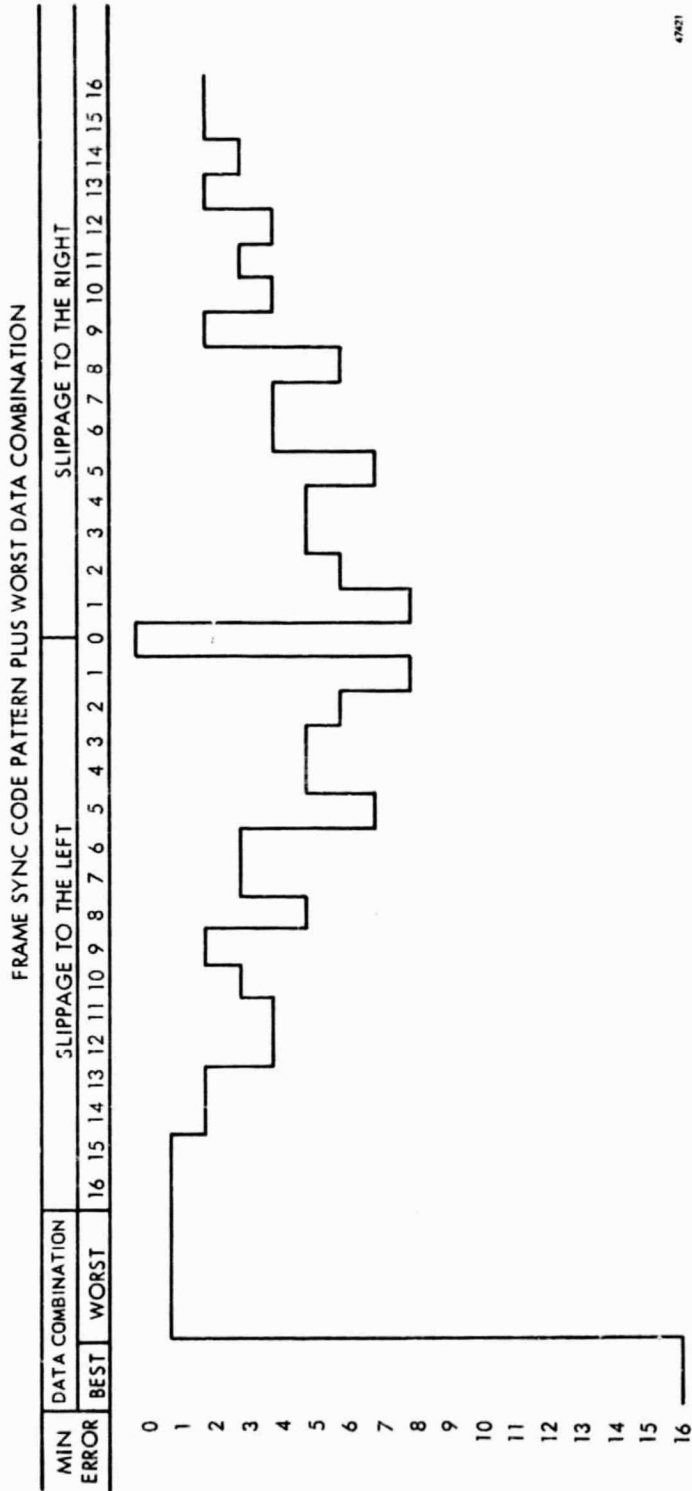


Figure 69A. Frame Sync Pattern Slippage Error Chart for Table 9A

NIMBUS PCM GROUND STATION - "A" FORMAT MODIFICATION
 MINOR FRAME LENGTH - 62 1/2, 8-BIT WORDS
 FRAME SYNC CODE - 01111101101000110 → DIRECTION OF ENTRY TO INPUT SHIFT REGISTER

PATTERN SLIPPAGE Vs ERROR INDICATION

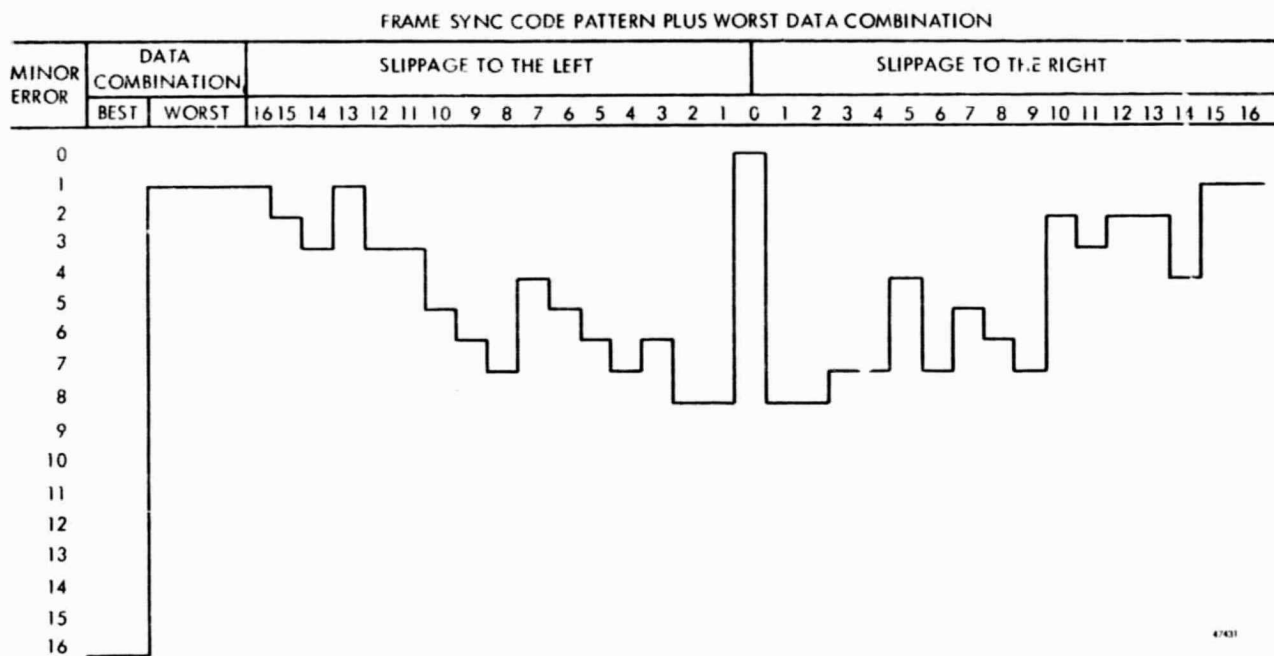


Figure 69B. Frame Sync Pattern Slippage Error Chart for Table 9B

Table 9B. Deviation Checks from Modified Sync Pattern

FRAME SYNC PATTERN																							
x	0	x	x	x	1	1	1	1	0	1	1	0	1	0	0	0	1	1	0	x	x	x	
0	x	x	x	1	1	1	1	0	1	1	0	1	0	0	0	1	1	0	x	x	x	x	
x	x	x	1	1	1	1	0	1	1	0	1	0	0	0	1	1	0	x	x	x	x	x	
x	x	1	1	1	1	0	1	1	0	1	0	0	0	1	1	0	x	x	x	x	x	x	
x	1	1	1	1	0	1	1	0	1	0	0	0	1	1	0	x	x	x	x	x	x	x	
1	1	1	1	0	1	1	0	1	0	0	0	1	1	0	x	x	x	x	x	x	0	x	
1	1	1	0	1	1	0	1	0	0	0	1	1	0	x	x	x	x	x	x	0	x	x	
1	1	0	1	1	0	1	0	0	0	1	1	0	x	x	x	x	x	x	0	x	x	x	
1	0	1	1	0	1	0	0	0	1	1	0	x	x	x	x	x	x	0	x	x	x	x	
0	1	1	0	1	0	0	0	1	1	0	x	x	x	x	x	x	0	x	x	x	x	x	
1	1	0	1	0	0	0	1	1	0	x	x	x	x	x	x	0	x	x	x	x	x	x	
1	0	1	0	0	0	1	1	0	x	x	x	x	x	x	0	x	x	x	x	x	x	x	
0	1	0	0	0	1	1	0	x	x	x	x	x	x	0	x	x	x	x	x	x	0	x	
1	0	0	0	1	1	0	x	x	x	x	x	x	0	x	x	x	x	x	x	0	x	x	
0	0	0	1	1	0	x	x	x	x	x	x	0	x	x	x	x	x	x	0	x	x	x	
0	0	1	1	0	x	x	x	x	x	x	0	x	x	x	x	x	x	0	x	x	x	x	
0	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	0	x	x	x	x	x	x	
x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	
x	x	x	x	x	x	0	x	x	x	x	x	x	x	0	x	x	x	x	x	0	x	x	
x	x	x	x	x	0	x	x	x	x	x	x	0	x	x	x	x	x	0	x	x	x	x	
x	x	0	x	x	x	x	x	x	0	x	x	x	x	x	x	0	x	x	x	x	x	x	
x	x	x	x	0	x	x	x	x	x	0	x	x	x	x	x	x	0	x	x	x	x	x	

Slip Left	Errors
-----------	--------

0	0
1	8
2	8
3	6
4	7
5	6
6	5
7	4
8	7
9	6
10	5
11	3
12	3
13	1
14	3
15	2
16	1

WORST
CASE
CODE
PATTERN

1
1
1
1
1

FRAME SYNC PATTERN																							
0	x	x	x	x	0	1	1	1	0	1	1	0	1	0	0	0	1	1	0	x	x	x	
x	0	x	x	x	x	0	1	1	1	0	1	1	0	1	0	0	0	1	1	0	x	x	
x	x	0	x	x	x	x	0	1	1	1	0	1	1	0	1	0	0	0	1	1	0	x	
x	x	x	0	x	x	x	x	0	1	1	1	0	1	1	0	1	0	0	0	1	1	0	
x	x	x	x	0	x	x	x	x	0	1	1	1	0	1	1	0	1	0	0	0	1	1	
x	x	x	x	x	0	x	x	x	x	0	1	1	1	0	1	1	0	1	0	0	0	1	
x	x	x	x	x	x	0	x	x	x	x	0	1	1	1	0	1	1	0	1	0	0	0	
x	x	x	x	x	x	x	0	x	x	x	x	0	1	1	1	0	1	1	0	1	0	0	
0	x	x	x	x	x	x	x	0	x	x	x	x	0	1	1	1	0	1	1	0	1	0	
x	0	x	x	x	x	x	x	0	x	x	x	x	0	1	1	1	0	1	1	0	1	0	
x	x	0	x	x	x	x	x	x	0	x	x	x	x	0	1	1	1	0	1	1	0	1	
x	x	x	0	x	x	x	x	x	x	0	x	x	x	x	0	1	1	1	0	1	1	1	
x	x	x	x	0	x	x	x	x	x	x	0	x	x	x	x	0	1	1	1	0	1	1	
x	x	x	x	x	0	x	x	x	x	x	x	0	x	x	x	x	0	1	1	1	1	0	
x	x	x	x	x	x	0	x	x	x	x	x	x	0	x	x	x	x	0	1	1	1	1	
0	x	x	x	x	x	x	0	x	x	x	x	x	0	x	x	x	x	0	1	1	1	1	

Slip Right	Errors
------------	--------

0	0
1	8
2	8
3	7
4	7
5	4
6	7
7	5
8	6
9	7
10	2
11	3
12	2
13	2
14	4
15	1
16	1

Error Check For 0110001011011111 Frame Sync Pattern

Table 9C. Deviation Checks from Modified Sync Pattern

FRAME SYNC PATTERN																								
0	x	x	x	x	1	0	1	1	0	1	0	1	0	1	1	0	1	0	1	0	x	x	x	
x	x	x	x	1	0	1	1	0	1	0	1	0	1	1	0	1	0	1	0	x	x	x	x	
x	x	x	1	0	1	1	0	1	0	1	0	1	1	0	1	0	1	0	x	x	x	x	x	
x	x	1	0	1	1	0	1	0	1	0	1	1	0	1	0	1	0	x	x	x	x	x	x	
x	1	0	1	1	0	1	0	1	0	1	1	0	1	0	1	0	x	x	x	x	x	x	x	
1	0	1	1	0	1	0	1	0	1	1	0	1	0	1	0	x	x	x	x	x	x	x	0	
0	1	1	0	1	0	1	0	1	1	0	1	0	1	0	x	x	x	x	x	x	x	0	x	
1	1	0	1	0	1	0	1	1	0	1	0	1	0	x	x	x	x	x	x	x	0	x	x	
1	0	1	0	1	0	1	1	0	1	0	1	0	x	x	x	x	x	x	x	0	x	x	x	
0	1	0	1	0	1	1	0	1	0	1	0	x	x	x	x	x	x	x	0	x	x	x	x	
1	0	1	0	1	1	0	1	0	1	0	x	x	x	x	x	x	x	0	x	x	x	x	x	
0	1	0	1	1	0	1	0	1	0	x	x	x	x	x	x	x	0	x	x	x	x	x	x	
1	0	1	1	0	1	0	1	0	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	
0	1	1	0	1	0	1	0	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	0	
1	1	0	1	0	1	0	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	0	x	
1	0	1	0	1	0	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	0	x	x	
0	1	0	1	0	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	0	x	x	x	
x	x	0	x	x	x	x	x	x	x	0	x	x	x	x	x	x	0	x	x	x	x	x	x	
x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	
x	x	x	x	0	x	x	x	x	x	x	0	x	x	x	x	x	x	0	x	x	x	x	x	
x	0	x	x	x	x	x	x	x	0	x	x	x	x	x	x	0	x	x	x	x	x	x	x	
x	x	x	x	x	0	x	x	x	x	x	x	0	x	x	x	x	x	x	0	x	x	x	x	

Slip Left	Errors
0	0
1	13
2	4
3	7
4	7
5	3
6	9
7	0
8	7
9	3
10	3
11	4
12	1
13	4
14	1
15	1
16	1
	1
	1
	1
	1
	1
	1

WORST
CASE
DATA
PATTERN

FRAME SYNC PATTERN																								
0	x	x	x	x	1	0	1	1	0	1	0	1	0	1	1	0	1	0	1	0	x	x	x	
x	0	x	x	x	x	1	0	1	1	0	1	0	1	0	1	1	0	1	0	x	x			
x	x	0	x	x	x	x	1	0	1	1	0	1	0	1	0	1	1	0	1	0	x			
x	x	x	0	x	x	x	x	1	0	1	1	0	1	0	1	0	1	1	0	1	0			
x	x	x	x	0	x	x	x	x	1	0	1	1	0	1	0	1	0	1	1	0	1			
x	x	x	x	x	0	x	x	x	x	1	0	1	1	0	1	0	1	0	1	1	0			
x	x	x	x	x	x	0	x	x	x	x	1	0	1	1	0	1	0	1	0	1	1			
0	x	x	x	x	x	x	0	x	x	x	x	1	0	1	1	0	1	0	1	0	1			
x	0	x	x	x	x	x	x	0	x	x	x	x	1	0	1	1	0	1	0	1	0			
x	x	0	x	x	x	x	x	x	0	x	x	x	x	1	0	1	1	0	1	0	1			
x	x	x	0	x	x	x	x	x	x	0	x	x	x	x	1	0	1	1	0	1	0			
x	x	x	x	0	x	x	x	x	x	x	0	x	x	x	x	1	0	1	1	0	1			
x	x	x	x	x	0	x	x	x	x	x	x	0	x	x	x	x	1	0	1	1	0			
x	x	x	x	x	x	0	x	x	x	x	x	x	0	x	x	x	x	1	0	1	1			
0	x	x	x	x	x	x	0	x	x	x	x	x	x	0	x	x	x	x	1	0	1			

Slip Right	Errors
0	0
1	13
2	4
3	7
4	7
5	3
6	9
7	1
8	8
9	2
10	4
11	3
12	2
13	4
14	1
15	3
16	1

Error Check For 0101011010101101 Frame Sync Pattern

1.19.1 Independent Decommutation. - The independent Digital Decommutator assembly would require the following inputs from the system; word rate, major frame rate, subframe rate and the 7 bit broadside data. Sync Confirmed and B-Squelch are used also to prevent non-valid operation. There are 84 single channel outputs for the digital data routed through recorder input connector for 84 separate traces. The Time Code would be available on a single output for serial trace or 21 bit broadside output for a "Nixie" or similar display. A fixed-multi-styli, electrosensitive writing recorder with 150 channel capacity and paper speeds compatible with the present systems analog recorders would adequately handle the digital and Time Code outputs. Channel arrangements would be hard-wired for simplicity and interchangeable in groups of 10 by changing input cable connectors to the recorder or by re-arranging individual channels at a wiring terminal strip. (The Block Diagram is shown in figure 70).

1.19.1.1 The logic of the Digital Decommutator contains its own timing. A 6-stage word and four stage subframe counter driving matrix gates provide decommutation timing, AND gated with the 7-bit parallel data to set proper "0" or "1" data in an output register per each channel. The Time Code data is handled the same to sort out six subcommutated 7-bit channels for a 21-bit broadside input to a storage and serializing (shift) register. The output registers have drivers to route data to inputs to the recorder or other display.

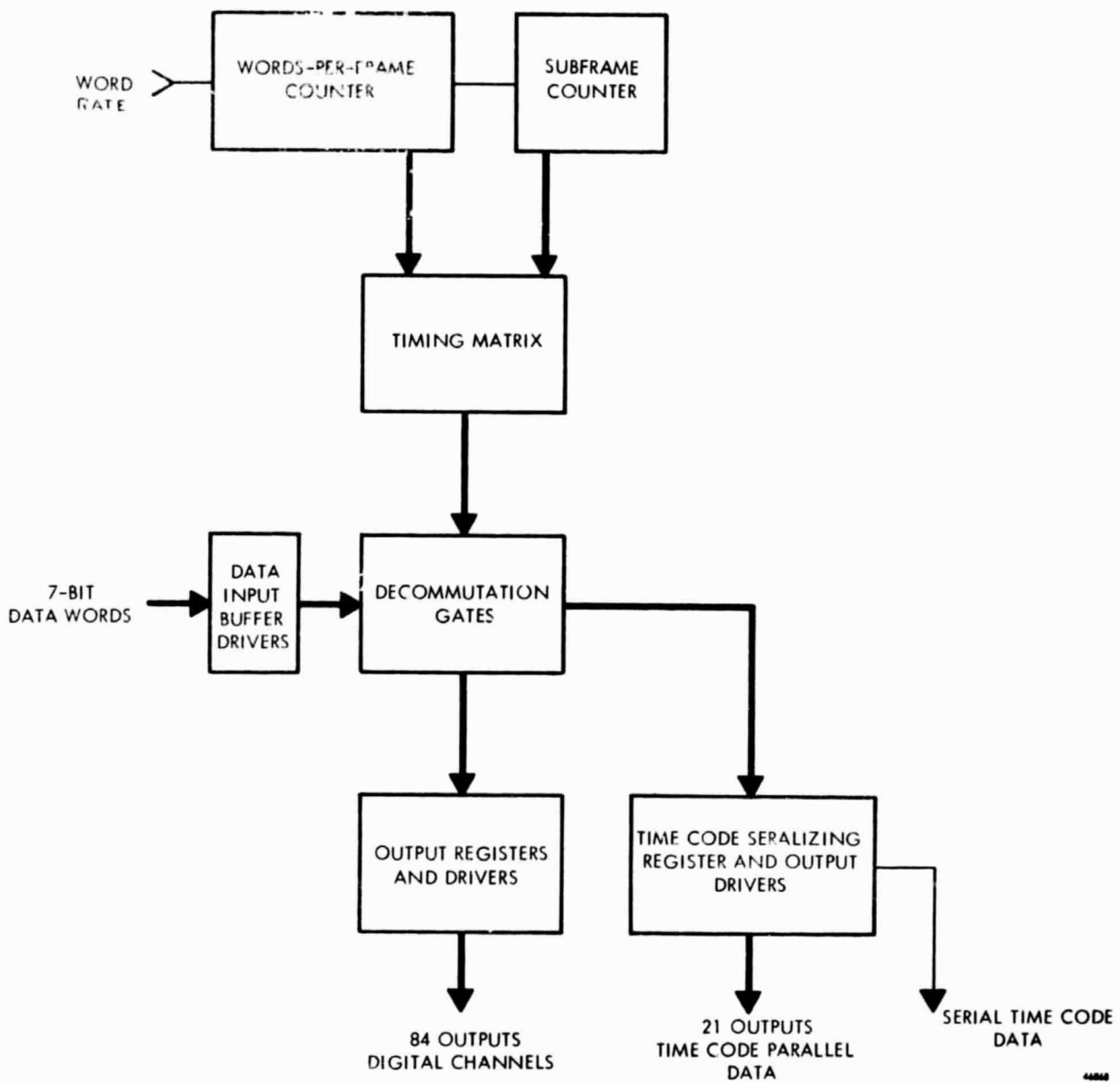


Figure 70. Independent Digital Decommulator Block Diagram

1.19.1.2 The Time Code serializing requires additional logic. Figure 71 shows details of the proposed approach. The time code data words are sorted and routed to proper stages of the output serializing register. Thirty-four stages will provide for data and spacing. The first stage contains a fixed "0" input so that the register clears itself as the data is shifted out serially. The units and tens information of seconds, minutes and hours are routed to the stages indicated leaving "0's" in non-addressed stages. An internal clock with start, stop and rate control is used to drive the shift register for proper serial readout rate. The register is loaded during subframe 1. The beginning of frame 2 starts the internal clock wherein the rate has been set compatible with recorder paper speed. The beginning of frame 1 stops the clock so new data can be read-in. System timing or timing from the word and frame counters of the Digital Decommutator could be used in place of, or in conjunction with the internal clock by switch selection. Time Code readout period is limited to a 15 subframe time interval. A Time Code reference trace would improve visual read of Time Code data trace. Ideally the spacing between units and tens, and seconds, minutes and hours should be clearly defined. A trace of the Time Code serial shift rate would provide some advantage with minimum effort. A more beneficial reference trace would require another serial shift register to

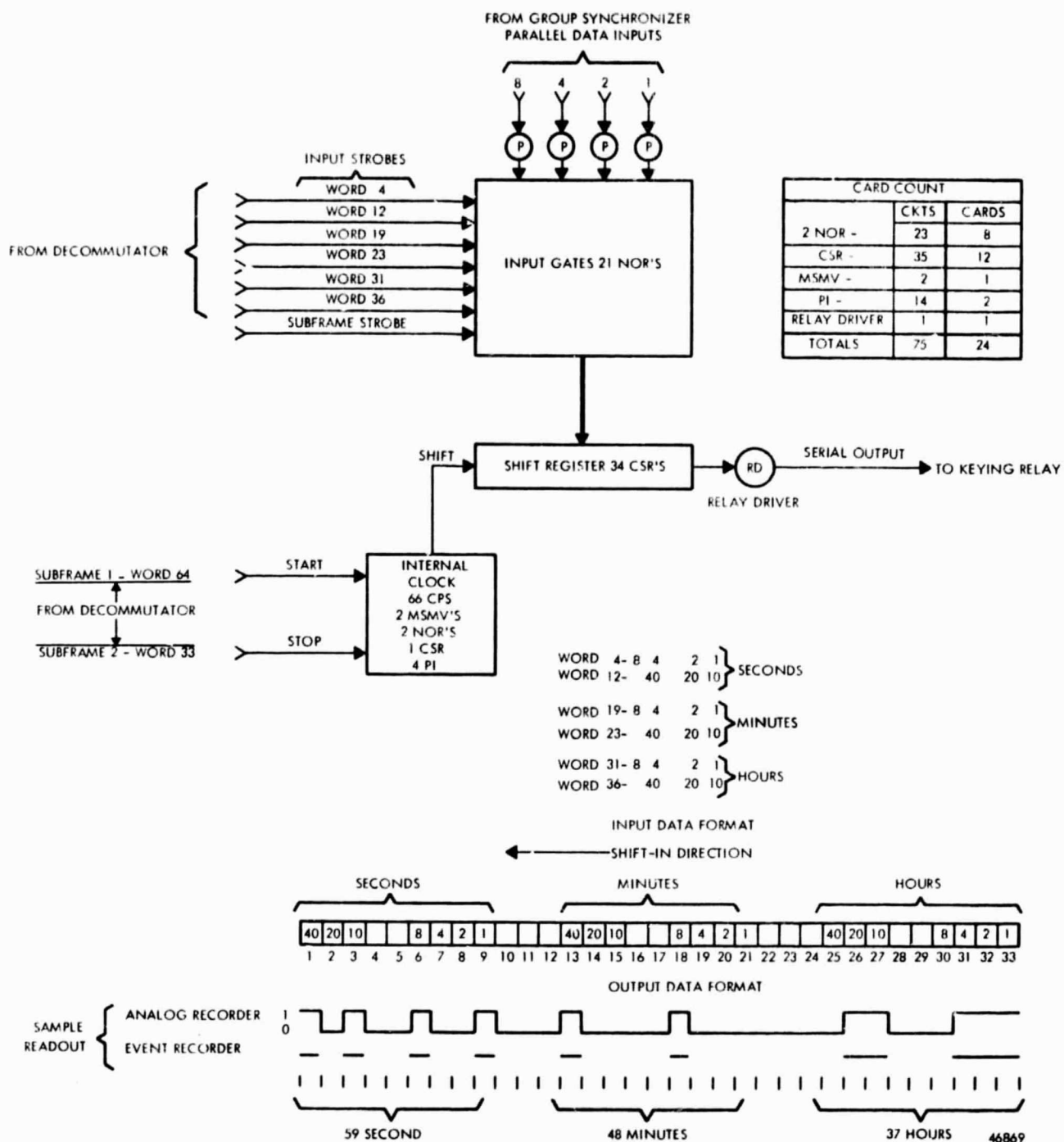


Figure 71. Time Code Display System Logic Diagram

store and shift out spacing information.

1.19.1.3 The packaging of the independent Digital Decommutator would require a separate cabinet to house the event recorder, a Time Code Nixie display panel and a logic drawer for the decommutation and drive logic. A separate logic power supply could be housed in this cabinet or power supplied from the existing system. Minimum panel space requirements would be approximately 24 inches.

1.19.2 Decommutator Logic Added to Prevent System. - Later in the study program more importance was attached to making the Digital Decommutator a part of the existing system; especially endeavoring to use the patch panel spares capability of the existing Decommutator assembly. This would provide a method of arranging digital channels to be displayed on a particular recorder trace by front panel patch selection. A Digital Channels Decommutator drawer to be added to the existing system is thereby proposed as per the following detailed description.

1.19.2.1 The Digital Channels Decommutator drawer will contain four units: the Time Code Decommutator/Serializer Unit, the Prime Channel Digital Decommutator Unit, the Subcom Channel Digital Decommutator Unit, and the Time Code Data Locator. This proposed new drawer will contain 64 standard circuit cards and derive all its inputs from the existing Group Synchronizer and

Decommutator without modification to either except for wiring to to the desired signals and wiring up an additional 32 hole section of the existing Decommutator patch panel. The Digital Channels Decommutator drawer will supply 86 outputs to drive the proposed 150 channel event recorder. The 86 outputs include 56 prime channel on-off functions, 28 subcom channel on-off functions, Time Code in serial form, and Time Code locator (reference) marks. The Time Code may be applied to any or all of three events marker channels by patching on the Decom patch panel. The Time Code locator marks may be placed on any or all of three adjacent event marker channels. The on-off functions are in groups of seven per their assignments in their respective telemetry words and any of the twelve groups may be connected to any of twelve groups of seven event markers. This allows switching of a group of functions to another event marker area in case of failure of an event marker that was being used for a critical function. The new drawer may be located in the cabinet with the new event recorder or in Cabinet 3 where the telemetry receiver was previously located. If the drawer is located in Cabinet 3, cabling will be required to carry 90 wires to drive 90 event markers. If the drawer is located in the event recorder cabinet, cabling will be required to carry 50 wires,

most of which are signals from the system. In that case, five power inverter cards will need to be added in the system to drive the signals on the cable to the event recorder cabinet.

- 1.19.2.2 The Prime Channel Digital Decommulator unit (figure 72) has as inputs the seven pairs of normal and inverted bit lines from the Group Synchronizer and eight transfer pulse lines from the Decom patch panel. The transfer pulse lines carry word gate pulses for word gates 5, 13, 21, 29, 37, 45, 53, and 61. On the patch panel any of these word gates may be selected for any of the eight groups of seven staticizing registers. The eight words listed above are those which carry the 56 prime channel on-off functions. For example, the case where word gate 5 is connected to the trigger inputs of the first group of register stages. When Word 5 time occurs, the data which is present (Word 5) at the steering inputs of those register stages (and all others) from the Group Synchronizer is shifted into the first register group. The data is held by the register group, and its outputs to the respective event markers hold until word gate 5 occurs again to repeat the process. Thus, we load the eight prime channel digital words as they are available into staticizing registers where they are separated into 56 individual bits (on-off functions) and sent to event recorder channels.

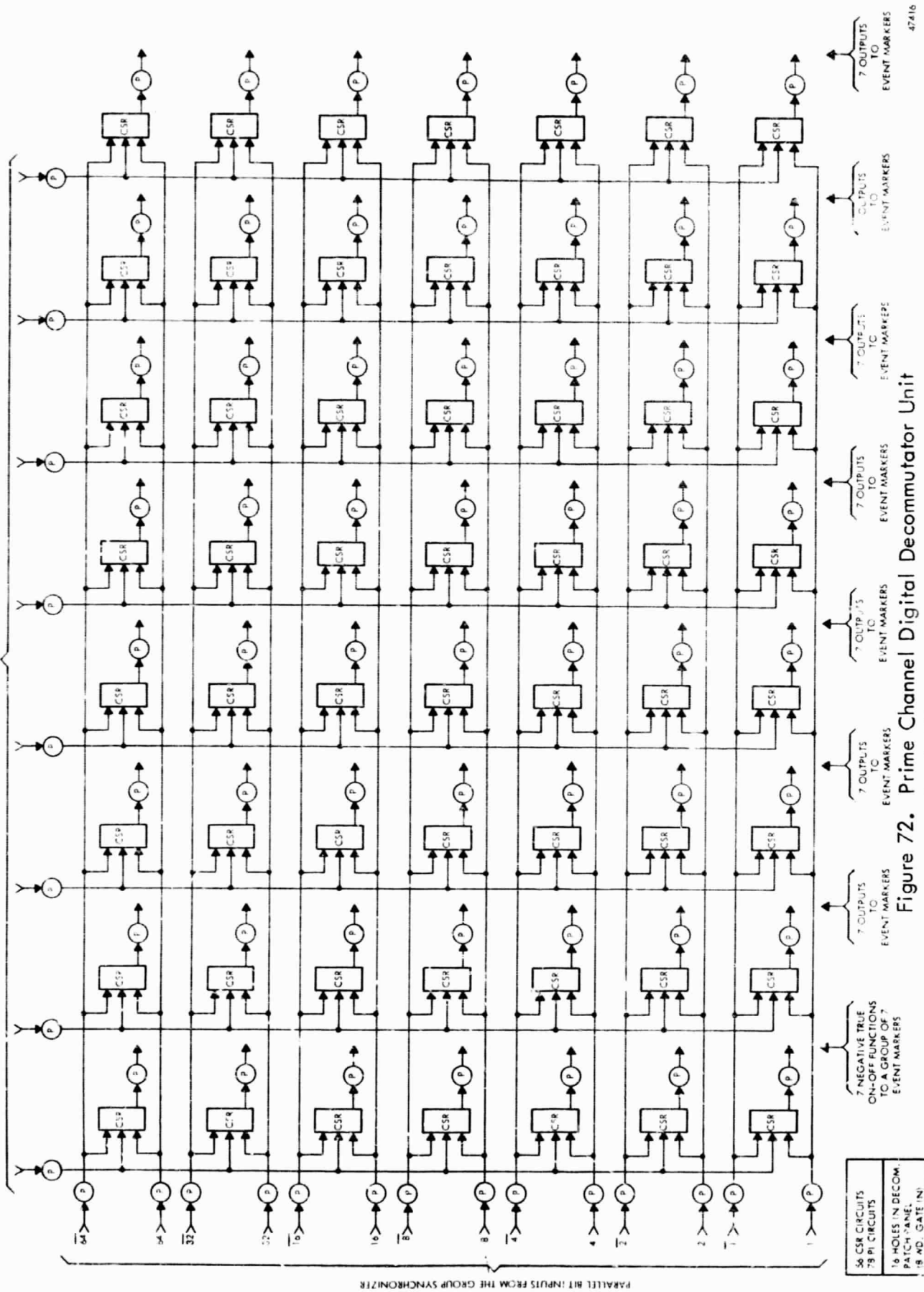


Figure 72. Prime Channel Digital Decommutator Unit Logic Diagram

1.19.2.3 The Subcom Channel Digital Decommulator unit (figure 73)

operates quite similarly to the Prime Channel Decommulator.

In the subcom unit, since there are only four words to decommutate (4, 12, 19, 23), there are only 28 outputs to event markers. As in the prime unit, the seven pairs of normal and inverted bit lines from the Group Synchronizer are connected to the steering inputs of the staticizing registers to be shifted in when transfer pulses occur. The basic difference in the subcom unit is that the transfer pulses, which are word gates patched in at the Decom Patch Panel, are not allowed to shift the registers except during subframe 2. Therefore, the registers are only updated once per major frame by the subcom digital data, whereas the prime unit registers are updated 16 times per major frame by the prime digital data.

1.19.2.4 The Time Code Decommulator/Serializer unit (figure 74) consists of a parallel-to-serial converter with decommutation gates to load it. The Time Code data appears in subframe 1 with units of seconds in Word 4, tens of seconds in Word 12, units of minutes in Word 19, tens of minutes in Word 23, units of hours in Word 31, and tens of hours in Word 36. The decommutation gates that load the shift register are enabled only during subframe 1 and each group responsible for loading the various bits of time infor-

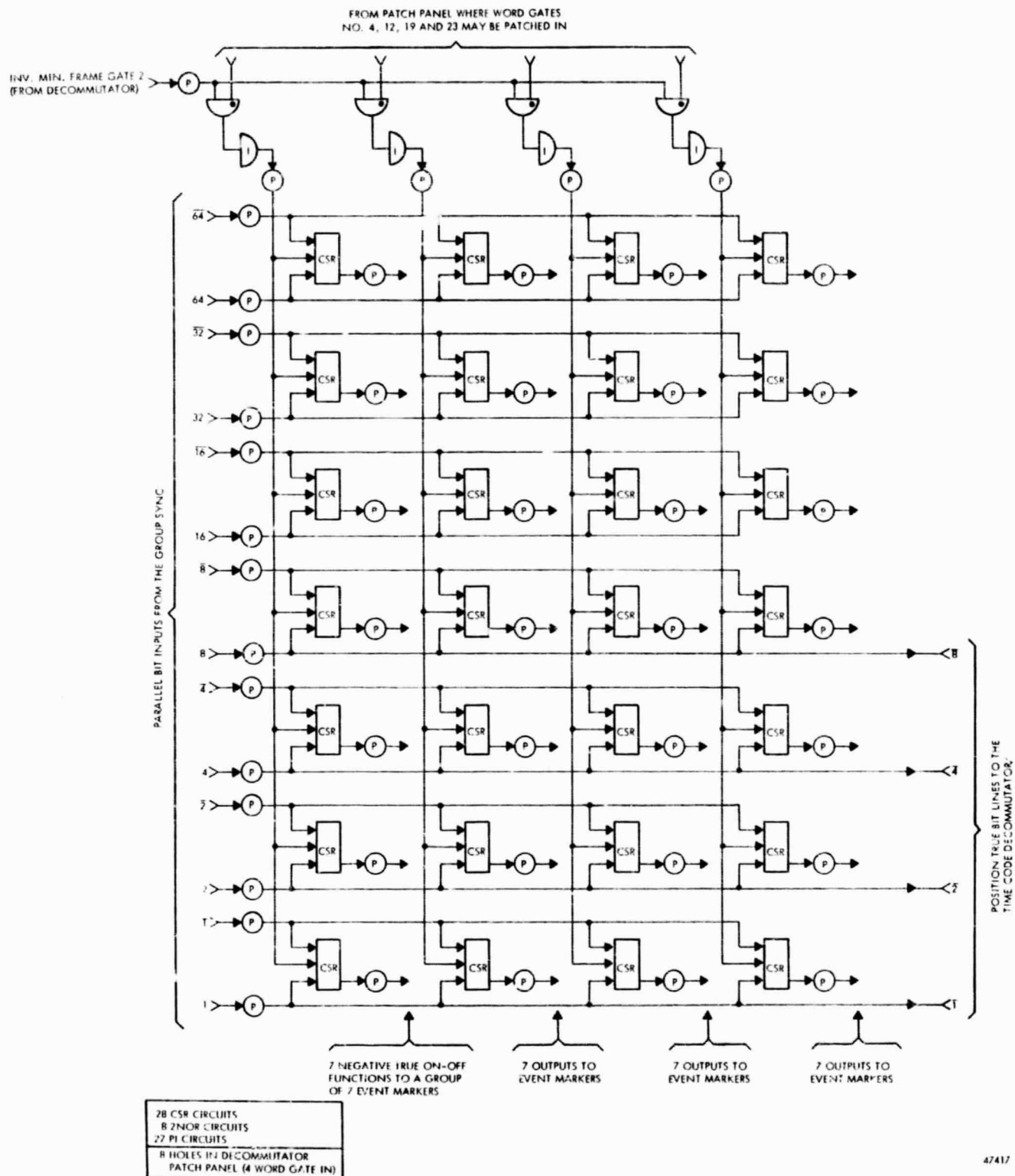


Figure 73. Subcommutated Channel Digital Decommulator
Unit Logic Diagram

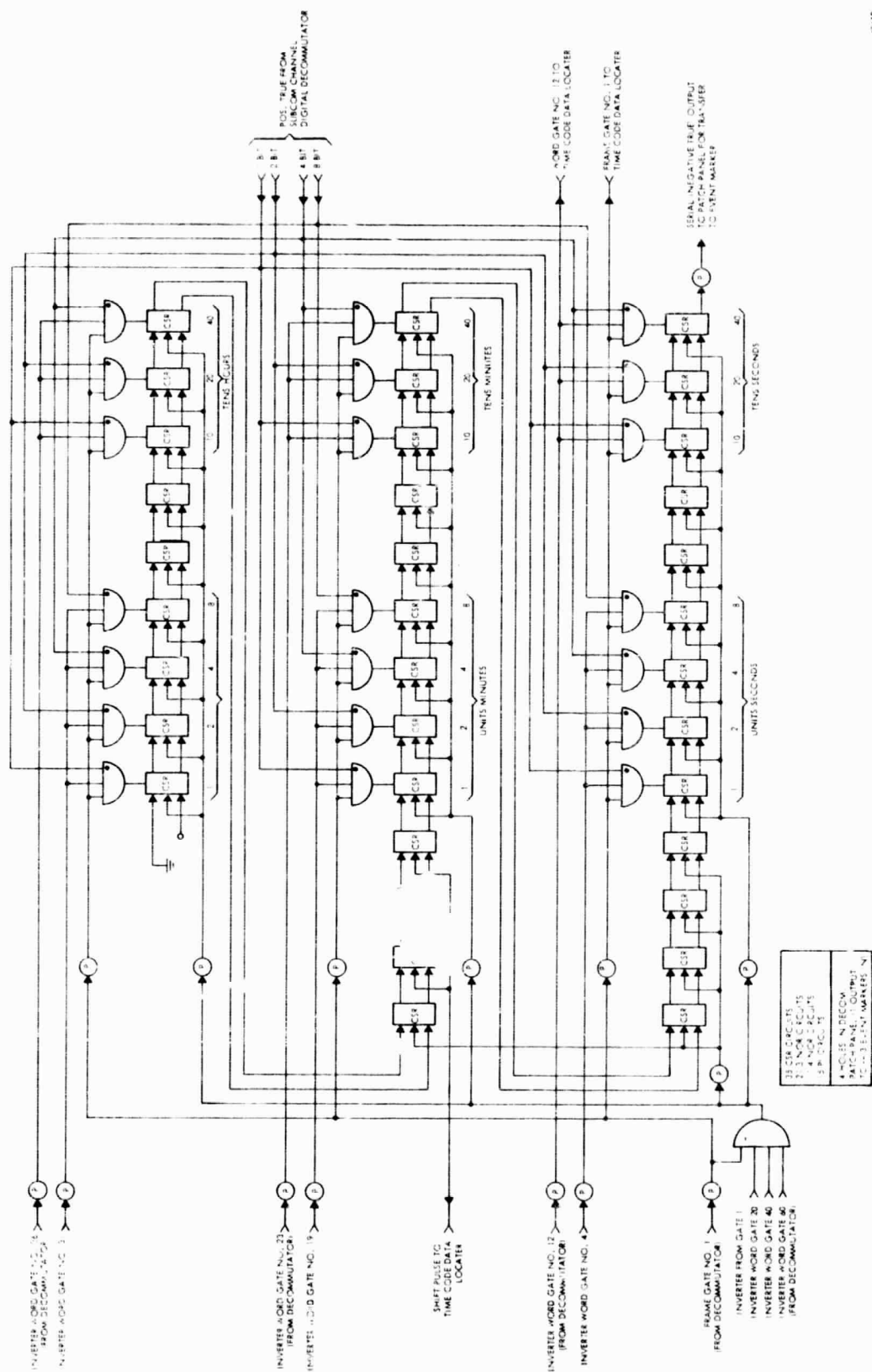


Figure 74. Time Code Decommutator/Serializer Unit
Logic Diagram

mation is available. Other than the frame and word gate pulses, the third input to the decommutation gates is the data, which is gated into set the shift register when the gate is fully enabled. Since all loading occurs in the first subframe, shifting of the shift register is inhibited during the first subframe. After the first subframe the shifting begins and bits are shifted out at the rate of three bits per subframe, so that by the end of subframe 13 all data is out of the register. Even though the register is clear, shifting still occurs until the beginning of the next major frame, so zeros are put out for about one-fourth of a major frame. Tens of seconds appear first, then units of seconds, tens of minutes, tens of hours, and last is units of hours.

- 1.19.2.5 The Time Code Data Locator unit (figure 75) consists of a ring shift register which is loaded with a pattern of bits during the first subframe and then is shifted simultaneously with the Time Code shift register. The pattern of bits produced, marks the first third of the Time Code data to facilitate reading it, and the register circulates around and repeats itself until it has run through the pattern a total of three times to mark all of the Time Code data (figure 76). After it has cycled three times, its output is inhibited during subframes 14, 15, and 16 so no more marking occurs. In subframe 1 then, when shifting is inhibited, the register is reloaded and starts its cycle again.

MARKS PLACED ON CHANNEL ADJACENT TO TIME CODE BY DATA LOCATOR

TIME CODE DATA	_____	_____	_____	_____	_____	_____	_____
	140 20 101	18 4 2 11	140 20 101	18 4 2 11	140 20 101	18 4 2 11	140 20 101
	TENS SECONDS	UNITS SECONDS	TENS MINUTES	UNITS MINUTES	TENS HOURS	UNITS HOURS	TENS HOURS
	5 9	3 5	1 6				
	SECONDS	MINUTES	HOURS				

DATA IS SHIFTED
OUT THIS WAY

THIS END APPEARS
FIRST ON THE
EVENT MARKER

Figure 76. Time Code Locator Trace

Table 10. Circuit and Card Count for Proposed Digital Channel

Decommutator Subsystem:

132 CSR Circuits Require	44 CSR Cards
148 PI Circuits Require	15 PI Cards
12-Nor Circuits and 21 3-Nor Circuits and 2 4-Nor Circuits Require	4 3/4 -Nor Cards
82-Nor Circuits Require	<u>12 -Nor Card</u>

64 Cards total (to
be located in a
separate drawer)

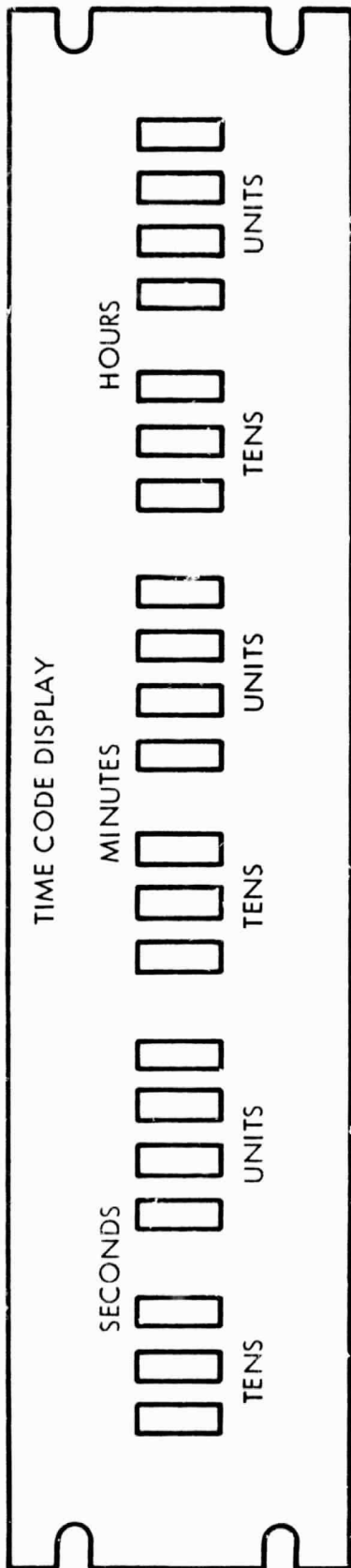
32 holes in the recycling area of the existing decom patch panel are required. The many patch boards now being used could be re-silk screened to identify the Digital Channel patch area or patch panel decals are available to change this area.

- 1.19.3 Event Recorder. - The Brush multi-styli, electrosensitive writing recorder is the type event recorder proposed to record and display the digital channels. The Model 14361500 accomodating up to 150 channels is complete in only 15 1/2 inch panel space. A copy of Brush's specification sheet is enclosed (Appendix X, Section 4) here for a detailed description. This unit has chart speeds compatible with the Brush Analog recorders used in the present NIMBUS Ground Station. The Brush Trans-Switcher input switch circuits are proposed to drive the event recorder and are considered a part of it. They provide solid

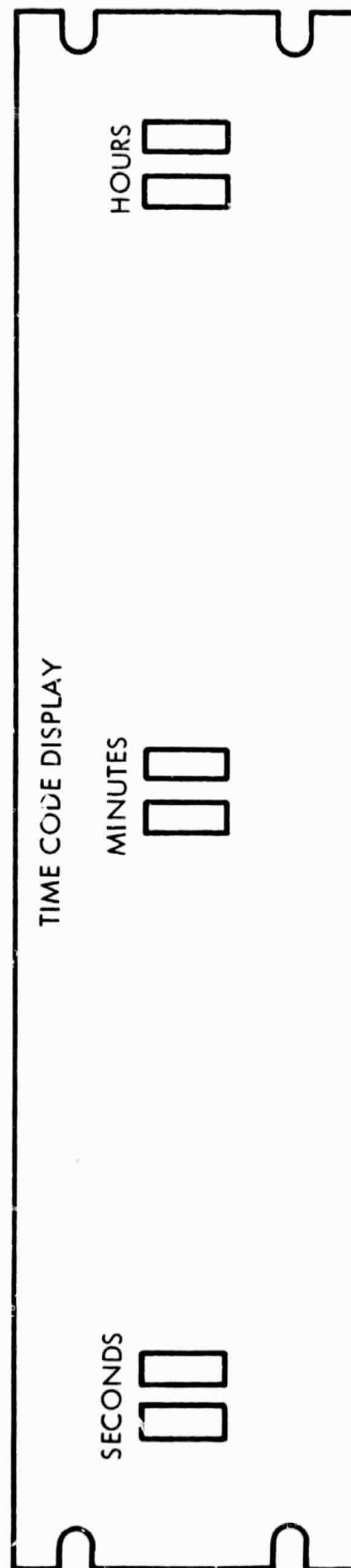
state switching that the normal system logic levels will drive adequately. The Brush specification sheet (Appendix XI, Section 4) describes in detail these input circuits. The Model 11340203 or 11340204 is preferred. These circuits plug in the event record requiring no additional space or external power other than input signal.

1.19.4 Time Code Display. - The Time Code will be recorded as a serial trace or a channel or channels of the event recorder. It is proposed that since a broad-side output is available that a visual display also be included with a remote output connection to route Time Code data to any other display sites. The rapid indication display would be helpful as a search area indicator during playback of recorded data for further processing. The display could be packaged as a separate panel or in the front of the Digital Decommutator Drawer.

1.19.4.1 A simplified visual display panel was used on the breadboard test setup to display Time Code data. It comprised a labeled panel with 21 subminiature amperex glow-tube lamps arranged to indicate each BCD Time Code word (figure 77). The data input is routed to 21 CSR storage stages that directly drive the indicator lamps. A small 60 VDC (less than 5 ma needed) and 1 volt filament supply powers the glow-tubes. The CSR's and power supply would be included on this panel.



AMPEREX TYPE 6977 GLOW-TUBE INDICATOR BCD DISPLAY



"NIXIE" UNITARY DISPLAY

Figure 77. Time Code Display Panels

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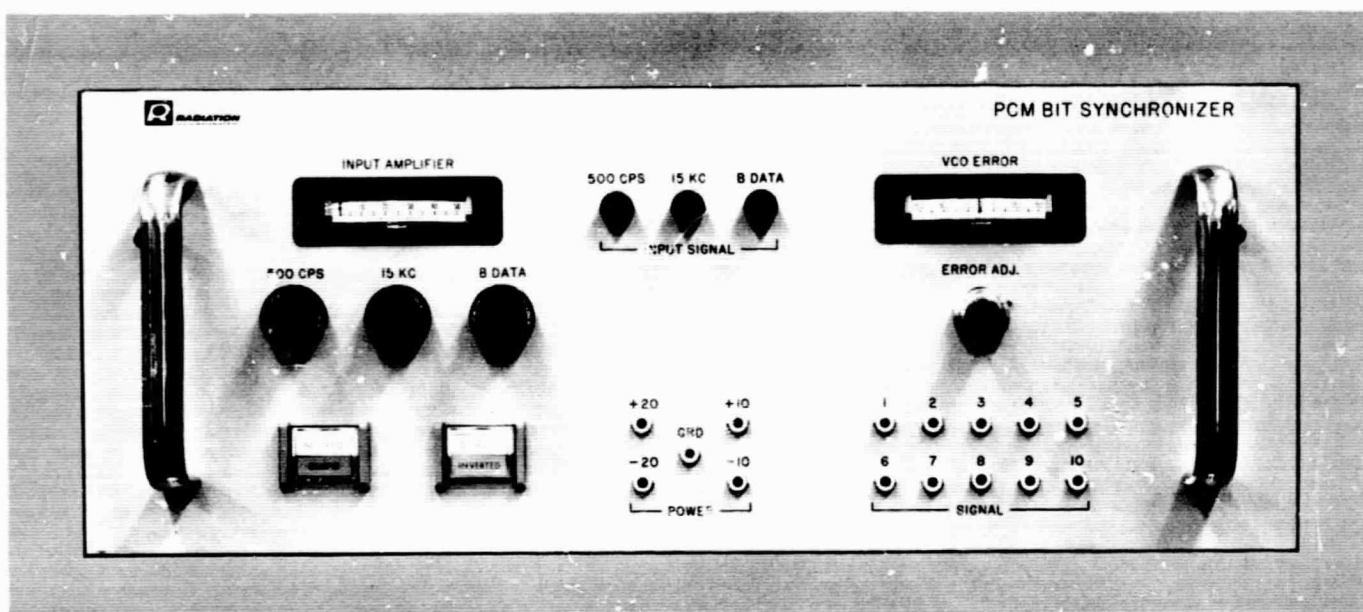
1.19.4.2 A more sophisticated display panel would use "NIXIE" type read-out lamps converting the BCD to unitary for easier rapid reading. The miniature "NIXIE's" Model 104549-1 complete with converter drivers and power supply easily package right on the display panel are moderate in cost using two tubes per word for a total of 6 "NIXIE's" required.

1.20 SUBCARRIER MODULATION STUDY. - Performance checks in the NIMBUS Bit Synchronizer and other Radiation Bit Synchronizers have indicated that improvements could be made to the bit synchronization of the NIMBUS System. If the distortion and overshoot of the present gated sine wave signal could be eliminated the present NIMBUS Bit Synchronizer could be modified to integrate over the full bit interval with a subsequent 2 to 3 db signal-to-noise improvement. This would be very close to the theoretical optimum for RZ type signal. However an NRZ type signal offers a theoretically 3 db better S/N performance over the RZ type signal. Thus the ground equipment study effort was first directed to investigating the modification required for the NIMBUS Ground Station to handle NRZ type signals. It became evident normal NRZ type modulation presented combined problems (paragraph 1.13). It was decided that split phase type modulation was actually an NRZ type signal (one state for a "0" and the opposite of a "1") and very nearly the same S/N performance improvement of the Bit Synchronizer could be obtained with this signal.

1.20.1 Investigation of Handling NRZ/NRZI Type Modulation. - Even though split phase modulation is proposed, primarily for ease of implementation in

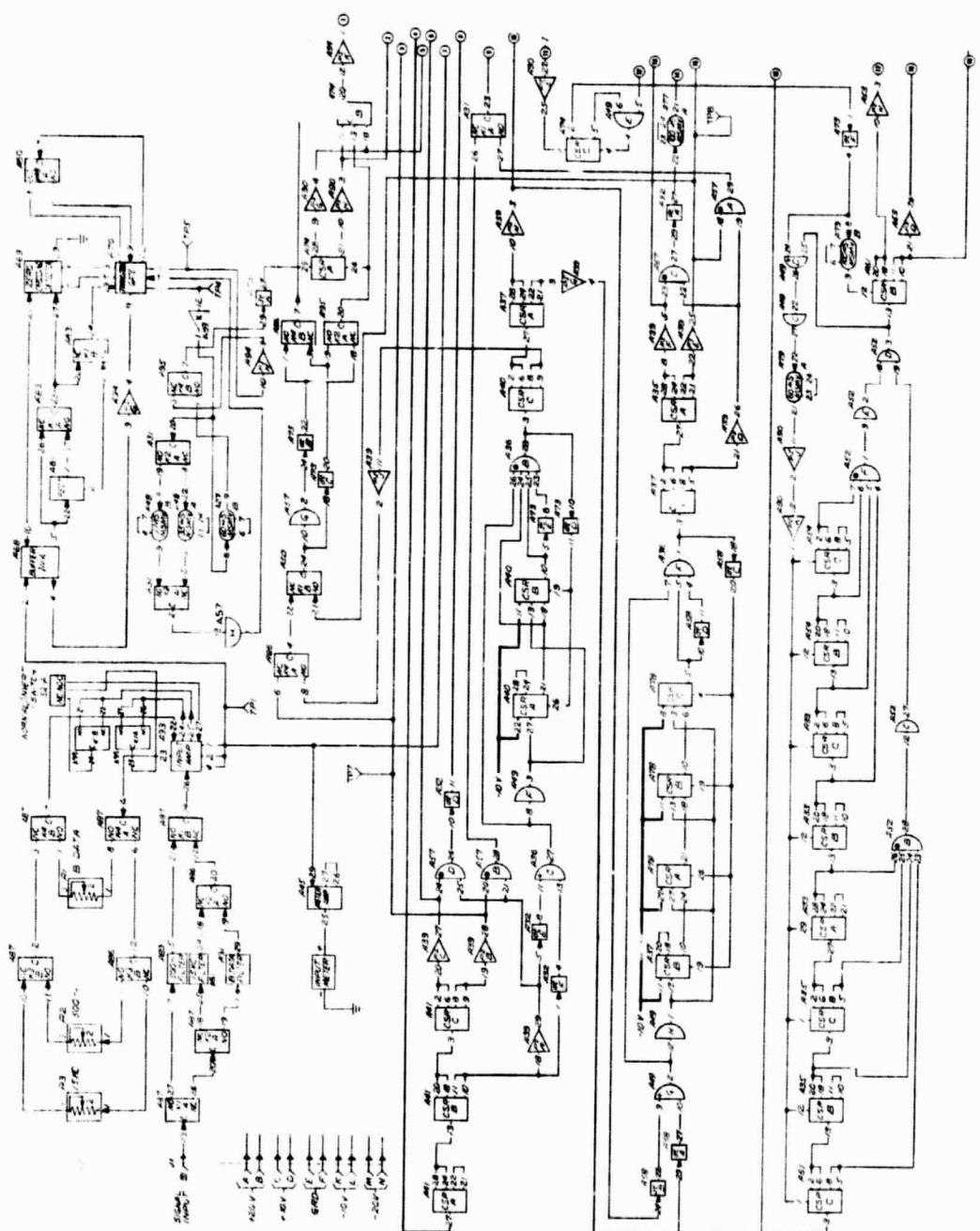
the airborne equipment, a preliminary investigation was made into accepting normal NRZ signals through the Ground Station. The findings are presented mainly for documentation. The squelch detection circuitry would require modification and is more of a problem with NRZ signals where automatic detection of several bit rates are required. The data content directly affects the frequency content of the input signal train. A possible detection method would be to use a string of alternate "1" and "0's" at the beginning of each type data transmission to indicate data type. The frame sync code pattern could produce the required detectable excitation for the squelches.

1.20.1.1 The present NIMBUS Bit Synchronizer (figures 78 and 79) would require modification to by pass the input filter, add dc restoration to the output of the input amplifier for better operation of the zero crossing detector and change sync timing loop to utilize some minimum number of level changes (worst case code patterns). If NRZI type signal is used such that a "0" is indicated by a change of level of the signal and a "1" is indicated by no-change, then the present NIMBUS word sync pattern (a "0" bit at beginning of each word) would guarantee at least one level change (data transition) per 8 bit intervals as worst case data. The bit decision circuitry would also require changing to make bit decisions by full period integration of the bit interval. Using much of the present synchro-



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Figure 78. PCM Bit Synchronizer Panel



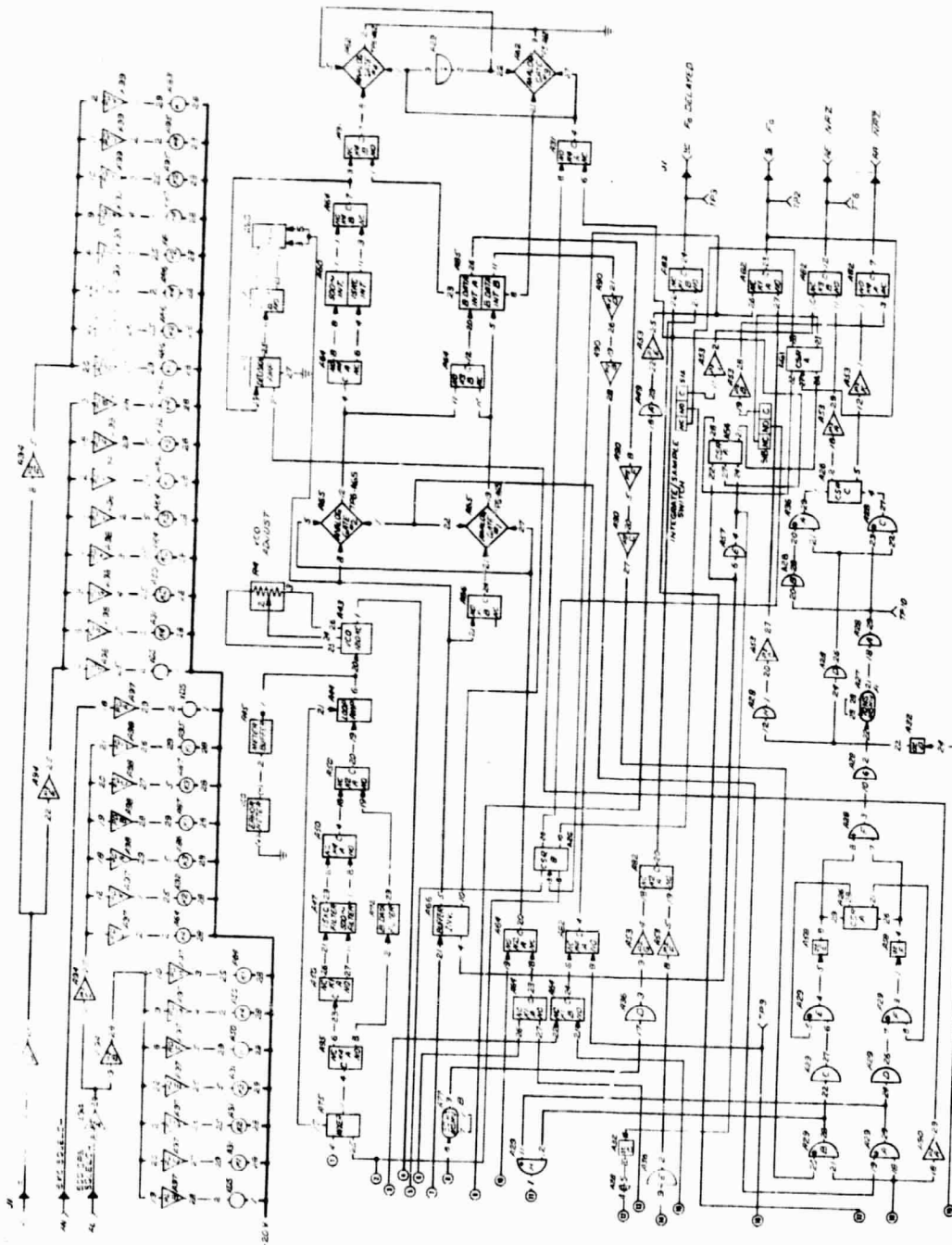


Figure 79. Bit Sync Logic Diagram (Sheet 2 of 2)

nizer's logic this could be accomplished by inverting the NRZ signal routing it through a second analog gate, opened during the off half cycle the 1st analog gate, and to a second integrate circuit. Both integrate circuits would be routed to differential inputs of the decision amplifier. The present level determining logic would then provide NRZI output if this type signal is used or NRZ if that is used. Conversion of NRZI to NRZ is easy enough to implement by using a differentiator, inverter and flip-flop reset by bit rate.

1.20.1.2 A second method of bit decision logic requires no input analog gate and only one integrate circuit. The NRZ signal is routed directly to the integrate and dump circuit with dump control occurring at end of each full bit interval. Output of integrator is routed to two decision amplifiers, one biased as an "up" level detector, and the other as a "down" level detector. The outputs set or reset a flip-flop reconstructing NRZ or NRZI output. One decision amplifier, a buffer inverter, a differentiator and 2 2-Nors would need to be added to existing bit decision logic (figure 80).

1.20.2 Split Phase Modulation. - The investigation into handling split phase modulated signal led to building breadboard circuitry to ascertain feasibility and make S/N performance checks. Modifications to the NIMBUS Bit Synchronizer were in two areas:

a. Synchronized timing loop

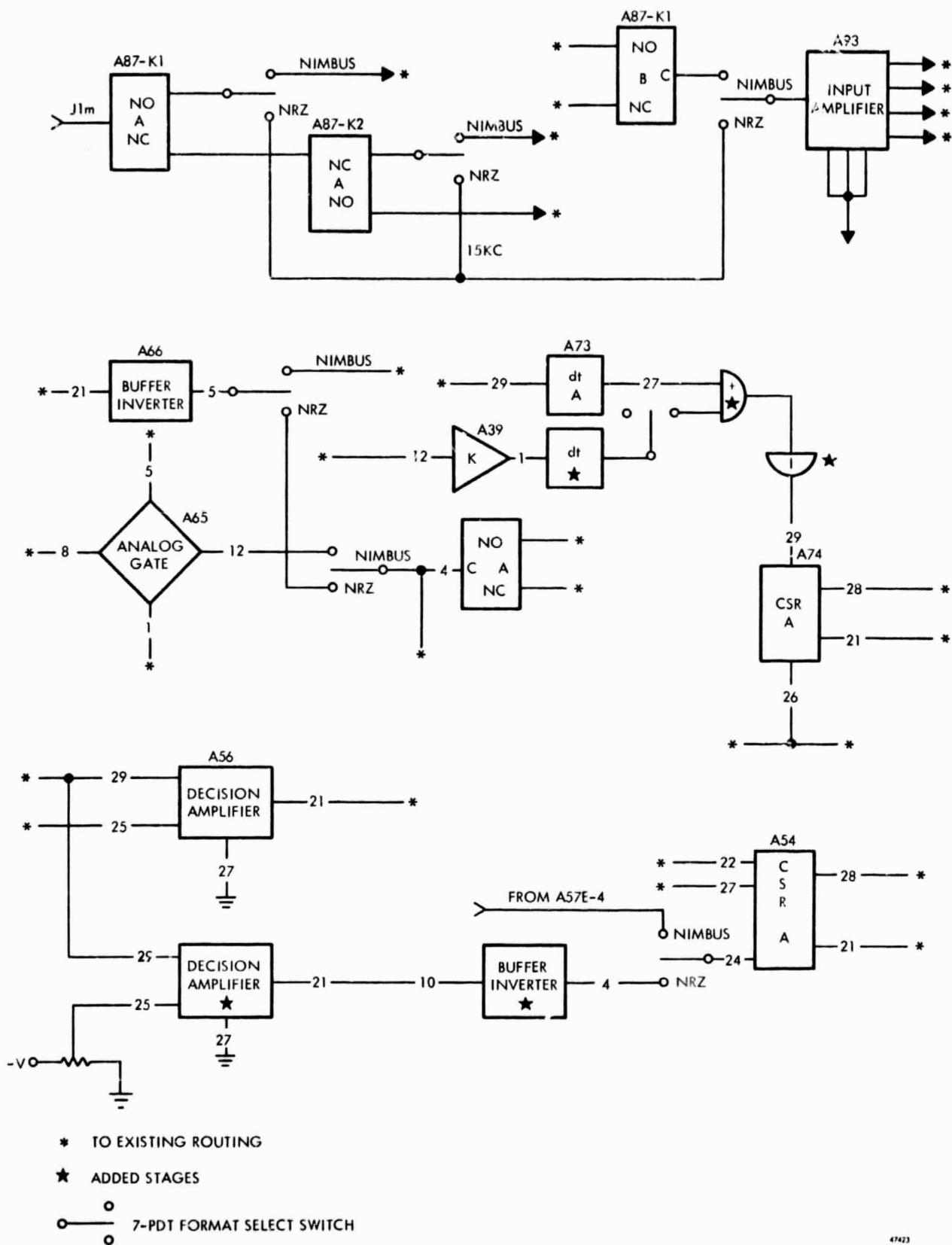
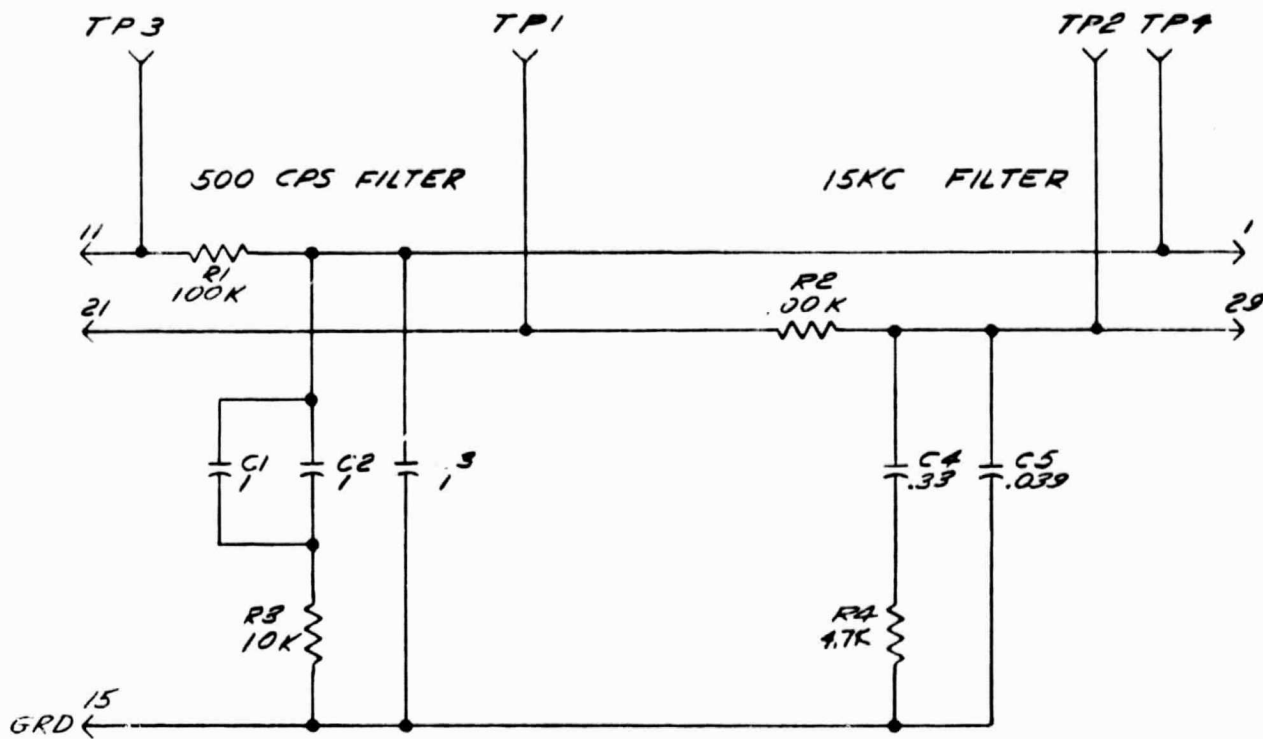
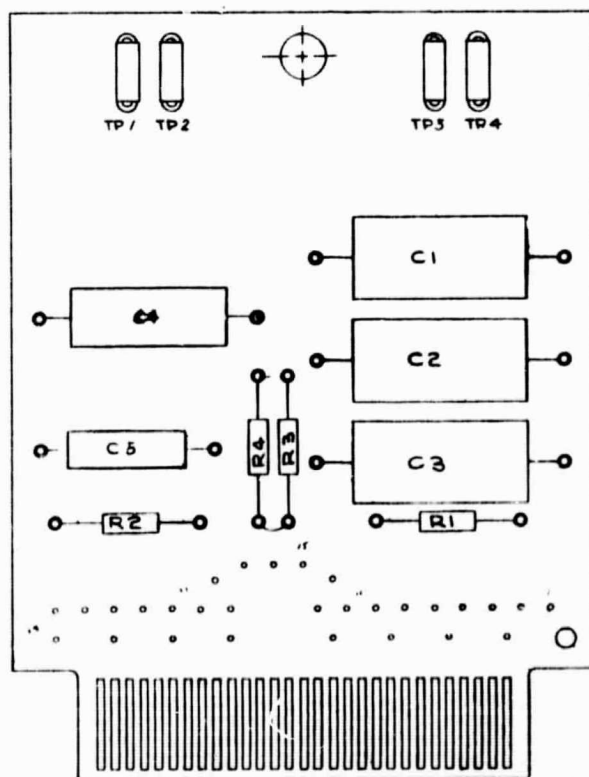


Figure 80. Changes to Bit Synchronizer to Process NRZ Data

1.20.2.1 To use maximum number of data transitions as sync information it was necessary to full wave rectify the incoming signal (as is done in B data mode) and sync the loop at double the bit rate. This was done by forcing relay control to A83A-K1 to select A data signal through rectifier A81 to the Level Detector portion of Transition Gate A70. The Zero Crossing Detector signal path was not used. The output from the Level Detector on pin 11 was routed through driver A39K, and the normal signal path was changed, breaking the input to inverter A57H and routing output of A39K to A57H. The output of A57H was changed to go input to differentiator A73A to trigger data CSR A74A of phase detector logic. Thus the rectified input through the level detector generates maximum number of transitions (2 per bit interval for no phase change and 1 per bit interval of phase change). However it is now necessary to run the phase detector at twice the bit rate to sync with increased transition rate. This was done by changing the input (clock path) to relay A86-K4-NC from bit rate at A39B to twice bit rate at A39A. Also it was necessary to change the loop filter A47 for twice the bit rate. This was done by cutting the time constant in half; C3 (figure 81) was changed to .5 mfd and C5 to .02 mfd. This was a minimum effort change to the loop and should be looked into further for optimum performance at twice the bit rate.



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Figure 81. Loop Filter (500/15KC) Schematic Diagram
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1.20.2.2 Bit decision logic was investigated with efforts toward simplified logic design to detect phase changes in the signal. It was felt that it should not be necessary to determine the correct phase of the signal as is required in split phase level type where one phase is a "0" and the opposite phase is a "1". A split phase mark type signal had been chosen where a phase change indicates a "0" and no phase change a "1". Functionally, there was need to integrate and dump for maximum noise immunity in order to determine the phase of a bit interval and compare it with the phase of the next bit interval.

1.20.2.3 The first approach tried was to utilize a matched filter integrator. Past tests on the matched filter integrator indicated this type to be optimum for waveforms that did not change with data content. Split phase signals are very uniform in waveshape with very little distortion generated in changing phase. The output of the matched filter should merely change polarity for opposite phase signal (see figure 82 for logic block diagram.). The $\pm$ peak detectors were used for dc restoration but were not found necessary with split phase data. They also supplied automatic level control (ALC) for the level detectors but would not be necessary if the input signal level was reasonably constant. Looking at the waveforms it can be seen that for one phase of data with respect to the clock, the dump occurs at the time of phase change when a "0" occurs (waveform 2 and 3) resulting in an integrator output (waveform 5) whose polarity

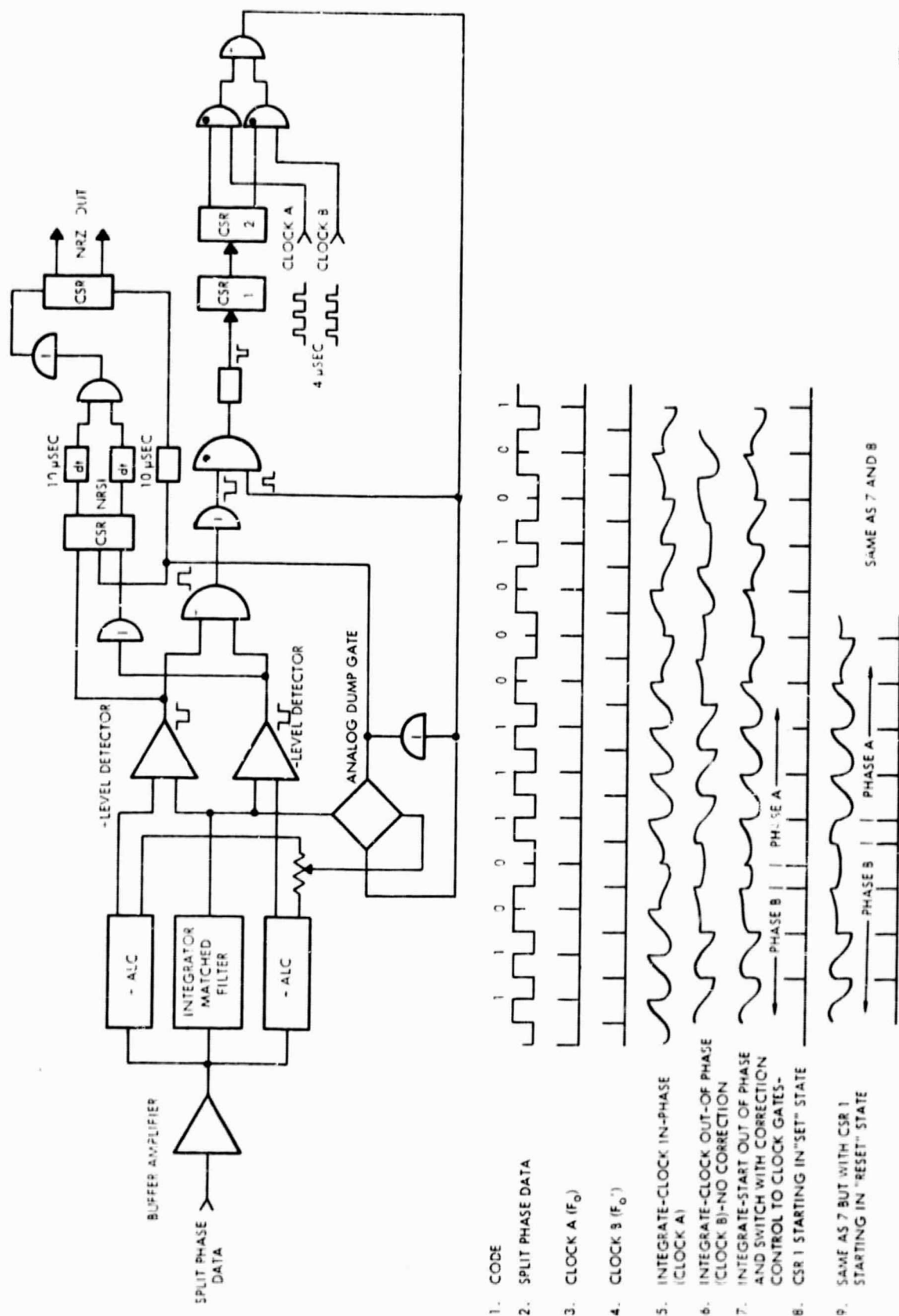


Figure 82. Matched Filter, Split Phase Decision Logic Diagram

changes for "0"s. However, with the signal and clock synced 180 degrees out of phase (waveforms 2 and 4) such that dump signal always occurs in between phase change times the integration output (waveform 6) has nearly zero output during phase change intervals and maximum level (either polarity) at dump time during no change intervals. The problem existed to determine which phase was the more useful and to provide phase correcting logic to maintain one phase. Since this was contrary to a simplified logic approach, a test was run employing the scheme shown where + and - level detectors were OR gated together and AND gates with the dump signal. If the clock and signal are in phase (waveforms 2 and 3), there will be an inhibit at this AND gate and no output to phase correcting logic. If the opposite phase is occurring there will be no inhibit pulse at the phase changes ("0"-bits) and the dump pulse will be routed through a differentiator generating a trigger on the trailing edge of the dump pulse toggle CSR1. Two phase correcting triggers (or one depending on the starting state of CSR1) switch CSR2 changing selection of clock to other phase which cause inhibiting pulses to occur and no further phase corrections unless errors occur of clock should change phase. The level decisions are clocked into the CSR at dump time. Each edge is differentiated and OR gated together to set the "0" side of NRZ output flip-flop. The "1" side is set by a narrow clock pulse such that when transitions occur they override and set a "0", and absence of transition allows a "1" to be set in generating NRZ from NRZ1.

- 1.20.2.4 A S/N performance check was run on the above simplified matched filters approach and indications were that there was no improvement over the present $1/2$ cycle integrate of the gated sine wave signal. It was noted that the addition of a second integrator operating off the opposite phase of the timing would be a better approach eliminating the need for phase correcting and error analysis logic. See (figure 83) for logic diagram and waveforms. This required four decision amplifiers as well as two matched filters but appears to offer solution to phase decision requirement.
- 1.20.2.5 The ideal matched filter for a square waveform signal is an RC integrator. Since the split phase signal decided upon was to be square wave with system processing introducing no appreciable degradation it was decided that a simple RC integrator was very adequate. The second approach used two integrate and dump circuits, one for each phase of the signal. See (figure 84) for logic diagram and waveforms. The purpose of this design was to insure that one integrate and dump circuit would integrate alternate half cycles irrespective of the data pattern of phase relation. The other integrate and dump circuit would perform the same function on "1's" (no phase change) except integrate over two consecutive polarity half cycles every "0" (phase change). Outputs of the level detectors (waveforms 4 and 5) are compared differentially in two separate decision

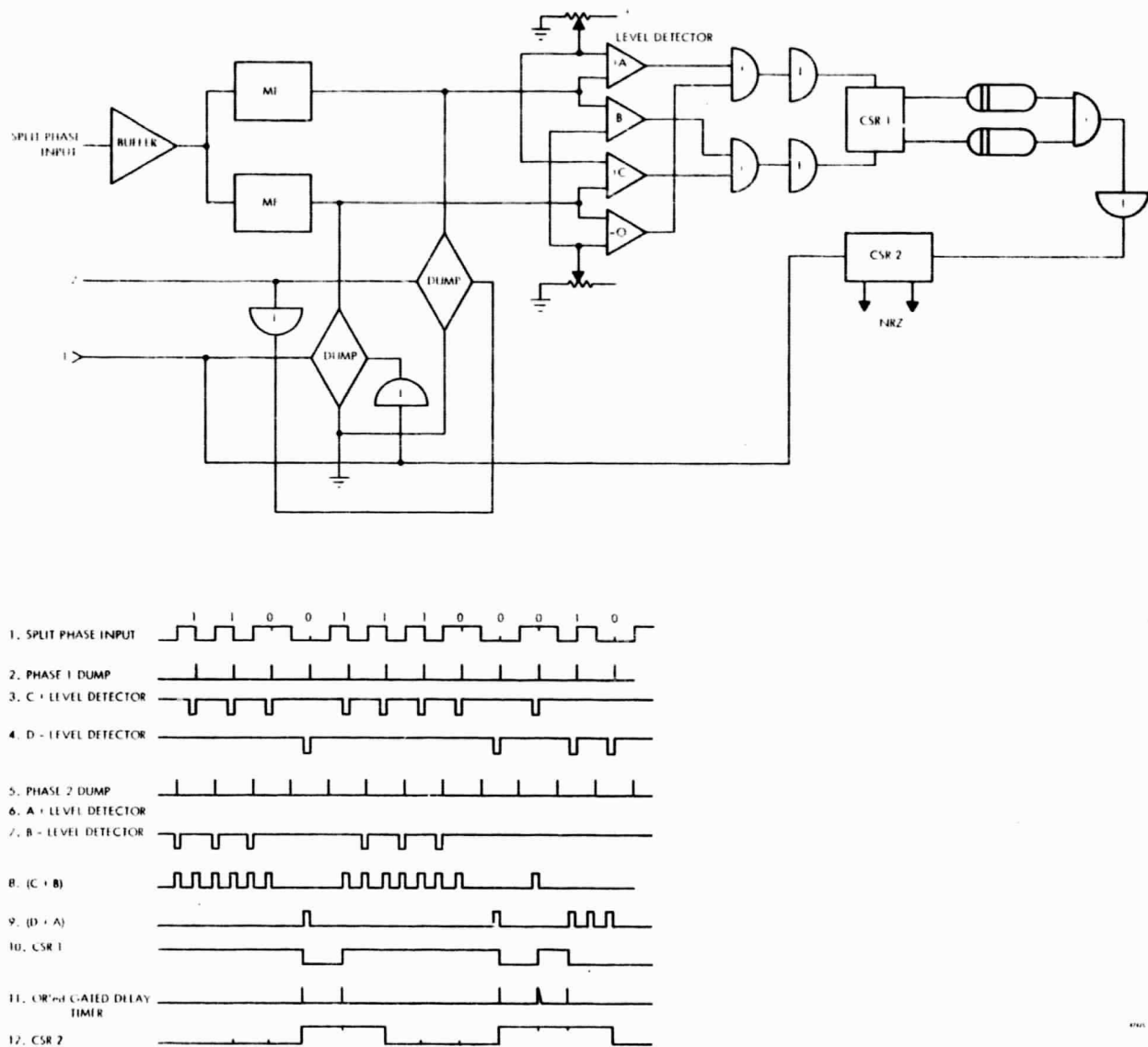
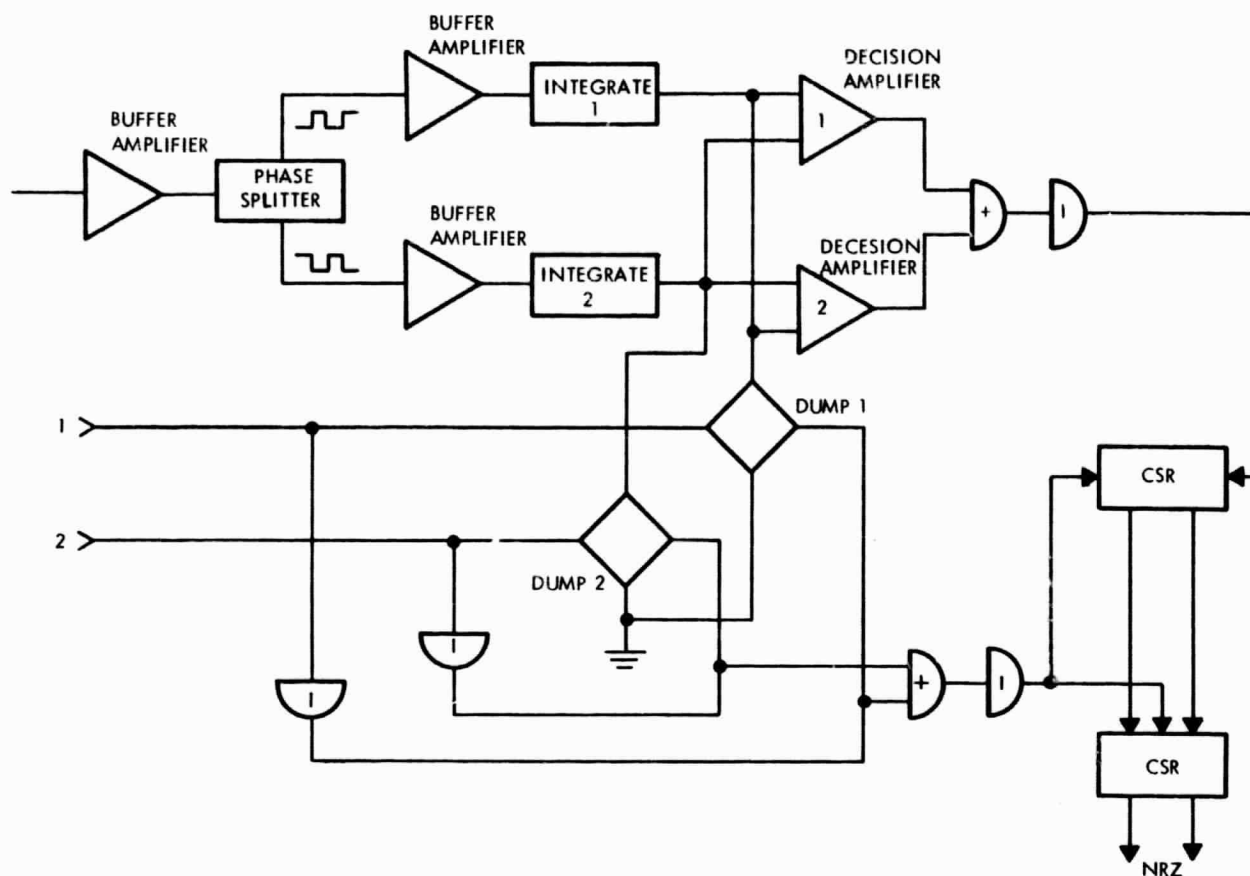


Figure 83. Double Matched Filter Logic Diagram



1. SPLIT PHASE INPUT
2. DUMP 1
3. DUMP 2

4. INTEGRATE 1

5. INTEGRATE 2

6. DECISION AMP 1

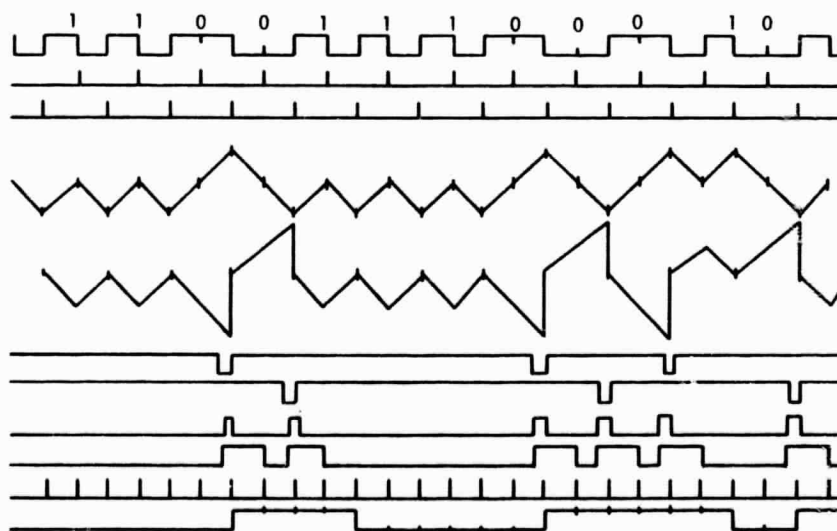
7. DECISION AMP 2

8. OR GATE DECISIONS

9. CSR 1

10. OR GATE CLOCK

11. CSR 2 (NRZ)

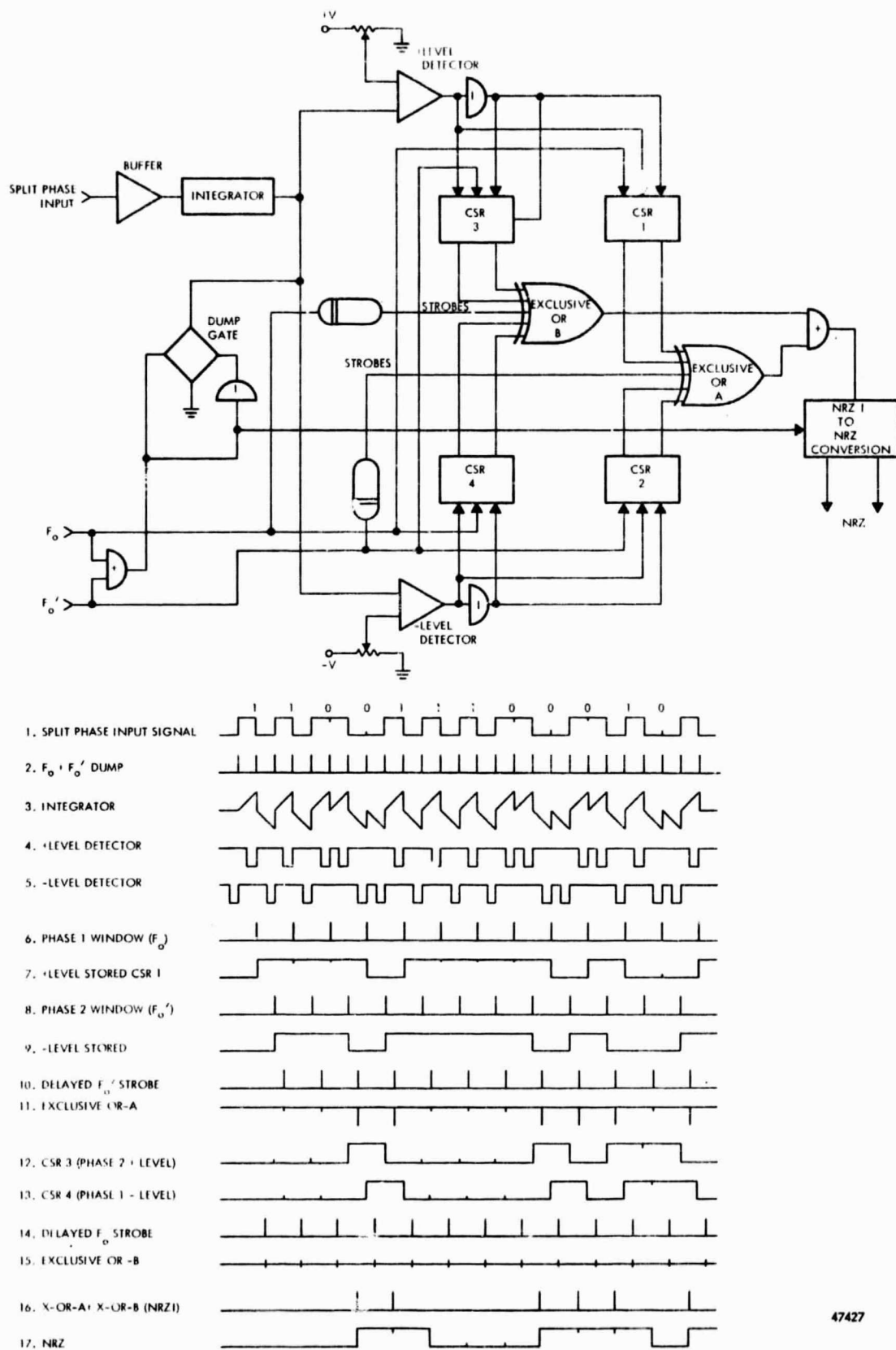


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Figure 84. Decision Logic (Approach 2) Diagram

amplifiers biased to trigger at 75% maximum difference. Outputs of the decision amplifiers were OR gated together indicating "O"s and routed to NRZ1 to NRZ conversion logic. This approach gave correct decisions but suffered from S/N performance because of the many false decisions from decision amplifiers when appreciable noise was present. To improve this, it was necessary to add a window on the output of the decision amplifiers. This required determining and maintaining correct phase of the timing for the window (sample) and once again involved more complex logic than desired.

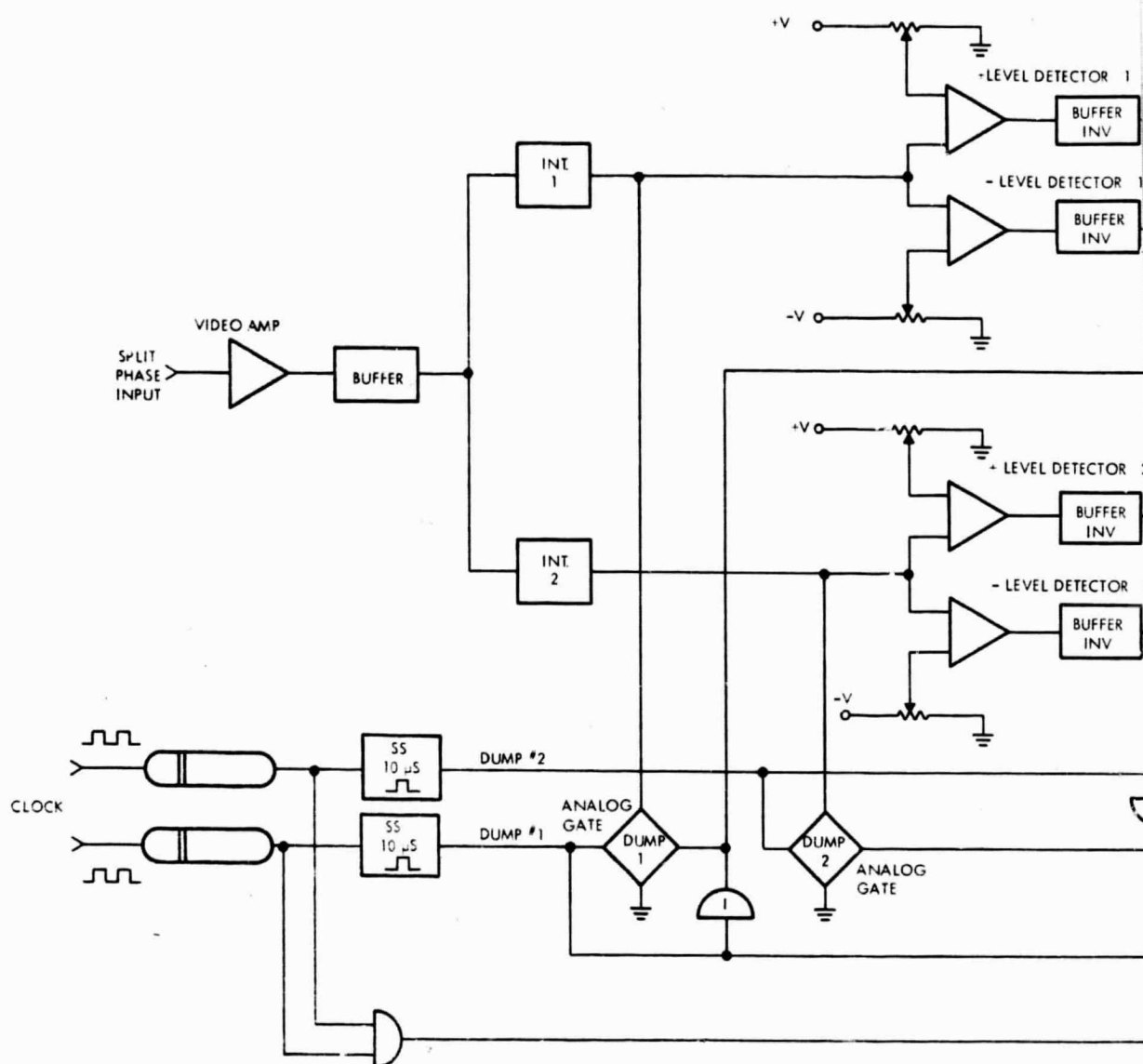
1.20.2.6 Study program time was now running out but a third approach was tried whereby one integrator was dumped at the end of each $1/2$ cycle (by each phase of the clock) at a 30kc rate. See figure 85 for logic waveforms. Plus level and minus level decisions were made in separate decision amplifiers biased from ground. However, separate windows were generated, one for each phase, to sample the decision amplifiers and store decisions in CSR's connected to Exclusive-OR logic looking for consecutive $1/2$ -bit polarities indicating a phase change. Since one phase of timing will produce no consecutive $1/2$ -bit polarities, with consecutive groups of two $1/2$ -bits at bit rate, regardless of data, there will be no output from one Exclusive-OR group. The other logic group looking at consecutive groups of two $1/2$ -bits, but delayed or displaced $1/2$ cycle, will produce an output each time a phase change occurs in

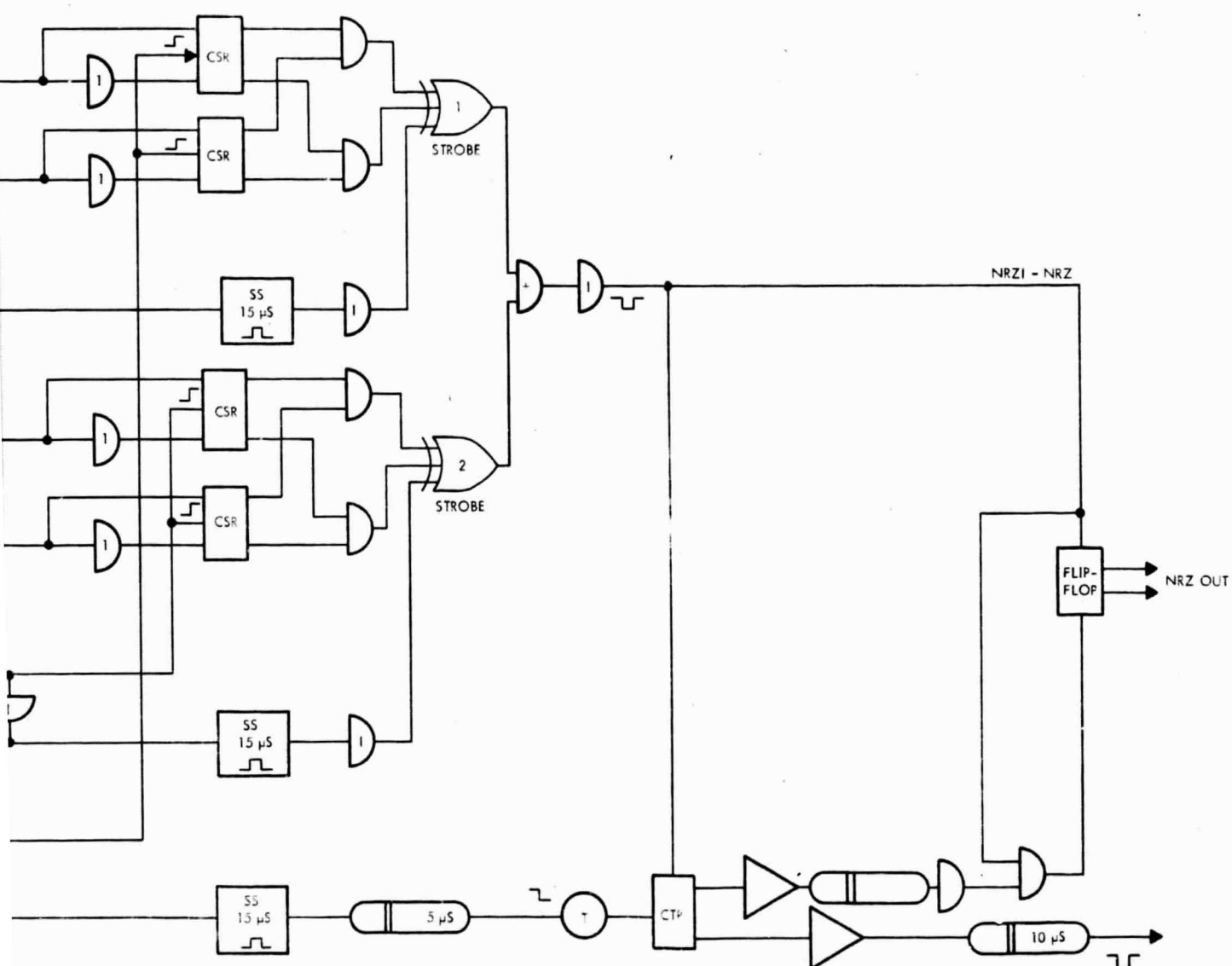


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Figure 85. Decision Logic (Approach 3) Diagram

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Figure 86. Full Cycle Bit Decision for Split Phase Signal Block Diagram

the signal. This output is then routed to trigger a flip-flop with resultant outputs as NRZ1. The next step converts to NRZ in a conventional manner.

1.20.2.7 The third approach was breadboarded and checked (figure 86) and proved to work quite satisfactorily and waveforms as predicted were still observed. However, closer investigation revealed shortcomings of this approach to be that the $1/2$ -bit comparisons were using effectively only $1/2$ cycle of data for decisions which again is 3db loss in S/N performance. The addition of a second integrator and two more level detectors (figures 87 and 88) would enable a similar technique to be used whereby integration would be performed over the full bit interval. Duplicate decision logic is furnished for both phases of timing. One phase would produce no level decision as value of integrator over a full bit interval at dump time would always be zero. The opposite phase of timing would produce maximum (twice the $1/2$ -bit integrated output level) level at bit decision (dump) time for "0" bits (phase change) and zero level for "1"s (no phase change). Therefore, regardless of the phase of the signal and the clock timing, phase changes would be detected through one logic path or the other, but not both. Having the paths OR gated together then eliminates the need to know the correct phase of the timing or if the timing is maintaining constant phase lock. There is no need for analysis decisions to determine if they

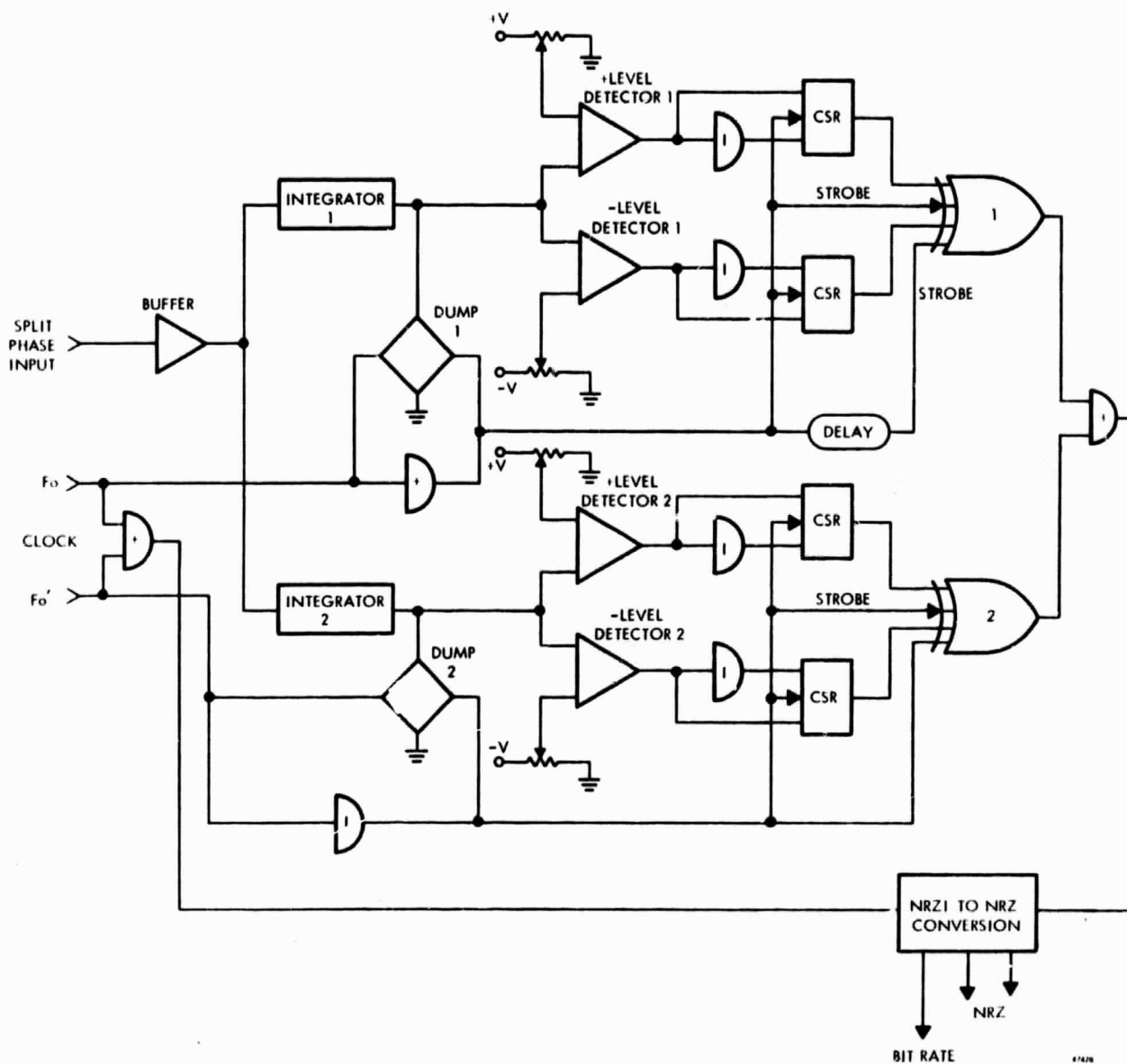
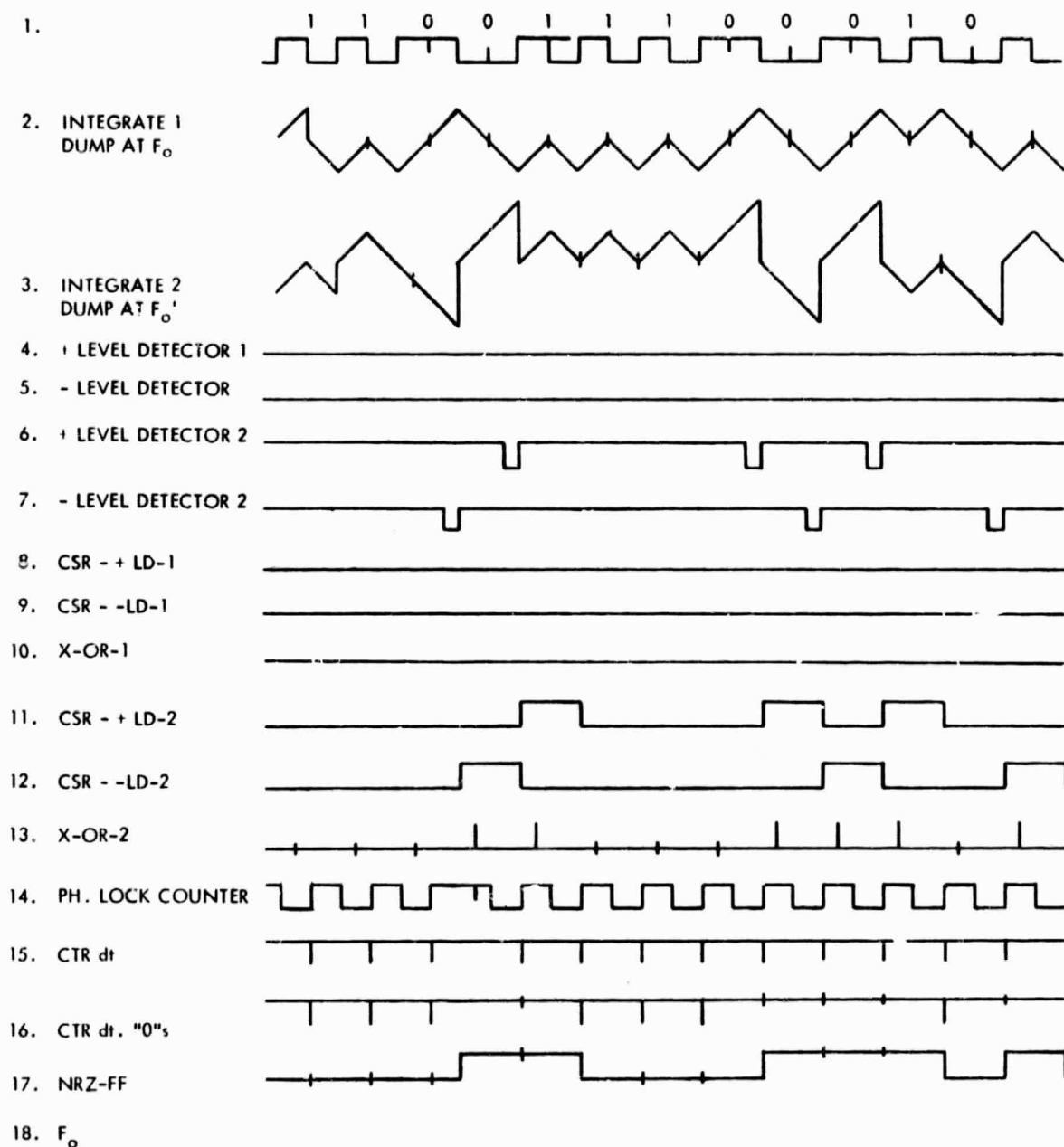


Figure 87. Full Cycle Bit Decision for Split Phase Signal Logic Diagram



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Figure 88 Full Cycle Bit Decision Waveforms

are likely to be reliable or are false indications because of improper timing.

- 1.20.2.8 Radiation's Universal Bit Synchronizer, Model 4041, as employed in the Series 540 PCM Acquisition and Stored Program Decommutation System (in fact the complete 540 Station) was available at Radiation for tests with NIMBUS new format data. (See Appendices XII and XIII for description and specifications of the Model 4041 Synchronizer and 540 Decom.) The Universal Synchronizer accepts, as one of its standard inputs, split phase mark (SPM) data. A program was derived and manually inserted into the 540 System enabling it to process the new format NIMBUS data. Tests were run using the breadboarded simulator and the S/N test set-up to obtain S/N performance data on the Universal Synchronizer and simplified logic. The 540 System has 3 decimal displays and 1 binary display. These were used to monitor decommutated data for proper data content.
- 1.20.2.9 A brief explanation of the bit decision technique used in the Universal Synchronizer for split phase data may be followed from figures 89 and 90. Three integrate and dump circuits are used. Two of these, integrator "A" and "B", have signal input gated in to integrate $1/2$ cycle in one circuit and the next $1/2$ cycle in the other circuit (waveforms D2, G2, F2 and I2). The dump time is the same on integrators "A" and "B" and their output is applied to differential inputs in one decision amplifier.

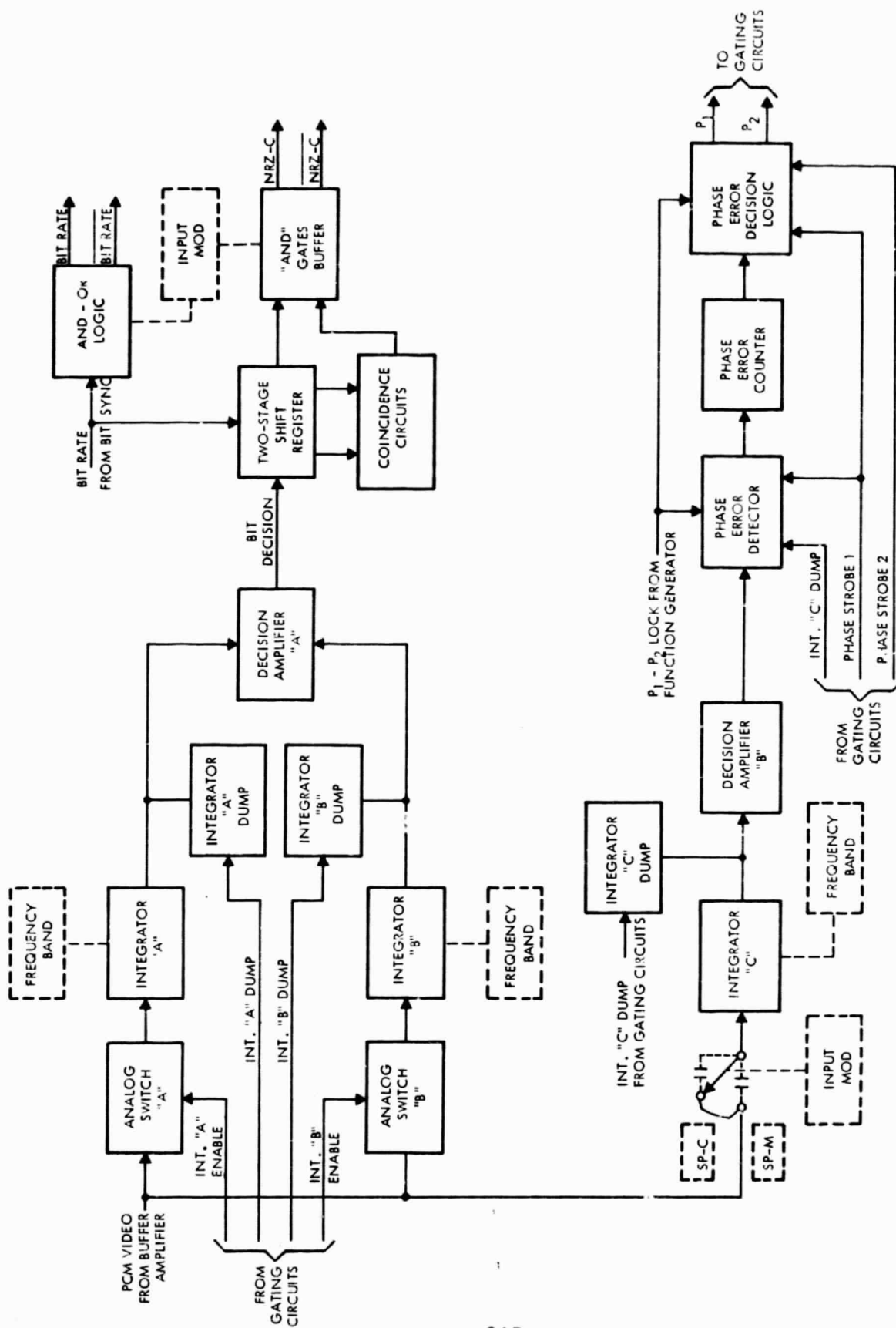
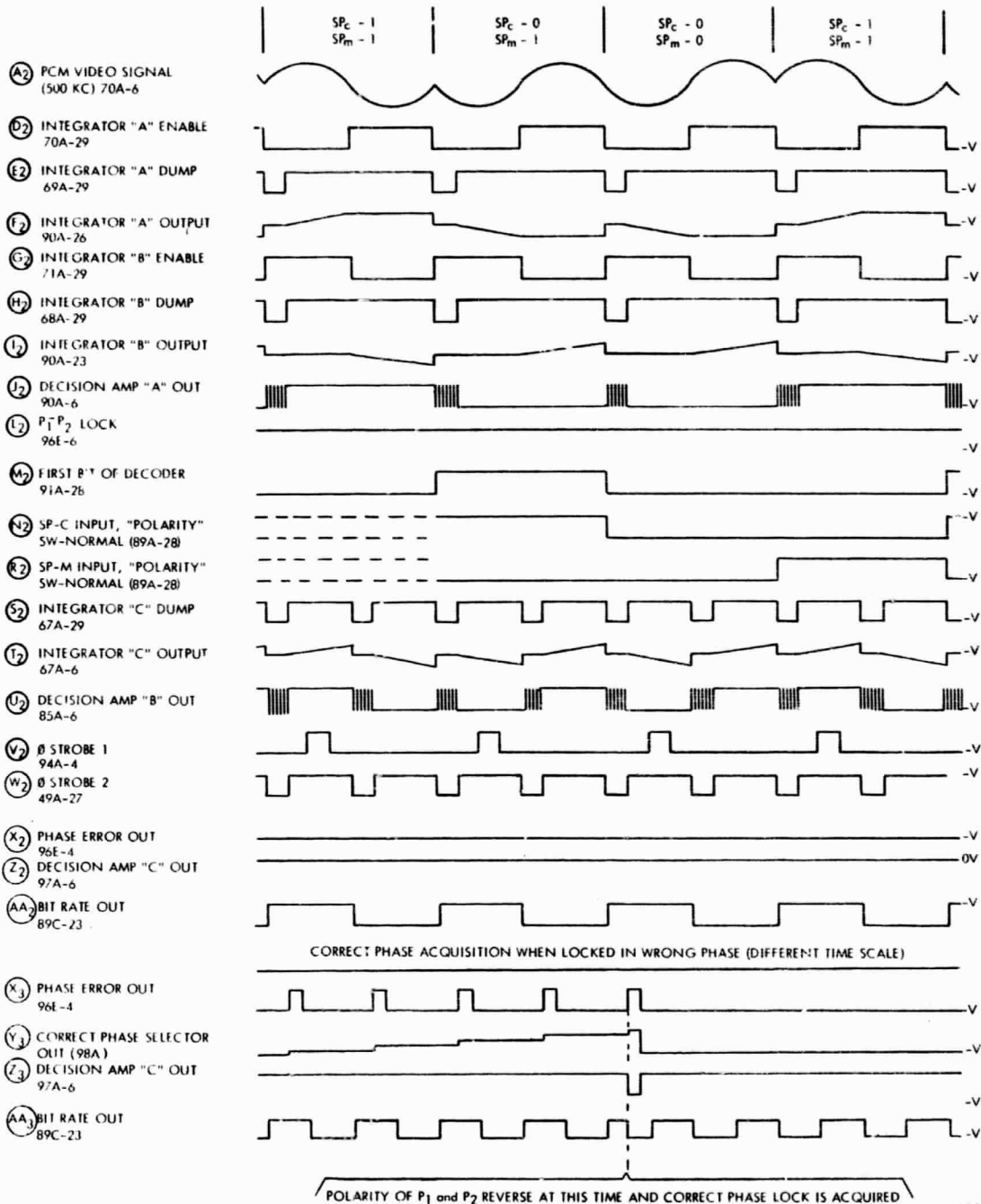


Figure 89. Universal Bit Synchronizer Logic Diagram

SPLIT-PHASE OPERATION LOCKED IN CORRECT PHASE

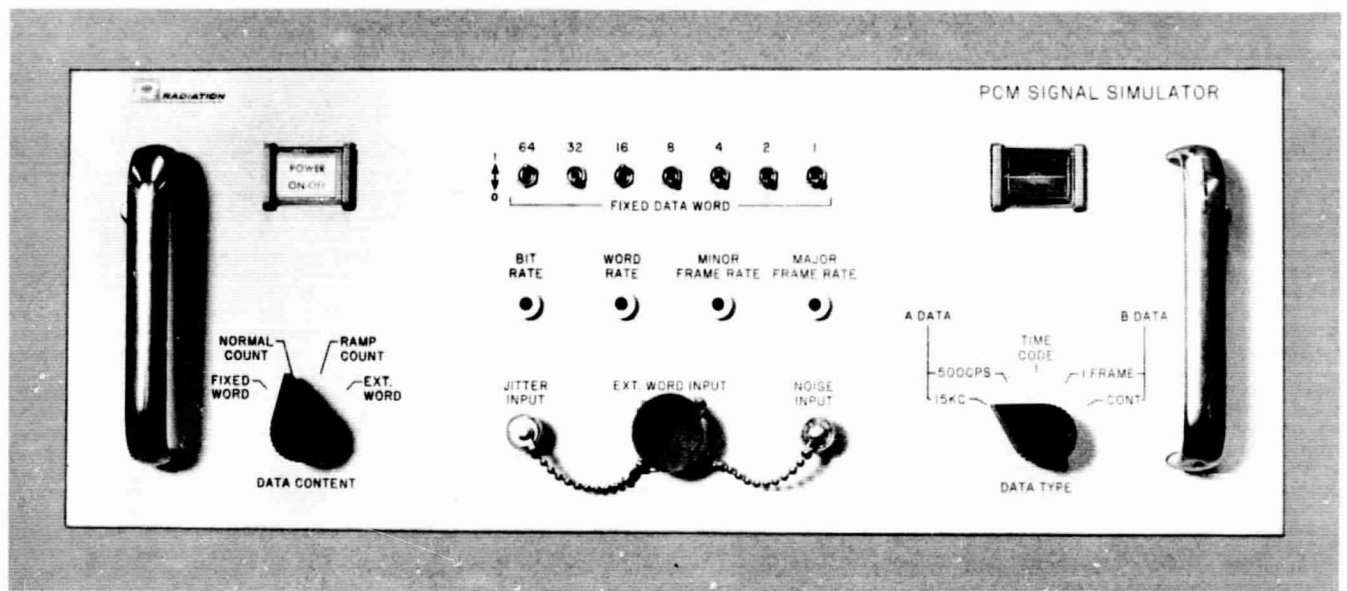


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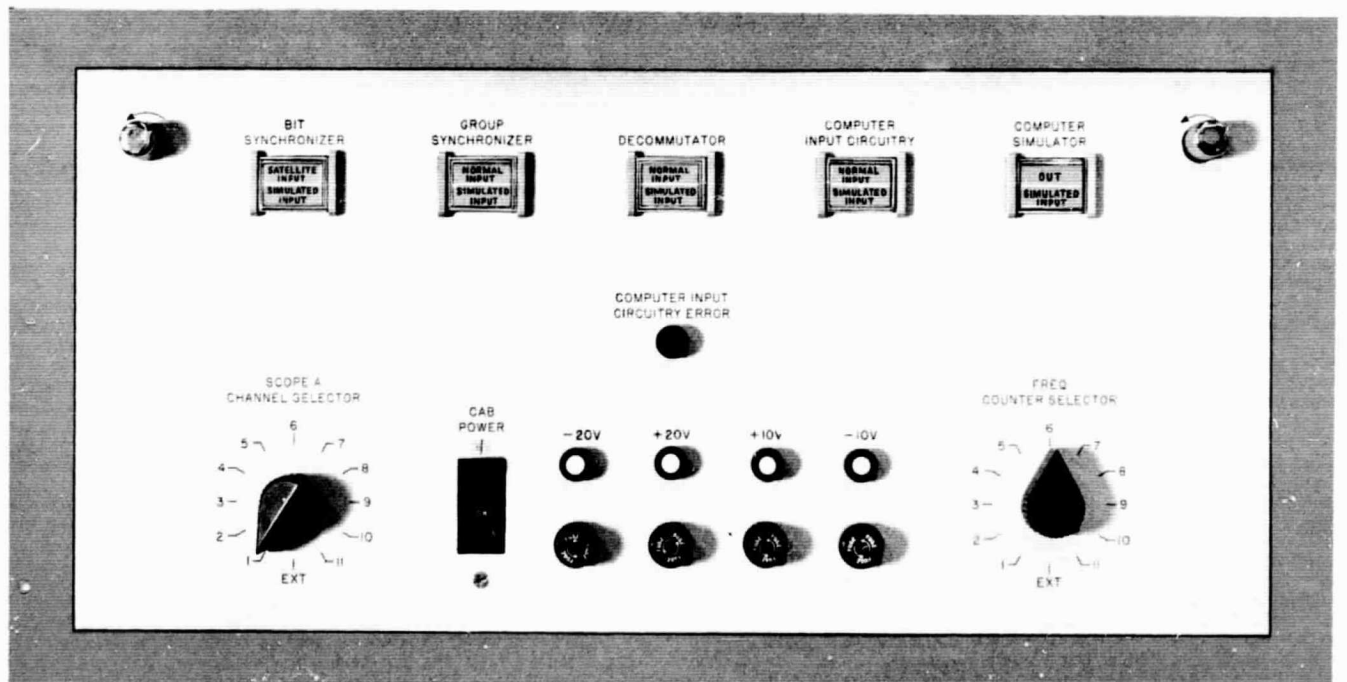
Figure 90. Universal Bit Synchronizer Waveforms

Essentially this makes use of full cycle integration for decisions as to phase polarity of input signal. The bilevel output signal is then routed to data decoder logic converting to NRZC output. The bit location ambiguity (phase determination) of the split phase signal is resolved by correct-phase-detector logic. Integrator "C" and Dump "C" operate over $1/2$ cycle (twice bit rate) intervals, reconstructing a digital version of the input waveforms at the output of Decision amplifier "B" with polarity decisions of each $1/2$ cycle made independently (waveforms S2, T2 and U2). This output is routed to a two-stage shift register where adjacent $1/2$ cycles are compared with phase one timing. If they are of same polarity, an output pulse is generated indicating phase of timing is wrong. The output of the comparator is loaded into a stage shift register where a five out of nine check for errors is made. If a total of five errors ever occurs in the nine stages as each comparison is shifted serially through the register, it is detected by a digital to analog weighting. The level detector logic generates a control signal selecting the other phase of timing and resetting the error check logic. This procedure has good noise immunity in that the wrong phase of timing has high probability of producing a greater rate of errors with average data than that produced by random noise in usable signal levels.

1.21 SIMULATOR MODIFICATION. - (See figures 91 and 92.) The use of the new format data will require changes to the Ground Station Simulator Assembly to enable its use in system



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1416-231B

Figure 91. Nimbus PCM Simulator

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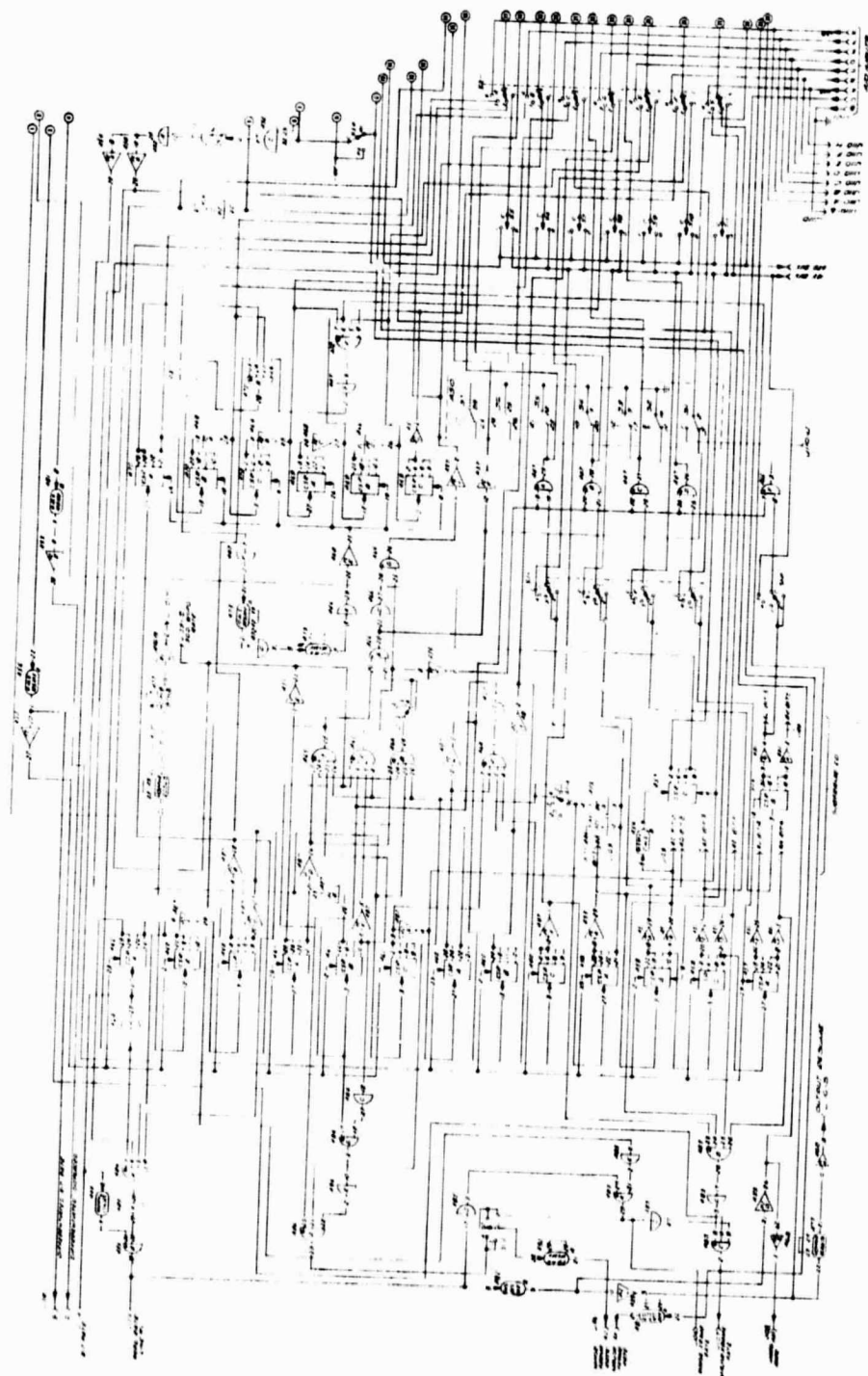


Figure 92. Simulator Logic Diagram (Sheet 1 of 2)

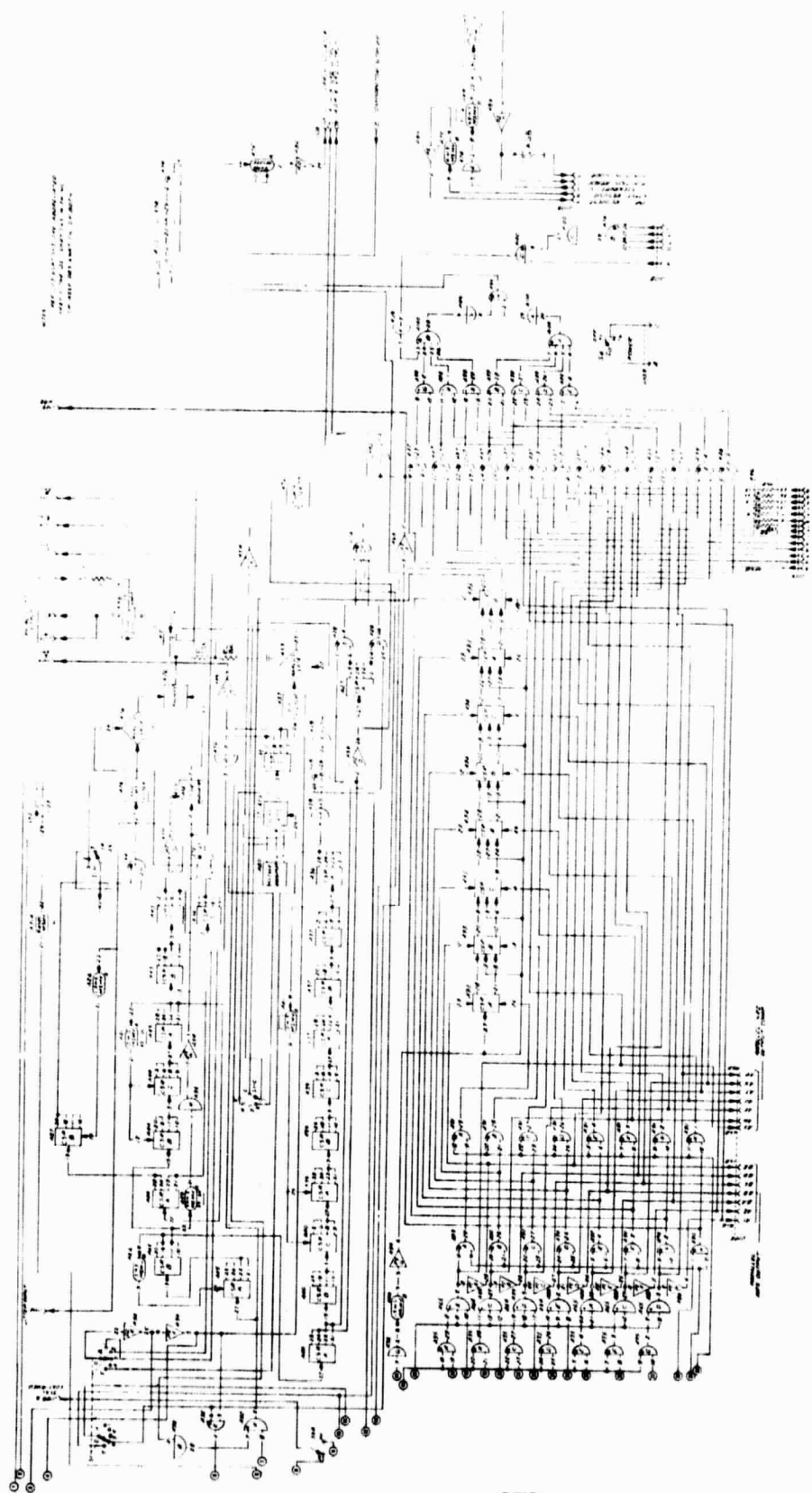


Figure 92. Simulator Logic Diagram (Sheet 2 of 2)

test and checkout. The words-per-frame length must be changed to $62 \frac{1}{2}$ words (500 bits). The frame sync code word length must be changed to 16 bits and either selectable or fixed to final choice of modified Barker code pattern. The additional capability of the new format containing digital channels and time code require further provisions in the Simulator to check the system processing of this data. A Time Code generator should be added and a method of controlling individual bits in any of the digital channels separate from the analog channels. The use of split phase signal modulation in place of the gated sine wave requires logic changes to furnish phase reversals of square wave bit rate for "0" bit indications.

1.21.1 Details of the modifications to the Simulator are shown in figure 93. Group A logic changes indicate a method enabling the bit counter to count four bits ($\frac{1}{2}$ word) for the first word count by bypassing the third stage of the bit counter. After the first word, the bit counter counts normal eight bits per word. Group B logic changes show reset routing required so that word counter is reset to a one count immediately after the 64 count, thereby maintaining a symmetrical serial count for 63 word counts. Thus, on "Normal Count" selection of "Data Contents" the word counter supplies a serial-advancing count with no interruptions (unsymmetrical) in count.

1.21.2 Inserting the correct frame sync bit at the correct time requires changes to the formatting gate circuitry which precedes the output register loading gates. Additionally, the subframe identification (SFID) $\frac{1}{2}$ word must now occur on the third word count. Group C logic changes indicate detailed requirements. A

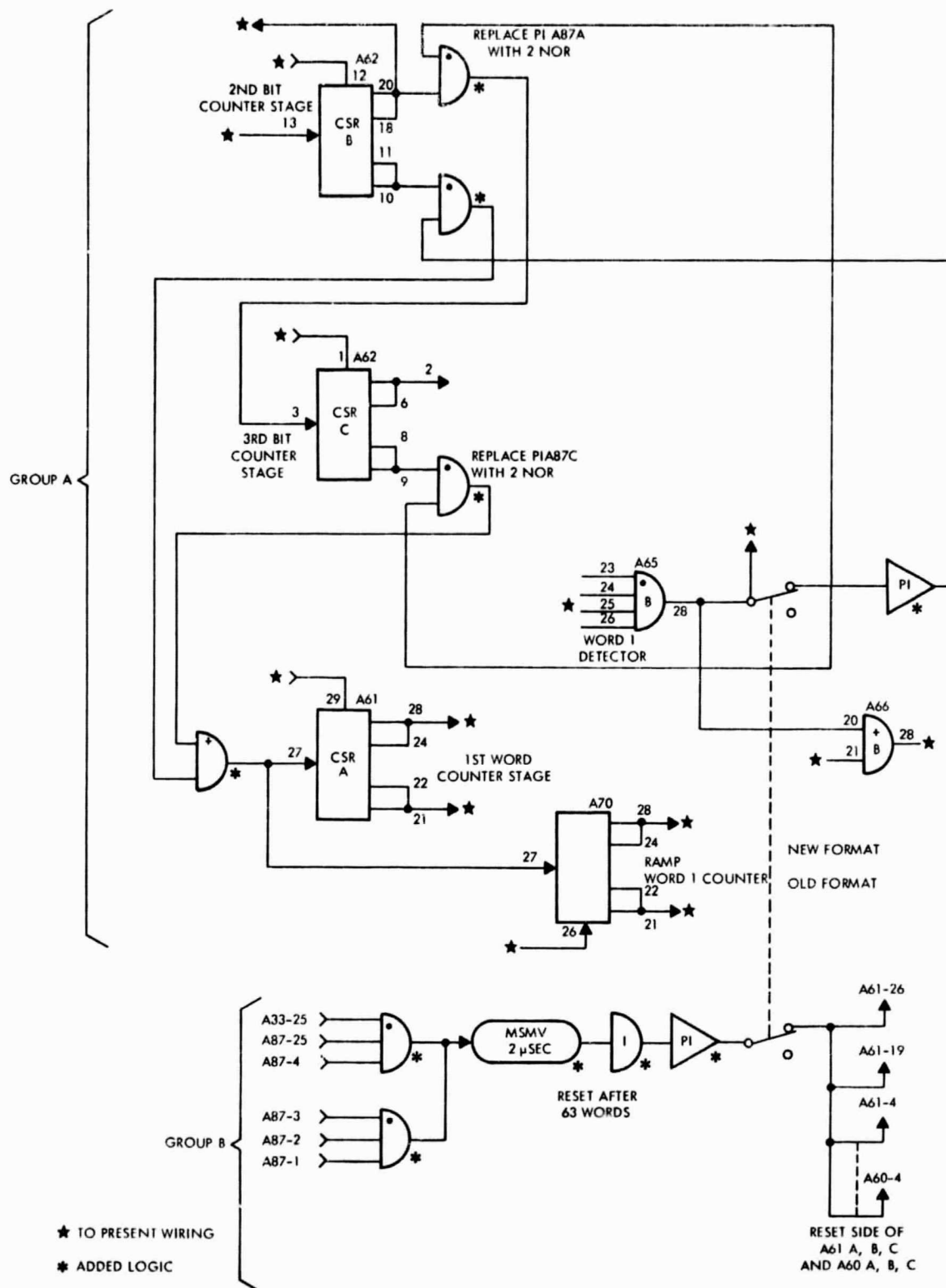


Figure 93. Simulator Logic Changes (Sheet 1 of 3)

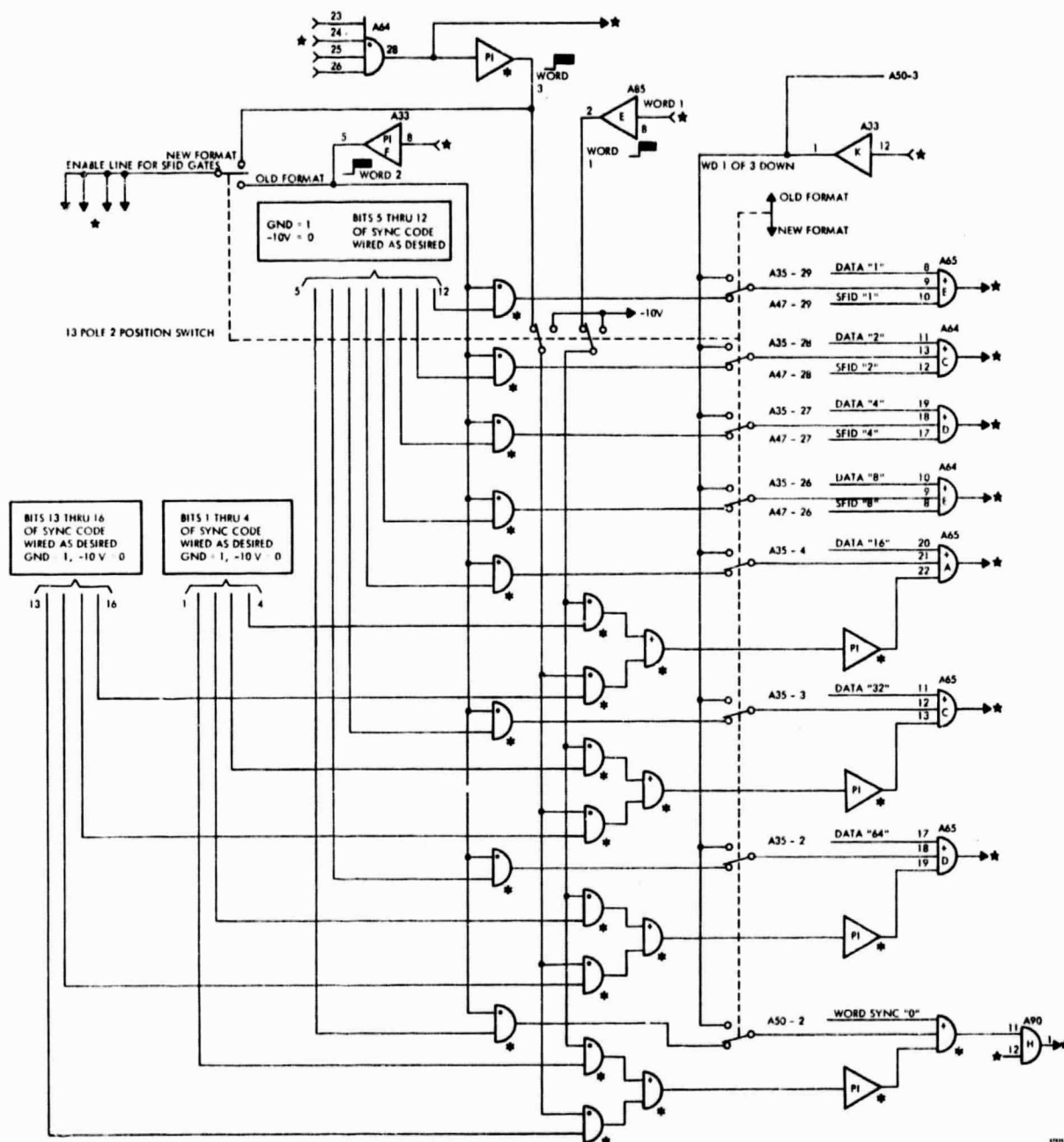


Figure 93. Simulator Logic Changes (Sheet 2 of 3)

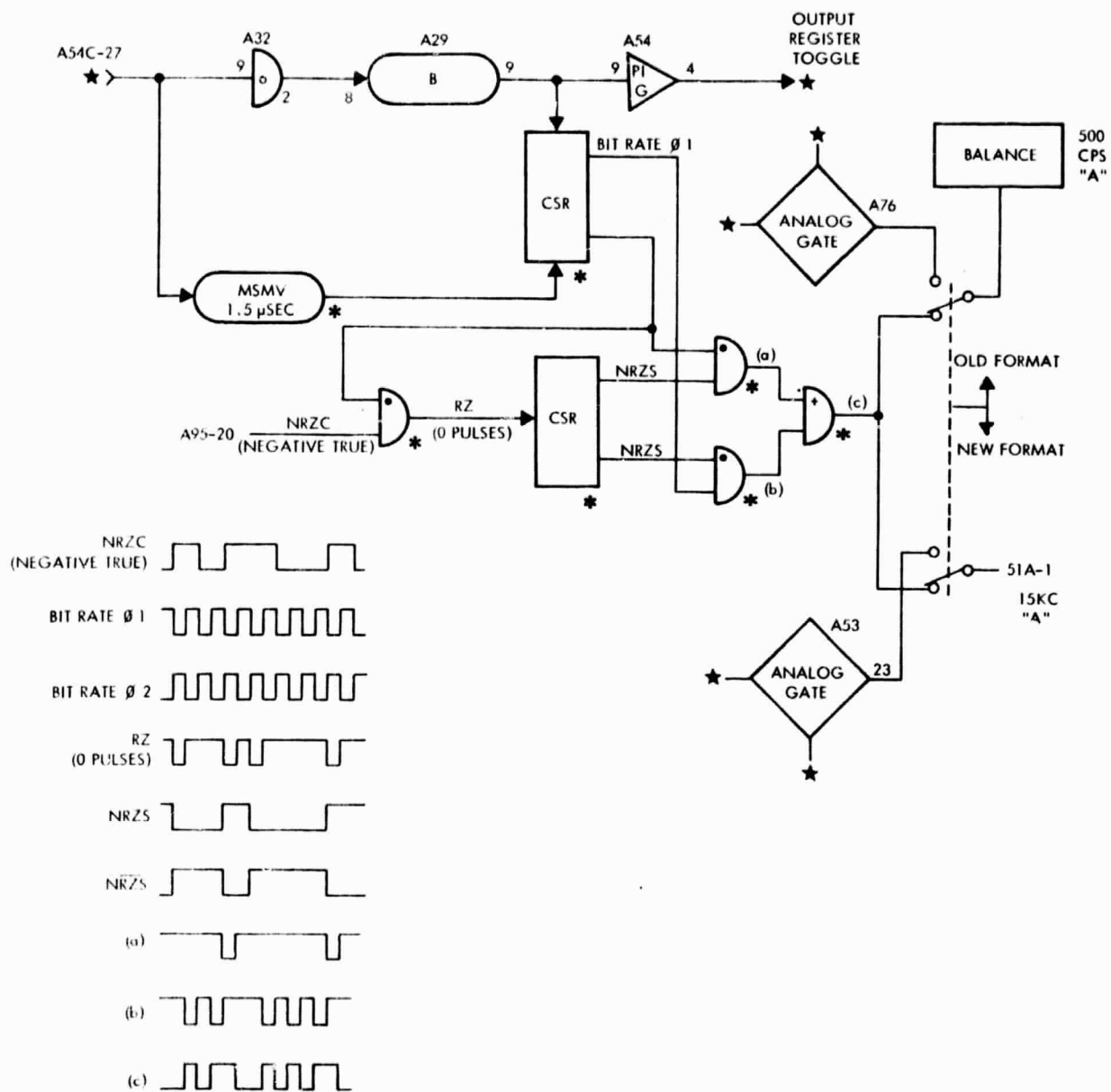


Figure 93. Simulator Logic Changes (Sheet 3 of 3)

fixed frame sync pattern can be wired in as is done in existing system, or the 16 inputs can be wired through 16 SPDT selector switches to ground or -10 volts to select "1"s or "0"s for simulated code pattern. Likewise, a switch is shown (2 position-13 poles) providing the capability to retain existing format or switch to the new format. The new format can be wired in, of course, by merely bypassing and deleting the switches.

- 1.21.3 Group D logic changes and waveforms explain the addition of an NRZ to split phase mark (SPM) converter and necessary switching to provide a SPM modulated video output signal in place of the gated sine wave. The normal NRZC data is sampled by one phase of the clock looking for "0" bit levels. Output of this gate toggles a CSR which selects one phase of the clock in one state and the opposite phase in the other state; thereby reversing phase of output signal each time a "0" bit occurs and no change of phase for "1"s.
- 1.21.4 In order to effectively check out the digital and Time Code channels' decommutation capability in the ground station, it is desirable to be able to place a word in any desired time slot in the PCM A data format while the rest of the time slots contain some different known word. To accomplish this will require an additional five cards in the simulator drawer: two 2 NOR cards and three switch cards. Each switch card would have seven switches. One card would permit bit by bit selection of the content of the unique word. Another switch card would use six switches for word slot selection in the subframe which was to contain the unique word. The last switch card would use four switches to select the subframe

in which the unique word was to appear.

1.22 STUDY PROGRAM FEASIBILITY TESTING CHRONOLOGY. -Certain tests were demonstrated before NASA personnel to prove feasibility. Basically, the output of the airborne NIMBUS PCM Telemetry was recorded on magnetic tape, and these tapes were used as input signals to the modified Ground Station. The ability of the Ground Station to synchronize on this data and decommutate portions of the data for content was observed to verify Airborne PCM correct formatting of all inputs, digital channel and Time Code capability and operating performance characteristics of the Ground Station.

1.22.1 To show feasibility of accepting the new proposed 62-1/2 word format and obtaining the same system performance, the Group Synchronizer and the breadboard simulator were modified. A tape was used which provided gated sine wave signals but with the new format. Tests were then run using the simulator and digital comparator to ascertain that no bit errors were being made and that the system performed normally with the new format. Noise was mixed with the simulated signal and data taken to determine:

- a. that S/N performance was not affected by new format or modifications and
- b. the sync acquisition characteristics with the new format.

Next the tape with the new format but the existing type signal (gated sine wave) was played into the system. Satisfactory handling of this data was noted by normal synchronization indication by the Group Synchronizer. A further check was made by decommutation of most of the data by patching in a glow-tube light display to the outputs of the Ground Station's D/A staticising registers. This

also verified that data on the airborne prepared tape was in the correct format, time slots, and Time Code values for synchronization with the system clock. Time Code readout advanced 16 seconds per each sample. The samples were taken once per major frame. At a bit rate of 500 cps and a subframe length of $62\frac{1}{2}$ eight-bit words for a total 500 bits, subframe rate occurs at 1 cps and, with 16 subframes per major frame, gives major frame repetition every 16 seconds. The use of split phase modulation affected both the control section (recognition of signal to fire squelches) and the Bit Synchronizer. The squelch operation was forced by manual switching. The fact was recognized that analog circuit design must be done on this section to optimize it for the new square wave split phase signal, but this problem was deemed irrelevant for the feasibility demonstration. The requirements necessary for bits decisions were quite extensive if the total logic of the Radiation Universal Bit Synchronizer were employed. Other incompatibilities made direct use of existing logic packages impractical. However, from this viewpoint it was decided that the Universal Bit Synchronizer would be used to demonstrate the practicality and performance gain (S/N) of the use of the split phase signal over the gated sine wave. And at the same time, breadboard work done on a simplified approach that could possibly be added to the NIMBUS Bit Synchronizer was displayed. The demonstrations were divided into two periods. The test set-up was observed (figure 94) and the signal routing explained to NASA personnel. The breadboard simulator was used to supply signals, and waveforms were observed on an oscilloscope defining the various signals and timing.



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The first demonstration utilized an airborne section-made tape with both real-time "A" and stored "A" data. This tape was played on a system Mincom recorder into the Universal Bit Synchronizer in Radiation's standard Decom station.

The output of the Universal Bit Synchronizer was routed to the NIMBUS Group Synchronizer and indication of "Locked" synchronization noted. The same signal was routed to the breadboard modification to the NIMBUS Bit Synchronizer, and a check made on the system sync-confidence. Some trouble was noted here in that the synchronization was not solid. An investigation revealed large noise spikes and abrupt fluctuation in amplitude of the signal from the Mincom tape playback. The input dynamic range of the Universal Bit Synchronizer is better than 15 to 1 and could handle this signal whereas the breadboard logic was developed to accommodate reasonably constant amplitude signals. Present NIMBUS system operation employs manual gain control and a dynamic input range of around 3 to 1. However, poor tape playback signal was traced to "dirty" tape. The Mincom was cleaned and the tape cleaned by several runs over a soft tissue. The signal was once again satisfactory for system synchronization and was shown. The second demonstration was performed using an airborne section-made tape with a continuous run of real-time "A" (500 cps) data. The slower data rate and continuous run on tape made a decommutation display more practical. The playback signal was routed to the Universal Bit Synchronizer and the Decom station was programmed to decommutate the data. The Time Code channels were observed and the time change at 16-second intervals noted. Then, using the test tape data

content tabulation, each prime digital channel was displayed and the correct seven bits noted. The four subcommutated digital channels were displayed and a digital readout verified. Several of the remaining analog channels were decommutated and binary display checked against the data tabulation. A similar check was also made using Test Tape 2, routing the playback signal through the Universal Bit Synchronizer for serial synchronization and bit decisions. The NRZ output was then routed back to the NIMBUS System to the Group Synchronizer. By patching in a breadboarded glow-tube display several selected digital channels were checked and verified for data content. The Time Code was also decommutated and read out continually. Thus the NIMBUS system was handling the new format satisfactorily and decommutation could be accomplished in a normal operational method. A further variation of this test routed the playback signal through the NIMBUS Bit synchronizer and breadboarded bit decision logic. Satisfactory synchronization and handling of the data was observed. Time Code and two digital channels being decommutated were observed on the glow-tube display. Operation here was limited to the "stored-A" data (15 kc) segments on the tape, since breadboarded bit decision logic was set up for only 15 kc bit rate. The third type of testing demonstrated was the method of determining signal-to-noise performance with simulator-supplied signals to the synchronizers. The reconstructed NRZ output of the synchronizer was compared with the simulator NRZ output in an "Exclusive-OR" bit comparator. The error indication was routed to a lab counter to display number of bit errors per 10-second interval. The number of

errors divided by 1.5×10^5 gave the bit error rate. Noise from the General Radio Noise Generator was passed through a 30 kc low pass filter to define the noise bandwidth. Noise and signal were measured on a Bruel and Kjaer VTVM to determine S/N ratio. See figure 95 for S/N Performance curves of data taken on the gated sine wave signal through the NIMBUS synchronizer compared with the split phase signal through the NIMBUS and also through the Universal Synchronizer. The breadboard split phase approach compared equally with the normal synchronizer handling of the gated sine wave signal. However, using the Universal Bit Synchronizer, S/N performance was obtained very close to the theoretical optimum, or about 4-5 db better than the gated sine wave signal. The demonstration showed actual test setup, and test data readings were taken for several points and compared with data taken on previous tests. One area of frequent misunderstanding in S/N performance tests is the noise bandwidth. In our test, this is clearly defined as twice the bit rate or 30 kc. It was felt this was an appropriate choice because the receiver bandwidth if. was thought to be between 30 kc and 50 kc. The last tests demonstrated the method of obtaining sync acquisition time data. The same test set-up as that used for the S/N performance check was used. The simulator was started and the start signal was routed to gate on a lab counter counting an internal 1 kc clock. A signal from the system Group Synchronizer indicating frame sync "locked" was routed to the lab counter to turn off the count operation. With signals mixed with noise giving 0, 1% and 10% error rates, the time was measured from random start to acquiring "locked"

frame sync. The same test was run for word synchronization. The demonstration of these tests merely showed arrangement used for obtaining this data. See Tables 11, 12 for comparative data for 64 and 62-1/2 word data formats.

1.23 CONCLUSIONS AND RECOMMENDATIONS. -For the Ground to handle the 62-1/2 word format only minor modifications are required. There are no problems in this area. The selection of the frame sync code patterns were checked. Further investigation could insure an optimum pattern. The decommutation of the digital channels and Time Code will require approximately one more drawer assembly of logic and considerable wiring to the patch panel and present system Decommutator assembly. The only concern in this area is the location of the added drawer. The possible locations are:

1. Receiver area in Cabinet 3. The three Lambda Supplies would be raised up, making room above the D-A drawers and opposite the patch panel in Cabinet 4.
2. Teletype Converter Drawer area in Cabinet 3. If the "B" data mode of operation is deleted, this space would be available.
3. Bottom panel area of Cabinet 4. This would require moving the Normal/Simulated input control relay assembly and re-arranging the rear connectors in this area. This would entail considerable wiring rework.
4. External to the present system. The Digital Decom drawer could be housed in another cabinet with its event recorder.

The proposed Brush Recorder Model 14 3615 00 is highly compatible with the present system and will be satisfactory for recording and displaying the digital data and Time Code reference. A visual Time Code display is recommended as being available at only little extra

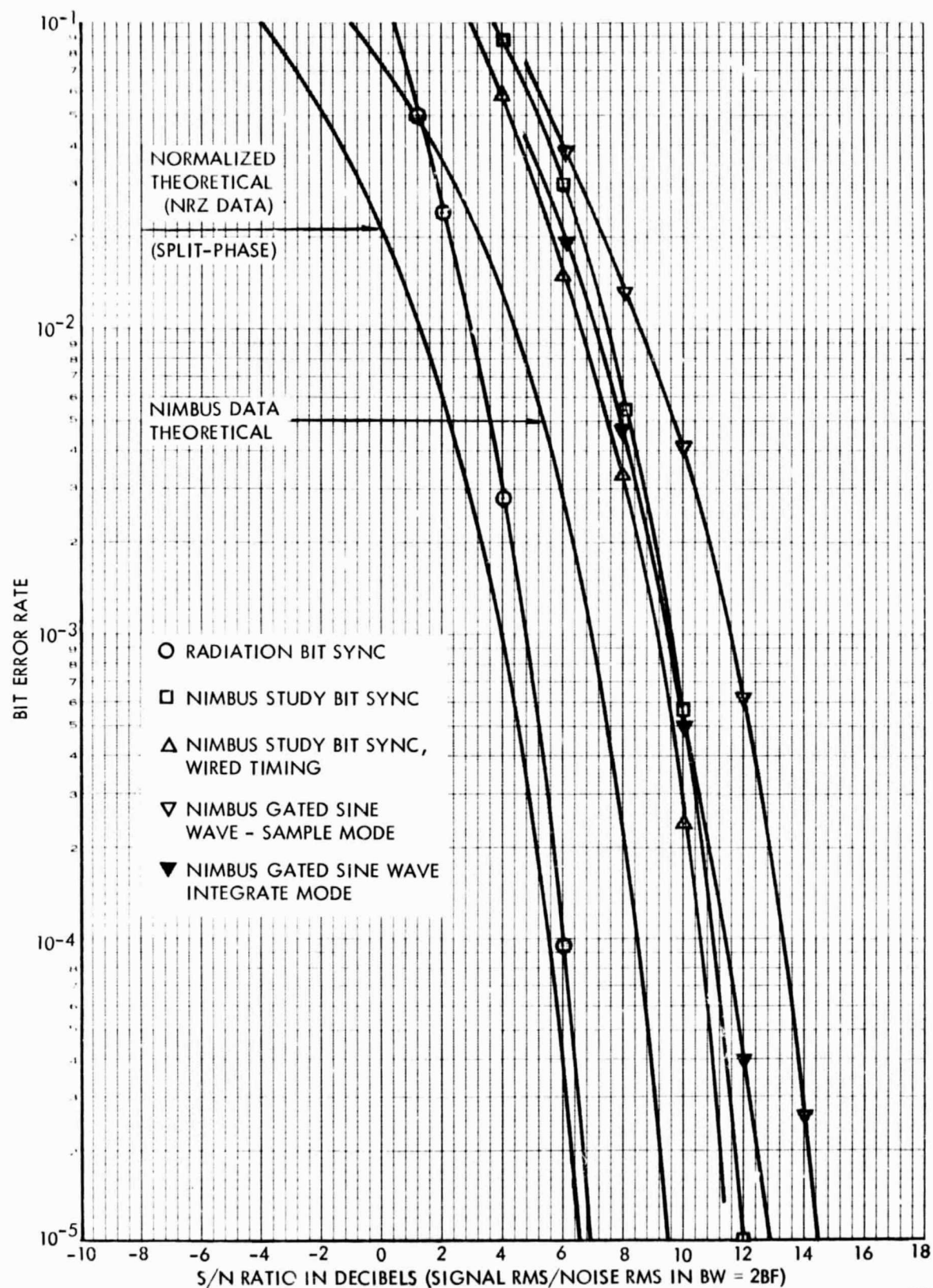


Figure 95. Signal to Noise Performance Comparison Data

but offering considerable operations ease in monitoring Time Code. The use of split phase modulated signal is practical and can be handled in the NIMBUS Ground Station. Modifications must be made to the NIMBUS Bit Synchronizer or it must be replaced with a version of the Radiation Model 4041 Universal Synchronizer. Modification of the NIMBUS Bit Synchronizer is practical. Much of the present logic can be used and, with deletions of some logic not needed, there is available space for the modification. Although time did not allow check of more sophisticated bit decision techniques, the performance obtained with the simplified approach indicated at least 3 to 4 db better S/N performance could be expected over the present system. The Universal Bit Synchronizer actually performed (See figure 95.) very close to theoretical optimum and about 5 db better than the present system. Further investigation should be made into optimum "squellch" operation with the split phase signal.

Table 11. Signal/Noise Performance Comparative Data

Format - New (62-1/2 Word)
 Word Data - Fixed = 01010101 and Random
 Signal - Split Phase Mark From Simulator

S/N RATIO db	WORD RATE	
	FIXED WORD RAD. B.S. - NIMBUS	RANDOM WORD RAD. B.S. - NIMBUS
12.0	- 0	- $7.15 \cdot 10^{-4}$
10.1	- $5.64 \cdot 10^{-4}$	- $1.32 \cdot 10^{-3}$
8.0	- $5.38 \cdot 10^{-3}$	- $7.65 \cdot 10^{-3}$
6.0	$9.3 \cdot 10^{-5}$ - $3.02 \cdot 10^{-2}$	$1.47 \cdot 10^{-4}$ - $3.65 \cdot 10^{-2}$
4.0	$2.8 \cdot 10^{-3}$ - $8.83 \cdot 10^{-2}$	$2.92 \cdot 10^{-3}$ - $9.8 \cdot 10^{-2}$
2.0	$2.42 \cdot 10^{-2}$ - $1.94 \cdot 10^{-1}$	$2.46 \cdot 10^{-2}$ - $2.23 \cdot 10^{-1}$
1.25	$4.94 \cdot 10^{-2}$ -	$5 \cdot 10^{-2}$ -
A check was run on the NIMBUS breadboard using wired timing from the simulator to determine error rate contribution from the NIMBUS synchronizer timing loop.		
S/N RATIO	ERROR RATE	
	FIXED WORD	RANDOM WORD
12 db	0	0
10	$2.37 \cdot 10^{-4}$	$3.0 \cdot 10^{-4}$
8	$3.32 \cdot 10^{-3}$	$3.4 \cdot 10^{-3}$
6	$1.47 \cdot 10^{-2}$	$1.42 \cdot 10^{-2}$
4	$5.82 \cdot 10^{-2}$	$5.7 \cdot 10^{-2}$
2	$1.53 \cdot 10^{-1}$	$1.55 \cdot 10^{-1}$

Table 12. Sync Acquisition Comparative Data

Error Comp. Switch	Error Rate	Frame Sync Acquisition Time	
		64 Word Format Frames	62-1/2 Word Format Frames
High	0%	2.6	2.96
High	1%	3.91	3.68
High	10%	9.83	14.3
Low	0%	1.8	1.72
Low	1%	2.66	2.35
Low	10%	5.56	9.68

SECTION II

NEW TECHNOLOGY

2. NEW TECHNOLOGY.

2.1 GENERAL. - A basic improvement in the analog multiplexer would significantly improve the over-all PCM telemetry subsystem characteristics since the multiplexer contains well over two thirds the system circuitry.

2.2 REQUIREMENT FOR STUDY. -The analog multiplexer basically consists of a memory gate circuit (ferrite core transformer and a matched transistor pair) which is repeated for each of the 667 analog input lines and a large number of similar transformer row and column transformer drivers. Repetitive circuitry will generally best lend itself to replacement by integrated circuitry since only a few basic circuit types must be developed. Therefore, if the multiplexer circuits can be redesigned utilizing circuits adaptable to microelectronic integrated circuit techniques, a significant improvement may be possible at reasonable cost.

2.3 STUDY OBJECTIVES. - This study was made to determine a feasible method for redesigning the analog multiplexer utilizing microelectronic circuits, and to develop the necessary integrated circuits sufficiently to prove their performance. A new type of analog gate should be considered since the conventional matched chopper transistor pairs or integrated chopper transistors both require a transformer drive circuit. The transformer precludes the efficient use of integrated circuits due to its large physical size and multi-interconnections. Also, it is considered that the reliability of a silicon integrated circuit is inherently greater than a multi-winding transformer. Radiation is presently designing a complete typical PCM system entirely utilizing microelectronic circuits. Since the analog multiplexer requirements

are in many ways similar, considerable advantage may be made of the work being done by this Radiation Technical Advancement Program.

2.4 NEW DESIGN REQUIREMENTS. - For a new design to be of significant improvement to warrant rebuilding the present magnetic shift register driven multiplexer it is considered that the following requirements should be met. By meeting the requirements of requirement f. below, future integrated circuit analog multiplexers will be able to take advantage of experience and data which would be obtained from the redesign of the Nimbus Analog Multiplexer.

- a. High usage of integrated circuits
- b. Large resulting decrease in physical size
- c. Small, if any, additional increase in power consumption
- d. Reliability improvement by decrease in number of high failure rate type components
- e. Negligible reduction, if any, in multiplexer and system performance
- f. Maximize the following desirable characteristics for future systems: High isolation (low feedback current), low offset voltage, high voltage breakdown (allows wide range of input voltages), low power consumption, and low capacitance to fixed potentials as well as low input to output capacitance to minimize crosstalk.

2.5 ANALOG GATE. - Isolation requirements for any practical gating device from the fixed system voltages must be as high as possible otherwise the gating device will allow a current to flow from the fixed voltages to the varying analog input. This causes a voltage offset in the transducer source impedance. Practical low-level multiplexing systems require that this current be in the nanoampere range. If the use of a transformer isolated drive circuit is precluded, another isolated gating device must be found.

2.6 NEW DEVICES FOR ANALOG GATES. -A study of other devices has resulted in the following being considered:

- a. Optoelectronic Integrated Chopper Transistor (such as Texas Instrument type PEX 3002)
- b. Diffused N or P Channel Unipolar Field Effect Transistor (such as Siliconix type U 137)
- c. Diffused N or P Channel Metal Oxide Semiconductor Field Effect Transistor (MOSFET) (such as General Micro-Electronics type X-1004)

2.6.1 Optoelectronic Integrated Chopper Transistor. - The optoelectronic integrated

chopper, (figure 96) is basically a conventional integrated chopper transistor which is saturated by the optoelectronic coupling of an adjacent gallium arsenide diode. Ideally optical coupling should provide extremely high isolation. The optoelectronic integrated chopper would meet the analog electrical requirements for the Nimbus Analog Multiplexer but is considered undesirable because of the current drive requirements to the gallium arsenide diode. One hundred milliamperes drive current is specified. Such a large drive current would impose a severe maximum collector resistance requirement on the digital drive circuit transistor which is not readily available with present diffused integrated circuit techniques. (Low resistance collector connection to transistor substrate is not available due to component isolation requirements in integrated circuits.) Also, it is generally desirable to keep the drive current requirements low to minimize power consumption. Another severe limitation is the complicated physical construction which precludes the use of only conventional all diffused integrated circuits. Furthermore, the analog electrical specifications severely limit the use of this device for future systems; since breakdown voltages are only $\pm 5V$, operation is only possible to 10 kc, and capacitance is relatively high.

2.6.2 Unipolar Field Effect Transistor. - A P channel diffused unipolar FET is shown in

figure 97. With no control or gate voltage applied, the source to gate is connected by the equivalent of a silicon resistor formed by the channel. When a back bias is applied to the gate, the increasing depletion layer in the vicinity of the P N junction is designed to effectively open the source to drain conducting path. Good leakage isolation is obtained since the feedback current is limited to the back biased junction leakage. Offset must be zero since no junction is crossed. Typical ON resistances in the 200 ohm range may be obtained with capacitances comparable to the integrated chopper transistors. A primary disadvantage is that a back bias voltage is required to prevent source to drain path from conducting. Thus, whenever the system power is removed, all the input channels will be shorted together. This normally shorted channel characteristic is considered serious enough to rule out the use of conventional FET for most multiplexing applications although many of their other characteristics are desirable. A stopgap solution would be to provide a battery in the equipment to provide a back bias to keep the channels open when power is removed but its physical size would diminish the value of integrated circuit packaging and it would eventually discharge. The fact that the circuit connection between the FET gate and the digital drive circuit is not simple or straightforward is another disadvantage of the conventional FET. This complexity is due to the fact that the P N junction must be forward biased to allow a FET to conduct, but only a few nanoamperes of forward current should flow to minimize feedback current once the FET junction has started conducting. This problem is easily overcome in the MOSFET, (next paragraph), by insulating the control terminal.

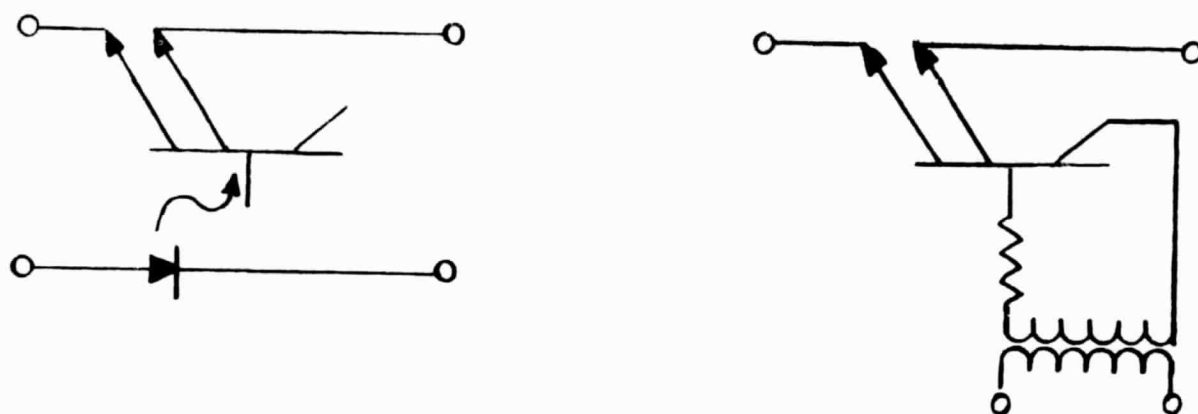
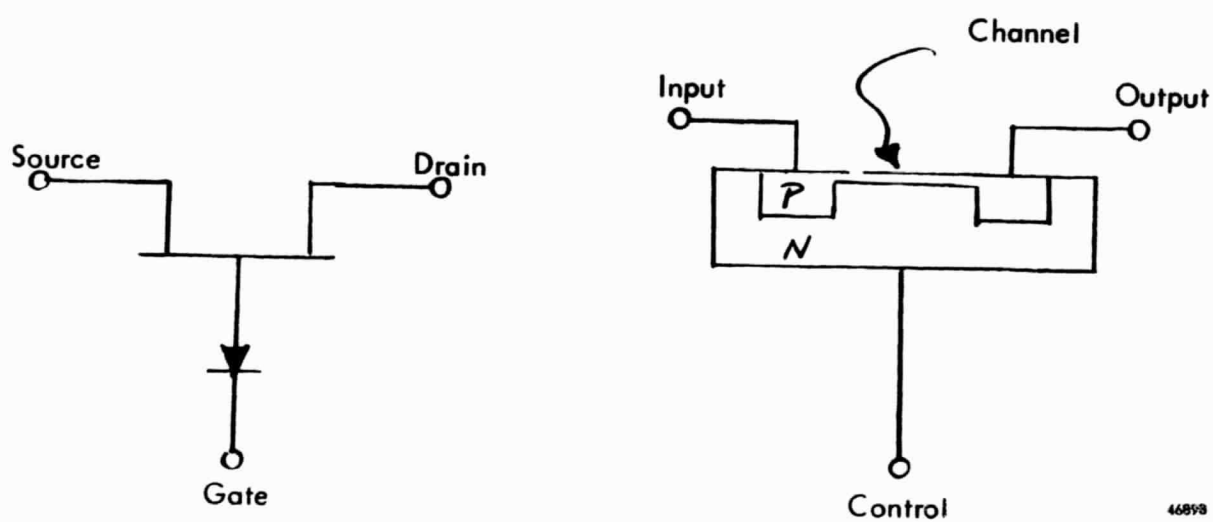


Figure 96. Optoelectronic and Conventional Dual Emitter Chopper Transistors



P Channel Unipolar Field Effect Transistor

Figure 97. P Channel Unipolar Field Effect Transistor (FET)

2.6.3 Metal Oxide Semiconductor Field Effect Transistor. - A MOSFET is shown in figure 98.

To obtain source to drain conduction, a negative voltage is applied to the metallic gate which directs the resulting field through the oxide insulation to the N substrate, thereby attracting holes to the semiconductor surface under the gate. The net result is a conducting path being formed between the source and drain "P" diffused areas. When the negative gate voltage is removed, the "P" channel disappears and the source and drain junctions are back biased by the more positive body voltage. Absolute isolation is assured for the gate terminal and the always back biased source and drain junction leakages can be kept in the nanoampere range. The resulting drive circuits are simple since the isolated gate need only be voltage switched for the ON and OFF conditions. Therefore, drive currents are minimal and power consumption is low. The offset of the MOSFET is zero. Present junction breakdown voltages of 25V are possible with increases anticipated, thus allowing a future wide range of input voltages. Capacitance to ground is comparable to the integrated chopper, and crosstalk is minimized since the source to drain capacity is less than 1 picofarad. Gate ON resistance is less than 500 ohms and could be decreased at the expense of more capacitance to ground.

2.7 SELECTION OF MOSFET FOR ANALOG GATE.- The general gating requirements for future systems as well as all the Nimbus analog signal input specifications can be met with the MOSFET. Significant advantages over the conventional FET is the simplicity of drive circuitry and the open circuit feature of all gates when system power is turned off. The basic advantage of the MOSFET over the transformer driven matched chopper transistor gate is the

elimination of the bulky, relatively unreliable transformers. Not only are most parameters of the MOSFET superior to those of the optoelectronic chopper, but future development will probably favor the MOSFET. Another advantage over the optoelectronic chopper is simplicity of drive circuits and physical construction. Since the MOSFET can be built by similar planar techniques used for normal transistor integrated circuits a complete micro-electronic analog commutator is possible.

2.7.1 Analog Gate Drive Requirements. - A basic MOSFET drive circuit is shown in

figure 99. Since the input signal voltage range is always less than zero (0 to -6.4V) the source to body junction will remain back biased if the body is returned to ground. Similarly the drain to body junction is reverse biased. The P channel MOSFET will remain OFF as long as the insulated control gate potential is equal to or greater than the source or drain voltage. At this time, the only conduction will be the body junction leakage currents to ground. The control gate is, therefore, returned to ground through a resistor, to assure it is normally OFF. If the NPN transistor is saturated, the analog gate will conduct. The -24V power input line is a convenient voltage to bias the control gate for conduction. The minimum gate to source voltage during conduction will then be $24 - 6.4 \approx 17\text{V}$ which is more than sufficient to form a conducting channel from source to drain. When the NPN transistor stops conduction, the control gate will recharge to ground and the analog input gate will be effectively open. An inherent immunity to cracking (temporary closing) of the analog gate due to system noise is provided since the control gate requires at least a two volt threshold to the source before any source to drain conduction is started.

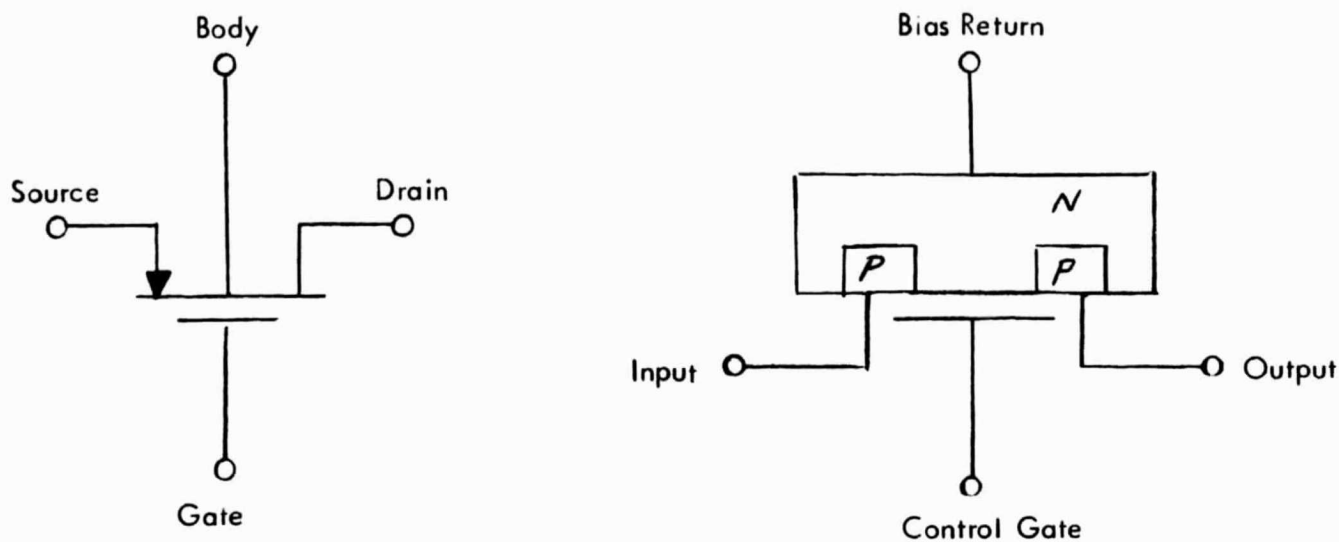


Figure 98. P Channel Metal Oxide Semiconductor Field Effect Transistor

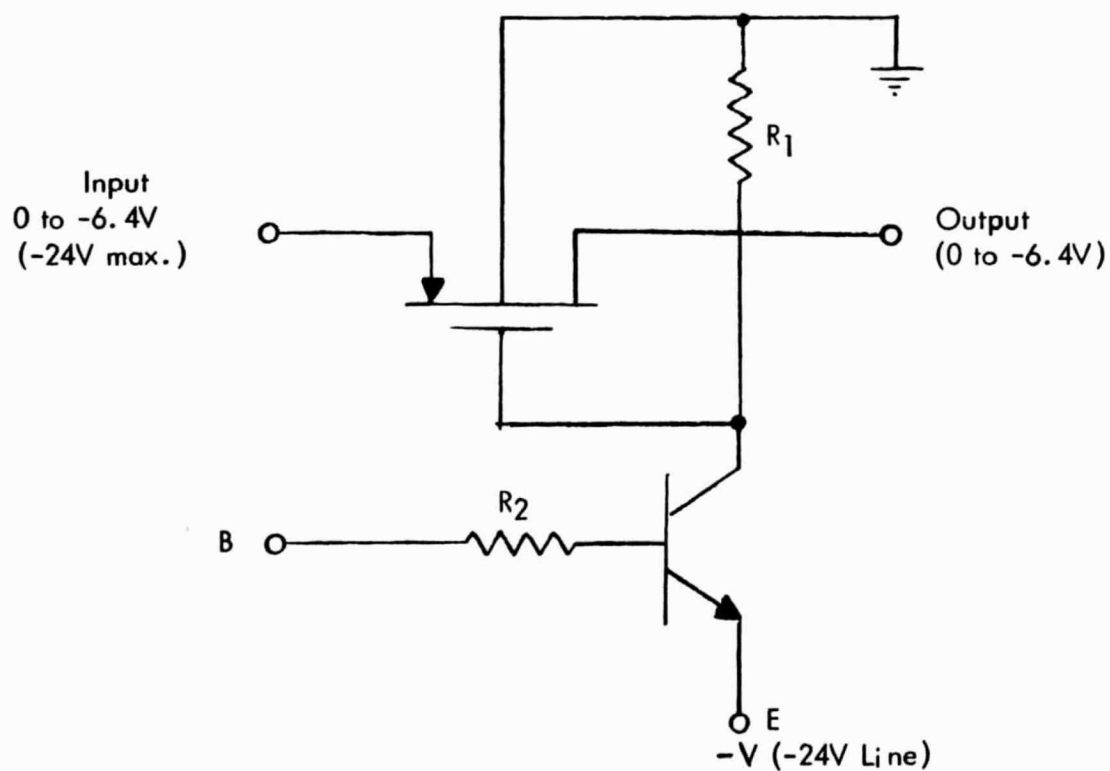
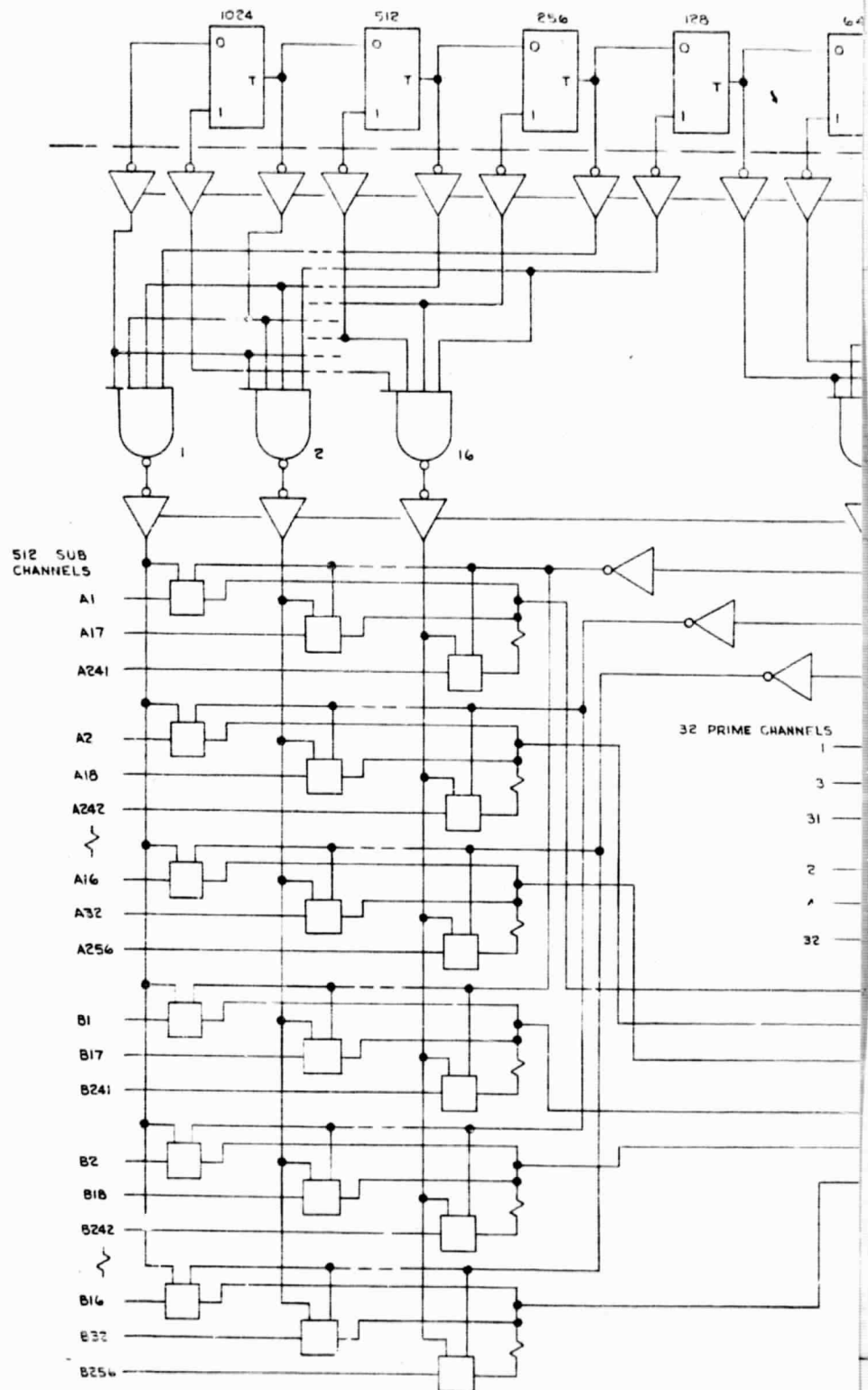


Figure 99. Basic MOSFET Drive Circuit

Protection against overvoltage negative input signals is provided by the MOSFET gates since the basic body junctions are capable of withstanding 24 volts without breakdown, damage, or excessive leakage. Thus, protection is assured for any analog input voltage from ground to the negative supply voltage. With a small modification in the buffer amplifier, the system would now be able to withstand these overvoltages without damage. The MOSFET transistor can be operated with the source and drain interchanged. The drain is connected to the analog gate output, rather than the input, to reduce feedback current and line capacity; since the drain body junction is constructed physically smaller than the source body junction. Low leakage and capacitance is most important at the drain or analog gate output because any analog signal path is connected to many more analog gate outputs than inputs. This is a result of the physically tiering or grouping of the analog switches. The turn on and turn off transient current in the input and output lines caused by the source and drain capacity to the control gate should not be overlooked. For a 25 volt switching gate transient and 10 pf capacity, 250 pico coulombs must be supplied from the analog signal source for each series conducting MOSFET in the single path. The simple solution is to allow sufficient settling time before starting the coding process. Presently this time is provided by a 110 usec delay in the coder. Thus, for an eleven time constant settling time a maximum 10 usec RC time constant could be allowed. For a maximum 3K source impedance, approximately 3,000 pf capacity would be allowable at the analog input. Another possibility is to provide a sufficiently large parallel capacitor at the analog source such that the transferred charge and leakage

currents have negligible effect on the input voltage during the sample period. Detailed information on MOSFET specifications are included in Appendix V.

2.7.2 Prevention of System Catastrophic Failure. - Since the system contains a large number of analog gates considerable over-all reliability advantage can be obtained by isolating failures to a small number of gates. MOSFET failures are basically isolated by tiering 16 or less analog inputs (figure 100). The effect of failures in any of the input MOSFET gates either disables the individual gate or all in a tiered group. The following failures will only cause the loss of a single input: Short circuit S-B, G-B; open circuit S, D. A tier of gates will fail if: Short circuit S-D, B-D, S-G, G-D; open G. All gates outside of a tier are protected, since any gate can withstand the full negative supply voltage. Often the output of a tier of input gates is connected to the input of another tier (figure 101). This second tier is often referred to as sequencer gates. The effect of failures in such a tier of sequencer gates is similar to that in the tier of input gates except a failure causes the loss of all the channels in an input tier or all the channels in the sequencer tier, which may be an undesirable large number of channels. The probability of this second undesirable failure may be reduced by only driving an input gate when its sequencer is driven. Then a shorted gate in the sequencer will not interfere with the other gates in the sequencer tier. If this drive limitation is used, the only failures in the sequencer gates that can effect more than a single input tier are B-D and G-D shorts. The B-D short failure may be avoided by leaving the body terminal in the sequencer MOSFET gates open. The body connection only served as a bias return and the result of it being open will allow



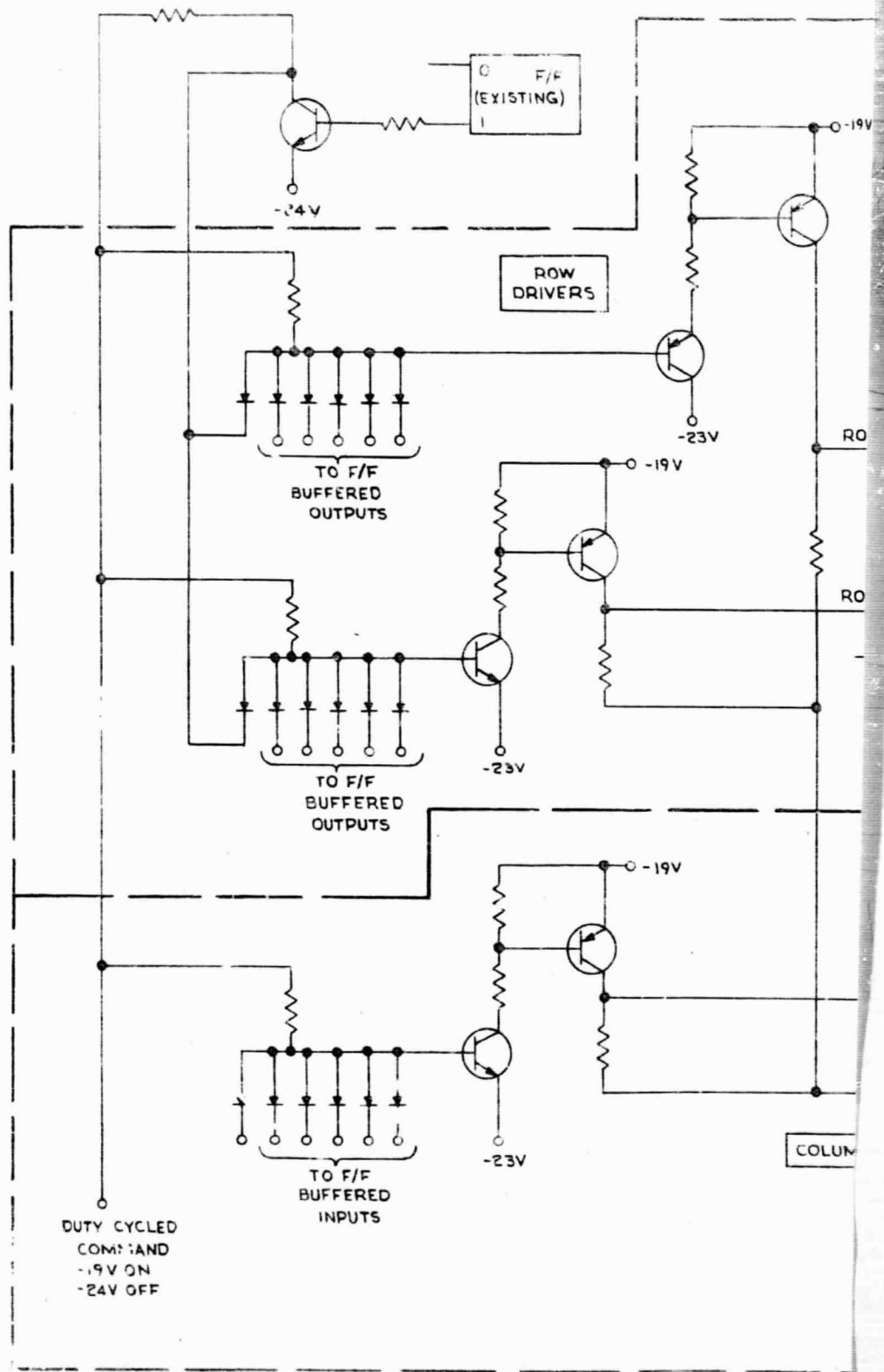
gate junction leakage currents to flow from input to output separately. Thus, the only failure in the sequencers that can cause the loss of more than a single input tier is a gate to drain short.

2.8 MEMORY DRIVE CIRCUITS.—The present analog multiplexer utilizes row and column driven ferrite cores to saturate matched transistor pairs. Since the rows and columns are driven at different rates, the transformer core must serve as a memory. Thus, one driver may reset 16 cores and the set pulse from the other driver type will produce an output only on the core that has been previously reset. The problem then is to provide an equivalent drive circuit that does not require a magnetic core for memory and maintains the low power consumption inherent with the magnetic scheme.

2.8.1 Circuit Approach. — Another source of memory in the present system is the 11 flip-flops in the Unit A sequencer, and 7 flip-flops in the Unit B sequencer which operate at the word rate or slower. Effective use can be made of the flip-flop memory only if it can be directly coupled to the analog gates with a minimum power consumption. Due to the low duty cycle of analog sample time to OFF time, the low average power requirement may be met if leakage currents only are flowing during the OFF intervals. Thus, a scheme which only switches power to a synchronizer flip-flop decoding network during the ON interval may be considered. The MOSFET will be driven by an NPN transistor which serves as an AND gate in a row and column driven matrix. The row and column driver outputs are power switched ON with timing provided by diode AND gates. Both the diode AND gates and their buffered inputs from the synchronizer flip-flops are power switched at the low duty cycle. Thus, the row and column

are now coincident and depend directly on the state of the synchronizer flip-flops. Therefore, memory is no longer required in the gate circuit. Power consumption has been minimized by the low duty cycle power switching.

2.8.2 Circuit Details. - Figure 102 indicates the circuit details for a typical row and column drive matrix. Any desired gate may be driven by selection of its row and column in the matrix. The MOSFET gate (figure 99) is driven by an NPN transistor which performs the function of an AND gate. An output is provided when the emitter is connected to -24V by a column driver saturated NPN transistor and the base is connected to -19V by a row driver saturated PNP transistor. Timing for the row and column drivers is provided by a six input AND gate matrix. This diode matrix is driven by the NPN inverted buffered output of the existing synchronizer flip-flops. Voltage levels are maintained by biasing the six input AND gate NPN emitters a volt above -24V. Positive voltage is switched to the flip-flop buffers and the six input AND gates only during the sample period (less than 1% duty cycle). Thus for more than 99% of the time none of the transistors or diodes in the microelectronic portion of the analog multiplexer are conducting with the exception of leakage currents. During this period, the only power dissipated is in the base circuit of the flip-flop buffers. A simple power supply circuit is shown in figure 103. The -19V is provided by a capacitor which is charged through a series resistor, R1, directly from the input power line. The zener diode regulates the -19V. Two series diodes provide the -23V from the current through R2 and the six input AND gate NPN emitters. Another AND gate provides the -19V switched output during the sample period.



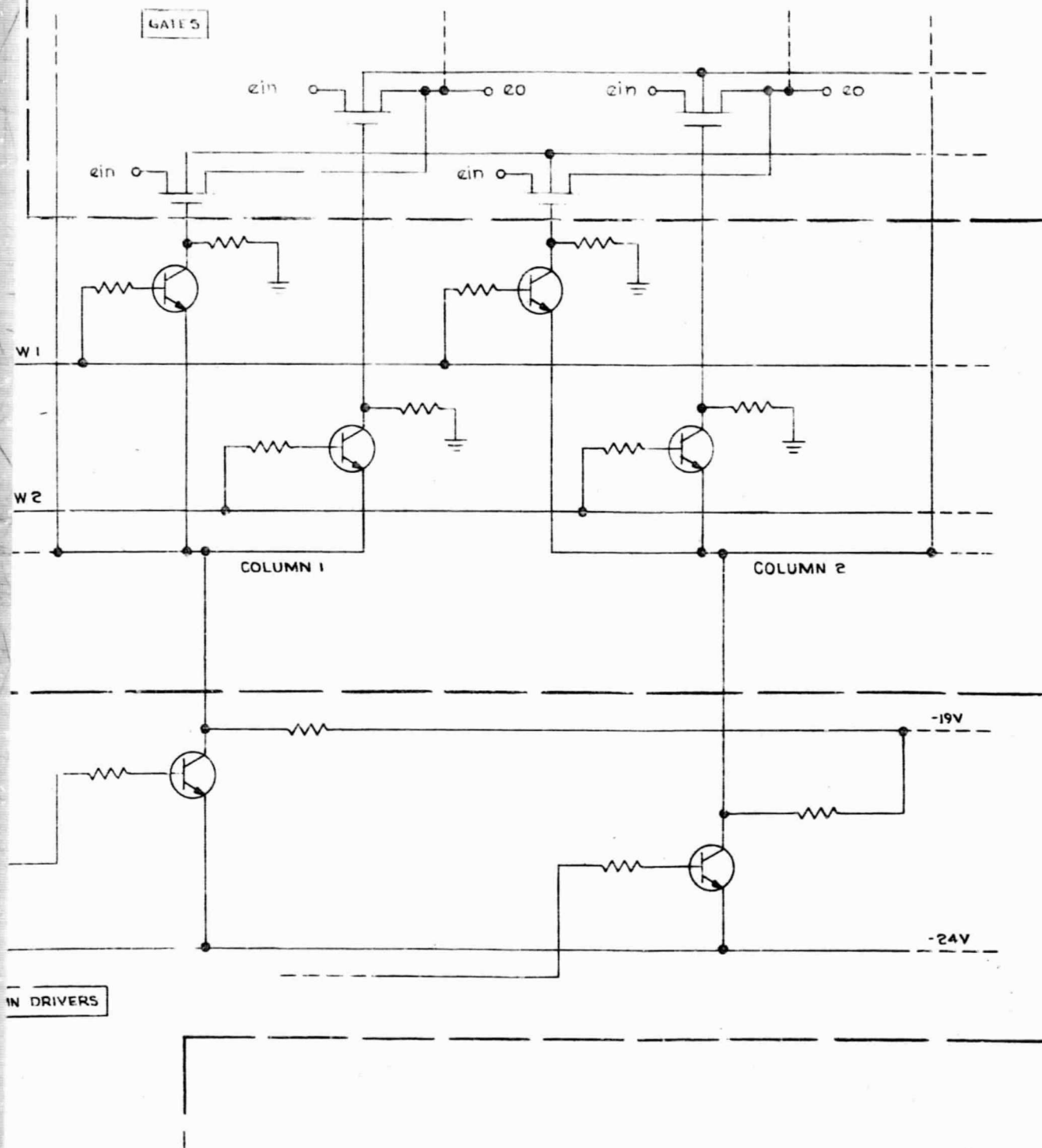


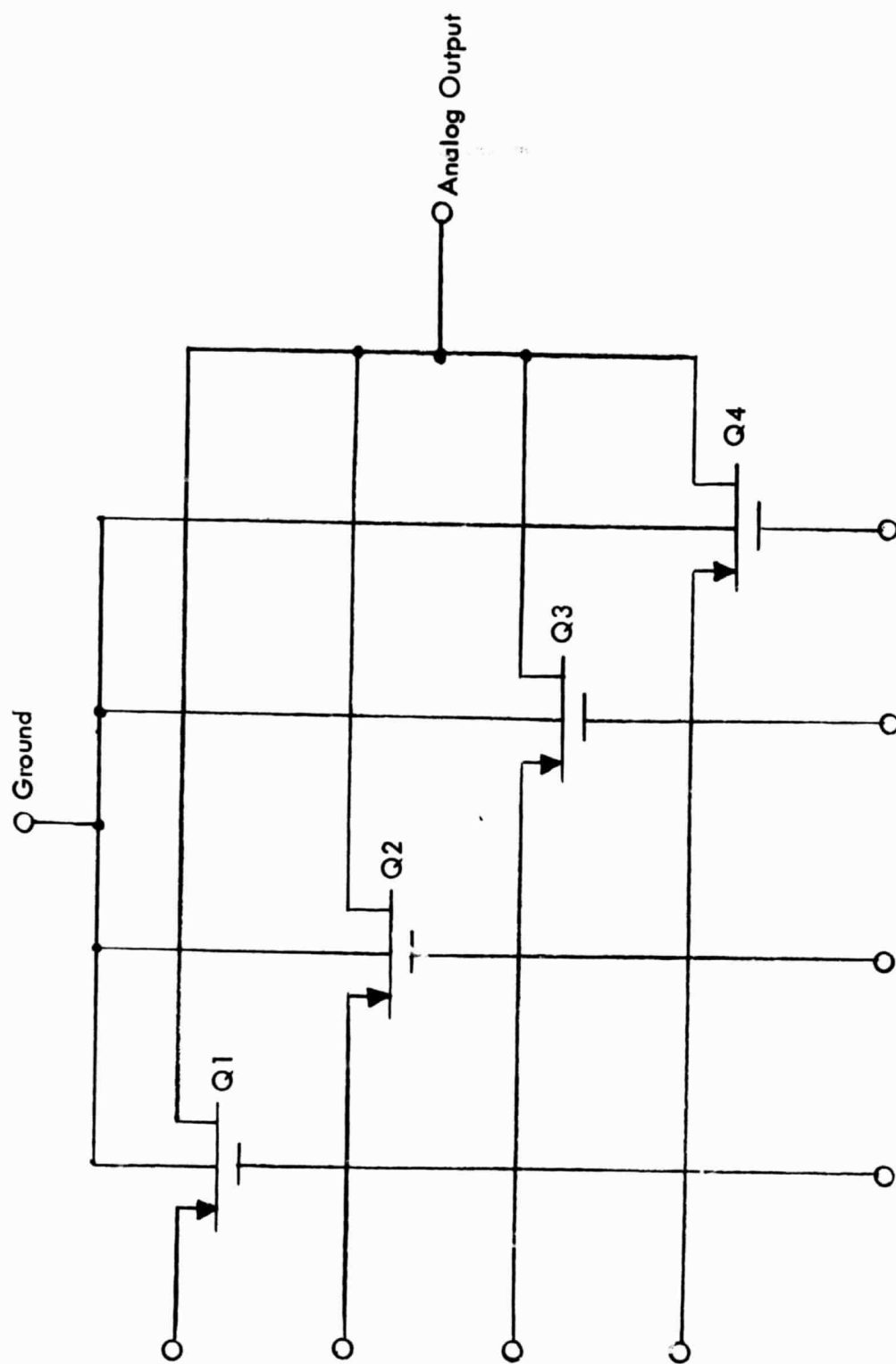
Figure 102. Row and Column Drive Matrix Schematic Diagram

2.8.3 Circuit Interfaces. - All microelectronic portions of the analog multiplexer can be constructed by interconnecting three basic circuits. These three circuits are shown in figures 104, 105, and 106. A comparison to figure 102 indicates how the three basic circuits serve all the functions required in the analog multiplexer. The power supply portion of the analog multiplexer utilizes a standard six input and/nand gate as well as two discrete resistors, two diodes, one zener diode and one capacitor. The total interface to the rest of the PCM telemetry system consist of analog inputs, analog outputs, synchronizer flip-flop outputs, -24V supply and ground, and sample command.

2.9 MULTIPLEXER CONFIGURATION. - The microelectronic analog multiplexer configuration which performs all the functions of the present Unit A multiplexer becomes self-evident with a study of the logic diagram (figure 100) and comparison with the schematic diagram (figure 102). A logic diagram for Unit B multiplexer is obvious.

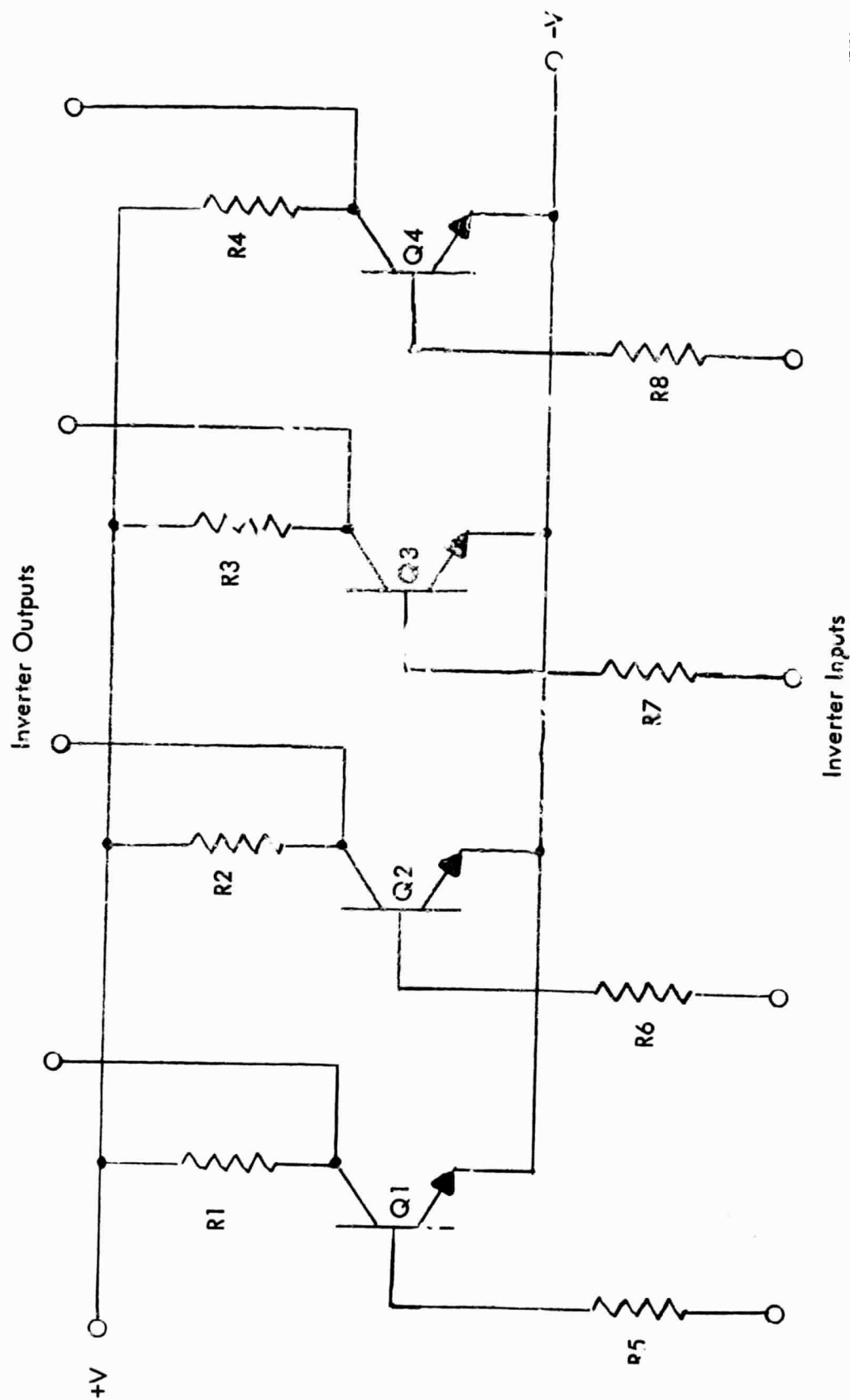
2.9.1 Note that the probability of a failure affecting more than 16 input channels is greatly reduced, since any second tier sequencers for the sub-commutated channels only has an input present when it is sampled. (paragraph 2.7.2).

2.9.2 The total power consumption for the microelectronic Unit A multiplexer is 250 milliwatts. This compares favorably to the present 204 milliwatts power consumption. Most of the above power is required to supply the base drive current to the NPN inverters which buffer the Sequencer Flip-Flop



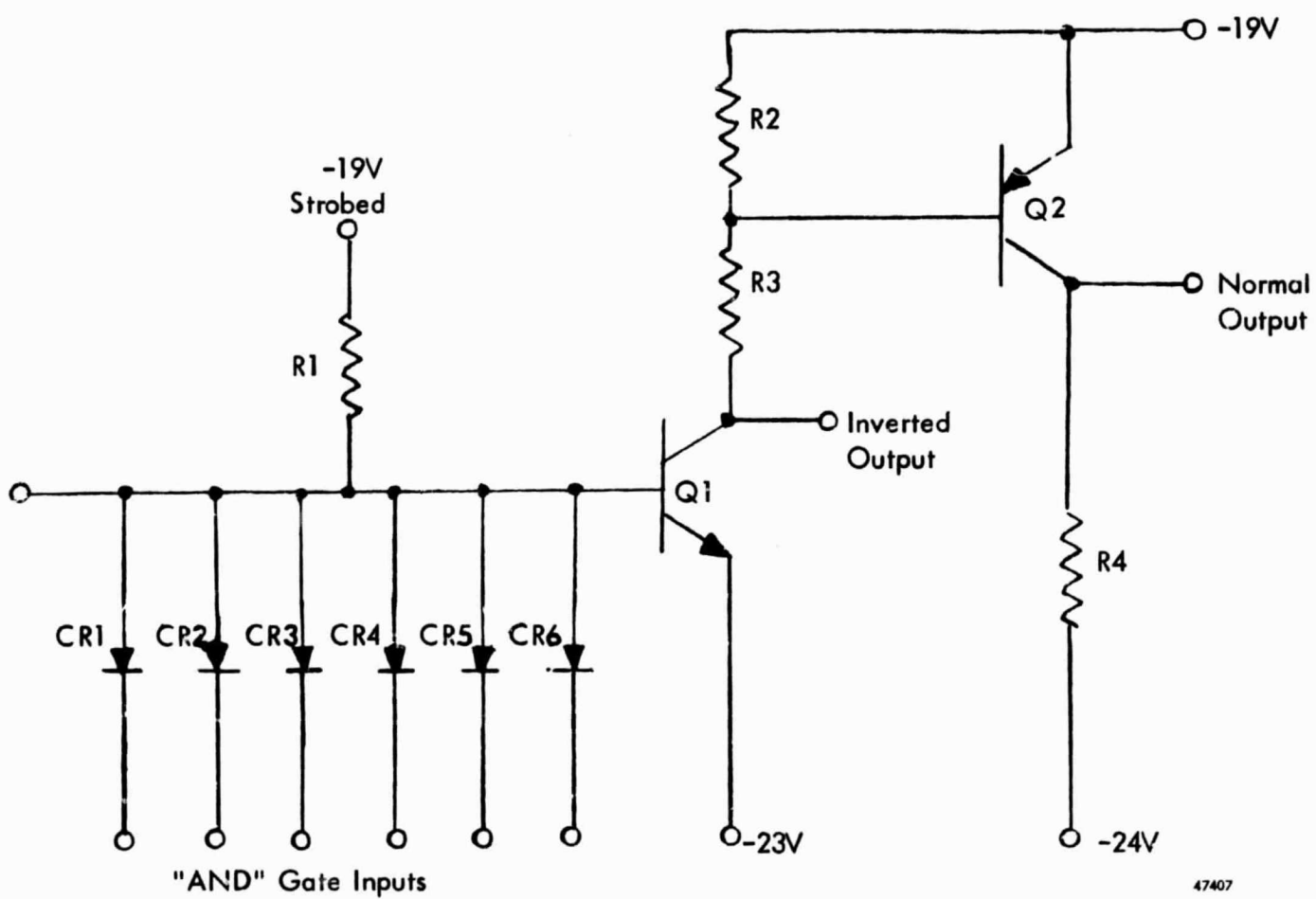
47405

Figure 104. MOSFET Analog Gate



47405

Figure 105. NPN Inverter



47407

Figure 106. Six Input AND/NAND Gate

outputs. Comparison of this microelectronic analog multiplexer design with design requirements indicate that all requirements have been met or exceeded.

2.9.3 During a redesign of the analog multiplexer many format changes could be incorporated. These changes could include the number of prime and sub-commutated channels, the number of time slots (i.e. sampling rate), the ratio of prime to sub-prime sampling rates and additional subcommutation. When considering changes it is desirable to keep a binary relationship for the required number of row or column drivers in any matrix.

2.10 ELECTRICAL TEST RESULTS. - An eight channel MOS Analog Gate circuit was breadboarded and tested from -70 to $+125^{\circ}\text{C}$. The analog gate operated as expected and tradeoffs of power and switching speed were incorporated.

2.10.1 Pairs of MOS analog gates were tested for use in a low-level differential multiplexer. Common mode rejection as well as changes in junction leakage currents are of prime importance in this application. A great advantage of the MOS gate over any other type is the availability of the body terminal to which input and output capacitances and leakages are referenced. By floating all the multiplexer body terminals at the common mode voltage of the sampled transducer a great reduction in apparent capacity and leakage changes can be realized. Thus, much superior common mode rejection and common mode input impedance is possible for differential applications. The differential amplifier provides the unity gain common mode biasing voltage as a by-product of its operation.

2.10.2 After attempting to solder the MOS transistors in the breadboard, a problem soon became apparent. Excessive leakages were found in some units and examination showed cracks in the insulating oxide between the gate and substrate. The cause of this oxide breakdown was excessive voltage applied to this gate. The voltage was applied to the gate by the soldering iron since it was only isolated from the line voltage by 7 megohms. The MOS transistors are specified to withstand $\pm 75V$ transients. Since a picoampere of current is sufficient to crack the oxide any high voltage transient from even a high impedance source can damage the oxide. Therefore, sufficient care in handling and assembly must be taken to assure that overvoltage is not applied to the gate. Once assembled, the gate is connected to the body or ground by the return resistor R_1 shown in figure 99 (typically 30K). Thus, the resistor assures protection from any induced overvoltages.

2.10.3 Eight units were tested by measuring B-S and B-D junction leakages with a back bias of 25 volts. Gate to a common body, source, drain leakage was measured at ± 25 volts. The gate leakage was always less than 1 picoampere. It may be noted that the increase in junction leakage current was almost linear to 10V and then appears to increase roughly exponentially. One transistor was tested for junction breakdown which was approximately 150V. A prime objective of the work Radiation is currently doing on the MOS transistor in the Physical Electronics Division is to decrease the B-S and B-D junction leakages for future critical low-level use. The presently available

units are more than capable of meeting the Nimbus high-level requirements.

2.10.4 The eight measured units were first tested for 72 hours at 25 volts on the junctions with -45V and +25V alternately applied to the gate. The operating temperature range was -70°C to +150°C. Next, the units were tested with zero or 25 volts on the junctions and the following transient gate voltage to simulate operating conditions: Normally +25V with 30 us at -45V, F.T. < 2 usec R.T. < 5 usec at 1 KC. The test was run 48 hours from -70°C to +150°C. All units survived the tests and junction and gate leakages were negligibly changed.

2.11 MECHANICAL CONSIDERATIONS. - The new technology was sufficiently encouraging to warrant an investigation of the present PCM package to determine how it may be improved to take advantage of the size reduction offered by use of the MOSFET integrated circuit analog multiplexer design.

2.11.1 Assumptions. - Several assumptions were made concerning system make-up to provide a base from which to define a new package:

- a. Use of MOSFET analog multiplexer with integrated circuit drivers as detailed in paragraph 2.1 for Unit "A" and Unit "B" multiplexers.
- b. Inclusion of PCM Study System innovations as given in paragraph 1.5.
- c. Microelectronic digital gates.
- d. Redundant coders using discrete components.

2.12 PHYSICAL SIZE REDUCTION. - The resulting investigation revealed that a reduction of 50% in volume, and a weight savings of approximately 45% over that of the present system is possible. To achieve such dramatic savings in an already skillfully designed package requires a relay of the system. A standard Nimbus module of 8X 6X 6 1/2 inches was chosen as the most feasible size package. New cards, modules, and connectors were considered. The packaging changes are detailed in the subsequent paragraphs.

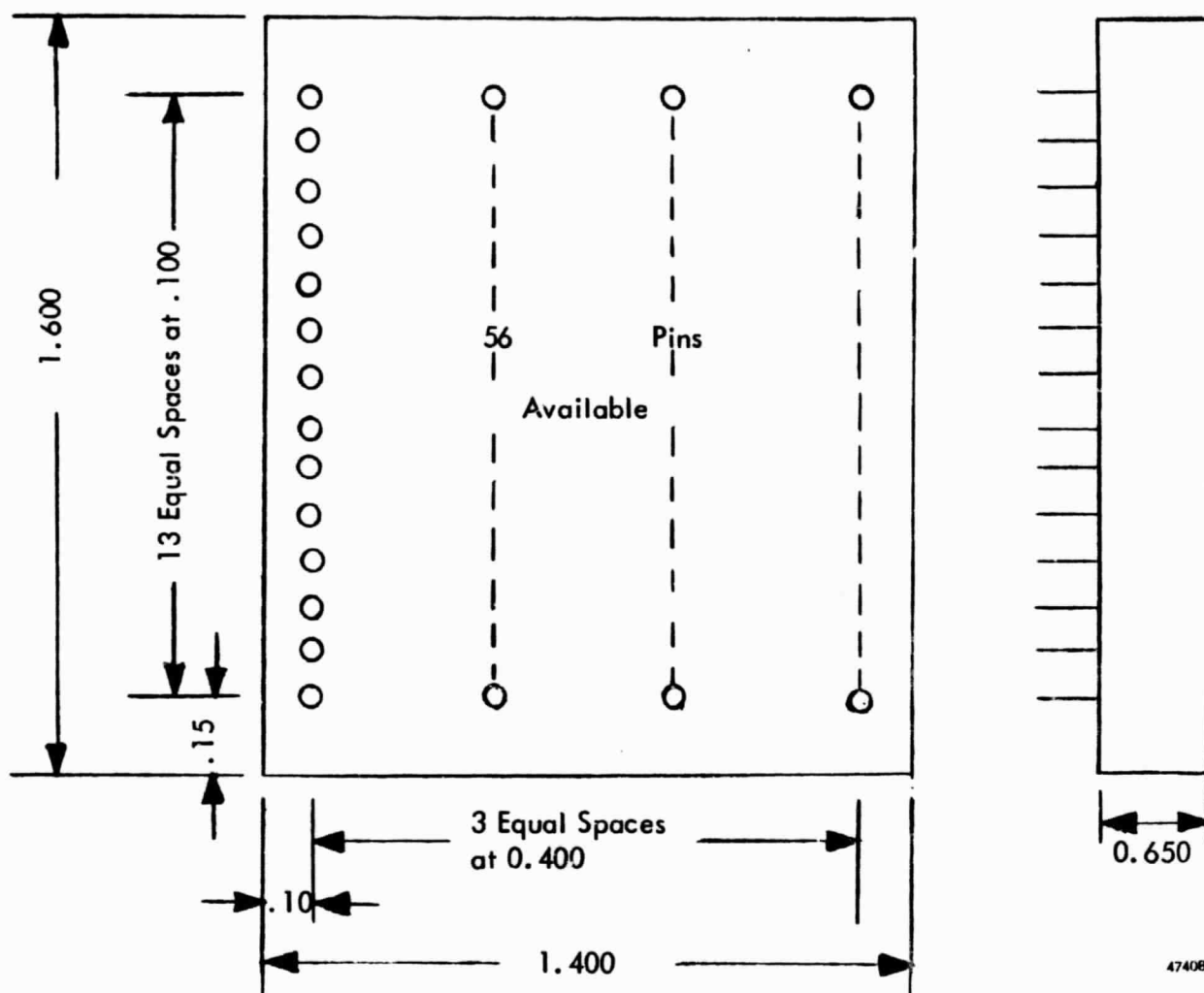
2.13 PACKAGING. - The discrete components will be packaged in welded cordwood modules similar to those used in the present Nimbus system. The integrated circuits, which are to be supplied in flat packages, are to be mounted to small cards (referred to as carrier cards). The carrier cards are epoxy laminate cards with printed circuitry on each side. Their size is approximately 1.50 X .50 X .035 inches. The integrated circuit packages are placed flat against the surface of these cards, and the leads are either welded or soldered directly to the appropriate printed circuitry. Each carrier card in the Digital circuitry portion of the system accommodates two integrated circuit packages, while each carrier card in the Analog circuitry portion of the system accommodates four integrated circuit packages. The reason for the difference is due to the manner in which each must be electrically connected into the system. Interconnection lead wires are attached, and the carrier cards are epoxy coated for protection purposes. The next higher assembly is achieved by positioning four completed carrier cards into a holding fixture so that the cards are

all parallel and equally spaced with each other. Sheets of mylar with welded module wiring patterns printed on them, which have been previously punched for location over the protruding leads, are then made by welding nickel ribbon to them as is done in the standard cordwood modules. Both the cordwood and integrated circuit welded modules are then foamed with urethane rigid foam so that the resulting modules are compatible with the present system packaging concept.

2.13.1 Modules - A typical new module layout is shown in Figure 107. Tables 13, 14, 15 and summarize the utilization of new modules. Modules D1 through D7 in Table 13 replace those modules listed under "Old Module Replaced." Modules D8 through D24 are the new modules required for the digital multiplexer. Table 14 should be self explanatory. Table 15 merely indicates how the present coder modules would be grouped into new modules to save space and lead pins.

Modules requiring relay layout because of redesign, etc. are given in Table 16.

2.13.2 Printed Circuit Cards. - In order to package the system into the smaller Nimbus module size of 8 X 6 X 6 - 1/2 inches, all of the circuit cards would have to be entirely redone. Since this was considered necessary, it was decided to strive for attaining the greatest volume reduction possible. The resulting 50% volume savings is a direct result of the ability to fit the electronics onto 5.75 X 5.25 X .037 inch printed circuit cards. As in the previous systems, the cards are of fiber glass base, epoxy resin, temperature



NOTE:
All Dimensions in Inches.

Figure 107. Typical Microelectronic Module

Table 13 New Module Utilization Summary Digital Circuitry

New Module Designation	Old Replaced	Module Contents	Quantity Per System	Pins Utilized Per Module
D1	C-17	Bias Amp & 3 Core Drivers	1	10
D-2	20	4 Core Drivers	1	11
D-3	C-1	Word Rate Counter	1	Present & 3
D-4	C-2	Word Rate Counter	1	Present & 2
D-5	M-23	8:1 Count Sync		10
	M-24			
D-6	M-25	1/2-65:1 Count Sync	2	11
D-7	M-26	16:1 Count Sync	1	11
D-8		Dig. Mpxr Gates	4	40
D-9		Trans. Data Storage	1	11
D-10		Trans. Data Storage	1	10
D-11		Programmer	1	18
D-12		Programme	1	20
D-13		Programmer	1	19
D-14		Programmer	1	20
D-15		Programmer	1	18
D-16		Programmer	1	27
D-17		Programmer	1	26
D-18		Coder Control	1	7
D-19		1 CPS Reset	1	9
D-20		1 CPS Reset	1	21
D-21		Time Code Strobe	2	8
D-22		Time Code Strobe	1	15
D-23		I. D. Buffer	1	10
D-24		Dig Mpxr Pwr Strobe	1	9

Table 14 New Module Utilization Summary Analog Circuitry

New Module Designation	Old Module Replaced	Module Contents	Quantity Per System	Pins Utilized Per Module
A-1	M-1 thru M-22 and M-34 thru M-37	2 Inverter Packs 16 AND/NAND Gates	3	28
A-2		2 Inverters, 4 AND/ NAND Gates, 1 Analog Gate	1	13
A-3		1 AND/NAND Gate, 4 Inverters, Power Supply Conventional Components	1	45
A-4		8 Analog Gate Packs, 8 Inverter Packs	1	55
A-5		8 Analog Gate Packs, 8 Inverter Packs	20	51
A-6		2 Analog Gate Packs 4 Inverter Packs	1	20

Table 15 New Module Utilization Summary Coder Circuitry

New Module Designation	Old Module Replaced	Quantity Per System	Pins Utilized Per Module
CR-1A	C-19, C-26	1	Less pins per Funct' on than Present System
CR-1B	C-18, C-26	1	
CR-2	(2) C-25 (1) C-26	2	
CR-3	C-7, C-8, C-11	2	
CR-4	C-12, C-13	1	
CR-5	C-21, C-22	2	
CR-6	C-1, C-2	2	
CR-7	C-4, C-5, C-6	2	
CR-8	C-14, C-15, C-28	2	
CR-9	C-16, C-24, C-27	2	
CR-10	C-9	2	
CR-11	(2) C-10	6	

Table 16 Modules Requiring Relayout

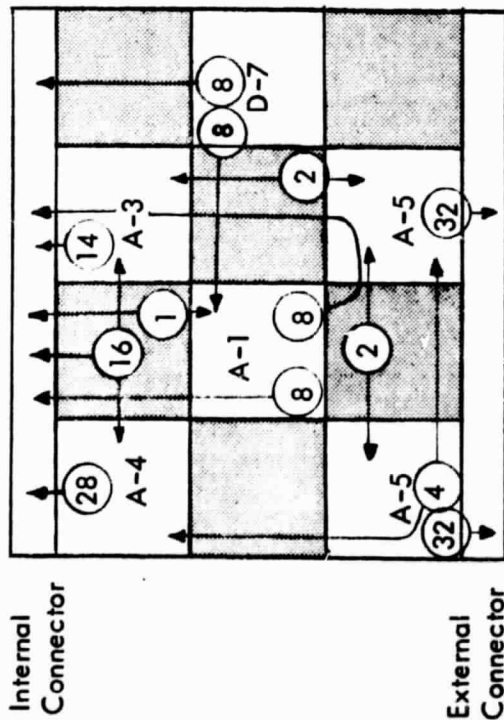
New Module Designation	Old Module Designation
R-1	M-27
R-2	M-28
R-3	M-29
R-4	M-30
R-6	M-32
R-7	M-33

temperature resistance material with circuitry on two sides, electro-deposited solder coated, and utilize plated through holes for the interconnections. The repackaged system will consist of nine trays, or eighteen cards. Each card has six modules, and is checkerboarded so that the assembled cards can interlock as in the present system. The cards have connectors on both ends, one for internal jumper wires, and the other for external interfaces. Card layouts are shown in (figure 108 through 113). Trays 7 and 8 are utilized for the coders, and tray 9 for the power supply. This allows ease of removal of either or both coders at a future date, should it be desired to remove them to a separate unit or to reduce them in size or quantity of functions. In order to fabricate the above cards, eighteen new layouts, one new master drawing, and one new drill template would be required. All of the cards would be able to utilize the new pin spacing and module placement on the cards. This assists in minimizing costs for the redesign of the system. To accommodate all of the pin requirements, the printed circuitry would be laid out under the following criteria:

Conductor width:	.015 inch
Land (terminal) width:	.060 inch
Hole size:	.035 inch
Conductor spacing:	. -12 inch

Pins used

$$\text{per Connector} = 28 + 8 + 16 + 1 + 14 + 8 + 8 = 83$$



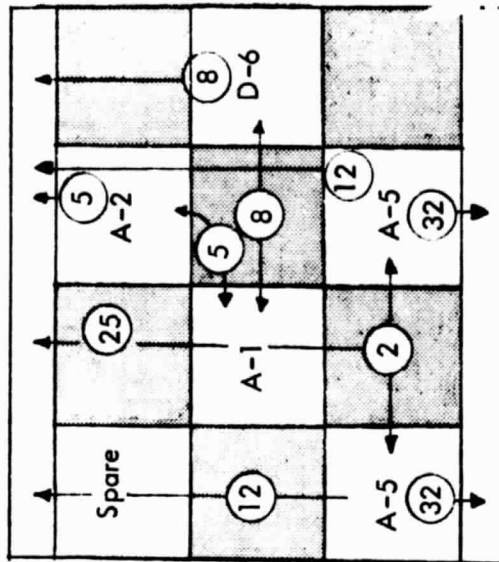
Pins used

$$\text{per Connector} = 32 + 32 = 64$$

Card A

Module	Quantity
A-1	1
A-3	1
A-4	1
A-5	2
D-7	1

$$12 + 2 + 25 + 5 + 12 + 8 = 64$$



$$32 + 32 = 64$$

Card B

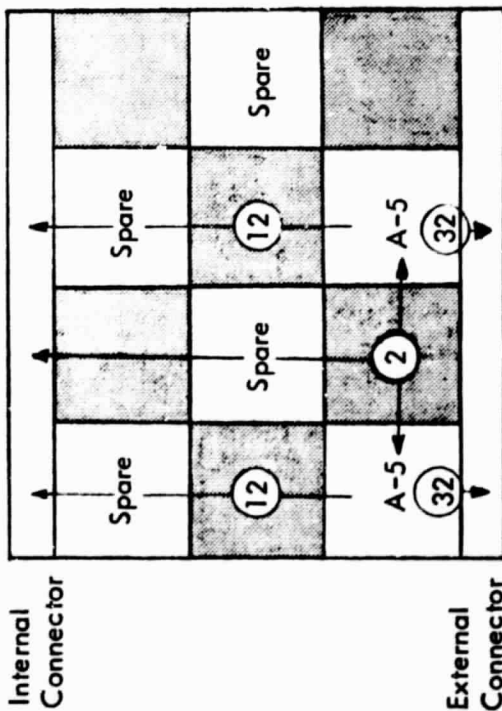
Module	Quantity
A-1	1
A-2	1
A-5	2
D-5	1
Spare	1

47409

Figure 108. Tray 1 Layout

Pins used

$$\text{per Connector} = 12 + 2 + 12 = \underline{26}$$



Pins used

$$\text{per Connector} = 32 + 32 = \underline{64}$$

TRAY NO. 2

Card A

Module	Quantity
A-5	2
Spare	4

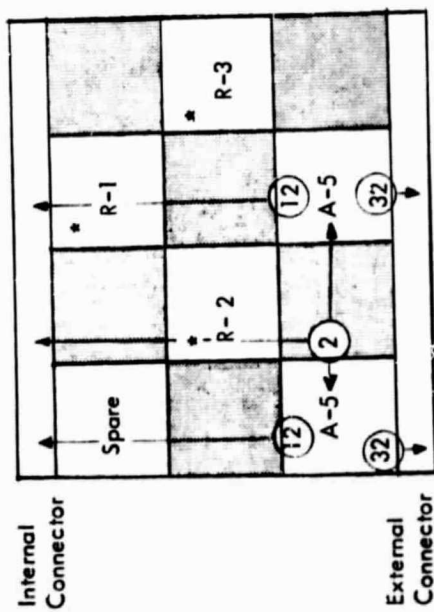
Card R

Module	Quantity
A-5	2
Spare	4

47410

Figure 109. Tray 2 Layout

$$\text{Pins used per Connector} = 12 + 2 + 12 = \underline{26}$$



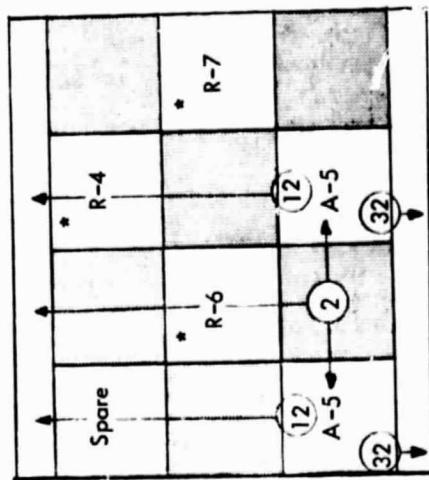
$$\text{Pins used per Connector} = 32 + 32 = \underline{64}$$

TRAY NO. 3

Card A

Module	Quantity
A-5	2
R-1	1
R-2	1
R-3	1
Spare	1

$$12 + 2 + 12 = \underline{26}$$



* Modules R-1, R-2, R-3, R-4, R-5, R-6, and R-7 have minimal pin and wiring utilization.

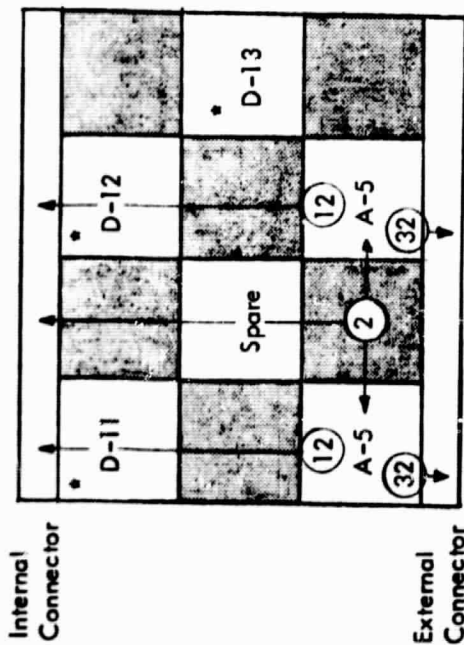
$$32 + 32 = \underline{64}$$

Card B

Module	Quantity
A-5	2
R-4	1
R-6	1
R-7	1
Spare	1

Figure 110. Tray 3 Layout

$$\text{Pins used per Connector} = 12 + 2 + 12 = \underline{26}$$

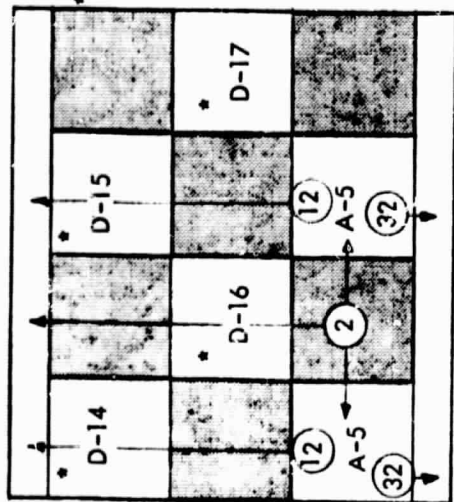


$$\text{Pins used per Connector} = 32 + 32 = \underline{64}$$

Card A

Module	Quantity
A-5	2
D-11	1
D-12	1
D-13	1
Spare	1

$$12 + 2 + 12 = \underline{26}$$



$$32 + 32 = \underline{64}$$

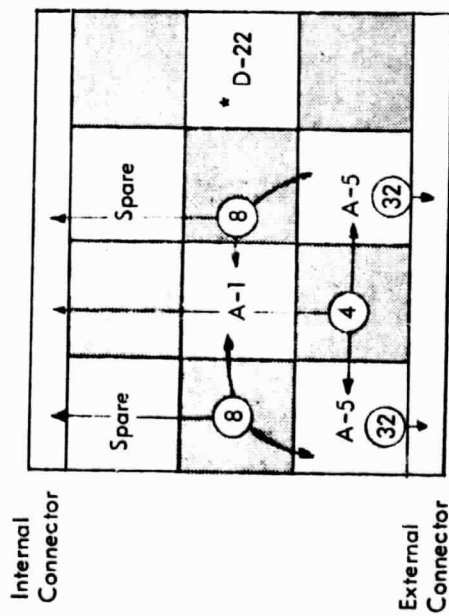
Card B

Module	Quantity
A-5	2
D-14	1
D-15	1
D-16	1
D-17	1

* Modules D-11 thru D-17 are Programmer modules. Their exact wiring requirements have not been determined at this time, but the wiring and pins needed is judged to be minimal.

Figure 111. Tray 4 Layout

$$\text{Pins used per Connector} = 8 + 4 + 8 = 20$$

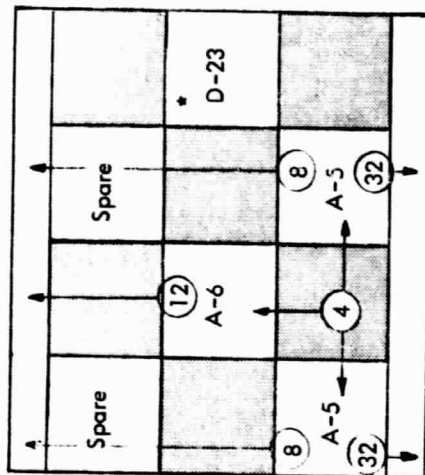


$$\text{Pins used per Connector} = 32 + 32 = 64$$

Card A

Module	Quantity
A-1	1
A-5	2
D-22	1
Spare	2

$$8 + 12 + 8 = 28$$



Modules D-22 & D-23 Considered to have minimal pin and wiring requirements.

$$32 + 32 = 64$$

TRAY NO. 5

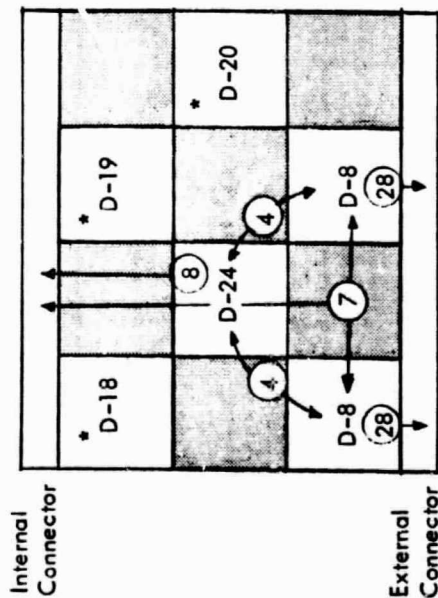
Card B

Module	Quantity
A-5	2
A-6	1
D-23	1
Spare	2

47413

Figure 112. Tray 5 Layout

Pins used
per Connector = $7 + 8 = 15$

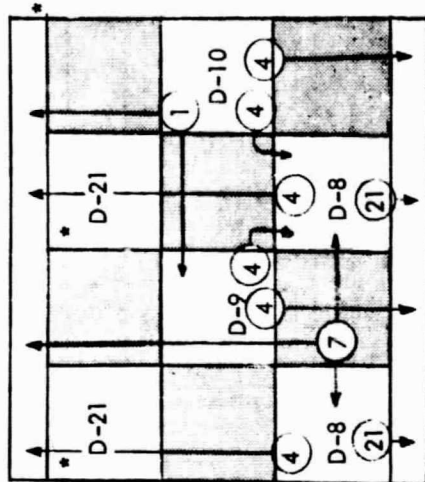


Pins used
per Connector = $28 + 28 = 56$

Card A

Module	Quantity
D-8	2
D-18	1
D-19	1
D-20	1
D-24	1

$4 + 7 + 4 + 1 = 16$



$21 + 4 + 21 + 4 = 50$

TRAY NO. 6

Card B

Module	Quantity
D-8	2
D-9	1
D-10	1
D-21	2

* Modules D-18, D-19, D-20, & D-21, are considered to have minimal pin and wiring requirements.

47414

Figure 113. Tray 6 Layout

In order to insure the proper tolerance and that the circuitry is of the proper cross-sectional area, fine line etching techniques will have to be employed in the fabrication of the cards. Although this technique requires about twice the amount of process time as the normal etching does, it will assure that the necessary line and spacing requirements are obtained.

2.13.3 Connectors. - Due to deficiencies in the presently utilized connector, a search was made into the selection of a new connector for use with the redesigned package. The limiting factors imposed on the connector selection were: (See Appendix III for performance)

- a. Pin requirements per card
- b. Physical size of the connectors
- c. Adaptability to the system
- d. Reliability of the contacts
- e. Ease of insertion and removal
- f. Polarization of connector

Following much investigation, a tentative connector was selected. It is the AMP-MECA 16 contact Wire-to-Board connector. This is a small, light weight connector presently under development by AMP, Inc., Harrisburg, Pennsylvania. It utilizes crimp contacts which are inserted in a Lexan molded body. The male contacts are of the flat blade types, which slide into a pre-formed beryllium copper receptacle. This receptacle has four (4) spring loaded

rib contacts which grip the blade on two opposite sides. The male body is held in place by edges of the molded female part, so the only possible movement is in the insertion-removal direction. Tests indicate that the average insertion removal forces are 8 ounces per contact, or 8 pounds for a sixteen contact connector. Vibration tests run at AMP have indicated no measurable electrical discontinuities of over one microsecond while the connector was subjected to 0.06 inch DA or 10 g vibration, which ever is less, at a frequency span of from 10 to 500 cps. This was done in the three mutually perpendicular planes for three hours per plane for a total vibration time of nine hours. Additional tests will have to be run to assure that the connector can surpass the Nimbus test specs, however. Presently, no means are provided for physically holding the male portion in the female receptacle in the insertion-removal direction. Contact retention is the only holding force. Since the proposed connector is presently in the prototype stage of development, however, there is a good possibility that a feature to accomplish this can be incorporated. Due to utilization spacing, this will necessitate a device which requires a minimum amount of space. Jack screws, etc. cannot be used because of this problem. Additional effort will have to be expended in this area.

Plans call for the use of six of the sixteen contact connectors per card edge, or 96 contacts per edge. This provides enough contacts to meet the maximum requirement of any of the cards along with providing a minimum of 10% spare pins. This also allows all of the internal connections to be made at

one edge of the card, while keeping all of the external connections on the other edge. External pin requirements are listed in table 17.

2.14 FABRICATION AND ASSEMBLY. - The system package will be made of sheet metal similar to the present units. Mounting to the spacecraft will be accomplished in the same manner. The printed circuit cards will be held in position by internal keying bars which will prevent any shift of the card stack. The electronics will be compression loaded as in the present system. No problems should be encountered in qualifying the system to test requirements. A holding fixture will be necessary for positioning and holding the carrier cards prior to and during module welding. In order to foam the modules, one new mold is required due to the new module sizes.

2.14.1 Handling. - Certain handling procedures are applicable to microelectronic assemblies which are beyond the requirements of conventional procedures.

CAUTION

During fabrication, assembly, and test of the MOS unit extreme care must be used to prevent the effects of electrostatic charges on the MOS unit from work benches, test equipment, human handling, and other factors.

The test procedures for the MOS unit (Appendix 14) describe the stringent procedure to be followed when handling a MOS unit.

Table 17 External Connections

Pins Required	Function
502	Analog "A" Unit
125	Analog "A" Unit: Redundant Lines
125	Analog "B" Unit
84	Digital
42	Digital: Redundant Lines
2	Time Code
2	100 cps
2	-24V (for Inhibit T.C.)
2	"A" Unit: NRZ Output
2	"A" Unit: Bit Rate Input
8	"A" Unit: -24V
6	"A" Unit: Power Ground
8	"A" Unit: Signal Ground
8	"A" Unit: Coder Test Points
5	"A" Unit: Analog Mpxr Test Points
20	"A" Unit: Sync. Test Points
5	"A" Unit: Digital Mpxr Test Points
2	"B" Unit: 5 kc $\emptyset$ Shift Output
2	"B" Unit: 5 kc Mod. Freq. Input
2	"B" Unit: 10 cps Bit Rate
2	"B" Unit: (+) Emergency Operation
2	"B" Unit: (-) Emergency Operation
2	"B" Unit: (+) Normal Operation
2	"B" Unit: (-) Normal Operation
2	"B" Unit: (+) Read Command
2	"B" Unit: (-) Read Command
7	"B" Unit: Primary Power Ground
7	"B" Unit: Signal Ground
4	"B" Unit: -24.5V
8	"B" Unit: Coder Test Points
5	"B" Unit: Sync. Test Points
1	"B" Unit: Mpxr Test Points
<u>998</u>	
100	10% Spare Contacts
<u>1098</u>	Total Pins Required
Total External Pin Capability = (16) (6) (9) (2), or 1728 pins	

SECTION III

BIBLIOGRAPHY

3. BIBLIOGRAPHY

3.1 GENERAL. This section lists the publications which are either referenced directly from the preceding sections or included to provide a greater depth of background material which is applicable to this study.

3.2 LISTING

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18. "Attainable Error Probabilities in Demodulation of Random Binary PCM/FM Waveforms" by E. F. Smith, I. R. E. Transactions on Space Electronics and Telemetry, December 1962.
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SECTION IV

APPENDICES

4. APPENDICES

4.1 INTRODUCTION. - This section includes all the information necessary to complete technical information requirements for this report. Some of the data presented in the appendices is included in the preceding text sections to preserve continuity only.

4.2 LIST OF APPENDICES.

- I Contract NAS 5-3787
- II Reliability Test Program
- III Amp-Meca Connector Test Data
- IV Reliability Calculation Forms
- V MOSFET Specification RAD 106510 (Semiconductor Device Set)
- VI Beacon Transmitter Modulation Signal Compatibility
- VII "A" Unit Modulator Modification
- VIII Design Study Test Tapes
- IX Specification, Integrated Digital Gate
- X Brush Event Recorder Specifications
- XI Brush Solid State Switching Specifications
- XII Model 4041 PCM Signal Conditioner and Bit Synchronizer
- XIII Series 540 PCM Decommutation System
- XIV Five Channel MOS Transistor Functional Test Procedure
- XV Glossary

APPENDIX I

CONTRACT NAS 5-3787

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION NEGOTIATED CONTRACT	Contract No. NAS5-3787
--	-------------------------------

ISSUING OFFICE

NAME NATIONAL AERONAUTICS AND SPACE ADMINISTRATION GODDARD SPACE FLIGHT CENTER	ADDRESS GLENN DALE ROAD GREENBELT, MARYLAND
---	--

CONTRACTOR

NAME RADIATION INCORPORATED	ADDRESS MELBOURNE FLORIDA
---------------------------------------	--

CONTRACT FOR Design Study to Determine Feasibility of Incorporation of Additional Performance Capability in the Nimbus PCM Telemeter	AMOUNT Cost \$92,600 Fee 7,200 Total \$99,800
--	---

APPROPRIATION AND OTHER ADMINISTRATIVE DATA

Control Number: PC 61610; Req. 653-898-64; OPCODE 07947; JO 653M25-01, (1C)

Type of Contract: Cost-Plus-Fixed-Fee

Administration By: NASA/Goddard Space Flight Center,
Greenbelt, Maryland

Appropriation and Account Chargeable: R&D 80X0108(64) FPC C2

Office to Make Payment: Fiscal Office, Goddard Space Flight
Center, Greenbelt, Maryland

Technical Officer: Benjamin Schlachman, Code 653

Contract Negotiator: H. Lee Tomlinson, Code 247

Security Classification: This Contract is unclassified as defined in
DD Form 441 and NASA Management Manual Para-
graph 6.b.

Priority Rating: DO-C9 Certified for national defense use
under DMS Regulation 1.

This negotiated contract is entered into pursuant to the provisions of 10 U.S.C. 2304 (a) (II) and any required Findings and
Determination have been made.

THIS CONTRACT is entered into as of APR 6 1964, by and between the United States of America, hereinafter called the
Government, represented by the Contracting Officer executing this contract, and Radiation Incorporated

(I) a corporation organized and existing under the laws of the state of Florida

(II) a partnership consisting of _____

(III) an individual trading as _____

hereinafter called the Contractor. The parties hereto agree that the Contractor shall furnish and deliver all supplies and perform all the
services set forth in the attached Schedule, for the consideration stated herein.

NASA FORM 487 (4/59)

HLT/ae

SCHEDULE

OBJECTIVE

The objective of this design study is to determine the feasibility of modifying the existing NIMBUS PCM Telemetry System to incorporate (a) time-coding, (b) digital channels, (c) synchronization of the PCM System with the Clock Subsystem, (d) digital tape recorder, (e) reliability of PCM frame synchronizer and the effects of such on the directly related NIMBUS PCM Ground Stations and acceptance test equipment.

I. STATEMENT OF WORK

The Contractor shall:

- Item 1. Perform the design study outlined in the objective in accordance with the Constraints and Requirements set forth in Paragraph II below and in general conformance with the Contractor's Proposal. In the event of conflict, the Contract Schedule shall prevail.
- Item 2. Furnish the Type I and Type III Reports as required by "Specifications for Contractor-Prepared Monthly, Periodic, and Final Project Reports," TID-S-100 dated August 1962 which is incorporated herein by reference.

II. CONSTRAINTS AND REQUIREMENTS

1.. Constraints

- 1.1 The study approach shall be along the line requiring the minimum modification to existing equipment and the minimum additional components. Additional components shall be similar to qualified and acceptable units in the present system to the maximum degree possible in accomplishing the objective set forth above.
- 1.2 The modifications and additions shall be capable of being incorporated in the same module size of the present multicoder. The volume reserved for the 256 channel expansion may be utilized. To the extent that this previously reserved volume is not adequate, consideration shall be given to utilizing micro-miniaturized circuitry. However, the effort that may be applied in this direction shall in no event exceed 10% of the total estimated cost of the contract.

SCHEDULE

1.3 Total additional power requirements shall be less than 1.50 Watts.

1.4 No study shall be undertaken to improve the Raymond Tape Recorder or the Hughes Beacon Transmitter.

2. Requirements

2.1 The synchronization with the Spacecraft Clock approach shall be directed towards converting the number of words per minor frame of 64 in the present system to 62.5 words per minor frame for the new system. The number of eight bit words in the prime channels, the number of minor frames per major frame and bit rate shall remain unchanged.

2.2 Time-Code shall utilize six time slots in the subcommutated channels of the first minor frame, as follows:

(1) units of seconds, (2) tens of seconds, (3) units of minutes, (4) tens of minutes, (5) units of hours, and (6) tens of hours.

2.3 In providing for digital data channels determine the feasibility of utilizing:

2.3.1 Four (4) prime analog channels for twenty-eight (28) digital channels

2.3.2 Fourteen (14) digital data channels in the sub-commutated matrix.

2.3.2.1 Seven (7) of the sub-commutated digital channels having a storage bistable circuit for registering occurrences of slow repetition rate. The storage bistable shall reset at major frame rate (every 16 seconds).

2.3.3 The last half word of each minor frame in combination with the present synch word to optimize the synch word code.

2.3.4 An alternative approach shall be provided should the approach set out in 2.3.1, 2.3.2 and 2.3.3 above not prove feasible.

SCHEDULE

- 2.4 Consider the application of utilizing the eight (8) track digital tape transport for a single and two (2) orbit capability (see Specifications dated January 1964 for "MRIR-PCM Endless Loop Digital Tape Recorder Subsystem").
- 2.5 System reliability requires that:
 - 2.5.1 Time-Code and digital channels shall be operational with the "A" Coder and redundant "B" Coder.
 - 2.5.2 The system shall also operate from the PCM Standby Clock upon command. Analog and Digital channels shall not be affected because of failure of the Spacecraft Clock. This shall be applicable to the "A" PCM only.
 - 2.5.3 The system shall be capable of operation with two PCM Spacecraft Tape Transports as in the present system.
 - 2.5.4 Synch operations use digital generation of synch and sub-frame words or the isolation of these words from the prime data channels.
- 2.6 The PCM Ground Station and modifications shall be compatible with the Spacecraft PCM telemetry changes.
 - 2.6.1 Circuitry for a Multichannel "on-off" event recorder shall be provided for the digital channels.
 - 2.6.2 Circuitry for the conversion of Time-Code NRZ signals to binary code for read-out on the Brush Recorder event markers shall be provided.
 - 2.6.3 Time-Code indication shall also be provided for the event recorder.
- 2.7 Investigate and determine functional design parameters and specifications for the modifications of PCM Test Sets and ground station simulators for the simulation and testing of time-code and digital channels..

SCHEDULE

2.8 Fabricate breadboards and/or laboratory test equipment as necessary to demonstrate the results of the studies as follows:

2.8.1 Those studies pertaining to the airborne equipment, excluding the digital tape recorder phase.

2.8.2 Those studies pertaining to the ground station modifications demonstrating synchronization and the PCM time slots for the digital channels and time code. Exclude the time code event marker and the digital channel event recorder. This demonstration shall be performed by the Contractor on the PCM ground station at GSFC utilizing a mincom tape generated by the Contractor with the airborne equipment modified as a result of the study.

III. GOVERNMENT FURNISHED PROPERTY

1. The following Government furnished property will be provided:

- (a) one (1) PCM Multicoder
- (b) one (1) Telemetry Electronics Module
- (c) one (1) Raymond Tape Recorder
- (d) one (1) Mincom Tape Recorder

Items (a), (b), and (c) will be furnished within forty-five (45) days from date of award. Item (d) will be furnished within four and one-half (4 1/2) months from date of award.

2. The PCM ground station at Goddard Space Flight Center shall be made available for the performance of the demonstrations set forth in Paragraph II, 2.8.2.

IV. PERFORMANCE AND DELIVERY

1. Schedule

Item 1. All engineering effort required by the study shall be completed within five and one-half (5 1/2) months after the "entered into" date of the Contract.

Item 2. (a) Type I Reports shall be delivered within ten (10) days following the period reported.

SCHEDULE

- Item 2. (b) A draft of the Type III (Final Report) shall be furnished within six (6) months from date of award. The report in final form shall be furnished within three (3) weeks after approval of the draft. This report shall include all drawings, computations, sketches, and information developed during the study as well as any experimental data taken during or applicable to the performance of this study. Comparative data on various alternatives shall be included in the report. The final report shall be sufficiently comprehensive and conclusive to permit a design specification to be obtained directly from this report both with regard to the additions and/or modifications to the existing spacecraft PCM subsystem, PCM ground stations, Acceptance Test Equipment and ground station Simulator.

2. Distribution

- Item 2. (a) Furnish two (2) copies direct to the Technical Officer by name, Code 653; one (1) copy to the Contracting Officer by name, Code 247.
- (b) The Final Report in draft form shall be furnished in five (5) copies to the Technical Officer with a notice of transmittal to the Contracting Officer. Distribution of the report in final form will be provided by the Technical Officer at the time of approval of the draft. The number of copies shall not exceed thirty-five (35).

V. TECHNICAL DIRECTION

The performance of the work required under this contract shall be subject to the technical direction and surveillance of Benjamin Schlachman, Technical Officer, Systems Engineering Branch, Code 653.

SCHEDULE

As used herein "technical direction" is direction to the Contractor which fills in details, requires pursuit of certain lines of inquiry, or otherwise serves to accomplish the contractual statement of work.

The technical direction to be valid:

- (1) must be issued in writing consistent with the general scope of the work set forth in this contract;
- (2) may not constitute new assignment of work or change to the expressed terms, conditions or specifications incorporated into this contract;
- (3) shall not constitute a basis for any increase in the contract fee or extension to the contract delivery schedule. As used herein surveillance includes, but is not restricted to, the right of prior review and consent by the Technical Officer to any contractor-initiated internal changes or subcontract changes within the terms, conditions and specifications of the prime contract which the contractor estimates will result in additional costs in excess of \$25,000. Nothing contained in this Article authorizes the contractor to incur costs in excess of the estimated cost or other limitation on funds set forth in this contract.

VI. ESTIMATED COST AND FIXED FEE

The total estimated cost of this Contract is \$92,600 exclusive of the fixed fee of \$7,200. The total of estimated cost and fixed fee is \$99,800.

VII. PAYMENT OF FIXED FEE

The fixed fee shall be paid in monthly installments based upon the percentage of completion of work as determined by the Contracting Officer.

VIII. SUBMISSION OF CLAIMS FOR REIMBURSEMENT

In accordance with the provisions of the clause of this contract entitled Allowable Cost, Fixed Fee and Payment, invoices or vouchers and any required supporting statements or certificates, properly

SCHEDULE

identifiable with the contract number, will be submitted by the contractor to the contracting officer or his authorized representative. Reimbursement claims should be submitted on Standard Form 1034 (Public Voucher for Purchases and Services other than Personal) and Continuation Sheet 1035 in original and six (6) copies. An analysis of total vouchered charges shall be provided on each reimbursement claim showing current and cumulative costs broken down by cost elements (i.e. material, direct labor, overhead, etc.) and fixed fee, when applicable. Where the amount of fee claimed depends on a computation based on physical progress or rate of delivery of the completed item, the basis for computing the fee installment shall be shown on the voucher.

IX. INSPECTION AND ACCEPTANCE

Final inspection and acceptance for all items shall be performed by the Contracting Officer or his authorized representative as named in Paragraph V above and shall be performed at Goddard Space Flight Center, Greenbelt, Maryland.

X. OVERHEAD

The contractor shall be reimbursed for overhead costs, not otherwise reimbursable under this contract as a Direct Cost, at billing rates acceptable to the contracting officer or his duly authorized representative, subject to appropriate adjustment when final rates are established in accordance with Clause No. 132 entitled "Negotiated Overhead Rates."

XI. CONTENTS OF CONTRACT

This Contract consists of:

1. The Title Page (NASA Form 437)
2. The Schedule in seven pages
3. The General Provisions NASA Form 417 (1-63)
4. Alterations to NASA Form 417 (1-63)
5. Clause 66 entitled "Contractor and Subcontractor Cost or Pricing Data"
6. Clause 86 entitled "Accident Prevention"
7. Clause 88 entitled "Implied Licenses"
8. Clause 100 entitled "Materials Reports"
9. Clause 104 entitled "Stop Work Order"
10. Clause 132 entitled "Negotiated Overhead Rates"
11. The Signature Page

The rights and obligations of the parties to this contract shall be subject to and governed by the Schedule and the General Provisions. To the extent of any inconsistency between the Schedule or the General Provisions, and any specifications or other provisions which are made of this contract by reference or otherwise, the Schedule and the General Provisions shall control. To the extent of any inconsistency between the Schedule and the General Provisions, the Schedule shall control.

IN WITNESS WHEREOF, the parties hereto have executed this Agreement as of the day and year first above written.

THE UNITED STATES OF AMERICA

By


(SIGNATURE)

H. LEE TOMLINSON

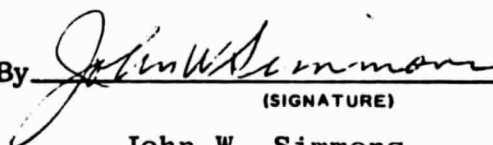
(CONTRACTING OFFICER)

CONTRACTOR

RADIATION INCORPORATED

(NAME OF COMPANY OR INDIVIDUAL)

By


(SIGNATURE)

John W. Simmons

(TYPED NAME)

Director of Contracts

(TITLE)

Melbourne, Florida

(ADDRESS)

APPENDIX II

RELIABILITY TEST PROGRAM

TEST REPORT
ON
INTEGRATED DIGITAL GATES
FOR
NIMBUS

JANUARY 22, 1965

Reliability Components Group
Prepared By

PREPARED BY:

J. Wolcott
J. Wolcott
Components Engineer

APPROVED BY:

J. F. House
J. F. House
Section Head
Reliability Engineering

CHECKED BY:

E. J. Heisel
E. J. Heisel
Test Engineer

APPROVED BY:

L. M. York
L. M. York
Program Manager

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ADMINISTRATIVE DATA

1.0 SCOPE

1.1 Purpose

The purpose of this test is to investigate the operational reliability of the subject integrated circuit devices for use in space electronic equipment.

1.2 General Information

1.2.1 Description of Test Sample

An integrated four input digital gate.

Type I - An early prototype

Type II- A later improved version of the Type I.

1.2.2 Manufacturer:

Radiation Inc. Physical Electronics Division.

1.2.3 Part Number:

Radiation Part No. 106626

1.2.4 Quantity Tested:

27 Type I
35 Type II

1.2.5 Applicable Documents:

Specifications - Radiation Inc.
106626 - Integrated Circuit Device

Standards
MIL-STD-202 Test Methods for Electronic and

Electrical Component Parts

MIL-STD-750 Test Methods for Semiconductor
Devices

1.2.6 Disposition of Test Samples:

Retained by Reliability Components Group for
further evaluation.

1.2.7 Test Conducted By:

Radiation Inc. Reliability Components Test Lab.

1.2.8 Test Report Date:

January 22, 1965

2.0 ABSTRACT

2.1 Summary

The subject integrated circuit devices were placed in an operational life test which simulated electrical operation of the devices by applying pulsed voltages to the device in a manner similar to the system power supply and signal inputs. The life test was run at an elevated temperature of +85°C with a 6 hour subcycle at -20°C performed five days out of every seven.

Each device was monitored daily for functional operation and end point measurements were made at specified intervals to determine parameter degradation.

The total amount of time accumulated on the devices was 2831.6 hours on the Type I and 1748.0 hours on the Type II for a total of 137,633.2 unit hours of test time.

Since this test was intended to be an investigation rather than a qualification, the data was used only to determine degradation and not to pass or fail devices by predetermined limits.

2.2 Results

No catastrophic failures (shorted or open devices) occurred during the test program. During the daily monitoring of the functional operation, degradation of one Type I circuit S/N 36 was noted. This circuit displayed unacceptable functional characteristics at the start of the test program, and therefore, further degradation is attributed to an initial defect not to a device failure.

2.3 Conclusions

The results of this study show the subject integrated circuit device to be stable and reliable for its intended use.

TABLE I

Time Performed Test Performed		O L D						N E W					
		0	114.2	330.4	531.7	1025.2	2003.6	End 2831.6	0 & 1748.0 End	186.8	279.7	539.7	1012.0
Parameter	Conditions												
h_{fe}	$V_{CE} = 50$ @ $T_A = -10^\circ C$ $I_C = 1ma$	X				X	X	X	X				
h_{fe}	$V_{CE} = 1V$ @ $T_A = -10^\circ C$ $I_C = 1ma$		X	X	X	X	X	X					
h_{fe}	$V_{CE} = 5V$ @ $T_A = +65^\circ C$ $I_C = 1ma$	X				X	X	X					
h_{fe}	$V_{CE} = 5V$ @ $T_A = -20^\circ C$ $I_C = 1ma$								X				
R_1		X				X	X	X	X	X	X	X	X
R_2		X				X	X	X	X	X	X	X	X
R_3		X				X	X	X	X	X	X	X	X
R_4		X				X	X	X	X	X	X	X	X
$V_{CE(sat)}$	$I_C = 1ma$ $I_b = .1ma$	X				X	X	X	X	X	X	X	X
$V_{CE(sat)}$	$I_C = 10ma$ $I_b = 1ma$	X				X	X	X	X				
V_{CBf}	$I_C = 1ma$								X				
V_{bef}	$I_b = 1ma$	X				X	X	X					
BV_{cbo}	$I_C = 100\mu a$	X				X	X	X	X				
I_{cbo}	$V_{CB} = 20V$	X				X	X	X	X	X	X	X	X
I_{cbo}	$V_{CB} = 30V$		X	X	X								
I_{cbo}	$V_{EB} = 5V$		X	X	X	X	X	X					
$I_R(CR1)$	$V_R = 30V$		X	X	X	X	X	X	X	X	X	X	X
$I_R(CR2)$	$V_R = 30V$		X	X	X	X	X	X	X	X	X	X	X
$I_R(CR3)$	$V_R = 30V$		X	X	X	X	X	X	X	X	X	X	X
$I_R(CR4)$	$V_R = 30V$		X	X	X	X	X	X	X	X	X	X	X
$I_R(CR5)$	$V_R = 30V$		X	X	X	X	X	X	X	X	X	X	X
$I_R(CR6)$	$V_R = 30V$		X	X	X	X	X	X	X	X	X	X	X
$I_R(CR7)$	$V_R = 30V$		X	X	X	X	X	X	X	X	X	X	X
$I_R(CR8)$	$V_R = 30V$		X	X	X	X	X	X	X	X	X	X	X
C_{ib}	5V 140kc	X							X				
C_{ob}	5V 140kc	X							X				
V_{be}	$I_b = 1ma$, $T_A = +25^\circ C$								X				
V_{be}	$I_b = 1ma$, $T_A = -20^\circ C$								X				

3.0 TEST PROCEDURES

3.1 Initial Electrical Parameters

The parameters specified in the original revision of the detail part specification were measured on the Type I devices prior to placing these units on life test. The Type II devices were measured to a revised set of parameters since they were manufactured to these parameters. Following the experience gained on the Type I and II specifications the 106626 detail part specification was generated to set forth the finalized requirements. Hence, several different parameters and conditions exist for the measurement of these circuits. The listing in Table I details the parameters tested, the conditions used and the times at which the measurements were made.

It should be noted that the detail part specification 106626 (See Appendix of the Nimbus Study Report) requires that the devices must meet the diode reverse leakage, the transistor reverse voltage base to collector, and the functional tests, and that the remaining parameters be used to establish design guidelines. For this reason, and to gain as much information as possible, all units were placed on test even if they did not fully meet all parameters.

The functional test used for the purposes of this study was to monitor the waveform at the collector of each transistor. The amplitude of the waveform must be 20 volts minimum. This test was performed on a GO-NO-GO basis daily.

3.2 Operating Life Test

3.2.1 The specimens were placed in a chamber, and the temperature was cycled between the high +85 degrees C, and the low -20 degrees C, test temperature. Each cycle consisted of 24 hours operation at the high test temperature with the low temperature subcycle performed during five out of every seven cycles. The low temperature subcycle consisted of reducing the chamber temperature at a maximum rate of 5°C/minute to the low test temperature. The low test temperature was maintained for $6 \pm 1/2$ hour and the temperature was then increased to the high test temperature at a maximum rate of 5°C/minute. The temperature remained at the high test temperature for the remainder of the cycle.

3.2.2 The units were subjected to a simulated switching operation which provided a stress on the device equal to that of the actual operation. During the operating



FIGURE 1
LIFE TEST CIRCUIT

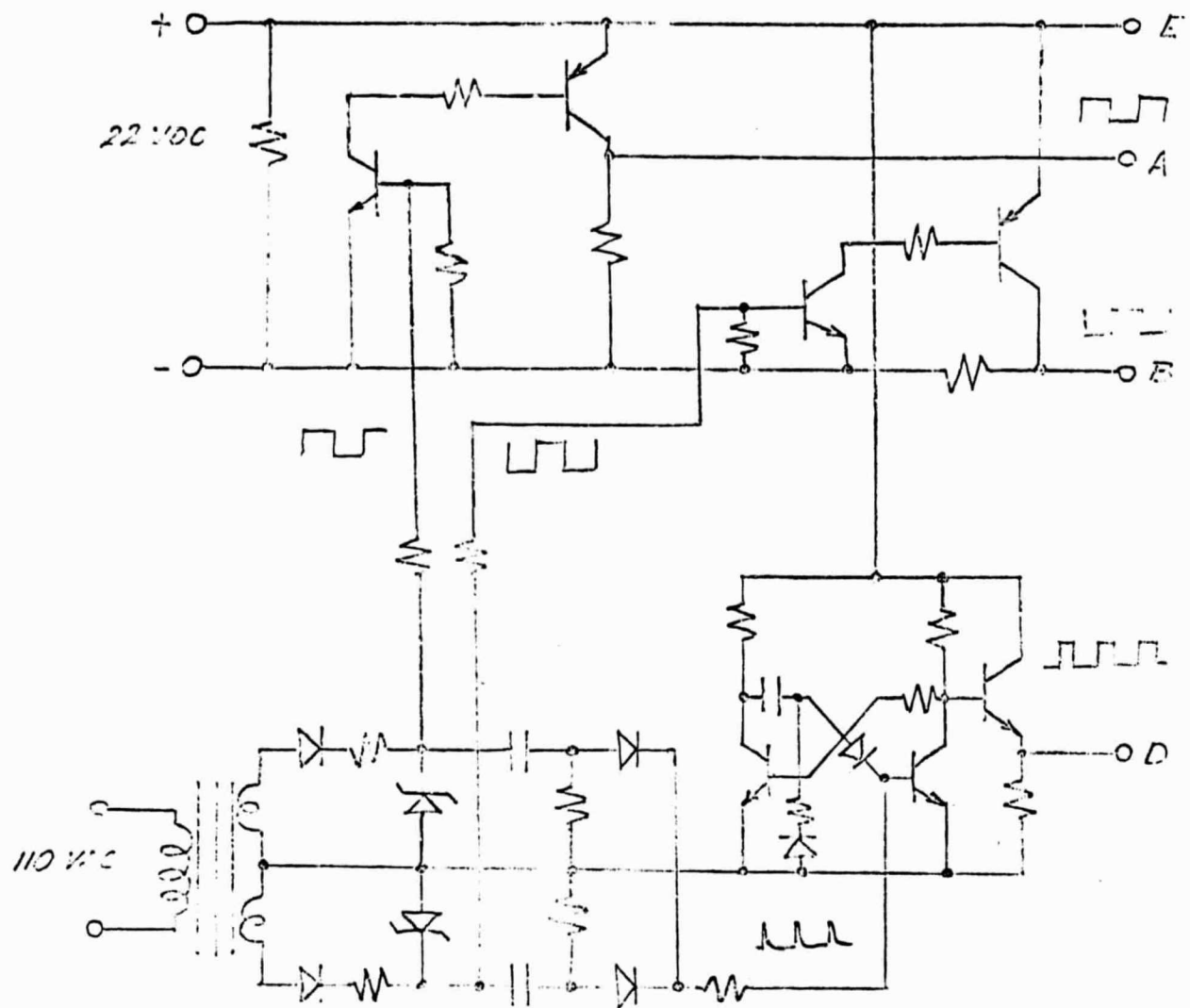


FIGURE 2
WAVEFORM GENERATOR

life test, the input lines were bussed together to form a single input, and the output lines were bussed together to form a single output. Switching was performed at a 120 cps rep rate.

Figure 1 shows a typical schematic and waveforms applied to the device. Figure 2 shows the schematic of the waveform generator used to supply the voltage for the life test.

2.2.2 Life Test Circuit Operation

The waveform generator, Figure 2, places 0 volts on the input diodes and -22 volts on the output diodes on one half of the operation cycle and reverses the voltages for the other half cycle. The transistor is turned on with a strobe pulse during each half cycle. Thus, current is drawn through each diode once each cycle, through each resistor twice each cycle and through the transistor twice each cycle. In addition, each diode is subjected to a reverse voltage once each cycle. The 1K resistors in series with the diodes are for the purpose of protecting the waveform generator from damage in case of shorts or catastrophic failures. The 68 K resistor in series with the transistor base limits the strobe pulse current.

3.2.4

The end points were measured at intervals throughout the test corresponding to 0, 100, 250, 500, 1000 and each subsequent 1000 hours. (Refer to 3.1 and Table I.)

4.0

RESULTS

Three Type I devices failed to meet initial functional tests. These three devices did not have sufficiently high collector-base breakdown voltage to pass the initial electrical tests; however, they were placed on test along with the good devices for additional information. One of these units, S/N 36 showed further degradation between 570 and 600 hours. This has not been counted as a device failure since it was definitely an initially defective unit.

Nine of the Type II devices were only partially operative at the start of the test, but were also placed on test for additional information. These devices had either low collector base breakdown voltage, excessive diode reverse current leakage or both. These failures were also indicated by the functional test. None of the Type II devices degraded from their initial measurement.

The results of this test show that the units have not been sufficiently screened to eliminate electrical failures prior to this test. This result was anticipated, but it was decided to place all units on test rather than only the electrically good units so that as much information on the reliability of the device could be gathered as possible.

The results also showed that of those devices which meet the initial electrical requirements, all successfully completed the life test under conditions equal to or more severe than that expected in the Nimbus Satellite.

APPENDIX III

AMP-MECA CONNECTOR TEST DATA

APPENDIX III

The proposed AMP wire-to-card MECA-type connectors were exposed to the vibration test requirements specified for the Nimbus System. During the test, the connectors received both sinusoidal and random vibration. The connectors were checked for physical unmating and monitored for noise due to scrubbing of the contacts. In addition, contact resistance was measured before and after the vibration test. The physical test and card arrangement and set-up is described in report EE-1152, a copy of which is attached.

No evidence of the connector halves having any tendency to come apart was present. No physical damage occurred to the cards or connectors as a result of the test. With the exception of Card No. 1, noise generation was negligible, and contact resistance showed no significant changes.

Card No. 1 showed an excessive amount of generated noise during vibration, and did not complete the specified tests. Subsequent examination of the card showed that, on two wires in one connector and one in another, more than eight (8) of the 19 strands of the wires had been severed. Tying a power source into this card and monitoring current, major fluctuations in the current were induced by "wiggling" the wires which contained the broken strands. Further examination of the wires involved showed that the strands were broken immediately above the crimp joint, and that the crimp joints were not as well centered as on the contacts where the wire strands were intact. These observations lead to the conclusion that poor crimp joints, with the resulting broken wire strands, were the cause of the noise generation on Card No. 1.

The results obtained from Cards No. 2 and 3 are such as to lead to the recommendation of the use of these connectors on future programs where a small, light-weight, wire to card connector is needed. If this is done, a short indoctrination period in the proper use of the specified crimp tools would be undertaken to preclude any problems such as encountered in Card No. 1.

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PURPOSE

The submitted miniature connectors were tested to see if they could physically meet the vibration requirements specified in Environmental Specification for Nimbus Systems, National Aeronautics and Space Administration, dated 1962.

ADMINISTRATIVE DATA

Item Tested:	Miniature Connectors
Manufacturer:	AMP Incorporated
Manufacturer's Model Number:	Prototype
Environmental Specification:	Environmental Specification for Nimbus Systems, National Aeronautics and Space Administration, dated December 1962
Quantity Items Tested:	18
Security Classification:	Unclassified
Date Test Completed:	28 September 1964
Test Conducted By:	Radiation Incorporated
Disposition of Specimens:	Returned to Engineering, Radiation Incorporated

ABSTRACT

The submitted connectors were subjected to a vibration test to the requirements specified for the Nimbus systems. During this test the connectors were exposed to sinusoidal and Gaussian random vibration. The connectors were monitored for generation of noise due to scrubbing of their contacts. In addition contact resistance was measured before and after the vibration test. Six connectors were mounted on a printed circuit type card and their contacts wired in series to simulate normal mounting conditions. Each card was then exposed to the vibration conditions specified above.

There was no physical damage to the cards as a result of the vibration test. The noise generation due to contact scrubbing was negligible. The contact resistance showed no significant change as a result of the vibration test.

TEST EQUIPMENT

<u>ITEM</u>	<u>MFG.</u>	<u>MOD.</u>
1. Power Amplifier	Ling Electronics	PP/20/24/C
2. Console	Ling Electronics	R-1004-C
3. Random Console	Ling Electronics	ASDE-80
4. Shaker Table	Ling Electronics	A-246
5. Servo (cycling)	Ling Electronics	S-CO-2
6. Oscillator	Ling Electronics	S-CO-2
7. Tracking Filter	Spectral Dynamics Corp.	SD101A
8. True RMS Meter	Ballantine	320
9. Oscilloscope	Tektronix	545A
10. Type D Plug-In	Tektronix	Type D
11. Accelerometer	Endevco	2213C
12. Amplifier	Endevco	2614
13. Power Supply	Endevco	2622
14. Sine/Noise Mixer	Ling Electronics	MA-2-A
15. Milliammeter	Weston	901
16. Volt Meter	Electro Inst	
(a) Power Unit		3000 A
(b) Volt Meter		3500
(c) Preamplifier		3020Q
17. Constant Current Supply	Radiation	

1.0 DESCRIPTION OF TEST SAMPLE

The miniature connectors tested were ten-pin connectors measuring approximately $3/4"$ x $3/4"$ x $1/4"$. Six of these connectors were mounted on a printed circuit card to simulate actual test conditions and the contacts connected in series. Three of these cards were made up to provide three groups to be tested. See Figure 1.

2.0 FACILITIES AND EQUIPMENT REQUIREMENTS

2.1 Ambient Conditions

Unless otherwise specified the following are the considered ambient conditions:

Temperature	$25^{\circ}\pm 10^{\circ}\text{C}$
Relative Humidity	90% or less
Barometric Pressure	Local Ambient

2.2 Control Tolerances

Unless specified herein the maximum environmental control tolerances held during the test program were as follows:

Vibration Amplitude	$\pm 5\%$
Vibration Frequency	$\pm 5\%$
Random Vibration Levels	± 3 db

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Connectors Mounted On Printed Circuit Cards

Figure 1

2.3 Measurement Tolerances

Unless otherwise specified the maximum environmental test tolerances were as follows:

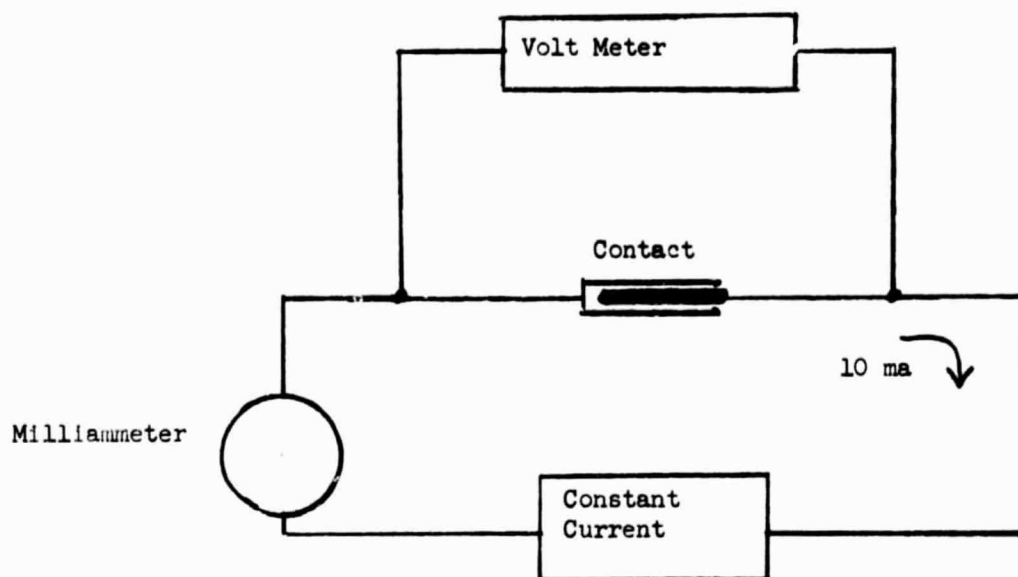
Vibration Amplitude	$\pm 5\%$
Vibration Frequency	$\pm 5\%$
Random Vibration	± 1 db
True RMS Voltage	$\pm 3\%$
DC Voltage	$\pm .01$ or 1 digit, whichever is greater
DC Current	$\pm .5\%$ FS

3.0 ELECTRICAL MEASUREMENTS

3.1 Contact Resistance

The connectors were subjected to a contact resistance test prior to and at the completion of the vibration test.

Each card was individually set up to monitor contact resistance as shown in Figure 2. With 10 milliamps flowing through the circuit, the voltage drop of each contact was measured on one of the connectors designated as a sample connector. There was one sample connector per printed circuit card. In addition to the individual contact resistance, the total resistance of the series connectors on each card was recorded. The measurements taken before and after the vibration test were compared for evidence of any change.

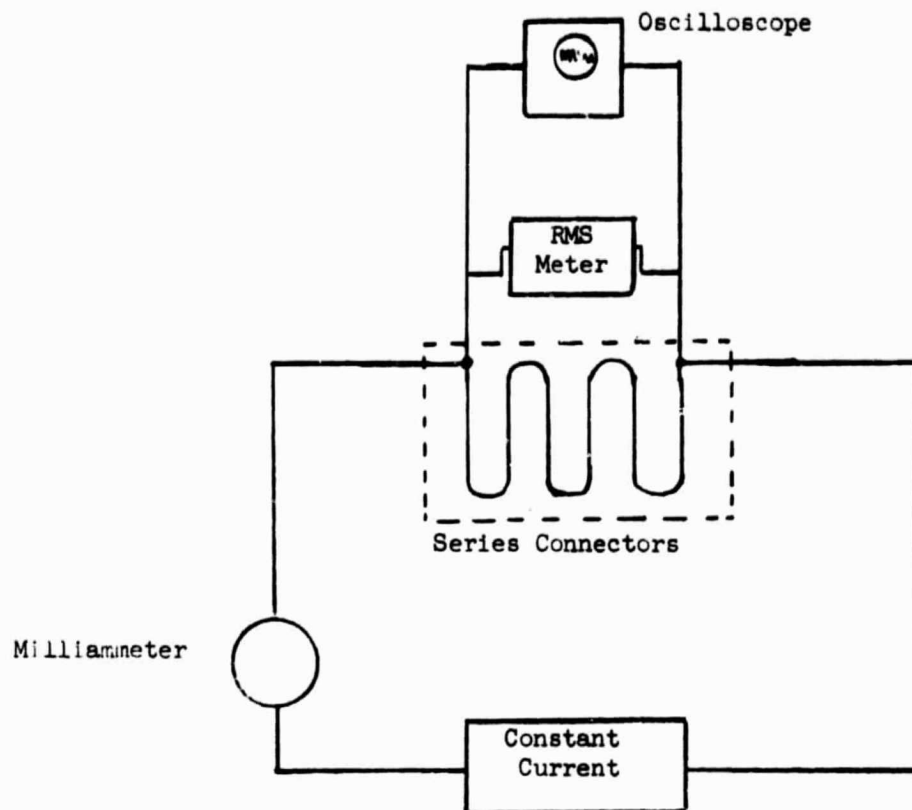


Contact Resistance Test Setup

Figure 2

3.2 Noise Measurements

During the vibration test, the connectors were monitored for generation of electrical noise due to scrubbing of their contacts. Figure 3 shows the test setup for monitoring this condition. With 10 milliamps flowing through the circuit, the change in voltage due to the change in contact resistance during vibration was measured with a true RMS meter and an oscilloscope. The readings recorded were the total voltage generated from 6 connectors or 60 contacts in series.



Noise Monitor Circuit Test Setup

Figure 3

4.0 VIBRATION ENVIRONMENT

4.1 Test Procedure

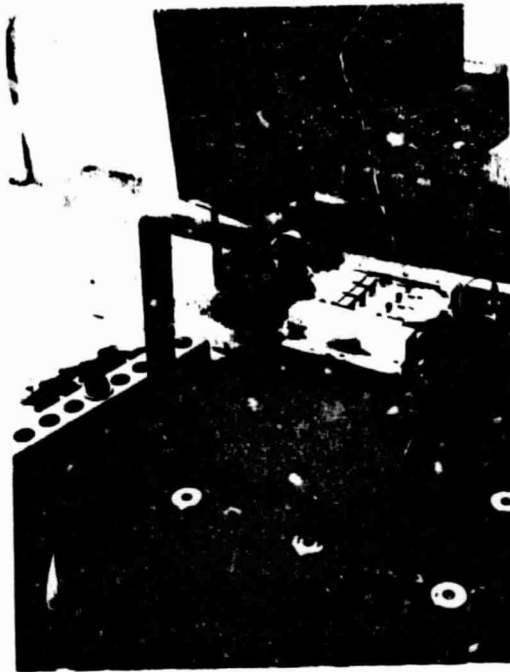
Each printed circuit card with six connectors was mounted on a test fixture which in turn was rigidly mounted to the vibration shaker. Figure 4 is a typical test setup of the vibration test. Each of the cards were then subjected to a sinusoidal vibration input of 10 g's peak or .25" double amplitude, whichever was less. The vibration input was swept from 5 - 2000 cps at a constant octave sweep rate of 2 minutes per octave. The sinusoidal vibration test was conducted in each of three mutually perpendicular axes as shown in Figure 5.

At the completion of the sinusoidal sweep in each axis the printed circuit cards were subjected to a random vibration test. The power spectral density level during this test was 0.2 g²/cps from 20 to 2000 cps (20 g's RMS). The random vibration input was applied for a period of 4 minutes in each axis.

During the vibration test, the connectors were monitored for noise generation as described in paragraph 3.2. Prior to and at the completion of the vibration test, the contact resistance of the connectors was measured as described in paragraph 3.1.

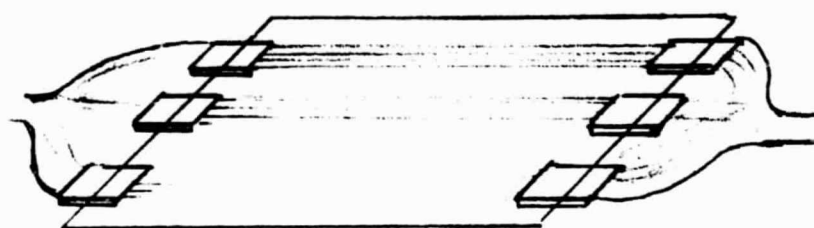
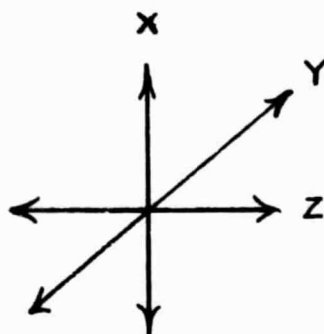
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Typical Vibration Test Setup

Figure 4



Definition of Axis

Figure 5

4.2 Test Results

At the completion of the vibration test, the connectors were examined for any evidence of damage and none was observed. It was also observed that there was no physical discontinuity between the two halves of the connectors as a result of the vibration test.

The contact resistance measurements taken prior to and at the completion of the vibration test showed no significant change in contact resistance. The noise generated during the vibration test due to scrubbing of the contacts was negligible in each of the three axes of vibration on cards 2 and 3. Card No. 1 showed an excessive amount of generated noise during vibration. When checking the card, indication of a loose connection was observed; however, none could be found. As a result, this card was only vibrated in the X and Y axes. It should be noted that the quantity of potting compound around the leads from the connectors on this card was greater than that of cards 2 and 3. All data taken before, during and after the vibration test is shown in the appendix.

A P P E N D I X

Test Data Sheets

DATA SHEETTEST Contact Resistance-Initial DATE 9-21-64CARD NUMBER one ENGINEER K. ColeTotal Series Resistance of Card: 3.25 ohms (Includes Lead Resistance)

Contact Resistance of one Connector on Card: __

<u>Contact No.</u>	<u>Contact Resistance (Milliohms)</u>
--------------------	---------------------------------------

1	4.0
2	3.5
3	4.4
4	4.2
5	4.9
6	4.0
7	4.9
8	4.0
9	4.9
10	3.5

DATA SHEETTEST Post Vibration Resistance Meas. DATE 9-28-64CARD NUMBER One ENGINEER K. OleTotal Series Resistance of Card: 3.31 ohms (Includes Lead Resistance)

Contact Resistance of one Connector on Card:

<u>Contact No.</u>	<u>Contact Resistance (Milliohms)</u>
1	4.9
2	4.6
3	4.7
4	4.3
5	4.5
6	3.7
7	4.0
8	3.9
9	4.6
10	4.2

DATA SHEETTEST Contact Resistance Initial DATE 9-21-64CARD NUMBER Two ENGINEER K. ColeTotal Series Resistance of Card: 2.92 ohms (Includes Lead Resistance)

Contact Resistance of one Connector on Card: .

<u>Contact No.</u>	<u>Contact Resistance (Milliohms)</u>
1	3.6
2	3.3
3	4.0
4	3.3
5	3.7
6	3.6
7	3.7
8	3.7
9	3.7
10	3.7

DATA SHEETTEST Post Vibration Resistance Meas. DATE 9-28-64CARD NUMBER Two ENGINEER K. ColeTotal Series Resistance of Card: 2.99 ohms (Includes Lead Resistance)

Contact Resistance of one Connector on Card:

<u>Contact No.</u>	<u>Contact Resistance (Milliohms)</u>
1	3.8
2	4.0
3	3.7
4	3.7
5	4.0
6	4.2
7	3.4
8	4.2
9	3.7
10	4.3

DATA SHEETTEST Cont. Res. - Initial DATE 9-21-64CARD NUMBER Three ENGINEER K. ColeTotal Series Resistance of Card: 2.97 ohms (Includes Lead Resistance)

Contact Resistance of one Connector on Card:

<u>Contact No.</u>	<u>Contact Resistance (Milliohms)</u>
1	4.7
2	3.4
3	3.8
4	3.5
5	3.9
6	3.4
7	3.5
8	3.3
9	4.3
10	3.1

DATA SHEETTEST Post Vibration Resistance Meas. DATE 9-28-64CARD NUMBER Three ENGINEER K. ColeTotal Series Resistance of Card: 3.03 ohms (Includes Lead Resistance)

Contact Resistance of one Connector on Card:

<u>Contact No.</u>	<u>Contact Resistance (Milliohms)</u>
--------------------	---------------------------------------

1	4.2
2	3.2
3	4.0
4	3.2
5	3.7
6	3.3
7	3.1
8	3.4
9	3.9
10	3.3

DATA SHEETTEST Vibration 'X' Axis DATE 9-21-64CARD NUMBER ONE ENGINEER K. Cole

Static Noise Level:

RMS Meter 130 μ V RMS Oscilloscope < 200 μ V Pk

Noise Level During Random Vibration:

* RMS Meter 22.5 millivolts rms Oscilloscope 8.0 millivolts Pk
4.0 " " 3.5 " "

Noise Level During Sine Sweep Vibration:

<u>Frequency</u>	<u>RMS Meter μV RMS</u>	<u>Oscilloscope μV Pk</u>
15	130	< 200
30	190	225
60	140	225
120	320	2000
170	600	3,000
240	500	2500
280	130	200
330	200	600
480	160	225
960	250	1000
1200	140	200
1700	< 100	< 200
1920	< 100	< 200

* The noise level during vibration in this axis varied between these points.

DATA SHEET

TEST Vibration "X" Axis DATE 9-21-64
CARD NUMBER Two ENGINEER K. Cole

Static Noise Level:

RMS Meter 150 μ V Rms Oscilloscope < 200 μ V Pk

Noise Level During Random Vibration:

RMS Meter 115 μ V Rms Oscilloscope < 200 μ V Pk

Noise Level During Sine Sweep Vibration:

<u>Frequency (Cps)</u>	<u>RMS Meter (Rms)</u>	<u>Oscilloscope Pk</u>
15	125 μ V	< 200 μ V Pk
30	130 "	
60	125 "	
120	110 "	
140	100 "	
280	115 "	
560	100 "	
700	100 "	
1120	100 "	
2000	100 "	

DATA SHEETTEST Vibration "X" Axis DATE 9-21-64CARD NUMBER Three ENGINEER K. Cole

Static noise Level:

RMS Meter < 100 μ V Rms Oscilloscope < 200 μ V Pk

Noise Level During Random Vibration:

RMS Meter < 100 μ V Rms Oscilloscope < 200 μ V Pk

Noise Level During Sine Sweep Vibration:

<u>Frequency (cps)</u>	<u>RMS Meter (μV Rms)</u>	<u>Oscilloscope (μV Pk)</u>
15	<u>< 100</u>	<u>< 200</u>
30		
60		
120		
240		
480		
960		
1920		
2000		

DATA SHEETTEST Vibration 'Y' Axis DATE 9-21-64CARD NUMBER One ENGINEER K. Cole

Static Noise Level.

RMS Meter 125 μ V Rms Oscilloscope < 200 μ V Pk

Noise Level During Random Vibration:

RMS Meter 2 millivolts Rms Oscilloscope 40 mV Pk

Noise Level During Sine Sweep Vibration:

<u>Frequency (cps)</u>	<u>RMS Meter</u>	<u>Oscilloscope</u>
15	130 μ V	200 μ V
30	100 mV	200 mV Pk
35	130 μ V	200 μ V
60	125 μ V	200 μ V
120	160 μ V	400 μ V
180	1.8 mV	-
210	8 mV	-
240	3.5 μ V	-
300	130 μ V	200 μ V
480	240 μ V	1 mV
600	500 μ V	1 mV
800	140 μ V	200 μ V
960	300 μ V	1 mV
1180	600 μ V	-
1920	400 μ V	500 μ V

DATA SHEET

TEST Vibration "Y" Axis DATE 9-23-64
 CARD NUMBER Two ENGINEER K. Cole

Static Noise Level:

RMS Meter < 100 μ V RMS Oscilloscope < 200 mV Pk

Noise Level During Random Vibration:

RMS Meter < 100 μ V RMS Oscilloscope < 200 mV Pk

Noise Level During Sine Sweep Vibration:

<u>Frequency</u>	<u>RMS Meter</u>	<u>Oscilloscope</u>
<u>15</u>	<u>< 100 μV RMS</u>	<u>< 200 mV Pk</u>
<u>30</u>	<u>"</u>	<u>"</u>
<u>60</u>	<u>"</u>	<u>"</u>
<u>120</u>	<u>"</u>	<u>"</u>
<u>240</u>	<u>"</u>	<u>"</u>
<u>480</u>	<u>"</u>	<u>"</u>
<u>960</u>	<u>"</u>	<u>"</u>
<u>1920</u>	<u>"</u>	<u>"</u>
<u>2000</u>	<u>"</u>	<u>"</u>

DATA SHEETTEST: Vibration "Y" Axis DATE 9-23-64CARD NUMBER Three ENGINEER K. Cole

Static Noise Level:

RMS Meter 400 μ V RMS Oscilloscope 600 μ V Pk

Noise Level During Random Vibration:

RMS Meter 470 Oscilloscope 700 μ V Pk

Noise Level During Sine Sweep Vibration:

<u>Frequency</u>	<u>RMS Meter</u>	<u>Oscilloscope</u>
15	400 μ V	600 μ V Pk
30	400	600
60	400	600
120	250	600
240	250	600
480	250	600
960	460	900
1920	460	900
2000	460	900

DATA SHEETTEST Vibration Z Axis DATE 9-28-64CARD NUMBER Two ENGINEER K. Cole

Static Noise Level:

RMS Meter < 100 RmsOscilloscope < 200 PK

Noise Level During Random Vibration:

RMS Meter < 100 RmsOscilloscope < 200 PK

Noise Level During Sine Sweep Vibration:

FrequencyRMS MeterOscilloscope

15	< 100 μ V	< 200 μ V
30	"	"
60	"	"
120	"	"
240	"	"
480	"	"
960	"	"
1920	"	"
2000	"	"

DATA SHEETTEST Vibration Z AxisDATE 9-28-64CARD NUMBER ThreeENGINEER K. Cole

Static Noise Level:

RMS Meter < 100 μ v RMS Oscilloscope < 200 μ v Pk

Noise Level During Random Vibration:

RMS Meter 160 μ v Oscilloscope 200 μ v

Noise Level During Sine Sweep Vibration:

<u>Frequency</u>	<u>RMS Meter</u>	<u>Oscilloscope</u>
15	160 μ v	200 μ v
30	160 μ v	200 μ v
60	160 μ v	200 μ v
120	160 μ v	200 μ v
240	"	"
480	"	"
960	"	"
1920	"	"
2 KC	"	"

APPENDIX IV

RELIABILITY CALCULATION FORMS

RELIABILITY CALCULATION FORM

RADIATION
INCORPORATED

DATE: _____

PROJECT NO. 1858

UNIT TITLE: 1 CPS Reset

S/N: _____

COMPONENT	N	$\lambda \times 10^{-5}$	$N \lambda \times 10^{-5}$	REMARKS
Resistors, MIL-R-11C	50	.001	.050	< 10% Stress
Capacitors, Ceramic	11	.001	.011	< 20% Stress
Diodes (Si)	21	.010	.210	< 10% Stress
Transistors (Si)	17	.020	.340	< 10% Stress

* BASED ON TEMPERATURE AND STRESS

0.011 = λ TOTAL (%/1000 HOURS)

= MTBF (HOURS)

DATE: _____

PROJECT NO. 1858

UNIT TITLE: Time Code Storage

S/N: _____

COMPONENT	N	$\lambda \times 10^{-5}$	$N \lambda \times 10^{-5}$	REMARKS
Resistors, MIL-R-11C	72	.001	.072	< 10% Stress
Capacitors, Ceramic	17	.001	.017	< 20% Stress
Diodes (Si)	29	.010	.290	< 10% Stress
	1	.019	.019	< 30% Stress
Transistors (Si)	23	.020	.460	< 10% Stress

* BASED ON TEMPERATURE AND STRESS

. 358

= λ TOTAL (%/1000 HOURS)

= MTBF (HOURS)

RELIABILITY CALCULATION FORM

RADIATION
INCORPORATED

DATE: _____

PROJECT NO. 1658

UNIT TITLE: Transient Data Storage

S/N: _____

COMPONENT	N	$\lambda \times 10^{-5}$	$N\lambda \times 10^{-5}$	REMARKS
Resistors, MIL-R-11C	43	.001	.043	< 10% Stress
Transistors (Si)	15	.02	.30	< 10% Stress

* BASED ON TEMPERATURE AND STRESS

0.343 = λ TOTAL (%/1000 HOURS)

= MTBF (HOURS)

RELIABILITY CALCULATION FORM

RADIATION
INCORPORATED

DATE: _____

PROJECT NO. 1858

UNIT TITLE: I. D. Buffers

S/N: _____

COMPONENT	N	$\lambda \times 10^{-5}$	$N \lambda \times 10^{-5}$	REMARKS
Resistors, MIL-R-11C	12	.001	.012	< 10% Stress
Transistors (Si)	8	.02	.160	< 10% Stress

* BASED ON TEMPERATURE AND STRESS

. 172

= λ TOTAL (%/1000 HOURS)

= MTBF (HOURS)

RELIABILITY CALCULATION FORM

RADIATION
INCORPORATED

DATE: _____

PROJECT NO. 1858

UNIT TITLE: Digital Multiplexer - Power Strobe

S/N: _____

COMPONENT	N	$* \lambda \times 10^{-5}$	$N \lambda \times 10^{-5}$	REMARKS
Resistors, MIL- R - 11C	13	.001	.013	< 10% Stress
	1	.001	.001	< 20% Stress
Capacitors, Ceramic	2	.001	.002	< 10% Stress
Diodes (Si)	9	.013	.117	< 20% Stress
Transistors (Si)	6	.020	.120	< 10% Stress

* BASED ON TEMPERATURE AND STRESS

.253 = λ TOTAL (%/1000 HOURS)

= MTBF (HOURS)

RADIATION
INCORPORATED

PROJECT NO. 1858

S/N: _____

* BASED ON TEMPERATURE AND STRESS

= MTBF (HOURS)

RELIABILITY CALCULATION FORM

RADIATION
INCORPORATED

DATE: _____

PROJECT NO. 1858

UNIT TITLE: Bias Amplifier and Core Drivers

S/N: _____

COMPONENT	N	* $\lambda \times 10^{-5}$	N $\lambda \times 10^{-5}$	REMARKS
Resistors, MIL-R-11C	25	.001	.025	< 20% Stress
	7	.002	.014	< 40% Stress
Transistor (Si)	17	.020	.340	< 10% Stress
Diode (Si)	1	.010	.010	< 10% Stress

* BASED ON TEMPERATURE AND STRESS

.389 = λ TOTAL (%/1000 HOURS)

= MTBF (HOURS)

RELIABILITY CALCULATION FORM

RADIATION
INCORPORATED

DATE: _____

PROJECT NO. 1858

UNIT TITLE: Digital Multiplexer Gate

S/N: _____

COMPONENT	N	* $\lambda \times 10^{-5}$	N $\lambda \times 10^{-5}$	REMARKS
Resistors, MIL-R-11C	105	.001	.105	< 10% Stress
Transistor (Si)	15	.020	.300	< 10% Stress
Diode (Si)	210	.010	2.100	< 10% Stress

* BASED ON TEMPERATURE AND STRESS

2.505

= λ TOTAL (%/1000 HOURS)

= MTBF (HOURS)

APPENDIX V

MOSFET SPECIFICATION

RAD 106510 (Semiconductor Device Set)

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106510	REVISIONS									
	SYM	DESCRIPTION	DATE	APPROVED						
	A	CHG BY JRG 12/2/64 CHK BY MB 12/2/64 ECO NO. 16494 A	12/1/64	J. Wolcott						
	(1) Revised per ECO, sheets 1, 2, 3, 4, 5, 6, 7, 9									
DESCRIPTION: Five-channel integrated MOS - FET Analog Multiplexer. NOTE: When referring to Radiation part number, specify drawing number and pertinent dash number. If there are any deviations between this specification and the manufacturer's part, this specification shall have precedence. This Detailed Part Specification (DPS), in conjunction with General Specification(104118) provides a complete procurement specification for items described herein.										
Fairchild Semiconductor Corp Mountainview, California					07263					
MANUFACTURER					CODE IDENT. NO.		PART NO.		REMARKS	
PROCUREMENT SPECIFICATION										
REVISION INDEX	SHEET	1	2	3	4	5	6	7	8	9
REV	REV	A	A	A	A	A	A	A	A	A
DRAWN BY J. Blaker 8/31/64		 RADIATION INCORPORATED / MELBOURNE, FLORIDA								
CHECKED BY J. Blaker 8/31/64										
ENGINEER J. Blaker 9/14/64										
PROJECT ENGINEER J. Blaker 9/11/64										
STANDARDS ENGINEER, RCL J. Blaker 9/2/64										
APPROVAL H. C. Blaker 9/19/64		CODE IDENT NO.		SIZE		106510			REV A	
91417		A								
SCALE		NEXT DWS					SHEET		1 OF 9	

R-460

1. SCOPE

This document specifies the requirements for a high-reliability five-gate monolithic MOS field effect device for use in space electronic equipment.

2. REFERENCED DOCUMENTS

RAD dwg 104113 Transistor, General Specification for
MIL-STD 105 Sampling Procedures & Tables for Inspection by Attributes

3. REQUIREMENTS

3.1 Electrical Requirements.

3.1.1 Absolute Maximum Ratings* (Ref 6.1)

Source to Drain Voltage, V_{SDS} (body tied to source):	-40 volts
Drain to Source Voltage, V_{DSS} :	-40 volts
Gate to Source Voltage, V_{GSS} :	+50 volts, $V_{DS} = 0$
Gate to Source Voltage (transient), V_{GSS} :	+50 volts, $V_{DS} = 0$
Total Dissipation, P_C : @25°C Ambient:	150 mw
Maximum Junction Temperature, Operating:	+175°C
Storage:	+200°C

3.1.2 Recommended Maximum Ratings* (Ref 6.1)

Source to Drain Voltage, V_{SDS} (body tied to source):	-25 volts
Drain to Source Voltage, V_{DSS} :	-25 volts
Gate to Source Voltage, V_{GSS} :	+25 volts,
Gate to Source Voltage (transient), V_{GSS} :	-45 volts
Total Dissipation, P_C : @25°C ambient:	45 mw

3.2 Mechanical Requirements.

The units shall be packaged in a fourteen pin flat-pack as shown in Figures 2 and 3.

3.3 Marking.

Each unit shall be marked with the Radiation part number, serial number, lot number, and vendor symbol or trademark as minimum markings.

3.4 Lead Material. Material shall be Kovar with gold plate, 200 u-in. $\pm$ 100 u-in.

4. QUALITY ASSURANCE PROVISIONS

4.1 Qualification Inspection (Ref GPS 4.4.5)

*Body lead shorted to source lead unless otherwise noted.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES FRACTIONS $\pm$ 1/64; ANGLES $\pm$ 1° DECIMALS: 3 PLACE $\pm$.005 2 PLACE $\pm$.02	 RADIATION INCORPORATED CODE IDENT NO. 91417	SIZE		REV
		A	106510	A
		SHEET 2		

R-460-1

4.1.1

Group 1 - All Units (85)

Parameters shall be measured at 25°C ±2°C, unless otherwise specified. No failures allowed for parameters so noted; total of 1 failure allowable for all other tests noted by numeral 1 in Table I. Body lead is shorted to source lead unless otherwise noted.

TABLE I

Test	Symbol	Conditions	MIN	MAX	Units	Failures Allowed
Drain to Source Breakdown Voltage	BV_{DSS}	$V_{GS} = V_{BS} = 0$ $I_D = 1 \mu a$ (Ref 6.3)	-40		volts	0
Source to Drain Breakdown Voltage	BV_{SDS}	$V_{GD} = V_{BD} = 0$, $I_S = 1 \mu a$	-40		volts	0
Gate Threshold Voltage	V_{GST}	$I_D = 10 \mu a$, $V_{GS} = V_{DS}$, $V_G = 0$	-3	-6	volts	1
Drain to Source Leakage Current	I_{DSS1}	$V_{GS} = 0$, $V_{DS} = -25V$ (Ref 6.3)		0.1	na	0
Drain to Source Leakage Current	I_{DSS2}	$V_{GS} = 0$, $V_{DS} = -25V$, $T_A = 85^\circ C$ (Ref 6.3)		5.0	na	0
Drain-Body and Source Body Leakage Current	I_{BD+BS}	$V_{GS} = V_{DS} = 0$, $V_B = +25V$ $T_A = +85^\circ C$		10	na	1
Gate Input Resistance	R_{IS}	$V_{GS} = -20V$, $V_{DS} = 0$	10^{13}		ohms	1
Dynamic Drain Resistance	r_d	$V_{GS} = -20V$, $V_{DS} = 0$		1500	ohms	1
ON Current	I_{SDS}	$V_{DS} = -5V$, $V_{GS} = -20V$	1.0		ma	1
Source Capacity (Source-Drain + Source-Body + Source-Gate)	C_s	$V_{DG} = V_{DB} = V_{BG} = 0$, $V_S = -5V$		2.0	pf	1
Drain Capacity (Drain-Source + Drain-Body + Drain-Gate)	C_d	$V_{GS} = V_{SB} = V_{GB} = 0$ $V_D = -5V$		2.0	pf	1
Drain to Source Capacity	C_{ds}	$V_B = V_G = +8V$, $V_{DS} = 0$		2.0	pf	1
Gate Capacity	C_g	$V_G = +8V$, $V_{DS} = V_{DB} = V_{SB} = 0$		3.0	pf	1

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES.

TOLERANCES

FRACTIONS: $\pm 1/64$; ANGLES: $\pm 1^\circ$
DECIMALS: 3 PLACE: $\pm .008$
2 PLACE: $\pm .02$



RADIATION
INCORPORATED

CODE IDENT NO. 91417

SIZE

A

106510

REV

A

SHEET 3

4.1.2 Group II (Ref GPS 3.5) - 45 Units

TABLE II

4.1.2.1 Subgroup II (a) - 20 Units

GPS Test Para	Test	Failures Allowed
4.6.20.1	Temperature Cycling	1
4.6.20.2	Thermal Shock	
4.6.18.3	Hermetic Seal	
4.6.25	Vibration Variable Frequency (40G level)	
4.1.2.2	Subgroup II (b) - 25 Units	1
4.6.32	Storage Life, 150°C	
4.6.20.2	Thermal Shock	
4.6.23	Shock	
4.6.22.1	Acceleration	

4.1.2.3 Group II Post Test End Points (Conditions as specified in Para 4.1.1).

Drain to Source Leakage Current, I_{DSS1} : ≤ 0.1 na MAX

Drain-Body and Source-Body Leakage Current, I_{BD+BS} : ≤ 10.0 na MAX

Gate Threshold Voltage, V_{GST} : $-3.0V \leq V_{GST} \leq -6.0$ volts

4.1.3 Group III - 40 Units

Operating Life Test per Figure 1 @ $T_A = 100^\circ\text{C}$, free air Ref GPS 4.6.33

4.1.3.1 Group III Post Test End Points (Conditions as specified in Para 4.1.1)

Drain to Source Leakage Current, I_{DSS1} : ≤ 1.0 na MAX

Drain-Body and Source-Body Leakage Current, I_{BD+BS} : ≤ 10.0 na MAX

Gate Threshold Voltage, V_{GST} : $-3.0V \leq V_{GST} \leq -6.0$ volts

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES.

TOLERANCES

FRACTIONS $\pm 1/64$; ANGLES $\pm 1^\circ$
DECIMALS, 3 PLACE $\pm .005$
2 PLACE $\pm .02$



RADIATION
INCORPORATED

CODE IDENT NO. 91417

SIZE

A

106510

REV

A

SHEET 4

R-460-1

- 4.2 Acceptance Inspection.
- 4.2.1 Screening (Ref GPS 3.5 and 4.5.1) Read and Record

TABLE III

GPS Test Para	Test or Conditioning	Conditions	Acceptance Criteria
4.6.18.3	Hermetic Seal (Ref 6.2)	Helium or Radiflo	$\leq 10^{-6}$ cc/sec
4.6.22.2	Acceleration (Ref 6.2) in Y1 axis only		No shorts or opens
4.6.1	Visual and Mechanical		
	Drain to Source Leakage Current, I_{DSS1}	$V_{GS}=0, V_{DS}=-25V$ (Ref. 6.3)	≤ 0.1 na
	Gate Threshold Voltage, V_{GST}	$I_D=10 \mu A, V_{GS}=V_{DS},$ $V_G=0$	-3.0 V MIN -6.0 V MAX
	Aging, 336 hours	$V_G=V_B=0, T_A=100^\circ C$ $V_S=V_D=-30$ volts	
	Drain to Source Leakage Current, I_{DSS1}	$V_{GS}=0, V_{DS}=-25 V$ (Ref 6.3)	≤ 0.1 na
	Gate Threshold Voltage, V_{GST}	$I_D=10 \mu A, V_{GS}=V_{DS},$ $V_G=0$	-3.0 V MIN -6.0 V MAX

- 4.3 Group A Inspection (Ref GPS 3.4 and 4.5.2.1) Read and Record
- 100% Testing. Reject all units failing to comply with the requirements of Table IV.

TABLE IV

Test	Symbol	Conditions	MIN	MAX	Units
Drain to Source Breakdown Voltage	BV_{DSS}	$V_{GS}=V_{BS}=0, I_D=1 \mu A,$ (Ref 6.3)	-40		volts
Source to Drain Breakdown Voltage	BV_{SDS}	$V_{GD}=V_{BD}=0, I_S=1 \mu A$	-40		volts
Gate Input Resistance	R_{IS}	$V_{GS}=-20V, V_{DS}=0$	10^{13}		ohms

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES.

TOLERANCES

FRACTIONS: $\pm 1/64$; ANGLES: $\pm 1^\circ$
DECIMALS: 3 PLACE: $\pm .005$
2 PLACE: $\pm .02$



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CODE IDENT NO. 91417

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TABLE IV (continued)

Test	Symbol	Conditions	MIN	MAX	Units
Dynamic Drain Resistance	r_d	$V_{GS} = -20V, V_{DS} = 0$		1500	ohms
ON Current	I_{SDS}	$V_{DS} = -5.0V, V_{GS} = -20V$	1.0		ma

4.4 Group B Inspection (Ref GPS 3.4 and 4.5.2.2)

Sample size shall correspond to an AQL of 0.065, P(A) ≥ 0.95 and a LTPD of 1.5, P(A)=0.10 as defined in MIL-STD-105.

TABLE V

Test	Symbol	Conditions	MIN	MAX	Units
Drain to Source Leakage Current	I_{DSS2}	$V_{GS} = 0, V_{DS} = -25V,$ $T_A = +85^\circ C$ (Ref 6.3)		5.0	na
Drain-Body and Source-Body Leakage Current	I_{BD+BS}	$V_{GS} = V_{DS} = 0, V_B = +25V$ $T_A = +85^\circ C$		10.0	na
Source Capacity (Source-Drain + Source-Body + Source-Gate)	C_s	$V_{DG} = V_{DB} = V_{BG} = 0$ $V_S = -5V$		2.0	pf
Drain Capacity (Drain-Source + Drain-Body + Drain-Gate)	C_d	$V_{GS} = V_{SB} = V_{GB} = 0$ $V_D = -5V$		2.0	pf
Drain-Source Capacity	C_{ds}	$V_B = V_G = +8V, V_{DS} = 0$		2.0	pf
Gate Capacity	C_g	$V_G = +8V, V_{DS} = V_{DB} = V_{SB} = 0$		3.0	pf

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES.

TOLERANCES

FRACTIONS $\pm 1/64$; ANGLES $\pm 1^\circ$
 DECIMALS: 3 PLACE $\pm .005$
 2 PLACE $\pm .02$

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4.5 Group C Inspection (Ref GPS 3.5 and 4.5.2.3)

One defect allowed in each subgroup.

TABLE VI

GPS Test Para	Test or Examination	Sample Size	Symbol	Limits		Units
				MIN	MAX	
4.5.1	Subgroup I	15				
4.6.20.1	Temperature Cycling		I_{DSS1}		0.1	na
4.6.20.2	Thermal Shock					
4.6.25	Vibration, Var Freq(50 G)		I_{BD+BS}		10.0	na
4.6.18.3	Hermetic Seal (MIL-STD-202, Method 112, Cond B)		V_{GST}	-3.0	-6.0	volts
4.5.2	Subgroup II	25				
4.6.32	Storage Life, 150°C		I_{DSS1}		1.0	na
4.6.20.2	Thermal Shock					
4.6.23	Shock		I_{BD+BS}		10.0	na
4.6.22.1	Acceleration		V_{GST}	-3.0	-6.0	volts
4.5.3	Subgroup III	25				
4.6.33	Operating Life (per Fig. 1, 1000 hours) $T_A = 100^\circ C$		I_{DSS1}		1.0	na
			I_{DSS2}		10.0	na
			I_{BD+BS}		10.0	na
			V_{GST}	-3.0	-6.0	volts

5. PREPARATION FOR DELIVERY

5.1 Ref GPS 5.0

5.2 Units shall be packed in containers marked "MOS Field Effect Device-Special Handling Required".

6. NOTES

6.1 Absolute maximum ratings are those ratings which if exceeded may impair the serviceability of the device. Recommended maximum ratings are the maximum ratings recommended for equipment reliability requirements.

6.2 Performance of these tests during normal manufacturing and testing shall be considered conformance to these requirements.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES FRACTIONS: $\pm 1/64$; ANGLES: $\pm 1^\circ$ DECIMALS: 3 PLACE: $\pm .005$ 2 PLACE: $\pm .02$	 RADIATION INCORPORATED CODE IDENT NO. 91417	SIZE A	106510	REV A
		SHEET 7		

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6.3

The five common drain currents may be averaged for maximum leakage. Do not exceed 40 volts during the test for breakdown voltage.

6.4

All transistors must be on common substrate utilizing metallized interconnections except for singular bond connections to pins.

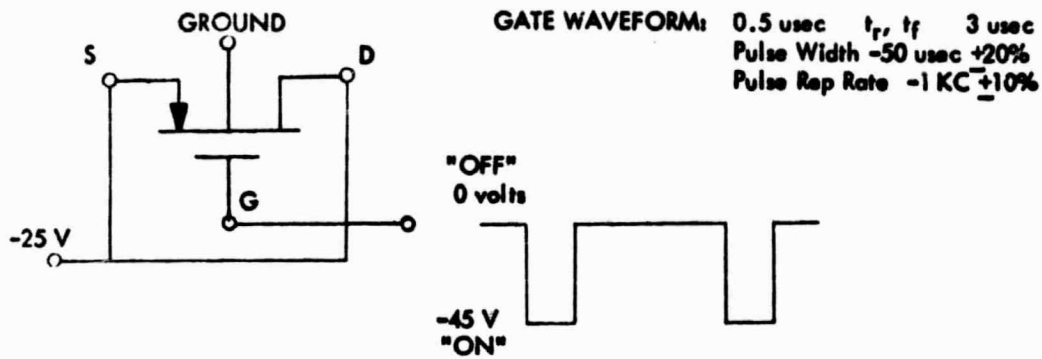


Figure 1 - Operating Life Conditions

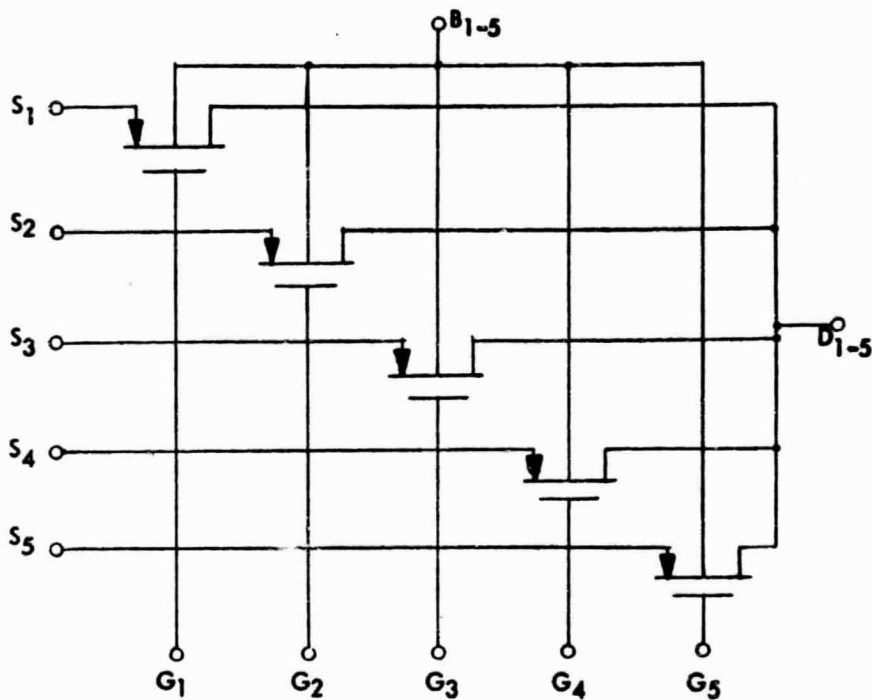


Figure 2(a) = Electrical Configuration

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES.

TOLERANCES

FRACTIONS: $\pm 1/64$; ANGLES: $\pm 1^\circ$
DECIMALS: 3 PLACE $\pm .003$
2 PLACE $\pm .02$



RADIATION
INCORPORATED

CODE IDENT NO. 91417

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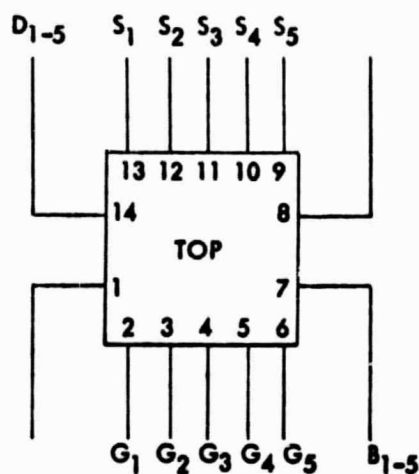
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Pins 1 and 8 not connected.

Figure 2(b) Mechanical Configuration

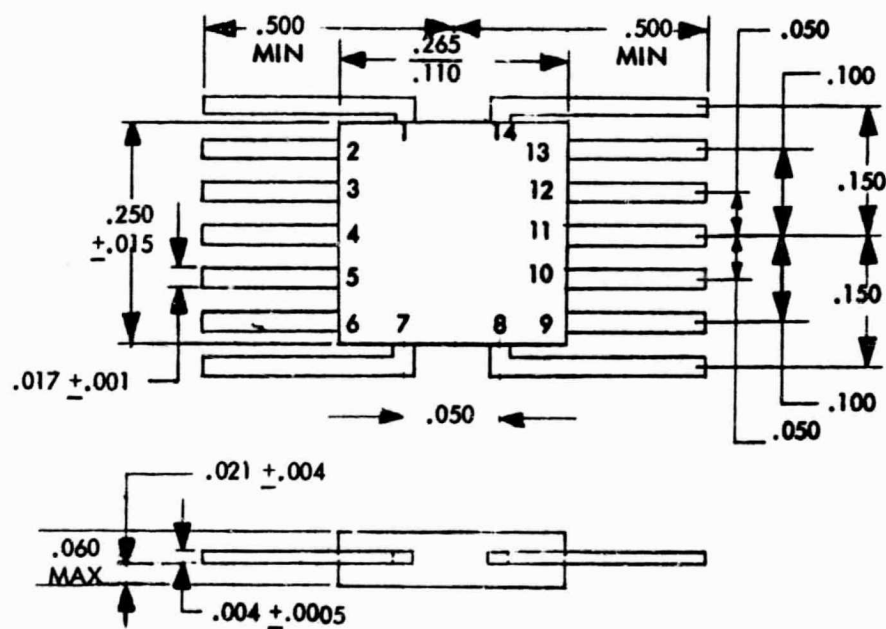


Figure 3 Outline Drawing
All leads are evenly spaced.

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES.

TOLERANCES

FRACTIONS: 1/64; ANGLES: 1°
DECIMALS: 3 PLACE: .005
2 PLACE: .02



RADIATION
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CODE IDENT NO. 91417

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APPENDIX VI

BEACON TRANSMITTER MODULATION SIGNAL COMPATIBILITY

1.0 GENERAL

This report is submitted to clarify the capability of the Hughes Nimbus Beacon Transmitter pertaining to the different types of modulation signals that are now under consideration for use by the Nimbus Telemetry Group. Where the transmitter is not compatible with a given modulation signal, necessary modification to the transmitter is noted. Two modulation signals are considered. These two signals are NRZ PCM and SPLIT PHASE PCM.

2.0 PROPOSED MODULATION SIGNALS

The two proposed modulation signals are presented below for reference.

BIT	1	1	1	0	1	0	0	0	1
	1	1	1	1	1	1	1	1	1

SPLIT PHASE
Waveform



NRZ
Waveform



If either signal is used, and realtime data is transmitted, the telemetry signal is to be algebraically added to the standard time code signal which is amplitude modulated onto a 10 KC square wave. If the recorded transmission mode is used, there is a 30:1 increase in frequency of the bit rate.

3.0 TRANSMITTER COMPATIBILITY

The transmitter in its present form will pass the uppermost frequency to be transmitted from either of the two modulation waveforms in the

direct or record mode of transmission. The assumption is made here that the first and third harmonics of the 15 KC wave in the record mode of the split phase wave are sufficient for good data transmission. Addition of the split phase waveform to the time code should present no problem as the frequencies do not overlap. No low frequency coupling problem exists with the split phase PCM signal. Use of the NRZ code with the transmitter will present a problem in the transmitter and in the ground station. The transmitter must be made to transmit DC in order to pass all possible data that may be generated. The ground station must also be DC coupled to pass this data. DC coupling in the ground station will allow DC distortion terms and other low frequency mixing products that are generated in the transmitter when time code and NRZ are added to decrease the received signal to noise ratio. The magnitude of this S/N degradation will depend on the transmitter distortion.

The transmitter will require extensive redesign in order to pass DC modulation. With the present method of modulation, there will be a reduction in efficiency if a DC capability is achieved. Modifications must be made to the transmitter modulator and at least two of the RF stages in order to obtain DC capability and retain the present power output.

4.0 SUMMARY

The Hughes Nimbus Beacon Transmitter in the present form is capable of handling the proposed split phase PCM signal in the real-time or the record mode. For use with NRZ data, the transmitter will require extensive modification.

APPENDIX VII

"A" UNIT MODULATOR MODIFICATION

APPENDIX VII

"A" Unit Modulator Modification

1.0 Introduction

1.1 In addition to the study of split phase recording which is covered in the main body of this report, a short study was conducted to determine what improvement could be made in the characteristics of the playback signal by modifying the character of the A unit modulator signal prior to the record process.

2.0 Modification of Modulator Gating Level

2.1 As stated previously in the main report, the "A" unit data signal consists of a gated 500 cps sine wave. Each gated cycle of the sine wave represents a "0" in the output binary code. The sine wave at present is gated at the cosine or 90° point rather than at the zero crossover point due to the fact that the record head differentiates the input signal. An illustration of this signal is shown in Figure A1. The principal difficulty with the present playback signal is caused by differentiation of the sharp transition in the modulator signal from the OFF level to the cosine level. This results in an apparent overshoot on the leading and trailing edges of the playback sine wave signal as shown in Figure A2 and A3. It can also be noted in these figures that the first and last half cycle of a series of sine waves are lower in amplitude than the rest of the signal.

2.2 In order to reduce the effects of the transition from the OFF level to the signal level, a D.C. bias level was applied to the modulator transformer T-1 in module I6. This was accomplished by connecting a resistor of approximately 180K between the transformer center tap and the -24.5 volt supply. It also requires the reversal of the transformer primary or secondary leads to provide the necessary phase relationship for use with a negative bias. The resultant modulator output with the bias level set at 75% of the peak-to-peak signal is shown in Figure A4. This signal was recorded and the playback signal is shown in Figures A5 and A6. This playback signal can be seen to differ from the original signal in the amount of overshoot and the signal symmetry. The positive half cycles are now of equal amplitude. The negative half cycles are of smaller amplitude on the first half cycle in a series and reach a maximum amplitude of approximately 90% of that achieved by the positive half cycles.

2.3 The gating OFF level was then changed to the 67% point as shown in Figure A7 and a recording was made of this signal. The playback from this recording is shown in Figures A8 and A9. The resulting waveform shows a slight increase in overshoot component and a decrease in amplitude of the first positive half cycle. The negative half cycles now approach 95% of the positive half cycles.

2.4 Due to the fact that the modulator output is no longer symmetrical about the OFF level, the "A" Unit Real Time output from I-7 will require an increase in size of the coupling capacitor to the time code amplifier to prevent differentiation of the Real Time signal.

2.5 Some distortion of the playback signal is due to noise on the record signal which is apparently picked up in the tape transport unit during each transition of the two 100 cps motor drive signals. An illustration of this noise is shown in Figure A10. Figure A11 shows an undistorted record signal across a dummy head. Figure A12 shows the effects of the noise on the playback signal. The amplitude of this noise is about 6% of the peak-to-peak amplitude of the record signal. Filtering of this noise would be difficult due to the fact that the maximum noise components have a frequency close to the 500 cps record signal.

3.0 Conclusions

3.1 The playback waveform appears to offer some improvement over the present waveform when the OFF level of the modulator is maintained at approximately 70% of the maximum peak-to-peak amplitude of the gated sine wave. Full evaluation of this improvement should be made by the ground station on a comparative basis with the present type of waveform. Since the "A" Real Time signal is also changed, this fact should also be taken into account as to the effect on the ground station operation.

3.2 The physical changes to the Telemetry Electronics to accomplish this modification would be quite simple. One additional resistor would be added to module I7 and the coupling capacitor C5 in module I7 would be increased in size to 2.2 uf. Transformer T1 in module I6 would also require a reversal of leads 1 and 2.

MODULATOR OUTPUT

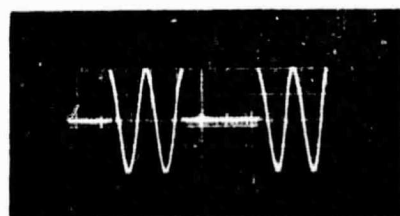


Fig. A1 (50%)

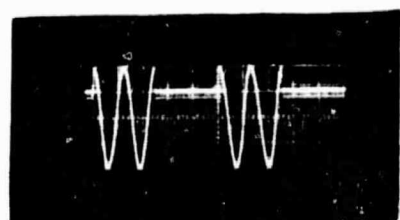


FIG. A4 (75%)

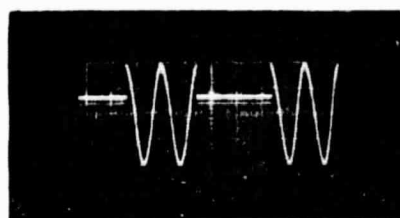


FIG A7 (67%)

PLAYBACK SIGNAL

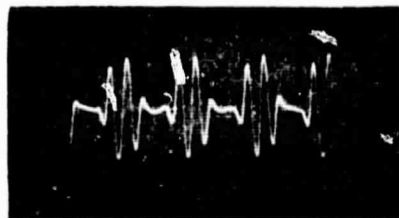


FIG. A2

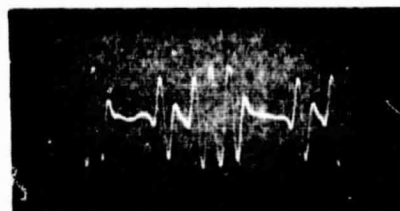


FIG. A3

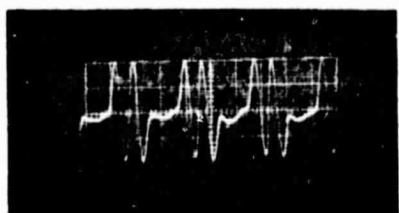


FIG. A5

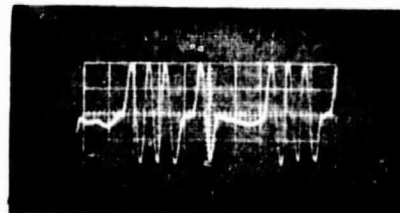


FIG. A6

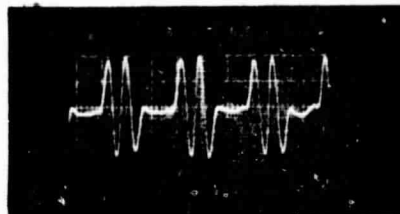


FIG. A8



FIG. A9

RECORD HEAD SIGNAL

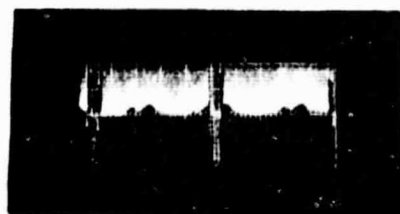


FIG. A10

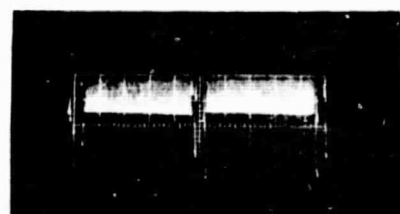


FIG. A11

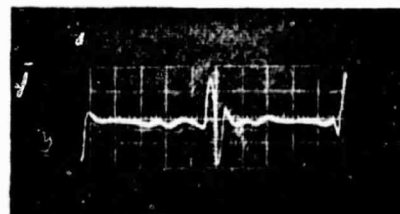


FIG. A12

47415

PLAYBACK

APPENDIX VIII

DESIGN STUDY TEST TAPES

NIMBUS DESIGN STUDY TEST TAPES

Three MINCOM test tapes for checkout and testing of the NIMBUS ground station compatibility with the new PCM format were prepared utilizing modified Multicoder SN004, clock Unit SN 7, Telemetry Electronics SN005 and airborne Tape Transport SN2. The format of each tape included a 62.5 word length subframe synchronous with the clock time code frame, a twenty bit subframe synchronization word, which includes subframe identification, time code data through tens of hours, and digital information channels. Location of the above information in the format is shown in Table 1 and Figure 011. Composition of the sync word is shown in Figure 4.1.

Test Tape #1 was made using the gated sine wave modulation employed in all previous systems. The digital and analog channel input format is shown in Table 2. All subcommutated channels other than those indicated in the format had an analog input of 5.10 volts. (Binary readout of 1100110). The tape contains one 220 sec. segment of playback signal from the airborne recorder. This signal occurs approximately two minutes from the start of the tape. The rest of the tape time is occupied by Time Code and "A" Real Time signals containing the same format as the playback data.

Test Tape #2 was made using the proposed split phase (M) code modulation. This tape contains three playback segments. The first playback segment has a format in which all analog channel words have a readout of 1110100 and all digital words (each word containing seven channels) had a readout of 0110011. The second playback segment has a format identical to that of Test Tape #1. The third playback segment has a format identical to that of segment two except that subcommutated channels other than those shown in the format table had an analog input of 0.00 volts. Each playback segment is preceded and followed by "A" Real Time data containing the same format as the enclosed playback segment.

Tape #3 was continuous tape of "A" Real Time data utilizing the split phase (M) code. The 10 KC time code signal is not mixed with Real Time signal on this tape. All analog channels in this format are 0.00 volts. Digital channels are as shown in Table 2.

Test Tape #1 was prepared primarily to check out the system modification which synchronized the PCM to the Master Clock, and the addition of the digital channels including time

code data. As shown in Table 2, the digital channel words include a word in which all seven digits in the word are "0" and words in which all seven digits are "1". These are worst case condition digital words. The time code words values are controlled by the master clock output and are read out during subframe one. The time code count can be verified by checking to see that the count advances sixteen seconds each readout.

Test Tape #2 was prepared primarily for checkout of the ground station compatibility with the split phase (M) code modulation and for comparison of this code with the gated sine wave modulation as to their respective signal to noise ratio capabilities.

Test Tape #3 was made for preliminary checkout of ground station logic modifications. The large number of channels with "0" code on them is to simulate worst case conditions for bit synchronization.

TABLE 1

<u>Subframe</u>	<u>Subframe Time Slot</u>	<u>Information</u>
All	62.5	Sync Word
	1	Sync Word
	2	Sync Word and Subframe Count
	5	Digital Channels 1-7
	13	Digital Channels 8-14
	21	Digital Channels 15-21
	29	Digital Channels 22-28
	37	Digital Channels 29-35
	45	Digital Channels 36-42
	53	Digital Channels 43-49
All	61	Digital Channels 50-56
1	4	Time Code - Units seconds
1	12	Time Code - Tens seconds
1	19	Time Code - Units minutes
1	23	Time Code - Tens minutes
1	31	Time Code - Units hours
1	36	Time Code - Tens hours
2	4	Digital Channels 57-63
2	12	Digital Channels 64-70
2	19	Digital Channels 71-77
2	23	Digital Channels 78-84 (storage)

TABLE 2

TEST TAPE FORMAT TAPE #1

<u>SUBFRAME</u>	<u>TIME SLOT</u>	<u>DIGITAL READOUT</u>	<u>ANALOG</u>	<u>CHANNEL</u>
A11	5	0 0 0 0 0 0 0	0.00	Digital 1-7
	6	0 0 0 0 0 1 1	.15	
	9	0 0 0 1 0 0 0	.40	
	10	0 0 0 1 1 0 0	.60	
	13	0 0 1 0 0 0 1	.85	Digital 8-14
	14	0 0 1 0 1 0 1	1.05	
	17	0 0 1 1 0 1 0	1.30	
	18	0 0 1 1 1 1 0	1.50	
	21	0 1 0 0 0 1 1	1.75	Digital 15-21
	22	0 1 0 0 1 1 1	1.95	
	25	0 1 0 1 1 0 0	2.20	
	26	0 1 1 0 0 0 0	2.40	
	29	0 1 1 0 1 0 1	2.65	Digital 22-28
	30	0 1 1 1 0 0 1	2.85	
	33	0 1 1 1 1 1 0	3.10	
	34	1 0 0 0 0 1 0	3.30	
	37	1 0 0 0 1 1 1	3.55	Digital 29-35
	38	1 0 0 1 0 1 1	3.75	
	41	1 0 1 0 0 0 0	4.00	
	42	1 0 1 0 1 0 0	4.20	
	45	1 0 1 1 0 0 1	4.45	Digital 36-42
	46	1 0 1 1 1 0 1	4.65	
	49	1 1 0 0 0 1 0	4.90	

TABLE 2 CONTINUED

TEST TAPE FORMAT TAPE #1

<u>SUBFRAME</u>	<u>TIME SLOT</u>	<u>DIGITAL READOUT</u>	<u>ANALOG</u>	<u>CHANNEL</u>
All	50	1 1 0 0 1 1 0	5.10	
	53	1 1 0 1 0 1 1	5.35	Digital 43-49
	54	1 1 0 1 1 1 1	5.55	
	57	1 1 1 0 1 0 0	5.80	
	58	1 1 1 1 0 0 0	6.00	
	61	1 1 1 1 1 0 0	6.20	Digital 50-56
All	62	1 1 1 1 1 1 1	6.35	
2	4	1 1 1 1 1 1 1	6.35	Digital 57-63
2	12	1 1 1 1 1 1 1	6.35	Digital 64-70
2	19	1 1 1 1 1 1 1	6.35	Digital 71-77
2	23	1 1 1 1 1 1 1	6.35	Digital 78-84

Subcommutated channels not shown have a value of 5.10 for tape #1 and tape #2 segment 2 and a value of 0.00 for tape #2 segment 3.

APPENDIX IX

SPECIFICATION, INTEGRATED DIGITAL GATE

RAD 106626

"REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR."

REVISIONS														
SYM	DESCRIPTION	DATE	APPROVED											
CHG BY	CHG BY	ECO NO.												
DESCRIPTION: Four-Input Integrated circuit digital gate. NOTE: When referring to Radiation part number, specify drawing number and pertinent dash number. If there are any deviations between this specification and the manufacturer's part, this specification shall have precedence. This Detail Part Specification (DPS), together with General Specification 104118, forms a complete procurement specification for the item(s) listed herein.														
MANUFACTURER		CODE IDENT. NO.	PART NO.	REMARKS										
PROCUREMENT SPECIFICATION														
REVISION INDEX	SHEET													
	REV													
DRAWN BY <i>[Signature]</i> 12/8/64 CHECKED BY <i>[Signature]</i> 12/10/64 ENGINEER <i>[Signature]</i> 12-9-64 PROJECT ENGINEER <i>[Signature]</i> 12-9-64 STANDARDIZATION <i>[Signature]</i> 12-10-64		 RADIATION INCORPORATED MELBOURNE, FLORIDA												
APPROVAL <i>[Signature]</i> 12-10-64 APPROVAL		TITLE INTEGRATED CIRCUIT DEVICE												
		CODE IDENT. NO.	SIZE	REV										
		91417	A											
		106626												
SCALE		NEXT DWS	SHEET 1 of 28											
		1858												

1.0 GENERAL

1.1 Scope

This specification covers the requirements for a high-reliability digital gate for use in space electronic equipment.

1.2 Description

The integrated circuit digital gate consists of two(2) flat packs, each having four digital inputs, four digital outputs, one strobe input, one power input, and two (2) tie point leads at the junction of the driver transistor and collector resistors. (See Figure 1)

2.0 APPLICABLE DOCUMENTS

The following specifications and standards, of current issue, form a part of this specification to the extent specified herein.

Military:

MIL-STD-202

Test Methods for Electronic and Electrical Component Parts

MIL-STD-750

Test Methods for Semiconductor Devices

NASA:

NPC 200-3

Inspection System Provisions for Suppliers of Space Materials,
Components and Services

Radiation:

Dwg 104118

Transistor, General Specification

Dwg 407654

Header-Ltd, Flat Package

3.0 REQUIREMENTS

3.1 Electrical Requirements

3.1.1 The integrated circuit devices shall meet the requirements of this specification throughout all environments specified herein.

3.1.2 All of the following electrical specifications are general guidelines to establish design criteria for the part. Final acceptance of any device will be dependent upon performance to the parameter test of Para 3.1.2.1, the functional test of Para 3.1.2.2 and Appendix I.

3.1.2.1 Parameter Tests

The following parameter checks are necessary to insure that the circuit meets customer interface specifications.

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES.

TOLERANCES

FRACTIONS: $\pm 1/64$; ANGLES: $\pm 1^\circ$
DECIMALS: 3 PLACE: $\pm .008$
2 PLACE: $\pm .02$



RADIATION
INCORPORATED

CODE IDENT NO. 91A17

SIZE

A

106626

REV

SHEET 2

R-460-1

(1) Diode Reverse Leakage, $I_R = 200$ na max at
 $V_R = 24$ volts and $T_A = 65^\circ\text{C}$

(2) Reverse Voltage Base to Collector, $BV_{BC} = 40$ volts min,
 $I_R = 100$ ua and $T_A = 25^\circ\text{C}$

3.1.2.2 Functional Tests

Each integrated circuit is to be checked functionally over the operating range of -10°C to 65°C , according to the test procedure in Appendix II. These tests are "Go" "No-Go" tests to determine proper circuit operation in the PCM system.

3.1.3 Temperature Range for Proper Operation of Circuits: -10°C to $+65^\circ\text{C}$

3.1.4 Transistors

Forward base-collector voltage drop,
 $V_{BCF} = 0.8\text{V}$ max at 1 ma and 25°C

Forward base-emitter voltage,
 $V_{BE1} = 0.61\text{V}$ min at 1 ma and $+65^\circ\text{C}$

Forward base-emitter voltage,
 $V_{BE2} = 1.1\text{V}$ max at 1 ma and -10°C

Saturated collector-emitter voltage,
 $V_{CE1(\text{sat})} = 0.5\text{V}$ min at $I_B = 0.1$ mA, $I_C = 1.0$ mA, $T_A = -10^\circ\text{C}$

Saturated collector-emitter voltage,
 $V_{CE2(\text{sat})} = 3.0\text{V}$ max at $I_B = 1.0$ mA, $I_C = 10$ mA, $T_A = +65^\circ\text{C}$

DC current gain,
 $HFE_1 = 20$ min at $I_C = 1$ mA, $V_{CE} = 5.0\text{V}$, $T_A = -10^\circ\text{C}$

DC current gain,
 $HFE_2 = 200$ max at $I_C = 1$ mA, $V_{CE} = 5.0\text{V}$, $T_A = +65^\circ\text{C}$

Leakage current,
 $I_{CBO} = 50$ nanoamps max at 24V and 25°C

Peak reverse voltage base-collector,
 $BV_{CBO} = 40$ volts min at 25°C , $I_R = 100$ ua

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES.

TOLERANCES

FRACTIONS $\pm 1/64$; ANGLES $\pm 1^\circ$
DECIMALS: 3 PLACE $\pm .003$
2 PLACE $\pm .02$



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INCORPORATED

CODE IDENT NO. 91417

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3.1.5 Diodes

Forward base-collector voltage drop,
 $V_{BCF} = 0.8$ volts max at $I_F = 1$ mA and 25°C

Reverse voltage base-collector,
 $V_{BC} = 40$ volts min at 25°C , $I_R = 100$ μA

Leakage current,
 $I_L = 200$ nanoamps max at $V_R = 24\text{V}$ and $T_A = 65^\circ\text{C}$

Forward current,
 $I_F = 10$ mA min at 25°C , $V_F = 1.3\text{V}$

3.1.6 Resistors

Nominal resistance is $45\text{K} \pm 20\%$ at 25°C .

The temperature coefficient of resistance is 0.5% per $^\circ\text{C}$ max.

Maximum tolerance is $\pm 30\%$ from -10°C to $+65^\circ\text{C}$.

Capacity per 1000 ohms to "N" isolation region = 2.5 pf max.

Capacity of "N" region to "P" substrate = 40 pf max.

All "N" regions per 45K section must be floating with respect to the other "N" regions.

The parasitic PNP beta from the resistor to the substrate is a maximum of 0.01 at 25°C .

3.1.7 Capacitors - Stray Parasitic

$$C = \frac{2C_0 (\sqrt{V_2 + 1} - \sqrt{V_1 + 1})}{V_2 - V_1}$$

where

C = equivalent capacity

C_0 = zero - volt capacity

V_1 = minimum voltage across C_0

V_2 = maximum voltage across C_0

and values for C_0 are $C_{0b} = 9$ pf max @ 5.0V , $f = 140$ KC

$C_{1b} = 6$ pf max @ 5.0V

$f = 140$ KC

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES FRACTIONS $\pm 1/64$; ANGLES $\pm 1^\circ$ DECIMALS: 3 PLACE $\pm .005$ 2 PLACE $\pm .02$	 RADIATION INCORPORATED CODE IDENT NO. 91417	SIZE A 106626	REV SHEET 4
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Collector of NPN to "P" substrate = 20 pf max @ 5V

"P" resistor material to "N" isolation region = 2 pf/K ohm max.

3.2 Mechanical Requirements

3.2.1 Package

The package housing the integrated circuit chip shall be in accordance with Radiation drawing 407654.

3.2.2 Sealing

All units shall be hermetically sealed and tested for leaks to MIL-STD-202, Method 112, Procedure III.

3.2.3 Identification and Marking

All flat packs shall be marked with a red dot adjacent to Pin #1, serialization, manufacturer's name or symbol and RI part number as minimum requirements, per Para 3.7 of Radiation drawing 104118, except subparagraph 3.7.1.

3.2.4 Array Element Interconnection

Elements within the array are to be connected by means of metallization patterns. No elements shall be interconnected by gold bonding.

3.2.5 External Pin Configuration

The integrated circuit chip shall be connected to the external package leads as shown in Figure 2. Pins 4 and 11 shall be tied together by internal connections.

3.2.6 Workmanship shall conform to the highest available standards.

3.3 Environmental Requirements

Devices procured to this specification shall be capable of performing within specification limits over the range of environments listed below.

3.3.1 Temperature Range

Operating	-10°C to +65°C
Storage	-55°C to +200°C

3.3.2 Humidity

Storage	0 to 100% RH
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UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES FRACTIONS $\pm 1/64$; ANGLES $\pm 1^\circ$ DECIMALS: 3 PLACE $\pm .003$ 2 PLACE $\pm .02$	 RADIATION INCORPORATED CODE IDENT NO. 91417	SIZE		REV
		A	106626	
		SHEET 5		

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3.3.3 Vibration (three mutually perpendicular axis)

Sine 10 to 3000 cps, 40 "G" rms.
Random 10 to 3000 cps, 0.133 g²/cps

3.3.4 Shock (three mutually perpendicular axis)

1500 G half-sine, 0.5 millisecc duration

3.3.5 Acceleration (three mutually perpendicular axis)

20,000 G for 1 minute.

4.0 QUALITY ASSURANCE PROVISIONS

4.1 General

4.1.1 Test Conditions

All tests shall be performed at 25°C $\pm$ 5°C, 50% $\pm$ 20% relative humidity, and ambient barometric pressure, unless otherwise specified.

4.1.2 Definition of Failure

Any device which fails to meet all requirements of this specification shall be considered a failure. Failure of a single device in more than one test or parameter shall constitute a single failure.

4.1.2.1 Failure Reports

All failures during qualification and lot acceptance testing shall be reported on Radiation Form 236. All failures shall be reported within 3 days and a failure analysis report submitted within 10 days to Reliability Engineering, Radiation Systems Division.

4.2 Qualification Test Sequence

4.2.1 Group A - Initial Electrical Parameters

All specimens shall be tested for compliance to the requirements of 3.1.2.

4.2.2 Group B - Environmental Qualification Inspection - 65 Units.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES FRACTIONS $\pm$ 1/64; ANGLES $\pm$ 1° DECIMALS: 3 PLACE $\pm$.005 2 PLACE $\pm$.02	 RADIATION INCORPORATED CODE IDENT NO. 91417	SIZE		REV	
		A	106626		
		SHEET		6	

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TABLE I

104118 Test Para	Test	No. of Defects Allowed
4.2.2.1	Subgroup Ia - 15 Units	1
4.6.20.1	Temperature Cycling	
4.6.20.2	Thermal Shock	
4.6.18.3	Hermetic Seal	
	Terminal Strength (see Note 6.4)	
4.2.2.2	Subgroup Ib - 15 Units	1
4.6.32	Storage Life 200°C	
	T = 1000 hours	
4.2.2.3	Subgroup II - 10 Units	1
4.6.25	Vibration Variable Frequency	
4.6.23	Shock	
4.6.22.1	Acceleration	
4.6.21	Moisture Resistance	
4.2.2.4	Subgroup III - 40 Units	1
4.6.33	Operating Life +65°C (See Note 6.3) T = 5000 hours	

4.2.3 End Points

The following end points shall be performed within 72 hours after completion of each subgroup and at intervals of 100, 250, 500, 1000, and every subsequent 1000 hours ±24 hours of Subgroups Ib and III.

4.2.3.1 Functional Test

Each device shall be checked for performance when tested per Paragraph 3.1.2.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES FRACTIONS: $\pm 1/64$; ANGLES: $\pm 1^\circ$ DECIMALS: 3 PLACE $\pm .000$ 2 PLACE $\pm .02$	 RADIATION INCORPORATED CODE IDENT NO. 91417	SIZE	106626	REV
		A		SHEET 7

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4.3 Acceptance Screening Requirements - 100% Inspection, lot acceptance criteria per Para 4.5.1 and lot acceptance data per Para 4.5.2.6 of 104118.

TABLE II

Ref Para	Test or Conditioning	Conditions	Acceptance Criteria
	Visual & Mechanical		*
3.1.2	Functional Test	+25°C	Para 3.1.2.2
3.2.2	Hermetic Seal	MIL-STD-202, Method 112	10 ⁻⁸ cc/sec
3.3.1	High Temperature Storage	200°C for 168 hours min	Functional test @ +25°C
3.3.5	Acceleration	20,000 G in the "Z" axis (Fig. 2)	No shorts or opens
	Burn-in (Note 6.3)	T _A = 65°C T = 336 hours	Para 3.1.2.2 @ -10°C, +25°C, +65°C, Para 3.1.2.1
	X-Ray (to be performed last)	MIL-STD-202, Method 209	*

* Vendors workmanship standards to be approved by Radiation Systems Division Reliability Section to establish accept-reject criteria.

4.4 Group C - Acceptance Lot Inspection - 25 Units per Lot

TABLE III

104118 Test Para	Test	No. of Defects Allowed
4.4.1	Subgroup I - 10 Units	1
4.6.20.1	Temperature Cycling	
4.6.20.2	Thermal Shock	
4.6.18.3	Hermetic Seal	
4.6.32	Storage Life T _A = 200°C, 1000 hours. Functional Test (Para 3.1.2)	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES.

TOLERANCES

FRACTIONS ± 1/64; ANGLES ± 1°
DECIMALS, 3 PLACE ± .003
2 PLACE ± .02



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TABLE III (cont'd)

104118 Test Para	Test	No. of Defects Allowed
4.4.2	Subgroup II - 15 Units	1
4.6.33	Operating Life +65°C (See Note 6.3) T = 1000 hours	

Functional Test (Para 3.1.2) Measurement to be performed at the times specified in 104118 Para. 4.6.33

4.5 Electrical Test Methods

The electrical tests required by this specification shall be performed in accordance with the test methods specified in MIL-STD-750. In the event of conflict between the specification and MIL-STD-750, the specification shall govern.

4.6 Environmental Tests

The environmental requirements specified herein refer to those tests as specified in MIL-STD-750 or Radiation drawing 104118 to the extent specified herein.

5.0 PREPARATION FOR DELIVERY

N/A

6.0 NOTES

6.1 Test data shall be permanently recorded in final form at the time of measurement.

6.2 A test procedure which shall include a test equipment index shall be submitted and approved prior to proceeding with qualification testing.

6.3 Life Test Conditions

The units shall be subjected to a simulated switching operation which will provide a stress on the device equal to that of the actual operation.

6.3.1 During the operating life test, the input lines shall be bussed together to form a single input, and the output lines shall be bussed together to form a single output. Switching will be performed at a 120 cps rep rate. Care will be taken to ensure that the average stress is equally applied to all gates.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES FRAC. - 1/64; ANGLES ± 1° DECIM. 3 PLACE ± .008 2 PLACE ± .02	 RADIATION INCORPORATED CODE IDENT NO. 91A17	SIZE		REV
		A	106626	
		SHEET 9		

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6.3.2 Figure 1 shows a typical schematic

6.4 Terminal Strength

Leads must be able to withstand four (4) 45° arc cycles of the case using a 2 oz ± 0.1 oz weight on the lead under test. The 45° arc cycles shall be in the 90° quadrant adjacent to the bottom of the header. The rate of bending shall be uniform and no faster than one (1) cycle/second.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES FRACTIONS $\pm 1/64$; ANGLES $\pm 1^\circ$ DECIMALS: 3 PLACE $\pm .000$ 2 PLACE $\pm .02$	 RADIATION INCORPORATED	SIZE	106626	REV
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CODE IDENT NO. 91417		SHEET 10		

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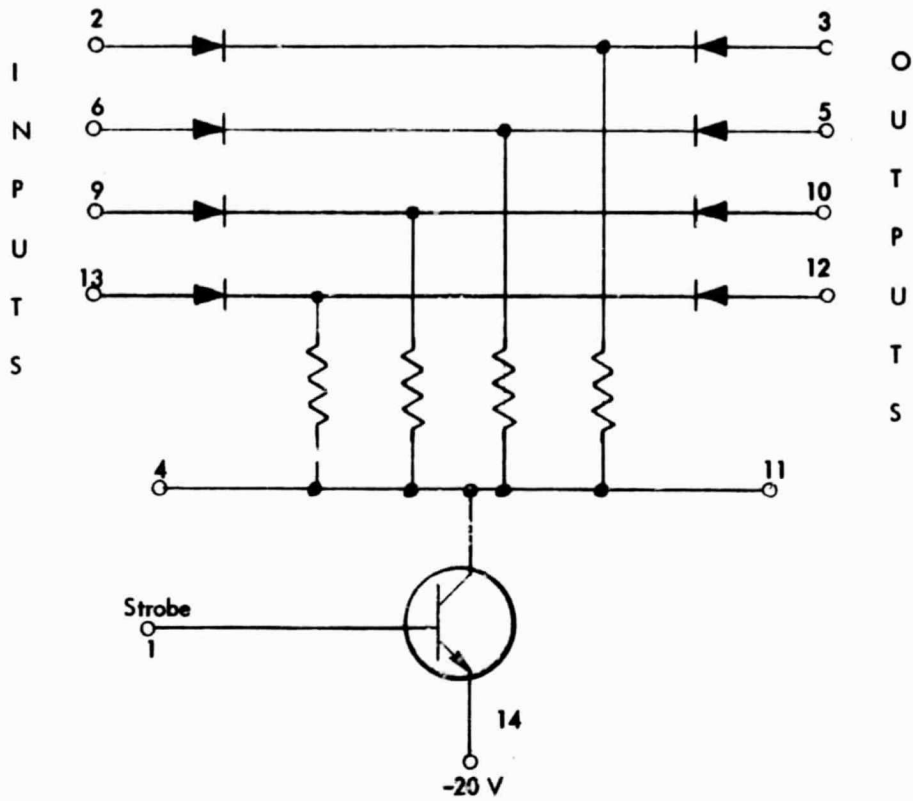
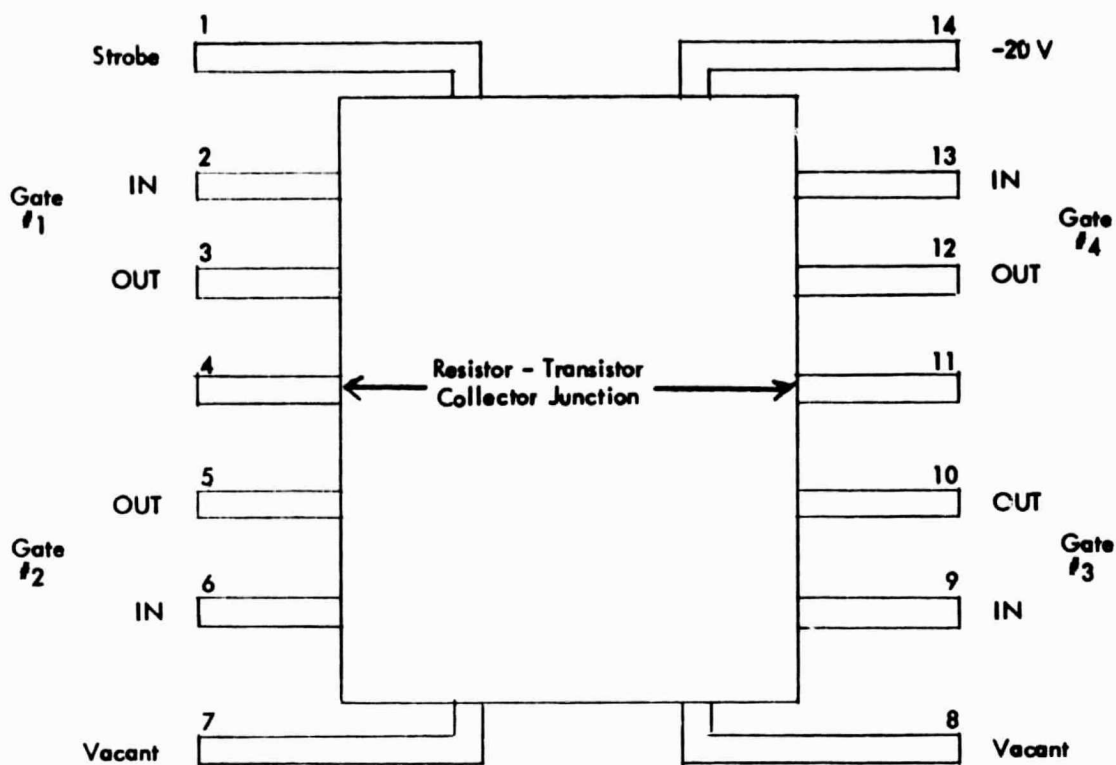


Figure 1
One 4 Input Integrated Circuit Digital Gate

 RADIATION INCORPORATED	CODE IDENT NO.	SIZE			REV
	91417	A	106626		
	SCALE			SHEET	11

NAS FORM 410-1 NOV 12-52



One 4-Input Integrated Circuit

Figure 2
Digital Gate Flatpack Pin Layout

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES.

TOLERANCES

FRACTIONS: $\pm 1/64$; ANGLES: $\pm 1^\circ$
DECIMALS: 3 PLACE $\pm .005$
2 PLACE $\pm .02$



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CODE IDENT NO. 91417

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APPENDIX I

Static Test Jig

The static test jig uses the transistor curve tracer to test the gate driver transistor's parameters, resistor values and diode breakdown voltages. The test jig can be replaced by clip leads used directly with the curve tracer for measuring the flat pack's parameters, however, the test jig is faster, safer, and protects the leads on the flat pack. An extension cable is provided for temperature testing of the flat pack while measuring the circuit parameters with the curve tracer.

Figure A1 shows the complete test set-up schematic diagram. The test jig consists of a 3 PDT switch, a one pole 8 position switch, an extension cable to the AUGAT card connector, an AUGAT flat pack test card and a mini-box. The 3 PDT switch, SW1, selects the component type to be tested with position 1 testing the transistor Q1 only and with position 2 testing both the diodes and resistors only. The single pole 8 position switch, SW2, selects all 8 diodes, one at a time, with the diode CR numbers corresponding to the switch positions. Thus, position 1 tests CR1 and R1 while position 2 tests CR2 and R1. Since adjacent switch positions (in odd-even order) select two diodes connected to the same resistor, the resistance readings shown by the curve tracer should be the same for both positions.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES FRACTIONS: $\pm 1/64$; ANGLES: $\pm 1^\circ$ DECIMALS: 3 PLACE $\pm .003$ 2 PLACE $\pm .02$	 RADIATION INCORPORATED CODE IDENT NO. 91417	SIZE A	106526 SHEET / 3	REV
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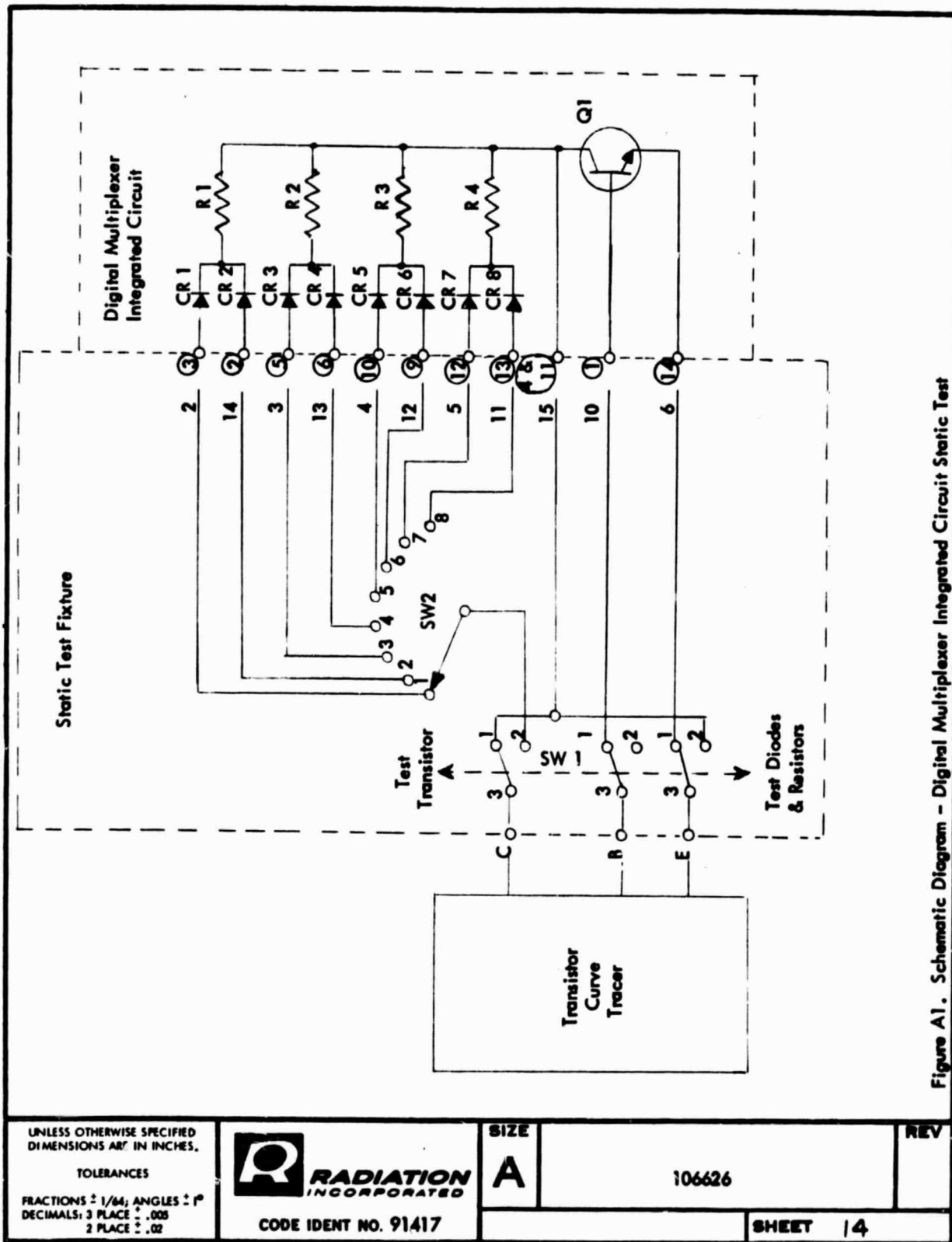


Figure A1. Schematic Diagram - Digital Multiplexer Integrated Circuit Static Test

APPENDIX II

Functional Tests Using Dynamic Test Jig

The dynamic jig proves that the integrated circuit performs its system function properly. This test is a "go" "no go" type test that will tell if the chip is functionally operating. An oscilloscope is used to monitor flat pack operation, therefore, the waveform itself will tell what part of the circuit has failed. A power supply of -20 VDC provides the operating voltage.

Figure A2 is the logic diagram for the complete dynamic test setup. The test jig generates a 200 usec strobe to the gate driver transistor, and sequential "1's" and "0's" to the gate inputs to simulate actual system operation. Figure A3 contains the timing diagram of the test jig output waveforms together with the outputs from a properly operating 4 bit gate digital multiplexer flat pack. During the proper operating sequence, a "1" (-5 volt level) is connected to gate #1; the gate is strobed and the output "1" appears at position #1 on the timing diagram, this sequence continues through gates 2, 3, and 4 so that all 4 "1's" appear as the first four pulses (0V to -8 volts) on the timing diagram. Then a "0" (-1 volt level) is connected sequentially to gates 1 through 4 so that the 4 "0" pulses occur as shown on the timing diagram (0V to -2 volts). Then the entire sequence repeats.

Figure A4 is the schematic diagram of a 70 cps $\pm 10\%$ astable flip-flop that generates the basic clock frequency for test jig operation. The basic 200 usec strobe pulse repetition rate is 14 milliseconds.

Figure A5 is the schematic diagram of a counter stage and this circuit is used three times to provide the 8:1 counter flip-flop function.

Figure A6 is the schematic diagram of the bi-level generator and is repeated four times to provide the four pulses necessary for checking each of the 4 gates in the flat pack. The input circuit is a 3 input "AND" gate wired to the 8:1 counter to provide the first four counts (one from each of the four circuits) that simulate the sequential "1's" into the 4 gates in the flat pack. The following four counts from the 8:1 counter are not used, therefore, 4 sequential "0's" are then fed into the 4 gates in the flat pack.

Figure A7 is the schematic diagram of the 200 usec strobe driver which is used to control the digital multiplexer gate driver "ON" time. This strobe pulse is located in the center of the "1's" being fed into the gate circuits to provide optimum gating.

The values for components used in all of these schematics reflects the design of the Nimbus system so that proper signal simulation can be achieved. The outputs from the digital gate are all tied together into one circuit so that a single beam oscilloscope can be used to perform the test.

Failure Analysis

The four bit digital gate chip has only four components that give different failure conditions. These four are the driver transistor Q1 (refer to figure A1) the diodes CR1 and CR2, and the resistor R1. (Diodes CR3 through CR8 and resistors R2 through R4 have the same failure conditions as CR1, CR2, and

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES FRACTIONS: $\pm 1/64$, ANGLES: $\pm 1^\circ$ DECIMALS: 3 PLACE: $\pm .003$ 2 PLACE: $\pm .02$	 RADIATION INCORPORATED CODE IDENT NO. 91417	SIZE A 106626	REV SHEET 15
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R1, thus, only one gate will be discussed). The chart of Figure A8 lists the failures and the effect on the output waveform.

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES.

TOLERANCES

FRACTIONS $\pm 1/64$; ANGLES $\pm 1^\circ$
DECIMALS: 3 PLACE $\pm .003$
2 PLACE $\pm .02$



RADIATION
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CODE IDENT NO. 91417

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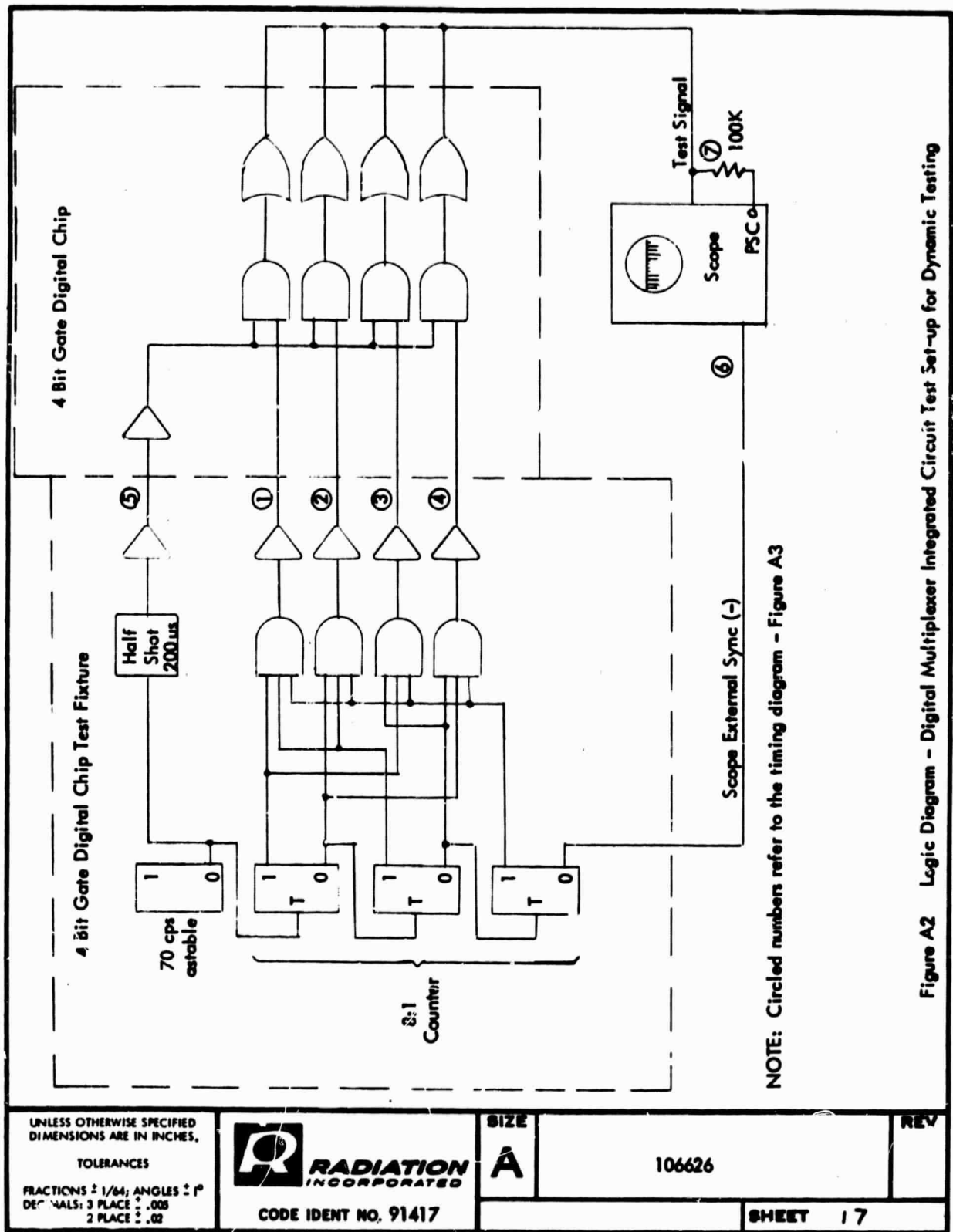


Figure A2 Logic Diagram - Digital Multiplexer Integrated Circuit Test Set-up for Dynamic Testing

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES.

TOLERANCES

FRACTIONS: $\pm 1/64$; ANGLES: $\pm 1^\circ$
DECIMALS: 3 PLACE $\pm .005$
2 PLACE $\pm .02$



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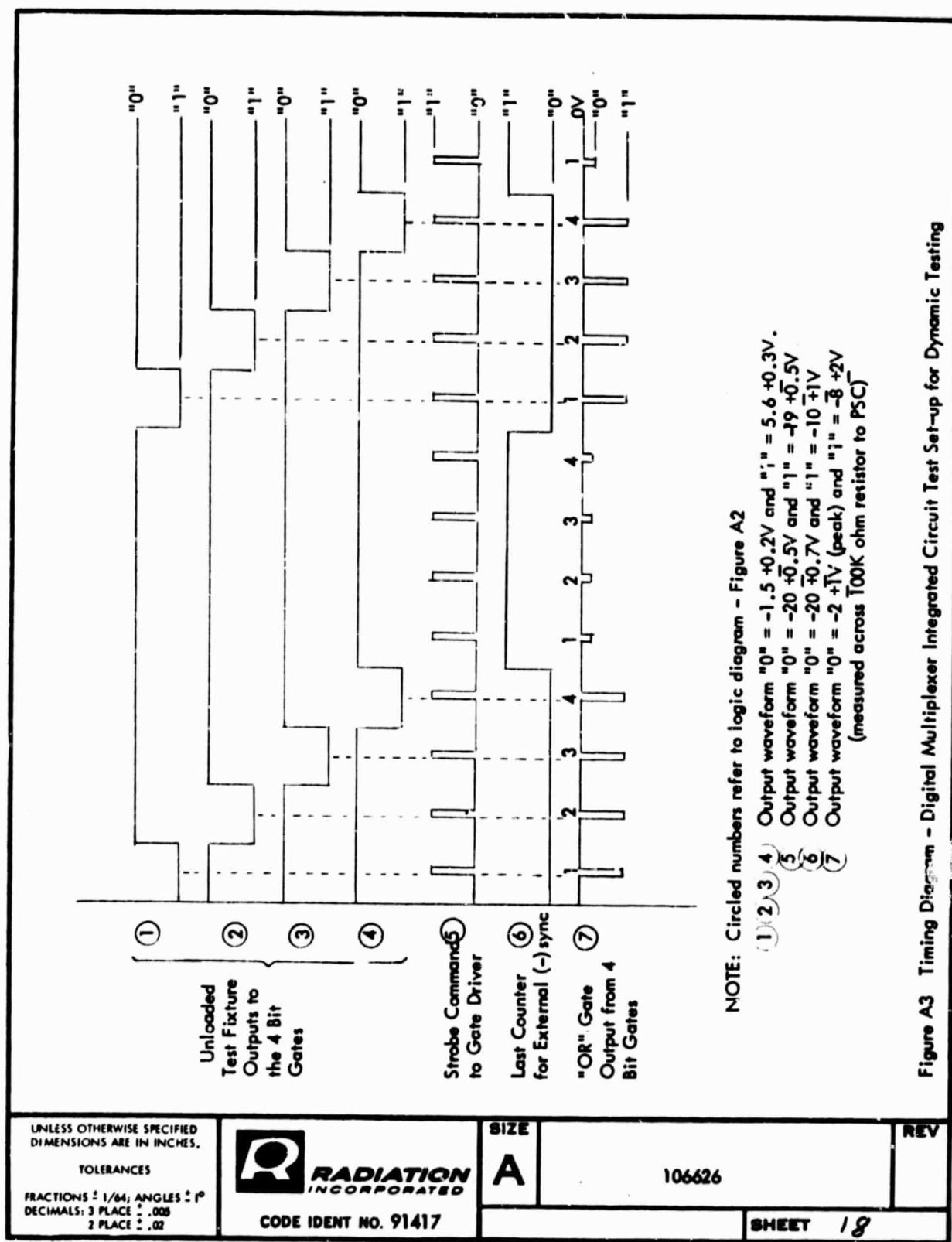
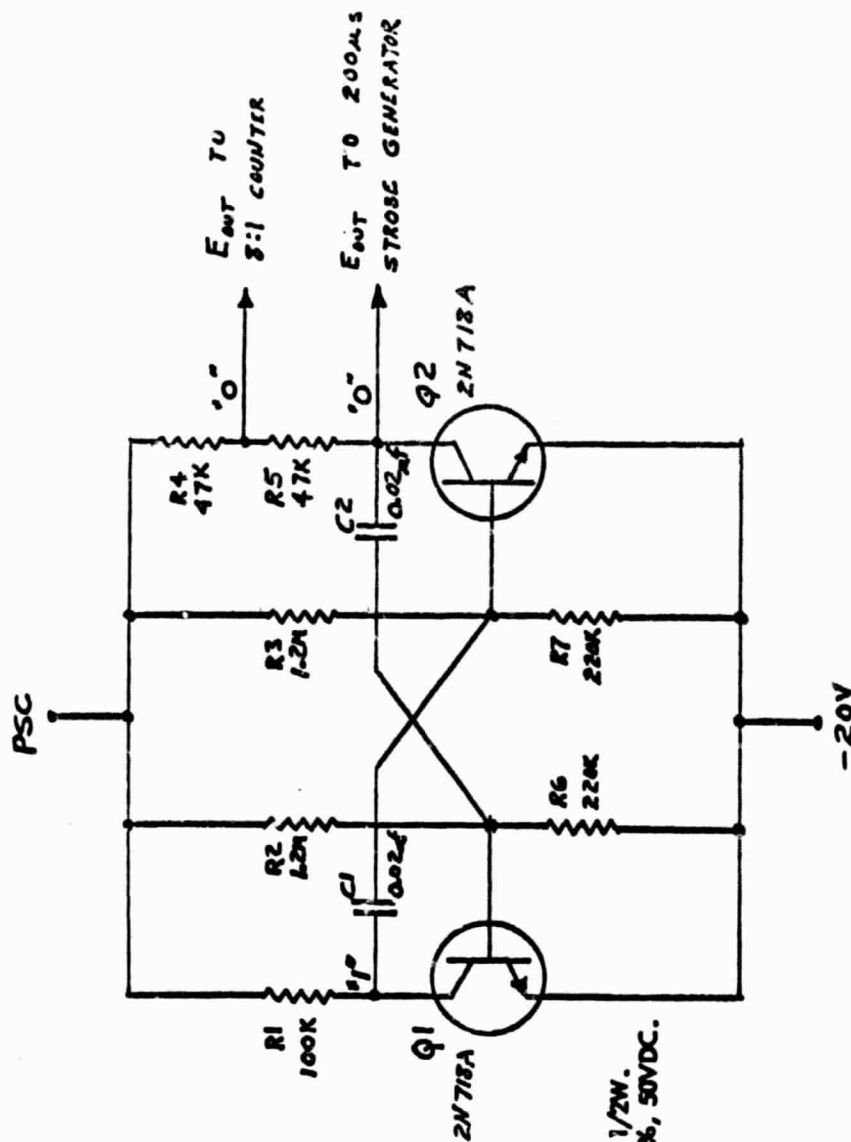


Figure A3 Timing Diagram - Digital Multiplexer Integrated Circuit Test Set-up for Dynamic Testing



NOTES:
All resistors 5%, 1/2W.
All capacitors 10%, 50VDC.

FIGURE A4. SCHEMATIC DIAGRAM - 70 CPS ASTABLE FLIP-FLOP

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES.

TOLERANCES

FRACTIONS: 1/64; ANGLES: 1°
DECIMALS: 3 PLACE: .005
2 PLACE: .02



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INCORPORATED

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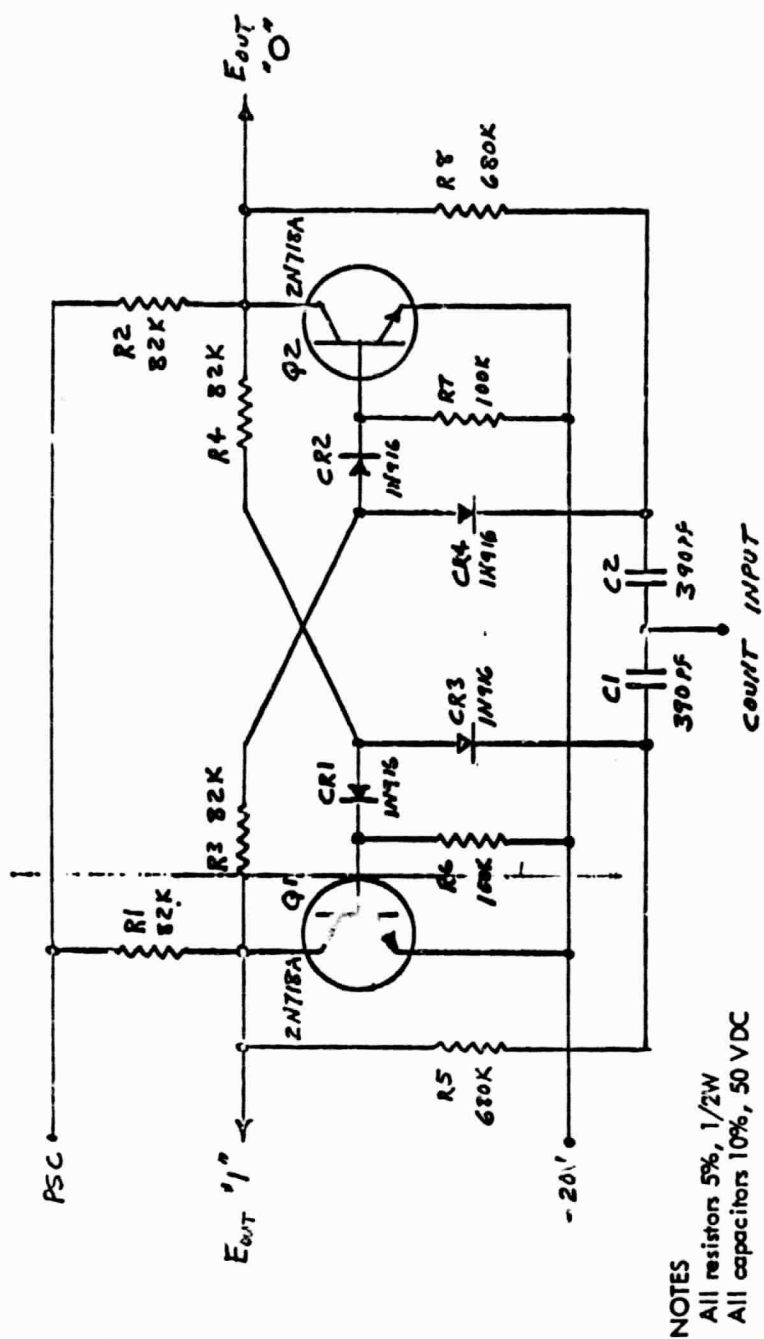
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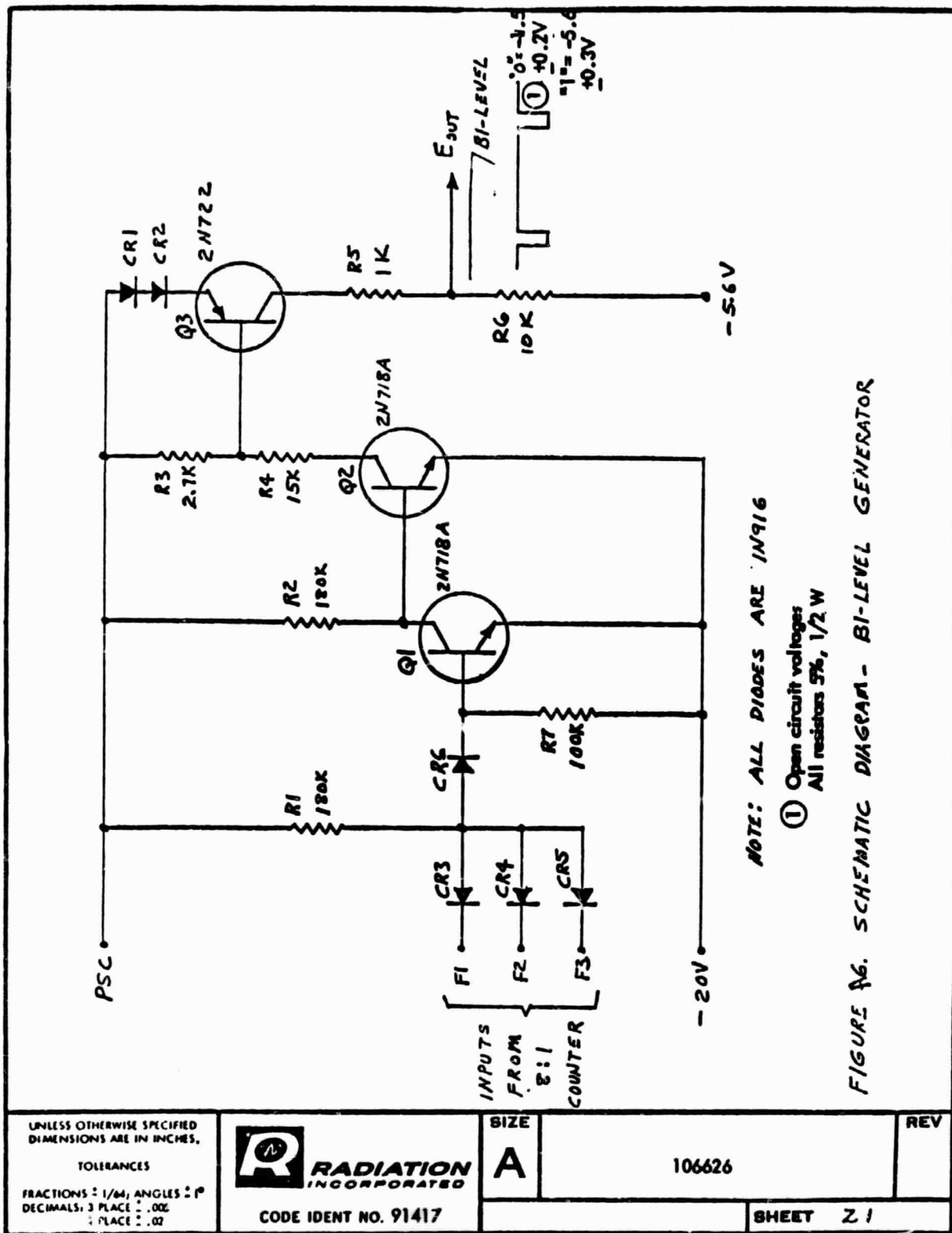
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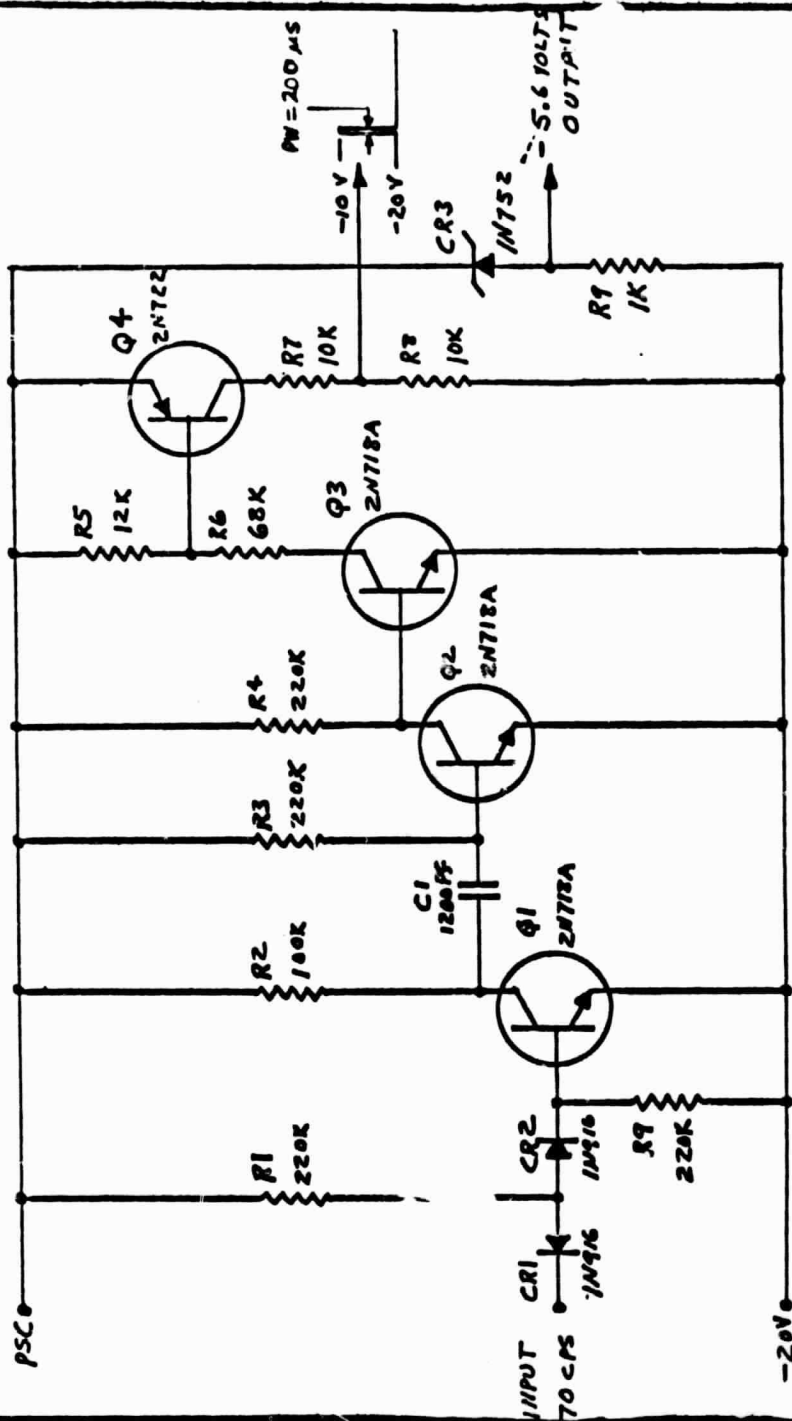
NOTES
 All resistors 5%, 1/2W
 All capacitors 10%, 50 VDC

FIGURE A5. SCHEMATIC DIAGRAM - COUNTER FLIP-FLOP

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES FRACTIONS: 1/64, ANGLES: 1° DECIMALS: 3 PLACE: .005 2 PLACE: .02	 RADIATION INCORPORATED CODE IDENT NO. 91417	SIZE A	106626	REV
R-460-1	SHEET 20	SHEET 20	SHEET 20	SHEET 20



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NOTES: All resistors 5%, 1/2 W
All capacitors 10%, 50 VDC
Figure A7 Schematic Diagram - 200 μsec strobe driver

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES.

TOLERANCES

FRACTIONS: 1/64; ANGLES: 1°
DECIMALS: 3 PLACE: .003
2 PLACE: .02



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CODE IDENT NO. 91417

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**Figure A8
Failure Analysis Chart**

Failure Mode	Component	Flat Pack Pin No.	Output Waveform	Remarks
OPEN	CR 1 CR 3 CR 5 CR 7	3 5 10 12	Continuous "1's" all Bit Times	Any one input diode opening up, allows all strobe pulses to pass through the gate
	CR 2 CR 4 CR 6 CR 8	2 6 9 13	#1 Missing #2 One #3 "1" #4 Pulse	Any one output diode opening up, removes only that particular "1" pulse from the output.
	R 1 R 2 R 3 R 4	4 & 11 4 & 11 4 & 11 4 & 11	#1 Missing #2 One #3 "1" #4 Pulse	Any one resistor opening up, removes only that particular "1" pulse from the output.
	Q 1	6,7,1 & 12	No output pulses	Output level is 0 volts
SHORT	CR 1 CR 3 CR 5 CR 7	3 5 10 12	#1 The #2 Input #3 Gate Pulse #4 Appears	Any one input diode shorting, allows that particular input gate "1" level to pass to the output.
	CR 2 CR 4 CR 6 CR 8	2 6 9 13	#1 Only #2 One #3 "1" #4 Pulse Appears	Any one output diode shorting allows only that one pulse appear as a "1" at the output.
	R 1 R 2 R 3 R 4	4 & 11 4 & 11 4 & 11 4 & 11	Continuous "1's" all Bit Times	The strobe pulses are applied (at a -20 volt level) directly to the output for every bit time.
	Q1 C - E Q1 C - E Q1 B - E	14 to 4 & 11 1 to 4 & 11 1 to 14	Square Wave No output pulses	Input Gate pulses are directly "OR" gated together to form a square wave

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES.

TOLERANCES

FRACTIONS: 1/64; ANGLES: °
DECIMALS: 3 PLACE: .008
2 PLACE: .02



**RADIATION
INCORPORATED**

CODE IDENT NO. 91417

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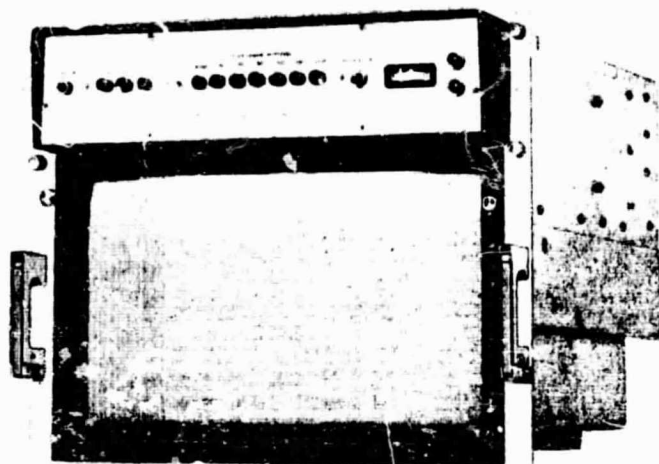
APPENDIX X
BRUSH EVENT RECORDER SPECIFICATIONS

brush

DATA SHEET

150 channel
operations monitor
model 14 3615 00

- 1.25 ms response
- solid state input switching
- interchangeable switch functions
- internal chart takeup
- complete in 15-1/2" panel space



MEETS MIL-I-26600
(RFI), Class I

simultaneously records multiple events in sequence against time

The Operations Monitor model 14 3615 00 records on-off, go/no-go or other two-state operations in order of occurrence, duration and time relationship. Up to 150 channels may be monitored simultaneously with time accuracies of 1.25 milliseconds. Resolution of pulses as short as 2.5 milliseconds is possible with 100% confidence.

Each channel is recorded by a fixed stylus which writes by pulsed electrical current on electro-sensitive paper. Pulse repetition rate varies with chart speed ensuring a clear, continuous line when a "write" condition exists and instant stoppage of the line when input is switched to a "no-write" condition. Depending on switching logic employed, a "write" condition may represent ON and a "no-write" condition OFF, or vice versa. The record appears in parallel lines, present in one condition, absent when switched to the alternate condition. Styli are arranged in equally spaced groups of ten. Channel identification numbers are preprinted on chart. Overall display is an orderly illuminated presentation, easy to see and interpret.

TRANS-SWITCHER solid state input switching,
interchangeable logic *

To eliminate mechanical relays and insure positive response, solid state switching circuits, disposed ten to a circuit board, are plug-mounted in the recorder. Switching circuits are available for a variety of recording modes, including "ON-write", "OFF-write", redundancy-check and adjustable-threshold types. Decade circuit boards, each governing ten channels, may be interchanged and intermixed as required.

Complete unit, including pulse power supply, switching logic and chart rewind, is contained in a shielded rack-mounting enclosure which occupies only 15-1/2" of panel space. System meets MIL-I-26600, Class I specifications for RFI emanation. Twelve chart speeds from .05 mm/sec. to 200 mm/sec. are disposed in two ranges, operable by pushbuttons, electrically controlled. All chart functions may be remotely controlled.

(*) For selection of switching logic, see associated data sheet, "TRANS-SWITCHER Solid State Switching Circuits for Operations Monitor model 14 3615 00"

brush INSTRUMENTS
DIVISION OF CLEVELAND 37TH AND PERKINS, CLEVELAND 14 OHIO
X-2

APPENDIX XI
BRUSH SOLID STATE SWITCHING SPECIFICATIONS

brush

TRANS-SWITCHER

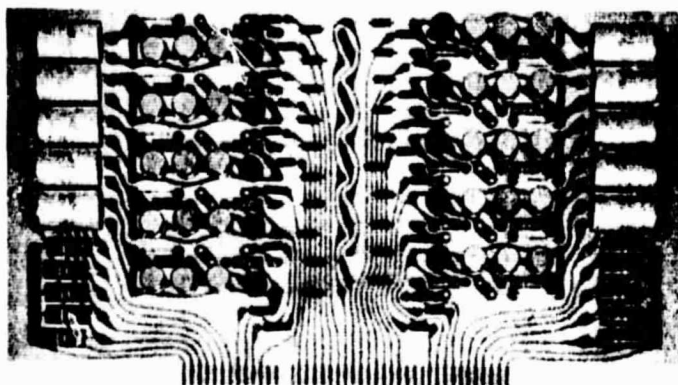
solid state decade

switching circuits

series 3400

FOR

OPERATIONS MONITOR model 14 3615 00



Trans-Switcher series 3400 decade circuit boards are designed to supplant electromechanical relays for input switching to individual channels of the Brush Operations Monitor model 14 3615 00 and subsequent variations of this improved event recorder. Each board controls ten switching circuits. Boards are plugged into receptacles inside the Operations Monitor, so that no additional panel space is required.

Models available fall in two categories: (1) those for use where inputs derive from external switch or relay action; and (2) those utilizing the presence or absence of a voltage signal at rated level. For an ON/WRITE condition, triggering voltage of 4 or 5 volts, (depending on specific model used) insures appearance of trace. For an OFF/NOT-WRITE condition, input of 1 volt or less insures non-appearance of trace. The one-volt leeway from zero voltage forestalls possible erroneous indications from unwanted system noise.

Switching response is virtually instantaneous (no greater than 1.25 milliseconds.) Ambiguities as to occurrence and timing of events are thereby eliminated. Boards may be interchanged or intermixed as required.

EXTERNAL SWITCH INPUTS

External input switching, sine-ended 11 3402 00

Controls ten channels, actuated by external relays or switches with contacts capable of handling 600 volts, 6ma. Common ground; 27K limiting resistors. External switch closure produces a "not-write" condition.

External input switching, floating 11 3402 01

Controls ten input channels, actuated by external relays or switches with contact ratings of 15 volts, 300 ma. All channels floating and isolated from each other and from ground - thus are isolated from extraneous system voltages. External switch closure produces a "not-write" condition.

VOLTAGE INPUTS

Switching pulse, high impedance (27K), flotation 11 3402 02

Controls ten channels, producing a "write" condition on application of voltage of 4.0v DC or higher to maximum of 60v. 27K input impedance. All channels floating and isolated from each other and from ground, Voltage, NOT WRITE: 0 - 1volt.

Switching pulse, high impedance (27K), floating
- with all-circuits confidence check 11 3402 03

Identical to model 11 3402 02 (above) but includes test-circuit and reference source to insure that all channels write at specified input of 5 volts or higher and do not write below specified voltage level of 1.5 volt.

Test circuit connects with momentary pushbuttons on Operations Monitor panel.

Switching pulse, adjustable threshold -
- with all-circuits confidence check 11 3402 04

Controls ten channels, producing a "write" condition on application of voltages whose minimum may be adjusted be-

tween 5 and 25 volts by means of variable potentiometers for each channel. Permits setting all channels to write simultaneously on application of a specific voltage input. Floating inputs. Impedance varies with setting, but is never less than 27K. Includes test-circuit and reference, connected with test pushbuttons on Operations Monitor panel.

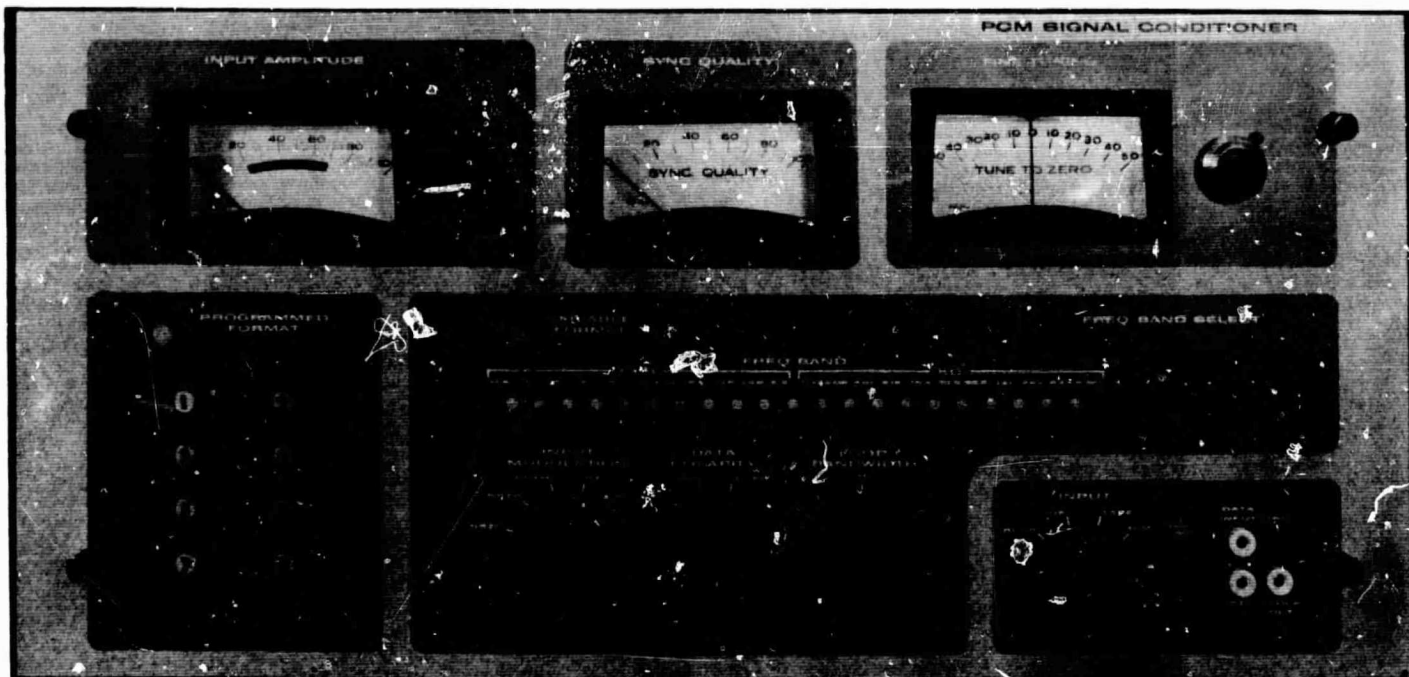
Paired-channel, "redundancy-check" -
with all-circuits confidence check 11 3402 05

Controls 5 event channels, producing "write" condition on odd-numbered and "not-write" condition on even-numbered styli with application of 5 volts or higher. Reversal of writing occurs when voltage is removed. Resulting adjacent traces thereby establish event with certainty. All channel pairs are floating and isolated from each other and ground. 15K input impedance. Includes test-circuit and reference, connected with test pushbuttons on Operations Monitor panel.

brush INSTRUMENTS
DIVISION OF **GEVITE** 3714 AND PERKINS, CLEVELAND 14, OHIO

APPENDIX XII

MODEL 4041 PCM SIGNAL CONDITIONER
AND BIT SYNCHRONIZER



The Radiation Model 4041 Signal Conditioner and Bit Synchronizer reconstructs and synchronizes noisy PCM signals over a wide range of signal-to-noise ratios and bit frequencies. Output is the regenerated data and bit rate clock.

The unit is designed for applications requiring a high degree of reliability, and is currently in use in on-line spacecraft checkout systems which require very high reliability. Plug-in type printed circuit cards are used throughout, and all circuitry is solid-state. Unnecessary circuit complication has been avoided in order to achieve a straightforward design and retain operating accuracy. The probability of operator error has been greatly reduced by human engineering, and the layout and function of all meters and controls is specifically planned for ease and accuracy of operation.

Input to the Model 4041 Signal Conditioner and Bit Synchronizer may be serial PCM signals, in all major formats, from telemetry receivers, magnetic tape, PCM signal simulators, or other sources of serial PCM data. The unit derives bit rate clock from the incoming data, and with the aid of the clock determines whether a "one" or "zero" was transmitted in each bit period. Pulse integration and dump bit detection are used for all input codes to provide optimum performance under widely varying signal-to-noise ratios.

Split phase signals are synchronously rectified and integrated over the bit period. Bit error probability is improved, since the noise above and below the bit rate frequency is minimized by the noise cancelling effect of recirculation; and synchronous integration provides filtering at all bit rates without the necessity of additional input filtering.

The phase lock loop of the synchronizer employs a transition detector which adaptively varies the loop bandwidth proportionally to the incoming signal's bit density. Analog operation of the loop provides improved performance over other techniques, specifically as related to acquisition time and the effect of missing pulses. In selecting the design criteria for this equipment, emphasis was placed on performance in terms of bit slippage, which directly affects decommutation accuracy, rather than phase error. These and other features provide a measured performance within 1 db of the theoretical bit error probability for rectangularly shaped or filtered PCM signals.

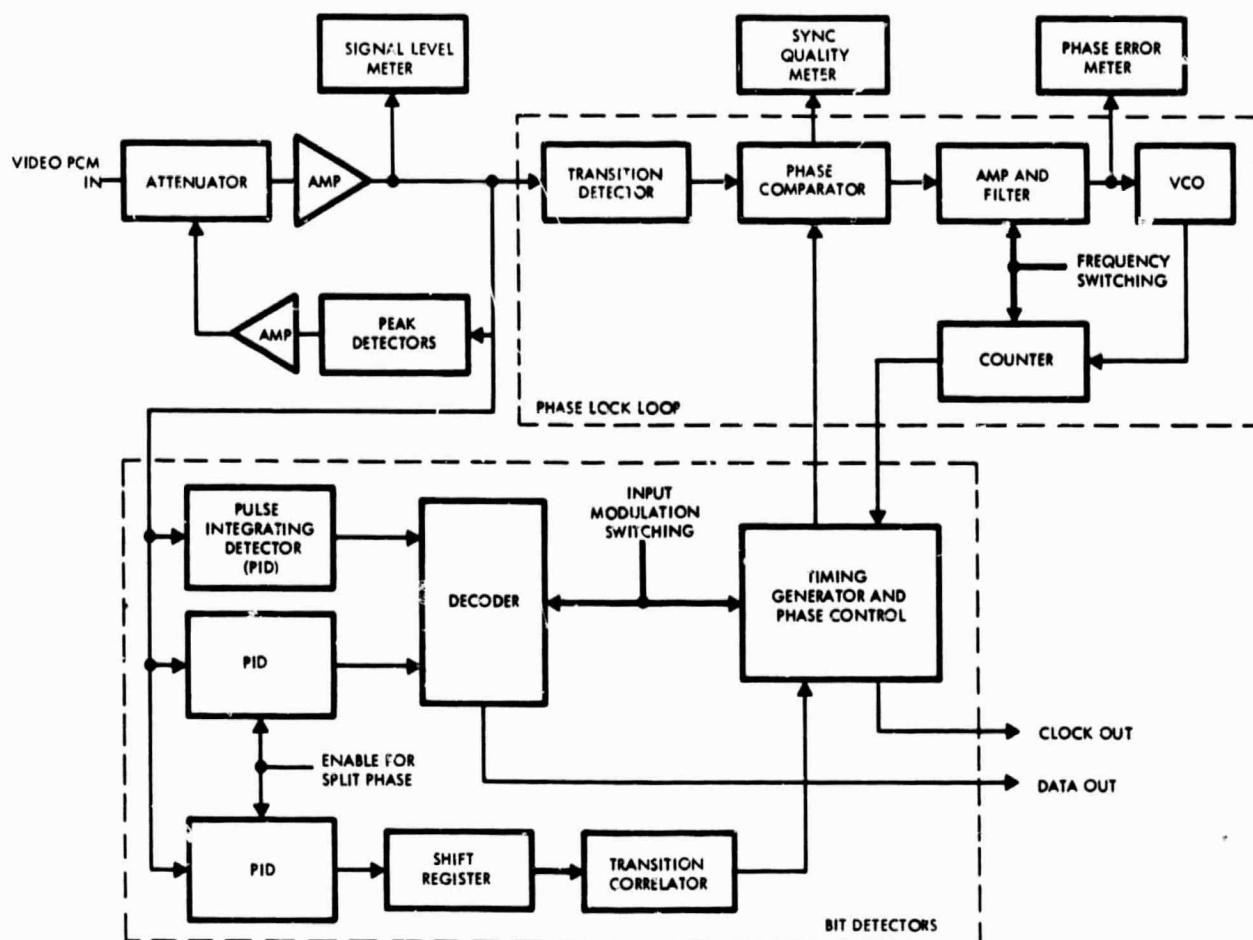
Eight different PCM formats are pre-programmed on plug-in type printed circuit cards. Special cards can be supplied for any specific formats and bit rates within the unit's operating capabilities. Any of the eight programmed formats can be selected by a coded signal from remote programming equipment.

Additional PCM formats can also be set manually at the Synchronizer's control panel, with the FREQUENCY BAND SELECT switch controlling the coarse and fine frequency of the VCO and the loop filter and INPUT MODULATION, DATA POLARITY, and LOOP BANDWIDTH switches selecting corresponding parameters.

Input Amplitude, Sync Quality, and Fine Tuning meters are provided for monitoring the equipment's performance. The Sync Quality meter is read in conjunction with the Fine Tuning meter for positive indication that the synchronizer is locked onto the correct bit frequency rather than a harmonic.

In addition to the circuit interface connectors at the rear of the chassis, front panel monitoring points and input/output connectors are provided for convenience in testing and evaluation. Four inputs are switch selectable. Test points on each printed circuit card facilitate checkout and maintenance.

Operating voltages required for the Model 4041 Signal Conditioner and Bit Synchronizer are $-10 \pm 5\%$ at 2.2 amp.; $+10 \pm 5\%$ at 0.250 amp.; $-26 \pm 5\%$ at 0.350 amp.; $+26 \pm 5\%$ at 0.600 amp.; and $-24 \pm 20\%$ at 0.600 amp. (this indicator load may be combined with -26 volt load). A power supply to furnish these requirements is available as optional equipment.



SPECIFICATIONS

INPUT

Coding NRC-C, NRZ-S, NRZ-M, RZ, Split-phase C, Split-phase M.

Bit frequency range:

NRZ 1 – 1,000,000 bits/sec.

RZ/Split-phase 0.5 – 500,000 bits/sec.

Signal amplitude range 0.5 – 60 volts peak-to-peak.

DC offset 60% of input amplitude.

Dynamic range 15:1.

Impedance Greater than 10,000 ohms (shunted by not more than 30 pf).

SYNCHRONIZATION

Bit error rate Within 1 db of theoretical.

Bit jitter accommodation Sinusoidal FM of $\pm 6\%$ of bit rate at frequencies 0.5% of bit rate and below; $\pm 3\%$ at any frequency. Phase modulation of $\pm 20\%$ of a bit period.

Acquisition Range $\pm 10\%$ of bit rate.

Sensitivity Bit slippage will be less than one in 10^5 bits at an FM receiver IF S/N ratio of 7 db or more, with bit rate offset of $\pm 4\%$ and bit rate deviation of $\pm 0.7\%$ at a frequency of 0.1% of bit rate.

Bit rate tracking range $\pm 20\%$.

OUTPUT

Format Serial NRZ-C, normal and inverted, NRZ-M; bit rate clock, normal and inverted.

Amplitude -0.1 ± 0.1 volt and -10 ± 0.5 volts (unloaded) from a 50 ohm source.

Rise and fall times 0.1 microsecond maximum.

DIMENSIONS

Height 8.75 inches

Width 19.0 inches

Depth 19.75 inches

APPENDIX XIII
SERIES 540 PCM DECOMMUTATION SYSTEM

RADIATION SERIES 540—AN AUTOMATIC PCM DECOMMUTATION SYSTEM WITH MAGNETIC CORE MEMORY PROGRAMMING

The Radiation Incorporated Series 540 PCM Acquisition and Stored Program Decommulation System combines the flexibility of a random access 8192 x 40 bit, 5-microsecond memory with a high-performance Model 4041 Signal Conditioner and Bit Synchronizer.

The system accepts all major PCM coding forms, including serial PCM/NRZ (mark or change), serial PCM/Split Phase (mark or change), and serial RZ; with continuous coverage of bit rate ranges from 1 to 1,000,000 bits/second NRZ and 0.5 to 500,000 bits/second split phase and RZ. PCM formats and bit rates can be selected automatically by the stored program processor, or manually. System input can be PCM signals from telemetry receivers, magnetic tape reproducers, or any other source of serial PCM signals. A Radiation Model 4042 Signal Simulator provides a wide range of

PCM data and synchronization test signals for system checkout and calibration.

In addition to demultiplexed data, continuous outputs are available for data formatted into parallel words and truncated words. For each serial word entering the system, output words are available in binary or BCD. Both most significant and least significant bit binary outputs are provided for either MSB or LSB input.

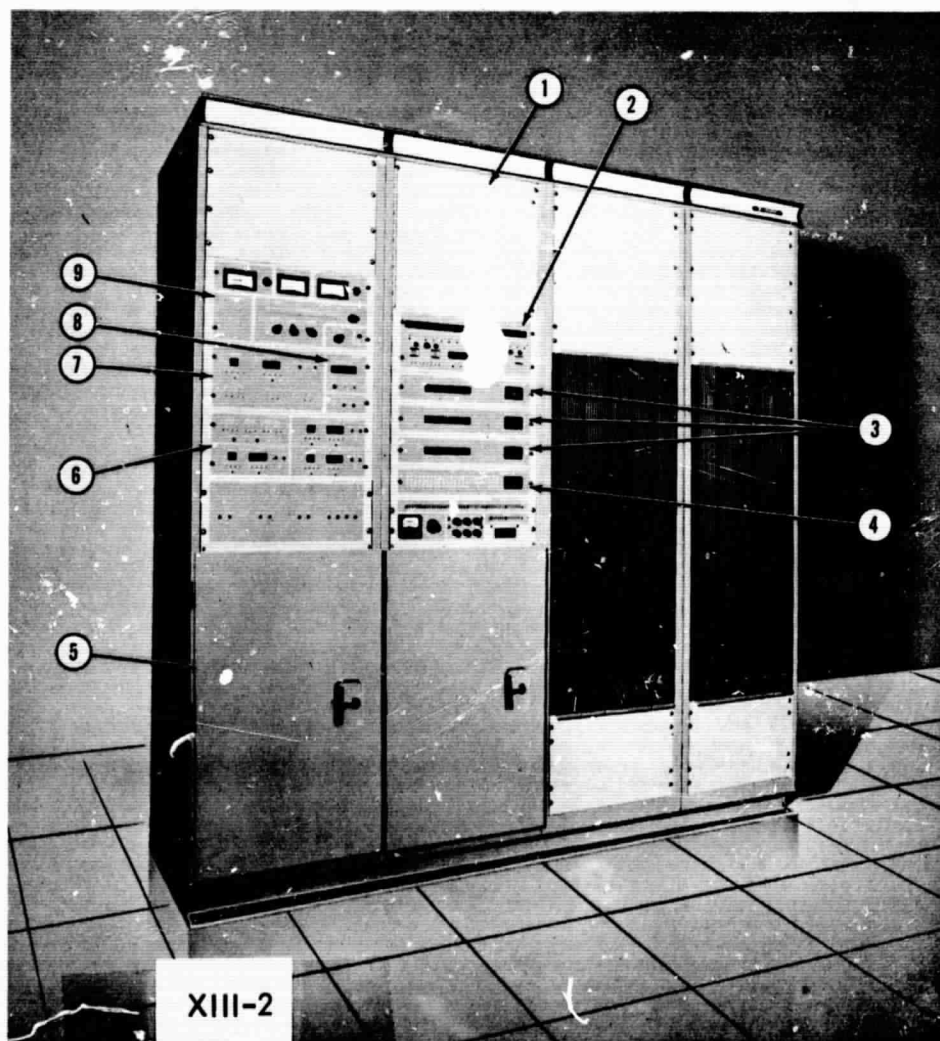
The probability of operator error has been greatly reduced by human engineering. The control panel layout is specifically planned for ease and accuracy of operation. Programs can be modified during decommutation to achieve optimum processing efficiency. Preset programs can be selected manually, or automatically under computer control. The operator can utilize the binary and decimal displays to process data points or to determine system performance

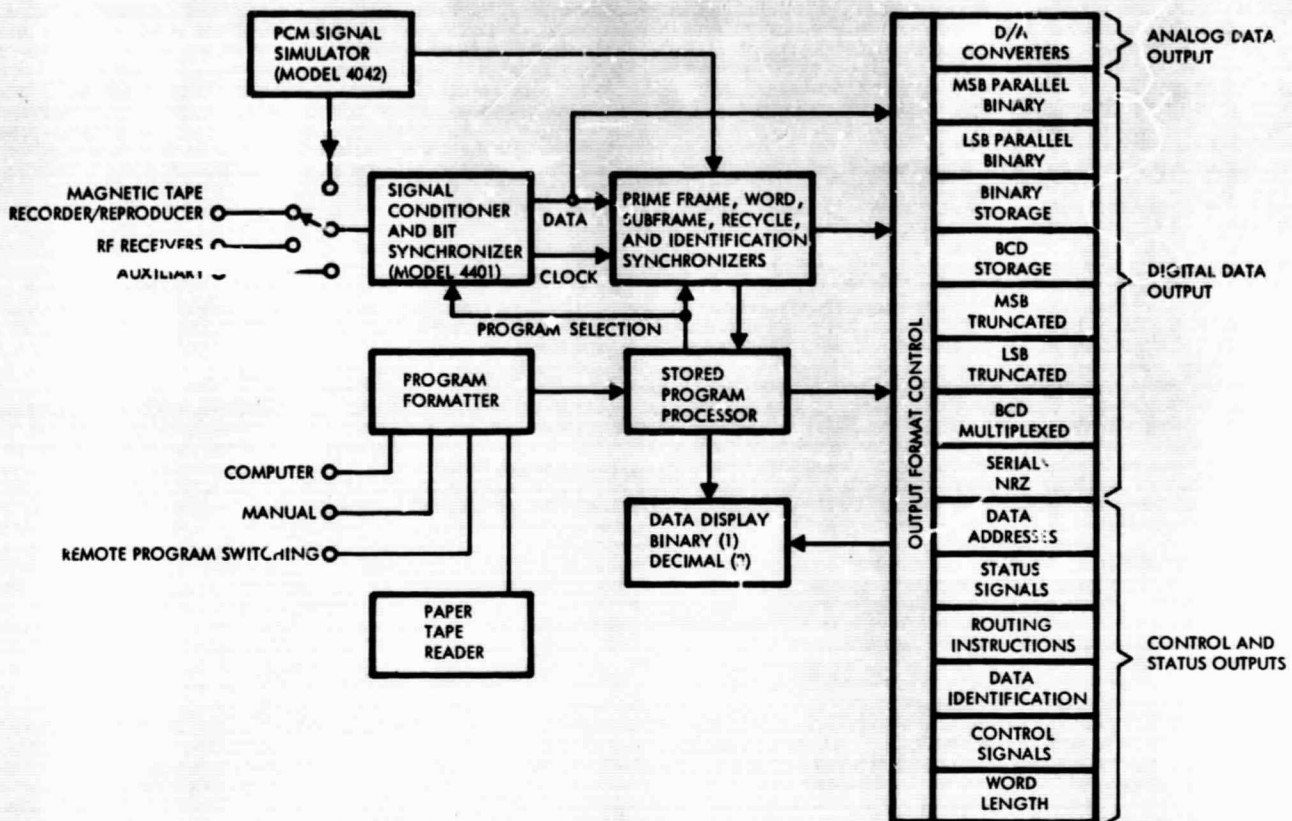
by monitoring key data words or synchronization words.

A modular approach is used throughout the system and down to the logic element level, thus facilitating system maintenance and future modifications or additions. Power supplies are loaded well below ratings to insure sufficient DC power for future additions, and space is provided for additional logic drawers.

The modules, mounting hardware, connectors, and wire wrap connections used in the Series 540 system meet military specifications for severe environmental conditions. The system has been designed to meet the requirements of NASA NPC 200-3 and NPC 250-1, Quality Assurance and Reliability Specifications. In addition special precautions are taken to suppress RFI, including use of RFI cabinets, gaskets, and connectors, to insure correct operation with other equipment.

1. PERFORATED TAPE READER
2. PROGRAM CONTROL
3. DECIMAL DISPLAYS
4. BINARY DISPLAY
5. MODEL 4042 SIGNAL SIMULATOR
6. WORD AND SUBFRAME SYNCHRONIZERS
7. PRIME FRAME SYNCHRONIZER
8. PARITY
9. MODEL 4041 SIGNAL CONDITIONER AND BIT SYNCHRONIZER





Series 540 System — Simplified Diagram

SYSTEM DESCRIPTION

Signal Conditioner and Bit Synchronizer

Input to the Series 540 PCM Decommutation System is through the Radiation Model 4401 Signal Conditioner and Bit Synchronizer, which reconstructs and synchronizes noisy PCM signals. This unit derives the bit rate clock from the incoming data, and with the aid of the clock determines whether a "one" or "zero" was transmitted in each bit period. Outputs are clock and the reconstructed serial data.

Integrate and dump bit detection is used for all input codes to provide optimum performance over widely

varying signal-to-noise ratios. Split phase signals are synchronously rectified and integrated over the bit period. Thus, the noise above and below bit rate frequency is minimized, due to the noise cancelling effect of rectification; and bit error probability is improved.

The phase lock loop of the synchronizer employs a transition detector which adaptively varies the loop bandwidth proportionally to the incoming signal's bit transition density. These and other features provide a measured performance within 1 db

of the theoretical bit error probability for rectangularly shaped or filtered PCM signals.

Both manual and automatic selection of formats is provided. In automatic operation, any of 8 preprogrammable formats may be selected by the stored program decommutator. In manual operation, the VCO and loop filter frequencies are switch-selected.

Input Amplitude, Sync Quality, and Fine Tuning meters are provided on the front panel.

Group Synchronizer

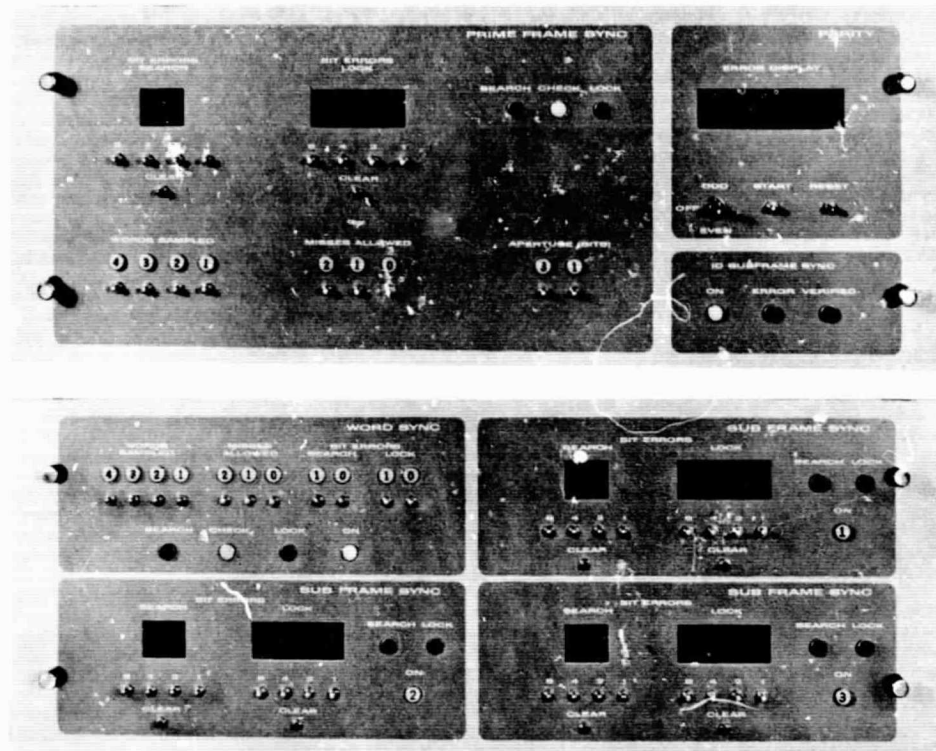
The Group Synchronizer receives reconstructed data and bit rate clock from the Signal Conditioner, and format control codes and quality criteria from the Stored Program Processor. Since the formats are stored in the synchronizer as they are selected, readdressing the memory for format during data processing is eliminated. In addition, the operator can modify a stored format or set up an entire format manually at the control panel.

The Group Synchronizer provides prime frame, subframe (recycle and ID code), and word synchronization. Three modes of operation are utilized at each level of synchronization acceptance: search, check, and lock. The synchronizer steps through each mode automatically, as determined by the signal quality and the formatted error criteria.

To eliminate guesswork in programming the synchronizer, a set of synchronizer performance curves is included in the system's software. With these, Group Synchronizer performance can be determined as a function of the bit error rate, format, and synchronizer parameter settings.

Prime Frame Synchronization

In processing, the prime frame sync pattern is transferred from memory into the storage register, and parallel comparisons are made to detect the sync pattern. Quality parameters are set up at this time. Sync code acquisition steps the Prime Frame Synchronizer to check, and starts the Stored Program Processor. Subsequent sync patterns which occur at the correct time are counted, and if no sync pulse appears, an error is counted. When the prescribed number of Words Sampled is reached before Errors Allowable, the syn-



chronizer steps to lock, and the number of Bit Errors Allowable changes to correspond with the lock setting. The synchronizer "flywheels" at the confidence level established in reaching the lock mode, and monitors the sync position. If sync becomes false, the synchronizer reverts to search. Single slippages can be corrected without reverting to search.

Subframe (Recycle) Synchronization.

The subframe sync code is detected with the same type of parallel correlator used in prime frame code recognition. When prime frame sync has been acquired the Stored Program Processor indicates the time-slot(s) for the subframe code.

Split-syllable sync codes are accommodated by storing the partial patterns until a complete code has been accumulated. The subframe synchronizer advances from search to lock in a manner similar to the Prime Frame synchronizer. Again, the allowed bit errors are automatically switched upon reaching lock.

Subframe (ID) Synchronization.

The ID code may be from 4 to 9 bits in length, and can appear as a sepa-

rate word or within a data word. The ID synchronizer accepts either MSB or LSB codes in conjunction with ascending or descending count.

ID verification forces the Stored Program processor to the correct time-slot, in phase with data. Phasing is retained as long as prime frame sync and ID code sync are maintained. If transmission fade or temporary loss of data causes sync loss, the ID synchronizer forces the memory to the anticipated time-slot, so that data processing remains constant. The ID circuit then reacquires sync normally.

Word Synchronization

The word sync code can appear at either end of a data word. The code and the number of bits are programmed by the Stored Program Processor. Operation of the Word Synchronizer is similar to that of the Prime Frame Synchronizer.

Parity Count

Manual or programmed initiation of the parity count frame starts the parity error count for 99 consecutive frames. Up to 999 errors are displayed decimally, and the display retains its status until reset.

Stored Program Processor

An 8192 x 40 bit, 5-microsecond memory is incorporated in the Stored Program Processor. The memory has no fixed partitioning, and its full capacity is available for either acquisition programming, data word programming, or a combination of the two. Any number of programs can be stored, up to the capacity of the memory. It is operated as a fully random access memory. Normally, format control words are read out sequentially during the initial program selection. The memory need not be accessed for format controls during a data run, and the system's inherent speed is thus increased.

Each memory data word is allocated a unique address, and every word contains 6 bits for the selection of the next word. No multiple accessing is required during decommutation, regardless of the number of subcommutations in the format, and more efficient use is made of the memory's speed.

Data processing begins when format control word "1" reads the initial format address (normally,

prime frame sync) into the memory address register. The register will hold the address until the first prime frame sync word has been acquired. This gates the address out, and the appropriate memory word is read to provide controls and addresses for sequencing the memory.

Inputs to the Stored Program Processor are by paper tape, computer, or manual entry. Words can be re-written by appropriate control of the restore portion of the read/restore cycle and proper encoding of the input device. New programs may be written into the memory on a "time-sharing" basis while the existing program is being decommutated, in order to eliminate down time for programming.

A 300 character per second paper tape reader is provided for inserting format information into the system's memory unit.

Output Format Control

The Output Format Control unit receives serial regenerated data from the Signal Conditioner, timing from the Group Synchronizer, and program control instructions from the Stored Program Processor. Analog and digital data outputs are provided, as well as status, control, and routing information for external devices. Parallel binary and BCD data are also provided to the system displays.

Analog outputs are through the

D/A converters, each of which includes a decoder for the addresses from the Stored Program Processor. Thus, any measurand, whether it appears as a supercommutated, prime or subcommutated channel, can be routed to any converter.

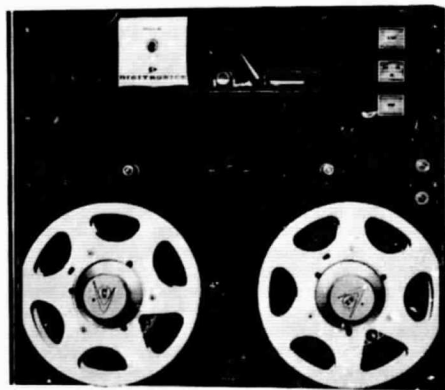
Both MSB and LSB serial binary data are converted to MSB and LSB parallel binary, and to MSB and LSB truncated binary, for system outputs. All serial binary data is also converted for parallel BCD multiplexed output.

Any designated channel may be stored in the output registers in either binary or BCD. Selection is made in the Output Format Control by decoding the program control instructions from the Stored Program Decommutator. BCD channels to be stored receive their data from the BCD multiplexed output, and binary channel data is received from the MSB parallel binary output.

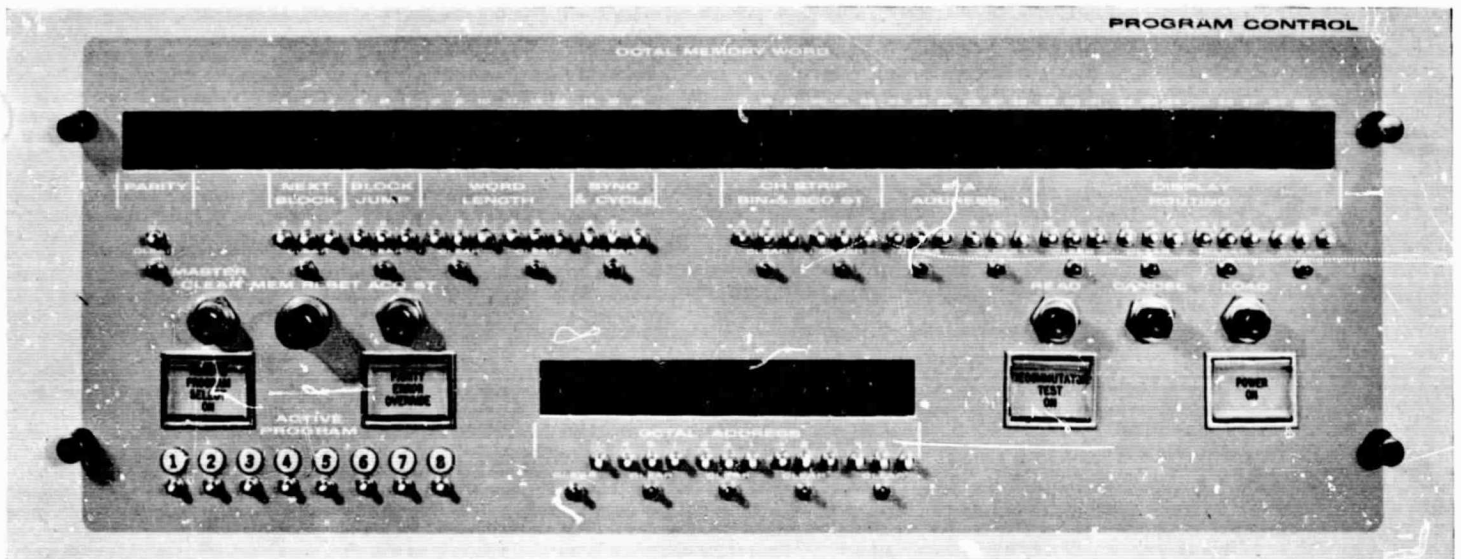
Outputs are also provided to three decimal displays and one binary display.

Additional Capability

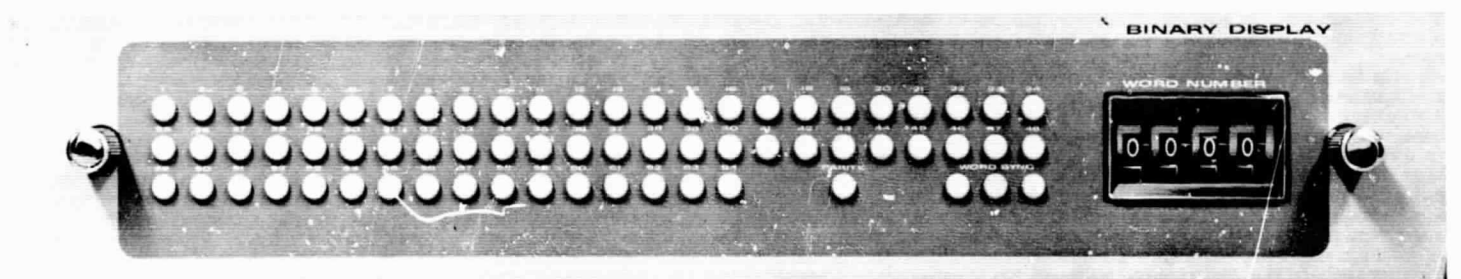
Ample memory capacity and logic module space is provided for the addition of a Data Correction feature, to allow the scale factoring, offsetting, and linearizing of data during decommutation. The system can also be expanded to incorporate data redundancy reduction in order to reduce the bandwidth of data for transmission or processing.



Stored Program Tape Reader Panel



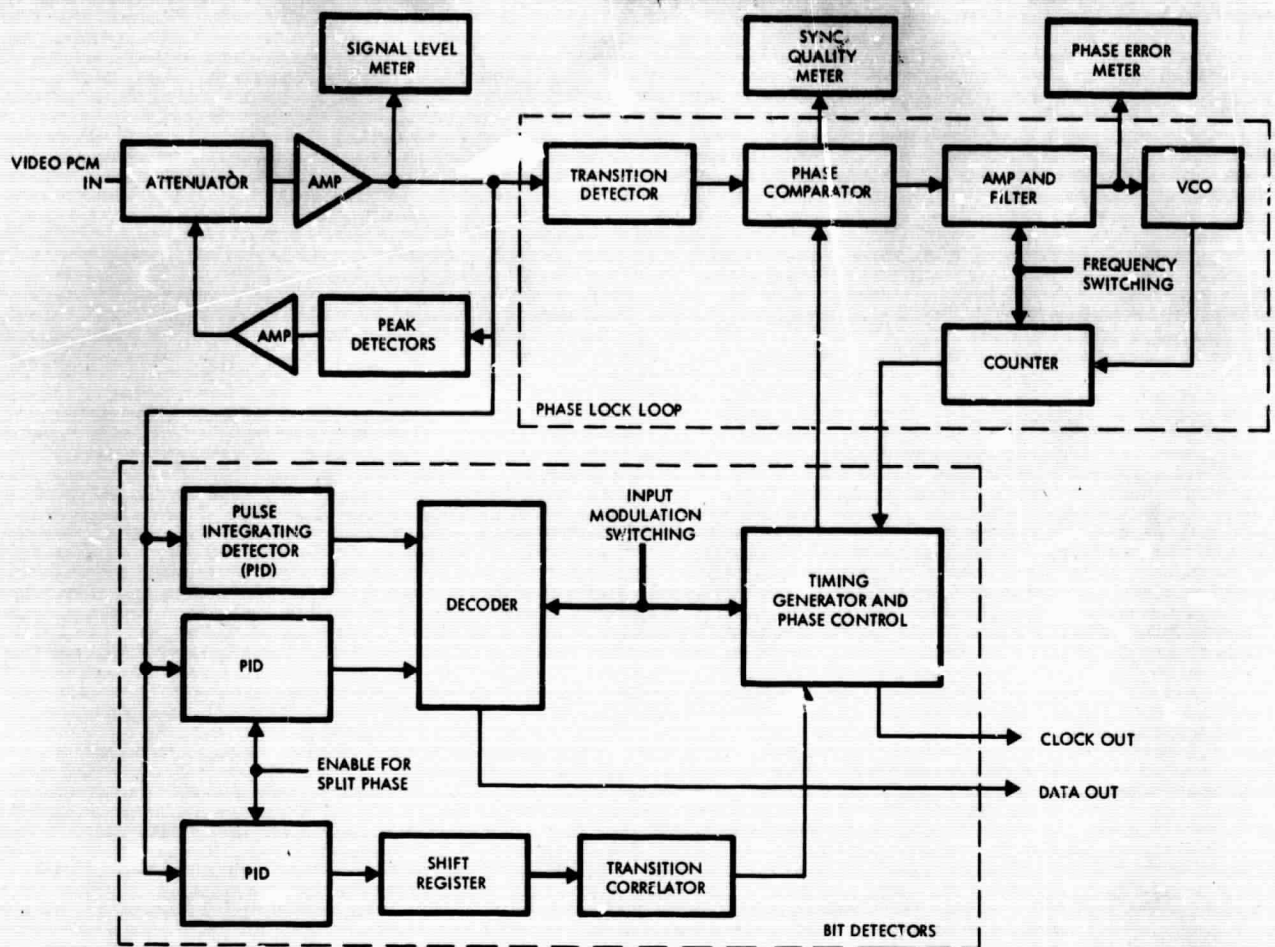
Stored Program Control Panel



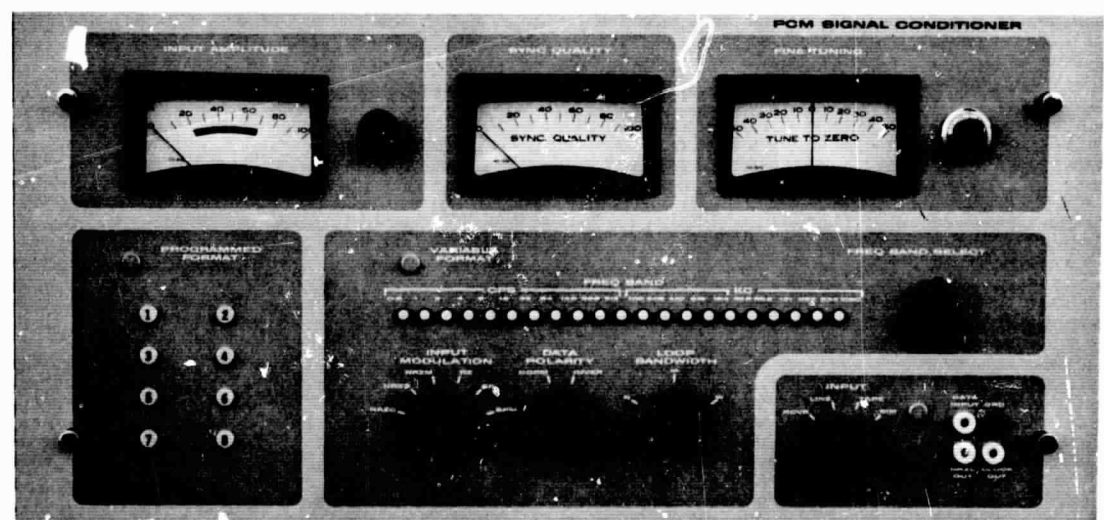
Binary Displays



Decimal Displays



Block Diagram of Model 4041 Signal Conditioner and Bit Synchronizer



RADIATION MODEL 4041 SIGNAL CONDITIONER AND BIT SYNCHRONIZER

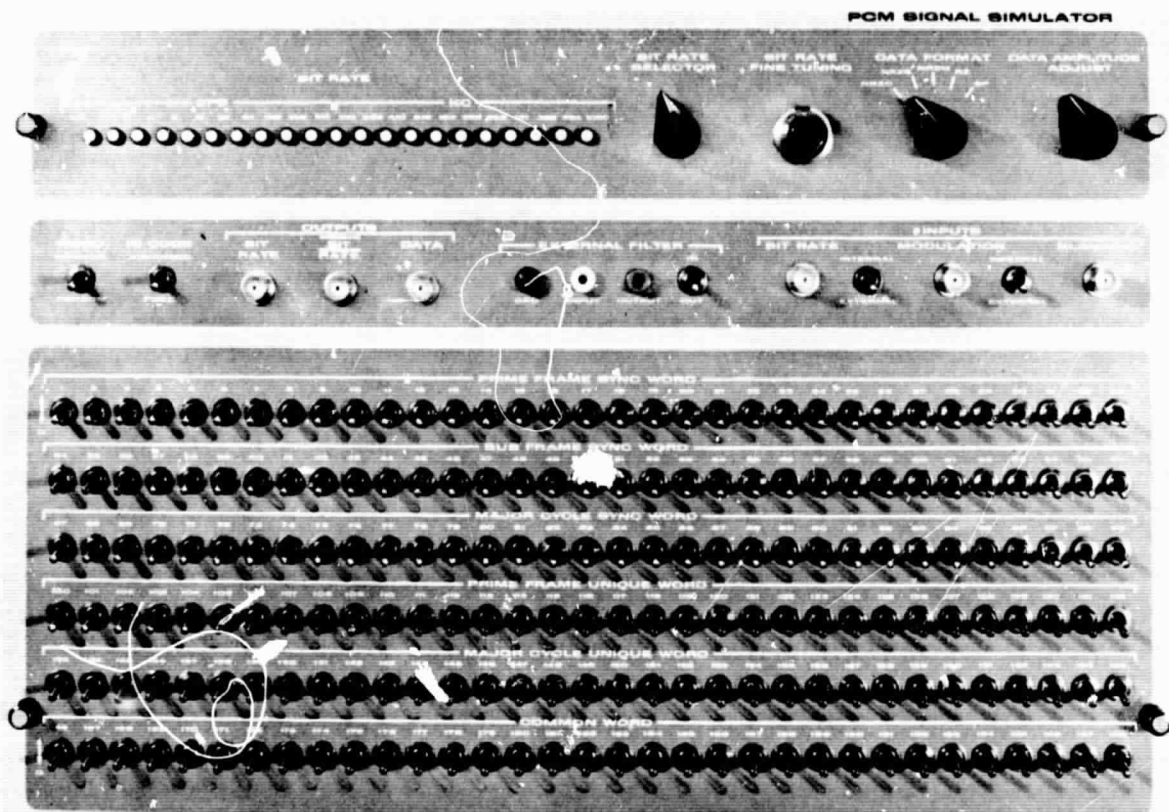
The Radiation Model 4041 Signal Conditioner and Bit Synchronizer, a basic component of the Series 540 System, is designed for applications requiring a high degree of reliability. The unit is currently in use in on-line spacecraft checkout systems.

Plug-in type printed circuit cards are used throughout, and all cir-

cuitry is solid-state. Unnecessary circuit complication has been avoided in order to achieve a straightforward design and retain operating accuracy.

The Model 4041 maintains synchronization with a 3% bit jitter frequency, or a jitter of $\pm 25\%$ of a bit period at frequencies up to bit

rate, with a signal-to-noise ratio of 15 db. It will follow bit rate variations of $\pm 20\%$ with 50% transitions. As a basic universal PCM synchronizer, the unit is extremely versatile, featuring both automatic selection of eight programmed formats and manual formatting at the control panel.



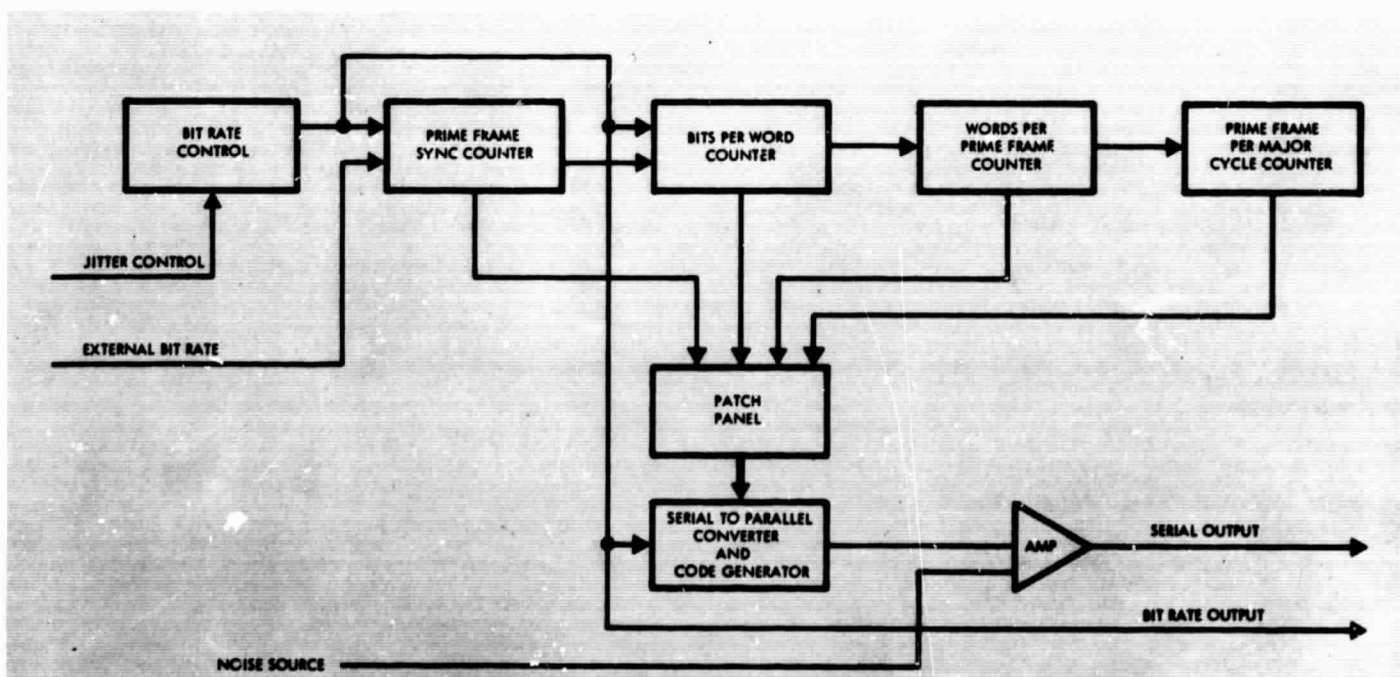
RADIATION MODEL 4042 SIGNAL SIMULATOR

The Model 4042 Signal Simulator, included in Radiation's Series 540 PCM System, generates test data for quick, precise checkout of the system. Evaluation of PCM telemetry receiving and processing is convenient and accurate, as a wide range of PCM data and synchro-

nization signals are available. Noise and signal faults can be introduced in controlled increments, and errors are simulated with switches on the control panel. Controls include Bit Rate and Format, Prime Frame Length, Word Length, and Word Synchronization. Any word synchro-

nization, parity, and data combination can be set up. The unit is capable of simulating a major cycle in which word length can be 4-33 bits, prime frame length 4-512 words, and major cycle length up to 512 prime frames. A display panel permits monitoring key points during simulation.

Block Diagram of Model 4042 Signal Simulator



PERFORMANCE SPECIFICATIONS

SYSTEM INPUTS

Bit Frequency	1 to 1,000,000 bits per second, NRZ; 0.5 to 500,000 bits per second, split phase and RZ.
Signal Range	0.5 to 60 volts peak-to-peak.
Dynamic Range	15 to 1 without adjustment.
DC Offset	60% of input peak-to-peak amplitude.
Input Impedance	Greater than 10,000 ohms shunted by not more than 30 uuf or decreased to match the input source.
Input Selection	Selector switch for four inputs.
Polarity	Reversible.
Connection	Single-Ended.
Codes Accepted	RZ, NRZ (C, M & S), Split Phase (C & M).
Word Bit Arrangement	MSB first or LSB first.

BIT SYNCHRONIZATION

Bit Error Rate	Within 1 db of theoretical (see typical performance curve).
Jitter	Maintains Synchronization with a jitter of $\pm 25\%$ of a bit period.
Acquisition Range	$\pm 10\%$ with 50% transition at a signal-to-noise ratio of 15 db.
Tracking Range	$\pm 20\%$.
Maintenance of Bit Synchronization	$\pm 25\%$ of a bit period with a signal-to-noise ratio of -4 db and a noise bandwidth equal to the bit rate.
Sensitivity	Bit slippage threshold of 8 db or better. (Bit slippage threshold defined as the signal-to-noise ratio in an FM receiver IF, normalized to a bandwidth equal to the bit rate, at which the bit synchronizer slips one or more bits in one out of 10,000 bit frames on the average.)
Data Output	Regenerated serial NRZ (M and C).
Monitors	Meters provided for input amplitude level, sync status (quality) and fine tuning.
Modes	Manual or automatic selection of up to 8 predetermined bit rates and other associated parameters.

PRIME FRAME SYNCHRONIZATION

Sync Word	7 to 64 bits.
Modes of Operation	Search, Check and Lock.
Aperture	0 to ± 1 bit, one setting applicable for both the check and lock modes.
Status Indicators	Search, Check and Lock with RESET to search available.

SUBFRAME RECYCLE SYNCHRONIZATION

Subchannels	512 or more depending on number of programs stored in memory.
-------------	---

Sync Word	7 to 64 bits.
Modes of Operation	Search and lock.
Status Indicators	Search and lock.

SUBFRAME ID SYNCHRONIZATION

ID Code Words	Up to 9 bits (MSB or LSB first).
Location	Any position in either a data word or sync word.
Status Indications	ID Error and ID Verified.

WORD SYNCHRONIZATION

Sync Word	Up to 6 bits.
Modes of Operation	Search, Check and Lock.
Aperture (Lock Mode)	0 bits.
Status Indicators	Search, Check, Lock and an ON indicator.

SUPERCOMMUTATION

Channels to be supercommutated are provided with the same data routing address.

PARITY

"ODD", "EVEN", or "NONE" available. The start of an ODD or EVEN parity count sequence is programmed or manual. A decimal display indicates up to 999 parity errors in 99 consecutive frames. Manual or remote reset.

STORED PROGRAM DECOMMUTATOR

Word Length	Any length; i.e., variable word length from 4 to 64 bits (wired for 4 to 33 and expandable to 64).
Word Rate	Prime or subcommutated word rates up to 200,000 per second.
Prime Frame Length	512 or more depending on arrangement of memory.
Subframe Length	Up to four independent subframe ratios can be accommodated with lengths to 512 words or greater. Subframe synchronizers may be set up to provide decommutation for sub-subchannels.
Programming	Accepts programs from computers, punched paper tapes or manually from the system control panel. A photoelectric paper tape unit is provided which accepts 1 inch 8 channel tape for programming.
Channel Stripping	Any combination of channels may be stripped from the total multiplex by stored program instructions.
Program Selection	Selection of any one of the stored programs may be made manually, automatically or remotely.

DIGITAL DATA OUTPUT CAPABILITY

MSB Parallel Binary	Up to 64 bits per word.
LSB Parallel Binary	Up to 64 bits per word.
BCD Multiplex	Up to 6 BCD characters per word.
BCD Storage	Up to 5 BCD stores of 6 digits each.
Binary Storage	Up to 5 binary stores of 33 bits each.
MSB Truncated	4 to 15 bits per character.
LSB Truncated	4 to 15 bits per character.
ON/OFF Storage	Capability provided for ON/OFF data storage in the binary storage registers.
Miscellaneous	Bits per word numbering; 6 binary bits. Sync Status Signals for all synchronizers. Word Numbering: 9 binary bits and 11 BCD bits. Channel Numbering: 36 binary bits and 24 BCD bits. Read-Out Commands: As required with each system output. End of Word Pulse. End of Prime Frame Pulse. End of Prime Frame Sync Word. Data flag to indicate good or bad data. Clock: Two output phases.
Serial Digital Data	NRZ-C and NRZ-M.
Output Waveform Characteristics	"ONE" level is -10 ± 4 , -0 volts; "ZERO" level is -0 ± 0 , -0.4 volts; rise and fall time less than 100 nanoseconds; and the output impedance is less than 93 ohms. In addition, the MSB output and one 12 bit binary data address are capable of driving up to 1500 feet of coaxial cable.

DATA DISPLAYS

Binary	One 64-bit indicator provided with thumbwheel channel selector switch.
Decimal	Three 6-digit decimal displays are provided for BCD data with thumbwheel channel selector switches.

ANALOG DATA OUTPUT CAPABILITY

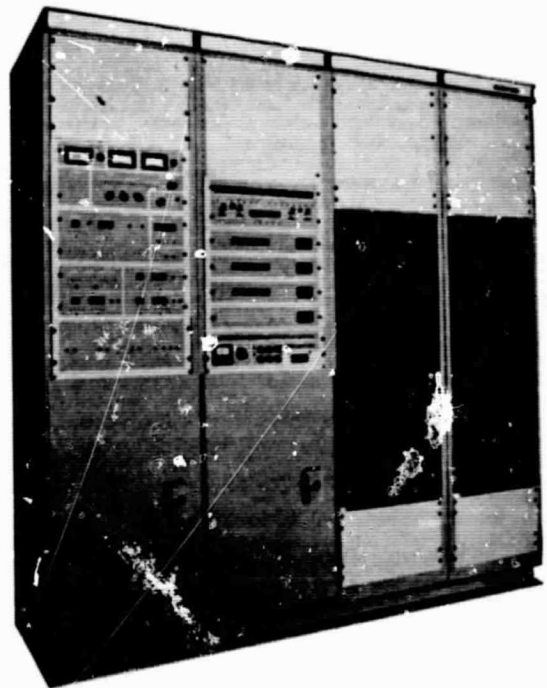
Voltage	0 to -5 volts.
Output Impedance	1K ohms (Lower output impedances optional).
Resolution	One part in 256.
Linearity	Better than 0.1%.
Long Term Stability	Better than 0.1% over temperature range from 25 to 50° C.

POWER REQUIREMENTS

Voltage	120 volts $\pm 10\%$, 57 to 63 cps, single phase.
Power	Less than 5000 watts.

PACKAGING

Size	Two assemblies, one 6' x 6' x 2' and one 6' x 2' x 2'.
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APPENDIX XIV

FIVE CHANNEL MOS TRANSISTOR

FUNCTIONAL TEST PROCEDURE

U. S. BLUE PRINT PAPER CO. CLEARPRINT 1000H

SYM	DESCRIPTION			DATE	APPROVED
	CHG BY	CHK BY	ECO NO.		

[illegible]

TEST PRECAUTIONS

1. Assure all electrical equipment is grounded by the third wire to electrical ground. Assure HP 425A microammeter is on current scale.
2. Only put flat packs in the holder with a 100K connection between common gates and drain.
3. When inserting MOS flat packs in holder or removing from holder the following precautions will be taken.

- A. Ground bench top.
- B. Attach ground straps from bench top to wrist.
- C. Plug empty flat pack holder into grounded connector and discharge to bench top.
- D. Discharge hands and tweezers to bench top.
- E. Discharge flat pack container foil to bench top.
- F. Insert flat package in its holder. Assure 100K connection is closed.
- G. Closely check pin numbers of flat pack and holder.

Repeat above process when removing MOS flat pack from its holder and always store flat pack in metal foil container.

4. Always plug flat package into connector called for in procedure when designated.
5. Always assure flat pack faces operator so that pin 1 in connector corresponds to pin 1 in flat pack.
6. Assure power supply cannot cause overvoltage transients.
7. Do not use soldering iron while testing transistors.



CODE IDENT NO.

91417

SIZE

A

108810

REV

SCALE

SHEET 2

- 1.00 Disconnect voltmeter. Record serial number of flat pack.
- 1.01 Adjust power supply #1 to 25V DC.
- 1.02 Adjust power supply #2 to 0V DC.
- 1.03 Switch SW-1 to OFF position.
- 1.04 Switch SW-2 to (-) position.
- 1.05 Plug flat pack holder into connector #1.
- 1.06 Connect ammeter ground clip to terminal #A and power tip to terminal #1.
- 1.07 Switch SW-1 to (+) position.
- 1.08 Record current on data sheet.
- 1.09 Adjust power supply #2 from 0V DC to 25V DC.
- 1.10 Record current on data sheet.
- 1.11 Switch SW-2 to (+) position.
- 1.12 Record current on data sheet.
- 1.13 Switch SW-1 to OFF position.
- 1.14 Remove flat pack holder from connector #1.
- 1.15 Remove current probe from terminal #1.
- 2.01 Plug flat holder into connector #2.
- 2.02 Connect current probe to terminal #2.
- 2.03 Switch SW-1 to (+) position.
- 2.04 Remove wire plugged into flat pack holder. Don't panic!
- 2.05 Record current on data sheet.
- 2.06 Plug in wire that was removed on flat pack holder.



CODE IDENT NO.	SIZE		REV
91417	A	108810	
SCALE	SHEET 3		

- 2.07 Switch SW-1 to (-) position.
- 2.08 Remove wire plugged into flat pack holder.
- 2.09 Record current on data sheet.
- 2.10 Plug in wire that was removed on flat pack holder.
- 2.11 Switch SW-1 to OFF position.
- 2.12 Remove flat pack from connector #2.
- 2.13 Remove current probe from terminal #2.
-
- 3.01 Plug flat pack into connector #3.
- 3.02 Switch SW-1 to (-) position.
- 3.03 Connect current probe to terminal #S1-3.
- 3.04 Record current on data sheet.
- 3.05 Connect current probe to terminal #S2-3.
- 3.06 Record current on data sheet.
- 3.07 Connect current probe to terminal S3-3.
- 3.08 Record current on data sheet.
- 3.09 Connect current probe to terminal S4-3.
- 3.10 Record current on data sheet.
- 3.11 Connect current probe to terminal S5-3.
- 3.12 Record current on data sheet.
- 3.13 Adjust power supply #1 to 40V DC.
- 3.14 Repeat paragraph 3.03 to 3.12 recording current on data sheet.
- 3.15 Adjust power supply #1 back to 25 V DC.
- 3.16 Switch SW-1 to OFF position.



CODE IDENT NO.

91417

SIZE

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108810

REV

SCALE

SHEET 4

- 3.17 Remove current probe from terminal S5-3.
- 3.18 Remove flat pack holder from connector #3.
- 4.01 Connect voltmeter across power supply #1.
- 4.02 Adjust power supply #1 to 6.5V DC.
- 4.03 Switch SW-2 to (-) position.
- 4.04 Plug flat pack holder into connector #4.
- 4.05 Switch SW-1 to (-) position.
- 4.06 Connect current probe to terminal #S1-4.
- 4.07 Record current on data sheet.
- 4.08 Connect current probe to terminal #S2-4.
- 4.09 Record current on data sheet.
- 4.10 Connect current probe to terminal #S3-4.
- 4.11 Record current on data sheet.
- 4.12 Connect current probe to terminal #S4-4.
- 4.13 Record current on data sheet.
- 4.14 Connect current probe to terminal #S5-4.
- 4.15 Record current on data sheet.
- 4.16 Adjust power supply #1 to 1V DC.
- 4.17 Repeat paragraph 4.06 to paragraph 4.15. Recording current on data sheet.
- 4.18 While connecting current probe to S1-4 through S5-4 adjust power supply #2 until ammeter is at 10 ua. The voltage adjusted to will be recorded on data sheet.



CODE IDENT NO.	SIZE		REV
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SCALE		SHEET 5	

- 4.19 Switch SW-1 to OFF position.
- 4.20 Remove current probe from terminal #S5-4.
- 4.21 Remove flat pack holder from connector #4.
- 5.01 Plug flat pack holder into connector #5.
- 5.02 Connect current probe to terminal #5.
- 5.03 Switch SW-1 to (-) position.
- 5.04 Adjust power supply #1 to 40V DC.
- 5.05 Remove wire plugged into flat pack holder.
- 5.06 Record current on data sheet.
- 5.07 Plug in wire that was removed on flat pack holder.
- 5.08 Adjust power supply #1 to 25V DC.
- 5.09 Switch SW-1 to OFF position.
- 5.10 Remove flat pack holder and insert into common grounded connector.
- 5.11 Sign and date data sheet.
- 5.12 Follow safety precautions to put flat pack into its proper container.
- 6.01 If leakages in section 2.0 or 3.0 exceed limit rerun 2.01 to 3.12 with same empty flat pack holder used during test. Record flat pack holder leakage on data sheet.



CODE IDENT NO.

91417

SIZE

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REV

SCALE

SHEET 6

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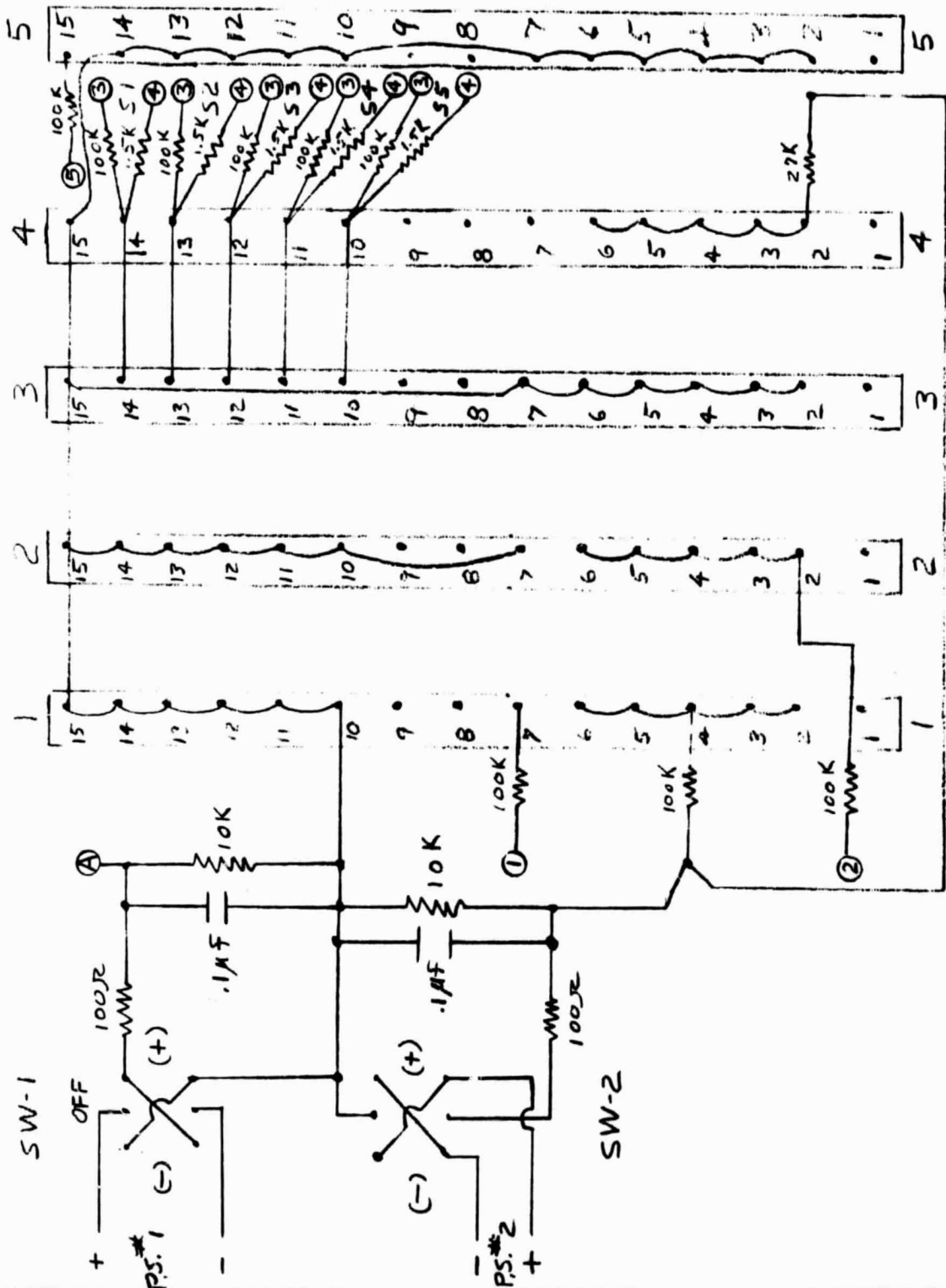


FIGURE 1 TEST CIRCUIT SCHEMATIC



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SCALE

SHEET 7

RAD FORM 459-1 REV 12-62

XIV-8

DATA SHEET

Record serial number of flat pack under test _____.

Related Para. #	Test	Symbol	Terminal Data	Limit
1.08	Drain-Body & Source Body Leakage Current	$I_{BD} + BS$	1 - - -	< 1na
1.10			1 - - -	< 1na
1.12			1 - - -	< 1na
		F.P.Holder Leakage		
2.05	Gate Input Current	- - - -	2 - - -	< 20pa
2.09		- - - -	2 - - -	< 20pa
3.04	Source to Drain Leakage Current	- - - -	S1 - 3 - - -	< 100pa
3.06		- - - -	S2 - 3 - - -	< 100pa
3.08		- - - -	S3 - 3 - - -	< 100pa
3.10		- - - -	S4 - 3 - - -	< 100pa
3.12		- - - -	S5 - 3 - - -	< 100pa
3.14	Source to Drain Breakdown Leakage @ 40V	I_{DSSI}	S1 - 3 - - -	< 1 ua
			S2 - 3 - - -	< 1 ua
			S3 - 3 - - -	< 1 ua
			S4 - 3 - - -	< 1 ua
			S5 - 3 - - -	< 1 ua

DATE OF TEST _____

TEST OPERATOR _____



CODE IDENT NO.

91417

SIZE

A

108810

REV

SCALE

SHEET 8

DATA SHEET

Record serial number of flat pack under test _____.

<u>Related Para. #</u>	<u>Test</u>	<u>Symbol</u>	<u>Terminal Data</u>	<u>Limit</u>
4.07	On Current	I_{SDS}	S1 - 4 - - -	> 1ma
4.09			S2 - 4 - - -	> 1ma
4.11			S3 - 4 - - -	> 1ma
4.13			S4 - 4 - - -	> 1ma
4.15			S5 - 4 - - -	> 1ma
4.17	Dynamic Drain Current	I_{IS}	S1 - 4 - - -	> 330ua
			S2 - 4 - - -	> 330ua
			S3 - 4 - - -	> 330ua
			S4 - 4 - - -	> 330ua
			S5 - 4 - - -	> 330ua
4.18	Gate Threshold Voltage	V_{GST}	S1 - 4 - - -	3V-9V
			S2 - 4 - - -	3V-9V
			S3 - 4 - - -	3V-9V
			S4 - 4 - - -	3V-9V
			S5 - 4 - - -	3V-9V
5.06	Drain to Source Breakdown Voltage	BV_{DSS}	5 - - -	< 5ua

DATE OF TEST _____ OPERATOR _____

DATA REVIEWED BY _____ DISCREPANCIES _____

**RADIATION
INCORPORATED**

CODE IDENT NO.

91417

SIZE

A

108810

REV

SCALE

SHEET 9

APPENDIX XV

GLOSSARY

Glossary Terms

A-D-Analog-to-Digital

A process for converting an analog signal to a digital signal.

"A"- Data

Data handled by "A" unit of airborne Telemetry System. Differs from "B" data handled by "B" unit. The "A" data signal is at a 500 cps bit rate, gated sine wave type modulation. A single cycle represents a "0" bit (see waveforms, figure XV-1) and the absence of a cycle of the sine wave represents a "1" bit, "A" data is transmitted at two rates defined as A'Real which is at real time 500 cps bit rate and A-Stored which is at 15 kc bit rate derived from airborne tape playback at 1:30 speed increase.

A- Real

"A" data transmitted at real time bit rate of 500 cps.

A - Stored

"A" data transmitted from magnetic tape stored playback at 1:30 tape speed increase resulting in 15 kc bit rate.

A Unit

The continuous operating multi-coder unit which samples 542 channel at a 500 cps bit rate. This data is stored on magnetic tape for subsequent read out.

Barker Code

A binary code suitable for PCM frame synchronization having optimal correlation properties with the unique property when decoded of relative immunity to phase displacement by random pulses immediately adjacent to the pattern, and relative immunity to phase displacement error in the transmitted code. Reference: Communication Theory; Willis Jackson; Academic Press Inc., London, 1953.

BCD - Binary Coded Decimal

A method of indicating an arabic numeral 0-9 by using 4 or more binary digits. Common weighting of bits are 1, 2, 4, 8; 1, 2, 4, 4; and 1, 2, 2, 4.

"B" Data

Data handled by "B" unit of the NIMBUS Airborne Telemetry System. The "B" data signal has a 10 kc video carrier frequency biphasic (split phase) modulated by a 10 cps bit rate. (See waveform figure XV-1.)

Bit - Abbreviation of "binary digit"

A single character having two distinct states of a binary word. "0" bit and "1" bit are common definitions for the two states (others are true/false, true/complement, yes/no, etc.)

Bit Synchronizer

A logic assembly in the NIMBUS PCM Ground Station that receives the serial PCM data train from which it generates synchronized bit rate timing and regenerates noise-free serial NRZ data.

Bit Interval

The time duration of single bit.

Bit Rate

The repetition frequency of bits.

Beacon Transmitter

The 136 Mc. amplitude modulated transmitter used for transmitting the PCM telemetry data to the ground station.

B Unit

This multi-coder unit samples 125 channels at a 10 cps bit rate and operates for one frame upon command.

CDC

Control Data Corporation. Manufacturer of the computer used with the NIMBUS PCM Ground Station.

Clock

A primary source of synchronizing signals.

Coder

The circuitry used to convert the sampled analog inputs to a digital code.

CSR

Counter Shift Register - A bistable logic element used in the NIMBUS system as a binary counter, memory stage or shifting register.

D C Restoration

The process of establishing a dc component to a signal.

Decom

Abbreviation for Decommutator. A logic assembly in the NIMBUS PCM Ground Station whose function is to provide patch board selectable signals to demultiplex (sort out) individual data channels.

Differentiator

A logic assembly in the NIMBUS PCM Ground Station whose output waveform is negative going pulse triggered from a positive going edge of a waveform. (See NIMBUS PCM Ground Station Instruction Manual for circuit and details).

Digital Output

The magnitude of a stimulus represented in the form of a series of discrete quantities coded in a system of notation, distinguished from analog output.

D-A - Digital-to-Analog

A process for converting digitally coded data to an analog or continuous function signal representing a measured parameter. In PCM systems this usually involves decoding a group of binary bits by summing their defined analog voltages or current weights resulting in a signal whose amplitude represents the measured parameter.

Exclusive - OR

A logic circuit used in the NIMBUS PCM Ground Station to perform bit comparisons in binary word comparators performing the logical expression $(A \cdot B) + (\bar{A} \cdot \bar{B}) = C$.

Flip-Flop

A bistable multivibrator.

F₀

A letter symbol used in the NIMBUS PCM Ground Station description defined as bit rate occurring at beginning of the bit interval.

F₀'

Same as F₀ except delayed in time occurring in the middle of the bit interval.

Flywheeling

A descriptive term denoting the condition of system timing running but not synchronized with or there is no indication of synchronization with the reference timing. In the case of the Ground Station "flywheeling" denotes the system timing is functioning not under control of or synced with the input data (there may be no input) but at a sustaining or search mode determined by characteristics of bit synchronizer timing loop.

Frame

A group of words comprising one cycle of a commutator.

Gated Sine Wave

Describes present NIMBUS "A" data signal modulation. A complete cycle of a sinewave at the bit rate represents a "0" bit and the absence (sine wave gated off) of a cycle represents a "1" bit (see waveform figure XV-1.)

Group Synchronizer

A logic assembly in the NIMBUS PCM Ground Station that searches the serial bit synchronized data train for recognition of word sync and frame sync patterns which enable it to provide parallel data output word rate, and frame start timing.

Half Shot (Similar to Ground Station Term Differentiator)

A circuit which puts out a pulse whose width is determined by an R C time constant. The circuit must be activated by a pulse having a greater width than the required output pulse width.

ISR

Input Shift Register. A logic group in the Group Synchronizer Assembly in the Ground Station comprising 20 storage stages with buffered drivers arranged to accept the serial NRZ bit train and shift it sequentially at bit rate through the complete register. Thus a maximum of 20 bits are available for broadside read.

Integrate and Dump

A portion of the bit decision logic in the Bit Synchronizer of the Ground Station. The serial data is routed to an R-C integrate circuit for a portion of the bit interval controlled by synchronized loop timing. At or near the end of the bit period a level decision is made on the integrate circuit and it is then "dumped" (discharged) to ground in a short interval ready to process the next bit.

Integrated Circuit

A complete electronic circuit produced as a unit by micro electronic techniques.

Major Frame

The lowest frequency frame in the format constituting one complete sampling cycle of the multiplexer in which each transducer input is sampled at least once. In the NIMBUS format an "A" data major frame is 1024 words (16 minor frames) long.

Master Clock

The telemetry subsystem unit which provides frequency standards, time code signals, command outputs and motor drive frequencies.

Matched Filter

A circuit whose function is to filter the combination of signal and noise, so as to maximize the ratio of peak signal voltage to rms noise at the system output. Reference: Information Transmission, Modulation, and Noise; Mischa Schwartz.

Micro electronics

The art of miniaturizing electronic components.

Mincom

Manufacturer of the analog tape recorder used in the Ground Station. Mincom Div., Minnesota Mining and Manufacturing Co.

Minitract Time Code

A pulse width modulated serial code train which provides satellite time data in binary coded decimal form.

Minor

A frame of lower frequency than the prime frame. Also referred to as subframe. In the NIMBUS format a minor frame is 64 words long, and there are 16 minor frames per major frame.

MOSFET

Metal oxide semiconductor field effect transistor.

MSMV

Monostable multivibrator (one-shot, single shot).

Multicoder

The subsystem unit containing the A and B unit multiplexers and two analog to digital converters.

Multiplexer

The circuitry used to sequentially sample the inputs from the telemetry transducers.

Nixie

A trade name for a neon glow type indicator tube with switching circuits manufactured by Burroughs Corporation.

NOR

A logic circuit used in the NIMBUS Telemetry System. See the instruction manual for circuit specifications.

NRZ

Non-return-to-zero. A binary signal waveform whereby the state of the bit is defined by a level or a change of a level. (See waveform figure for various type of NRZ). This signal differs from RZ (return-to-zero) in that there is no defined start or finish (t_0) reference level.

OSR

Output Shift Register. A group of logic in the Group Synchronizer assembly in the Ground Station comprising 7 stages of storage with broadside input and output routing data words to rest of the system.

Patch Panel

A grouping of circuit terminals and mating plug-in cords for selectable routing of signals used in the Decommutator assembly of the Ground Station. The specific function in the Ground Station is the patching of the necessary transfer signal to decommutate any desired data channels for display on any of the available 32 analog recorder traces.

PCM

Pulse code modulation, in which the modulating wave is sampled quantized and coded. Also used to designate the unit which performs this function.

PI - Power Inverter

A logic circuit used in the Ground Station as an inverting stage, buffer and driver. See the Instruction Manual for detailed circuit.

PINCH Unit

Planar Integrated Chopper.

Prime Channel

A data channel sampled once per prime frame.

Prime Frame

The highest frequency frame containing a sync pattern (also referred to as a "minor frame").

Programmer

A term used to include the synchronizer and its associated multiplexer matrix.

P.S.C.

Power supply common, this is the return line for the primary -24.5 volt power supply in the Airborne Telemetry System.

Register

One or more bistable storage stages used to group, sort or store binary bit addresses.

RZ

Return-to-zero - A binary signal waveform the state of the bit is defined by a voltage level but differs from NRZ in that the signal starts from a reference level and returns to this level after defining the bit. (See waveform figure XV-1.)

RZ/NRZ Converter

The circuit which converts the return-to-zero pulses from the output shift register to a non-return-to-zero coded output.

Serializer

A group of logic that performs parallel-to-serial data conversion.

SFID

Subframe Identification. In the NIMBUS format, a 4-bit word following the frame sync pattern identifies the prime (minor, sub) frame by number 0-15.

Shift Register

A group of bistable stages so connected that a shift signal will cause a transfer of stored bits from one to the next. The Ground Station uses a standard CSR logic circuit for each stage of such a register.

S P - Split Phase

A binary signal waveform whereby the bit state is defined by the phase or change of phase of the signal. (See waveform figure for various types of split phase). In the airborne signal recording process for split phase (diphase or frequency doubling) a "0" bit is represented by two pulses of current in the same direction, each pulse lasting for half a bit time. A "1" is represented by two pulses of current in opposite directions.

Squelch

A two level (on or off) control signal developed in the Control Drawer of the Ground Station to automatically switch circuit operation to process the different types of (A-real, A-stored, time code and "B") data. The squelch circuits are essentially separate tuned circuits and saturable switches set to detect the different bit rates of each type of data.

Subcommutated channels

A channel sampled at a rate lower than the prime (minor) frame rate.

Subframe

Usually referred to as a frame of lower frequency than the prime frame; however, in reference to the NIMBUS format this term is used interchangeably with prime frame and minor frame.

Standby Clock

This circuit in the Telemetry Electronics provides 500 cps bit rate and two phase 100 cps for A unit operation in the event of failure of the Master Clock.

Stored Data

The data from the A unit multi-coder which has been stored in the magnetic tape recorder unit.

Staticizing Register

This term is used to denote the input bit storage register portion of the D-A converters in the Ground Station.

Strobe

A logic signal usually a short pulse used to query condition of logic gates at a particular time.

Sync Acquisition

The process of attaining synchronization of the system timing with (in the Ground Station) input data train.

Sync Confidence

A signal generated by the Ground Station Group Synchronizer denoting the status of the combined attainment of bit sync, frame sync and (when selected by switch) word sync and SFID. This signal is routed to the rest of the system indicating data is valid.

Synchronizer

In the Airborne Telemetry System this term refers to the binary counters used to provide timing for sampling the multiplexer gates.

Tape Transport

The electro mechanical portion of the airborne tape recorder, including drive motors, tape and tape head. The record-playback amplifiers are located in the Telemetry Electronics unit.

TME - Telemetry Electronics

The subsystem unit containing the switching relays for selecting the desired data output and controlling the tape transport operational mode. It also provides the electronic circuits for the stored data and an emergency clock unit.

Unitary

A coding system in which each character has a single state or value. Commonly used in phrase binary-to-unitary converter whereby a n -bit binary input define 2^n discrete values and therefore the unitary output require 2^n outputs.

VCO

Voltage Controlled Oscillator.

Video

This term is used in the description of the Ground Station operation denoting the Ground Receiver (demodulated) output signal.

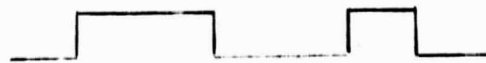
Window

A term used to describe a timing check interval. Usually a window (search period) is generated by system timing to occur around the time of an expected event enabling check logic to verify the occurrence.

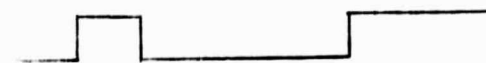
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BINARY
BIT STATE

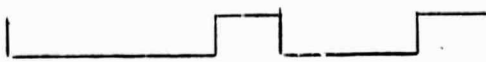
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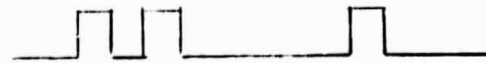
NRZ NRZ (C) NRZ (L)



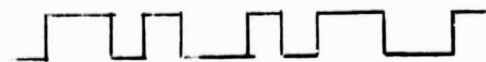
NRZI NRZ(M)



NRZI NRZ(S)



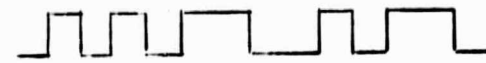
RZ



SPLIT-PHASE BI-PHASE MANCHESTER



SPLIT-PHASE (M)



SPLIT-PHASE (S)



GATED SINE WAVE

"B" DATA

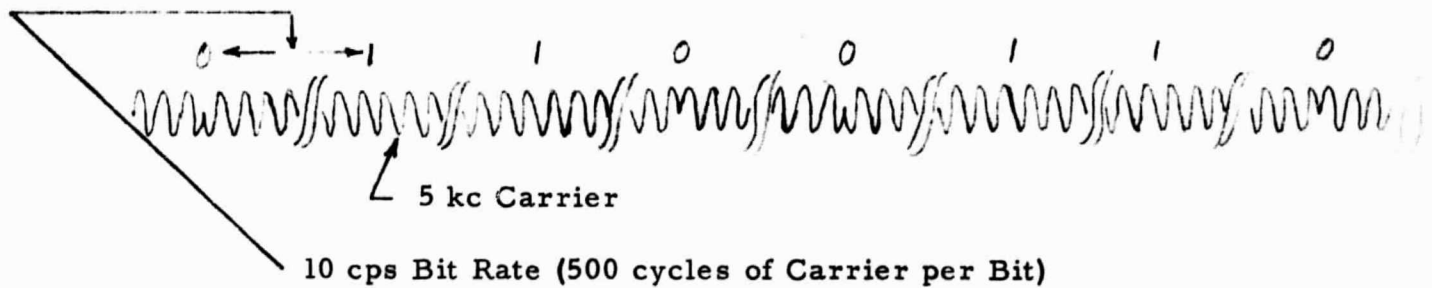


Figure XV-1. Waveforms