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FOR
NIMBUS DESIGN STUDY
CONTRACT NO. NAS 5-3787

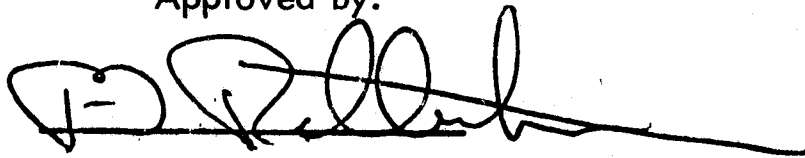
Prepared by
RADIATION INCORPORATED
MELBOURNE, FLORIDA
For
GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND

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Approved By:

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Project Manager

ABSTRACT

This addendum to the Final Report for Contract No. NAS 5-3787 describes the study required because of inadequacies noted in the Nimbus PCM initial design study and noted in the Final Report. In addition, a reliability improvement study was performed (report submitted under separate cover). As a result of this study, an electrical model PCM telemetry subsystem was fabricated and tested. This system consisted of a PCM Telemetry Unit and a Telemetry Electronics Unit. These units were electrically and physically compatible with the Nimbus Spacecraft as described in the Nimbus B PCM Telemetry Subsystem specification dated February 1965, except that the units were designed to meet only the temperature cycling environmental requirements specified therein. The model was packaged in the smallest possible Nimbus module that utilized components and techniques directly applicable to flight system design and fabrication. The model had improved package design, improved connectors, added digital channel capability, telemetered time code, synchronization with the spacecraft clock, extensive block redundancy, increased channel fault voltage, saturated recording, improved sync capability, greater immunity to variations in spacecraft power, and increased coding resolution on selected channels. The B telemetry and standby clock were removed.

The increased electrical capability, including a PCM that was redundant except for the input channel gates, was packaged one-half the size of the Nimbus I and II PCM system.

The new system operates within specifications, provides increased capability with an increase in reliability, and permits a substantial decrease in volume. These improvements were attained with only a minor increase in power consumption.

The scope of the study extension also included breadboard modifications to one Bench Test Equipment (to demonstrate the new system capabilities) and modifications to Ground Station No. 2 for compatibility with the new electrical model.

The modifications to Ground Station No. 2 included the addition of an improved bit synchronizer, addition of digital channel decommutation capability, addition of an event recorder, and additional capabilities to process split-phase data and to display time code. Also included were modifications to allow synchronization with new format and modifications to the simulator to allow testing of the new ground station capabilities.

After the system was fabricated and successfully demonstrated at Radiation Incorporated's facilities, the new Electrical Model and the Ground Station modifications were delivered to the General Electric Company.

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SECTION I

GENERAL

1.0 INTRODUCTION.

This addendum contains information and data obtained during the extension of the Nimbus Design Study, Contract NAS 5-3787. The study extension included: design and fabrication of new airborne equipment (PCM Telemetry Subsystem), comprised of a PCM unit and a telemetry electronics unit (TME) (figure 1); modification of PCM Ground Station System 2 (figure 2); and breadboard modification of one Bench Test Equipment (BTE) (figure 3) sufficient to demonstrate the new system capability.

Discussions and supporting illustrations are presented, as follows:

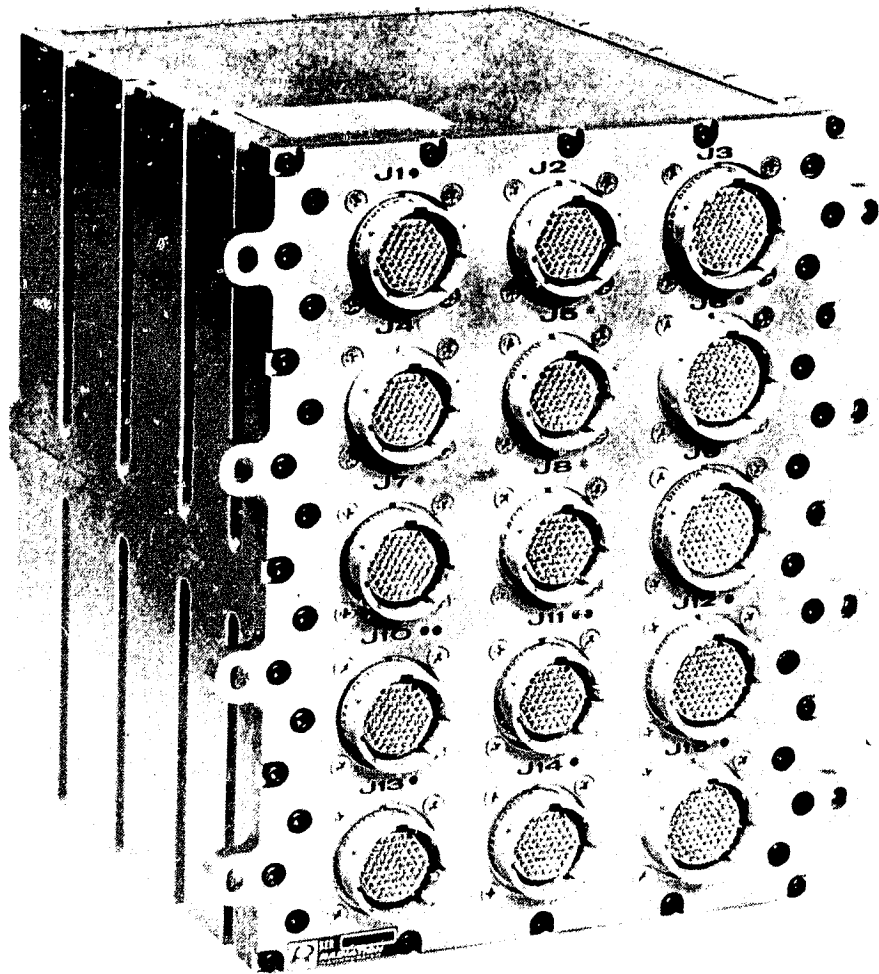
- a. Volume 1: Section I — General
 Section II — Detailed Discussion
 Section III — New Technology
- b. Volume 2: Appendix I — Drawings
 Appendix II — Failure Reports
 Appendix III — Failure Rate Data Sheets
 Appendix IV — Mechanical Model Test Report
 Appendix V — Encoding Accuracy
 Appendix VI — Use of 10-Bit Coding Capability
 Appendix VII — MOSFET Handling
 Appendix VIII — Glossary of Terms

Detailed table of contents, list of tables, and list of illustrations provide easy access to particular areas of interest. Generally, tables, charts, and simplified diagrams are included with the text; detailed logic and schematic diagrams are presented in Appendix I.

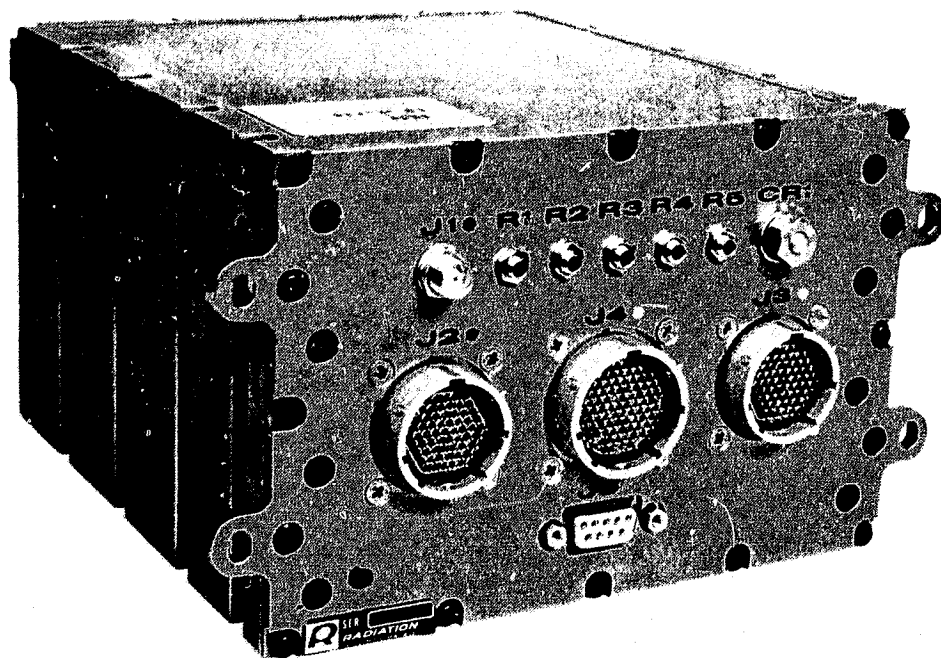
1.1 SCOPE.

The purpose of the original Nimbus Design Study was to provide digital channel capability and add time code to the PCM code train with minimum modification to Nimbus A System equipments. Results of this study included a change in modification from gated-sine wave to digital recording techniques to improve the air-to-ground signal-to-noise ratio, as detailed in the Final Report for Nimbus Design Study dated 1 February 1965.

During the study extension, original study results were expanded and improved into the present system configuration, and a reliability study was conducted to determine the amount of redundancy required for the Nimbus Program. The scope of work involved in the study extension is discussed in the following paragraphs.



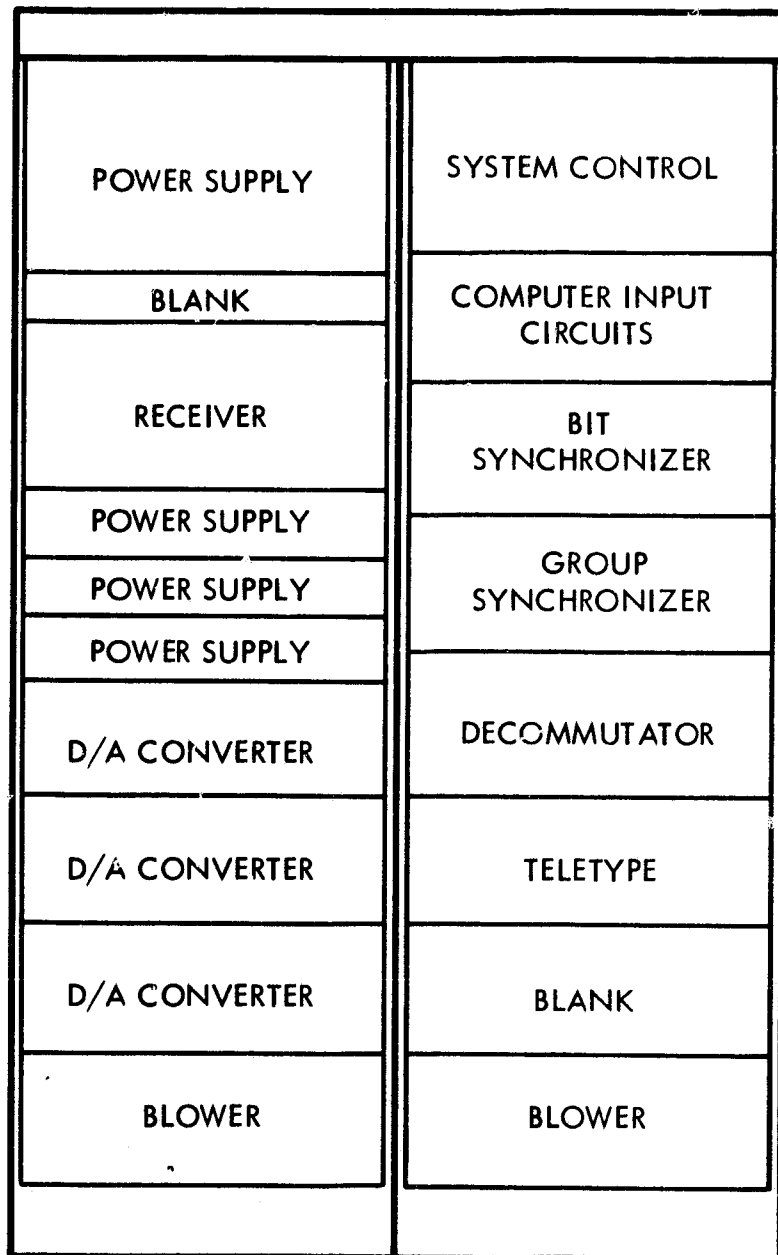
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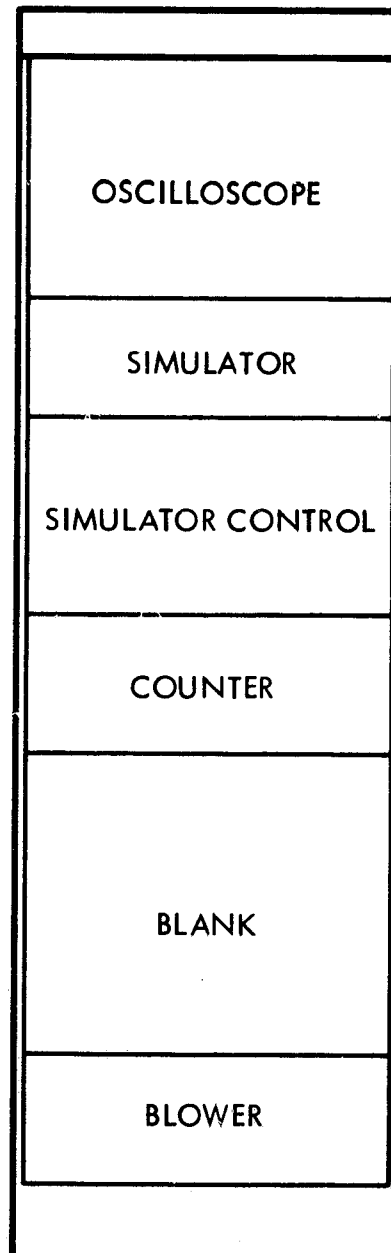
TME

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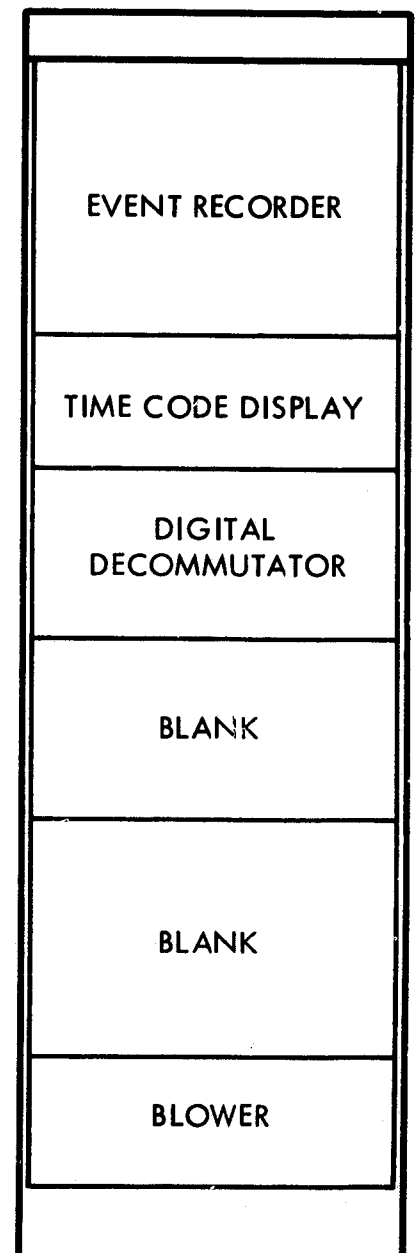
Figure 1. PCM and TME Units



CONTROL ELECTRONICS (CABINET 3/4)



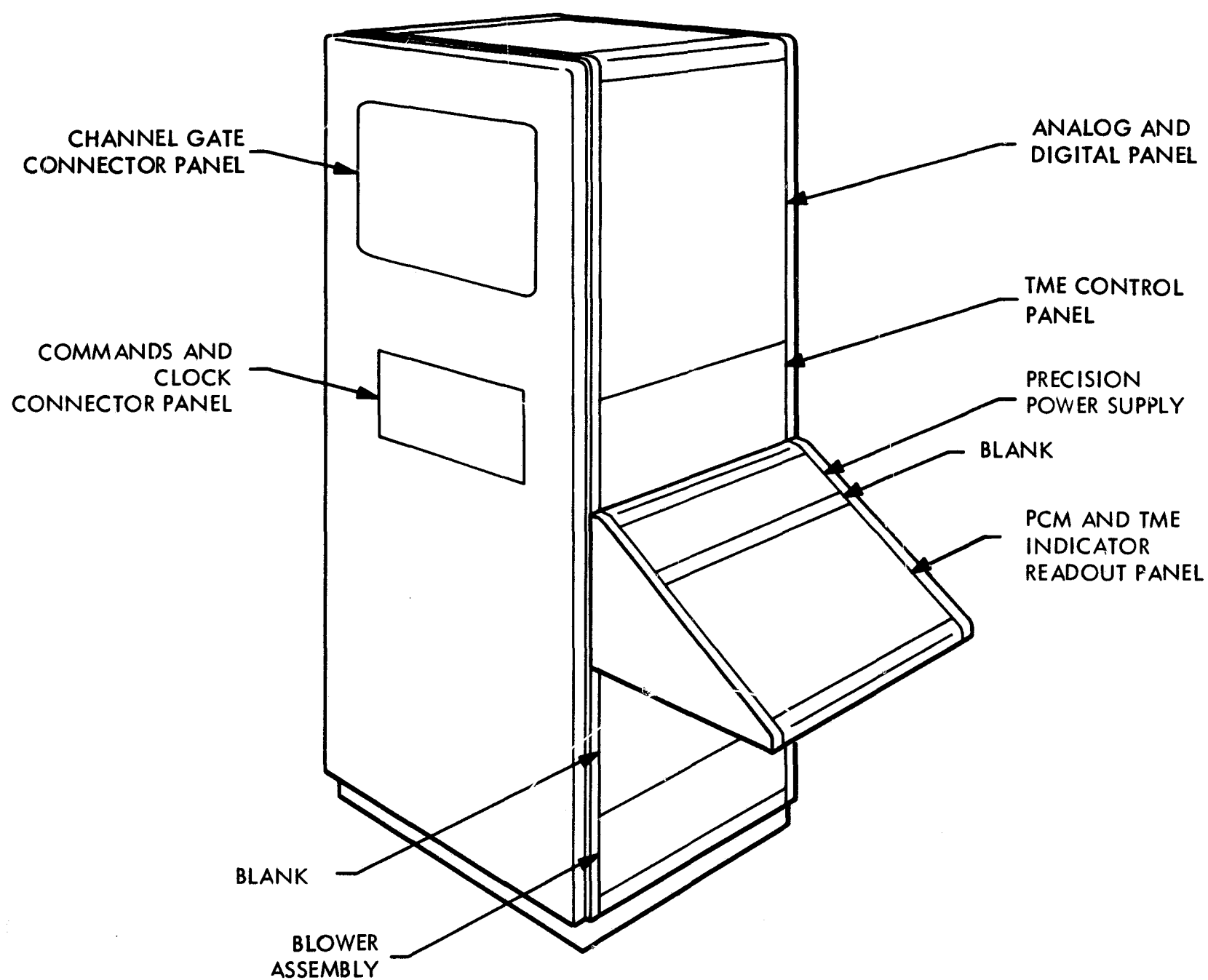
SIMULATOR AND TEST EQUIPMENT (CABINET 5)



EVENT RECORDER AND TIME DISPLAY (CABINET 6)

57510

Figure 2. PCM Ground Station System 2, Front View



57509

Figure 3. Bench Test Equipment, Front View

1.1.1 AIRBORNE EQUIPMENT SCOPE OF WORK.

A new PCM Telemetry Subsystem was designed and built to provide increased capability and improved performance over the Nimbus A and C systems as well as the preliminary study model. The mechanical scope of work involved the electrical and mechanical packaging of the PCM and TME units. The task was to package each unit in the smallest possible Nimbus module, using components, materials, and techniques that could be applied directly to the Nimbus B units. The resulting PCM Telemetry Subsystem has the following major characteristics:

- a. Nonredundant analog channel input gates, with a maximum of eight channel gates per output sequencer.
- b. Nonredundant digital channel input gates, with a maximum of 5 channel gates per sequencer.
- c. Block-redundant facilities, as follows:
 - (1) Analog-to-Digital Converters in PCM
 - (2) DC-to-DC Converters in PCM
 - (3) Programmers in PCM
 - (4) Output Registers and NRZ-to-Split-Phase Converters in PCM
 - (5) Time Code Converters in PCM
 - (6) Sync and ID Converters in PCM
 - (7) Analog and Digital Multiplexer Control Circuits in PCM
 - (8) Record Amplifiers in TME
 - (9) Playback Amplifiers in TME
 - (10) Summing Amplifiers in TME
 - (11) Tape Recorders (Raymond)
 - (12) Transmitters (Hughes)
- d. Increased fault voltage protection and analog and digital channel gates.
- e. Increased protection with proper system operation over an increased voltage range of the Nimbus regulated bus.
- f. Increased total channel capability.
- g. Size of new PCM box reduced to 1/2 of the Nimbus A PCM box size.
- h. Box connectors changed to a more reliable type.
- i. Boxes designed to withstand much higher G levels.
- j. Split-Phase Mark 0 Code for recording on tape and for modulating transmitters.
- k. Two tape recorder circuits for 2-orbit capability.

1.1.2 GROUND STATION EQUIPMENT SCOPE OF WORK.

PCM Ground Station System 2 was modified to make the data handling capabilities compatible with the new Nimbus B format. Requirements for additional display and recorder facilities were satisfied by inclusion of a digital data recorder and a time code display unit.

1.1.3 BENCH TEST EQUIPMENT SCOPE OF WORK.

The Nimbus A bench test equipment (BTE) was modified to permit checkout of the new PCM Telemetry Subsystem that was designed and built during the study extension. The modified BTE was used only one time to perform the PCM Subsystem demonstration test and to provide data for the demonstration test data sheets. The BTE design was adequate to perform the demonstration of all PCM Telemetry Subsystem design objectives. After successful completion of the demonstration test, the BTE was disassembled so that some of the hardware can be used in the BTE's for Nimbus B.

1.2 NIMBUS A AND NIMBUS B PCM SUBSYSTEM COMPARISON.

The following paragraphs and supporting charts compare Nimbus A and Nimbus B Subsystem capabilities and discuss modification of existing equipment and addition of new equipment required to support Nimbus B.

1.2.1 PCM UNIT.

1.2.1.1 ELECTRICAL CHARACTERISTICS. Nimbus A and Nimbus C PCM units are capable of sampling analog transducers only so that, if digital transducers were sampled, seven bits of data (instead of one bit) would be required in the output format. These systems are very inefficient. To solve this problem, the Nimbus B PCM unit has digital as well as analog channel capability. Figure 4 presents a comparison between Nimbus A and Nimbus B PCM output formats.

PCM Output Format	Nimbus A	Nimbus B
Sync and ID Channels (1 SPS)	2*	2.5*
Prime Analog Channels (1 SPS)	30	21
Subcommutated Analog Channels (1/16 SPS)	512	434
Time Code Channels (1/16 SPS)	0	42 (six 7-bit words)
Prime Digital Channels (1 SPS)	0	63 (nine 7-bit words)
Subcommutated Digital Channels (1/16 SPS)	0	280 (forty 7-bit words)
Total Channels	542	799**
Bit Rate	500 cps	500 cps
Word Rate	62.5 cps	62.5 cps
Subframe Rate	0.976 cps	1 cps
Major Frame Rate	16.39 seconds	16 seconds
Bits Per Word	8	8
Words Per Subframe	64	62.5
Subframe Per Major Frame	16	16
* Nimbus A unit-sync words all "1's" or all "0's"; Nimbus B unit-sync words selectable by bit in any combination of "1's" and "0's."		
** 454 analog, 343 digital, and 1 time code.		

Figure 4. PCM Output Format Comparison Chart - Nimbus A Versus Nimbus B

Although analog channel capability has decreased slightly, digital channel capability has increased from 0 to 343 channels. In addition, Nimbus C clock time code of seconds, minutes, and hours was added to the PCM data, and the number of sync bits was increased to improve data recovery and handling capabilities.

The Nimbus B PCM Telemetry Subsystem has the following input channel capability:

- 21 Prime Analog Channels at 1 sample per second (SPS)
- 63 Prime Digital Channels at 1 SPS
- 434 Subcommutated Analog Channels at 1/16 SPS
- 280 Subcommutated Digital Channels at 1/16 SPS
- 1 Subcommutated Time Code Channel at 1/16 SPS (consisting of units and tens of seconds, minutes, and hours)

Figure 5 is a PCM function comparison chart that shows the major differences between Nimbus A and Nimbus B PCM Telemetry Subsystem electronics.

PCM Function	Nimbus A	Nimbus B
Output Code	NRZ	Split-Phase/Mark 0
Power	0.75 watts (approximate)	1.75 watts (approximate)
Analog-to-Digital Converter	Pulsed power 7-bit weighted current	Continuous power 10-bit ramp current
Power Supply	None	DC-to-DC converter
Multiplexer	Magnetic core and "bright switches" - analog only	MOSFET - analog and digital
Fault Voltage Range	0 to -10 volts	+0.5 to -35 volts
Line Voltage Range	-22 to -26 volts	-18 to -35 volts
Output Register	Magnetic core	Transistor
Programmers	Magnetic cores and transistors	Transistors
Analog Gates per Sequencer	16	8
Digital Gates per Sequencer	None	5
Major Frame Sync Pulse Outputs	No	Yes
Synchronous with Clock	No	Yes

Figure 5. PCM Function Comparison Chart - Nimbus A Versus Nimbus B

1.2.1.2 MECHANICAL CHARACTERISTICS. The mechanical packaging of the Nimbus B PCM utilizes a compression-packaged technique first proven on the Nimbus A and Telstar PCM telemetry systems. In utilizing this technique, the electronics are integrated into what is effectively one mass, allowing a thin-walled light-weight housing design to be utilized. This housing design is possible because the walls of the unit are in tension only, while the bending moment is applied to the rigid ends of the housing. In both Nimbus A and B systems, weights of these end panels are minimized, while rigidity is maintained by drilling holes in the panel, which are then filled with foam. The rigidity is enhanced in the Nimbus B unit by adding a bonded-on panel, thus creating a "sandwich" structure. Characteristics of the Nimbus A and B systems are compared in figure 6.

Characteristic	Nimbus A	Nimbus B
Size	8" x 6" x 13"	8" x 6" x 6-1/2"
Weight	22 lbs.	13.5 lbs.
Housing		
Design	Open-ended Box	Closed Box
Finish	Chromate Dip	Electroless Nickel
Connectors		
Manufacturer	U.S. Components	Deutsch
Type	Special Rectangular	Standard Cylindrical
Environmental Protection	No	Yes
Locking Device	Screw-lock	Bayonet-lock
Packaging Concept		
Printed Circuit Card Type	2-sided cards	2-sided/6 layer M/L
Internal Connections	Card Connectors	Feed-through Bus Wires and Hard-wiring
Components	Discrete	Discrete and Integrated Circuit
Internal Packaging Structure	No	Yes
Internal Vibration Isolation	No	Yes
Compression-Loaded	Yes	Yes
Component Packaging	Modular	Modular and Planar

Figure 6. PCM Mechanical and Packaging Characteristics - Nimbus A Versus Nimbus B

As shown in figure 6, significant changes have been made in the design and construction of the two systems. The Nimbus B unit affords significant improvements in the size, weight, environmental protection, and connector areas over the Nimbus A unit, while utilizing the proven techniques of the previous design.

1.2.2 TELEMETRY ELECTRONICS UNIT.

1.2.2.1 ELECTRICAL CHARACTERISTICS. Nimbus A and C telemetry electronic units (TME's) are more complex electrically and dissipate a little more power than the new Nimbus B TME. Nimbus A and B TME's operate directly from the Nimbus regulated bus; however, Nimbus B TME operation is more reliable with power line voltage variations because the method of recording is digital saturation split-phase, while the Nimbus A method of recording is non-saturated gated-sine wave. The phasing problem that was apparent in the Nimbus A TME does not exist in the Nimbus B TME. Figure 7 is a comparison chart of the Nimbus A and B TME's.

Item	Nimbus A	Nimbus B
Recorder Channels	2	2
Relays	Potter-Brumfield	Potter-Brumfield
Recording Type	Bias	Saturated
Input Power Lines	5	5
Redundant Electronics	No	Yes
2-Orbit Capability	No	Yes
Complex Circuits	Yes	No
Potentiometer Adjustments	Internal	External
Coaxial Connector	No	Yes
Standby Clock	Yes	No
Monitor Circuits	Yes	Yes (5)

Figure 7. TME Comparison Chart - Nimbus A Versus Nimbus B

1.2.2.2 MECHANICAL CHARACTERISTICS. As with the PCM, both Nimbus A and Nimbus B TME units utilize a compression-loaded mechanical system approach. A weight reduction in the Nimbus B TME was possible through elimination of the auxiliary clock and associated circuitry used in the Nimbus A TME unit. To reduce the environmental stresses transmitted through the unit, along with reducing housing fabrication costs, the new form factor (4 x 6 x 6-1/2 inches) was chosen over the old (2 x 6 x 13 inches). The volume required was due to packaging considerations caused by the necessity of using full crystal can relays. Initial design structure indicated that the required volume could be reduced by one-half if 1/2 crystal can relays were used. Extensive vibration testing of these relays indicated that questionable performance resulted from the 1/2 crystal can relays when they were exposed to the anticipated vibration limits of the TME. Since the Potter-Brumfield full crystal can relays successfully passed these tests, it was decided to use the larger relays, thereby requiring a larger housing.

Figure 8 provides a comparison of the mechanical and packaging characteristics of the Nimbus A and Nimbus B TME units.

Characteristic	Nimbus A	Nimbus B
Size	2" x 6" x 13"	4" x 6" x 6.5"
Weight	5.2 lbs.	4.25 lbs.
Housing		
Design	Open-ended Box	Closed Box
Finish	Chromate Dip	Electroless Nickel
Connectors		
Manufacturer	U.S. Components	Deutsch, Cannon (Multipin) GRFF (Coaxial)
Type	Special Rectangular	Standard Types
Environmental Protection	No	Yes
Locking Device	Screw-lock	Bayonet-lock Screw-lock Screw-on
Packaging Concepts		
Printed Circuit Card Type	2-sided	2-sided and 4-layer M/L
Internal Connections	Card Connectors	Hard-wiring
Internal Vibration Isolation	No	Yes
Compression-loaded	Yes	Yes
Component Packaging	Modular	Modular and Planar

Figure 8. TME Mechanical and Packaging Characteristics -
Nimbus A Versus Nimbus B

As with the PCM unit, the Nimbus B TME unit provides significant improvements in the environmental protection and connector areas, while achieving a slight reduction in weight from the previous systems.

1.2.3 BENCH TEST EQUIPMENT.

1.2.3.1 ELECTRICAL CHARACTERISTICS. The Nimbus B bench test equipment (BTE) is a slightly modified Nimbus A BTE. To simplify the test effort, the PCM and TME test sets were incorporated in one cabinet. The same basic functions are contained in both BTE's. Figure 9 is a comparison chart that shows the major differences between Nimbus A and Nimbus B BTE's.

Item	Nimbus A	Nimbus B
Frame Sync	2-Word detector	20-Bit detector
Analog Source Z	3.3K ohms	3.3K ohms
Digital Source Z	None	3.3K ohms*
Connectors	Cannon	Cannon
Channel Inputs	Closed circuit jacks	Closed circuit jacks
Separate Subframe ID Indicators	No	Yes
PCM Command to Test Set	No	Yes
100 Percent Capability to Test all PCM Subsystem Units Separately	Yes	No
Analog Source Voltage	Kepco Power Supply	Kepco Power Supply
Check 10-Bit Analog Words	No	Yes
*Digital channel source impedance was demonstrated as a separate test. Existing analog gate jacks were used for the digital channels and the resistors were not changed, which simplified the modification.		

Figure 9. BTE Comparison Chart - Nimbus A Versus Nimbus B

1.2.3.2 MECHANICAL CHARACTERISTICS. The existing Nimbus A BTE was modified with minimum change, to perform the minimum amount of testing required to prove the Nimbus B Study PCM Subsystem. The objective of the test equipment was to help prove that the study system met or exceeded all of the design criteria. One week of testing time was allowed and since testing time was not critical, an inexpensive, manually-operated test set satisfied the test requirements. To simplify testing, both the Nimbus A TME Test Set and PCM Test Set were modified and reassembled into a single cabinet, rather than the original two cabinets.

The previous PCM analog channel control panel and connectors were used directly in the new BTE, including the 3.3-k source impedance resistors. The old panel had an expansion capability that had never been utilized; therefore, sufficient closed circuit jacks were available for use as 21 prime analog jacks, 63 prime digital jacks, 434 subcom analog jacks, 280 subcom digital jacks, with approximately 30 jacks for monitor points, etc.

The TME and PCM Test Set control panels were rewired to accommodate new command functions which were nearly identical to the previous functions.

The TME and PCM Test Set chassis that contained the cards of NOR logic circuits were rewired to perform the new logic functions. The new logic was performed by 45 logic cards located in three logic trays.

Connecting cables to the PCM subsystem were rewired on one end to connect to the new Deutsch connectors.

The new BTE's for Nimbus B are of an entirely new mechanical design, and the mechanical design of the study BTE was not intended for later use.

After the successful demonstration of the Nimbus study PCM subsystem, the BTE was disassembled and the cabinet used for the Nimbus B BTE.

1.2.4 GROUND STATION EQUIPMENT.

The present PCM Ground Station System 2 equipment is housed in nine cabinets. These are: four analog recorder cabinets, a Mincom recorder cabinet, a simulator and test equipment cabinet, a two-cabinet group of control electronics, and an event recorder and time display cabinet.

Two PCM A signals and one time code signal are utilized in PCM Ground Station System 2. The first PCM A signal is comprised of a 63-1/2-channel frame, a tape recorder playback at a 15-kc bit rate, and a split-phase signal. The first 2-1/2 words are for frame synchronization and the next 1/2 word is for subframe synchronization. Word synchronization is the first bit of each word and is always a zero. The second PCM A signal is the same as the first PCM A signal except that a 500-cps bit rate is used. The time code signal is a 10-kc subcarrier that is amplitude-modulated 60 percent at 100 pps (nominal) with the Minitrack time code signal and is sent simultaneously with the second PCM A signal.

The following paragraphs contain a general discussion of the electrical and mechanical changes to PCM Ground Station System 2. A detailed discussion of the modifications is presented in Section II.

1.2.4.1 ELECTRICAL CHARACTERISTICS. Changes in the electrical characteristics of the PCM Ground Station System 2 equipment are discussed in the following paragraphs.

The original bit synchronizer was replaced by a 5220A bit synchronizer because the original unit was not capable of accepting split-phase/single (SP/S) input signals. The combination of SP/S signals and the new units provides better signal-to-noise ratio. The 5220A unit is completely programmable and is controlled by squelch circuits.

Squelch circuits in the system control unit were changed to accommodate the SP/S signals. In addition, programming signals were added to remotely control the bit synchronizer when switching from real-time to playback signals.

The group synchronizer was modified to permit operation with a 62-1/2-word format instead of the 64-word format. Parallel data outputs were added to the output shift register and routed to cabinet 6.

The decommutator was changed by adding parallel outputs to various word and frame pulses needed in the time code display unit. In this way, no extra loads were added to patch panel outputs. The area labeled RECYCLING on the old patch panel is now used for digital decommutator inputs. Patching arrangements are the same as with the analog decommutator; the patch panel holes are wired directly to the output connector and routed to the digital decommutator.

Since the new Nimbus B format has digital time code inserted in given words in the first minor frame, a time code display unit was added to the system. This unit decommutates and displays the digital time code on NIXIE tubes. The time code display unit also generates and distributes a serial time code to certain event recorder channels and to the analog recorder event markers. A relay, mounted in the analog recorder and controlled by the time code display unit, activates the analog recorder event markers.

The new Nimbus B format also has digital data recorded in certain words. A digital decommutator and a 150-channel event recorder were added to handle this data. The patch panel permits placing any decimal word in the format on any desired group of event recorder channels.

The most extensive modification was made to the simulator in cabinet 5. The simulator was changed to generate 62-1/2-word formats instead of 64-word formats, and the video output was changed from non-return-to-zero (NRZ) to split-phase/single (SP/S). A selectable sync word capability was added to replace the previous fixed sync word. In addition, a single word select feature was incorporated as a troubleshooting aid. This permits the operator to insert any bit combination into any single word slot in the format. A time code generator was added to simulate the time code words in the new Nimbus B format. Since there was not enough space in the simulator to house the additional circuitry, a card file was mounted in cabinet 5 to house the time code generator. This unit inserts a digital time code into the format at the proper time and updates the time code at a simulated time rate.

1.2.4.2 MECHANICAL CHARACTERISTICS. Changes in the mechanical layout of the PCM Ground Station System 2 were not extensive. The major change was the addition of a new single-unit cabinet to house the event recorder, digital decommutator, and time code display units. The cabinet is equipped with a blower and convenience outlets. Ac and dc power were brought in from cabinet 3/4 to a connector panel mounted in the top rear of the new cabinet.

The addition of the new cabinet required adding a connector panel in the top rear of cabinet 3 and three external cables to interconnect the two panels. Ac power, dc power, and signal leads were routed through these cables.

A single card file of 25 cards was mounted directly below the simulator and behind the simulator control panel in cabinet 5 to house the time code generator circuitry. Inputs, outputs, and power leads interface directly with the simulator.

A relay bracket unit was added to each of the four analog recorders and was mounted in the lower portion above the connector panel. An additional 4-wire shielded cable was required to handle signals to the relay bracket. The new cable was connected to spare pins in the signal cable connector in cabinet 3/4 and was terminated in another 5-pin connector to mate with the relay bracket unit at the analog recorders. All new cables were routed through existing overhead cable runs. Since the new cable was spot-tied to the signal cable, they can be considered a single cable with a multiple connector on one end.

Another output connector was added to the decommutator drawer to accommodate patch panel leads. These leads were brought out to a spare terminal board in cabinet 4 and were routed to the proper points.

The original bit synchronizer was removed and the 5220A bit synchronizer was mounted in its place. Since the 5220A is not as high as the original unit, a fill-in panel was mounted on the cabinet above the 5220A.

1.3 RELIABILITY.

During the reliability improvement study, it was determined that redundant multiplexer input gates were not feasible. The additional circuits required in the design of block-redundant input gates were prohibitive considering cost, package size and the interface problems. As a trade-off between reliability, cost and package size, the input gates were designed in a non-redundant configuration, using the following design criterion for increased reliability: "No single failure will cause the loss of more than eight analog channels and seven digital bit gates."

The above criterion was followed throughout the system design with deviations only in time code and real-time TME circuitry, power input to the summing amplifiers, and 500-cps from the Nimbus clock. These deviations are discussed in paragraph 2.6.6.

1.4 TEST AND DEMONSTRATION RESULTS.

The results of the mechanical model vibration test and the electrical model demonstration tests are discussed in the following paragraphs.

1.4.1 MECHANICAL MODEL VIBRATION TEST.

To evaluate the mechanical and packaging design of the PCM and TME units, mechanical models of each unit were fabricated and subjected to the qualification level vibration environment. These models were identical to the actual systems, except that dummy components were used in place of the electronic components. Accelerometers were positioned in locations where the highest stress levels were anticipated. Vibration levels were monitored, both in the major input axis and in both minor axes (crosstalk). In addition, fabrication and assembly of these models provided a means of determining what problems would arise in these areas, enabling them to be analyzed and corrected prior to assembly of the actual system.

1.4.2 ELECTRICAL MODEL DEMONSTRATION TEST.

The approved demonstration test procedure was performed, and the PCM and TME units operated properly. When the PCM Subsystem was accepted by the NASA Technical Officer, only one problem was encountered. This problem involved noise that appeared on the 10-bit coder calibration voltage when system cards were compressed into the final configuration. The noise produced an effective increase in calibration voltage and increased the normal -6.401-volt full-scale voltage to -6.416 volts; thus, full-scale voltage was increased by about 15 millivolts. This problem must be solved for the Nimbus B PCM Subsystems.

A detailed discussion of the tests conducted is presented in Section II. Supporting data sheets for these tests have been supplied separately.

1.4.3 CONCLUSIONS AND RECOMMENDATIONS.

1.4.3.1 ELECTRICAL. A new MOSFET gate should be added to coder input pulse amplitude modulation (PAM) lines to provide isolation from the large amount of multiplexer driver switching noise during calibration times. The additional ON resistance, approximately 2.2K ohms, would be insignificant because the majority of leakage current is caused by the overvoltage diodes at the output of the input channel gates. Thus, very little leakage current would flow through the added resistance, and the resultant offset would be measured in terms of microvolts. All other design problems were solved before the demonstration test and were incorporated in the Nimbus B PCM Subsystem design.

It is recommended that Nimbus B parts include General Instrument as well as Fairchild MOSFET gates so that the reliability of these new devices can be evaluated.

1.4.3.2 MECHANICAL. No major problems were encountered in the vibration testing of the PCM and TME units. However, a major problem during system assembly was caused by the stiffness of the Raychem wire. System assembly was extremely difficult because of the stiffness and large number of wires behind the front panels of the units. Because of this, a change from the Raychem to a multi-laminated Teflon wire (such as used on the LEM) was requested and approved for the Nimbus B Qualification and Flight system.

SECTION II

DETAILED DISCUSSION

2.0 INTRODUCTION.

This section presents detailed discussions of the Nimbus B PCM Subsystem design approach, electrical and mechanical interface, electrical and mechanical design, design testing, and reliability. Simplified drawings are included in this section; however, detailed drawings are referenced in the text and are contained in Appendix I.

2.1 SUBSYSTEM DESIGN APPROACH.

A reliability improvement study was conducted during the study program to determine the best design approach. The study results were published as the "Nimbus B Telemetry Reliability Improvement Study," dated July 1965, by Radiation Incorporated (Contract NAS5-3787). During the design review at NASA, Redundancy Approach 10 of 14 was selected as the most feasible due to size, weight, power, schedule, cost and complexity considerations.

The final design approach was identical to Redundancy Approach 10, with the following exceptions:

- a. Prime analog channel capability was decreased from 26 to 21.
- b. Subcommutated analog channel capability was decreased from 450 to 434.
- c. Prime digital channel capability was increased from 28 to 63.
- d. Subcommutated digital channel capability was increased from 168 to 280.
- e. Time code input was changed from parallel to serial, which necessitated the addition of Nimbus C 10-cps and 100-cps clock inputs.
- f. Since Radiation-built digital multiplexer diode gating circuits have a very low input impedance (27K ohms), the design was changed to use general purpose amplifiers (GPA's) and MOSFET input digital gates to increase the minimum input impedance to 500K ohms and save power at the input digital gate interface.

NOTE

Because of the G levels encountered during testing, TME relays were changed from the original Babcock and Filtor back to the Nimbus A type Potter-Brumfield.

2.2 SYSTEM INTERFACE

The Nimbus B PCM Telemetry Subsystem block diagram (figure 10) and the wiring diagram (figure 11) show the interfacing between the following functional areas: (a) telemetry monitor point, (b) digital source transducers, (c) analog source transducers, (d) other spacecraft equipment, (e) Nimbus C clock, (f) Nimbus B power source, (g) PCM, (h) TME, (i) tape recorders, and (j) redundant transmitters. These diagrams are self-explanatory and show how the functional blocks are connected to form a complete operating subsystem.

Detailed electrical and mechanical interface discussions and supporting data are contained in the "Nimbus B PCM Telemetry Subsystem Interface Manual," dated July 1966, by Radiation Incorporated (Contract NAS5-10139). This addendum covers only those portions of interface design and fabrication pertaining to the extension of the design study contract (NAS5-3787).

2.2.1 PCM ELECTRICAL INTERFACE.

The PCM electrical interface is accomplished through 15 connectors that are allocated as follows:

- a. J1 is allocated for all inputs from and outputs to the TME.
- b. J2 through J12, J14, and J15 are allocated for all analog transducer and digital transducer inputs.
- c. J13 is allocated for monitor inputs and is electrically identical to J1.

The PCM accepts analog and digital inputs from transducers, monitor points, Nimbus C clock, and the TME. These inputs are routed through the PCM, as shown in figure 12, and the resultant split-phase output data is sent to the TME for subsequent transmission.

2.2.2 PCM MECHANICAL INTERFACE.

The PCM unit is a standard 8" x 6" x 6.5" Nimbus module (figure 1-1), with dimensional tolerances and outline conforming to NASA drawing NIM-81D. There are 15 connectors on the front panel (mounting face) of the unit. These connectors are of a cylindrical multipin type manufactured by the Deutsch Company. Connector identification data is contained in tables 1 and 2.

Table 1. PCM Connector Identification Data

Connector Designation	Number of Contacts per Connector	Radiation Part No.	Manufacturer Part No.
J1, 2, 4, 5, 7, 8, 10, 11, 13, 14	61	110208-111	340-16-61P
J3, 6, 9, 12, 15	85	110208-115	340-18-85S

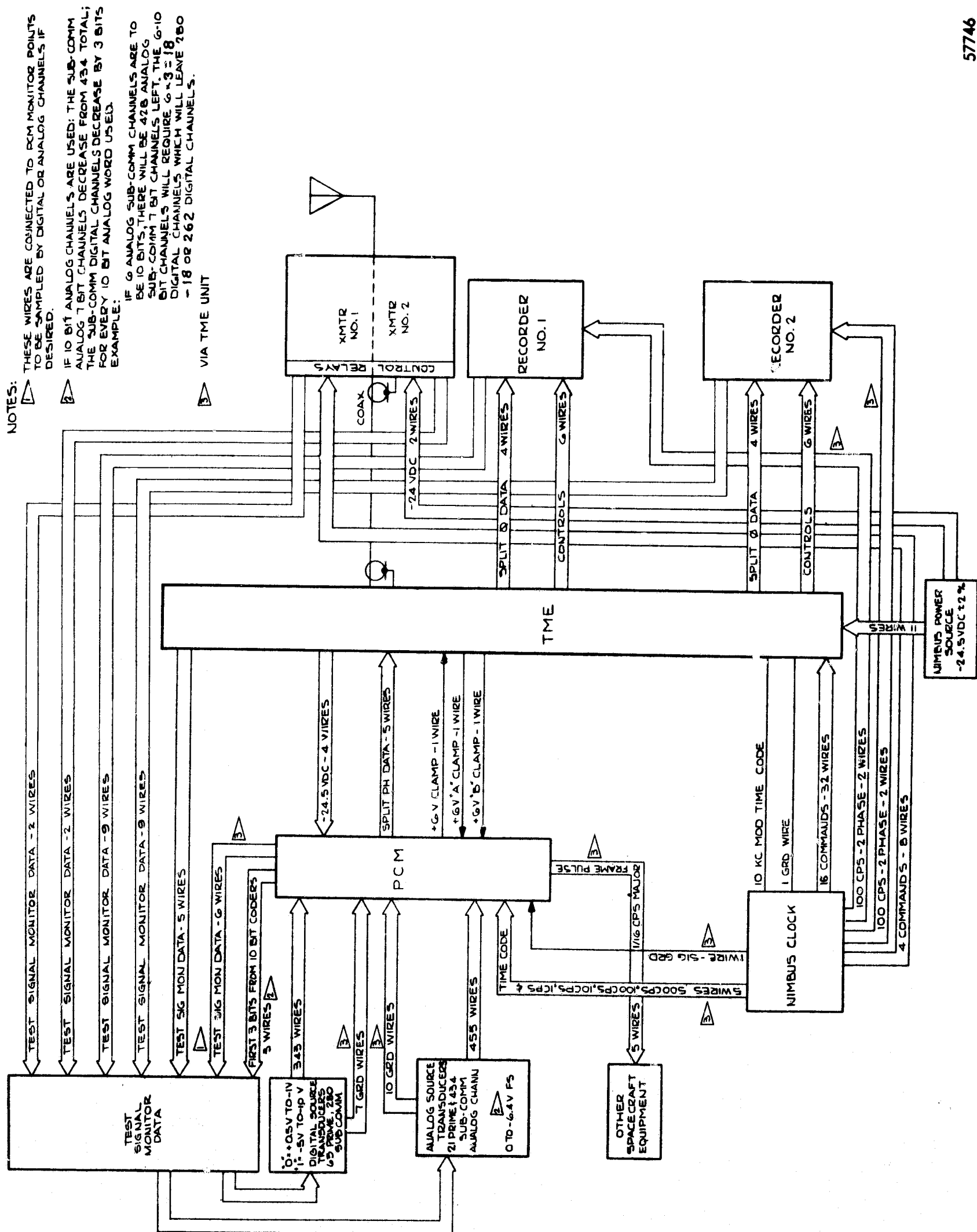
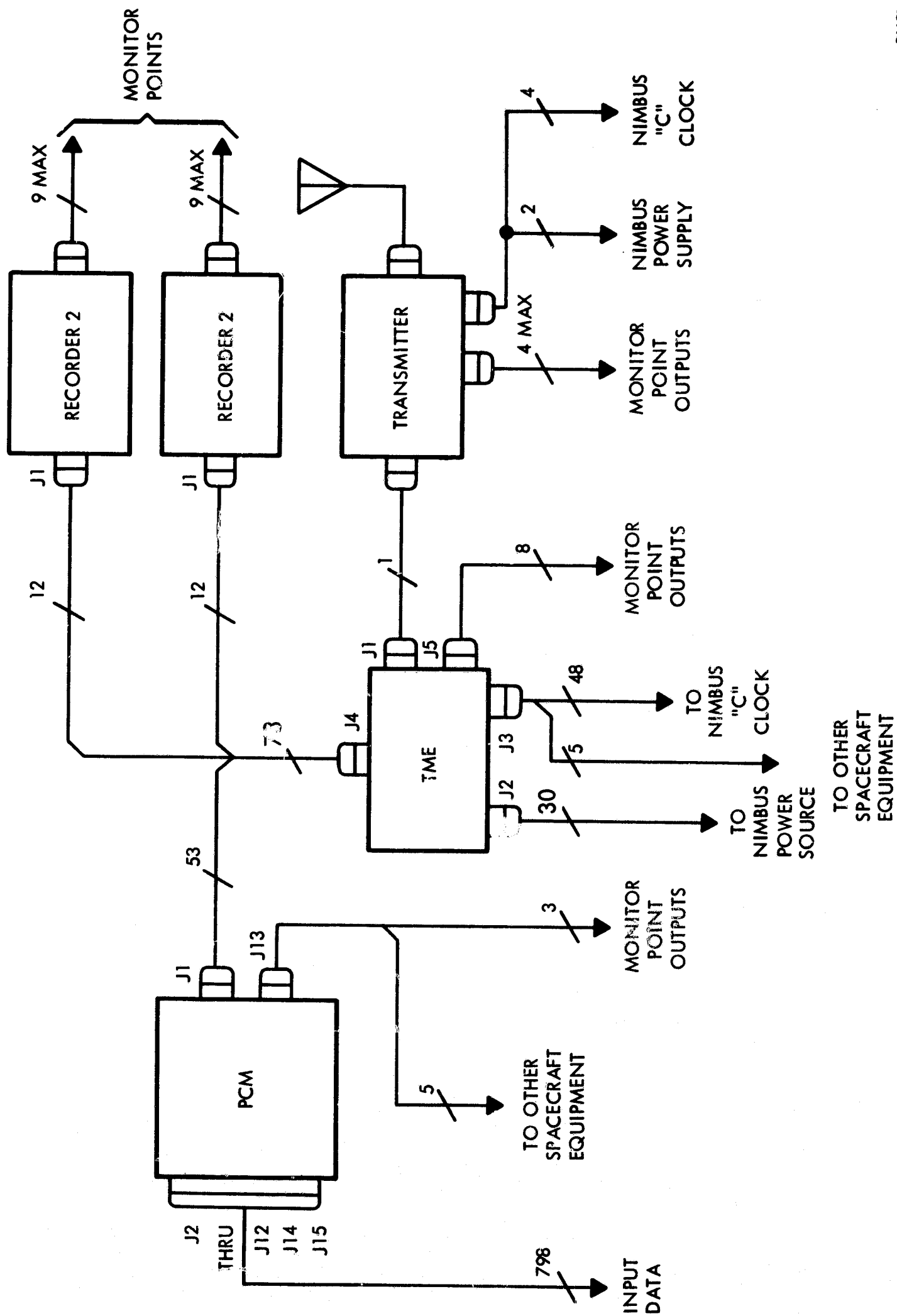
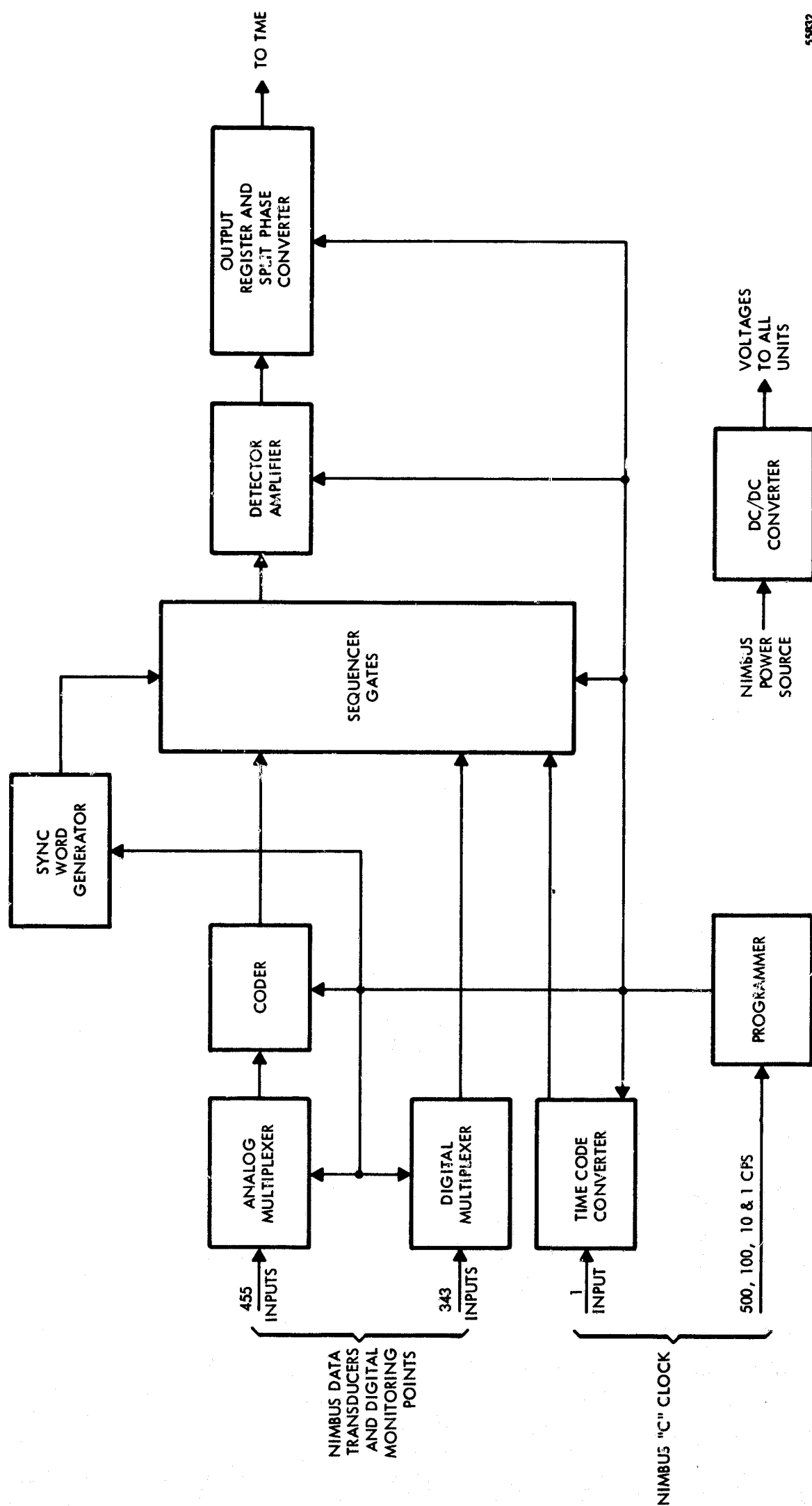


Figure 10. Nimbus B PCM Telemetry Subsystem, Simplified Block Diagram



56651

Figure 11. Nimbus B PCM Telemetry Subsystem, Interface Wiring Diagram



55832

Figure 12. PCM Signal Flow, Simplified Block Diagram

Table 2. PCM Mating Connector Identification Data

Number of Contacts per Connector	Radiation Part No.	Manufacturer Part No.
61	110207-129	346-16-615
85	110207-133	346-18-855

These connectors are of the bayonet-locking type, and meet all environmental performance criteria, along with providing the capability for 1,035 contacts through the combination of 61-pin (16 shell size) and 85-pin (18 shell size) connectors on the available surface area. In addition, they are available in crimp contacts, which provide for economical fabrication. Connector locations and usage are shown in figure 13.

2.2.3 TME ELECTRICAL INTERFACE.

The TME electrical interface is accomplished through five connectors, as follows:

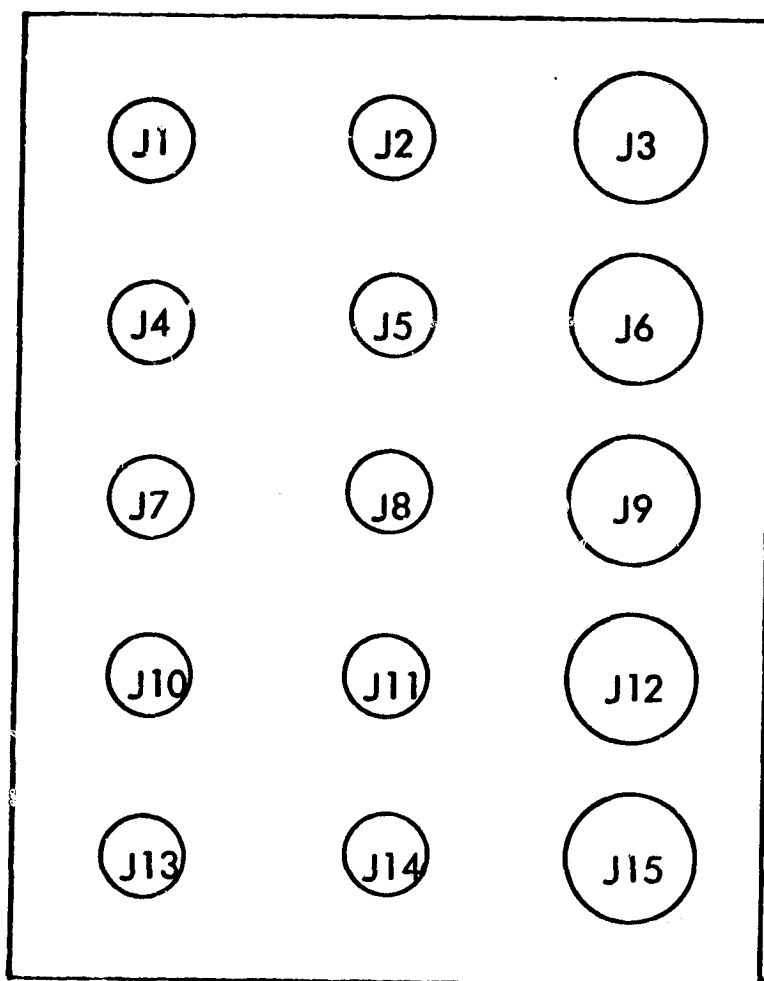
- a. J1 is the coaxial output connector to the transmitter.
- b. J2 is the interface connector to the Nimbus regulated bus for the PCM and the TME. All transducer signal grounds to the PCM are in this connector.
- c. J3 is the interface connector to the Nimbus C clock. All PCM clock signals, as well as all commands and time code to the TME, are in this connector.
- d. J4 is the interface connector to the PCM and both tape recorders.
- e. J5 is a monitor point connector.

The TME performs relay switching functions, as illustrated in the simplified block diagram (figure 14). All commands and the 10-kc time code inputs are received from the Nimbus C clock; the -24.5-volt input is received from the Nimbus regulated bus; and all split-phase data input is received in real-time from the PCM or, in playback, from the tape recorders. All output data is sent to the transmitter for transmission to the ground station.

2.2.4 TME MECHANICAL INTERFACE.

The TME unit is a standard 4" x 6" x 6.5" Nimbus module (figure 1-2) with dimensional tolerances and outline conforming to NASA drawing NIM-81D. There are five connectors on the front panel (mounting face) of the unit. Connector identification data is contained in tables 3 and 4.

All connectors have locking provisions (bayonet-lock shells, screw-type shells, or separate screw-locks). Connector locations and usage are shown in figure 15.



NOTES:

1. J3, J6, J9, J12, and J15 are 85-pin connectors, all others are 61-pin connectors.
2. Discrete component module connectors are J1 and J13.
3. Subcom matrix board connectors are:

J2, J3, and J4	Subcom Pair 1
J5, J6, and J7	Subcom Pair 2
J8, J11, and J12	Subcom Pair 3
J10, J14, and J15	Subcom Pair 4
4. Prime channel board connector is J9.

Figure 13. PCM Connector Locations and Usage

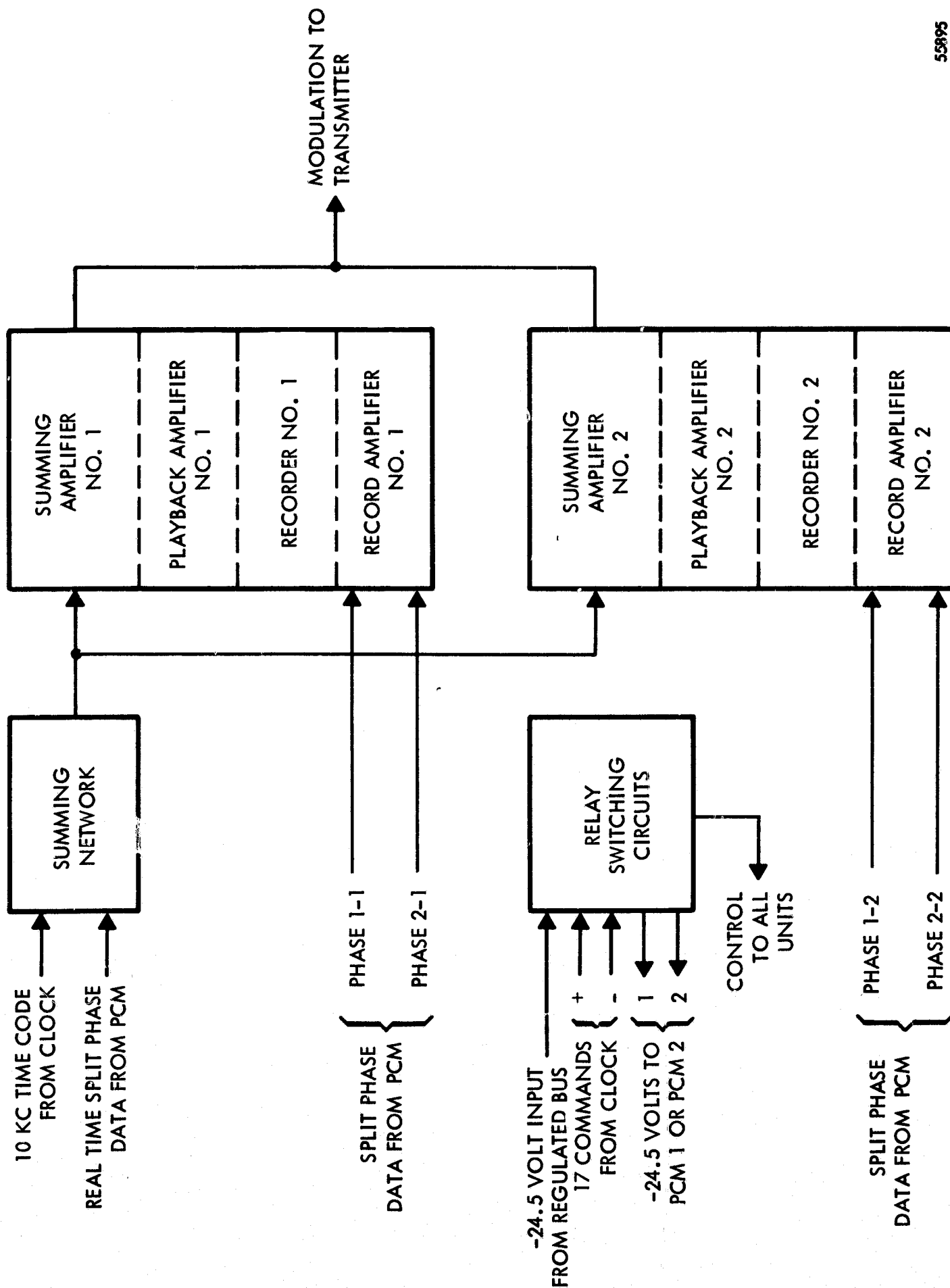


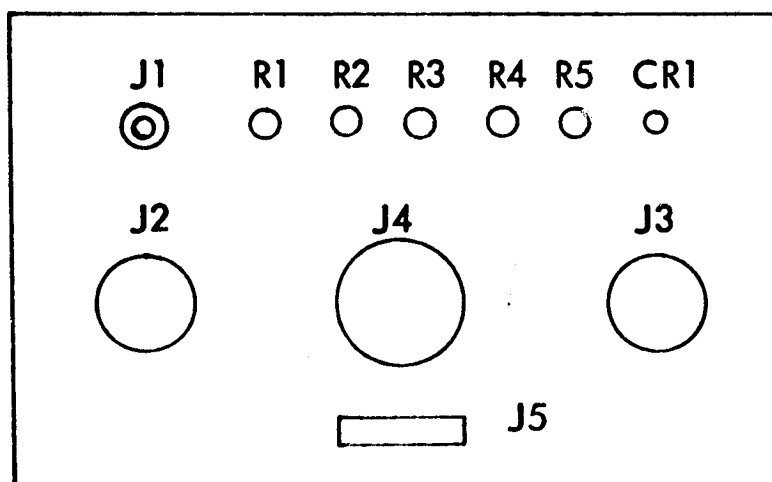
Figure 14. TME Unit, Simplified Block Diagram

Table 3. TME Connector Identification Data

Connector Designation	Connector Type	Number of Contacts per Connector	Radiation Part No.	Manufacturer Part No.
J1	RF	1	110206-001	GRFF 2265
J2, 4	Cylindrical Multi-Pin	61	110208-111	Deutsch 340-16-61P
J3	Cylindrical Multi-Pin	85	110208-115	Deutsch 340-18-85P
J5	"D" Shape Multi-Pin	9	106922-010	Cannon DEMA-9S-NMB-1

Table 4. TME Mating Connector Identification Data

Number of Contacts per Connector	Radiation Part No.	Manufacturer Part No.
1	104992-007	GRFF 2235A
61	110207-129	Deutsch 346-16-61S
85	110207-133	Deutsch 346-18-85S
9	106922-009	Cannon DEMA-9P-NMB-1



- Notes:**
1. J1 is a coaxial connector, and is the signal output to the transmitters.
 2. J2 and J3 are 61-pin connectors, and contain all signal and power lines to the TME.
 3. J4 is an 85-pin connector, and contains all wires connecting the TME and PCM.
 4. J5 is a 9-pin connector, and contains selected monitor points.

Figure 15. TME Connector Locations and Usage

2.2.5 PCM FORMAT CHARACTERISTICS.

The PCM output format is divided into 16 subframes of 62.5 words (time slots) each, as shown in table 5. Time slots alternate between two prime and two subcommutated words. Prime words repeat once every subframe (once every second); subcommutated words repeat once every major frame (once every 16 seconds). The following paragraphs present the major PCM output format characteristics.

Table 5. PCM Output Format

Word	Channel	Word	Channel
SUBFRAME 1			
1	Sync No. 1	33	1A10
2	Sync No. 2 and ID	34	1A11
3	1/16A1	35	1/16A10
4	1/16 Units Seconds	36	1/16 Tens Hours
5	1A1	37	1A12
6	1D1(69, 64, 59, 54, 49, 44, 39)	38	1A13
7	1/16A2	39	1/16A11
8	1/16A3	40	1/16A12
9	1D2(31, 26, 21, 16, 11, 6, 1)	41	1D6(32, 27, 22, 17, 12, 7, 2)
10	1A2	42	1A14
11	1/16D1(31, 26, 21, 16, 11, 6, 1)	43	1/16A13
12	1/16 Tens Seconds	44	1/16A14
13	1D3(67, 62, 57, 52, 47, 42, 37)	45	1D7(66, 61, 56, 51, 46, 41, 36)
14	1A3	46	1A15
15	1/16D2(171, 166, 161, 156, 151, 146, 141)	47	1/16A15
16	1/16A4	48	1/16A16
17	1A4	49	1A16
18	1A5	50	1A17
19	1/16 Units Minutes	51	1/16A17
20	1/16A5	52	1/16A18
21	1A6	53	1A18
22	1A7	54	1A19
23	1/16 Tens Minutes	55	1/16A19
24	1/16A6	56	1/16A20
25	1A8	57	1A20
26	1D4(34, 29, 24, 19, 14, 9, 4)	58	1D8(35, 30, 25, 20, 15, 10, 5)
27	1/16A7	59	1/16A21
28	1/16A8	60	1/16A22
29	1A9	61	1A21
30	1D5(70, 65, 60, 55, 50, 45, 40)	62	1D9(68, 63, 58, 53, 48, 43, 38)
31	1/16 Units Hours	62.5	Sync No. 63
32	1/16A9		

Table 5. PCM Output Format (Continued)

Word	Channel	Word	Channel
SUBFRAME 2			
1	Sync No. 1	33	1A10
2	Sync No. 2 and ID	34	1A11
3	1/16A23	35	1/16A37
4	1/16A24	36	1/16A38
5	1A1	37	1A12
6	1D1(69, 64, 59, 54, 49, 44, 39)	38	1A13
7	1/16A25	39	1/16A39
8	1/16A26	40	1/16A40
9	1D2(31, 26, 21, 16, 11, 6, 1)	41	1D6(32, 27, 22, 17, 12, 7, 2)
10	1A2	42	1A14
11	1/16A27	43	1/16A41
12	1/16A28	44	1/16A42
13	1D3(67, 62, 57, 52, 47, 42, 37)	45	1D7(66, 61, 56, 51, 46, 41, 36)
14	1A3	46	1A15
15	1/16A29	47	1/16A43
16	1/16A30	48	1/16A44
17	1A4	49	1A16
18	1A5	50	1A17
19	1/16A31	51	1/16A45
20	1/16D3(101, 96, 91, 86, 81, 76, 71)	52	1/16A46
21	1A6	53	1A18
22	1A7	54	1A19
23	1/16A32	55	1/16A47
24	1/16D4(241, 236, 231, 226, 221, 216, 211)	56	1/16A48
25	1A8	57	1A20
26	1D4(34, 29, 24, 19, 14, 9, 4)	58	1D8(35, 30, 25, 20, 15, 10, 5)
27	1/16A33	59	1/16A49
28	1/16A34	60	1/16A50
29	1A9	61	1A21
30	1D5(70, 65, 60, 55, 50, 45, 40)	62	1D9(68, 63, 58, 53, 48, 43, 38)
31	1/16A35	62.5	Sync No. 63
32	1/16A36		

Table 5. PCM Output Format (Continued)

Word	Channel	Word	Channel
SUBFRAME 3			
1	Sync No. 1	33	1A10
2	Sync No. 2 and ID	34	1A11
3	1/16A51	35	1/16A65
4	1/16A52	36	1/16A66
5	1A1	37	1A12
6	1D1(69, 64, 59, 54, 49, 44, 39)	38	1A13
7	1/16A53	39	1/16A67
8	1/16A54	40	1/16A68
9	1D2(31, 26, 21, 16, 11, 6, 1)	41	1D6(32, 27, 22, 17, 12, 7, 2)
10	1A2	42	1A14
11	1/16A55	43	1/16A69
12	1/16A56	44	1/16A70
13	1D3(67, 62, 57, 52, 47, 42, 37)	45	1D7(66, 61, 56, 51, 46, 41, 36)
14	1A3	46	1A15
15	1/16A57	47	1/16A71
16	1/16A58	48	1/16A72
17	1A4	49	1A16
18	1A5	50	1A17
19	1/16A59	51	1/16A73
20	1/16A60	52	1/16A74
21	1A6	53	1A18
22	1A7	54	1A19
23	1/16A61	55	1/16A75
24	1/16A62	56	1/16A76
25	1A8	57	1A20
26	1D4(34, 29, 24, 19, 14, 9, 4)	58	1D8(35, 30, 25, 20, 15, 10, 5)
27	1/16A63	59	1/16A77
28	1/16D5(102, 97, 92, 87, 82, 77, 72)	60	1/16A78
29	1A9	61	1A21
30	1D5(70, 65, 60, 55, 50, 45, 40)	62	1D9(68, 63, 58, 53, 48, 43, 38)
31	1/16A64	62.5	Sync No. 63
32	1/16D6(242, 237, 232, 227, 222, 217, 212)		

Table 5. PCM Output Format (Continued)

Word	Channel	Word	Channel
SUBFRAME 4			
1	Sync No. 1	33	1A10
2	Sync No. 2 and ID	34	1A11
3	1/16A79	35	1/16D7(32, 27, 22, 17, 12, 7, 2)
4	1/16A80	36	1/16D8(103, 98, 93, 88, 83, 78, 73)
5	1A1	37	1A12
6	1D1(69, 64, 59, 54, 49, 44, 39)	38	1A13
7	1/16A81	39	1/16D9(172, 167, 162, 157, 152, 147, 142)
8	1/16A82	40	1/16D10(243, 238, 233, 228, 223, 218, 213)
9	1D2(31, 26, 21, 16, 11, 6, 1)	41	1D6(32, 27, 22, 17, 12, 7, 2)
10	1A2	42	1A14
11	1/16A83	43	1/16A95
12	1/16A84	44	1/16A96
13	1D3(67, 62, 57, 52, 47, 42, 37)	45	1D7(66, 61, 56, 51, 46, 41, 36)
14	1A3	46	1A15
15	1/16A85	47	1/16A97
16	1/16A86	48	1/16A98
17	1A4	49	1A16
18	1A5	50	1A17
19	1/16A87	51	1/16A99
20	1/16A88	52	1/16A100
21	1A6	53	1A18
22	1A7	54	1A19
23	1/16A89	55	1/16A101
24	1/16A90	56	1/16A102
25	1A8	57	1A20
26	1D4(34, 29, 24, 19, 14, 9, 4)	58	1D8(35, 30, 25, 20, 15, 10, 5)
27	1/16A91	59	1/16A103
28	1/16A92	60	1/16A104
29	1A9	61	1A21
30	1D5(70, 65, 60, 55, 50, 45, 40)	62	1D9(68, 63, 58, 53, 48, 43, 38)
31	1/16A93	62.5	Sync No. 63
32	1/16A94		

Table 5. PCM Output Format (Continued)

Word	Channel	Word	Channel
SUBFRAME 5			
1	Sync No. 1	33	1A10
2	Sync No. 2 and ID	34	1A11
3	1/16A105	35	1/16A121
4	1/16A106	36	1/16A122
5	1A1	37	1A12
6	1D1(69, 64, 59, 54, 49, 44, 39)	38	1A13
7	1/16A107	39	1/16A123
8	1/16A108	40	1/16A124
9	1D2(31, 26, 21, 16, 11, 6, 1)	41	1D6(32, 27, 22, 17, 12, 7, 2)
10	1A2	42	1A14
11	1/16A109	43	1/16D11(33, 28, 23, 18, 13, 8, 3)
12	1/16A110	44	1/16A125
13	1D3(67, 62, 57, 52, 47, 42, 37)	45	1D7(66, 61, 56, 51, 46, 41, 36)
14	1A3	46	1A15
15	1/16A111	47	1/16D12(173, 168, 163, 158, 153, 148, 143)
16	1/16A112	48	1/16A126
17	1A4	49	1A16
18	1A5	50	1A17
19	1/16A113	51	1/16A127
20	1/16A114	52	1/16A128
21	1A6	53	1A18
22	1A7	54	1A19
23	1/16A115	55	1/16A129
24	1/16A116	56	1/16A130
25	1A8	57	1A20
26	1D4(34, 29, 24, 19, 14, 9, 4)	58	1D8(35, 30, 25, 20, 15, 10, 5)
27	1/16A117	59	1/16A131
28	1/16A118	60	1/16A132
29	1A9	61	1A21
30	1D5(70, 65, 60, 55, 50, 45, 40)	62	1D9(68, 63, 58, 53, 48, 43, 38)
31	1/16A119	62.5	Sync No. 63
32	1/16A120		

Table 5. PCM Output Format (Continued)

Word	Channel	Word	Channel
SUBFRAME 6			
1	Sync No. 1	33	1A10
2	Sync No. 2 and ID	34	1A11
3	1/16A133	35	1/16A149
4	1/16A134	36	1/16A150
5	1A1	37	1A12
6	ID1(69, 64, 59, 54, 49, 44, 39)	38	1A13
7	1/16A135	39	1/16A151
8	1/16A136	40	1/16A152
9	ID2(31, 26, 21, 16, 11, 6, 1)	41	ID6(32, 27, 22, 17, 12, 7, 2)
10	1A2	42	1A14
11	1/16A137	43	1/16A153
12	1/16A138	44	1/16A154
13	ID3(67, 62, 57, 52, 47, 42, 37)	45	ID7(66, 61, 56, 51, 46, 41, 36)
14	1A3	46	1A15
15	1/16A139	47	1/16A155
16	1/16A140	48	1/16A156
17	1A4	49	1A16
18	1A5	50	1A17
19	1/16A141	51	1/16D13(34, 29, 24, 19, 14, 9, 4)
20	1/16A142	52	1/16D14(104, 99, 94, 89, 84, 79, 74)
21	1A6	53	1A18
22	1A7	54	1A19
23	1/16A143	55	1/16D15(174, 169, 164, 159, 154, 149, 144)
24	1/16A144	56	1/16D16(244, 239, 234, 229, 224, 219, 214)
25	1A8	57	1A20
26	ID4(34, 29, 24, 19, 14, 9, 4)	58	ID8(35, 30, 25, 20, 15, 10, 5)
27	1/16A145	59	1/16A157
28	1/16A146	60	1/16A158
29	1A9	61	1A21
30	ID5(70, 65, 60, 55, 50, 45, 40)	62	ID9(68, 63, 58, 53, 48, 43, 38)
31	1/16A147	62.5	Sync No. 63
32	1/16A148		

Table 5. PCM Output Format (Continued)

Word	Channel	Word	Channel
SUBFRAME 7			
1	Sync No. 1	33	1A10
2	Sync No. 2 and ID	34	1A11
3	1/16A159	35	1/16A175
4	1/16A160	36	1/16A176
5	1A1	37	1A12
6	ID1(69, 64, 59, 54, 49, 44, 39)	38	1A13
7	1/16A161	39	1/16A177
8	1/16A162	40	1/16A178
9	ID2(31, 26, 21, 16, 11, 6, 1)	41	ID6(32, 27, 22, 17, 12, 7, 2)
10	1A2	42	1A14
11	1/16A163	43	1/16A179
12	1/16A164	44	1/16A180
13	ID3(67, 62, 57, 52, 47, 42, 37)	45	ID7(66, 61, 56, 51, 46, 41, 36)
14	1A3	46	1A15
15	1/16A165	47	1/16A181
16	1/16A166	48	1/16A182
17	1A4	49	1A16
18	1A5	50	1A17
19	1/16A167	51	1/16A183
20	1/16A168	52	1/16A184
21	1A6	53	1A18
22	1A7	54	1A19
23	1/16A169	55	1/16A185
24	1/16A170	56	1/16A186
25	1A8	57	1A20
26	ID4(34, 29, 24, 19, 14, 9, 4)	58	ID8(35, 30, 25, 20, 15, 10, 5)
27	1/16A171	59	1/16A187
28	1/16A172	60	1/16A188
29	1A9	61	1A21
30	ID5(70, 65, 60, 55, 50, 45, 40)	62	ID9(68, 63, 58, 53, 48, 43, 38)
31	1/16A173	62.5	Sync No. 63
32	1/16A174		

Table 5. PCM Output Format (Continued)

Word	Channel	Word	Channel
SUBFRAME 8			
1	Sync No. 1	33	1A10
2	Sync No. 2 and ID	34	1A11
3	1/16D17(35, 30, 25, 20, 15, 10, 5)	35	1/16A201
4	1/16D18(105, 100, 95, 90, 85, 80, 75)	36	1/16A202
5	1A1	37	1A12
6	1D1(69, 64, 59, 54, 49, 44, 39)	38	1A13
7	1/16D19(175, 170, 165, 160, 155, 150, 145)	39	1/16A203
8	1/16D20(245, 240, 235, 230, 225, 220, 215)	40	1/16A204
9	1D2(31, 26, 21, 16, 11, 6, 1)	41	1D6(32, 27, 22, 17, 12, 7, 2)
10	1A2	42	1A14
11	1/16A189	43	1/16A205
12	1/16A190	44	1/16A206
13	1D3(67, 62, 57, 52, 47, 42, 37)	45	1D7(66, 61, 56, 51, 46, 41, 36)
14	1A3	46	1A15
15	1/16A191	47	1/16A207
16	1/16A192	48	1/16A208
17	1A4	49	1A16
18	1A5	50	1A17
19	1/16A193	51	1/16A209
20	1/16A194	52	1/16A210
21	1A6	53	1A18
22	1A7	54	1A19
23	1/16A195	55	1/16A211
24	1/16A196	56	1/16A212
25	1A8	57	1A20
26	1D4(34, 29, 24, 19, 14, 9, 4)	58	1D8(35, 30, 25, 20, 15, 10, 5)
27	1/16A197	59	1/16A213
28	1/16A198	60	1/16A214
29	1A9	61	1A21
30	1D5(70, 65, 60, 55, 50, 45, 40)	62	1D9(68, 63, 58, 53, 48, 43, 38)
31	1/16A199	62.5	Sync No. 63
32	1/16A200		

Table 5. PCM Output Format (Continued)

Word	Channel	Word	Channel
SUBFRAME 9			
1	Sync No. 1	33	1A10
2	Sync No. 2 and ID	34	1A11
3	1/16A215	35	1/16A231
4	1/16A216	36	1/16A232
5	1A1	37	1A12
6	1D1(69, 64, 59, 54, 49, 44, 39)	38	1A13
7	1/16A217	39	1/16A233
8	1/16A218	40	1/16A234
9	1D2(31, 26, 21, 16, 11, 6, 1)	41	1D6(32, 27, 22, 17, 12, 7, 2)
10	1A2	42	1A14
11	1/16A219	43	1/16A235
12	1/16A220	44	1/16A236
13	1D3(67, 62, 57, 52, 47, 42, 37)	45	1D7(66, 61, 56, 51, 46, 41, 36)
14	1A3	46	1A15
15	1/16A221	47	1/16A237
16	1/16A222	48	1/16A238
17	1A4	49	1A16
18	1A5	50	1A17
19	1/16A223	51	1/16A239
20	1/16A224	52	1/16A240
21	1A6	53	1A18
22	1A7	54	1A19
23	1/16A225	55	1/16A241
24	1/16A226	56	1/16A242
25	1A8	57	1A20
26	1D4(34, 29, 24, 19, 14, 9, 4)	58	1D8(35, 30, 25, 20, 15, 10, 5)
27	1/16A227	59	1/16D21(66, 61, 56, 51, 46, 41, 36)
28	1/16A228	60	1/16A243
29	1A9	61	1A21
30	1D5(70, 65, 60, 55, 50, 45, 40)	62	1D9(68, 63, 58, 53, 48, 43, 38)
31	1/16A229	62.5	Sync No. 63
32	1/16A230		

Table 5. PCM Output Format (Continued)

Word	Channel	Word	Channel
SUBFRAME 10			
1	Sync No. 1	33	1A10
2	Sync No. 2 and ID	34	1A11
3	1/16A244	35	1/16A259
4	1/16D22(136, 131, 126, 121, 116, 111, 106)	36	1/16A260
5	1A1	37	1A12
6	1D1(69, 64, 59, 54, 49, 44, 39)	38	1A13
7	1/16A245	39	1/16A261
8	1/16A246	40	1/16A262
9	1D2(31, 26, 21, 16, 11, 6, 1)	41	1D6(32, 27, 22, 17, 12, 7, 2)
10	1A2	42	1A14
11	1/16A247	43	1/16A263
12	1/16A248	44	1/16A264
13	1D3(67, 62, 57, 52, 47, 42, 37)	45	1D7(66, 61, 56, 51, 46, 41, 36)
14	1A3	46	1A15
15	1/16A249	47	1/16A265
16	1/16A250	48	1/16A266
17	1A4	49	1A16
18	1A5	50	1A17
19	1/16A251	51	1/16A267
20	1/16A252	52	1/16A268
21	1A6	53	1A18
22	1A7	54	1A19
23	1/16A253	55	1/16A269
24	1/16A254	56	1/16A270
25	1A8	57	1A20
26	1D4(34, 29, 24, 19, 14, 9, 4)	58	1D8(35, 30, 25, 20, 15, 10, 5)
27	1/16A255	59	1/16A271
28	1/16A256	60	1/16A272
29	1A9	61	1A21
30	1D5(70, 65, 60, 55, 50, 45, 40)	62	1D9(68, 63, 58, 53, 48, 43, 38)
31	1/16A257	62.5	Sync No. 63
32	1/16A258		

Table 5. PCM Output Format (Continued)

Word	Channel	Word	Channel
SUBFRAME 11			
1	Sync No. 1	33	1A10
2	Sync No. 2 and ID	34	1A11
3	1/16A273	35	1/16A285
4	1/16A274	36	1/16A286
5	1A1	37	1A12
6	1D1(69, 64, 59, 54, 49, 44, 39)	38	1A13
7	1/16A275	39	1/16A287
8	1/16A276	40	1/16A288
9	1D2(31, 26, 21, 16, 11, 6, 1)	41	1D6(32, 27, 22, 17, 12, 7, 2)
10	1A2	42	1A14
11	1/16D23(67, 62, 57, 52, 47, 42, 37)	43	1/16A289
12	1/16D24(137, 132, 127, 122, 117, 112, 107)	44	1/16A290
13	1D3(67, 62, 57, 52, 47, 42, 37)	45	1D7(66, 61, 56, 51, 46, 41, 36)
14	1A3	46	1A15
15	1/16D25(206, 201, 196, 191, 186, 181, 176)	47	1/16A291
16	1/16D26(276, 271, 266, 261, 256, 251, 246)	48	1/16A292
17	1A4	49	1A16
18	1A5	50	1A17
19	1/16A277	51	1/16A293
20	1/16A278	52	1/16A294
21	1A6	53	1A18
22	1A7	54	1A19
23	1/16A279	55	1/16A295
24	1/16A280	56	1/16A296
25	1A8	57	1A20
26	1D4(34, 29, 24, 19, 14, 9, 4)	58	1D8(35, 30, 25, 20, 15, 10, 5)
27	1/16A281	59	1/16A297
28	1/16A282	60	1/16A298
29	1A9	61	1A21
30	1D5(70, 65, 60, 55, 50, 45, 40)	62	1D9(68, 63, 58, 53, 48, 43, 38)
31	1/16A283	62.5	Sync No. 63
32	1/16A284		

Table 5. PCM Output Format (Continued)

Word	Channel	Word	Channel
SUBFRAME 12			
1	Sync No. 1	33	1A10
2	Sync No. 2 and ID	34	1A11
3	1/16A299	35	1/16A313
4	1/16A300	36	1/16A314
5	1A1	37	1A12
6	1D1(69, 64, 59, 54, 49, 44, 39)	38	1A13
7	1/16A301	39	1/16A315
8	1/16A302	40	1/16A316
9	1D2(31, 26, 21, 16, 11, 6, 1)	41	1D6(32, 27, 22, 17, 12, 7, 2)
10	1A2	42	1A14
11	1/16A303	43	1/16A317
12	1/16A304	44	1/16A318
13	1D3(67, 62, 57, 52, 47, 42, 37)	45	1D7(66, 61, 56, 51, 46, 41, 36)
14	1A3	46	1A15
15	1/16A305	47	1/16A319
16	1/16A306	48	1/16A320
17	1A4	49	1A16
18	1A5	50	1A17
19	1/16D27(68, 63, 58, 53, 48, 43, 38)	51	1/16A321
20	1/16A307	52	1/16A322
21	1A6	53	1A18
22	1A7	54	1A19
23	1/16D28(207, 202, 197, 192, 187, 182, 177)	55	1/16A323
24	1/16A308	56	1/16A324
25	1A8	57	1A20
26	1D4(34, 29, 24, 19, 14, 9, 4)	58	1D8(35, 30, 25, 20, 15, 10, 5)
27	1/16A309	59	1/16A325
28	1/16A310	60	1/16A326
29	1A9	61	1A21
30	1D5(70, 65, 60, 55, 50, 45, 40)	62	1D9(68, 63, 58, 53, 48, 43, 38)
31	1/16A311	62.5	Sync No. 63
32	1/16A312		

Table 5. PCM Output Format (Continued)

Word	Channel	Word	Channel
SUBFRAME 13			
1	Sync No. 1	33	1A10
2	Sync No. 2 and ID	34	1A11
3	1/16A327	35	1/16A339
4	1/16A328	36	1/16A340
5	1A1	37	1A12
6	1D1(69, 64, 59, 54, 49, 44, 39)	38	1A13
7	1/16A329	39	1/16A341
8	1/16A330	40	1/16A342
9	1D2(31, 26, 21, 16, 11, 6, 1)	41	1D6(32, 27, 22, 17, 12, 7, 2)
10	1A2	42	1A14
11	1/16A331	43	1/16A343
12	1/16A332	44	1/16A344
13	1D3(67, 62, 57, 52, 47, 42, 37)	45	1D7(66, 61, 56, 51, 46, 41, 36)
14	1A3	46	1A15
15	1/16A333	47	1/16A345
16	1/16A334	48	1/16A346
17	1A4	49	1A16
18	1A5	50	1A17
19	1/16A335	51	1/16A347
20	1/16A336	52	1/16A348
21	1A6	53	1A18
22	1A7	54	1A19
23	1/16A337	55	1/16A349
24	1/16A338	56	1/16A350
25	1A8	57	1A20
26	1D4(34, 29, 24, 19, 14, 9, 4)	58	1D8(35, 30, 25, 20, 15, 10, 5)
27	1/16D29(69, 64, 59, 54, 49, 44, 39)	59	1/16A351
28	1/16D30(138, 133, 128, 123, 118, 113, 108)	60	1/16A352
29	1A9	61	1A21
30	1D5(70, 65, 60, 55, 50, 45, 40)	62	1D9(68, 63, 58, 53, 48, 43, 38)
31	1/16D31(208, 203, 198, 193, 188, 183, 178)	62.5	Sync No. 63
32	1/16D32(277, 272, 267, 262, 257, 252, 247)		

Table 5. PCM Output Format (Continued)

Word	Channel	Word	Channel
SUBFRAME 14			
1	Sync No. 1	33	1A10
2	Sync No. 2 and ID	34	1A11
3	1/16A353	35	1/16A369
4	1/16A354	36	1/16D33(139, 134, 129, 124, 119, 114, 109)
5	1A1	37	1A12
6	1D1(69, 64, 59, 54, 49, 44, 39)	38	1A13
7	1/16A355	39	1/16D34(209, 204, 199, 194, 189, 184, 179)
8	1/16A356	40	1/16D35(278, 273, 268, 263, 258, 253, 248)
9	1D2(31, 26, 21, 16, 11, 6, 1)	41	1D6(32, 27, 22, 17, 12, 7, 2)
10	1A2	42	1A14
11	1/16A357	43	1/16A370
12	1/16A358	44	1/16A371
13	1D3(67, 62, 57, 52, 47, 42, 37)	45	1D7(66, 61, 56, 51, 46, 41, 36)
14	1A3	46	1A15
15	1/16A359	47	1/16A372
16	1/16A360	48	1/16A373
17	1A4	49	1A16
18	1A5	50	1A17
19	1/16A361	51	1/16A374
20	1/16A362	52	1/16A375
21	1A6	53	1A18
22	1A7	54	1A19
23	1/16A363	55	1/16A376
24	1/16A364	56	1/16A377
25	1A8	57	1A20
26	1D4(34, 29, 24, 19, 14, 9, 4)	58	1D8(35, 30, 25, 20, 15, 10, 5)
27	1/16A365	59	1/16A378
28	1/16A366	60	1/16A379
29	1A9	61	1A21
30	1D5(70, 65, 60, 55, 50, 45, 40)	62	1D9(68, 63, 58, 53, 48, 43, 38)
31	1/16A367	62.5	Sync No. 63
32	1/16A368		

Table 5. PCM Output Format (Continued)

Word	Channel	Word	Channel
SUBFRAME 15			
1	Sync No. 1	33	1A10
2	Sync No. 2 and ID	34	1A11
3	1/16A380	35	1/16A396
4	1/16A381	36	1/16A397
5	1A1	37	1A12
6	1D1(69, 64, 59, 54, 49, 44, 39)	38	1A13
7	1/16A382	39	1/16A398
8	1/16A383	40	1/16A399
9	1D2(31, 26, 21, 16, 11, 6, 1)	41	1D6(32, 27, 22, 17, 12, 7, 2)
10	1A2	42	1A14
11	1/16A384	43	1/16A400
12	1/16A385	44	1/16D36(140, 135, 130, 125, 120, 115, 110)
13	1D3(67, 62, 57, 52, 47, 42, 37)	45	1D7(66, 61, 56, 51, 46, 41, 36)
14	1A3	46	1A15
15	1/16A386	47	1/16A401
16	1/16A387	48	1/16D37(279, 274, 269, 264, 259, 254, 249)
17	1A4	49	1A16
18	1A5	50	1A17
19	1/16A388	51	1/16A402
20	1/16A389	52	1/16A403
21	1A6	53	1A18
22	1A7	54	1A19
23	1/16A390	55	1/16A404
24	1/16A391	56	1/16A405
25	1A8	57	1A20
26	1D4(34, 29, 24, 19, 14, 9, 4)	58	1D8(35, 30, 25, 20, 15, 10, 5)
27	1/16A392	59	1/16A406
28	1/16A393	60	1/16A407
29	1A9	61	1A21
30	1D5(70, 65, 60, 55, 50, 45, 40)	62	1D9(68, 63, 58, 53, 48, 43, 38)
31	1/16A394	62.5	Sync No. 63
32	1/16A395		

Table 5. PCM Output Format (Continued)

Word	Channel	Word	Channel
SUBFRAME 16			
1	Sync No. 1	33	1A10
2	Sync No. 2 and ID	34	1A11
3	1/16A408	35	1/16A424
4	1/16A409	36	1/16A425
5	1A1	37	1A12
6	1D1(69, 64, 59, 54, 49, 44, 39)	38	1A13
7	1/16A410	39	1/16A426
8	1/16A411	40	1/16A427
9	1D2(31, 26, 21, 16, 11, 6, 1)	41	1D6(32, 27, 22, 17, 12, 7, 2)
10	1A2	42	1A14
11	1/16A412	43	1/16A428
12	1/16A413	44	1/16A429
13	1D3(67, 62, 57, 52, 47, 42, 37)	45	1D7(66, 61, 56, 51, 46, 41, 36)
14	1A3	46	1A15
15	1/16A414	47	1/16A430
16	1/16A415	48	1/16A431
17	1A4	49	1A16
18	1A5	50	1A17
19	1/16A416	51	1/16D38(70, 65, 60, 55, 50, 45, 40)
20	1/16A417	52	1/16A432
21	1A6	53	1A18
22	1A7	54	1A19
23	1/16A418	55	1/16D39(210, 205, 200, 195, 190, 185, 180)
24	1/16A419	56	1/16D40(280, 275, 270, 265, 260, 255, 250)
25	1A8	57	1A20
26	1D4(34, 29, 24, 19, 14, 9, 4)	58	1D8(35, 30, 25, 20, 15, 10, 5)
27	1/16A420	59	1/16A433
28	1/16A421	60	1/16A434
29	1A9	61	1A21
30	1D5(70, 65, 60, 55, 50, 45, 40)	62	1D9(68, 63, 58, 53, 48, 43, 38)
31	1/16A422	62.5	Sync No. 63
32	1/16A423		

2.2.5.1 SYNC AND ID WORDS. Time slots 1 and 63 (62.5) of every subframe contain sync words 1 and 63, respectively. Time slot 2 of every subframe contains sync word 2 and ID.

2.2.5.2 TIME CODE WORDS. Time code data appears in words 4, 12, 19, 23, 31, and 36 of subframe 1. Since time code data occurs at the subcommutated rate, each time code word is preceded by the prefix 1/16 and is designated by listing the information in that particular word, e.g., 1/16 Tens Minutes. Binary-coded-decimal (BCD) time code data occurs during the first four information bits of the particular word, or in bits 2 through 5; bit 2 is the least significant time code bit, and bit 5 is the most significant time code bit.

2.2.5.3 ANALOG CHANNEL WORDS. Prime analog channel words are designated by the prefix 1A and range from 1 to 21, e.g., 1A17. Table 6 shows the word assignment of each prime analog channel.

Table 6. Prime Analog Channel Word Allocation

Prime Analog Channel	Word Time During All 16 Subframes	Prime Analog Channel	Word Time During All 16 Subframes	Prime Analog Channel	Word Time During All 16 Subframes
1A1	5	1A8	25	1A15	46
1A2	10	1A9	29	1A16	49
1A3	14	1A10	33	1A17	50
1A4	17	1A11	34	1A18	53
1A5	18	1A12	37	1A19	54
1A6	21	1A13	38	1A20	57
1A7	22	1A14	42	1A21	61

Subcommutated analog channel words are designated by the prefix 1/16A and range from 1 to 434, e.g., 1/16A357. Table 7 shows the word assignments for each subcommutated analog channel.

The 10-bit coder capability occurs on prime or subcommutated analog channel words that are followed by prime or subcommutated digital words. The first seven bits of the 10-bit word appear in the selected analog channel word, and the last three bits of the 10-bit word appear as digital data in bits 2, 3, and 4 of the next word. However, the assigned digital channels for the first three bits of the digital word must be reconnected to the coder outputs designated 2^0 , 2^1 , and 2^2 . Thus, the extra three bits of analog word resolution reduce digital channel capability by three channels. The PCM output word format (table 5) shows the analog channels that can be used to increase resolution. Any analog channel (1A or 1/16A) that is followed by a digital channel (1D or 1/16D) can be used, depending on the desired sampling rate. For greater detail refer to appendix VI.

Table 7. Subcommutated Analog Channel Word and Subframe Allocation

Subcommutated Analog Channel	Word	Subframe	Subcommutated Analog Channel	Word	Subframe
1/16A1	3	1	1/16A42	44	2
1/16A2	7	1	1/16A43	47	2
1/16A3	8	1	1/16A44	48	2
1/16A4	16	1	1/16A45	51	2
1/16A5	20	1	1/16A46	52	2
1/16A6	24	1	1/16A47	55	2
1/16A7	27	1	1/16A48	56	2
1/16A8	28	1	1/16A49	59	2
1/16A9	32	1	1/16A50	60	2
1/16A10	35	1	1/16A51	3	3
1/16A11	39	1	1/16A52	4	3
1/16A12	40	1	1/16A53	7	3
1/16A13	43	1	1/16A54	8	3
1/16A14	44	1	1/16A55	11	3
1/16A15	47	1	1/16A56	12	3
1/16A16	48	1	1/16A57	15	3
1/16A17	51	1	1/16A58	16	3
1/16A18	52	1	1/16A59	19	3
1/16A19	55	1	1/16A60	20	3
1/16A20	56	1	1/16A61	23	3
1/16A21	59	1	1/16A62	24	3
1/16A22	60	1	1/16A63	27	3
1/16A23	3	2	1/16A64	31	3
1/16A24	4	2	1/16A65	35	3
1/16A25	7	2	1/16A66	36	3
1/16A26	8	2	1/16A67	39	3
1/16A27	11	2	1/16A68	40	3
1/16A28	12	2	1/16A69	43	3
1/16A29	15	2	1/16A70	44	3
1/16A30	16	2	1/16A71	47	3
1/16A31	19	2	1/16A72	48	3
1/16A32	23	2	1/16A73	51	3
1/16A33	27	2	1/16A74	52	3
1/16A34	28	2	1/16A75	55	3
1/16A35	31	2	1/16A76	56	3
1/16A36	32	2	1/16A77	59	3
1/16A37	35	2	1/16A78	60	3
1/16A38	36	2	1/16A79	3	4
1/16A39	39	2	1/16A80	4	4
1/16A40	40	2	1/16A81	7	4
1/16A41	43	2	1/16A82	8	4

Table 7. Subcommutated Analog Channel Word and Subframe Allocation (Continued)

Subcommutated Analog Channel	Word	Subframe	Subcommutated Analog Channel	Word	Subframe
1/16A83	11	4	1/16A124	40	5
1/16A84	12	4	1/16A125	44	5
1/16A85	15	4	1/16A126	48	5
1/16A86	16	4	1/16A127	51	5
1/16A87	19	4	1/16A128	52	5
1/16A88	20	4	1/16A129	55	5
1/16A89	23	4	1/16A130	56	5
1/16A90	24	4	1/16A131	59	5
1/16A91	27	4	1/16A132	60	5
1/16A92	28	4	1/16A133	3	6
1/16A93	31	4	1/16A134	4	6
1/16A94	32	4	1/16A135	7	6
1/16A95	43	4	1/16A136	8	6
1/16A96	44	4	1/16A137	11	6
1/16A97	47	4	1/16A138	12	6
1/16A98	48	4	1/16A139	15	6
1/16A99	51	4	1/16A140	16	6
1/16A100	52	4	1/16A141	19	6
1/16A101	55	4	1/16A142	20	6
1/16A102	56	4	1/16A143	23	6
1/16A103	59	4	1/16A144	24	6
1/16A104	60	4	1/16A145	27	6
1/16A105	3	5	1/16A146	28	6
1/16A106	4	5	1/16A147	31	6
1/16A107	7	5	1/16A148	32	6
1/16A108	8	5	1/16A149	35	6
1/16A109	11	5	1/16A150	36	6
1/16A110	12	5	1/16A151	39	6
1/16A111	15	5	1/16A152	40	6
1/16A112	16	5	1/16A153	43	6
1/16A113	19	5	1/16A154	44	6
1/16A114	20	5	1/16A155	47	6
1/16A115	23	5	1/16A156	48	6
1/16A116	24	5	1/16A157	59	6
1/16A117	27	5	1/16A158	60	6
1/16A118	28	5	1/16A159	3	7
1/16A119	31	5	1/16A160	4	7
1/16A120	32	5	1/16A161	7	7
1/16A121	35	5	1/16A162	8	7
1/16A122	36	5	1/16A163	11	7
1/16A123	39	5	1/16A164	12	7

Table 7. Subcommutated Analog Channel Word and Subframe Allocation (Continued)

Subcommutated Analog Channel	Word	Subframe	Subcommutated Analog Channel	Word	Subframe
1/16A165	15	7	1/16A206	44	8
1/16A166	16	7	1/16A207	47	8
1/16A167	19	7	1/16A208	48	8
1/16A168	20	7	1/16A209	51	8
1/16A169	23	7	1/16A210	52	8
1/16A170	24	7	1/16A211	55	8
1/16A171	27	7	1/16A212	56	8
1/16A172	28	7	1/16A213	59	8
1/16A173	31	7	1/16A214	60	8
1/16A174	32	7	1/16A215	3	9
1/16A175	35	7	1/16A216	4	9
1/16A176	36	7	1/16A217	7	9
1/16A177	39	7	1/16A218	8	9
1/16A178	40	7	1/16A219	11	9
1/16A179	43	7	1/16A220	12	9
1/16A180	44	7	1/16A221	15	9
1/16A181	47	7	1/16A222	16	9
1/16A182	48	7	1/16A223	19	9
1/16A183	51	7	1/16A224	20	9
1/16A184	52	7	1/16A225	23	9
1/16A185	55	7	1/16A226	24	9
1/16A186	56	7	1/16A227	27	9
1/16A187	59	7	1/16A228	28	9
1/16A188	60	7	1/16A229	31	9
1/16A189	11	8	1/16A230	32	9
1/16A190	12	8	1/16A231	35	9
1/16A191	15	8	1/16A232	36	9
1/16A192	16	8	1/16A233	39	9
1/16A193	19	8	1/16A234	40	9
1/16A194	20	8	1/16A235	43	9
1/16A195	23	8	1/16A236	44	9
1/16A196	24	8	1/16A237	47	9
1/16A197	27	8	1/16A238	48	9
1/16A198	28	8	1/16A239	51	9
1/16A199	31	8	1/16A240	52	9
1/16A200	32	8	1/16A241	55	9
1/16A201	35	8	1/16A242	56	9
1/16A202	36	8	1/16A243	60	9
1/16A203	39	8	1/16A244	3	10
1/16A204	40	8	1/16A245	7	10
1/16A205	43	8	1/16A246	8	10

Table 7. Subcommutated Analog Channel Word and Subframe Allocation (Continued)

Subcommutated Analog Channel	Word	Subframe	Subcommutated Analog Channel	Word	Subframe
1/16A247	11	10	1/16A288	40	11
1/16A248	12	10	1/16A289	43	11
1/16A249	15	10	1/16A290	44	11
1/16A250	16	10	1/16A291	47	11
1/16A251	19	10	1/16A292	48	11
1/16A252	20	10	1/16A293	51	11
1/16A253	23	10	1/16A294	52	11
1/16A254	24	10	1/16A295	55	11
1/16A255	27	10	1/16A296	56	11
1/16A256	28	10	1/16A297	59	11
1/16A257	31	10	1/16A298	60	11
1/16A258	32	10	1/16A299	3	12
1/16A259	35	10	1/16A300	4	12
1/16A260	36	10	1/16A301	7	12
1/16A261	39	10	1/16A302	8	12
1/16A262	40	10	1/16A303	11	12
1/16A263	43	10	1/16A304	12	12
1/16A264	44	10	1/16A305	15	12
1/16A265	47	10	1/16A306	16	12
1/16A266	48	10	1/16A307	20	12
1/16A267	51	10	1/16A308	24	12
1/16A268	52	10	1/16A309	27	12
1/16A269	55	10	1/16A310	28	12
1/16A270	56	10	1/16A311	31	12
1/16A271	59	10	1/16A312	32	12
1/16A272	60	10	1/16A313	35	12
1/16A273	3	11	1/16A314	36	12
1/16A274	4	11	1/16A315	39	12
1/16A275	7	11	1/16A316	40	12
1/16A276	8	11	1/16A317	43	12
1/16A277	19	11	1/16A318	44	12
1/16A278	20	11	1/16A319	47	12
1/16A279	23	11	1/16A320	48	12
1/16A280	24	11	1/16A321	51	12
1/16A281	27	11	1/16A322	52	12
1/16A282	28	11	1/16A323	55	12
1/16A283	31	11	1/16A324	56	12
1/16A284	32	11	1/16A325	59	12
1/16A285	35	11	1/16A326	60	12
1/16A286	36	11	1/16A327	3	13
1/16A287	39	11	1/16A328	4	13

Table 7. Subcommutated Analog Channel Word and Subframe Allocation (Continued)

Subcommutated Analog Channel	Word	Subframe	Subcommutated Analog Channel	Word	Subframe
1/16A329	7	13	1/16A370	43	14
1/16A330	8	13	1/16A371	44	14
1/16A331	11	13	1/16A372	47	14
1/16A332	12	13	1/16A373	48	14
1/16A333	15	13	1/16A374	51	14
1/16A334	16	13	1/16A375	52	14
1/16A335	19	13	1/16A376	55	14
1/16A336	20	13	1/16A377	56	14
1/16A337	23	13	1/16A378	59	14
1/16A338	24	13	1/16A379	60	14
1/16A339	35	13	1/16A380	3	15
1/16A340	36	13	1/16A381	4	15
1/16A341	39	13	1/16A382	7	15
1/16A342	40	13	1/16A383	8	15
1/16A343	43	13	1/16A384	11	15
1/16A344	44	13	1/16A385	12	15
1/16A345	47	13	1/16A386	15	15
1/16A346	48	13	1/16A387	16	15
1/16A347	51	13	1/16A388	19	15
1/16A348	52	13	1/16A389	20	15
1/16A349	55	13	1/16A390	23	15
1/16A350	56	13	1/16A391	24	15
1/16A351	59	13	1/16A392	27	15
1/16A352	60	13	1/16A393	28	15
1/16A353	3	14	1/16A394	31	15
1/16A354	4	14	1/16A395	32	15
1/16A355	7	14	1/16A396	35	15
1/16A356	8	14	1/16A397	36	15
1/16A357	11	14	1/16A398	39	15
1/16A358	12	14	1/16A399	40	15
1/16A359	15	14	1/16A400	43	15
1/16A360	16	14	1/16A401	47	15
1/16A361	19	14	1/16A402	51	15
1/16A362	20	14	1/16A403	52	15
1/16A363	23	14	1/16A404	55	15
1/16A364	24	14	1/16A405	56	15
1/16A365	27	14	1/16A406	59	15
1/16A366	28	14	1/16A407	60	15
1/16A367	31	14	1/16A408	3	16
1/16A368	32	14	1/16A409	4	16
1/16A369	35	14	1/16A410	7	16

Table 7. Subcommutated Analog Channel Word and Subframe Allocation (Continued)

Subcommutated Analog Channel	Word	Subframe	Subcommutated Analog Channel	Word	Subframe
1/16A411	8	16	1/16A423	32	16
1/16A412	11	16	1/16A424	35	16
1/16A413	12	16	1/16A425	36	16
1/16A414	15	16	1/16A426	39	16
1/16A415	16	16	1/16A427	40	16
1/16A416	19	16	1/16A428	43	16
1/16A417	20	16	1/16A429	44	16
1/16A418	23	16	1/16A430	47	16
1/16A419	24	16	1/16A431	48	16
1/16A420	27	16	1/16A432	52	16
1/16A421	28	16	1/16A433	59	16
1/16A422	31	16	1/16A434	60	16

2.2.5.3.1 PRIME ANALOG CHANNELS. The 21 prime analog channels (table 6) are sampled once each second. The total analog channel gate and associated sequencer on-time is 200 microseconds; however, the total on-time that the input transducer "sees" the coder is 170 microseconds. Thus, the normal minimum load impedance (input impedance) occurs for only 170 microseconds, which is the aperture time. Because of an overvoltage clamp circuit, the aperture time is determined by the 200-microsecond multiplexer on-time if the input analog transducer is presenting a fault condition greater than -20 volts to the PCM.

The source impedance should be less than 3.3K ohms for a guaranteed accuracy less than ± 0.7 percent error. If the transducer source impedances are greater than 3.3K ohms (up to 10K ohms), the expected accuracy is less than ± 1.0 percent error.

Supercommutation is possible by cross-strapping the prime channel inputs; however, supercommutation is not rhythmic because of the 62.5 word subframes. For example, refer to the output format shown in table 5 and note that channels 1A1 and 1A12 can be tied together for a 2-sample per second (SPS) rate and that 1A1, 1A6, 1A12, and 1A18 can be tied together for a 4-sps rate. This binary method cannot continue because no prime analog channels occur as the fifth word in the second group of eight words (words 9 through 16) or in the fifth word of the sixth group of eight words (words 41 through 48). However, prime digital words 1D3 and 1D7 can be cross-strapped for a 2-sps rate.

2.2.5.3.2 SUBCOMMUTATED ANALOG CHANNELS. The 434 subcommutated analog channels (table 7) are sampled once each 16 seconds. Subcommutated analog channel accuracy and aperture times are the same as discussed in paragraph 2.2.5.3.1.

Supercommutation of subcommutated channels is possible as described in paragraph 2.2.5.3.1; however, cross-strapping flexibility is decreased because of digital channel capability. One of the most important objectives, considered in the multiplexer design, was to make the design fail-safe so that any one failure would minimize total system loss of analog data.

Thus, digital words are placed throughout the format, where analog words are desired for supercommutating flexibility, to break up the rhythm of the analog words, thereby preventing a single failure from causing a loss of many analog channels. Separate sequencers for digital channels make this possible. In other words, this particular trade-off involves sacrificing analog and digital channel commutating flexibility for increased reliability.

2.2.5.4 DIGITAL CHANNEL WORDS. Prime digital channel words are designated by the prefix 1D and range from 1 to 9, e.g., 1D6. Each prime digital channel word contains seven digital channels that correspond to word bit positions 2 through 8; e.g., 1D6 (35, 30, 25, 20, 15, 10, 5); bit position 1 is the word sync (0) bit. Prime digital channels range from 1 to 70; however, channels 3, 8, 13, 18, 23, 28, and 33 are not used because only 63 prime digital channels are required. Table 8 shows word and associated bit assignments for each digital gate prime (DGP) channel.

Table 8. Prime Digital Channel Bit Positions

Prime Digital Channel	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8	Word
1D1	DGP69	DGP64	DGP59	DGP54	DGP49	DGP44	DGP39	6
1D2	DGP31	DGP26	DGP21	DGP16	DGP11	DGP6	DGP1	9
1D3	DGP67	DGP62	DGP57	DGP52	DGP47	DGP42	DGP37	13
1D4	DGP34	DGP29	DGP24	DGP19	DGP14	DGP9	DGP4	26
1D5	DGP70	DGP65	DGP60	DGP55	DGP50	DGP45	DGP40	30
1D6	DGP32	DGP27	DGP22	DGP17	DGP12	DGP7	DGP2	41
1D7	DGP66	DGP61	DGP56	DGP51	DGP46	DGP41	DGP36	45
1D8	DGP35	DGP30	DGP25	DGP20	DGP15	DGP10	DGP5	58
1D9	DGP68	DGP63	DGP58	DGP53	DGP48	DGP43	DGP38	62

Note: Channels 3, 8, 13, 18, 23, 28, and 33 are not used.

Subcommutated digital channel words are designated 1/16D and range from 1 to 40, e.g., 1/16D1. Each subcommutated digital channel word contains seven digital channels that correspond to bit positions 2 through 8, e.g., 1/16D25 (206, 201, 196, 191, 186, 181, 176); bit position 1 is the word sync (0) bit. Subcommutated digital channels range from 1 to 280. Table 9 shows word and associated bit assignments for each subcommutated digital gate (DG) channel.

Table 9. Subcommutated Digital Channels

Subcommutated Digital Channel	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8	Word	Subframe
1/16D1	DG31	DG26	DG21	DG16	DG11	DG6	DG1	11	1
1/16D2	DG171	DG166	DG161	DG156	DG151	DG146	DG141	15	1
1/16D3	DG101	DG96	DG91	DG86	DG81	DG76	DG71	20	2
1/16D4	DG241	DG236	DG231	DG226	DG221	DG216	DG211	24	2
1/16D5	DG102	DG97	DG92	DG87	DG82	DG77	DG72	28	3
1/16D6	DG242	DG237	DG232	DG227	DG222	DG217	DG212	32	3
1/16D7	DG32	DG27	DG22	DG17	DG12	DG7	DG2	35	4
1/16D8	DG103	DG98	DG93	DG88	DG83	DG78	DG73	36	4
1/16D9	DG172	DG167	DG162	DG157	DG152	DG147	DG142	39	4
1/16D10	DG243	DG238	DG233	DG228	DG223	DG218	DG213	40	4
1/16D11	DG33	DG28	DG23	DG18	DG13	DG8	DG3	43	5
1/16D12	DG173	DG168	DG163	DG158	DG153	DG148	DG143	47	5
1/16D13	DG34	DG29	DG24	DG19	DG14	DG9	DG4	51	6
1/16D14	DG104	DG99	DG94	DG89	DG84	DG79	DG74	52	6
1/16D15	DG174	DG169	DG164	DG159	DG154	DG149	DG144	55	6
1/16D16	DG244	DG239	DG234	DG229	DG224	DG219	DG214	56	6
1/16D17	DG35	DG30	DG25	DG20	DG15	DG10	DG5	3	8
1/16D18	DG105	DG100	DG95	DG90	DG85	DG80	DG75	4	8
1/16D19	DG175	DG170	DG165	DG160	DG155	DG150	DG145	7	8
1/16D20	DG245	DG240	DG235	DG230	DG225	DG220	DG215	8	8
1/16D21	DG66	DG61	DG56	DG51	DG46	DG41	DG36	59	9
1/16D22	DG136	DG131	DG126	DG121	DG116	DG111	DG106	4	10
1/16D23	DG67	DG62	DG57	DG52	DG47	DG42	DG37	11	11
1/16D24	DG137	DG132	DG127	DG122	DG117	DG112	DG107	12	11
1/16D25	DG206	DG201	DG196	DG191	DG186	DG181	DG176	15	11
1/16D26	DG276	DG271	DG266	DG261	DG256	DG251	DG246	16	11
1/16D27	DG68	DG63	DG58	DG53	DG48	DG43	DG38	19	12
1/16D28	DG207	DG202	DG197	DG192	DG187	DG182	DG177	23	12
1/16D29	DG69	DG64	DG59	DG54	DG49	DG44	DG39	27	13
1/16D30	DG138	DG133	DG128	DG123	DG118	DG113	DG108	28	13
1/16D31	DG208	DG203	DG198	DG193	DG188	DG183	DG178	31	13
1/16D32	DG277	DG272	DG267	DG262	DG257	DG252	DG247	32	13
1/16D33	DG139	DG134	DG129	DG124	DG119	DG114	DG109	36	14
1/16D34	DG209	DG204	DG199	DG194	DG189	DG184	DG179	39	14
1/16D35	DG278	DG273	DG268	DG263	DG258	DG253	DG248	40	14
1/16D36	DG140	DG135	DG130	DG125	DG120	DG115	DG110	44	15
1/16D37	DG279	DG274	DG269	DG264	DG259	DG254	DG249	48	15
1/16D38	DG70	DG65	DG60	DG55	DG50	DG45	DG40	51	16
1/16D39	DG210	DG205	DG200	DG195	DG190	DG185	DG180	55	16
1/16D40	DG280	DG275	DG270	DG265	DG260	DG255	DG250	56	16

2.2.5.4.1 PRIME DIGITAL CHANNELS. The nine prime digital channels (table 8) are sampled once each second. Each word contains seven digital channels, or events, that occur as bilevel functions; thus providing a total prime digital channel capability of 63 input channels. The operating range for a ZERO input is +0.5 to -1 volts, and the operating range for a ONE input is -5 to -24 volts. However, normal operating ranges are: ZERO = 0 to -1 volt and ONE = -5 to -10 volts, with the overvoltage fault condition being specified from +0.5 to -24 volts. The digital channels also contain fault clamp circuits so that voltages in excess of -20.5 volts cannot be applied to the digital channel output sequencers. Five digital channels operate in one fault clamp circuit such that there are essentially five digital channels per sequencer. If an input digital channel gate shorts (source to drain), a maximum of five digital bits is lost. All five bits are located in the same bit position in five different output words. The series clamp resistors in the digital multiplexer are 3.9K ohms instead of 1K ohm used in the analog multiplexer.

Source impedance to ground should be less than 50K ohms (ZERO input) and the source impedance to -5 volts should be less than 1 megohm (ONE input). It should be noted that a great deal of line capacity to ground (uncharged line capacity) results in reading-out a ZERO even when the desired input is a ONE. Therefore, the stray capacity should be charged to a voltage in excess of -5 volts to properly read out a ONE. If the capacity to ground is very low and uncharged, the output is a ZERO as long as the input resistance is less than 50K ohms. If it is not too important how soon (after the occurrence happens) the digital multiplexer reads out a ONE with the input charging from a ZERO with a great deal of line capacity (or a capacity type transducer), a charge resistor in excess of 1 megohm can be used since this is an external time constant problem.

Digital multiplexer gates are controlled in the same manner as the analog multiplexer gates. The digital multiplexer gate-on time is 200 microseconds, the duty cycle maximum is 1:30.8, and supercommutating is achieved in the same manner as described in paragraph 2.2.5.3.1.

NOTE

Because of printed circuit board symmetry, 35 digital channels are located on each end of the prime multiplexer board and provide a total digital capability of 70 prime channels. Since only 63 channels are desired in the output format, channels 3, 8, 13, 18, 23, 28, and 33 are not used.

2.2.5.4.2 SUBCOMMUTATED DIGITAL CHANNELS. The 40 subcommutated digital channels (table 9) are sampled once each 16 seconds. Each word contains 7 digital channels, or events, that occur as bilevel functions for a total of 280 subcommutated digital channel inputs. Operating voltage range, fault voltage range, input source impedance, input channels per sequencer, digital multiplexer on-time, maximum duty cycle power ratio, etc., are identical to those described for prime digital channels in paragraph 2.2.5.4.1.

2.3 SYSTEM ELECTRICAL DESCRIPTION.

This paragraph provides detailed electrical descriptions of the new PCM and TME units and the BTE and ground station equipment modifications.

2.3.1 PCM UNIT.

2.3.1.1 GENERAL. As shown in the detailed block diagram (figure 1-3), the PCM unit contains single-input nonredundant analog and digital channel gates and block-redundant multiplexer, dc-to-dc converter (power supply), programmer, analog-to-digital converter (coder), and output register and split-phase converter circuits. Block-redundant circuits provide alternate signal paths and are identified as 1 or 2 to designate use with PCM 1 or PCM 2. This block-redundancy capability is utilized by commanding the TME to switch to PCM 1 or PCM 2, as shown in the redundancy switching block diagram (figure 16). Thus, only one each of the following functions is used at one time .

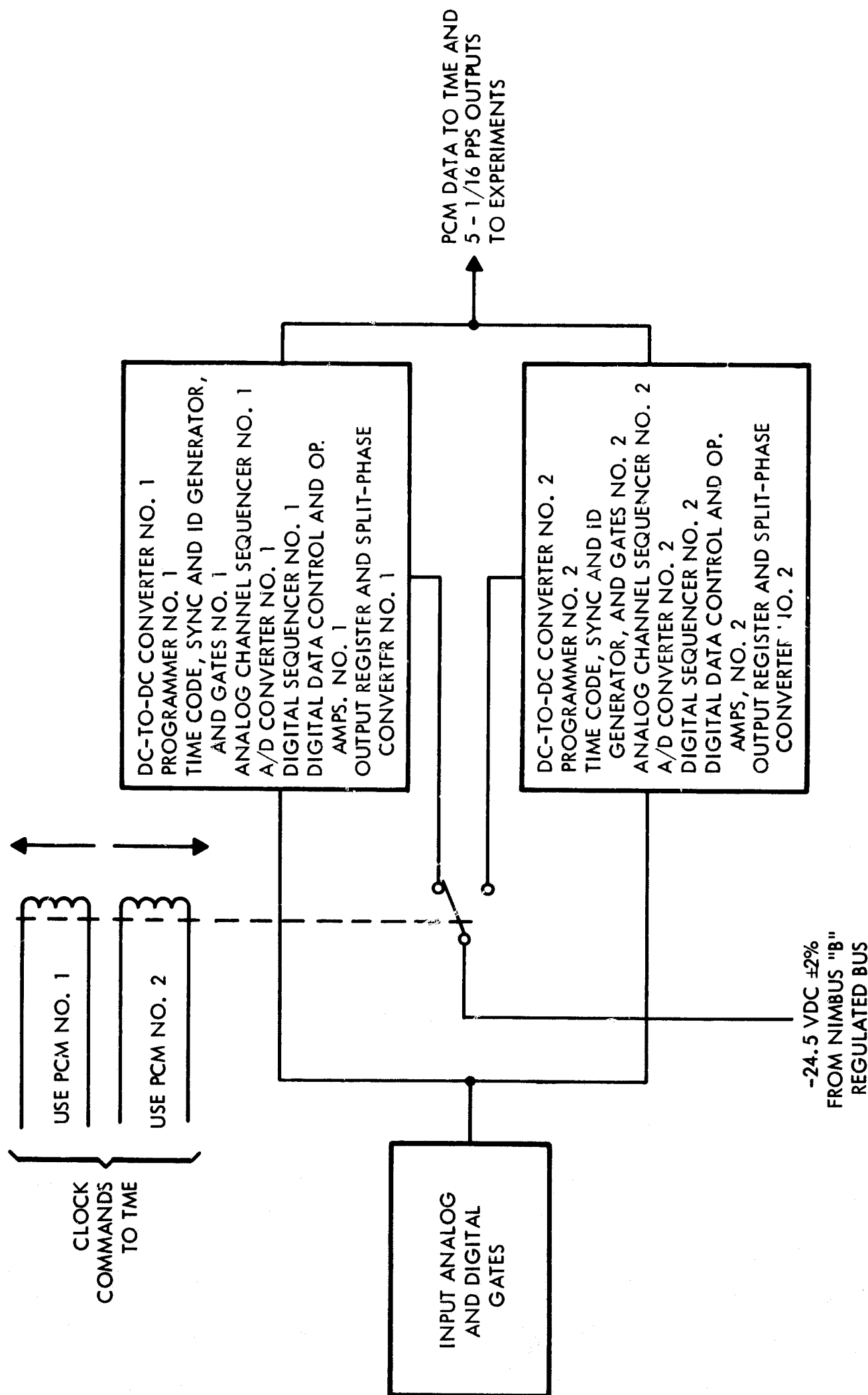
- a. Analog and digital multiplexer driver and sequencer circuits
- b. Digital multiplexer detection amplifier (GPA) and sequencer circuits
- c. Time code, sync, and subframe ID circuits
- d. Coder circuits
- e. Programmer circuits
- f. Power supply circuits
- g. Output register and split-phase converter circuits
- h. Telemetry monitor point circuits

The functional block diagram (figure 17) shows the following PCM inputs.

- a. Minus 24.5-volt ± 2 percent, signal from the TME
- b. Nimbus C clock (500-cps, 100-cps, 10-cps, 1-cps, and time code signals) through the TME
- c. Analog channels (21 prime at 1 sps and 434 subcommutated at 1/16 sps)
- d. Digital channels (63 prime at 1 sps and 280 subcommutated at 1/16 sps)

All prime analog and digital channels are sampled at a 1-cps (1-sps) rate. The nominal analog channel input voltage range is from 0 to -6.4 volts full-scale, with fault voltage protection from +0.5 to -35 volts. The specified maximum input source impedance is 3.3K ohms, which ensures an analog accuracy of 1 part in 128. The specified input impedance for an active analog channel is 1 megohm minimum with a 1-microampere maximum feedback current; whereas, the specified input impedance for an inactive analog channel is 10 megohms minimum with a 50-nanoampere maximum feedback current. Typical input impedances are larger and the feedback currents are smaller than specified. (The majority of the feedback current is caused by fault voltage protection diodes.)

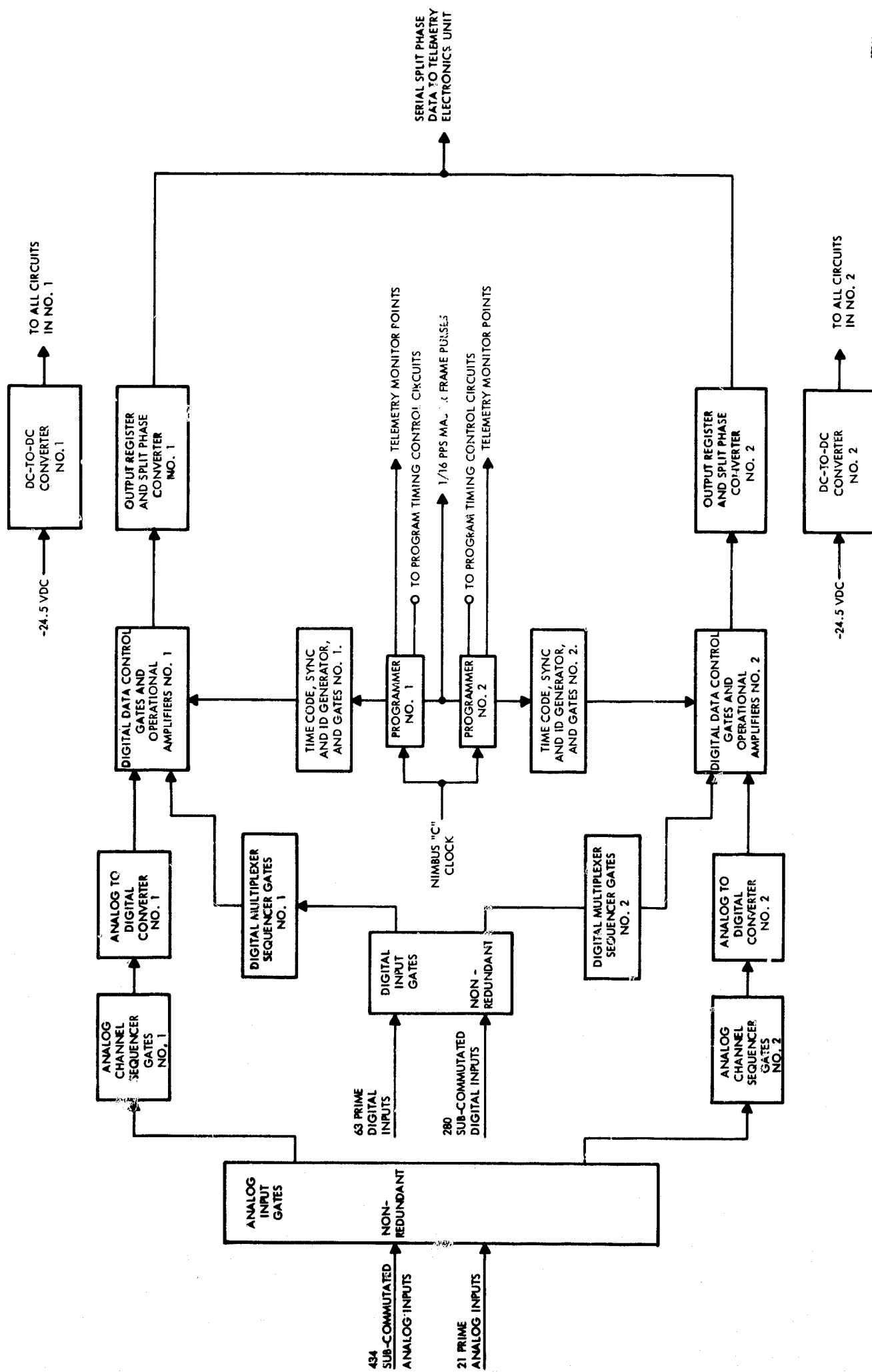
Analog channel aperture time is determined by the coder monostable multivibrator 170-microsecond pulse that allows storage of the analog sample on the storage (ramp) capacitor. The voltage level of the coded sample is the level of the ramp capacitor at the time the capacitor begins discharging.



NOTE: THE PCM REDUNDANCY SWITCHING RELAY IS LOCATED IN THE TME.

55881

Figure 16. PCM Unit, Redundancy Switching Block Diagram



5724

Figure 17. PCM Unit, Functional Block Diagram

The digital channel input voltage range is from 0 to -1 volt for a ZERO and from -5 to -10 volts for a ONE, with fault voltage protection from +0.5 to -35 volts. The specified maximum input source impedance is 50K ohms to ground and 1 megohm to -10 volts. With 0-volt input, a 50K-ohm maximum source impedance produces a ZERO at the digital multiplexer output; if the impedance increases beyond 50K ohms, the digital multiplexer output is a ONE. This means that an open-circuit digital channel produces a ONE output. However, if a large capacitance (due to cabling, capacitive transducers, etc.) is present, the circuit does not produce a ONE output unless the capacitance is fully charged. Thus, the input should be returned to a -10-volt (or -24-volt) power supply through a 1-megohm resistor. Actual voltage and resistance are determined by the RC time constant, digital data source repetition rate, and the number of samples that produce ZERO's before the circuit capacitance charges enough to produce the desired ONE output. The specified digital channel input impedance is 500K ohms minimum during sampling periods and 1 megohm minimum during nonsampling periods and when the PCM is turned off. Typical input impedances are larger than specified.

Digital channel aperture time is determined by the programmer 260-microsecond power pulse that applies power to the operational amplifiers. The actual digital sample is obtained by the programmer 15-microsecond strobe pulse that occurs in the middle of the 260-microsecond power pulse and applies either a ONE or ZERO to the output register, depending on the 260-microsecond dc voltage level appearing at the amplifier output. The amplifier reaches the proper dc voltage level within 15 to 30 microseconds following the leading edge of the 260-microsecond power pulse, and the 15-microsecond read-out pulse occurs 70 to 85 microseconds later.

All signals are routed through the PCM as shown in figure 17. Beginning at t_0 , the following events occur in sequence for subframe 1.

a. The -24.5-volt, ± 2 percent, signal is applied to PCM 1 or 2 through the TME from the Nimbus regulated bus.

b. The 500-cps and 100-cps signals from the Nimbus C clock are applied to programmer 1 or 2 to initiate sequencing action at the 500-cps bit rate, 62.5-cps word rate, 1-second subframe rate, and 16-second major frame rate.

c. Word 1 occurs and fixed (hard-wired selectable) subframe sync word 11011011 is applied through the eight word 1 digital data control gates and operational amplifiers to the 8-stage output (shift) register.

d. Word 2 occurs and the fixed (hard-wired selectable) first four bits of word 2 (1010) are applied through the first four digital data control gates and operational amplifiers into the first four shift register stages. At the same time, the four ONE outputs, or true sides, of the 4-stage 16:1 subframe counter are applied through the last four word 2 digital data control gates and the last four operational amplifiers to the last four shift register stages. Thus, the first four bits of word 2 are fixed, and the last four bits cycle from 0000 for subframe 1 to 1111 for subframe 16.

For example:

First Four Bits ↓	Last Four Bits ↓		First Four Bits ↓	Last Four Bits ↓
Word 2, Subframe 1 = 1010	0000		Word 2, Subframe 9 = 1010	1000
Word 2, Subframe 2 = 1010	0001		Word 2, Subframe 10 = 1010	1001
Word 2, Subframe 3 = 1010	0010		Word 2, Subframe 11 = 1010	1010
Word 2, Subframe 4 = 1010	0011		Word 2, Subframe 12 = 1010	1011
Word 2, Subframe 5 = 1010	0100		Word 2, Subframe 13 = 1010	1100
Word 2, Subframe 6 = 1010	0101		Word 2, Subframe 14 = 1010	1101
Word 2, Subframe 7 = 1010	0110		Word 2, Subframe 15 = 1010	1110
Word 2, Subframe 8 = 1010	0111		Word 2, Subframe 16 = 1010	1111

e. Word 3 occurs and subcommutated analog channel 1/16A1 is sampled at 1/16 sps and is applied through the analog sequencer gates (multiplexer) to the A/D converter (coder) for conversion to digital data. The seven most significant bits (MSB's) from the coder are applied through digital data control gates and operational amplifiers to the last seven shift register stages. The first stage automatically contains a ZERO from the word sync generator. (Bit 1 appears as a ZERO in all words except sync words 1 and 2.) The sampling rate is 1/16 sps.

f. Word 4 occurs and the units of seconds time code, stored in a 4-stage shift register, is applied through four digital data control gates and four operational amplifiers to shift register stages 2, 3, 4, and 5. Shift register stages 1, 6, 7, and 8 contain ZERO's from the word sync generator.

g. Word 5 occurs and prime analog channel 1A1 is processed the same as word 3, except the sampling rate is 1 sps.

h. Word 6 occurs and prime digital word 1D1 is sampled at 1 sps and is applied through digital multiplexer sequencer gates, digital data control gates and operational amplifiers to shift register stages 2 through 8. Since every digital word contains seven digital channels, each channel must be identified with respect to bit position within the word. As shown in table 8, prime digital word 1D1 contains prime digital channels 69, 64, 59, 54, 49, 44, and 39 in bit positions 2 through 8, respectively. These bits are applied to shift register stages 2 through 8, respectively; shift register stage 1 contains a ZERO from the word sync generator.

i. Words 7 through 62 are processed as described above.

j. Word 62.5 (first half of word 63) occurs and the third sync word bits (hard-wired selectable) 0111 are applied through four digital data control gates and operational amplifiers to the first four stages of the shift register.

k. The end of word 62.5 is detected and the 1-cps reset pulse is generated to reset bit and word counters to bit 1, word 1. This reset function is performed by either the 62.5 detect pulse or the external 1-cps clock pulse gated with the 500-cps clock pulse.

l. All data from words 1 through 62.5 is applied in parallel to the shift register and is shifted-out serially at a 500-cps rate into the split-phase converter.

m. The split-phase converter converts NRZ serial data into a serial split-phase Mark 0 code that is applied to three output drivers. One output driver provides real-time split-phase data to the summing network; the second output driver provides phase 1 data to two record amplifiers; and the third output driver provides phase 2 data to the opposite side of the same two record amplifiers.

n. The above process is repeated for the remaining 15 subframes, and then the next major frame begins. The 1/16-pps, 250-microsecond major frame pulse occurs in phase with the leading edge bit 1, word 1, and subframe 1 with respect to input data time for sync word 1. Since the coder requires a 2-millisecond conversion time for analog samples, all data is strobed into the shift register during the time of bit 2 (with respect to the programmer), which provides a 2-bit delay. Thus, the 1/16-pps pulse occurs 4 milliseconds, or 2-bit times, before bit 1, word 1, and subframe 1 with respect to the output split-phase data.

As shown in the functional block diagram (figure 17), the PCM produces the following outputs: (a) three least significant bit (LSB) outputs from the coder for 8-, 9-, or 10-bit analog word capability (available for use on J13 only); (b) one real-time split-phase Mark 0 code output to the TME for real-time transmission; (c) four split-phase Mark 0 code outputs (two each for phase 1 and phase 2) to the TME for recording on two recorders; (d) five 1/16-pps major frame sync pulse outputs to spacecraft experiments (via TME and J13); and (e) three telemetry monitor point outputs each to PCM 1 and PCM 2 circuits for temperature, major frame pulse, and power supply monitoring. (PCM 1 circuit monitor points are available on J5 in the TME; PCM 2 circuit monitor points are available on J13 in the PCM.)

The size and complexity of the Nimbus B analog and digital multiplexer is depicted in figure 18, which is a block diagram of the PCM from the multiplexer viewpoint. Nonredundant, single input analog and digital gates are designated multiplexer input section (PCM 1 and PCM 2). Block-redundant portions of the multiplexer are designated multiplexer output section (PCM 1) and multiplexer output section (PCM 2). Block-redundant discrete components that comprise the power supply, programmer, coder, and the output register and split-phase converter are designated discrete components (PCM 1) and discrete components (PCM 2). The multiplexer, comprised of integrated circuits, and the discrete components are discussed in the following subparagraphs.

2.3.1.2 MULTIPLEXER. The multiplexer consists of 13 multilayer printed circuit boards (integrated circuits). Table 10 lists the printed circuit board nomenclature and associated location.

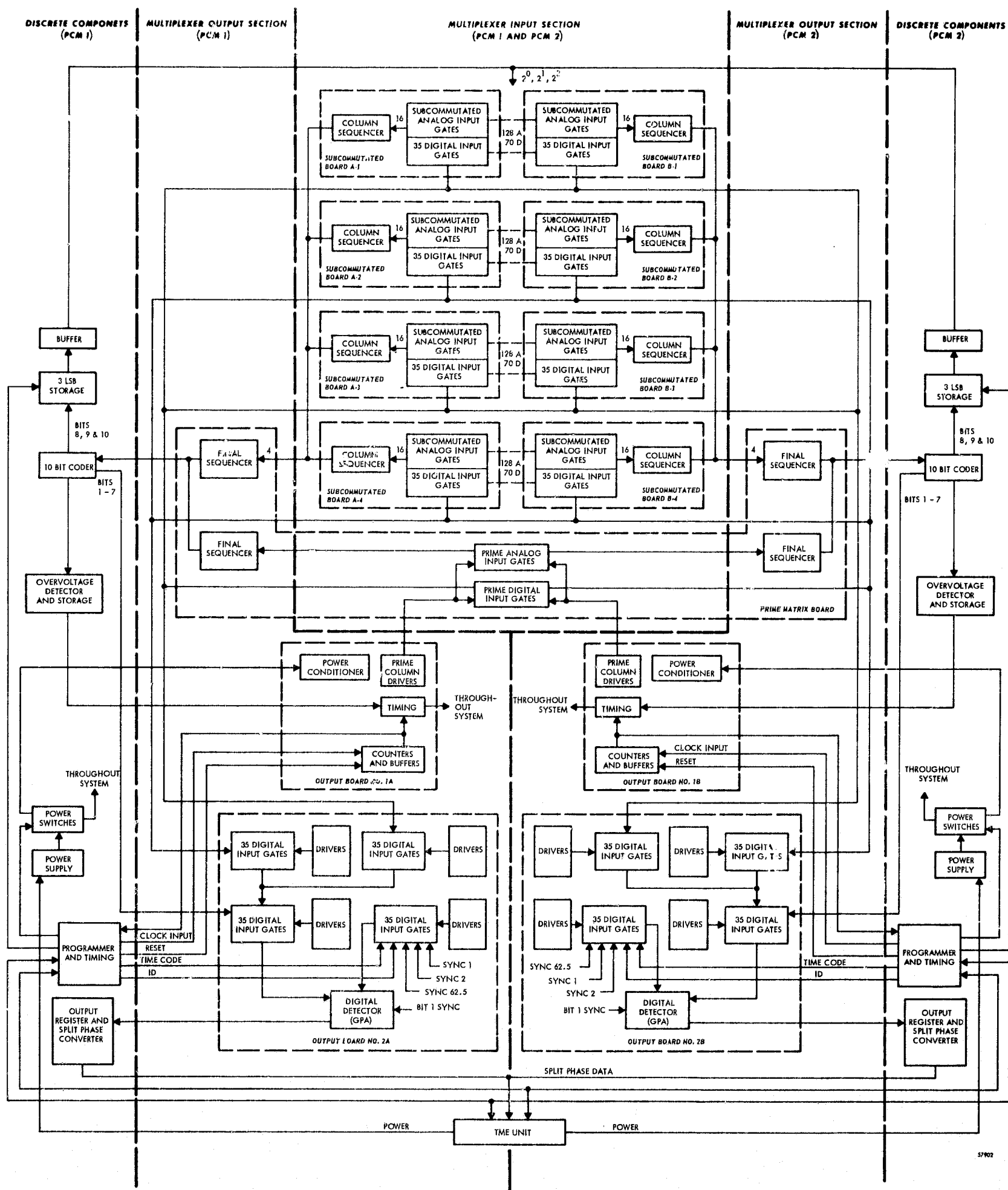


Figure 18. PCM Block Diagram (From Multiplexer Viewpoint)

Table 10. Multiplexer Printed Circuit Boards

Nomenclature	Location	Nomenclature	Location
Output Board I-A	1A3	Submatrix Board A3	1A10
Output Board II-A	1A4	Submatrix Board B3	1A11
Submatrix Board A1	1A5	Submatrix Board A4	1A12
Submatrix Board B1	1A6	Submatrix Board B4	1A13
Submatrix Board A2	1A7	Output Board I-B	1A14
Submatrix Board B2	1A8	Output Board II-B	1A15
Prime Matrix Board	1A9		

2.3.1.2.1 MULTIPLEXER PRINTED CIRCUIT BOARDS. Schematics for the 13 printed circuit boards are contained in Appendix I and are referenced in the following discussion. Throughout the following discussion and associated illustrations, A and B designations indicate use with PCM 1 and PCM 2, respectively. Only one PCM (1 or 2) is operating at any time.

Output boards I-A and I-B produce all timing for the PCM in operation. Power is applied to output board I-A or I-B, as required.

Output boards II-A and II-B contain interface circuitry between the multiplexer, coder, and output shift register. Since both boards operate in the same manner, only one board is considered. Output board II includes (a) all digital channel sequencers; (b) gates that control sync word, ID, time code, and analog or digital output gates; (c) associated drive circuitry; (d) fault-clamp zener diode circuit for analog and digital channel protection to -35 volts; (e) additional diodes and resistors to isolate the different A and B voltages; and (f) eight operational amplifiers that form the data output circuitry to the 8-stage shift register. Power is applied to output board II-A or II-B, as required.

The prime matrix board is an 8 (row) x 4 (column) matrix and accommodates 32 elements that contain all 21 prime analog and 63 prime digital channels. The matrix receives power from PCM 1 or PCM 2, as required, and is wired for maximum digital channel capability. If prime digital channels were not used, the prime matrix could accommodate 30 prime analog channels. However, one analog channel gate driver controls seven digital channels plus one analog channel if the selected time slot is a digital word. The one analog channel is wired to -15 volts (overvoltage), which, when applied to the coder and coded as full scale, commands the seven digital channels to read out.

Submatrix boards A1, B1, A2, B2, A3, B3, A4, and B4 accommodate all subcommutated analog and digital data. These boards are identical, except that the multilayers in four of the boards are reversed to simplify final packaging. The submatrix boards are grouped in pairs, i.e., A1 and B1, A2 and B2, A3 and B3, and A4 and B4. Although each pair forms a common unit, submatrices with A designations contain A (PCM 1) command circuitry and submatrices with B designations contain B (PCM 2) command circuitry. Regardless of whether A or B is operating, each submatrix pair jointly shares commands. Submatrices A1 through A4 contain columns 1 through 8, and submatrices B1 through B4 contain columns 9 through 16. Since

each column is equivalent to a minor frame and there is a total of eight submatrices, 512 elements (time slots) ($8 \times 64 = 512$) are directly controlled by the submatrices. However, all elements are not used.

The submatrix boards are wired for maximum subcommutated digital channel capability and accommodate 280 subcommutated digital channels. If subcommutated digital channels were not used, subcommutated analog channel capability would increase from 434 to 474 because 40 subcommutated analog channels are wired with overvoltage.

NOTE

If transistors or resistors were used to control overvoltage inputs to the analog channels that control the digital channels, the format could be changed. For example: the analog channels could monitor analog signals during take-off and then be connected to overvoltage inputs that would switch over to the more slowly varying digital channels after achieving orbit.

Figure 19 is a command and power signal flow block diagram that shows timing inputs from programmers 1 and 2 to output boards I-A and I-B and power inputs from power supplies 1 and 2 to output boards II-A and II-B, respectively. Output boards I-A and II-A control the PCM 1 (A) portion of the overall PCM data handling capability; output boards I-B and II-B control the PCM 2 (B) portion of the overall PCM data handling capability. If output boards I-A and II-A are being used, output boards I-B and II-B are not energized. Output boards I-A and I-B are timing boards and supply all commands to the other printed circuit boards. Output boards II-A and II-B are output circuit boards and supply all data to the output register. The prime matrix and eight submatrix boards contain two parallel output data sequencer gates and are used at all times. One output data sequencer gate is connected to PCM 1 and the other gate is connected to PCM 2.

Figure 20 is an analog channel data block diagram that illustrates the flow of analog data through the multiplexer. Submatrix boards A1 through A4 contain PCM 1 output sequencers, and submatrix boards B1 through B4 contain PCM 2 output sequencers; therefore, A channel data passes directly through PCM 1 output sequencers to the prime matrix board, and B channel data passes directly through PCM 2 output sequencers to the prime matrix board. However, A channel data must be applied to PCM 2 and B channel data must be applied to PCM 1 to provide PCM 1 and PCM 2 capability. This capability is achieved by the eight signal paths shown between A1 and B1, between A2 and B2, between A3 and B3, and between A4 and B4. The prime matrix board contains two output sequencers (PCM 1 and PCM 2) that alternate the subcommutated analog data from the submatrix boards with the prime data and provide output data to whichever coder (1 or 2) is being used. Output boards I-A, I-B, II-A, and II-B are not used for analog data processing.

The digital channel data block diagram, figure 21, illustrates the flow of digital data through the multiplexer. All prime and subcommutated digital data is applied to output

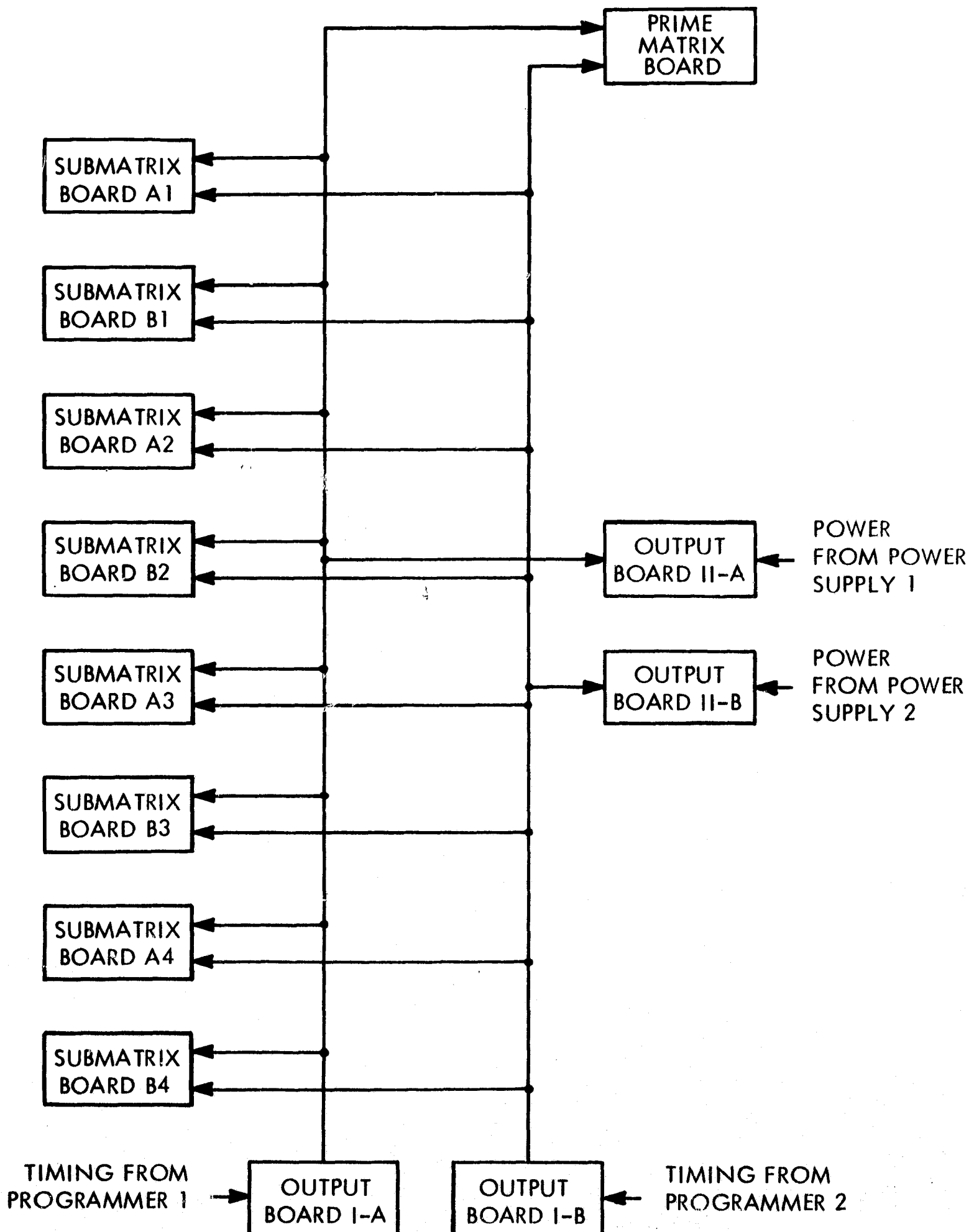


Figure 19. Multiplexer Signal Flow Block Diagram - Commands and Power

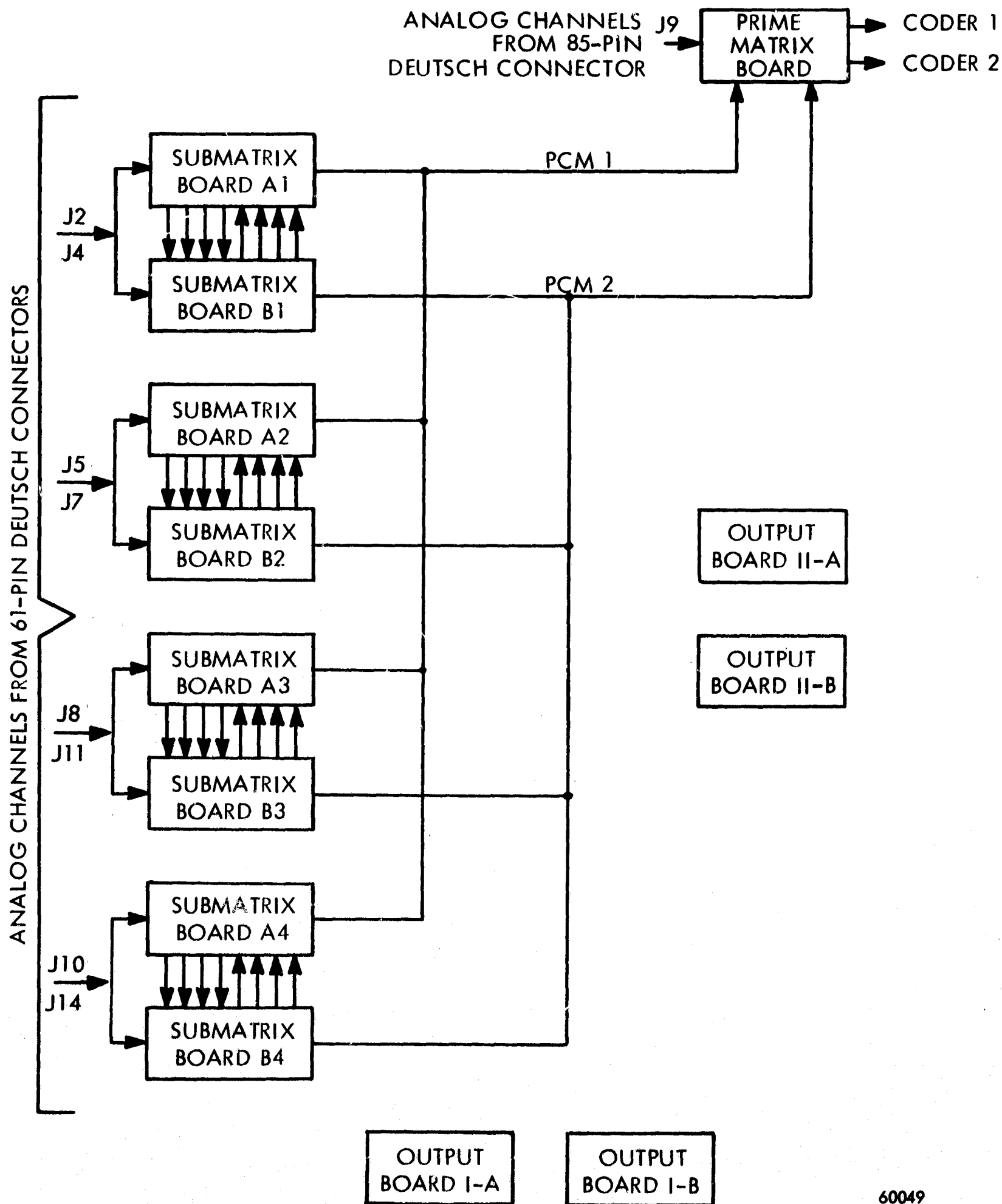


Figure 20. Multiplexer Signal Flow Block Diagram - Analog Channel Data

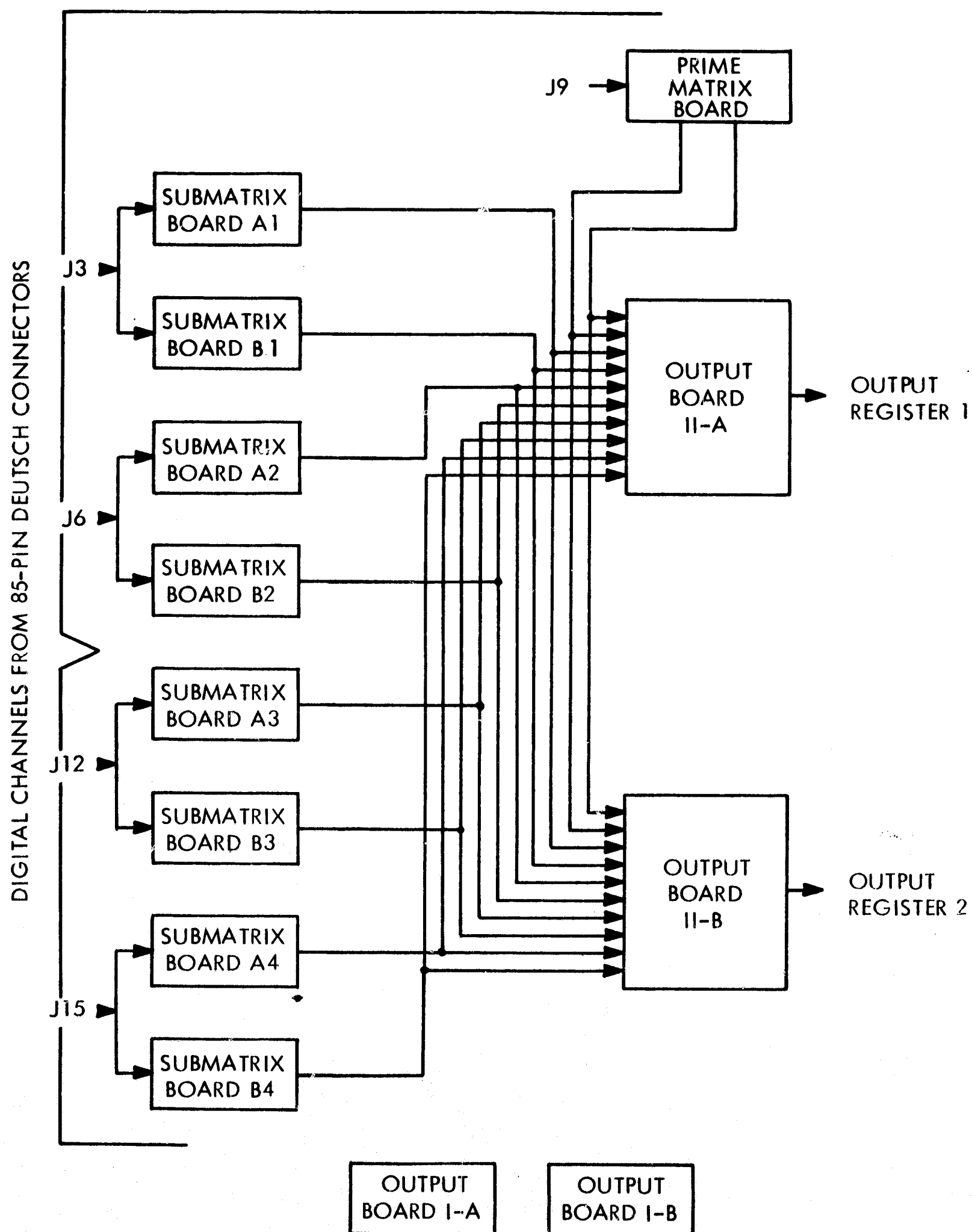


Figure 21. Multiplexer Signal Flow Block Diagram - Digital Channel Data

boards II-A and II-B on separate lines from the prime matrix and each submatrix board. Each data line represents seven outputs (one for each data bit position), with a maximum of five sequential channels on each line. Output board II-A provides the data output to the output register when PCM 1 is being used; output board II-B supplies the data output when PCM 2 is being used. Output boards I-A and I-B are not used for digital data processing.

The 13 multilayer circuit boards that comprise the multiplexer contain analog and digital channel input gates, time code gates, gate drivers, row and column drivers, sync and ID generator, analog and digital channel sequencers, word and subframe counters, GPA detector circuits, overvoltage protection circuits, and overvoltage control circuits. However, only four basic types of printed circuit boards are used. The four types are discussed in detail in the following subparagraphs; associated schematic, logic, and timing diagrams are used when necessary.

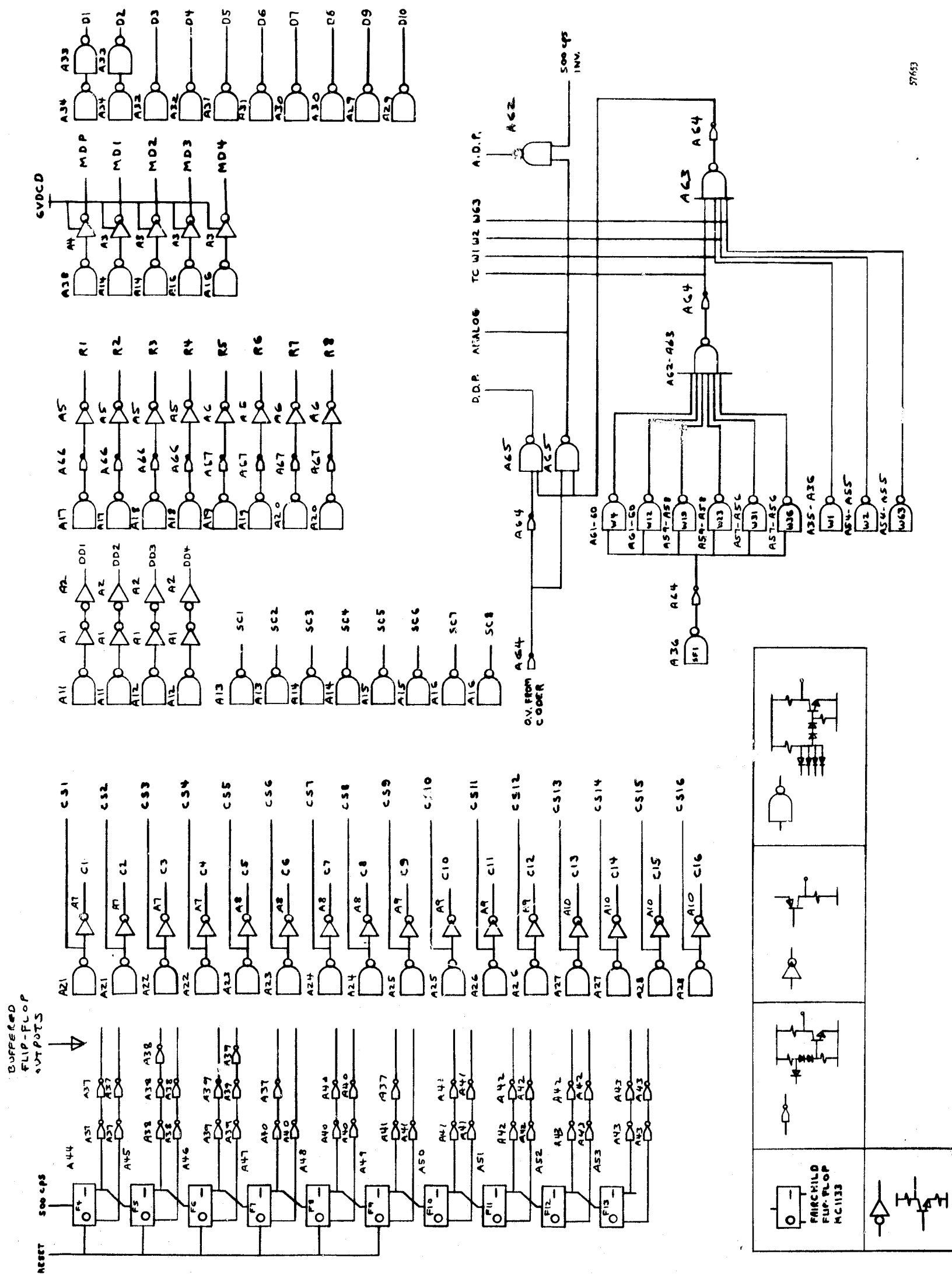
a. Output Board I. Output board I is block-redundant and furnishes the multiplexer timing commands. Figure I-4 and I-5 are schematic diagrams of output boards I-A and I-B, respectively. The output board I logic diagram is presented in figure 22.

The basic countdown is accomplished by the 62.5:1 word counter (flip-flops F4 through F9) and the 16:1 subframe counter (flip-flops F10 through F13). Each counter stage is contained in one flat-pack at locations A44 through A53, respectively. Inverters A37 through A43 buffer the flip-flop outputs from the NAND gate loads. The remaining NAND logic (C1 through C16, CS1 through CS16, DD1 through DD4, SC1 through SC8, R1 through R8, MDP, MD1 through MD4, and D1 through D10) produces the timing shown in figures 23 and 24. Figure 23 is a timing diagram of the prime commands from the word counter; figure 24 is a timing diagram of the subcommutated commands from the subframe counter. All commands are duty-cycled to conserve power, with the normally off condition being a positive level. Thus, the off condition appears as a positive pulse when duty-cycle power is applied. The on condition is signified by a lower level (absence of pulses).

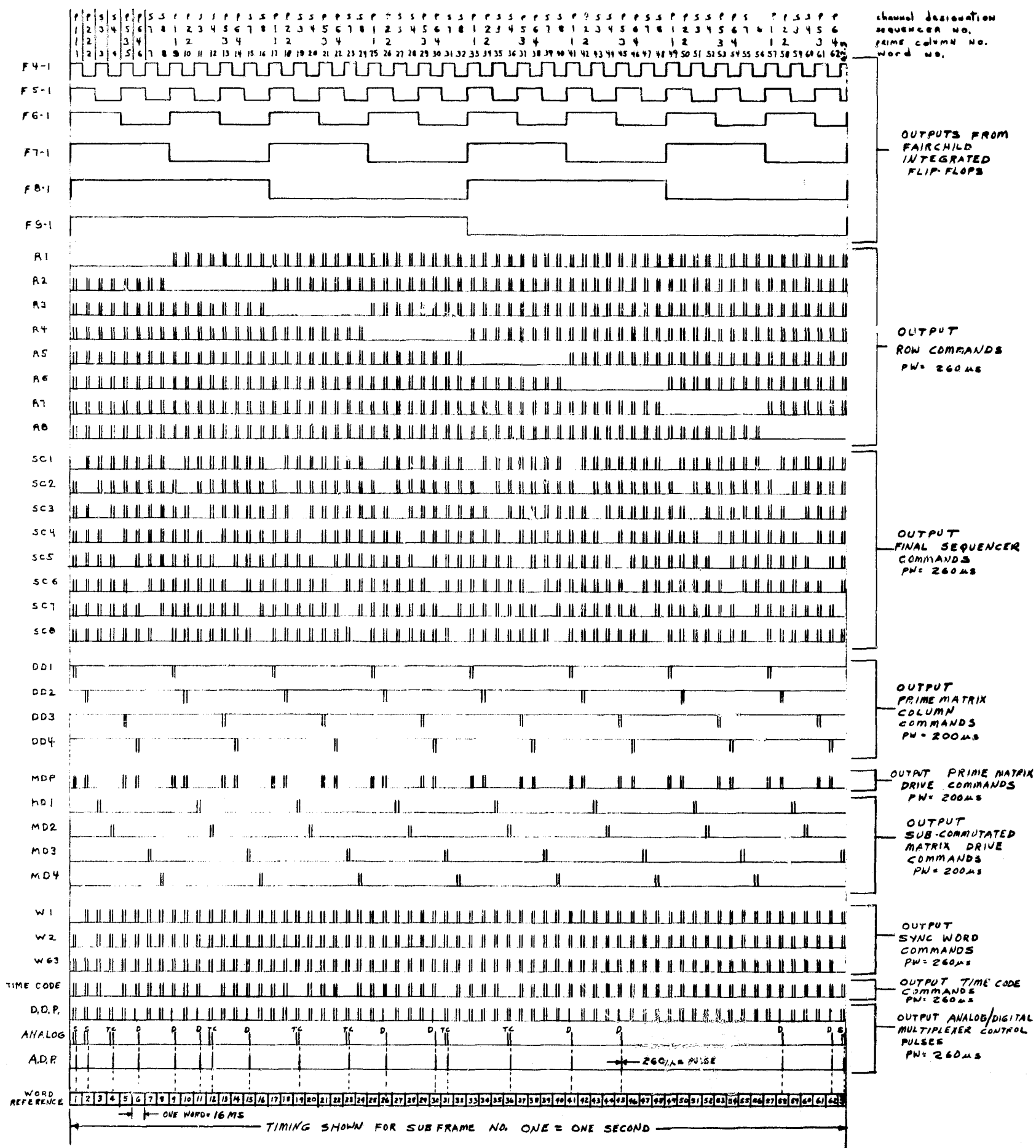
The logic circuits shown in the lower-right portion of figure 22 determine the multiplexer data output to the output register. When A64 receives an "up level" input from the coder, digital data is sent to the output register. When A64 receives a "down level" input, digitized analog data from the coder is read out. The remaining gates provide inhibit action during sync and time code word times.

b. Output Board II. Output board II is block-redundant and provides all system data to the output register. Figures I-6 and I-7 are schematic diagrams of output boards II-A and II-B, respectively. The output board II logic diagram is presented in figure 25.

Output circuits are provided by general purpose amplifiers (GPA's) A17, A22, A25, A28, A31, A38, A41, and A44 for word bit positions 1 through 8, respectively. Bit 1 (DT0-1) through bit 8 (DT0-8) outputs are connected directly to the output register. MOSFET gates A2, A4, A6, A12, A14, A16, and A21 provide sync, ID, and time code data when commanded by gate drivers A7 and A8. The resultant outputs are applied to the GPA's in parallel with outputs from analog and digital word final sequencer MOS gates A24, A27, A30, A35, A37, A40, and A43.



TIMING DIAGRAM - OUTPUT BOARD #1

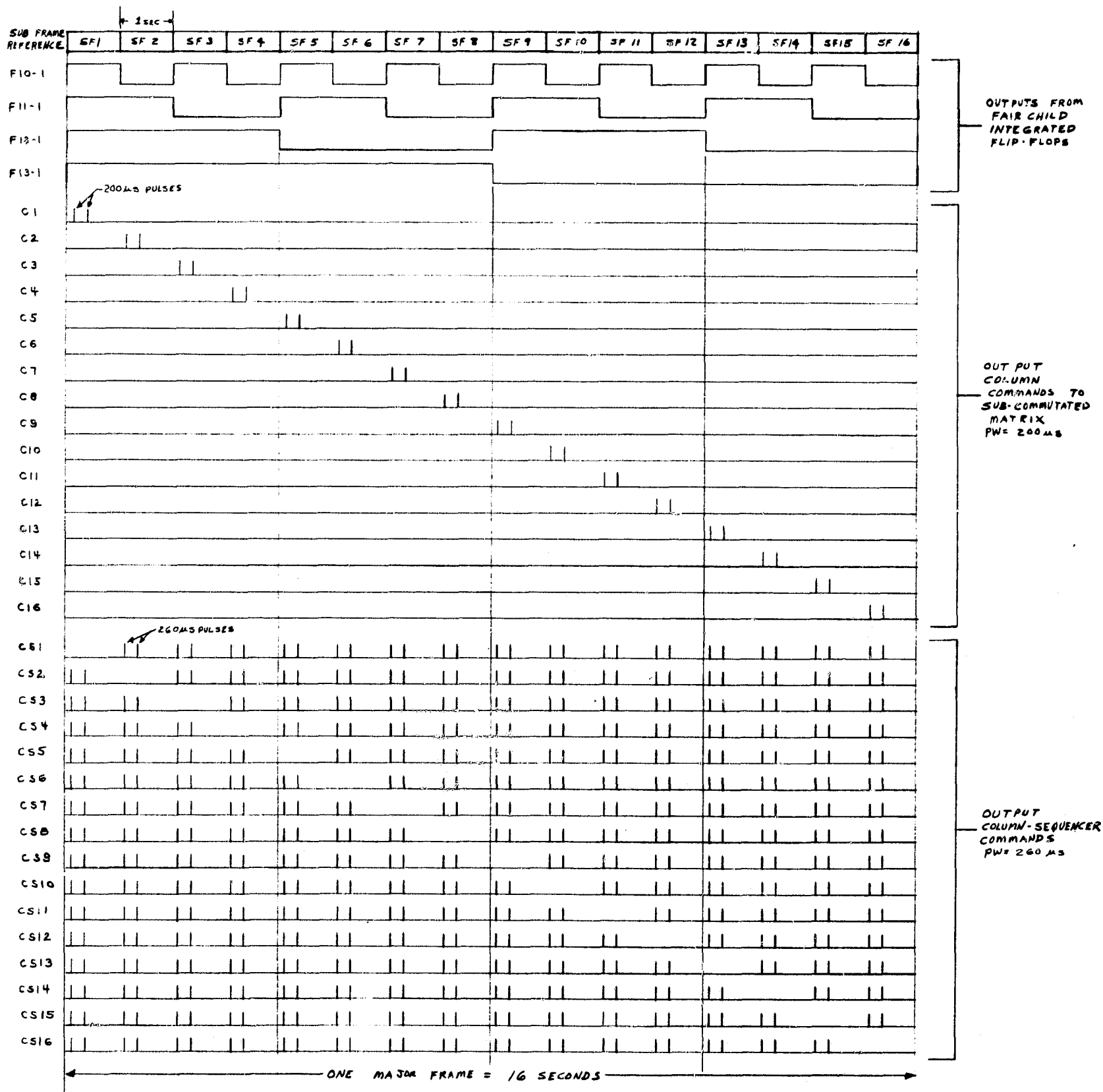


NOTES :

- ADP IS ABBREVIATION FOR "ANALOG DETECTION PULSE", DDP IS ABBREVIATION FOR "DIGITAL DETECTION PULSE". THESE PULSES ARE CONTROLLED BY THE "OVER VOLTAGE" COMMAND INTO THE CODER AND DETERMINE WHICH MULTIPLEXER GATE (ANALOG OR DIGITAL) IS READ INTO THE GPA'S AND OUTPUT REGISTER

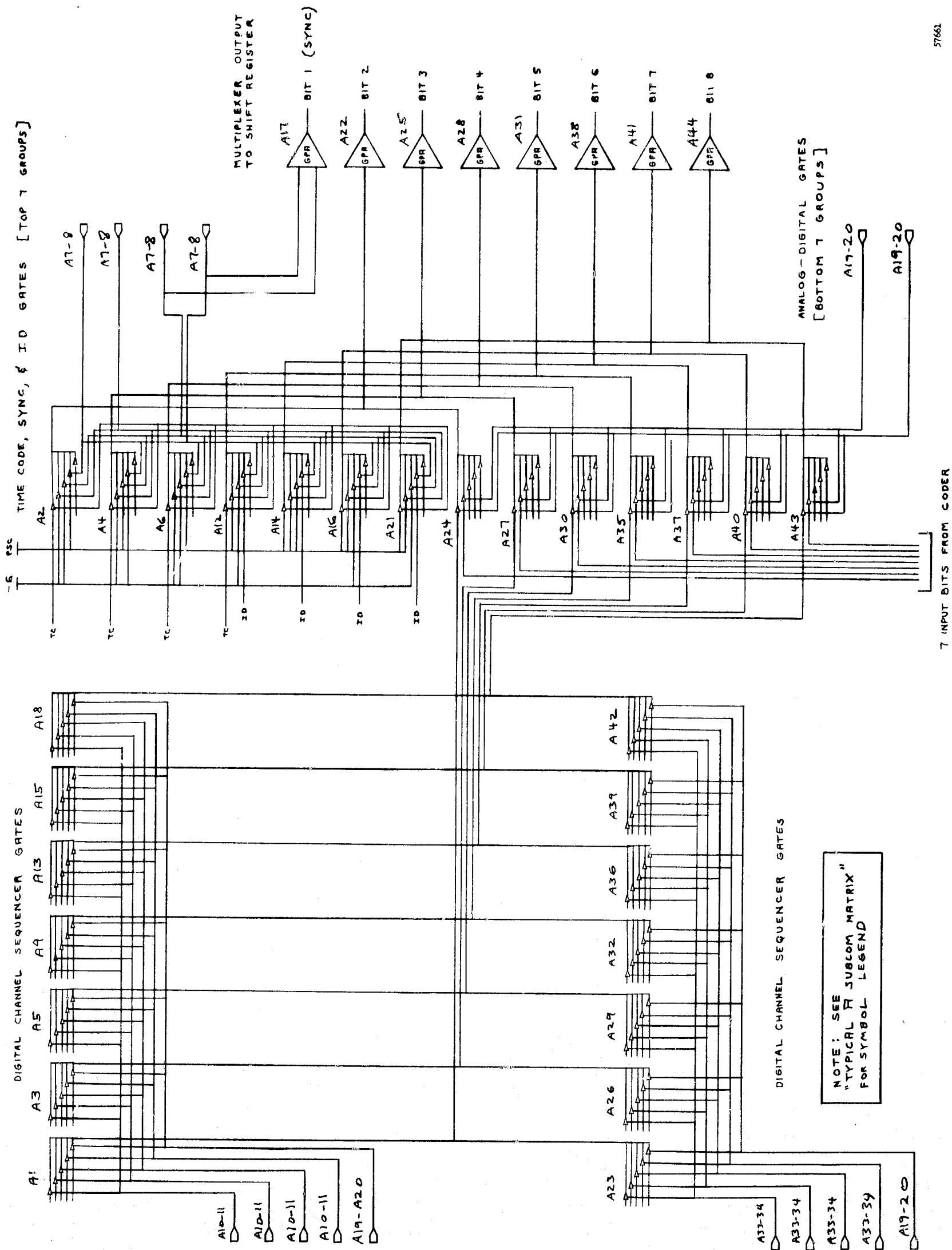
5765A

Figure 23. Output Board I - Prime Commands, Timing Diagram



57655

Figure 24. Output Board I - Subcommutated Commands, Timing Diagram



57661

Figure 25. Output Board II - Logic Diagram

These final sequencer gates are controlled by the overvoltage command from the coder through output board I. The final sequencer gate drivers are located in flat-packs A19 and A20, with digital commands controlling digital data and analog commands controlling analog data.

The second tier of sequencers for all digital data is comprised of A1, A3, A5, A9, A13, A15, A18, A23, A26, A29, A32, A36, A39, and A42; the associated gate drivers are located in flat-packs A10, A11, A19, A20, A33, and A34. As shown by the DGP numbers on the left side of figures I-6 and I-7, the top input to each MOSFET sequencer controls prime digital channels and the other four inputs to each sequencer control one-fourth of the subcommutated digital channels.

Special power conditioner circuits are shown in the right side of figures I-6 and I-7. These circuits are used to isolate redundant power inputs to the redundant multiplexer control circuits.

c. Prime Matrix Board. The prime matrix board is nonredundant and accepts all digital and analog channel inputs to the multiplexer. Figure I-8 is a schematic diagram of the prime matrix board. The prime matrix board logic diagram is presented in figure 26.

The prime matrix board contains 21 nonredundant analog channel input gates and 70 nonredundant digital channel input gates. However, only 63 digital channel input gates are used. Two block-redundant sets of output analog sequencers connect the analog input data sources (prime or subcommutated) to either coder 1 or coder 2. The digital channel input data is processed through two identical groups of 35 channel gates that are connected separately to output boards II-A and II-B.

Prime analog channel gates are contained in flat-packs A13 through A20; the associated gate drivers are located in flat-packs A28 through A35. Control drivers for PCM 1 (A) are A43 and A45; whereas, control drivers for PCM 2 (B) are A44 and A46. Prime analog channel sequencers (second tier), NPN drivers, and PNP drivers are A9, A8, and A7 for PCM 1 and A10, A11, and A12 for PCM 2, respectively. Subcommutated analog channel sequencers (second tier), NPN drivers, and PNP drivers are A3, A2, and A1 for PCM 1 and A4, A5, and A6 for PCM 2, respectively.

The first group of 35 digital channel gates is contained in flat-packs A21 through A27, and the second group is contained in flat-packs A36 through A42. Output boards II-A and II-B contain the second and third (final) tiers of digital channel sequencers.

Figure 26 shows the 4 column by 8 row prime matrix that generates all 32 prime time slots. Since only one column and one row are operating at any one time, only one channel gate can be turned on. During sync words 1 and 2, an open-circuit voltage is applied to the coder, with a resultant floating output from the MOSFET gates for prime time slots 1 and 2 (A13 and A15). During analog words 1A1 through 1A21, the associated channel input is coupled through the input gate and one output sequencer to the selected coder. During digital words, the associated analog channel gate supplies a -15-vdc level to the coder. The resultant overvoltage causes read-out from the digital data final sequencer in output board II-A or II-B. At

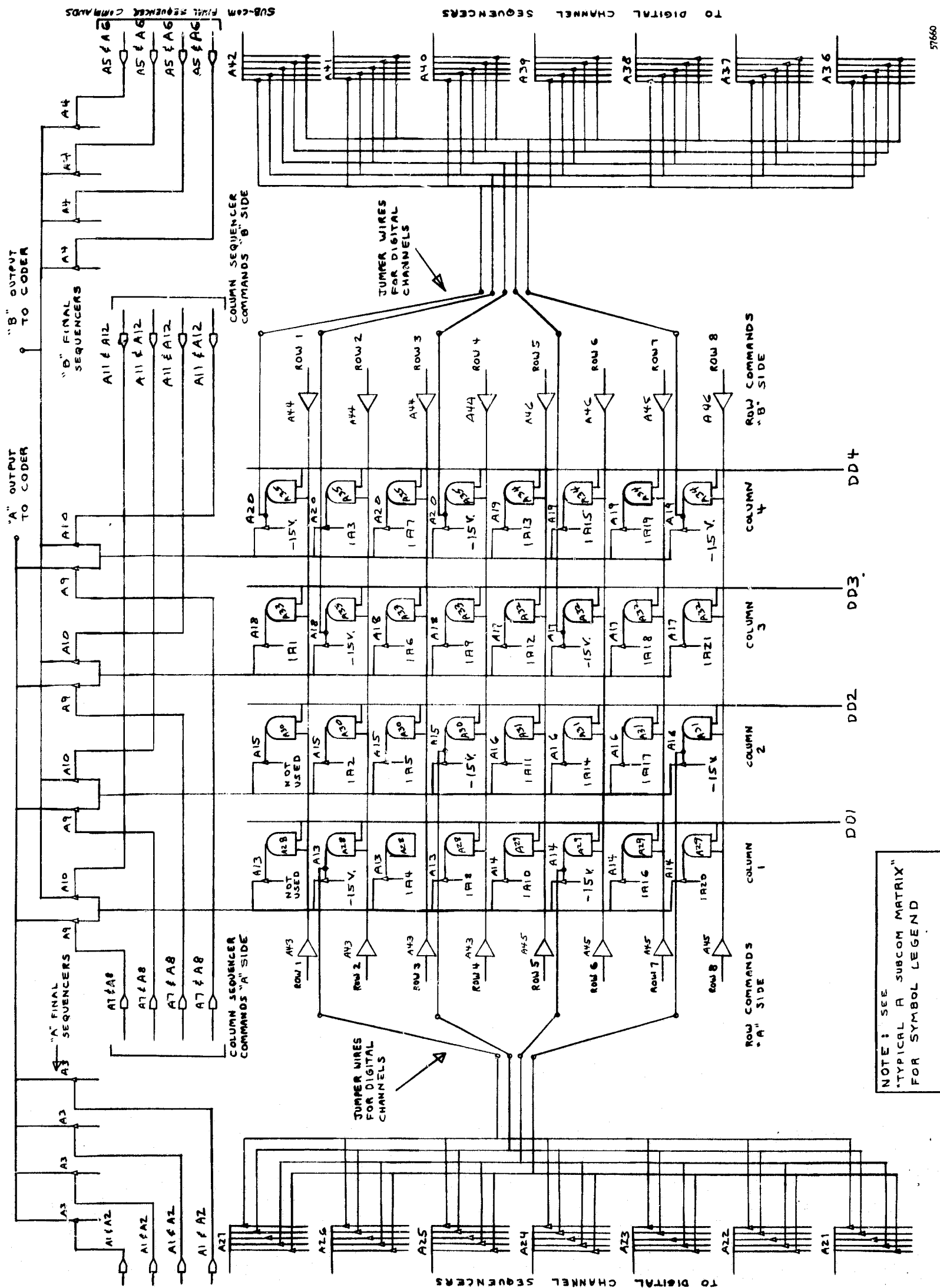


Figure 26. Prime Matrix Board, Logic Diagram

the same time, seven parallel digital gates open and allow digital data to flow through the final sequencers (controlled by the coder) to the GPA's. Thus, the prime gates consist of the following:

- (1) 21 Prime Analog Input Channels
- (2) 9 Overvoltage (-15-vdc) Commands to Coder for 63 Digital Channels
($9 \times 7 = 63$)
- (3) 2 Unused Gates During Sync Words 1 and 2

d. Submatrix Board. Eight submatrix boards contain the nonredundant input channel gates that control all 434 subcommutated analog channels and 280 subcommutated digital channels. All eight boards are identical, except that one multilayer is reversed in four boards to simplify wiring when the boards are fabricated in pairs (back-to-back). Separate schematics (figures 1-9 through 1-16) are presented for submatrix boards A1 through A4 and B1 through B4, respectively, to show proper input channel gate nomenclature and the front panel connectors involved. However, only one logic diagram (figure 27) is shown because all submatrix boards use the same logic. Submatrix board operation is identical to prime matrix board operation, except for frequency (1/16 cps) and the number of sequencers involved.

Subcommutated analog channel gates are contained in flat-packs A10 through A17 and A46 through A53; associated channel gate drivers are A21 through A28 and A31 through A38, respectively. Row command drivers are A29 and A30, with the redundant drivers located on the other board of the pair. Column command drivers are A54 and A55 for PCM 1 and PCM 2. The second tier of analog channel sequencers, NPN drivers, and PNP drivers are A4, A5, and A6 plus A7, A8, and A9, respectively. The redundant sequencers, NPN drivers, and PNP drivers are A1, A2, and A3 plus A18, A19, and A20, respectively.

Flat-packs A39 through A45 contain the 35 subcommutated digital channels. The seven outputs are applied to the second tier of sequencers on output board 11-A or 11-B.

Figure 27 shows the 8-row by 8-column matrix that can generate 64 time slots. Thus, the eight submatrix boards can provide 512 time slots; however, only 488 are used in the new 62.5 word frame. Since sync word 62.5 is a subcommutated time slot (63) that requires only 4 bits, the 16 subframes require only 8 time slots. This leaves a maximum of 480 subcommutated input data time slots. The assigned time slots are as follows:

- (1) 434 Subcommutated Analog Input Channel Time Slots
- (2) 40 Overvoltage (-15-vdc) Command Time Slots to Coder for 280 Digital Channels ($40 \times 7 = 280$)
- (3) 6 Time Code Output Time Slots
- (4) 8 Unused Time Slots During Sync Word 62.5 (16 Unused Channel Gates)

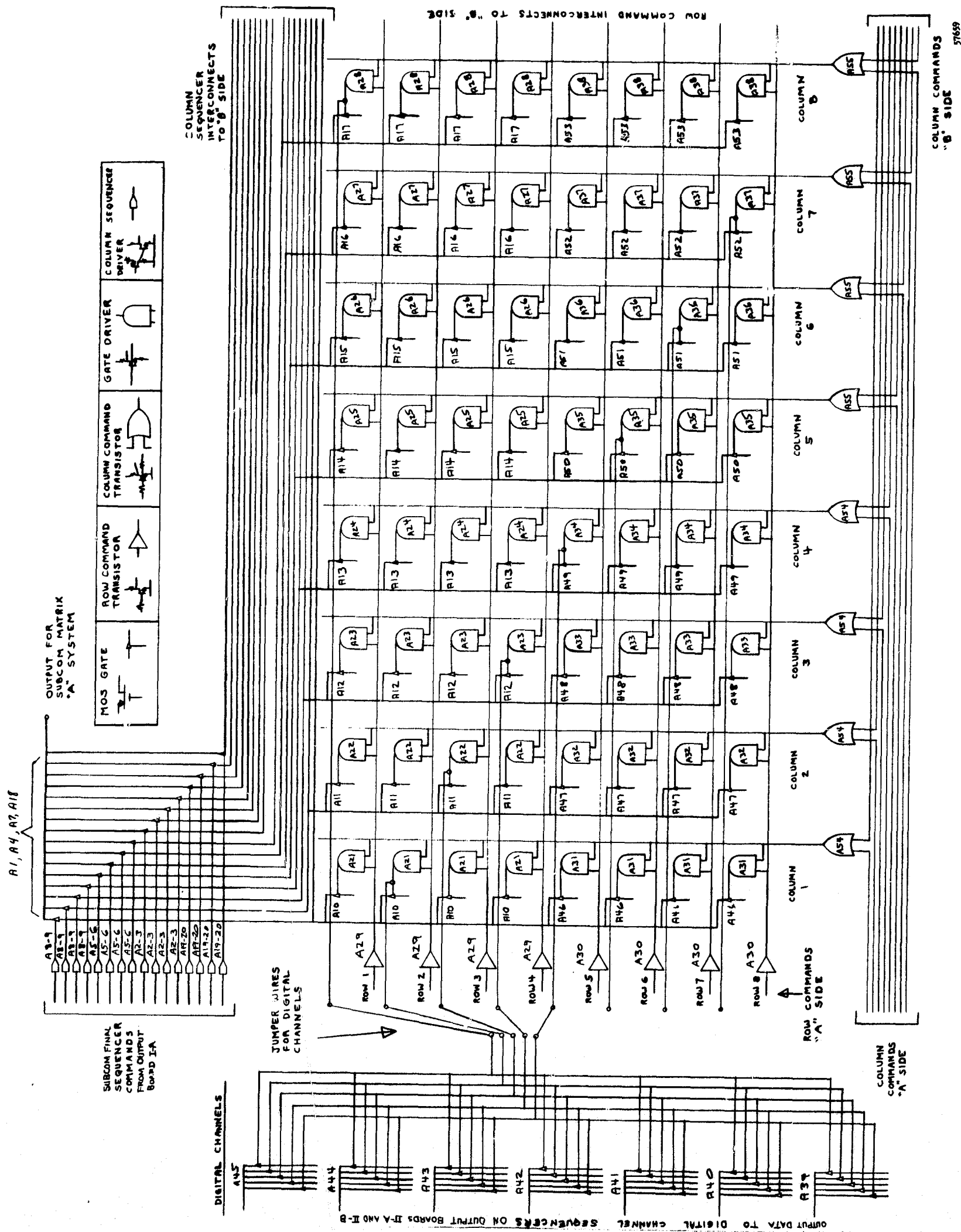


Figure 27. Submatrix Board, Logic Diagram

2.3.1.2.2 MULTIPLEXER TIMING. In the Nimbus B output format, one major frame completes a sampling of all channels. Each major frame contains 16 subframes; each subframe is comprised of 62.5 8-bit words. Subframe sync occurs during the first four bits of word 63 (62.5), the full eight bits of word 1, and the first four bits of word 2. The last four bits of word 2 contains subframe ID. Bit sync occurs in bit 1 of all other words and is a ZERO in all except words 1 and 2. The remaining seven bits contain data.

Figure 28 is a multiplexer timing diagram. The first six multiplexer counters (F4 through F9) generate word timing for the 62.5 words per subframe. These counters require 1 second to complete sampling of all 62.5 words (one subframe). Bit and word counters are externally reset by the 1-cps signal from the Nimbus C clock so the time code can be properly placed in the output format. The last four counters (F10 through F13) generate subframe timing and count-out the 16 subframes in each major frame. These counters require 16 seconds to complete sampling of all 16 subframes (one major frame) and are not reset.

Words alternate between two prime and two subcommutated words, as shown in the following sequence (8-member time slot pattern):

- a. Prime Matrix, Column 1
- b. Prime Matrix, Column 2
- c. Submatrix A1 or B1
- d. Submatrix A2 or B2
- e. Prime Matrix, Column 3
- f. Prime Matrix, Column 4
- g. Submatrix A3 or B3
- h. Submatrix A4 or B4

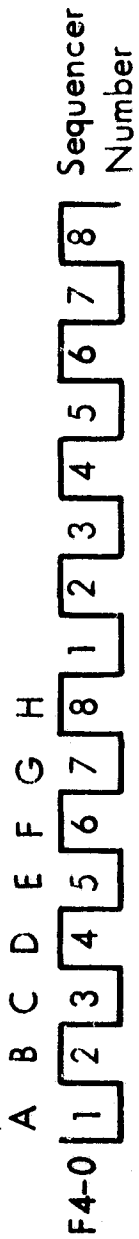
For example, the first eight elements sampled, beginning at t_0 , are:

- a. Row 1, Prime Column 1, Prime Matrix
- b. Row 1, Prime Column 2, Prime Matrix
- c. Row 1, Subcommutated Column 1, Submatrix A1 or B1
- d. Row 1, Subcommutated Column 1, Submatrix A2 or B2
- e. Row 1, Prime Column 3, Prime Matrix
- f. Row 1, Prime Column 4, Prime Matrix
- g. Row 1, Subcommutated Column 1, Submatrix A3 or B3
- h. Row 1, Subcommutated Column 1, Submatrix A4 or B4

After the row count cycles from 1 to 8, the subcommutated column moves to 2 and the prime column repeats the pattern shown above. This sequence continues until the subcommutated column count cycles through 16. Therefore, it is possible to assign an exact channel location for each time slot. Channel location assignments are made in accordance with the following rules:

- a. Subframe location is equivalent to subcommutated column position.

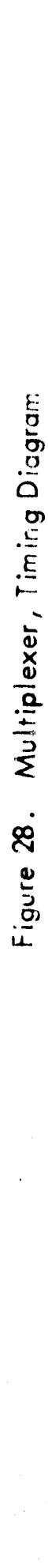
Notes



Notes:

- A. Prime Matrix, Column 1
- B. Prime Matrix, Column 2
- C. Submatrix A1 or B1
- D. Submatrix A2 or B2
- E. Prime Matrix, Column 3
- F. Prime Matrix, Column 4
- G. Submatrix A3 or B3
- H. Submatrix A4 or B4

Row Number



Column Number



Figure 28. Multiplexer, Timing Diagram

b. Row location depends upon time slot position, as follows:

<u>Time Slots</u>	<u>Row Location</u>
1-8	1
9-16	2
17-24	3
25-32	4
33-40	5
41-48	6
49-56	7
57-62.5	8

c. Subcommutated column or prime column location depends on position in the 8-member time slot pattern generating the prime, prime, subcommutated, subcommutated channel sequence.

The following examples illustrate use of the above rules:

a. Example 1. Find the location for time slot 31, subframe 1.

(1) Since subframe location equals subcommutated column position, the MOS gate is located in column 1.

(2) Since row location depends on time slot position and time slot 31 is in the fourth group of 8-member time slot pattern, the MOS gate is located in row 4.

(3) Since time slot 31 is the seventh member of the 8-member time slot pattern, the matrix position is submatrix A3 or B3. Since this channel is in the group composed of columns 1 through 8, the submatrix is A3.

(4) This channel is designated 1/16 units hours (table 5) and is the units of hours time code position. Thus, the MOS gate is not brought out to a connector.

b. Example 2. Find the location for time slot 36, subframe 14.

(1) Since subframe location equals subcommutated column position, the MOS gate is located in column 14.

(2) Since row location depends on time slot position and time slot 36 is in the fifth group of 8-member time slot patterns, the MOS gate is located in row 5.

(3) Since time slot 36 is the fourth member of the 8-member time slot pattern, the matrix position is submatrix A2 or B2. Since this channel is in the group composed of channels 9 through 16, the submatrix is B2.

(4) This channel is designated 1/16D33 (table 5) and is subcommutated (1/16) digital (D) channel 33 (33). Thus, the MOS gate is hard-wired on the submatrix board to the -15 volts for overvoltage.

c. Example 3. Find the location for time slot 18, subframe 6.

(1) Since subframe location equals subcommutated column position, the MOS gate is located in column 6.

(2) Since row location depends on time slot position and time slot 18 is in the third group of 8-member time slot patterns, the MOS gate is located in row 3.

(3) Since time slot 18 is the second member of the 8-member time slot pattern, the matrix position is prime matrix, prime column 2.

(4) This channel is designated 1A5 (table 5) and is prime (1) analog (A) channel 5 (5). Thus, this channel gates a prime analog signal.

The multiplexer counters are Fairchild MC1133 flip-flops that operate between PSC and +6 volts and utilize only 3 milliwatts per stage. However, the load capability is low. Figure 29 is a diagram of this counter. At t_0 , the ONE sides of the counters are set high. Since the counters switch on negative transitions, the ZERO sides are applied in a forward direction. Reset lines are normally +6 volts and are pulsed to ground for negative resets.

Westinghouse WM296 Hex NAND gates are used to buffer the flip-flop outputs. Figure 30 is a diagram of this buffer. It should be noted that each stage of buffering inverts the signal. Since power consumption is 11 milliwatts per gate, the Hex NAND gates, as well as the remaining multiplexer logic, are duty-cycled to reduce average power consumption to 1/40.

According to Westinghouse specifications, the gate fan-out at room temperature is 11 and at -55°C is 6. Since the low-temperature Nimbus specification is only -5°C, a nominal fan-out of 8 is used. Each Fairchild flip-flop is buffered from one to three times to provide sufficient drive to the Westinghouse logic.

Most of the multiplexer power supply voltages go through decoupling filters in programmer module 3. The decoupling filter on the +6-volt line consists of a 22-ohm resistor and a 300-microfarad capacitor to ground. Since the flip-flops are continuously on, this represents a constant current drain on the power supply of:

$$I_t = \frac{10 \text{ (flip-flops)} \times 3.3 \text{ (milliwatts per flip-flop)}}{6 \text{ (volts)}} = 5.5 \text{ milliamperes}$$

This current is taken direct from the power supply. If the current were taken out of the filter, there would be a constant voltage drop across the 22-ohm resistor. Multiplexer voltages are taken direct from the power supply in two places: (a) the +6-volt line for the counters and (b) the -6-volt line for sync data to the GPA's.

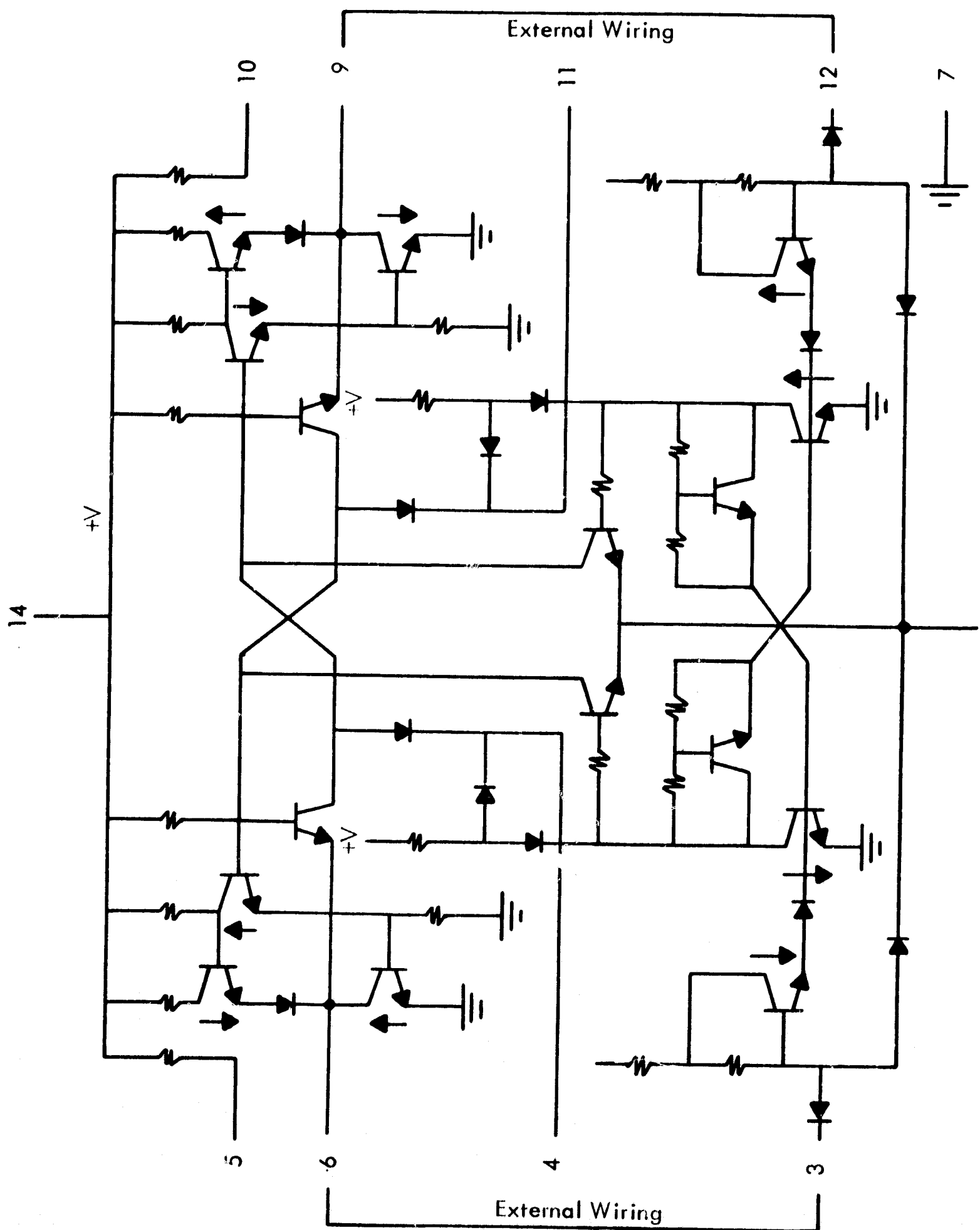


Figure 29. Fairchild MC1133 Flip-Flop, Schematic Diagram

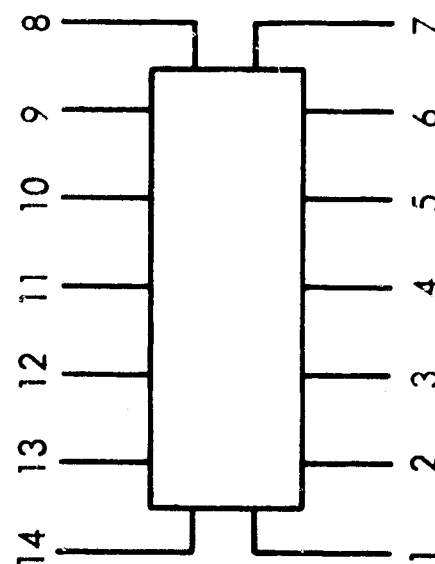
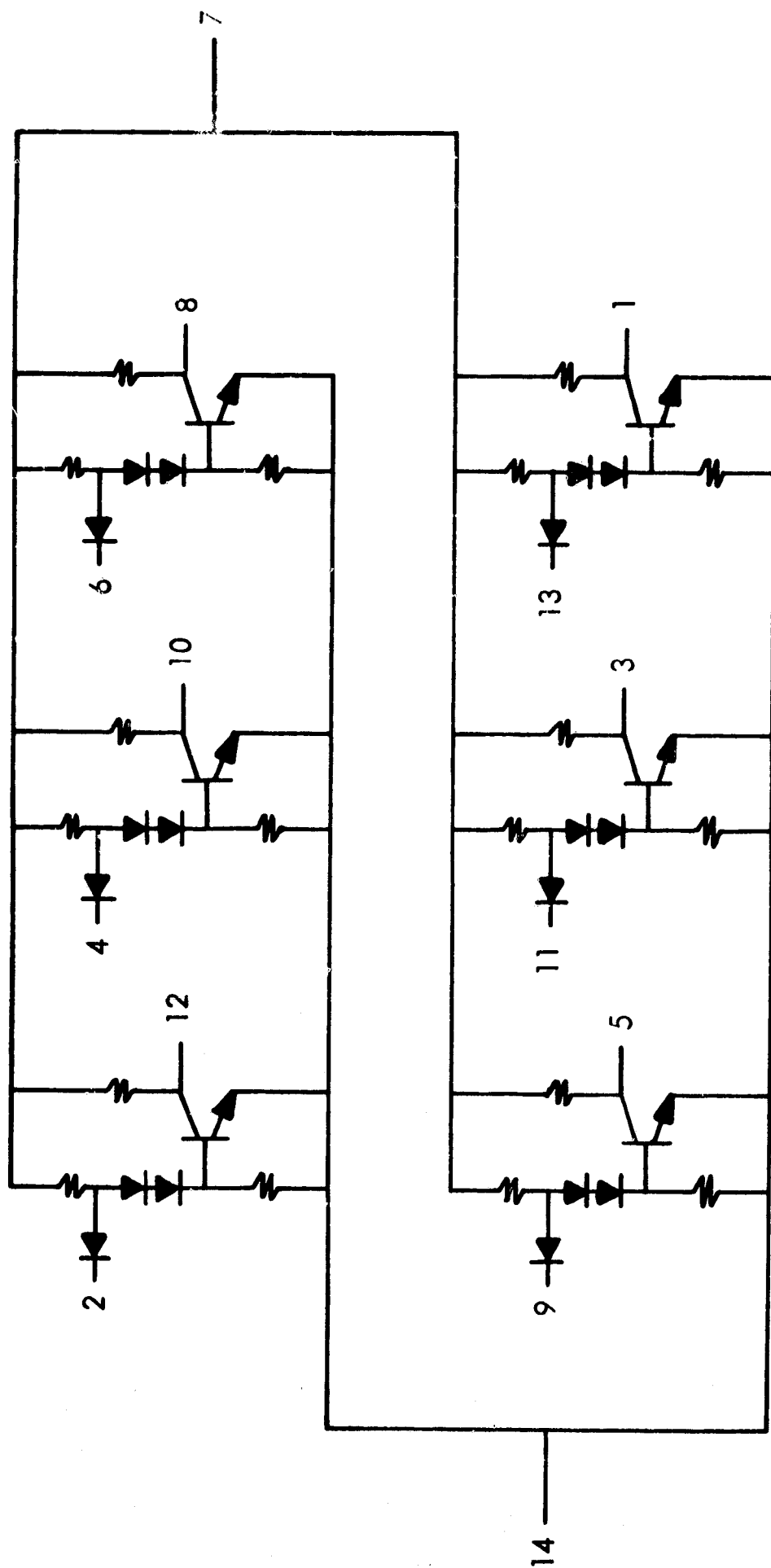


Figure 30. Westinghouse WM296 Hex NAND Gate, Schematic Diagram

2.3.1.2.3 MULTIPLEXER CONTROL CIRCUITRY AND MATRIX OPERATION. Row and column command circuitry controls operation of the multiplexer matrices. Figure 31 is a diagram of the row command circuitry. Row command circuitry utilizes a Westinghouse WM261 multiple-input dual NAND gate (figure 32) that is normally high and drops during row strobe time. The resultant output is applied through a normally low inverter to a Sprague PNP driver (figure 33), and causes the driver collector to return to -24 volts. (The PNP driver is normally on with the collector high.) This applies a positive voltage to the five 27K ohm resistors that go to the four row command transistors on the submatrices and the one row command transistor on the prime matrix. (The row command transistors are normally on.)

Collector voltages of the row command transistors are returned through external 3.9K ohm resistors to a matrix drive (MD) line. There are five MD commands: four for the submatrices and one for the prime matrix. The MD line swings from -24 to +6 volts at the delayed duty-cycle rate. Each MD line swings positive only during the strobe time for that particular matrix. The MD voltages save power and prevent switching transients in the logic from reaching the matrix. Thus, although five row command transistors in the different matrices receive base drive for any one strobe, only one submatrix or the prime matrix obtains collector voltage.

Figure 34 contains schematic and logic diagrams of the column command circuitry. Column command circuitry is identical to row command circuitry, except an inverter is not used because column command transistors are normally off.

Two differences exist between row and column command circuitry: (a) each column command PNP driver drives four column command transistors through 82K ohm resistors instead of five row command transistors through 27K ohm resistors; and (b) there is only one column command transistor common to A and B (PCM 1 and PCM 2), whereas there are two row command transistors for each row (one for A (PCM 1) and one for B (PCM 2)). Since prime column sequencing occurs at a different rate than submatrix column sequencing, prime column sequencers and drivers have their own timing and drive circuitry. Actual row command transistors and column command transistors are strobed at the delayed duty-cycle rate.

The actual row and column command matrix is shown in figure 35. Between strobes, the MD line holds the row line at -24 volts. During matrix strobes (but not a particular row), that row command transistor is turned on and the column command transistor is turned off. The row command transistor clamps the row line to -24 volts. The column command transistor applies a bias voltage of approximately -24 +5 volts through a collector resistor to the matrix column line column command (CC). Since the emitters of all gate drivers are then +5 volts with respect to the base, all gate drivers on that particular row are off.

When a matrix element is strobed, the associated row command transistor turns off and the associated column command transistor turns on. This applies +6 volts through some resistance to the row line and applies -24 volts to the column line. This selects a particular matrix element. When a matrix element turns on, the particular row line voltage is clamped at approximately -24 +2 volts. However, since the column bias voltage is -24 +5 volts, the remaining gate drivers on that row are still back-biased and are off.

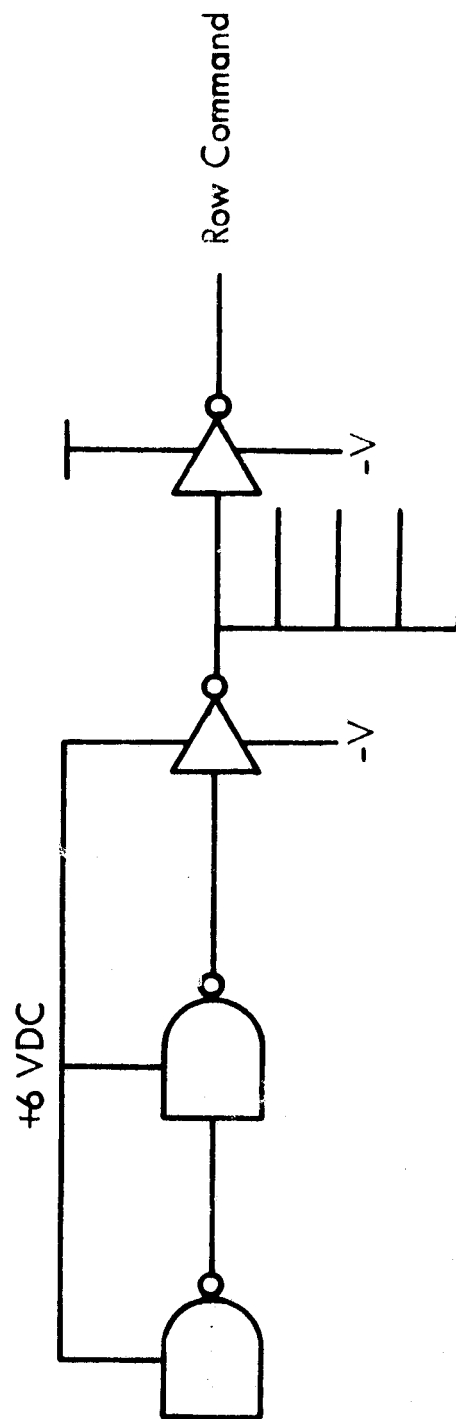
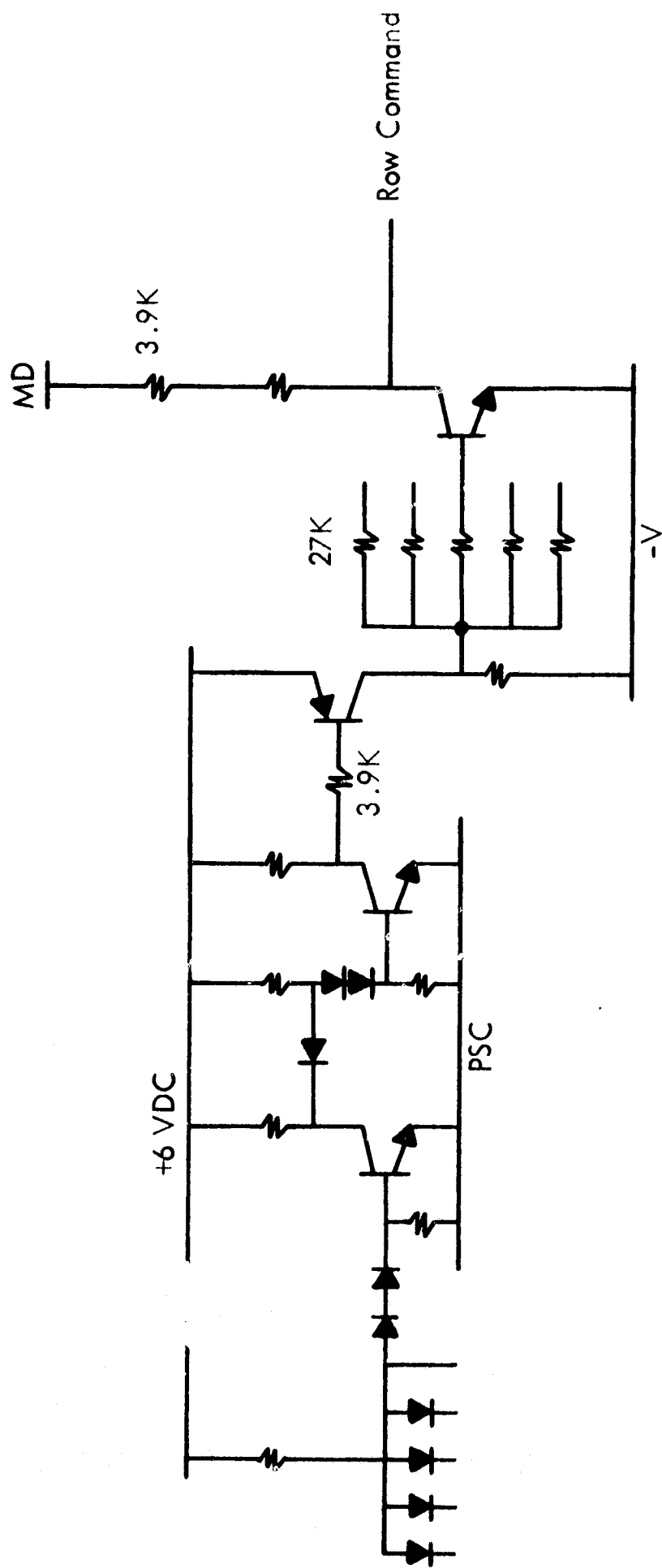


Figure 31. Row Command, Schematic and Logic Diagrams

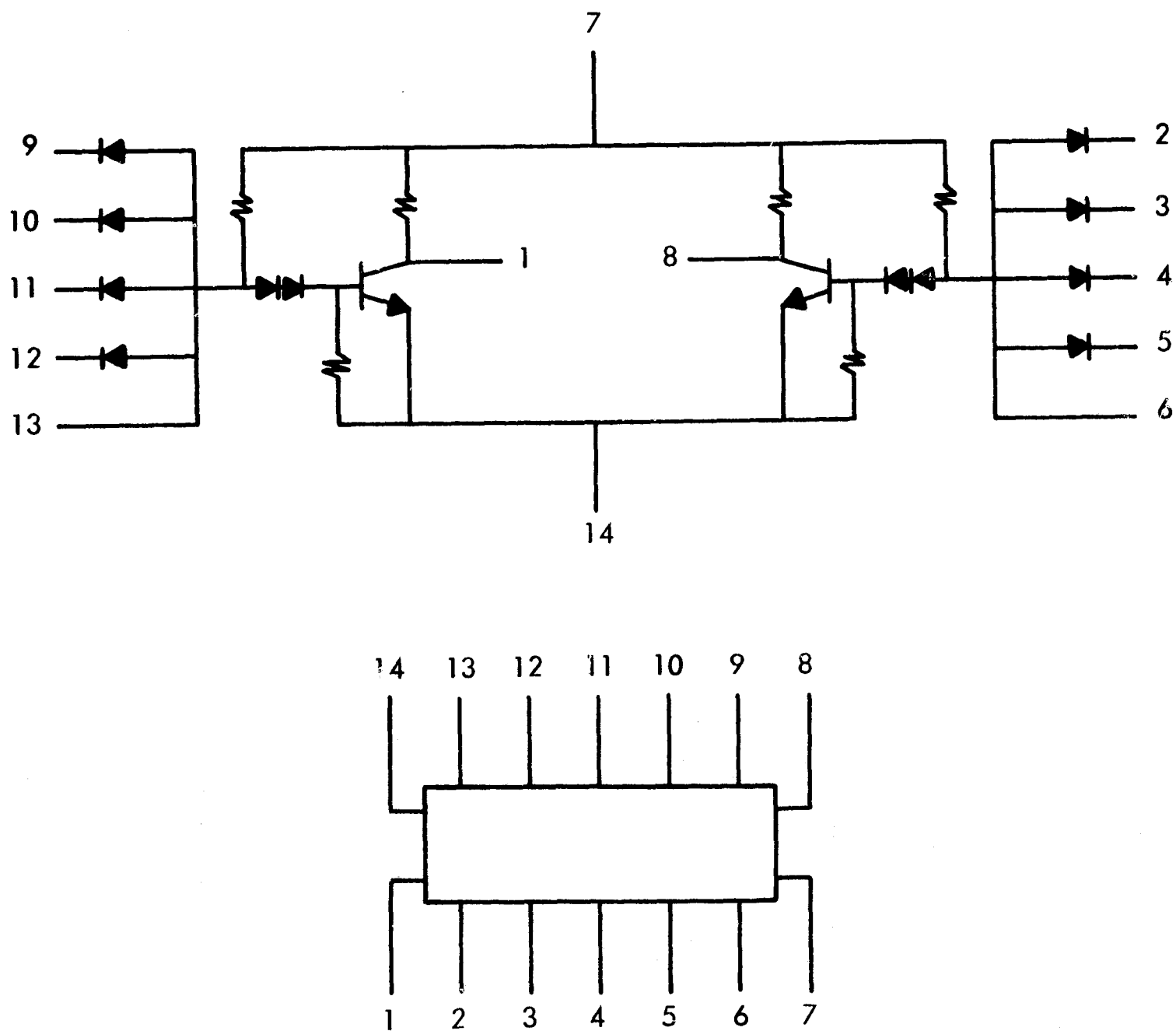


Figure 32. Westinghouse WM261 Dual NAND Gate, Schematic Diagram

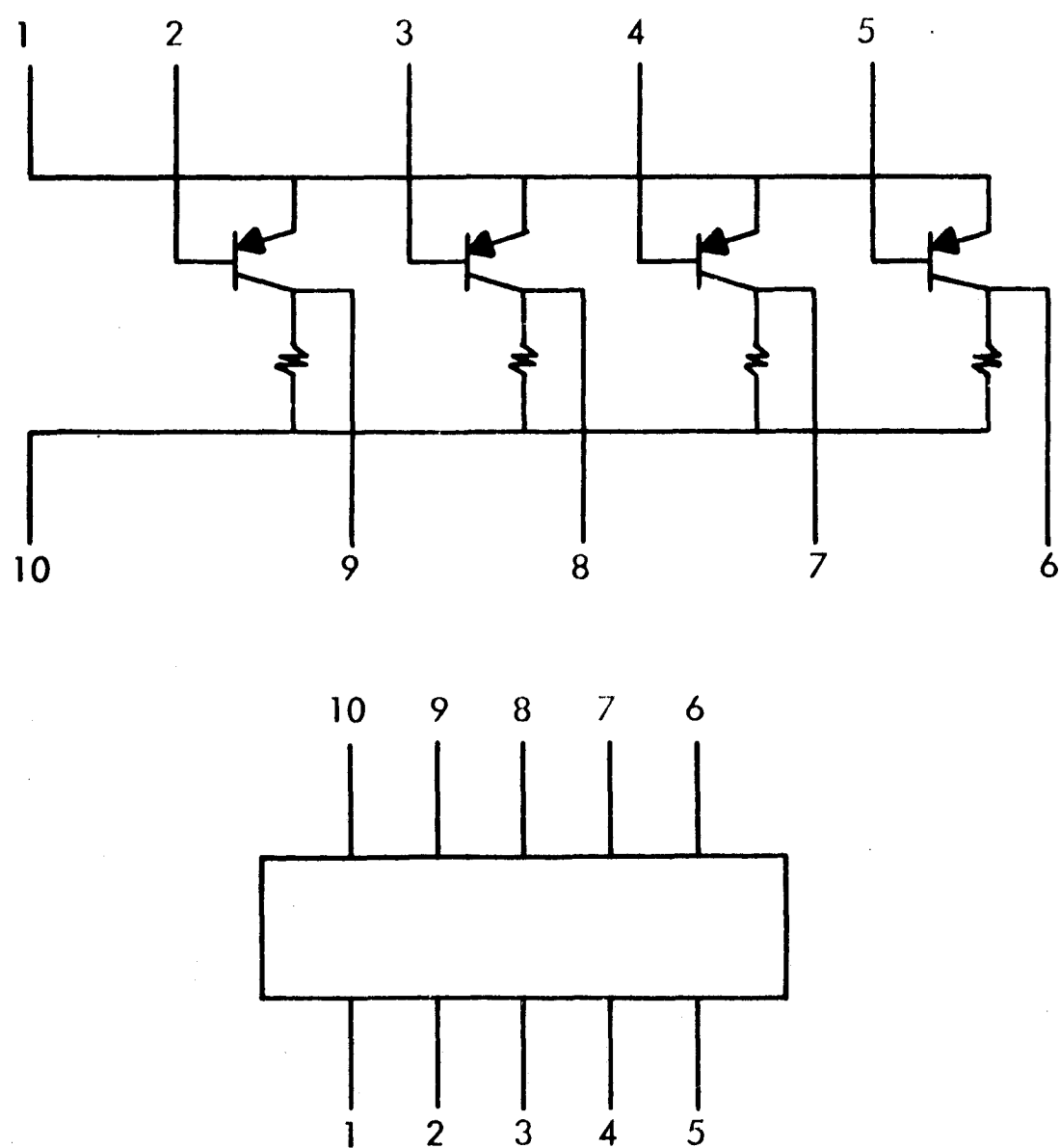


Figure 33. Sprague PNP Driver, Schematic Diagram

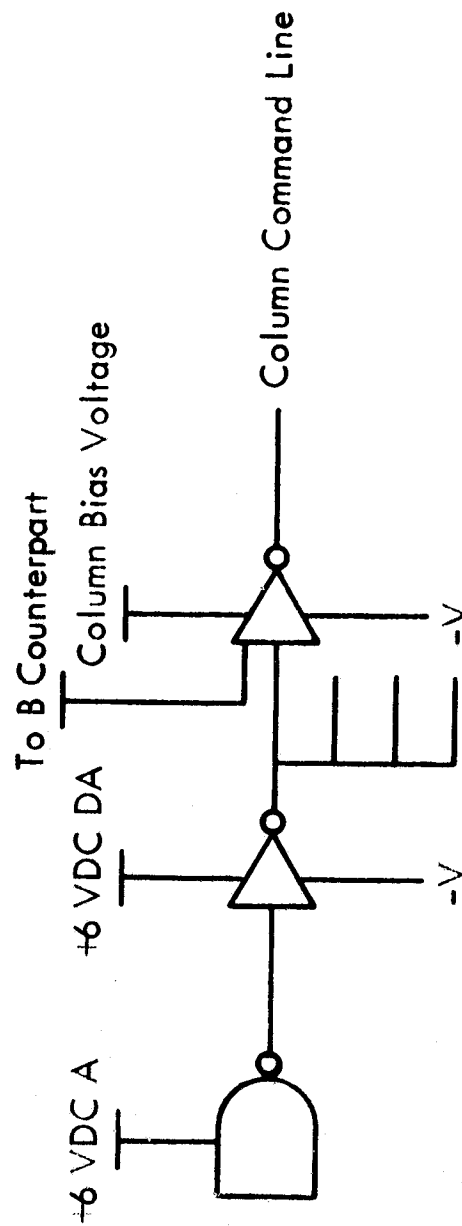
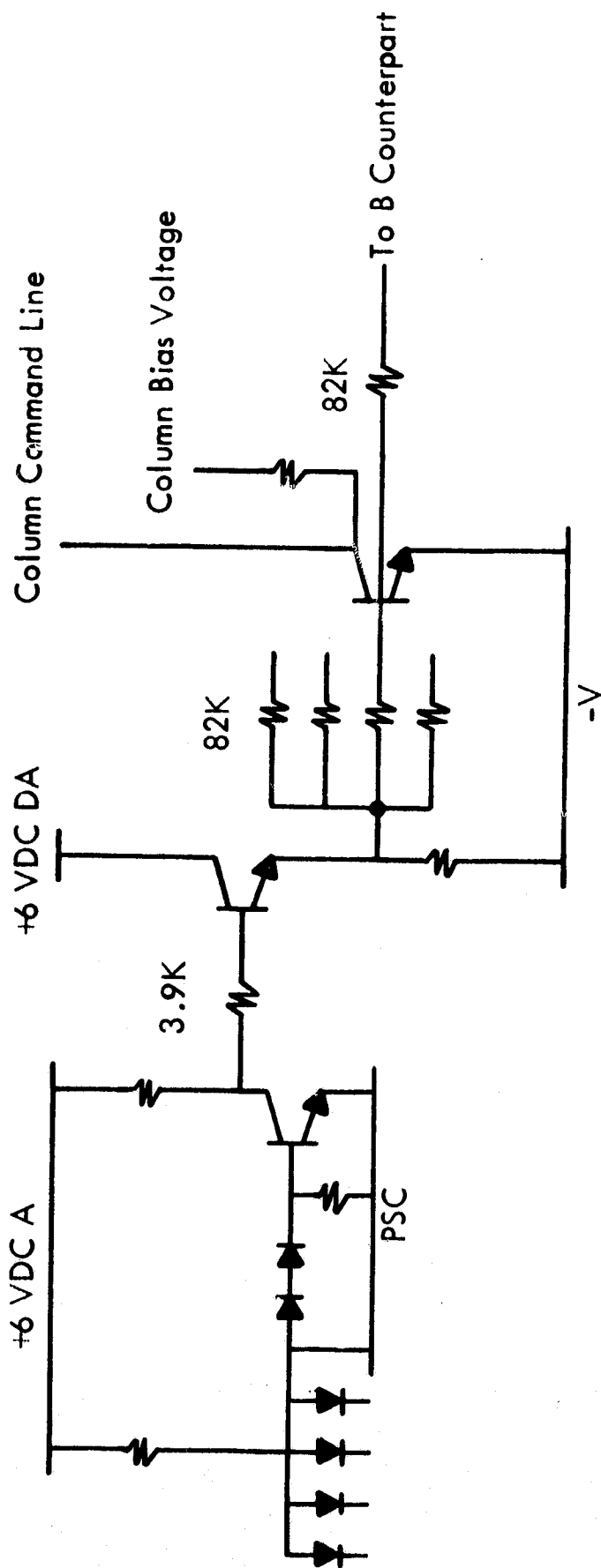


Figure 34. Column Command, Schematic and Logic Diagrams

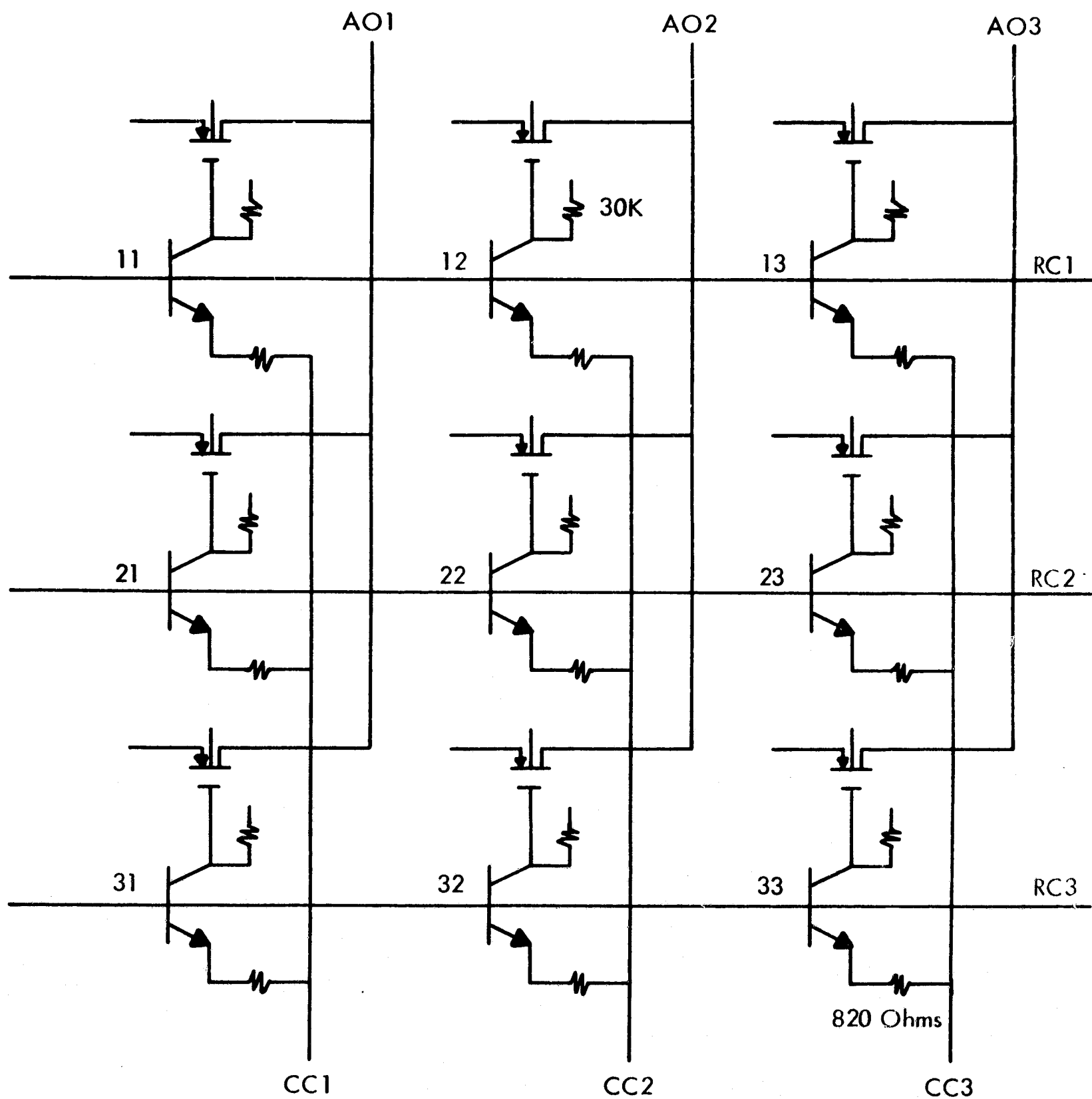


Figure 35 . Actual Row Command and Column Command Matrix, Schematic Diagram

a. Matrix Design Theory. When a gate driver is off, +6 volts is applied to the MOSFET gate through a 30K ohm flat-pack resistor and an external 3.9K ohm resistor to limit the current if the 30K ohm resistor shorts out. These external limiting 3.9K ohm resistors are used extensively throughout the multiplexer.

According to the Fairchild specification, the maximum threshold voltage for MOSFET gate turn-on is 7 volts. Figure 36 is a schematic diagram of the Fairchild MOS gate. Since the overvoltage used by the multiplexer for digital channel indication is -15 volts, this sets the minimum low voltage of the multiplexer at

$$V = -15 - 7 = -22 \text{ volts}$$

The negative voltage is set at -24 volts to allow for worst-case variations.

When the gate driver is on, the MOSFET gate voltage drops from +6 volts to -24 volts. The current flowing in the gate at that time is

$$I = (24 + 6) \text{ volts} / (30K + 0.82K + 3.9K) = 0.9 \text{ ma}$$

(The 0.82K ohm resistor is the gate driver emitter resistor and is discussed below.) Thus, at this time the base line of the on gate driver is clamped at

$$V = -24 + V_{CE(SAT)} + 0.9 \text{ ma} \times 820 \text{ ohms} + V_{BE(SAT)}$$

The approximate worst-case values of the above voltages are:

$$V = -24 + 0.2 + 0.8 + 0.8 = -24 + 1.8 \text{ volts}$$

Since the column bias voltage is set at -24 +5 volts, the remaining gate drivers in the row stay off.

Consider the simplified matrix shown in figure 37. Assume that the column command transistor is shorted-out, thus applying -24 volts to CC 1, and that strobing is for element 13. A minimum base voltage of

$$V = -24 + V_{CD(SAT)} + V_{BE(SAT)}$$

would be required to turn on element 13. However, since column 1 is assumed shorted-out, element 11 in the same row would need only

$$V = -24 + V_{BE(SAT)}$$

to turn on. Thus, element 13 may never turn on with the column command transistor for column 1 shorted-out.

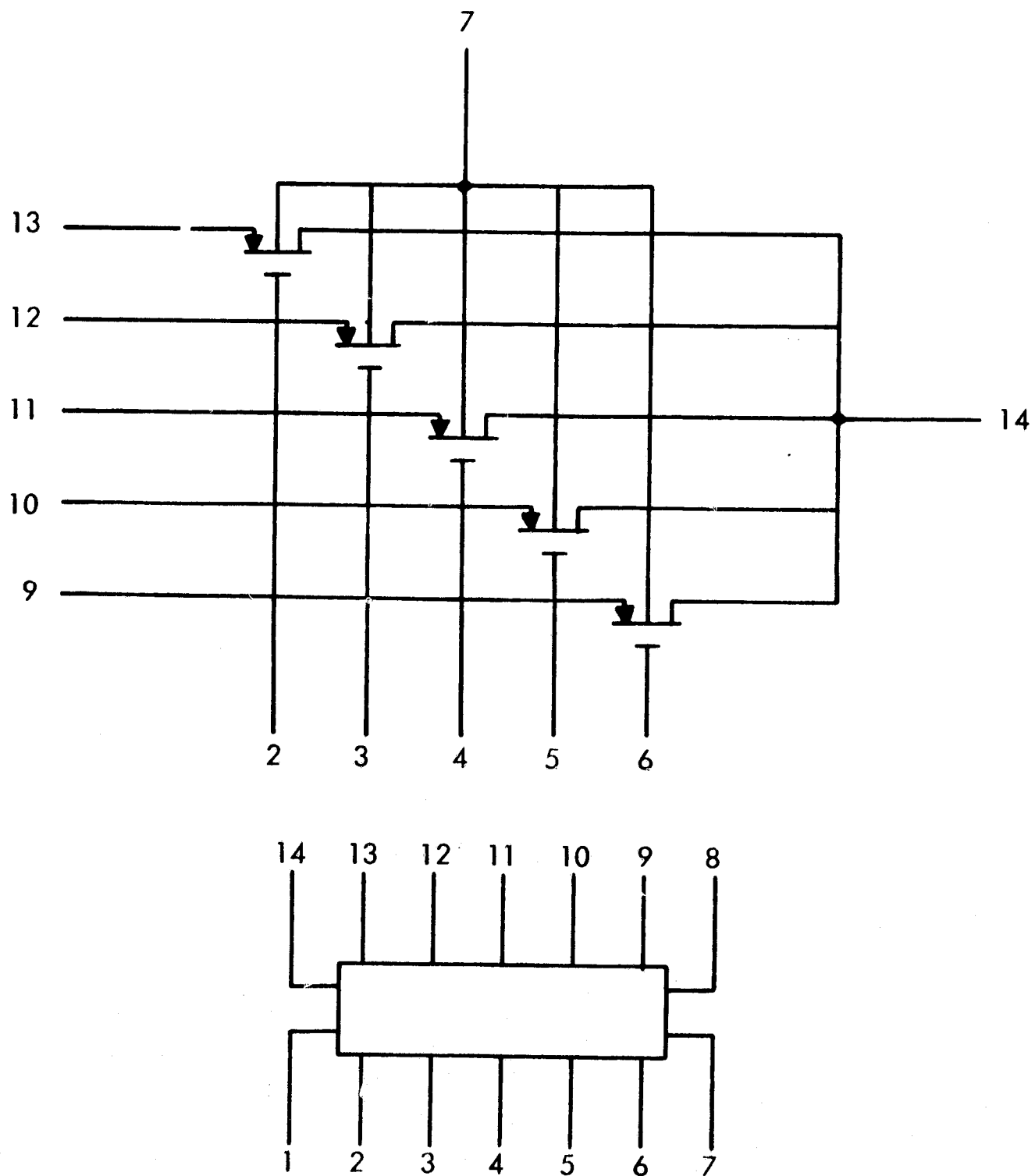


Figure 36. Fairchild MOS Gate, Schematic Diagram

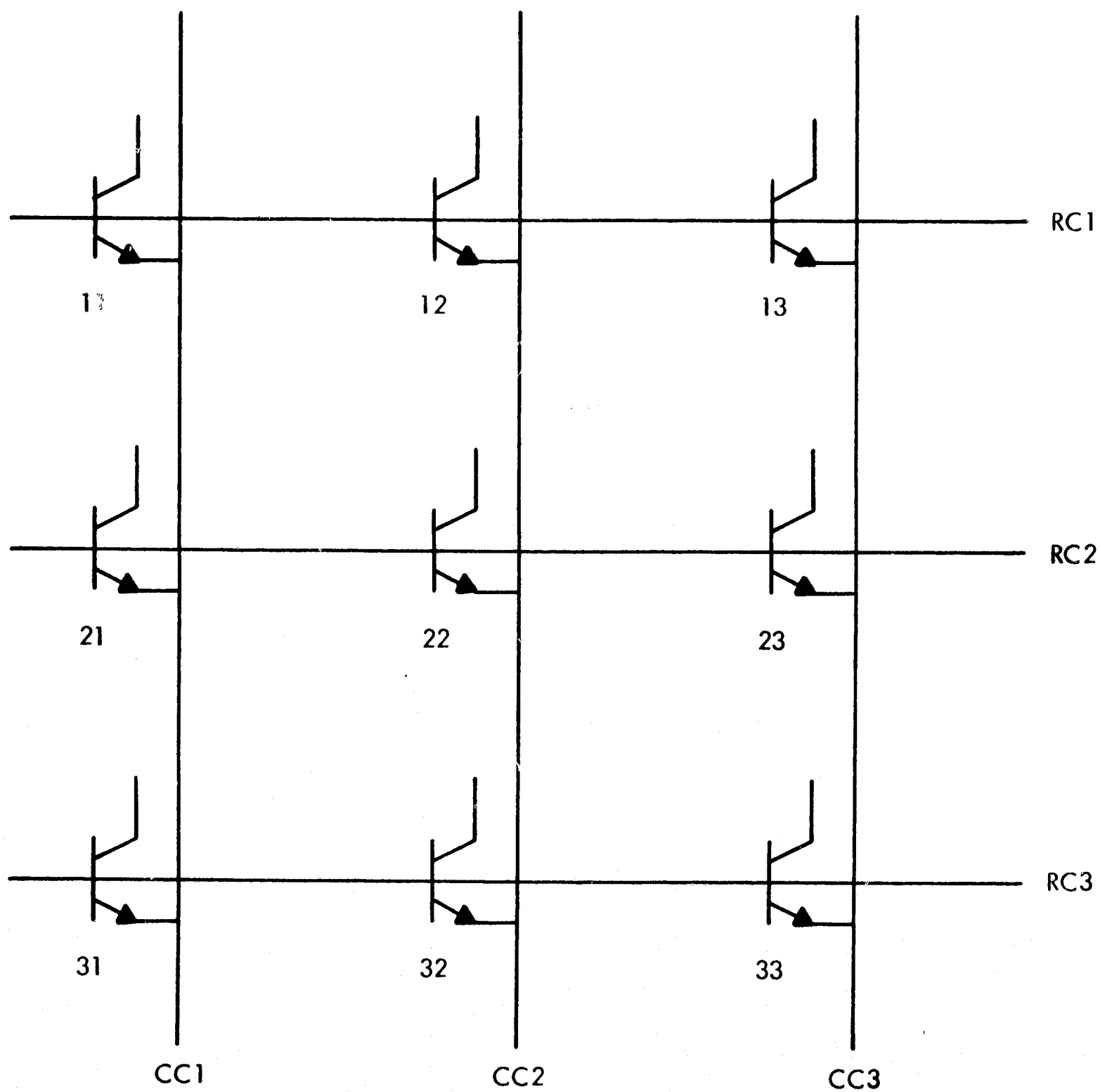


Figure 37. Row Command and Column Command Matrix, Simplified Schematic

The problem can be eliminated by an emitter resistor. Now the minimum base voltage for turn-on of element 13 with the same short would be

$$V = -24 + V_{CE(SAT)} + V_{BE(SAT)} + I_C R_E$$

The turn-on voltage for element 11 would then be

$$V = -24 + V_{BE(SAT)} + I_C R_E$$

The loss of $V_{CE(SAT)}$ would not be enough loss in voltage to prevent turn-on of element 13.

Notice that in the final matrix there is an emitter resistor for each gate driver. The reason for this configuration, rather than one resistor for each column line, is explained as follows. Consider the case with a single emitter resistor for an entire column line. Suppose the gate driver for element 13 has a base-emitter short. Then, although the column command transistor would supply the correct column bias voltage of -24 +5 volts through some resistance, the actual column line voltage would be -24 volts. If strobing for element 13, element 11 would have a much lower turn-on requirement because it would not have the emitter resistor voltage to overcome as would element 13. With an emitter resistor for each gate, both gates (11 and 13) would have emitter resistors to -24 volts if this particular fault occurs. Although element 13 would have a higher voltage to overcome than element 11 of $V_{CE(SAT)}$, it would not be enough to prevent turn-on of element 13.

b. Matrix Failure Analysis. Catastrophic failures in the matrix consist of various shorts in the gate driver. These failures are discussed below.

(1) Base-Emitter Short. A base-emitter short would connect the column command line to -24 volts through the shorted junction. This would set that column command line in a go state. The MOS attached to that particular gate driver would be permanently off. This short would lose only one channel and is the least effective short.

(2) Collector-Emitter Short. This short would supply the column bias voltage to the collector of the shorted gate driver. However, since the collectors of all gate drivers in the particular column are tied together through 30K ohms, this negative voltage would be felt at the MOS gates of all column members. Thus, all MOSFET gates in that column would be turned on, with the loss of eight channels.

(3) Collector-Base Short. This short would apply -24 volts to the collector of the shorted gate driver. Again, this would apply -24 volts to the common collector points, with the loss of eight channels. The collector-emitter and collector-base shorts are the worst failures. Both represent eight channel failures and a continual current drain on the power supply. The worst possible fault would be if the entire flat-pack shorted-out. Now the current would be limited by the external 3.9K-ohm resistor. This current would then be

$$I = (24 + 6) \text{ volts} / 3.9\text{K ohms} = 8.2 \text{ ma}$$

per 8-channel failure.

2.3.1.2.4 MULTIPLEXER REDUNDANCY. The basic multiplexer redundancy consists of one common matrix group that splits into the independent PCM 1 (A) and PCM 2 (B) systems. Each system has independent voltage supplies and timing circuitry. The different systems begin at the first stage of sequencing or at the column sequencer level as shown in figure 38. Outputs of the eight MOSFET gates of a common column of a common matrix are tied together. This common line feeds an A and a B column sequencer. In each system, outputs of the 16 column sequencers of a submatrix are tied together and pass through a third (final) sequencer. Prime channels merely pass through column sequencers. Thus, a subcommutated signal to the coder passes through three MOSFET gates and a prime signal passes through two MOSFET gates. The final multiplexer output to the coder is from one of eight gates; the four subcommutated final sequencers or the four prime column sequencers.

Column sequencers contain the same type circuitry as the column commands for the matrix. Each column NAND gate has five loads: one for the column PNP driver that drives the four submatrices and four for the four subcommutated column sequencers for that particular column. Two resistors limit current to the NPN gate driver (figure 39): (A) an external 3.9K ohm resistor in the emitter of the PNP driver, and (b) the 800-ohm emitter resistor in the NPN gate driver.

The +6-volt bias is applied to the MOS gates continuously, regardless of which system is on. However, the -24 volts are applied only to the column and final sequencers of the operating system. Voltages on the off system are clamped to PSC by the clamp circuit in the programmer. Again, each final sequencer has independent timing and driver circuitry.

2.3.1.2.5 MULTIPLEXER GENERAL PURPOSE AMPLIFIERS AND GATING CIRCUITRY. Information to the general purpose amplifiers (GPA's) is received through one of six sets of gates, as shown in figure 40 and listed below.

- a. Analog Information (from the coder)
- b. Digital Information (from within the multiplexer)
- c. Sync Word 63
- d. Sync Word 1
- e. Sync Word 2 and Subframe ID
- f. Time Code

Eight GPA's are required to accommodate the 8-bit per word format. Since the first bit of each word is a sync bit and is controlled by logic on the GPA inputs, seven bits of information are gated to the GPA's. Thus, each of the above commands controls seven MOSFET gates.

The GPA's are essentially level detectors that have the following response:

- a. 0 to -1 volt for a ZERO
- b. -5 to -10 volts for a ONE

The GPA's accept and convert the above voltages to one of two output levels for the shift register; +1.5 volts for a ZERO or -7 volts for a ONE. Figure 41 is an output versus input voltage

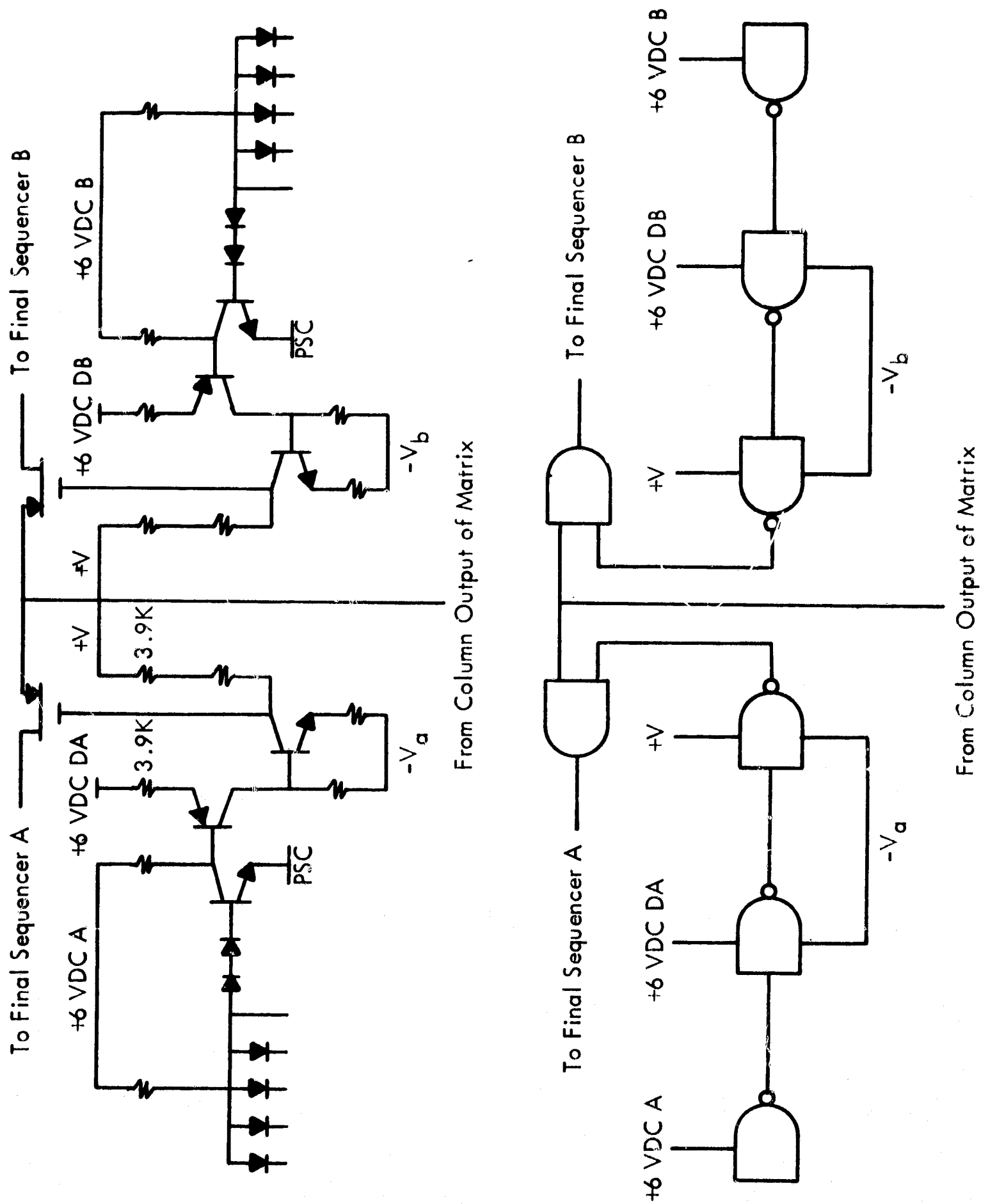


Figure 38. Multiplexer Redundancy, Schematic and Logic Diagrams

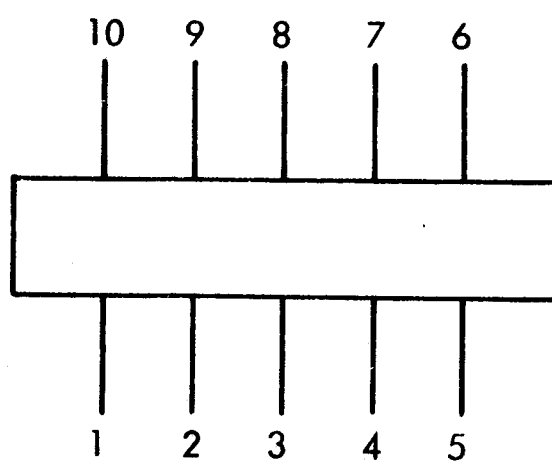
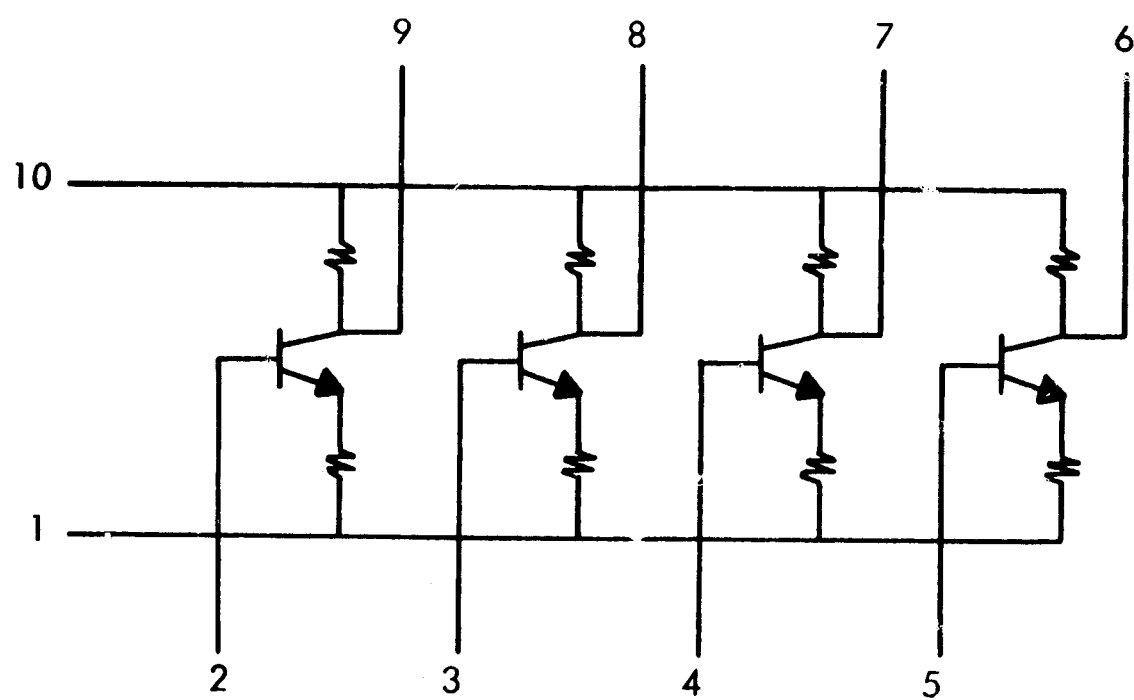


Figure 39. Sprague NPN Driver, Schematic Diagram

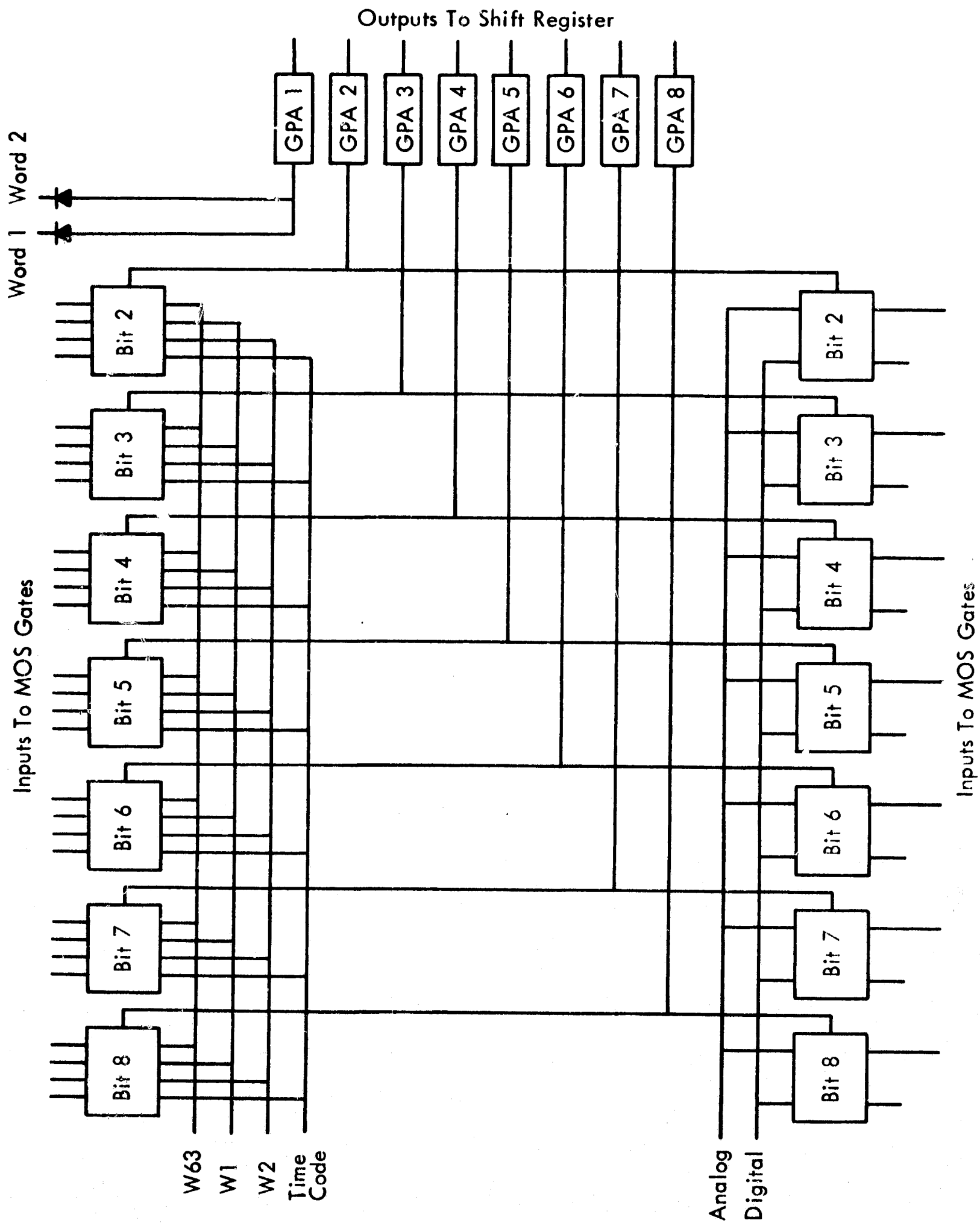
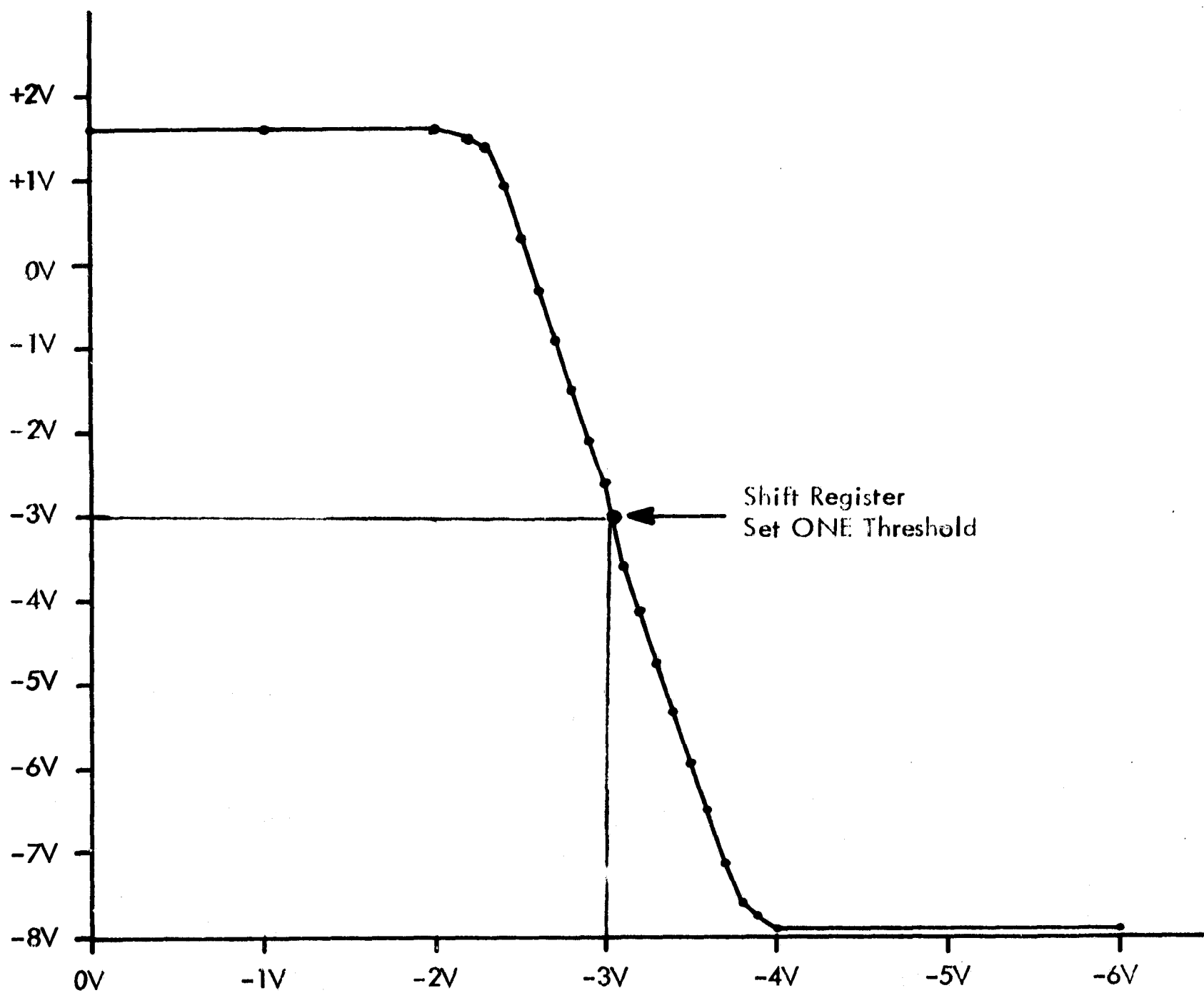


Figure 40. General Purpose Amplifier Input Gates



NOTE: The actual ONE/ZERO detect level over all conditions is -3.0 ± 0.75 volts.

Figure 41. General Purpose Amplifier, Output Versus Input Response Curve

response curve of the GPA in this particular configuration. According to the specification, there can be an indeterminate input in the range of -1 to -5 volts. Consequently, the GPA switching level is in the middle of this indeterminate range, which is -3 volts. Inputs to the MOSFET gates for the different sync bits are hard-wired to PSC for a ZERO or to -6 volts through 1.8K ohms for a ONE.

Figure 42 is a logic diagram of the GPA gating circuitry that produces the above commands. Each logic element is an inverter operating between PSC and +6 volts. Consider the case of an analog signal. The coder overvoltage circuit output is low at PSC. Thus, the first inverter in the line is high at +6 volts. The inverter that provides the ANALOG output is in a go condition. The second inverter is low; thus, the inverter that provides the digital detection pulse (DDP) output is inhibited with the output high. When the coder detects an overvoltage condition, the ANALOG line is inhibited and the DDP line is placed in a go condition. The DDP output is used by the multiplexer and the programmer to strobe data into the three storage flip-flops used to store the 10 bit coders' 3 LSB's.

The inverter labeled Time Code Gate is an OR gate with a normally high output that drops if words 4, 12, 19, 23, 31, or 36 occur during subframe 1. Gate levels of W1, W2, and W63 are compatible with the Time Code Gate level and are normally high. Outputs from these four gates are applied to an OR gate. The gate labeled Time Code-Sync OR Gate is the output of this network and the output is normally high. If any one of the above times occur, the outputs DDP and ANALOG outputs are automatically inhibited.

An additional output is shown on this diagram and is labeled ADP for analog detection pulse, as opposed to the ANALOG output. The ADP output is merely the ANALOG output gated with the 500-cps inverted signal and is used by the programmer to reset the three coder storage flip-flops to all ONE's. The ADP output is gated with the 500-cps inverted signal to prevent reset of the coder flip-flops before strobe time to the output shift register. The flip-flops must not be reset until after strobe time.

Figure 43 is a schematic diagram of the GPA. Notice the 2.2-megohm resistor across the input signal to the GPA's. Assume that one of the analog transducers read an overvoltage condition and provided an output voltage below -6.4 volts. The coder would then indicate an overvoltage and, during the second strobe, would open the digital final sequencer line to the GPA's. However, since that particular channel would have no input MOSFET gates on the digital line, the voltage to the GPA would be some indeterminate floating voltage. Therefore, resistors were added to read out ONE's to simulate the overvoltage condition on the analog channel input. The GPA negative voltage is duty-cycled to save power.

Consider how the resistors affect normal operation. According to the specification, digital source impedance must be less than 50K ohms. A digital signal passes through the digital transducer impedance, three MOSFET gates, and a limiting 3.9K ohm resistor. This is a total input impedance of:

$$R = 50K + 3 \times (2.2K) + 3.9K = 61K$$

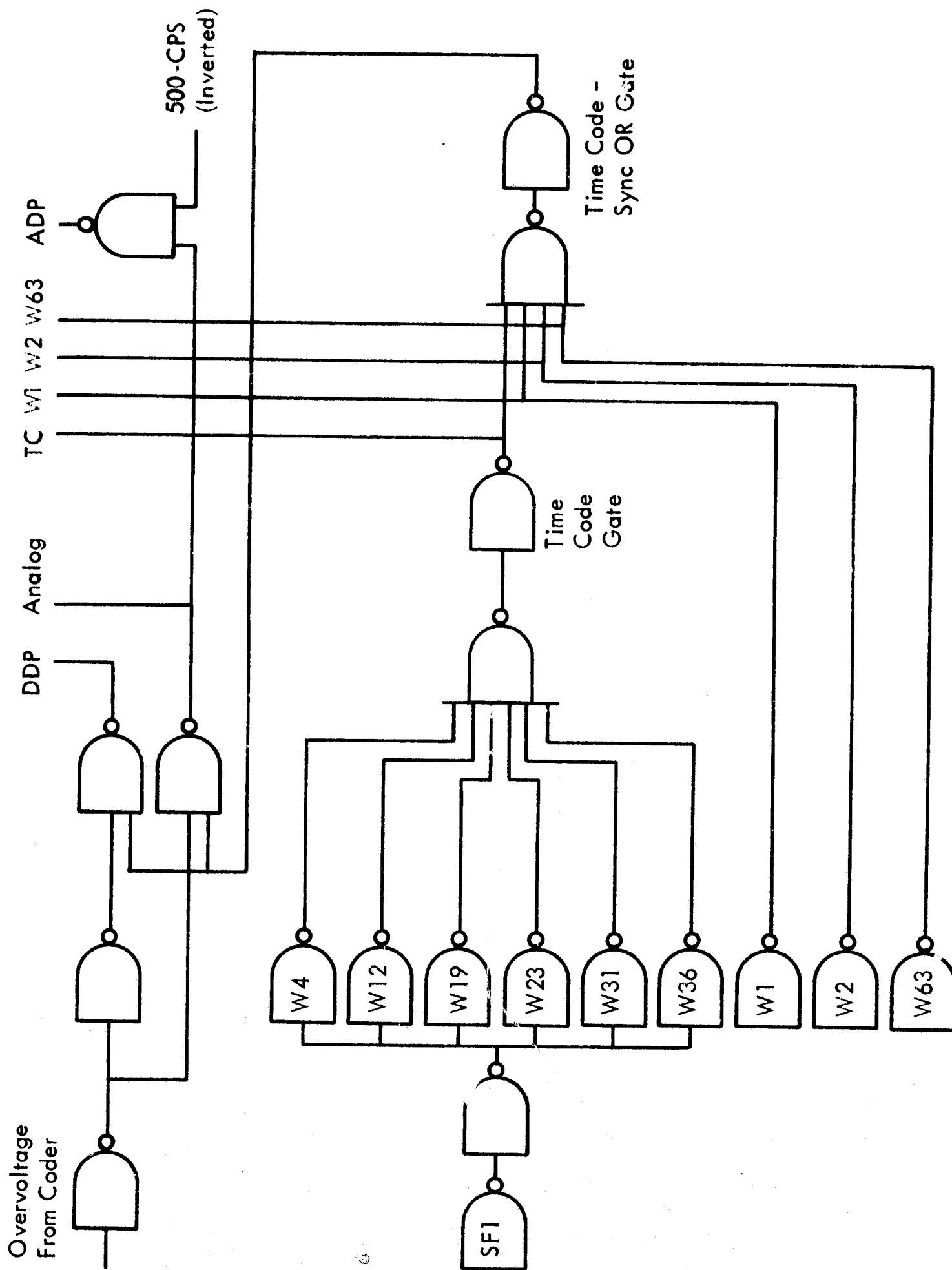


Figure 42. General Purpose Amplifier Gating Circuitry, Logic Diagram

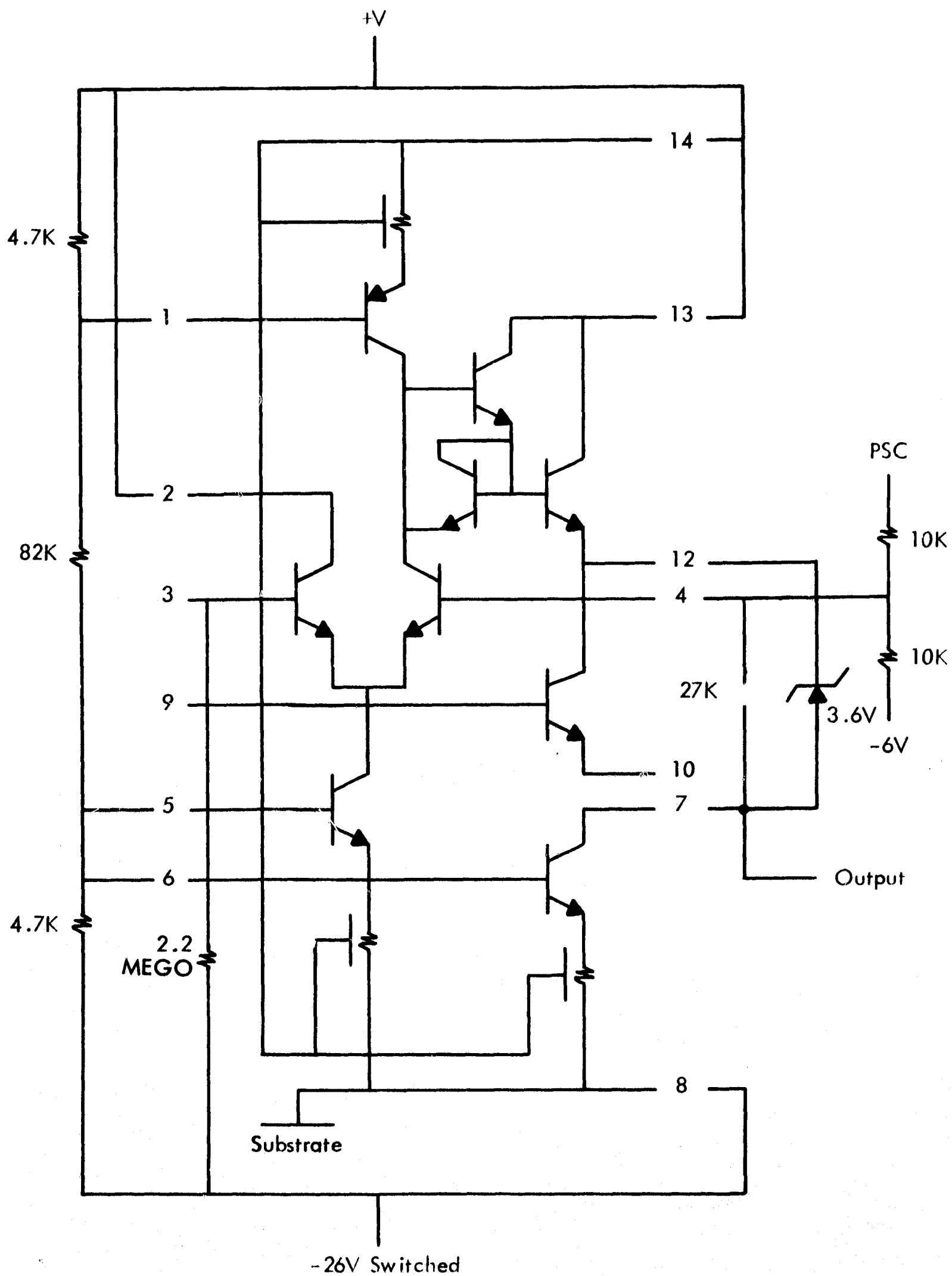


Figure 43. General Purpose Amplifier, Schematic Diagram

where 2.2K is the maximum MOSFET turn-on impedance. Since the 2.2-megohm resistors are returned to a -24-volt dc level, the input voltage to the GPA with the input at 0 volts, is -1.38 volts (worst case) which still produces a ZERO at the GPA output. The strobe to the shift register occurs during the middle of bit 8 of the word being shifted out and about 90 microseconds after the start of the delayed duty-cycle pulse.

2.3.1.2.6 DIGITAL MULTIPLEXER. Figure 44 is a schematic diagram of the digital multiplexer. A single MOSFET gate is attached to each gate driver in the matrix for analog channels. However, seven additional MOSFET gates are jumpered to the particular gate driver for digital channels. Just as analog signals from the multiplexer to the coder are sequenced, digital signals from the multiplexer to the output GPA's are sequenced. An analog signal to the coder passes through three MOSFET gates (maximum); a digital signal to the output GPA's passes through three MOSFET gates. Analog signals are sequenced on a column basis; whereas, digital signals are sequenced on a submatrix basis. An analog sequencer consists of one MOSFET gate; a digital sequencer consists of seven MOSFET gates in parallel that open at the same time.

Ten digital sequencers open at the following times:

- a. Prime Matrix, Prime Columns 1 and 2
- b. Submatrix A1
- c. Submatrix B1
- d. Submatrix A2
- e. Submatrix B2
- f. Prime Matrix, Prime Columns 3 and 4
- g. Submatrix A3
- h. Submatrix B3
- i. Submatrix A4
- j. Submatrix B4

Since each digital sequencer consists of seven MOSFET gates, this represents a total of 70 MOSFET gates in the digital sequencers second tier.

Each submatrix board has five analog channels jumpered with overvoltages (-15 volts) to indicate digital channel time slots in the format. Since there are eight submatrix boards and seven bits per channel, this represents a total of 280 subcommutated digital channels. Nine positions on the prime matrix board are jumpered with overvoltage. This represents a total of 63 prime digital channels.

2.3.1.2.7 MULTIPLEXER FAULT VOLTAGE PROTECTION. According to the specification, one possible fault condition on the multiplexer inputs is -24 volts. Since the MOSFET gate breakdown voltage is approximately 30 volts, additional circuitry had to be used because the body of the MOSFET is already returned to +6 vdc. The safety factor had to be installed before the column sequencer to retain the minimum 8-channel loss. The point between the series resistor and the column sequencer is zenered to approximately -20 volts as shown in figure 45. During normal operation (0 to -6.4 volts), the diode is always back biased and never interferes with operation. However, if the input voltage should go to -35 volts and break down the input

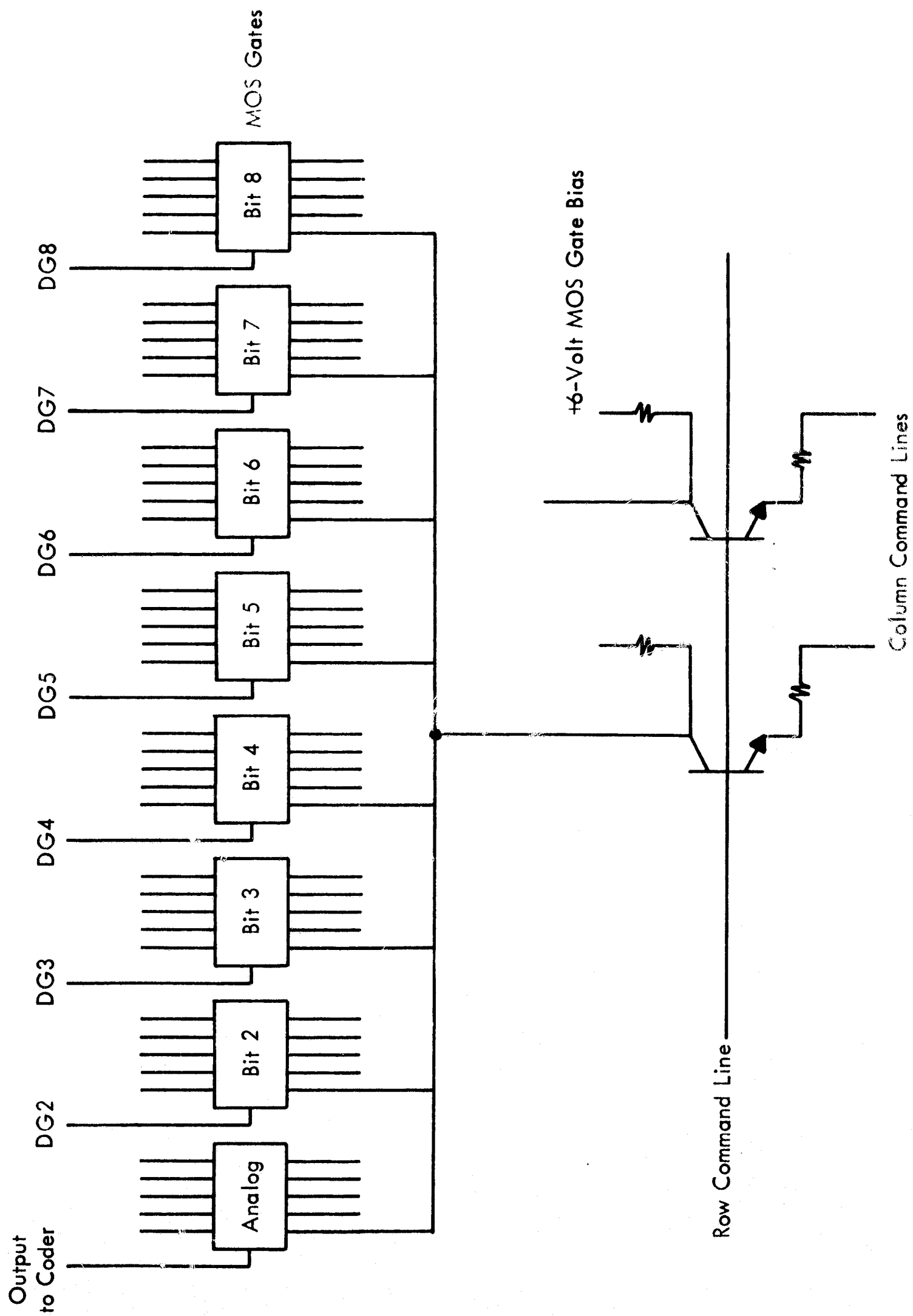
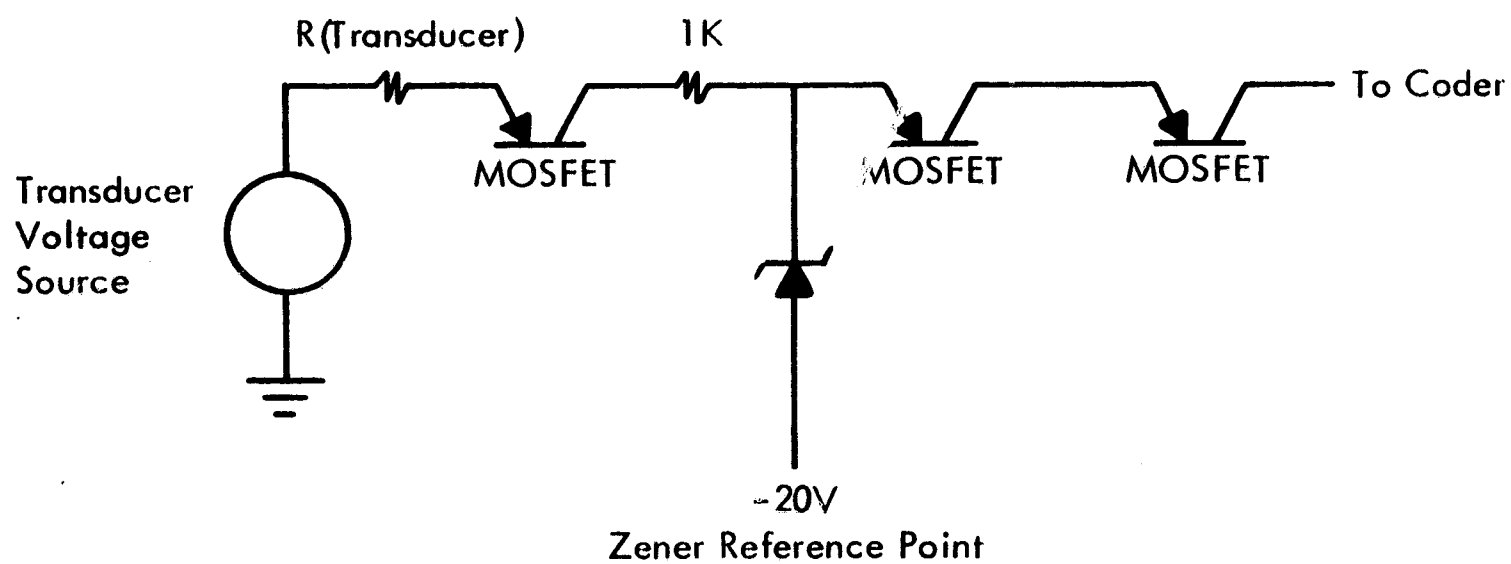


Figure 44. Digital Multiplexer, Schematic Diagram



NOTE: For digital channels the 1K resistor is replaced by 3.9K and the circuit output is connected to the GPA input.

Figure 45. Fault Protection Circuitry, Schematic Diagram

MOSFET gate, the input to the column sequencer would be clamped at -20 volts and the column sequencer MOSFET would only have 26 volts across it and would not be affected. This voltage clamp runs to a stud-mounted zener diode (in the TME) that is capable of dissipating up to 10 watts. Note that when this fault condition occurs, the shorted transducer and not the PCM furnishes the power.

According to the specification, the back current through the source must not exceed 1 microampere during sampling time. However, this figure is actually too high for the 10-bit capability. The total impedance from transducer voltage source to column sequencer is

$$R = R_{\text{transducer}} + R_{\text{MOS}} + 1K$$

$$R = 3.3K + 2.2K + 1K = 6.5K$$

With 1-microampere leakage, the voltage developed at the column sequencer input would be:

$$V = I_{\text{leakage}} R = (1 \text{ microampere}) \times (6.5K \text{ ohms}) = 6.5 \text{ millivolts}$$

Note that one bit of a 10-bit code with this range equals 6.25 millivolts, which is already a bit error. The leakage current should be such that a small percentage of the bit voltage is developed with the leakage current. The following table illustrates how this current leakage specification for the diodes was chosen:

Table 11. Diode Current Leakage

Temperature (°C)	Current (nA)
25	10
37	20
49	40
61	80
73	100

Since the upper temperature for Nimbus breadboard was +65°C, assume that leakage current at this temperature was 100 nA and a worst case impedance of 7K ohms. Now the voltage drop for error would be

$$V = (0.1 \text{ microampere}) \times (7K \text{ ohms}) = 0.7 \text{ millivolts}$$

This voltage drop is much less than the voltage per bit.

The digital channels contain a similar overvoltage protection circuit except that the resistor value is 3.9K ohms and there are 5 digital channels per clamp circuit.

2.3.1.3 POWER SUPPLY. The PCM unit contains two power supply modules; power supply 1 is used with PCM 1, and power supply 2 is used with PCM 2. Each power supply consists of an input voltage regulator, a dc chopper and saturable transformer, and diode rectifiers with output filtering for the various output dc voltages. A simplified block diagram of the power supply is shown in figure 46.

2.3.1.3.1 GENERAL. Figure 47 is a logic diagram of the power supply (PCM 1 or PCM 2). The power supplies are controlled by a relay in the TME such that only one power supply is operating at a time. The normal line voltage is -24.5 volts, ± 2 percent. However, series regulator Q2 is used so that proper PCM operation is possible with input voltages ranging from -19 to -35 volts (established at the lower end by measuring data from the system during the final demonstration test). The -35-volt limit must not be exceeded because of possible damage to the series regulator. The normal line current for all input operating voltages is approximately 65 milliamperes.

Negative voltage operating power is applied to the voltage regulator and the chopper networks through diode CR2. Diode CR2 is a reverse-polarity protection diode that provides circuit protection if input polarities are reversed. A reference voltage through diode CR3 is applied to one side of differential amplifier Q3. The other side of the differential amplifier receives a sampling of the output voltage taken from the high side of series regulator Q2. Differential amplifier Q3 compares the sample voltage and reference voltage and generates an error output when the input voltage is not -24.5 vdc. Error amplifier Q1 amplifies the error voltage and routes a correction voltage to series regulator Q2. The error correction circuit maintains a nearly constant voltage between the chopper input and the high side of series regulator Q2.

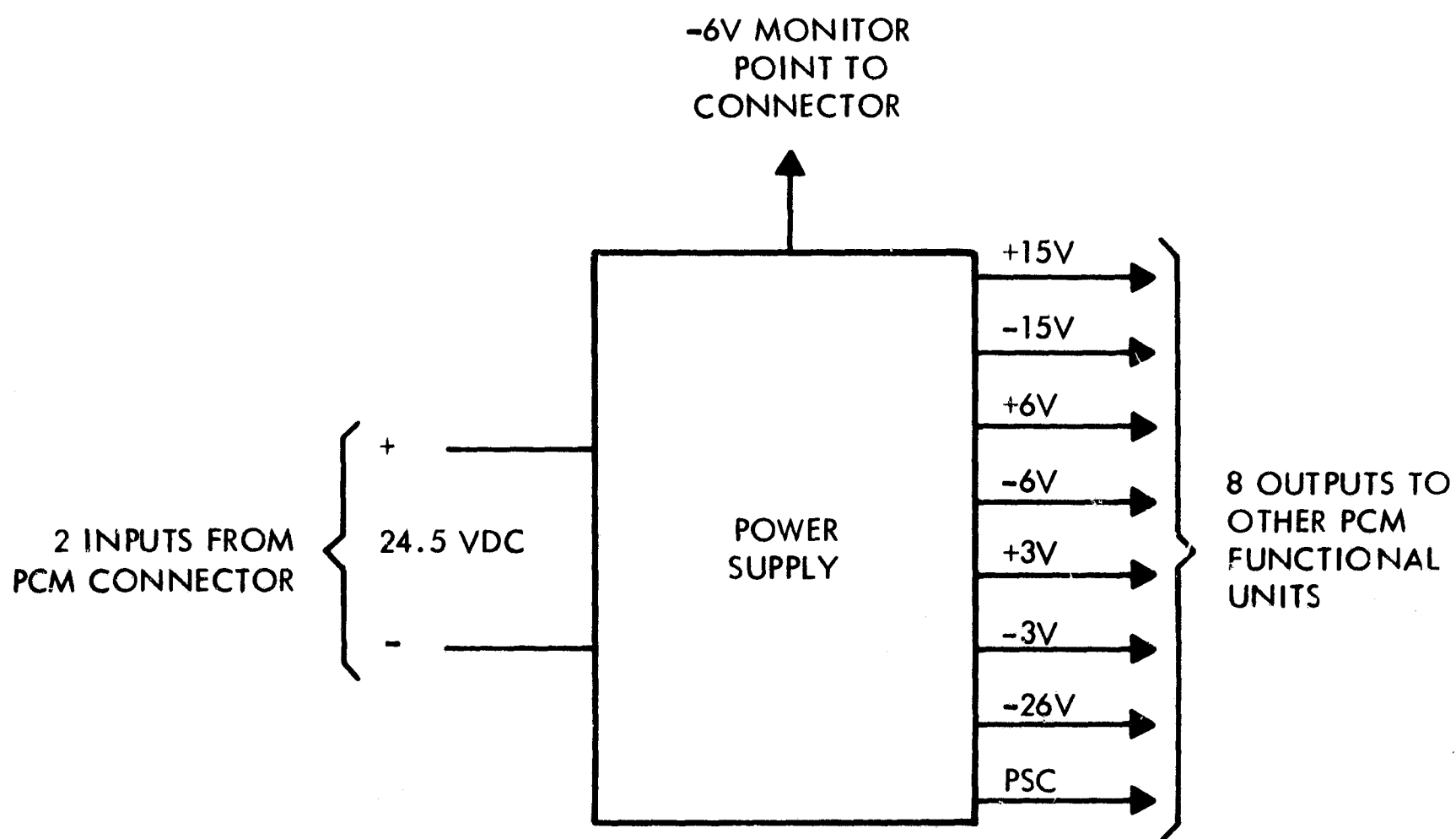
Input voltage to the chopper is converted to ac power voltages that are subsequently rectified and filtered to produce isolated dc outputs. An electrostatic shield between the primary and secondary of transformer T1 prevents noise feedback. The RFI filter is an LC filter that prevents the 50-kc primary chopper frequency from being returned to the power source.

Measurements have determined that the 50-kc noise is 4 milliamperes, peak-to-peak, which would develop only 0.4 millivolts across the specified 0.1-ohm maximum source impedance. The pulsed multiplexer duty cycle noise is approximately 20 milliamperes, peak-to-peak, which develops 2 millivolts across the 0.1-ohm power source impedance.

The measured turn on transient is 3 amperes peak, within one microsecond and returns to a nominal 2-ampere average within an additional microsecond. The nominal 2-ampere pulse width is 20 microseconds followed by an exponential decay to the nominal 65-milliampere steady state direct current (refer to figure 48).

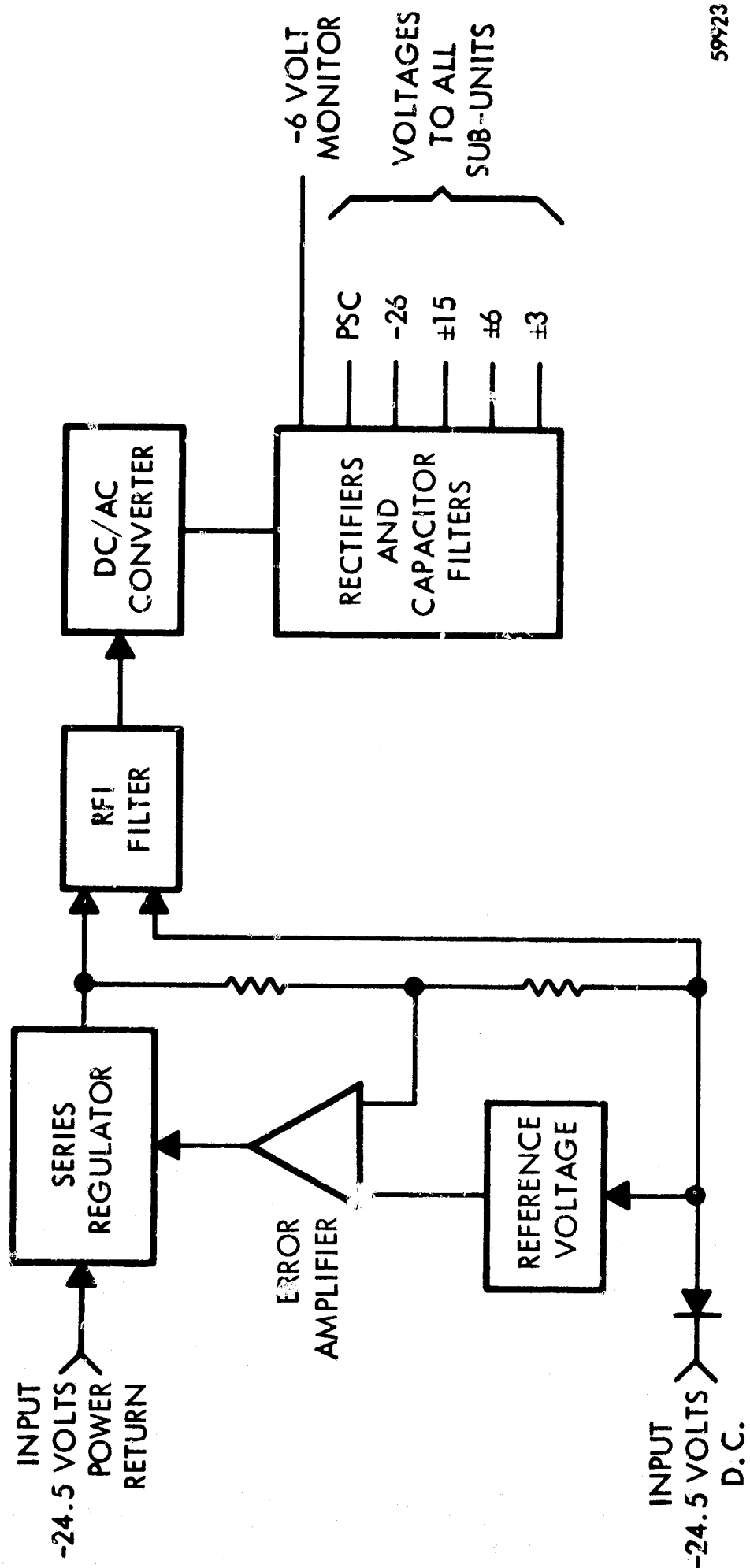
The power supply provides ± 15 volts, ± 6 volts, ± 3 volts, and -26 volts to the PCM electronics. In addition, a -6 volt monitor point is available at the connector for use as an analog channel indicating which power supply is on. The monitor point is protected against an accidental short to PSC or -24.5 volts.

2.3.1.3.2 DETAILED DESCRIPTION. Refer to the power supply logic diagram, figure 47, and schematic diagram, figure I-17. Input voltages of -23 to -35 volts are accepted by the



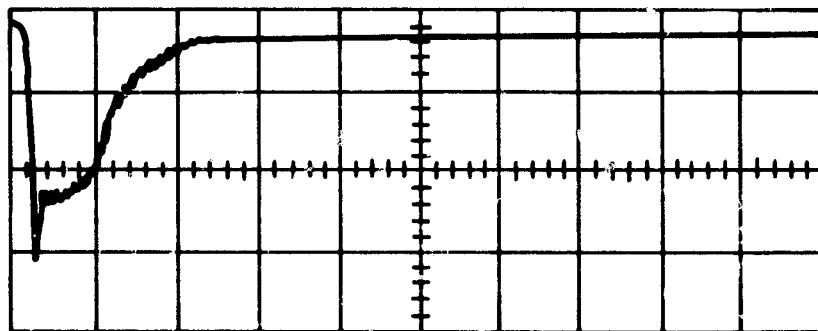
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Figure 46. Power Supply, Simplified Block Diagram



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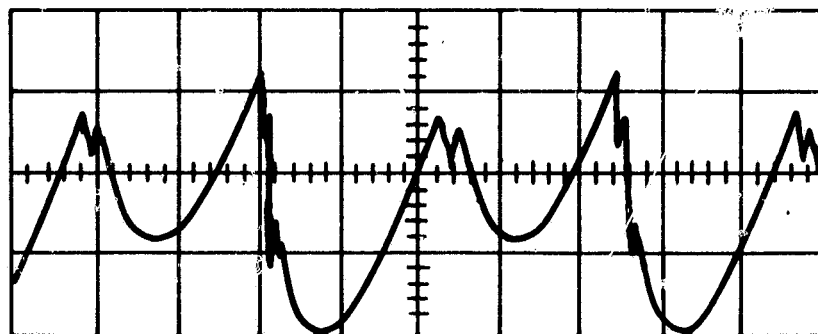
Figure 47. Power Supply, Logic Diagram



VERTICAL SCALE
HORIZONTAL SCALE

1A/CM
20 μ s/CM

A



VERTICAL SCALE
HORIZONTAL SCALE

1mA/CM
5 μ s/CM

B

55993

Figure 48. Power Supply Turn-On Surge and Feedback Ripple

input regulator and the regulator provides a nearly constant voltage to the dc-to-dc converter. This voltage is then stepped up or stepped down to supply the required voltage magnitudes and polarities to the PCM system. The converter runs at approximately 50 kilocycles.

The -24.5 ± 0.5 volt dc input is applied to the input terminals. Diode CR2 protects the supply if the external power is connected with the polarity reversed. The RFI filter, L1, L2, C1 and C2, blocks line ripple and short duration transients and prevents switching transients generated by switching of the converter from appearing on the input line.

The voltage regulator consists of a comparison amplifier (Q3), a reference voltage Zener diode (CR3), a DC amplifier (Q1), and a control element (Q2).

The comparison amplifier is formed by transistor Q3 and resistors R1 through R8. Transistor Q3 is a matched transistor used for self-compensation with temperature variation. The transistor also has high current gain characteristics to minimize its loading on the base networks. The function of this amplifier is to compare the output voltage with the reference voltage and to generate an error voltage that is proportional to the difference. A sample of the output voltage is applied to the base of Q3B for comparison with the reference voltage to the base of Q3A. If the regulator output voltage tends to increase due to line variation or temperature change, the voltage at the base of Q3B increases. The collector current of Q3A then decreases, causing the base-to-emitter voltage of transistor Q1 to decrease with resultant decreased current flow in the collector of Q1. Since the collector current of transistor Q1 provides base drive for transistor Q2, the output voltage is decreased by the amount required to correct for the line variation or temperature change. Diode CR1 is included in the circuit to ensure initial operation of the regulator at power turn-on.

The reference voltage at the base of Q3A is generated by the precision network formed by resistors R2, R5 through R8 and diode CR3. Diode CR3 is a temperature-compensated Zener diode, having approximately 750 ohms dynamic impedance and operating at 100 microamperes. Because the reference voltage network is within the feedback loop and consists of precision components having extremely good temperature characteristics, the Zener bias current remains constant with temperature and line variations.

The dc amplifier, transistor Q1, amplifies the difference voltage from the comparison element to develop required drive to the control element. The dc amplifier design is not critical because it is within a strong feedback loop. The amplifier must, however, have sufficient gain to furnish base current to transistor Q2, while still retaining circuit stability. The current gain should be large enough so that the base drive is only a portion of the collector current through Q3A.

The control element, transistor Q2, receives the correction voltage from the dc amplifier and makes the required corrections to maintain a constant output voltage.

The dc-dc converter is a standard design (except, perhaps, for the starting circuit), which utilizes the regulator output voltage to provide the necessary step-up, step-down functions to obtain the desired output voltage levels. Initial starting is assured by the asymmetrical start circuit formed by windings 4-5, 6-7, and 8-9, resistors R9 through R12, and diodes CR4

and CR19. At power turn-on, base current is supplied through resistor R9 to transistor Q4. (At power turn-on diode CR4 is back-biased, but diode CR19 is forward-biased and part of the starting current is routed through diode CR19. Diode CR19, resistor R10, and winding 6-7 is used after the converter starts to keep CR4 forward-biased when transistor Q4 is non-conducting.) Thus, transistor Q4 is initially turned on and current flows through winding 2-1 into transistor Q4. This changing current induces a voltage into the other windings. Induced voltages in windings 4-5, 6-7, and 8-9 are in a direction to turn off transistor Q5, back-bias diode CR19, and increase the base current of transistor Q4, respectively. The collector current of transistor Q4 increases until the core approaches saturation. As the core becomes saturated (L approaching zero), the collector current increases rapidly and is limited only by the transistor characteristics and the resistance in the collector circuit. When the core is saturated, the induced voltage in the windings is zero. The lack of sufficient base drive begins to turn off transistor Q4 with a resultant decrease in collector current. This collapsing collector current induces a voltage of the opposite polarity to bias transistor Q4 off and transistor Q5 on.

If, at power turn-on, the collapsing collector current of transistor Q4 does not induce sufficient voltage to turn on transistor Q5, transistor Q4 will again turn on and function as a blocking oscillator until the induced voltage across winding 4-5 is sufficient to turn on transistor Q5 and start the converter.

Full wave rectifiers and capacitor filters form the output circuitry. For isolation purposes, the output voltages are obtained from separate windings.

2.3.1.4 PROGRAMMER.

2.3.1.4.1 GENERAL. The PCM unit utilizes two redundant programmers with each programmer consisting of three modules, making a total of six programmer modules. Some functions implemented in the programmer modules are not considered a functional part of the programmer; however, these functions are included in the programmer description.

The programmer modules are designated module numbers 1, 2, and 3, and contain the following functional circuits:

Module No. 1

- 8:1 Bit Counter
- Multiplexer Timing Circuits
- 15-Microsecond Strobe Command Generator
- Coder Command Circuits

Module No. 2

- Time Code Circuits
- 1/16-PPS Pulse Generator
- 1 CPS Reset Circuits
- 1/16-PPS Pulse Generator Monitor Circuit

Module No. 3

Temperature Monitor Circuit
Multiplexer Clamp Circuit
Test Set Command Circuit
Subframe ID Buffers
3-Bit Coder Buffer Storage

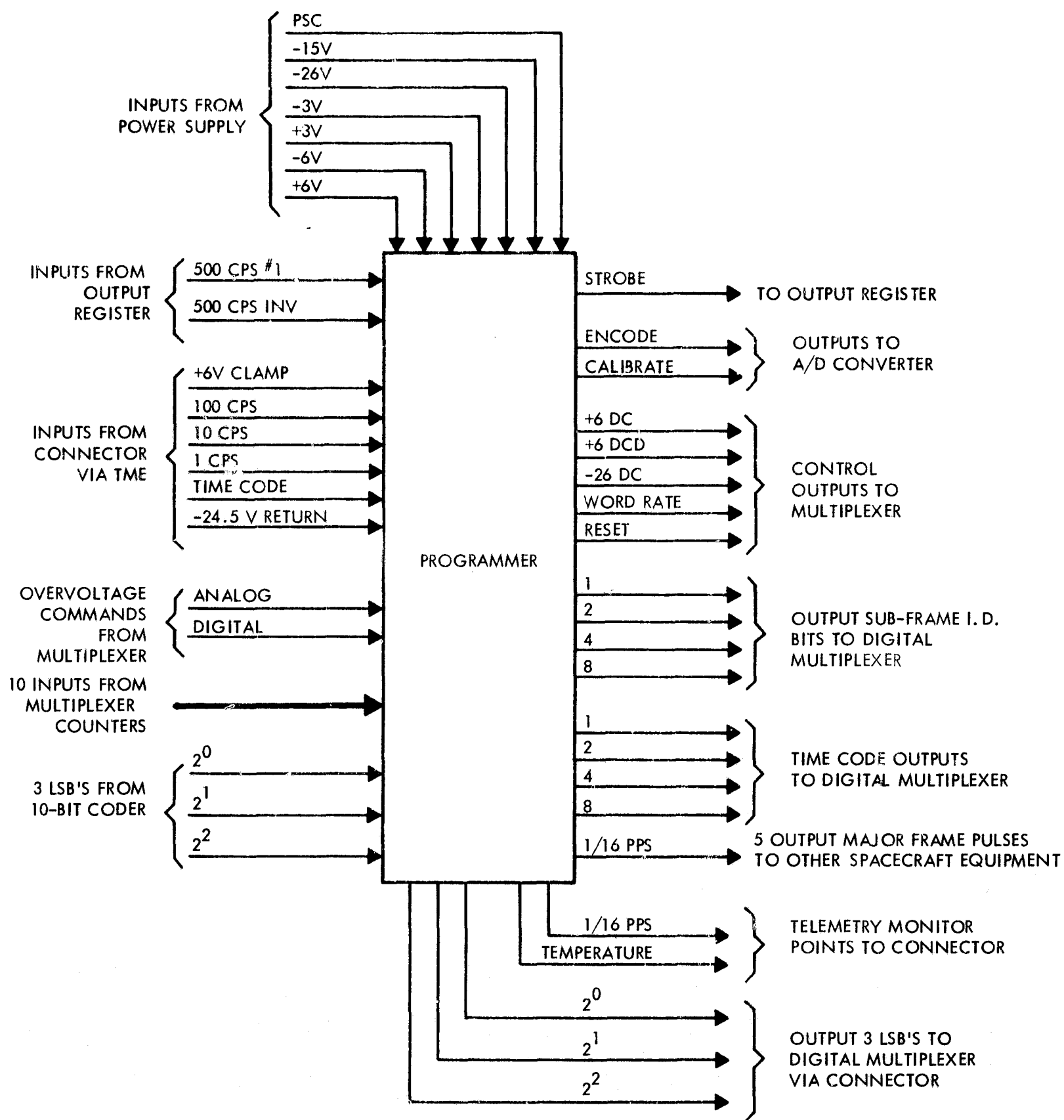
2.3.1.4.2 BLOCK DIAGRAM DESCRIPTION. Refer to the programmer block diagram, figure 49, and logic diagram, figure 50.

a. Programmer Module No. 1

(1) 8:1 Bit Counter. The 8:1 bit counter is a conventional 3-stage binary counter that counts at a 500-cps bit rate. The Nimbus C clock 500 cps (CY500) is routed through a buffer amplifier in the output register module to the counter, making the counter synchronous with the clock. (Refer to the time code control timing diagram, figure 51.) The three counter stages are externally reset at a 1-cps rate by the Nimbus C clock 1 cps (CY1A) or the detected word number 62.5 from the word counter. The external 1-cps clock provides for proper insertion of the external time code into the format. If the reset circuit fails, the counter is reset by word 62.5, ensuring that the output format always contains a subframe of 62.5 words per second. If, however, the 1-cps clock reset circuit fails, the time code data is lost. The outputs of the 8:1 bit rate counter control gates that generate commands to the coder, multiplexer, and generate read-in strobes to the output register.

(2) Multiplexer Timing Circuits. The multiplexer commands are duty-cycled to conserve power, and the basic multiplexer circuits operate on two commands (refer to multiplexer, coder, and output register timing diagram, figure 52). One command is a 260-microsecond signal that presets the multiplexer circuits for proper operation. The analog data to the coder or the digital data to the digital operational amplifiers (GPA) does not appear until approximately 30 microseconds later (when the 200 microsecond command appears). There are two 260-microsecond pulses; one which sets up the analog channel gates and a second to set up the digital channel gates. There are two 200-microsecond commands; one to gate analog data to the coder and the second to gate digital data from either the coder or the digital multiplexer through the operational amplifiers to the output register (when the strobe pulse appears). Normally saturated RC-coupled amplifiers (half-shots) provide controlled pulse widths and delay times to develop precise command signals. The output commands are routed to the multiplexer clamp circuit.

(3) 15-Microsecond Strobe Command Generator. The strobe command generator produces a 15-microsecond pulse to strobe the output of the operational amplifiers (multiplexer output board No. 2) into the 8-stage output shift register. (Refer to the timing diagram, figure 52.) The strobe command is delayed approximately 100 microseconds from the leading edge of the 200-microsecond operational amplifier operate command. Thus, the strobe command is optimally located in the center of the 200-microsecond gate. The strobe command also gates the first three least significant bits of all 10-bit coder data into buffer storage, so that any analog channel that is followed by a digital time slot can develop ten bits of resolution.



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Figure 49. Programmer, Simplified Block Diagram



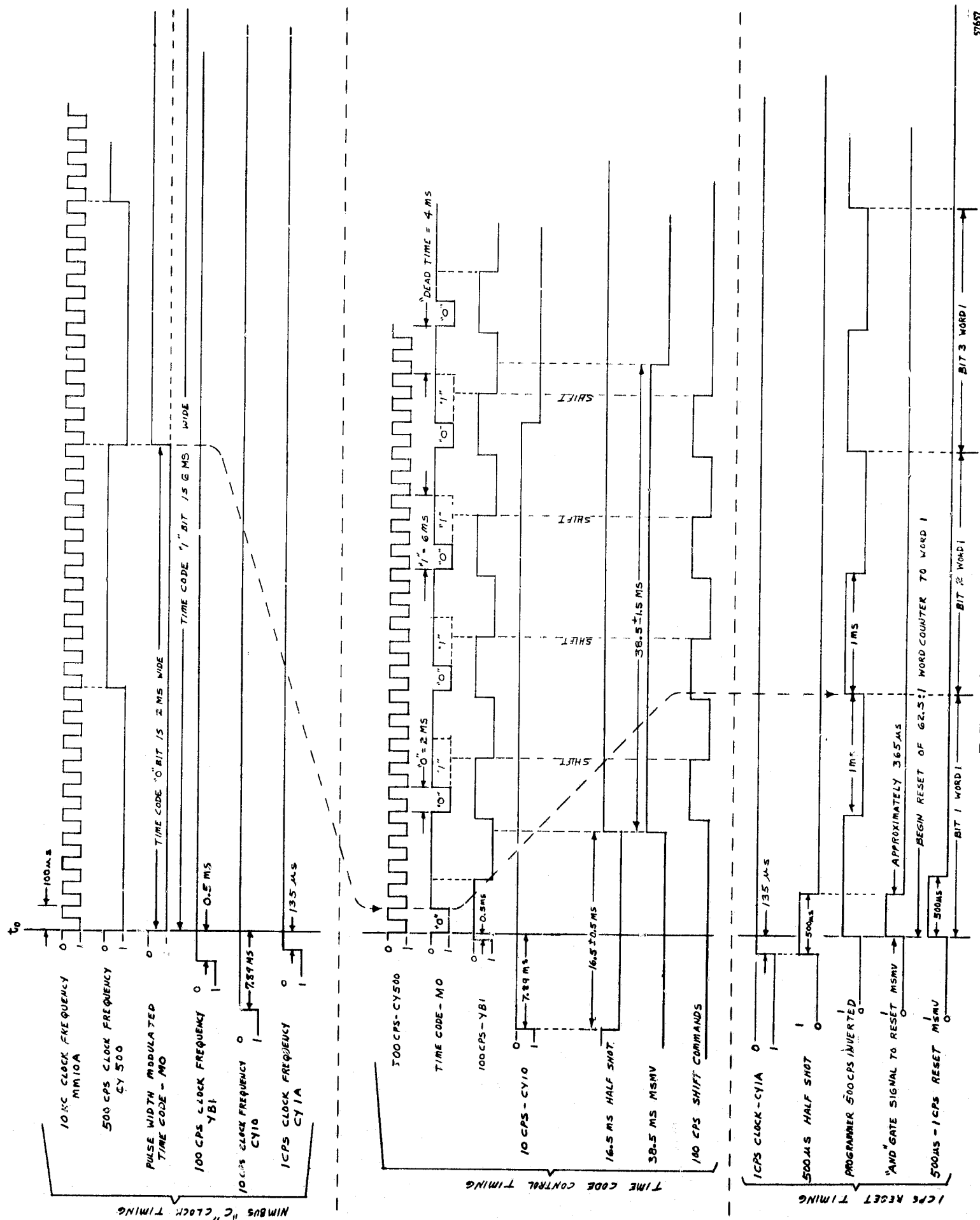


Figure 51. Time Code Control, Timing Diagram



Figure 52. Multiplexer, Decoder, and Output Register, Timing Diagram

The strobe command is developed during the last half of bit time 2 of every word and strobes analog or digital words into the output register. The timing sequence of each cycle is as follows: (1) the analog multiplexer gate is opened and the analog voltage is routed to the coder, (2) the coder 10-bit ramp operates for a maximum of 2.2 milliseconds and the input voltage is digitized, (3) the digital gates are operated to connect the output of the coder or a digital channel to the operational amplifiers, and (4) the command strobe loads the 8-bit parallel output from the amplifiers into the output shift register.

(4) Coder Command Circuits. The programmer develops encode commands and calibrate commands to the coder. (Refer to the timing diagram, figure 52.) The encode command occurs during bit time 1 of every word and commands the coder to sample the analog multiplexer PAM bus. The calibrate commands occur during bit times 3, 5, and 7 of every word to command the coder to check itself against a fixed full scale reference voltage. Both of these commands are of approximately 200 microseconds duration.

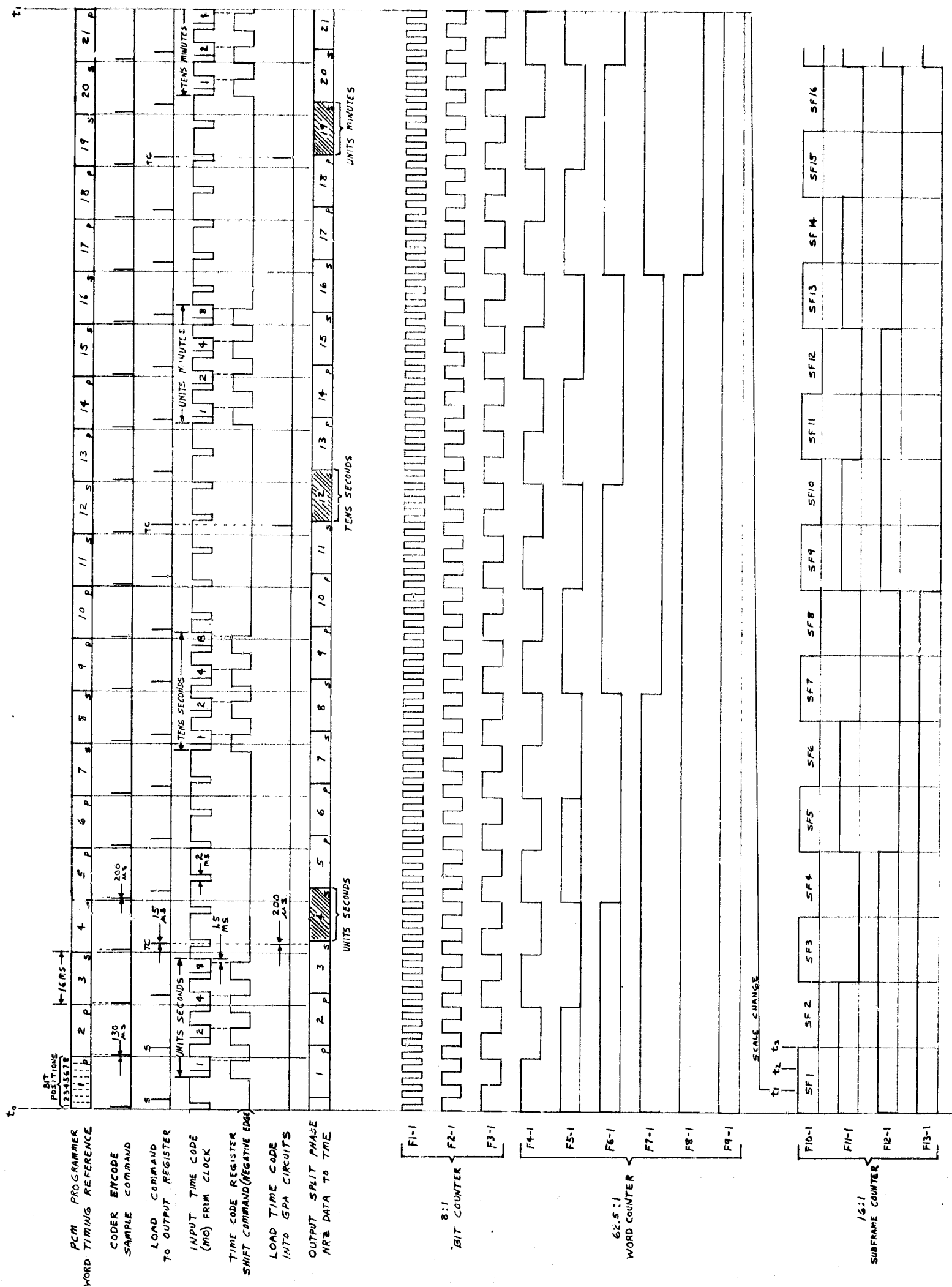
b. Programmer Module No. 2

(1) Time Code Circuits. The time code data to the PCM unit is received in serial form from the Nimbus C clock. (Refer to timing diagrams, figures 51 and 53.) The time code bit rate is 100 cps and the PCM bit rate is 500 cps. Because these bit rates are not compatible, the clock also furnishes a 10-cps signal and a 100-cps signal to properly position the four bits of time code in a 4-bit shift register. The four outputs from the shift register are routed directly through digital multiplexer channel gates so that the time code data is placed in the output format as six words of four bits each during subframe 1 only. The last three bits of all time code words are hard-wired to produce ZERO's.

The 10-cps signal, CY10, is applied to a precision half-shot ($\pm 3\%$), which produces a 16.5 millisecond time delay. The delayed pulse is then routed to a second precision half-shot ($\pm 3\%$) to generate a 38.5-millisecond gate pulse that allows only four cycles of the 100-cps signal (YB1) to shift time code data (MO) into the shift register. The digital multiplexer strobe pulse loads this information into the output register before the next four shift pulses load the next four bits of time code into the time code shift register.

The precision half-shots contain polycarbonate timing capacitors and "select at test" 1 percent resistors. This type of circuit is used in place of the conventional 10:1 counter arrangement that was used in the early part of the Nimbus Study Program to reduce the parts count by approximately one half. Thus, reliability has been increased at the cost of flexibility (the new circuit operates properly only with the Nimbus C clock).

(2) 1/16 PPS Pulse Generator. A special pulse generator circuit is provided with five 1-K ohm output resistors. The pulse generator circuit is capable of driving up to five external experiments of 10K ohms each. The generated pulse is the major frame rate pulse that occurs at the beginning of every major frame with respect to the input multiplexer. (The pulse occurs 2 bit times or 4 milliseconds prior to the beginning of the major frame with respect to the output split phase data.) The pulse output is negative-going 0 volts to -5 ± 1 volt with pulse width of 250 ± 50 microseconds. A special output is provided to operate the 1/16-pps monitor circuit described in subparagraph 2.3.1.4.2b(4).



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Figure 53. Time Code Storage and Readout, Timing Diagram (Sheet 1 of 3)

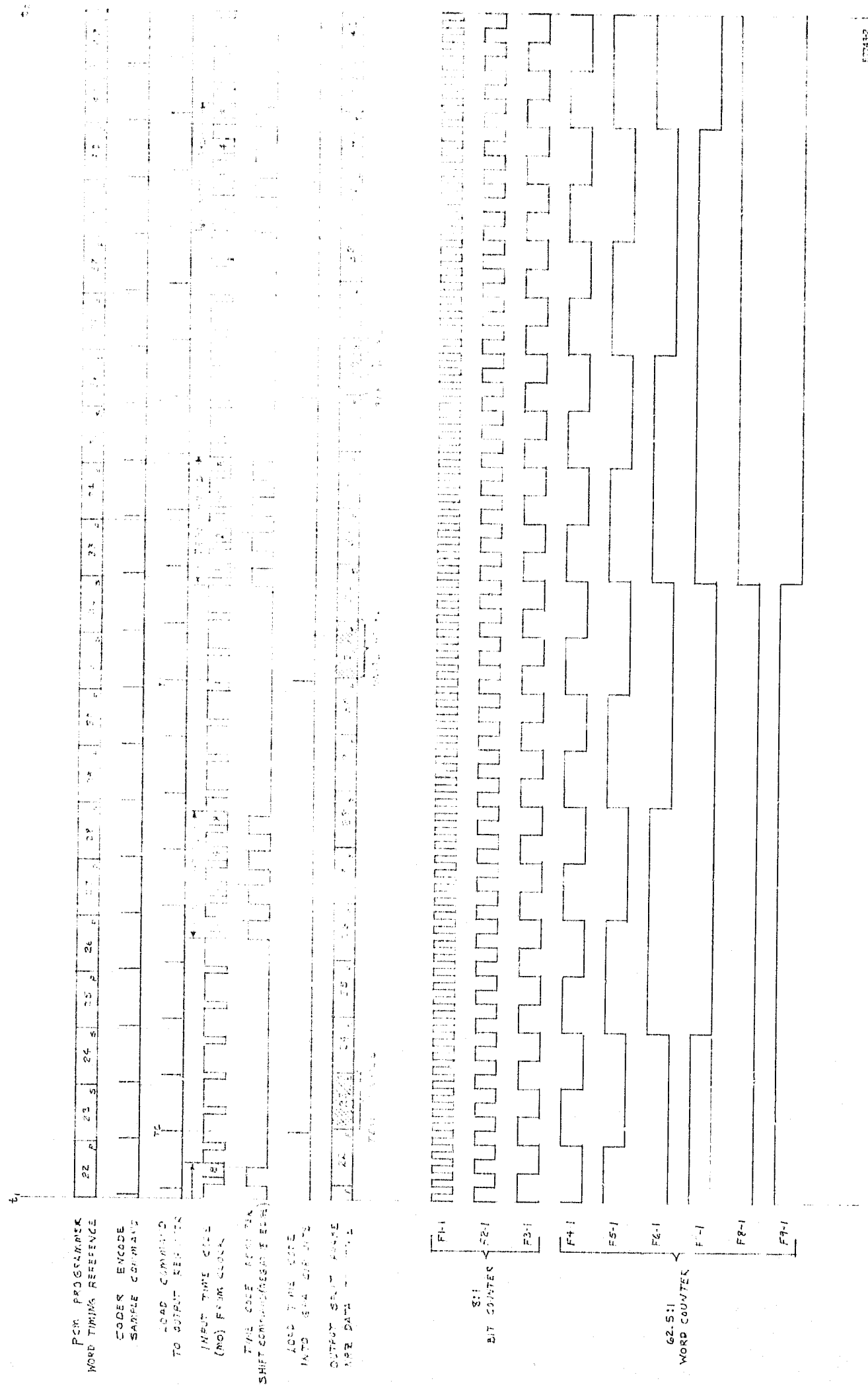
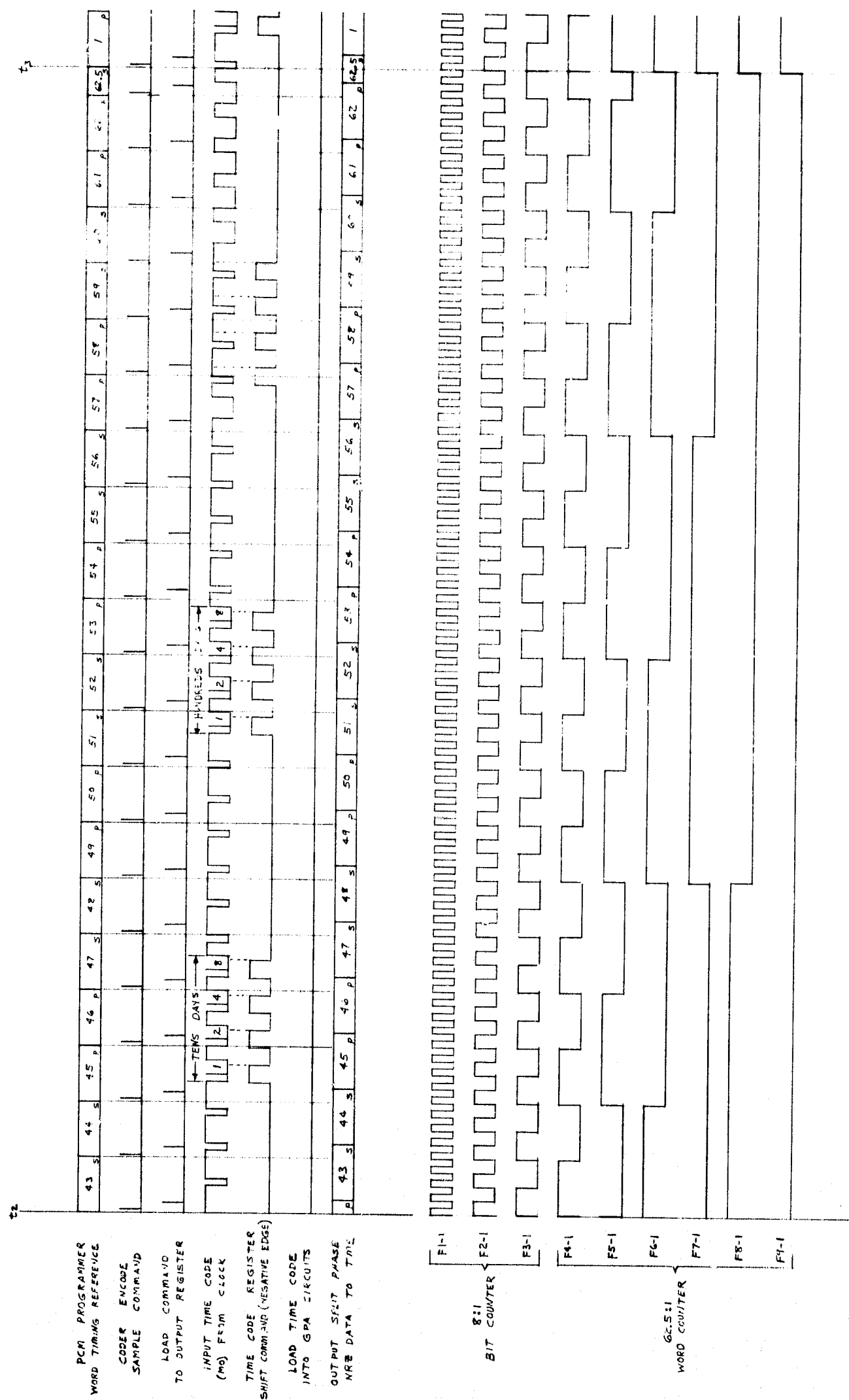


Figure 53. Time Code Storage and Readout, Timing Diagram (Sheet 2 of 3)



(3) 1-CPS Reset Circuits. Refer to timing diagrams, figures 51 and 53. The PCM word counter is a conventional 6-stage binary counter that would normally count 64:1. However, to synchronize the PCM to the Nimbus clock so that time code data is properly inserted into the PCM output format, the 64:1 counter is reset during the middle of word time 63, and, the 64:1 counter becomes a 62.5:1 counter. Because bit rate is 500 cps and there are 8 bits-per-word, there will be 500/8, or 62.5 words-per-second. To properly synchronize the counter, an external 1-cps reset from the clock is necessary. An internal 1-cps pulse is also generated so that the subframe length is not changed if the external 1-cps signal is lost. However, time code will no longer be properly inserted into the PCM format if the external 1-cps signal is lost.

The reset pulse generator is a 500-microsecond monostable multivibrator with an output driver to reset the 62.5:1 word counter and the 8:1 bit counter. The monostable multivibrator is driven from two AND gates and an OR gate. One AND gate detects the center of word time 63 for internal reset. The second AND gate detects the buffered 1-cps external signal (CY1A) which is ANDed with the 500-cps buffered bit rate to properly phase the external 1-cps reset. An output from the 1-cps buffer amplifier also resets the 1/16-pps monitor flip-flop as described in the following subparagraph.

(4) 1/16-PPS Pulse Generator Monitor Circuit. The 1/16-pps monitor flip-flop is set during the time of subframe 1 only, and can insert a ONE into any digital channel that occurs in subframe 1. The flip-flop is reset by the 1-cps external signal during subframes 2 through 16 such that a ZERO can be inserted into any digital channel that occurs during subframes 2 through 16. Thus, the 1/16-pps pulse generator monitor flip-flop provides a ONE and a ZERO monitor level for each major frame. An output resistor and series diode are provided to protect the circuit from an external short to either PSC or -24.5 volts.

c. Programmer Module No. 3

(1) Temperature Monitor Circuit. The temperature monitor circuit consists of a 1-percent resistance voltage divider with a thermistor in parallel with the resistor that is connected to PSC. The thermistor will provide temperature indications only after supply voltage is applied from an external source. The thermistor is of rod type construction so that internal current flow does not affect the temperature reading. The monitor output can be routed to any analog channel, with temperature changes of -10°C to $+65^{\circ}\text{C}$ resulting in voltage changes of -4.5 volts to -0.45 volts. Using a 7-bit coder with a voltage range of 0 volts to -6.4 volts full scale, the circuit has an overall accuracy of $\pm 2^{\circ}\text{C}$ with additional error introduced as the thermistor supply voltage varies. If resolution of $\pm 1^{\circ}\text{C}$ were to be required, the voltage source would have to be held to within $\pm 0.1\%$ and the coder resolution would have to be increased to at least 9 bits.

(2) Multiplexer Clamp Circuit. The multiplexer clamp circuit is necessary because two sets of drivers (block redundant) control the single input analog and digital multiplexer gates. Each set of drivers is controlled by a separate programming and timing circuit and a separate power supply. However, there are failures that could occur in the multiplexer that would allow the unused drivers to incorrectly command the multiplexer if the unused drivers

were left floating. For example, if failures occurred in PCM 1, and PCM 2 were then commanded to operate, the then unused circuits in PCM 1 could cause failure of PCM 2. To prevent this type of failure, the PCM multiplexer control circuits that are on clamp the off circuits to within approximately 0.5 volts of PSC. These clamps are either diode or saturated transistor circuits that control the +6-volt line, -26-volt line, +6-volt 260-microsecond duty cycle pulse line, +6-volt 200-microsecond delayed duty cycle pulse line, and the -26-volt, 260-microsecond duty cycle pulse line.

In the event of several failures, the multiplexer could draw extremely large pulse currents from the power supply and could introduce additional noise into the PCM through the power supply lines. To minimize this noise, the multiplexer clamp circuits provide very large RC filters so that pulse currents required by the multiplexer are supplied by large capacitors and are decoupled from the power supply. When switching from one PCM to the other, these large capacitors must be nearly discharged before the clamping action occurs, thereby preventing extremely large discharge currents from flowing through the clamping transistors and diodes. To ensure that overlap does not occur (both clamp circuits on for an instant of time) and to ensure that no line losses occur, a relay in the TME box is used to turn on the clamp circuit of the unused PCM. The same relay also applies power to the PCM that is in use. When the relay contact applies +6-volt dc power to the clamp circuit, the large filter capacitors for the +6-volt line and the -26-volt line are allowed to discharge through a resistance before the final clamp is applied. The discharge time is controlled by a 47-microfarad tantalum capacitor that provides a delay of approximately one second to discharge the filters before clamping the lines to within ± 0.5 volts of PSC.

(3) Test Set Command Circuit. In the manual checkout mode, the test set will readily check any one channel or word at a time; however, to automatically check out all analog channels against upper and lower limits, the test set must be commanded as to which words are analog and which are digital. In the Nimbus study system test set, the analog words are automatically compared until a test set command pulse is generated. The command pulse is generated just prior to a digital channel readout and prevents comparison of the next word against the analog limit switches. Comparison of a digital channel and the analog limit switches normally produces an error indication because it is unlikely that the seven digital bilevel channels will be selected with the same bit combination as the 7-bit analog output from the coder. The digital channels could be selected to compare with the limit switches, but that method is not practical.

The circuit presently in use produces a 0-volt to +6-volt 260-microsecond pulse that occurs one millisecond prior to the next output word when that word is from a digital channel. Sync words 1, 2, and 62.5 and the 6 time code words do not apply an overvoltage to the coder, as these words do not go through the same final sequencer as the digital channels. Therefore, no pulses are generated for these time slots; however, the test set contains AND gates for generating inhibit signals during these times to prevent comparison with the analog limit switches.

(4) Subframe ID Buffers. The level shifting buffer amplifiers are required to place the binary code status of the 16:1 subframe counter into the output format. The outputs

from the counter (F10 through F13) switch from 0 volts for a ZERO to +6 volts for a ONE, but the digital multiplexer requires 0 volts for a ZERO and -6 volts for a ONE. The code for subframe 1 is 0000 (binary zero), while the code for subframe 16 is 1111 (binary 15). The 4-bit code is routed to the digital multiplexer and gated to appear in the output format as the last four bits of word 2 in every subframe. This code changes once per second and recycles every 16 seconds.

(5) 3-Bit Coder Buffer Storage. (Refer to figure 52.) The Nimbus B coder has a resolution of 10 bits. Since it is a ramp coder, the output code circuit of the coder is a 10-stage counter. The Nimbus output format words consist of 7 bits of data plus one sync bit. Because the standard analog channels require a coding resolution of only 1 part in 128, only 7 bits (the last 7 stages of the 10-stage counter) of the coder are hard-wired to the digital multiplexer for gating into the output register. The remaining 3 least significant bits provide a maximum of 10 bits of resolution (1 part in 1024), but they can be inserted only during the next word time. Thus, a 10-bit analog word will have the 7 most significant bits in the first word and the 3 least significant bits in the second word. The system is normally wired such that all analog words are 7 bits, with greater resolution achieved by patching the remaining bits (bits 8, 9, and 10) back into the system as digital channel inputs. Therefore, the use of analog words requiring resolution greater than 7 bits will decrease the input digital channel capability. To provide maximum flexibility, a 3-stage storage buffer was added to the programmer and the coder is allowed to code all analog words to 10 bits of accuracy. The last seven bits are placed in the format, and the first three bits are stored until the next time slot. Because additional bits must be connected through digital channels, only an analog channel that precedes a digital time slot can be selected to have 8, 9, or 10 bits of accuracy. The remaining bits in the second word (bits 5, 6, 7, and 8) can still be used as digital channels.

The 3-bit storage register is reset to the ONE state when an overvoltage command is generated by the coder. This overvoltage command is developed when the coder has coded an input voltage equal to, or greater than, full-scale voltage of -6.4 volts. The coder uses full-scale measurement to determine whether input data is analog or digital and then produces the appropriate command to switch the output to the operational amplifiers and output register from the coder (when coder measures less than full scale) or from the digital multiplexer (when coder measures greater than full scale). The full scale voltage applied to the coder for digital channels requires analog input gates for all output prime and subcommutated data time slots. The digital channel matrix has been added to an already complete analog matrix, and the digital gates (7 bits per word) are operated in parallel with an analog gate. Thus, every digital channel has an analog gate to which an overvoltage signal (-15 volts dc) is hard-wired and, when the coder measures this voltage, a full scale command is generated to gate data from the digital multiplexer. When full-scale voltage on an analog channel is measured, the coder also gates data from the digital multiplexer. During analog time slots, however, the digital channel gates are not opened and an effective open circuit to the operational amplifiers results in a digital word containing all ONE bits. Thus, the proper data is gated, even though it is developed from an incorrect source.

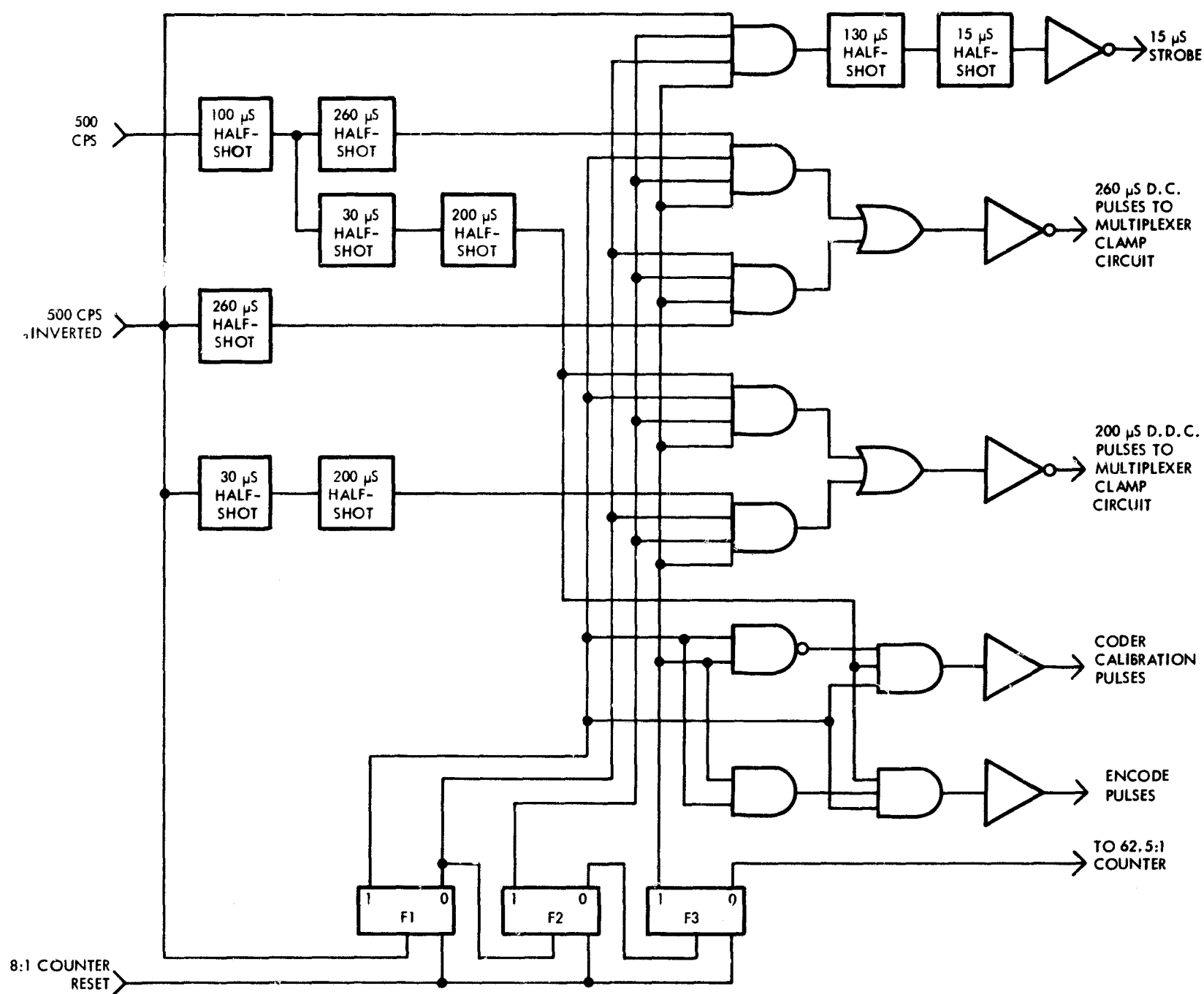
If an input analog channel measures full-scale voltage while programmed for 10 bits of resolution, the three least significant bits must be read out during the next time slot. Because of the command timing, and the overvoltage function of the coder, the three programmer storage flip-flops are reset to the ONE state for the conditions described above. The three flip-flops are then set to the ZERO state by the AND condition of a ZERO output from the coder and the 15-microsecond strobe command to the output register.

2.3.1.4.3 DETAILED DESCRIPTION.

a. Programmer Module No. 1. Refer to the programmer module No. 1 logic diagram, figure 54, and schematic diagram, figure I-18. Basic units of programmer module No. 1 are the 15-microsecond strobe generator, the duty cycle and delayed duty cycle pulse circuits, the coder command circuits, the 8:1 counter, and the timing half-shots and gates.

The 15-microsecond strobe generator circuit consists basically of two half-shots and an inverter formed by transistors Q1 through Q4. Transistors Q1 and Q2 form a 130-microsecond delay half-shot. A positive pulse at the base of transistor Q1 causes the transistor to saturate and discharge capacitor C2 through R3 and Q1. The time constant of R3 and C2 is set for 130 microseconds. As C2 discharges through R3 and Q1, normally saturated transistor Q2 is turned off. A positive 130-microsecond pulse is thus developed at the collector of transistor Q2. While Q2 is off, capacitor C3 charges through resistor R4, diode CR1, and the base-emitter junction of transistor Q3. When transistor Q2 turns on, capacitor C3 discharges through resistor R5 and turns off normally on transistor Q3. Capacitor C3 and resistor R5 are selected to hold Q3 off for 15 microseconds. When transistor Q3 turns off, transistor Q4 turns on and functions as an inverter.

Seven half-shots with associated diode gating circuits develop coder commands and duty cycle pulses for the multiplexer. These half-shots are similar in operation to those described in the preceding paragraph. A positive pulse at the base of transistor Q5 triggers the first series of half-shots. The first half-shot circuit has a pulse width of 100 microseconds as determined by resistor R14 and capacitor C5. The output of the first half-shot is positive-going pulse at the collector of transistor Q6. Transistor Q6 serves two purposes in that it is the output transistor of the 100-microsecond half-shot and the input transistor of the 260- and 30-microsecond half-shots. The trailing edge of the 100-microsecond pulse at transistor Q6 triggers both half-shots. The pulse width of the 260-microsecond half-shot is determined by resistors R84 and R16 and capacitor C6. The positive pulse output is taken from the collector of Q7. The pulse width of the 30-microsecond half-shot is determined by resistor R24 and capacitor C7 and the positive pulse output is taken from the collector of Q12. Transistor Q12 also serves two purposes in that it is the output transistor of the 30-microsecond half-shot and the input transistor of the 200-microsecond half-shot. The trailing edge of the 30-microsecond pulse at Q12 triggers the 200-microsecond half-shot. The pulse width of the 200-microsecond half-shot is determined by resistors R85 and R26 and capacitor C8 and the positive pulse output is taken from the collector of Q13. The second series of half-shots are formed by transistors Q18, Q19, Q21, and Q22 and function similarly to the series described above. A positive pulse at the base of transistor Q18 triggers a 260-microsecond half-shot and a 30-microsecond half-shot. The positive-going 260-microsecond half-shot output is taken from the collector of transistor



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Figure 54. Programmer Module No. 1, Logic Diagram

Q19. Resistors R86 and R40 and capacitor C9 determine the pulse width of the 260-microsecond half-shot. The pulse width of the 30-microsecond half-shot is controlled by resistor R53 and capacitor C10. The trailing edge of the 30-microsecond pulse from the collector of transistor Q21 triggers a 200-microsecond half-shot. The output of the 200-microsecond half-shot is taken from the collector of Q22, with half-shot pulse width determined by resistors R87 and R55 and capacitor C11. The outputs of the 200- and 260-microsecond half-shots are routed to diode AND gates that AND these outputs with signals from the 8:1 counters to develop required pulses for the coder and multiplexer.

The NPN-type transistors Q27 through Q32 form a three-stage counter that uses saturated stages and ac coupling. The three stages are identical and operate between PSC and +6 volts. The 500-cps inverted signal is differentiated and diode-coupled to the bases of the first bistable multivibrator, causing negative triggering of this multivibrator. The remaining stages are coupled and triggered in the same fashion. The 8:1 counters are dc reset once every second to develop the proper rate of 62.5 words-per-second. The outputs of the 8:1 counter are routed to diode AND gates that produce the appropriate system timing pulses.

The coder commands are developed by ANDing signals from the 8:1 counters and 200-microsecond half-shots. The resulting pulses are routed to two buffer amplifiers formed by transistors Q25 and Q23, and Q26 and Q24. A positive pulse at the base of transistor Q25 causes the transistor to saturate with resultant current flow through the base-emitter junction of transistor Q23 to turn on that transistor. The resulting output waveform is a positive-going 200-microsecond pulse. Operation of buffer transistors Q26 and Q24 is similar to that described for transistors Q25 and Q23.

The duty cycle and delayed duty cycle pulses are developed by ANDing signals from the 8:1 counter, the 200-microsecond half-shots, and the 260-microsecond half-shots. The resulting pulses are routed to two active OR gate and buffer circuits. Transistors Q8, Q9, Q10, and Q11 form one of the active OR gate and buffer combinations, from which is developed the 260-microsecond duty cycle pulses. Transistors Q8 and Q9 form an active OR gate. A positive signal to the base of transistor Q8 or Q9 causes that transistor to saturate, turning off normally on transistor Q10. When Q10 turns off, transistor Q11 turns on with a resulting 260-microsecond negative-going waveform to the multiplexer. Transistors Q14 through Q17 form the second active OR gate buffer assembly, having operation similar to that described above. The pulse from the second buffer assembly to the multiplexer is a negative-going, 200-microsecond pulse.

b. Programmer Module No. 2. Refer to the programmer module No. 2 logic diagram, figure 55, and schematic diagram, figure I-19. Programmer module No. 2 consists of a 1/16-cps pulse generator, a 1-cps reset circuit and a time code circuit.

The 1/16-cps pulses are produced by transistors Q17, Q18, and Q19. Transistors Q17 and Q18 form a 200-microsecond half-shot which drives buffer inverter transistor Q19. A positive pulse to the base of transistor Q17 causes saturation of the transistor to discharge capacitor C9. As capacitor C9 discharges, the base-emitter junction of transistor Q18 is back-biased and the transistor is turned off. Resistor R43 controls the discharge time of C9

and is chosen to hold transistor Q18 turned off for 200 microseconds. The output from the collector of transistor Q18 is routed to the base of inverting amplifier transistor Q19. The output from transistor Q19 is applied through diode CR29 and five 1-K ohm output resistors to the external circuits. Transistors Q20, Q10, Q11, and Q6 form the monitor circuit for the 1/16-cps half-shot. This monitor circuit develops a signal to a digital multiplexer channel when a 1/16-cps pulse appears. Transistors Q10 and Q11 are connected to form a bistable multivibrator, and transistors Q20 and Q6 provide the set and reset circuits for the multivibrator. When a 250-microsecond pulse is applied to the base of transistor Q20, the transistor conducts to cause current flow in the base-emitter junction of transistor Q11. This changes the state of the bistable multivibrator such that Q11 is saturated and Q10 is off. The 1-cps external reset pulse is inverted by transistor Q6, differentiated by capacitor C6 and resistor R30, and coupled through diode CR19 to the base of Q11. The bistable multivibrator is triggered on the negative edge of the input pulse such that the multivibrator returns to its normal state (transistor Q11 turned off). Diodes CR29 and CR30 protect the 250-microsecond half-shot circuit from shorts in the external circuits or in the monitor bistable multivibrator.

The 1-cps reset circuit resets the 8:1 and the 62.5:1 counters to obtain the required frame length of 62.5 words per second. The 1-cps reset circuit consists of a 500-microsecond monostable multivibrator formed by transistors Q1, Q2, and Q5, a 500-microsecond half-shot formed by transistors Q6 through Q9, and a 7-input AND gate formed by diodes CR1 through CR7.

The 500-microsecond monostable multivibrator furnishes reset pulses to the counters. A positive pulse to the base of transistor Q1 causes that transistor to saturate and discharge capacitor C1 through resistor R3. Capacitor C1 and resistor R3 determine the pulse width of the monostable multivibrator. Transistor Q2 is held off until capacitor C1 discharges. Resistors R1 and R4 provide a positive voltage to the base of transistor Q1 to hold the transistor turned on until C1 has discharged. The output of the monostable multivibrator is taken from the collector of Q2 and applied to the base of transistor Q5 and to the 8:1 counter reset line. The positive pulse to the base of transistor Q5 causes Q5 to saturate with a resultant negative-going pulse to the 62.5:1 counter reset line. Positive pulses from two sources are routed through an OR gate formed by diodes CR8 and CR9 to trigger the 500-microsecond monostable multivibrator. The first source of triggering for the multivibrator is the 1-cps pulse (CY1A) from the Nimbus clock. The positive-going edge of the 1-cps pulse turns off transistor Q6. When Q6 turns off, Q7 also turns off, thus turning on transistor Q8. Transistors Q8 and Q9 form a 500-microsecond half-shot similar in operation to the 250-microsecond half-shot in the 1/16-cps pulse generator. Capacitor C4 and resistor R22 determine the pulse width of this half-shot. The output of the 500-microsecond half-shot is taken from the collector of transistor Q9 and gated with the 500-cps No. 1 signal. The gated output is routed to the OR gate at the 500-microsecond monostable multivibrator input. The 7-input AND gate provides the second source of triggering for the 500-microsecond half-shot. This AND gate receives inputs from the internal counters and provides the proper timing pulses to operate the system at a 62.5 words-per-second rate. The output of the 7-input AND gate is routed through the OR gate at the 500-microsecond monostable multivibrator input. Normally, the 500-microsecond half-shot is triggered from the Nimbus clock; however, if a failure in the Nimbus clock occurs, the PCM will still be reset by signals from the internal counters.

The time code storage circuit consists of a storage shift register and a shift line driver and gating circuit. The shift register stores the serialized time code entering the PCM and provides parallel time code outputs to the digital multiplexer. The NPN-type transistors Q24 through Q31 form a 4-stage shift register that employs saturated stages and direct-coupled transfer through steering resistors. All four stages of the register are identical. Transistor Q21 is a level shifter and buffer transistor that drives transistor Q22. Transistors Q22 and Q23 are a complementary pair that are coupled to the shift register through steering resistors R80 and R81. The shift pulses are developed by gating a delayed 38.5-millisecond pulse with a 100-cps signal. Transistors Q12 through Q16 form two precision half-shots, similar in operation to the 250-millisecond half-shot used in the 1/16-cps pulse generator except that temperature compensation is furnished by diodes CR21, CR22, CR24, and CR25. The half-shot formed by Q13 and Q14 is triggered by the positive-going edge of the 10-cps pulse to develop a 16.5-millisecond output. The half-shot formed by transistors Q15 and Q16 is triggered by the trailing edge of the 16.5-millisecond pulse and develops a 38.5-millisecond output. This creates a 38.5-millisecond pulse that is delayed 16.5 milliseconds from the positive-going edge of the 10-cps clock pulse. Transistor Q12 is used to shift the incoming level and to drive transistor Q13. The 38.5-millisecond positive-going pulse is ANDed by a diode AND gate consisting of diodes CR12 and CR13 with the 100-cps (YBI) from the Nimbus clock which is received through buffers Q3 and Q4. The gated output is differentiated and diode-coupled to the bases of the shift register bistable multivibrators.

c. Programmer Module No. 3. Refer to the programmer module No. 3 logic diagram, figure 56 and schematic diagram, Figure I-20. Programmer module No. 3 consists of ID buffers, coder storage circuit, clamp circuit, and a temperature sensing circuit.

The four identical ID buffers are formed by transistors Q2 through Q5 and Q10 through Q13. When the base of transistor Q2 is returned to PSC, Q2 saturates and causes transistor Q10 to also saturate. The resulting waveform is a negative-going signal that stays negative as long as the base of Q2 is at PSC. The three remaining buffers operate similarly.

The coder storage circuit consists of three bistable multivibrators that store the first three bits of data from the 10-bit coder. The data is then routed to selected digital multiplexer channels at the proper time to develop a full 10-bit word. The storage bistable multivibrators are formed by NPN-type transistors Q21 through Q26. Transistors Q32, Q35, and Q38 are buffer amplifiers that provide outputs to the digital multiplexer. Transistors Q33, A34, Q36, Q37, Q39, and Q40 make up the set circuits of the three bistable multivibrators, and transistors Q6, Q7, Q1, Q9, Q15, and Q14 make up the timing circuits to strobe data into the bistable multivibrators. Transistors Q41 and Q8 are for external test purposes only. Transistors Q25 and Q26 make up one storage bistable multivibrator. In the normal condition, transistor Q26 is on and transistor Q25 is off. With transistor Q25 off, transistor Q38 is saturated and a -6-volt level is routed to the digital multiplexer to signify a ONE bit. The coder places either a -6-volt level (for a ONE) or a PSC level (for a ZERO) at the base of Q39. Two strobe pulses must then be received before the input from the coder can be stored in the bistable multivibrator. When a positive digital detection pulse from the multiplexer is received at the base of transistor Q7, the transistor saturates and causes transistor Q1 to saturate. With transistor Q1 saturated, +3 volts is applied through R8 to the base of Q6. In the center of the digital detection pulse, a 15-microsecond strobe pulse places -6 volts on the emitter of transistor

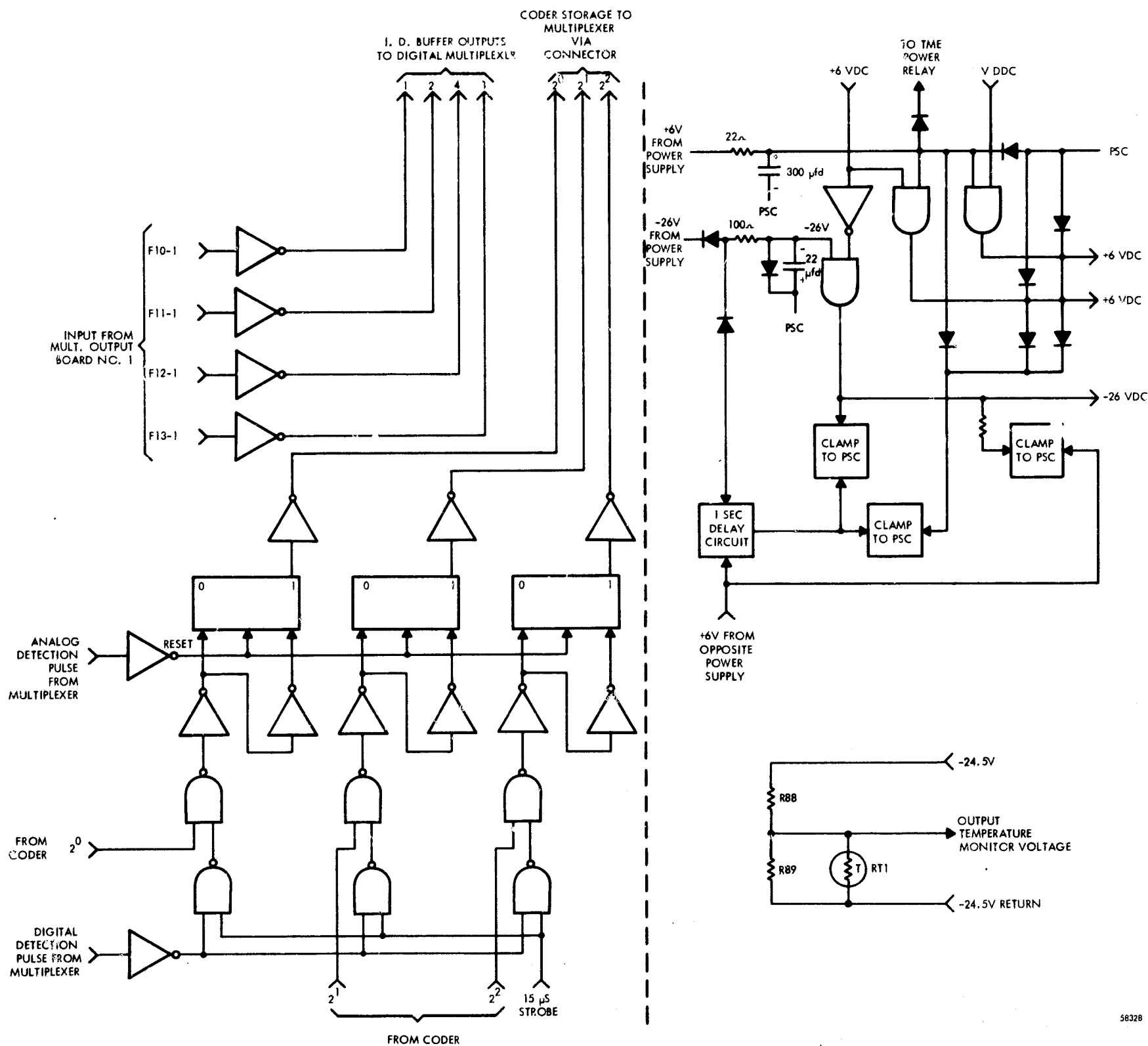


Figure 56. Programmer Module No. 3, Logic Diagram

Q6. Transistor Q6 functions as an AND gate in that it requires both the digital detection pulse and the 15-microsecond strobe to cause the transistor to conduct. When transistor Q6 turns on, transistor Q9 also turns on and places PSC on the emitters of bistable multivibrator set circuits, Q39 and Q40. If a ONE (-6 volts) is applied to the base of transistor Q39, the transistor turns on and transistor Q40 remains off. When transistor Q39 is on, current flows through the base-emitter junction of Q26, through diode CR27, and through resistor R79 to hold transistor Q26 on. Transistor Q25 then remains off and saturated transistor Q38 applies a -6-volt level (ONE) to the digital multiplexer. If a ZERO (PSC) is applied to the base of transistor Q39, the transistor remains off and transistor Q40 turns on. When transistor Q40 is on, current flows through the base-emitter junction of Q25, through diode CR28, and through resistor R73 to cause transistor Q25 to turn on. Transistor Q38 turns off when Q25 turns on and PSC (ZERO) is applied to the digital multiplexer. When set to the ZERO state, the bistable multivibrator remains in that condition until a positive analog detection pulse from the multiplexer resets the bistable multivibrator. The positive reset pulse is applied to the base of transistor Q15, causing that transistor to saturate and causing transistor Q14 to turn off. When the analog detection pulse is removed, transistor Q15 turns off and transistor Q14 turns on. The resulting square wave developed by transistor Q14 is differentiated and diode-coupled to the base of transistor Q25, causing negative triggering of the bistable multivibrator and turning transistor Q25 off. When transistor Q25 turns off, transistor Q38 turns on and applies a -6-volt level (ONE) to the digital multiplexer.

The clamp circuit includes a 260-microsecond duty cycle driver formed by transistors Q16 and Q17. When PSC is applied to the bases of these parallel drivers, the drivers saturate and produce a +6-volt pulse to the multiplexer. The base of the 200-microsecond delayed duty cycle pulse driver, transistor Q18, also receives a PSC pulse and develops the delayed +6-volt pulse to the multiplexer. The PSC level to the base of transistors Q16 and Q17 is also applied to the base of transistor Q19, causing Q19 to conduct. When Q19 conducts, Q20 conducts to develop a 260-microsecond, -26-volt duty cycle pulse to the multiplexer. The -26-volt line to the multiplexer is filtered by resistor R44 and capacitor C5. Because of failures that can occur in the redundant multiplexers, the duty cycle and voltage lines to the off multiplexer must be clamped to ground to ensure that a failure in the off multiplexer will not place a positive or negative voltage on the lines and cause a failure in the on multiplexer. When the clamp circuit is not clamping the power lines, capacitor C9 is charged to -26 volts through CR16, R49, and CR30. Diode CR30 is a 3.5-volt Zener diode that is forward-biased when C9 is charging. Capacitor C5 is also charged to -26 volts and capacitors C3 and C4 in the +6-volt line are charged to +6 volts. When power is switched off, a positive voltage is placed on the emitter of transistor Q31 causing that transistor to conduct. Capacitor C5 then begins to charge to +6 volts through R87, R67, Q31 and CR29, and C9 charges to +6 volts through R51 and CR30. When C5 reaches +0.5 volts, diode CR11 becomes forward-biased and clamps the -26-volt line to this voltage. Capacitor C9 and resistor R51 are selected such that the -26-volt line will be clamped to +0.5 volts before the voltage across C9 reaches zero. As the voltage across C9 reaches zero, the positive voltage through R51 and CR22 to the base of transistor Q29 causes that transistor to turn on. Transistors Q29 and Q30 turn on together and clamp the junction of C9, CR22, R49, and R51 to approximately +1.5 volts. At the same time, diode CR30 becomes reverse-biased through R59 and applies +3.5 volts to the positive end of C9. The positive voltage keeps C9 biased in the proper direction so that it will not be

damaged by a positive voltage applied to its negative terminal. When transistors Q29 and Q30 turn on, transistors Q28 and Q27 turn on. Transistor Q27 clamps the -26-volt line to -0.2 volt if a negative fault voltage occurs, and diode CR11 clamps the line to +0.5 volt if a positive fault voltage occurs. With transistor Q30 turned on, the +6-volt duty cycle lines and the +6-volt line are clamped through their associated diodes. Diodes CR12, CR13, and CR14 clamp these lines to +0.5 volts if a positive fault voltage occurs and diodes CR8, CR9, and CR10 clamp the lines to -0.5 volts if a negative fault voltage occurs. The external loads in the system and resistor R37 cause capacitors C3 and C4 to also be discharged before the voltage across C9 reaches zero.

The temperature sensing circuit is a voltage divider network formed by resistor R88 in series with the parallel combination of resistor R89 and thermistor RT1. The -24-volt supply voltage to the voltage divider network is switched on or off and the output of the network is routed to an analog channel in the multiplexer.

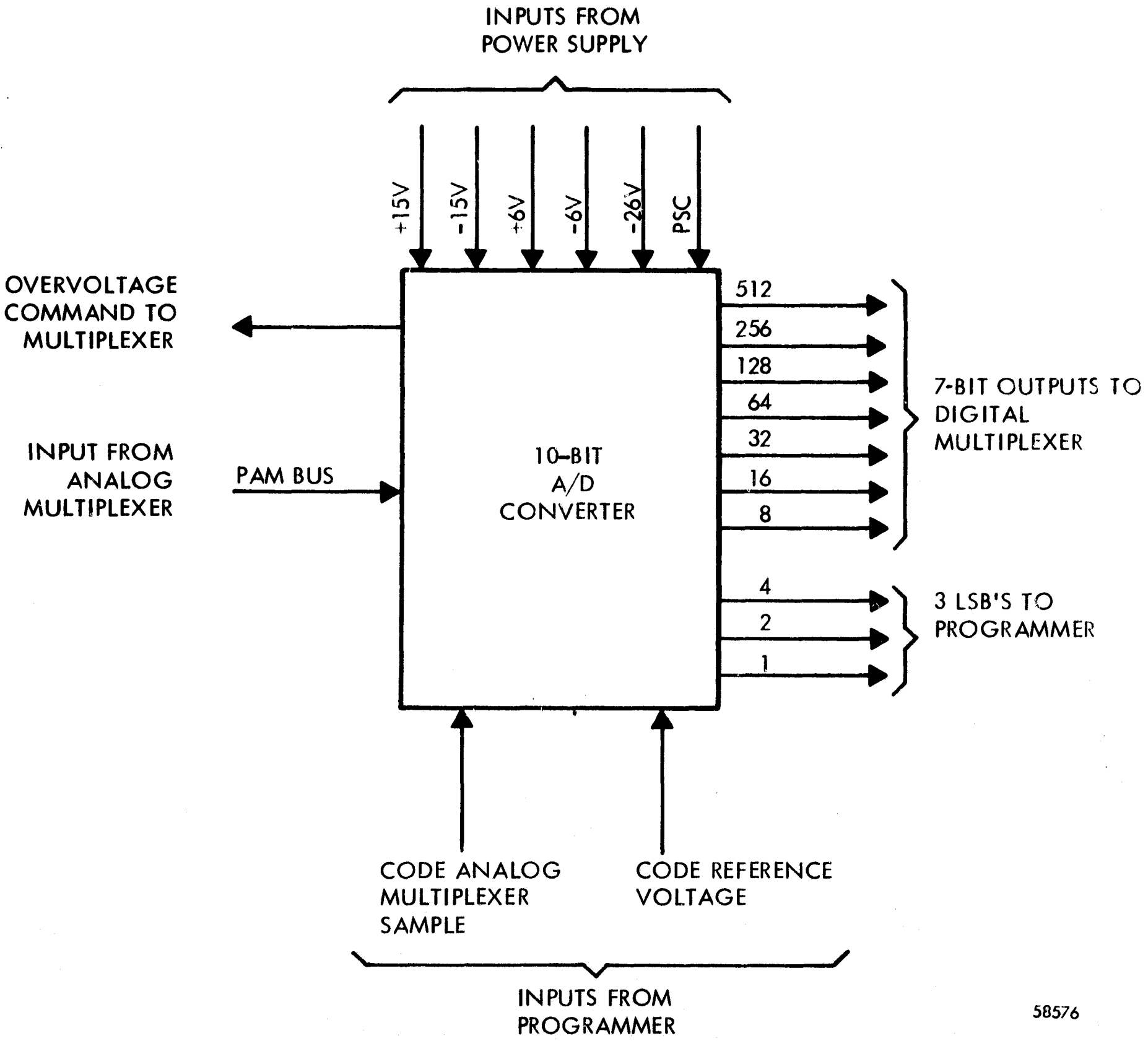
2.3.1.5 ANALOG-TO-DIGITAL CONVERTER (CODER).

2.3.1.5.1 GENERAL. The coder consists of three modules designated coder module numbers 1, 2, and 3. Coder module No. 1 is termed the analog module and contains all of the analog circuitry. Module No's. 2 and 3 are both digital modules, with coder module No. 3 containing the 10-stage ramp counter. Because the PCM unit is block redundant, there are two complete coders, making a total of six coder modules.

2.3.1.5.2 BLOCK DIAGRAM DESCRIPTION. Refer to the coder block diagram, figure 57, and simplified logic diagram, figure 58. The coder converts input analog signals of 0 volt to -6.4 volts full scale into equivalent 10-bit binary codes. The coder provides a resolution of 1 part in 1024, but only 7 bits (1 part in 128) are hardwired into the multiplexer. The additional 3 bits can be individually selected to provide 8-bit resolution (1 part in 256), 9-bit resolution (1 part in 512), or 10-bit resolution (1 part in 1024). The digital channel capability is reduced when an analog channel resolution greater than seven bits is selected. Increased resolution of analog channels is possible only when the channels are immediately followed by digital channels in the output format.

Upon receipt of a code command, the coder stores the input analog voltage sample and compares the sample with a 10-bit binary RC ramp function. If the input sample is -6.4 volts or more, the ramp will allow 1023 counts to a 10-stage counter. A full code count of 1023 turns off the coder so that the full code count is held and the counter does not recycle. The counter is advanced at a 500-kc rate (two microseconds per count) so that a full code ramp requires 2.046 milliseconds (1023×2 microseconds). Input signals that are less than full scale are coded faster; for example, a half scale input requires only half of the coding time required for a full scale signal.

During digital time slots, the coder is forced to code overvoltage. All digital time slots require the coder to switch in the required circuits for readout from the digital multiplexer, instead of from the coder. The overvoltage command not only controls the multiplexer, but is also applied to the programmer to develop an output to control the external PCM TEST SET in the automatic mode.



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Figure 57. Coder, Simplified Block Diagram



Figure 58. Coder, Simplified Logic Diagram

The three coder modules contain the following circuits:

Module No. 1

Buffer Amplifier
Leakage Current Clamp
Ramp Generator and Detector
Calibrate Reference and Switch

Module No. 2

500-KC Oscillator
Counter Input AND Gate
Encode/Calibrate Circuits
Counter Reset

Module No. 3

10 Stage Binary Counter
Overvoltage Detector

a. Coder Module No. 1.

(1) Buffer Amplifier. A low leakage diode clamp at the input to the buffer amplifier is connected to the -15 volt supply to prevent the PAM bus from going more negative than approximately -15.5 volts. The clamp protects the coder input from fault voltages in excess of -15.5 volts. The output of the buffer amplifier charges the ramp polycarbonate capacitor to the input sample voltage within a command time of 170 microseconds.

(2) Leakage Current Clamp. A special leakage current clamp circuit is used with the input buffer amplifier to cancel the feedback leakage currents. This circuit utilizes a select-at-test resistor that is selected during module test to minimize amplifier feedback current to the PAM bus line. The circuit is "boot-strapped" to the output of the amplifier to provide feedback current that is independent of the input signal voltage.

(3) Ramp Generator and Detector. The ramp generator is a constant current source that discharges the sampled voltage stored on the ramp capacitor. When the ramp operation begins (at the beginning of every cycle), the 500-kc count pulses are applied to advance the 10-stage counter. When the ramp constant current source has discharged the sample capacitor to zero volts, the 500-kc count pulses to the 10-stage counter are removed. Thus, the ramp function begins at the input sample voltage level and ends at zero volt. An input voltage of -6.257 millivolts operates the ramp for two microseconds, while an input voltage of -6.4 volts operates the ramp for 2.046 milliseconds. The weight-per-count is set at 6.257 millivolts (1023 counts equal to 6.400911 volts) and is consistent with earlier Nimbus PCM units. The Nimbus A and Nimbus B PCM units will produce the same 7-bit code for a given input voltage, as both have a resolution of 50 millivolts per least significant bit (for coding with 7-bit resolution of 0-volt to -6.4-volt full scale data).

(4) Calibrate Reference and Switch. The calibrate circuit contains a Zener diode reference (0.0005% per °C), connected to produce a full scale code (1023) at the coder output. The output of the Zener regulated reference is applied through an analog channel gate similar to the multiplexer analog channel gates. During the time of one output word, the coder receives one analog channel sample command and three calibrate commands. Therefore, the coder is calibrated three times as often as it codes input samples. The calibrate circuits control the amount of constant current discharging the ramp sample capacitor to compensate for circuit aging and frequency changes of the 500-kc oscillator.

b. Coder Module No. 2.

(1) 500-KC Oscillator. The 500-kc oscillator consists of a 1-megacycle free-running multivibrator (with an anti-lockup circuit), a 2:1 reduction counter, and output driver. The oscillator uses 5-percent room ambient glass dielectric capacitors and select-at-test 1-percent resistors to set the room ambient frequency to 1.1 megacycle ± 2 percent. The oscillator output frequency must be maintained at 500 kc or greater to prevent full scale counting time from overlapping the coder readout command. The anti-lockup circuit prevents both sides of the oscillator from turning on at the same time and ensures that the oscillator will oscillate every time that power is applied to the PCM unit. The 2:1 reduction counter provides symmetry to the output signal and the output driver provides load handling capability with faster control speeds.

(2) Counter Input AND Gate. The 500-kc bit rate count pulses to the 10-stage binary counter are controlled by a counter input AND gate such that the first count occurs at one count time after the constant current source begins to discharge the sample capacitor, and the count pulses are immediately removed when the sample capacitor discharges to zero volts. Synchronism of the first count with the ramp discharge is accomplished by a control flip-flop driven at the 500-kc bit rate. At t_0 , the flip-flop is set and the ramp function begins to discharge the sample capacitor. At $t_0 + 1$ bit time, the first count pulse is gated to the 10-stage counter. When the capacitor voltage crosses zero volts, the output of a differential amplifier inhibits the AND gate. Because the output of the differential amplifier is not synchronous with the 500-kc bit rate, the gate can be inhibited just before a count pulse. If the gate is inhibited just before occurrence of a count pulse, then the actual digitized code can be low by nearly one bit count. The limit in coder quantizing ability is stated as $\pm$ one-half bit, which provides a range of one bit.

(3) Encode/Calibrate Circuits. Because the coder operates at four times the frequency required for the Nimbus B program, and because the coder contains self-correction circuits, it was decided to encode the analog multiplexer output at the beginning of a cycle, and then calibrate the coder three times before the next sample command. To simplify the coder command circuitry in the programmer, the coder is allowed to operate four times during all word intervals including analog, digital, time code, sync, and I.D. words. The coder first receives a code command that opens an analog multiplexer gate and places a sample voltage on the ramp capacitor. This sample is either from an analog transducer circuit or a deliberate over-voltage (-15 volts) hard-wired within the PCM to switch the readout circuits to read data from the digital multiplexer. Analog coding is accomplished in the first four milliseconds of the

coding interval and, in the 12 milliseconds before the next code command, three calibrate commands, four milliseconds apart, are generated such that the coder operates once every four milliseconds. Each calibrate command occurs during a time when the analog multiplexer is not commanded and opens an analog channel gate within the coder to place a full-scale reference voltage on the coder input PAM bus. The precision reference voltage is stored on the sample capacitor which is discharged by the ramp constant current source in a time interval equal to a full scale count of 1023. If the count of 1023 occurs before the sample capacitor discharges to zero volts, the full scale detect signal modulates the constant current source to increase the slope of the ramp. If the ramp voltage crosses zero volts before the count reaches 1023, the zero level detect signal modulates the constant current source to decrease the slope of the ramp. If the zero volt crossing is detected coincident with a count of 1023, the coder is properly calibrated. By correcting the slope of the ramp, the coder remains calibrated regardless of temperature changes and aging of components.

(4) Counter Reset. The 10-stage binary counter is reset at the beginning of each word time such that all outputs are binary zeros. The all-zero code is considered to be the 0 count or the first binary level. The counter is also reset at the beginning of each calibrate cycle; thus, the counter reset frequency is four times per word or once every 4 milliseconds. Because a full scale ramp requires approximately 2 milliseconds, the coded binary data is available for the remaining 2 milliseconds before the counter is reset.

c. Coder Module No. 3.

(1) 10-Stage Binary Counter. The 10-stage binary counter is a standard counter that produces an output level of -1 volt for a binary ZERO and -6 volts for a binary ONE. The first three counter stages have special output buffer amplifiers to drive the 3-bit storage register in the programmer, while the remaining seven counter stages are connected directly to digital multiplexer gates. The digital multiplexer detects level changes -3 ± 0.75 volts; therefore, a logical ZERO is any voltage level between 0 volts and -2.25 volts while a logical ONE is any voltage level between -3.75 volts and -10 volts.

Output levels from the three least significant bit buffers (2^0 , 2^1 , and 2^2) are ZERO = 0 volts and ONE = -5.5 volts.

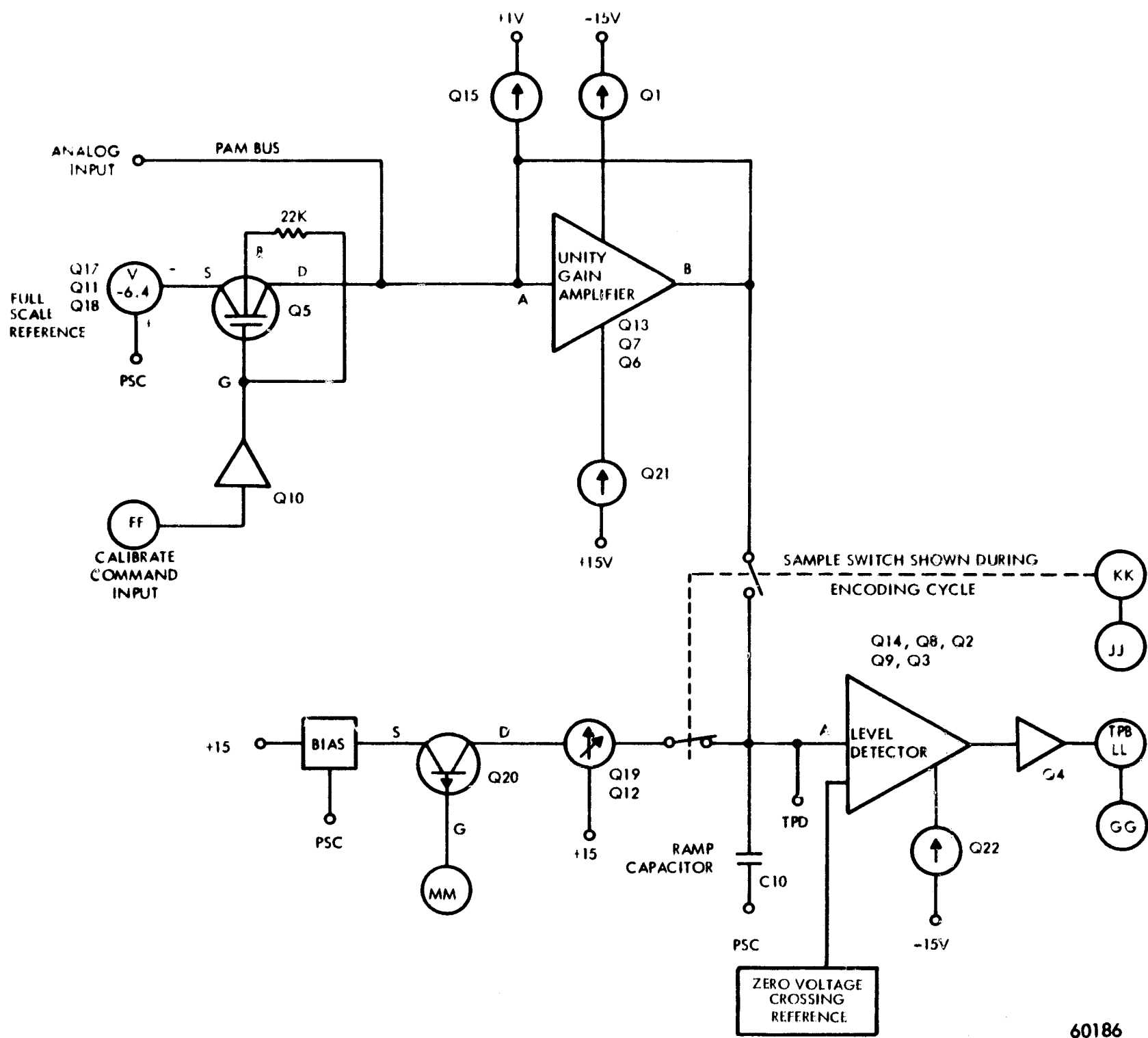
(2) Overvoltage Detector. The overvoltage detector circuit is a 10-input AND gate that turns on a transistor when all ten inputs are at the ZERO level. The inputs to this gate are wired from the opposite side of the normal data output so that when the output data is all ONE's (full scale binary count of 1023), the inputs to the AND gate are all ZERO's and an overcode level of +6 volts is produced. When the normal data output is any code other than full code, the output level from the overcode detector is 0 volts. This +6-volt overcode pulse is routed to the coder ramp control circuit described above and is also routed to the multiplexer for digital channel switching. The overcode pulse will be a square wave having a pulse width of approximately 2 milliseconds.

2.3.1.5.3 DETAILED DESCRIPTION. The detailed electrical description of the three coder modules are described in the following subparagraphs.

a. Coder Module No. 1. Refer to the coder module No. 1 logic diagram, figure 59, and schematic diagram, figure I-21. This module contains a unity gain buffer amplifier, a precision controllable constant current source, a ramp capacitor, a level detector, and a precision voltage reference source.

(1) Buffer Amplifier. The unity gain buffer amplifier consists of transistors Q13, Q21, Q15, Q1, Q6, and Q7. The analog or calibrate voltage input is applied to side A of differential amplifier Q13, which has a constant current generator, Q21, and current sink, Q1. Transistor Q13 is a precision differential amplifier with sides A and B having closely matched temperature characteristics. Transistor Q21 is a constant current generator, which functions to bias Q13 at a point of low drift and maximum gain. Resistors R8, R9, R29, R44, and R45 set the bias conditions. Transistor Q1 is a constant current sink, which provides the collector load for Q13B. Because Q1 has a high ac impedance, it has the effect of increasing the gain of Q13. Emitter-followers Q6 and Q7 isolate the differential amplifier from the load and provide current gain and low output impedance for charging the ramp capacitor. The emitter-followers also hold the base-collector junction of Q13B back-biased. Transistor Q7 drives ramp capacitor C10 and the base of Q13B. The feedback signal from emitter-follower Q7 to the base Q13B closes the amplifier loop and reduces the amplifier gain to unity. The amplifier open loop gain is very high, providing high input impedance, high accuracy (input to output) and low output impedance. The output impedance is sufficiently low to charge the capacitor C10 to approximately 15 time constants during the 170-microsecond sample time. Transistor Q15 tracks the base current of Q13A so that no current flows back to the analog source. Transistor Q15 is chosen such that its base-emitter junction closely tracks (over temperature variations) the base-emitter junction of Q13A. Resistor R28 is selected to set the base current of Q15 to cancel the feedback current to the analog source. Zener diode CR24 is used as a DC level shifter at the output of emitter-follower Q6. Resistor R28 and collector of Q13A, through R49, are bootstrapped to the input voltage through this diode. The bootstrap action ensures that the feedback current remains small (or nonexistent) over the analog input voltage range. Bootstrapping is required because the h_{ob} parameter of Q13A causes changes in base current when the analog input voltage varies. A change of base current in Q13A would cause current flow into the analog source, which would be reflected as an off-set voltage to the coder and introduce an error.

(2) Precision Voltage Reference Source. The precision voltage reference source is made up of transistors Q5, Q10, Q17, Q11 and Q18. Transistor Q17 is a differential amplifier in which the base of side B is referenced to 6.8-volt precision Zener diode CR14. The precision voltage on the base of Q17B holds a constant voltage across stable resistor R40. Resistor R40 sets the bias current through Q17. The base of Q17A follows the base of Q17B, and, through a precision resistor divider (R36 through R39 and R24), sets the reference voltage on the PAM bus. A voltage regulator circuit is included to hold the supply voltage across the precision reference voltage circuits constant. Series regulator Q11 prevents any change in supply voltage from affecting the precision reference voltage circuits. If the voltage at the collector of Q17B increases, transistor Q18 increases conduction. As the collector current of Q18 increases, the base current to Q11, normally furnished by R27, is channeled through Q18. Thus, Q11 conducts less and causes more voltage to be dropped across the transistor, thereby decreasing the voltage across the precision reference voltage circuits. Diodes CR15 and CR16 bias Q18 at the proper level so that it is compatible with Q17B. Capacitor C2 rolls-off the high frequency response of the regulator circuit and prevents the regulator circuit from oscillating. Transistor Q5, a MOS gate controlled by Q10, switches the calibrate voltage to the PAM bus.



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Figure 59. Coder Module No. 1, Logic Diagram

(3) Precision Controllable Constant Current Source. The precision constant current source is used to discharge ramp capacitor C10. The constant current discharge of the ramp capacitor produces a linear voltage ramp function. The precision current source is made up of transistors Q19, Q12, and Q20. Transistor Q19 is a differential amplifier in which side A is referenced to 6.7 volts by precision Zener diode CR17. Bias current for diode CR10 is set by resistor R18. The temperature-compensated Zener (CR17) impresses a constant voltage across the series combination of Q20 and the voltage divider filter network R51, R41, R42, and C9. The current that flows through this network is a precision current that is varied by field effect transistor (FET) Q20. This FET functions as a variable resistor and is the current control device. The bias voltage to the FET is from the ramp correction circuit in coder module No. 2. Transistor Q12 is a current amplifier that is connected through resistor R30 to ramp capacitor C10. As the current through Q19A varies, the current through Q12 varies. This variation in Q12 current changes the slope of the ramp to correct for errors in the coder. Zener diode CR7, in the emitter circuit of transistor Q12, permits use of a larger value of resistance for R19 to improve temperature stability of the precision current source. Resistor R43 and capacitor C7, with resistor R7 and capacitor C1, act as filter networks for the constant current circuits. Diode CR20 limits the positive charge across capacitor C10. During the time in which Q7 is charging capacitor C10, the current from current source transistor Q12 is routed through the emitter-base junction of Q7.

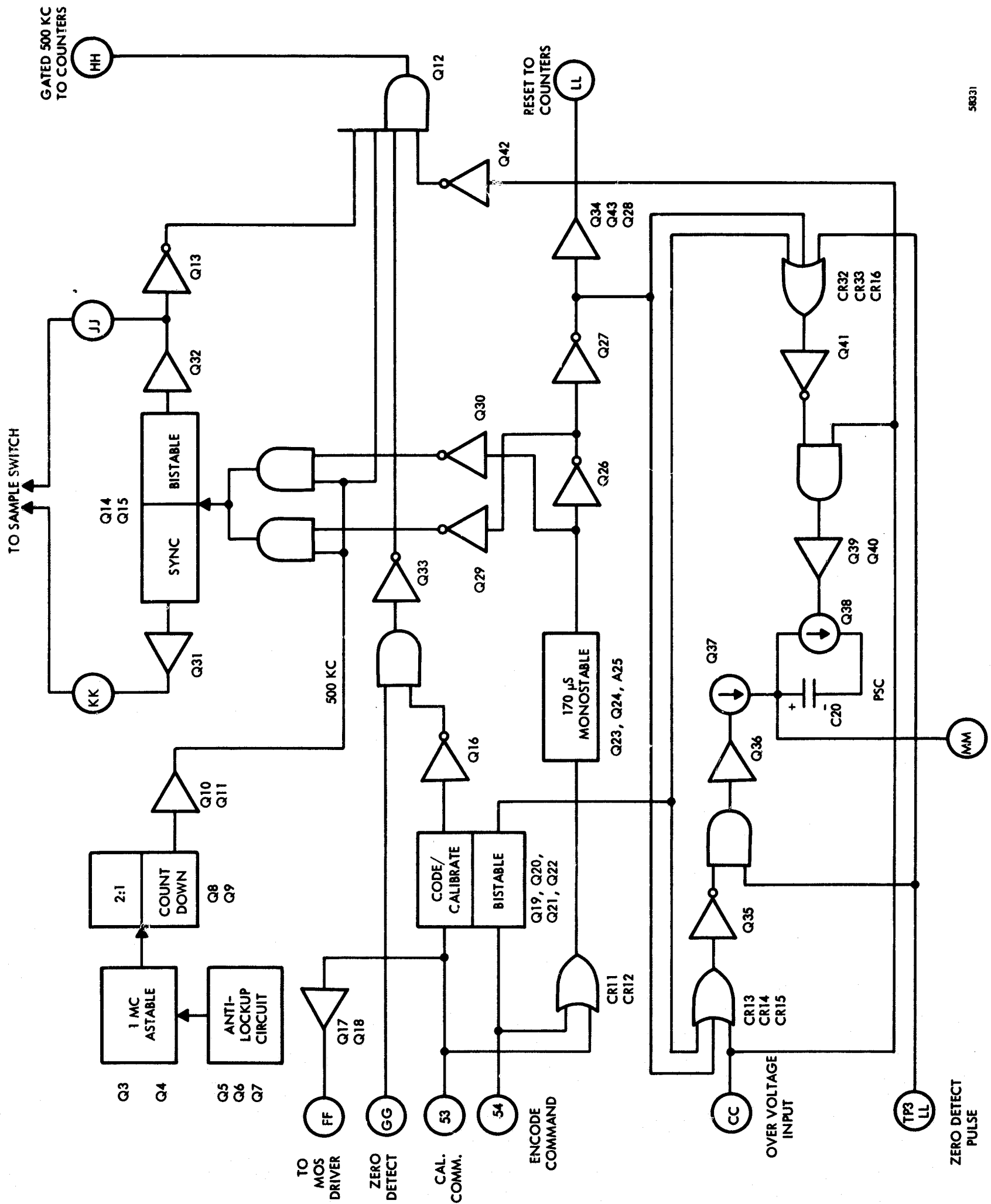
(4) Precision Ramp Capacitor. Ramp capacitor C10 has been chosen for minimum dielectric absorption, minimum loading effects, and good stability with respect to voltage variations. The dielectric material is polycarbonate.

(5) Level Detector. The level detector is a comparator that determines if the analog input voltage is greater or less than the zero reference level. In any comparator circuit there is an input range over which the amplifier output is indeterminate. The amplifier must have sufficient gain to make this ambiguity negligible. To achieve the required gain, three differential amplifiers stages (Q14, Q2 and Q3, and Q8 and Q9) are connected in cascade and an output driver transistor (Q4) is used. The level detector provides an inhibit pulse to external circuits when the ramp function crosses the zero reference level. The input to the level detector is at the base of Q14A. Transistor Q14 is biased by constant current sink Q22 so as to have low dc drift, low noise, and high gain. The input impedance to Q14A is high so as not to affect the discharge rate of ramp capacitor C10. The analog voltage on the base of Q14A is compared with the reference level set on the base of Q14B by R32, R33, and R48. Resistor R32 is selected for the ONE bit to switch in at the desired analog input magnitude. Diodes CR9 and CR12 are used to hold Q14 in the linear operating region. These diodes clamp the two sides of Q14 together, thus limiting the output swing to provide rapid recovery from saturation. The collectors of Q14 drive the second differential amplifier made up of Q2 and Q3. This second differential amplifier also has limiting diodes (CR5 and CR6) in the collector circuits to speed up the recovery time. The outputs of Q2 and Q3 drive the third differential amplifier made up of Q8 and Q9. Buffer amplifier Q4, at the output of the third differential amplifier, drives error detector circuits in coder module 2. Diode CR13 in the emitter circuit of Q4 is a dc level shifter to make transistor Q4 compatible with the output level of Q8.

(6) Sampling Switch. The sampling switch provides the coder with a sample and hold capability and disconnects the buffer amplifier from the capacitor during the linear discharge period. Because discharge paths other than the constant current source produce a nonlinear ramp (all loading effects result in a "bowed" ramp voltage), an extremely high impedance switching arrangement made up of diodes CR18, CR23, and CR19 is employed. After an analog signal has been impressed on ramp capacitor C10, transistors Q13 and Q7 are electrically disconnected by routing control signals to signal lines KK and JJ at the proper time. A positive signal to line KK is applied through diode CR19 to reverse-bias the base-emitter junctions of transistors Q6 and Q7 to present a very high impedance to capacitor C10. Simultaneously, a negative voltage is applied to signal line JJ and is routed through diodes CR18 and CR23 to reverse-bias the base-emitter junction of Q13A and the collector-base junction of Q21. Diodes CR11 and CR8 prevent emitter-base breakdown of Q13 and Q7 caused by the reverse-bias voltage placed on these junctions.

b. Coder Module No. 2. Refer to coder module No. 2 logic diagram, figure 60, and schematic diagram, figure 1-22. This module contains a 500-kc oscillator, a 170-microsecond sample monostable multivibrator, a sync bistable multivibrator and counter gate control circuit, a code/calibrate bistable multivibrator, a reset circuit, an exclusive OR gate with proportional control error correction circuit and a MOS gate command circuit.

(1) 500-KC Oscillator. Transistors Q3 through Q7 form a 1 megacycle oscillator with an anti-lockup circuit. Transistors Q3 and Q4 form an astable multivibrator circuit, and Q5 through Q7 form an anti-lockup circuit. For discussion purposes, assume that transistors Q5 through Q7 are not connected in the circuit, assume that transistor Q3 has just turned on, and assume that transistor Q4 has just turned off. Under these conditions, the voltage across capacitor C1 is approximately +6 volts, which makes V_{BE} of Q4 approximately -6 volts. The initial voltage across capacitor C2 is approximately zero and the base end of C2 is clamped to V_{BE} of Q3. Capacitor C2 is rapidly charged through resistor R5 to +6 volts. The RC time constant of R5 and C2 causes the leading edge of the output waveshape to be rounded. Transistor Q3 is held on by the current through resistor R4. The collector end of C1 is clamped to $V_{CE(SAT)}$ of Q3. Capacitor C1 charges such that V_{BE} of Q4 rises toward +6 volts. As V_{BE} of Q4 rises, Q4 begins to turn on with a resultant negative voltage excursion at the collector of Q4. The negative voltage is coupled through capacitor C2 to the base of Q3, turning Q3 off. Thus, the circuit is switched to the opposite state. The time that Q4 is held off is determined by the values of R3 and C1. The time that Q3 is held off is determined by the values of R4 and C2. Resistors R3 and R4 are selected at test to obtain the frequency of 1 megacycle and a symmetrical waveform. In an astable multivibrator, it is possible for both sides to turn on simultaneously when power is first applied and for the multivibrator to remain locked-up in this condition. To prevent such an occurrence, an anti-lockup device consisting of transistors Q5 through Q7 is employed. Transistors Q6 and Q7 form an OR gate with inputs from the collectors of Q3 and Q4, respectively. The output of the OR gate is taken from the collectors of Q6 and Q7 and applied to the base of Q5. If transistors Q3 and Q4 are both turned on, Q6 and Q7 are turned off, causing Q5 to turn on. With transistor Q5 turned on, current for Q3 is shunted to ground. With base drive removed, transistor Q3 turns off and astable operation commences. With either Q3 or Q4 turned off, Q6 or Q7 will be on to hold Q5 off. With transistor Q5 off, the anti-lockup circuit has no effect on the multivibrator operation. Diodes



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Figure 60. Coder Module No. 2, Logic Diagram

CR3 and CR4 prevent base-emitter breakdown of Q3 and Q4 when they are in a reverse bias condition. Diodes CR2, CR35, and CR1 are isolation diodes for the anti-lockup circuit. The output of the 1-megacycle oscillator is ac-coupled to a bistable multivibrator. The bistable multivibrator provides a symmetrical output and a 2:1 reduction in frequency. The bistable multivibrator is formed by NPN type switching transistors Q8 and Q9. The 1-mc signal from the astable multivibrator is differentiated and diode-coupled to the base of Q8 and Q9, causing negative triggering of the bistable multivibrator. The 500-kc output is taken from the collector of Q9 and applied through inverter Q10 to drive buffer amplifier Q11. Capacitor C8 is a speedup capacitor so that Q11 is turned on faster. Capacitors C6 and C7 speed up the bistable switching time.

(2) 170-Microsecond Sample Monostable Multivibrator. The sample monostable multivibrator is triggered by the leading edge of the analog encode command or the calibration command. The monostable multivibrator provides 170-microsecond analog sampling period control pulses and a reset pulse to the reset driver circuit.

The monostable multivibrator is formed by transistors Q23 through Q25. In the normal state, Q25 is held on by the base current through R54, and Q24 is held off by base resistor R55 which is clamped to $V_{CE(SAT)}$ of Q25. Capacitor C14 is charged to approximately 6 volts and C13 is approximately zero volts. Transistor Q24 is collector-triggered by the output from Q23, and Q23, which is normally off, is triggered by positive encode or calibrate pulses from the programmer. When Q23 turns on, capacitor C13 begins charging to approximately +6 volts through Q23 and R36. During this charge time (determined by R36 and C13), C13 appears as a short circuit to the collector of Q24 and to capacitor C14. This places -6 volts across diode CR19 and the base-emitter junction of Q25, reverse-biasing both and turning Q25 off. The resultant positive voltage excursions at the collector of Q25 are coupled through resistor R55 to the base of Q24 to turn on Q24. When Q24 turns on, capacitor C14 is grounded, thus holding the reverse-bias condition on Q25 for an interval determined by C14 and R54. Thus, transistor Q23 and capacitor C13 initiate the regenerative action, but after Q24 turns on, the circuit becomes independent of these two elements. When capacitor C14 has charged to V_{BE} of Q25, Q25 turns on and Q24 turns off to return the circuit to its normal state. The positive pulse at the collector of Q25 is applied to the base of Q26 and Q30. Diode CR19 prevents emitter-base breakdown of Q25 when Q25 is operating in the reverse-bias condition.

(3) Code/Calibrate Bistable Multivibrator. The code/calibrate bistable multivibrator (flip-flop) switches the coder between the analog encode and the calibrate mode of operation. The flip-flop is set and reset by the analog encode command and the calibration command, respectively. In the calibration mode, the exclusive OR gate and error correction circuit, plus other associated circuits, are placed in operation. In the encode mode, these circuits are inhibited to allow the coder to function normally.

The flip-flop is formed by transistors Q20 and Q21 and the triggering circuit is formed by transistors Q19 and Q22. For discussion purposes, assume that transistor Q21 is on, Q20 is off and that Q19 and Q22 are normally off. Transistor Q20 is held off because base resistor R45 is clamped to $V_{CE(SAT)}$ of Q21. Transistor Q21 is held on by base

current through resistors R46 and R48. A positive encode pulse through resistor R49 to the base of transistor Q22 turns on Q22. When Q22 saturates, the base current for Q21 is channeled to ground and Q21 is turned off. As the collector of Q21 goes positive, the rising voltage coupled through resistor R45 to the base of Q20, turns on Q20. The base resistor for Q21, resistor R48, is then at $V_{CE(SAT)}$ of Q20 and Q21 is held off and the bistable is in the opposite state. A positive calibrate pulse applied to the base of transistor Q19 will turn on that transistor and repeat the sequence described above with the opposite side of the flip-flop.

(4) Sync Bistable Multivibrator and Counter Gate Control Circuit. The sync bistable multivibrator synchronizes the encoding process initiated by the sample command with the 500-kc bit rate pulses. The leading edge of the sample monostable multivibrator pulse is gated with the 500-kc signal to provide starting synchronism. The trailing edge of the multivibrator pulse is gated with the 500-kc signal to provide sample stop synchronism, thereby eliminating the timing ambiguity present in conventional ramp coders. In addition, the sync bistable multivibrator controls the switches connecting the unity gain buffer amplifier to the analog bus and the ramp capacitor in coder module No. 1.

The sync bistable multivibrator and gating circuits are made up of transistors Q12 through Q16, Q26, Q29, Q30, Q31, Q32, Q33, and Q42. The bistable multivibrator composed of transistors Q14 and Q15 is similar in operation to the 2:1 reduction counter employed in the 500-kc oscillator except that it uses PNP transistors and positive triggering. Transistors Q31 and Q32 are buffers with inputs from the collectors of Q14 and Q15. Transistors Q29 and Q30 are buffers with output levels (+6 volts or PSC) which are the inverse of one another. The outputs of buffers Q29 and Q30 drive the triggering circuits of the bistable multivibrator. Transistor Q26 is an inverter at the output of the sample monostable multivibrator. Transistors Q12, Q42, Q13, Q33, and Q16 make up the counter gate control circuit in which Q12 is the output driver transistor that drives the 10-stage counter in module No. 3. Resistor R28, diode CR7, and resistor R29 form a voltage divider network to decrease the 500-kc signal to the sync bistable multivibrator. Diode CR22 clamps the negative swing on the base of transistor Q33 to about 0.5 volt to prevent base-emitter breakdown. Diodes CR10 and CR34 are also used to prevent base-emitter breakdown.

The counter gate control circuit is inhibited during sample time in the encode or calibrate mode, when a zero-detect pulse occurs in the encode mode, and when an overvoltage pulse occurs in the calibrate or encode modes. During sample time in the calibrate mode, a 170-microsecond pulse from the sample monostable multivibrator turns on transistors Q26 and Q30. When Q26 turns on, transistor Q29 turns off. The collectors of Q29 and Q30 are connected to the triggering circuits of the sync bistable multivibrator. With Q29 turned off, the collector of Q29 is at +6 volts, biasing diode CR8 such that the next positive 500-kc pulse will be routed through CR8 to turn off transistor Q14. This gated pulse provides the starting synchronism for the coder. With transistor Q30 turned on, diode CR9 is biased such that the 500-kc signal is inhibited and transistor Q15 turns on. The output levels of Q31 (signal line KK) and Q32 (signal line JJ) to the sampling switch are -15 volts and +6 volts, respectively. These voltage levels close the sampling switch connecting the unity gain buffer amplifier to the ramp capacitor and the PAM bus. The base of transistor Q13 also obtains current from the collector of Q32, through CR10 and R27, when Q32 is turned on. Transistor Q13

clamps the collector-base junction of Q12 to $V_{CE(SAT)}$ of Q13 and inhibits the 500-kc signal to the counter. After the 170-microsecond pulse from the sample monostable multivibrator has expired, transistors Q26 and Q30 turn off. With transistor Q26 turned off, transistor Q29 is turned on. Under these conditions, the collector of Q30 is at a +6 volt level, biasing CR9 so that the next positive 500-kc pulse is gated to turn Q15 off and provide the sample stop synchronism. The collector of Q29 is at $V_{CE(SAT)}$, biasing CR8 such that the 500-kc signal is inhibited and Q14 turns on. The output levels of Q31 (signal line LL) and Q32 (signal line JJ) to the sampling switch are then +6 volts and -15 volts, respectively. These voltage levels open the sampling switch to disconnect the unity gain buffer amplifier from the ramp capacitor and PAM line and start the encoding cycle. Transistor Q16 is turned on during the calibrate mode and its base drive is derived from the collector of Q20 in the code/calibrate bistable multivibrator during this time. The zero-detect pulse, generated by the level detector in coder module No. 1 when the ramp crosses zero, is routed to the base of transistor Q33 (signal line GG). Because transistor Q16 is on, the base of Q33 is clamped to $V_{CE(SAT)}$ of Q16 and Q33 is held off. The overvoltage pulse is routed through diode CR34 and resistor R98 and applied to the base of transistor Q42 to turn off that transistor. Transistor Q42 then clamps the emitter-collector junction of Q12 to $V_{CE(SAT)}$ of Q42, thus inhibiting the 500-kc signal to the counter. In the encode mode, transistor Q20 removes base drive from transistor Q16, and Q16 is turned off. After the sample and encode cycles have been completed, the zero detect pulse turns on transistor Q33, clamping the base of Q12 to $V_{CE(SAT)}$ of Q33 and again inhibiting the 500-kc signal to the counters.

(5) Exclusive OR Gate With Proportional Control Error Correction Circuit. The exclusive OR gate and correction circuit, formed by transistors Q35 through Q42, charges or discharges compensating capacitor C20 to a voltage proportional to the interval between the zero detect and overvoltage pulses. A full scale voltage (-6.4 volts) on the ramp capacitor should discharge in the amount of time it takes the counter to count to 1023. The overvoltage pulse signal line (CC) originates in module No. 3 and signifies that a count of 1023 has been reached by the 10-stage counter. Capacitor C20 furnishes bias voltage for the FET transistor in the precision current generator located in coder module No. 1. As the voltage across the compensating capacitor increases or decreases, the bias (signal line MM) increases or decreases on the FET transistor and the current to discharge the ramp capacitor increases or decreases. The change in ramp discharge current increases or decreases the ramp discharge time, thus adjusting the time of occurrence of the zero-detect pulse so that the zero-detect pulse and overvoltage pulse are coincident. Because the compensating capacitor charge or discharge time is proportional to the interval between the two pulses, any component aging, voltage or temperature variation, or other related source of error within the feedback loop is eliminated by the proportional control calibration correction. Three calibrate correction cycles are run for each analog input encoded and each correction cycle, after the initial calibration cycle, provides one-half of the corrections necessary in the previous cycle. Thus, a critically damped feedback condition is achieved and, although perfect correction is possible only after an infinite number of correction cycles, the actual error is insignificantly small.

Diodes CR13, CR14, and CR15, and resistors R37 and R38 form a 3-input OR-gate circuit which drives the base of transistor Q35. If Q35 receives an input from one of the three sources, the transistor turns on and the base of Q36 is clamped to $V_{CE(SAT)}$ of Q35

to keep Q36 from turning on. With no input to transistor Q35, transistor Q36 is turned on when a zero detect pulse is received through CR26 and R86. When transistor Q36 turns on, Q37 turns on and charges compensating capacitor C20 through resistor R90. Diodes CR32, CR33, and CR16, and resistors R39, R96, and R97 form a 3-input OR-gate circuit which drives the base of transistor Q41. If Q41 receives an input from one of the three sources, the transistor turns on and the base of Q40 is clamped to $V_{CE(SAT)}$ of Q41 to keep Q40 from turning on. With no input to transistor Q41, transistor Q40 is turned on when an overvoltage pulse is received through diode CR31 and resistor R94. When transistor Q40 turns on, Q39 turns off and Q38 turns on to discharge compensating capacitor C20 through resistor R91.

The signals gated by the OR circuit at the input to transistor Q35 are the code/calibrate bistable multivibrator output received through diode CR15 and resistor R38, the overvoltage pulse received through diode CR13 and resistor R37, and the 170-microsecond pulse from transistor Q27 that is received through diode CR14 and resistor R37. The signals gated by the OR circuit at the input to transistor Q41 are the code/calibrate bistable multivibrator output received through diode CR16 and resistor R39, the zero-detect pulse received through diode CR33 and resistor R97, and the 170-microsecond pulse from transistor Q27 received through diode CR32 and resistor R96.

During encode time the exclusive OR gate and correction circuit is inhibited by an output of the code/calibrate bistable multivibrator. An encode pulse turns off transistor Q21 and its collector rises to a positive level. The positive voltage level from transistor Q21 turns on transistors Q35 and Q41 to inhibit further operation of the correction circuit. During calibrate time, the first calibrate pulse changes the state of the code/calibrate bistable multivibrator, thus turning on transistor Q21 and removing base drive from transistors Q35 and Q41. With Q35 and Q41 turned off, the correction circuit is enabled. The first 170-microseconds after the calibrate pulse is sample time. The 170-microsecond monostable multivibrator develops a positive pulse to turn on inverter Q26 which turns off buffer amplifier Q27. The positive level from the collector of Q27 to the OR-gate turns on transistors Q35 and Q41, thus inhibiting the correction circuit. At the end of the 170-microsecond pulse, Q27 turns on and removes the base drive to transistors Q35 and Q41, thereby turning off these transistors and making the correction circuit again ready for use. The calibration circuit operates under three possible conditions. If the coding ramp is too short, the zero-detect pulse arrives before the overvoltage pulse. If the ramp is too long, the overvoltage pulse arrives before the zero-detect pulse. If there is no need for correction, the overvoltage and zero-detect pulse are coincident.

When the ramp is too short, the zero-detect pulse to the bases of transistors Q36 and Q41 turns on the transistors. With Q36 turned on, Q37 is turned on to charge capacitor C20 toward +15 volts. Transistor Q41 inhibits Q40 so that when the overvoltage pulse arrives, transistor Q40 cannot turn on. The overvoltage pulse is also routed through the OR circuit to the base of transistor Q35, and Q35 is turned on. With Q35 turned on, the base of Q36 is clamped to $V_{CE(SAT)}$ of Q35 and Q36 is turned off to stop the charging of capacitor C20.

When the ramp is too long, the overvoltage pulse to the bases of transistors Q35 and Q40 turns on the transistors. With Q40 turned on, Q38 is turned on to discharge

capacitor C20 through resistor R91. The base of transistor Q36 is clamped to $V_{CE(SAT)}$ of Q35 and, when the zero-detect pulse arrives, transistor Q36 cannot turn on. The zero-detect pulse is also routed through the OR circuit to the base of transistor Q41, and Q41 is turned on. With Q41 turned on, the base of Q40 is clamped to $V_{CE(SAT)}$ of Q41 and Q40 is turned off to stop the discharge of capacitor C20. If no correction is required, the zero-detect pulse and over-voltage pulse are coincident, and transistors Q35 and Q41 are turned on to inhibit operation of the correction circuit.

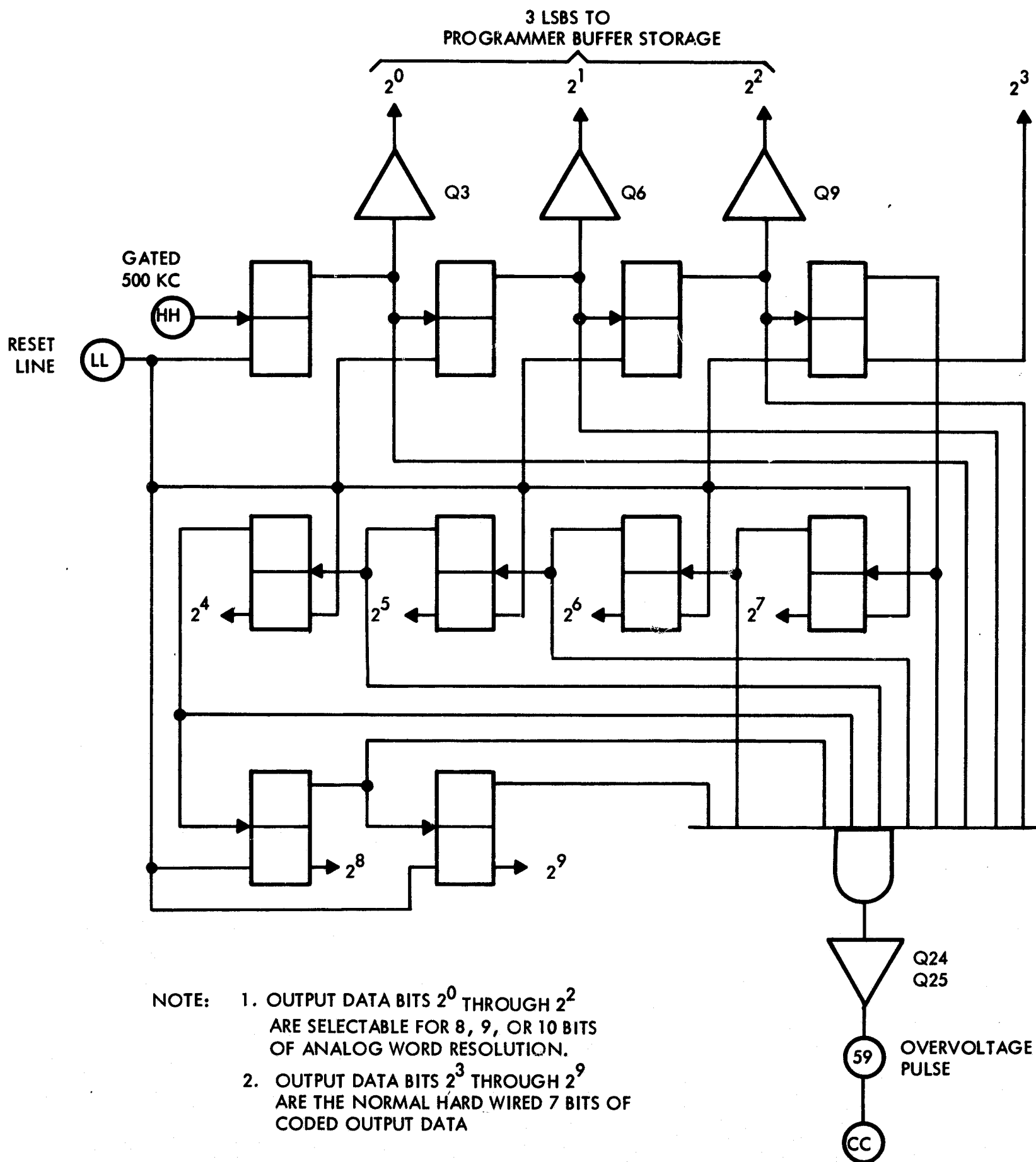
(6) MOS Command Circuit. The MOS command circuit generates gate signals to the MOS gate in coder module 1 during calibrate times to gate the precision reference voltage onto the PAM bus. The command circuit is formed by transistors Q17 and Q18. Positive calibrate pulses through resistor R41 are routed to the base of transistor Q18 and Q18 is turned on. When Q18 turns on, Q17 also turns on to develop a positive pulse to the MOS-driver (signal line FF) in coder module 1.

(7) Reset Circuit. The reset is formed by transistors Q34, Q43, and Q28 and develops reset pulses to the 10-stage counter in coder module 3 to reset the counter at the start of calibrate and encode cycles. The 170-microsecond sample monostable multivibrator pulse turns on inverter Q26, causing transistor Q27 to turn off. The voltage at the collector of Q27 is coupled through resistor R75 to the base of Q43 and Q43 is turned on. The collector of Q43 is coupled through resistor R78 to the base of Q34 and the NPN-PNP combination results in transistor Q34 being turned on when Q43 is on. The collector of Q34 is coupled through resistor R76 to the base of Q28 and, when Q34 is turned on, Q28 is also turned on. The voltage at the collector of Q28 is routed to module three at (signal line LL). The output on signal line LL is a zero to -7-volt pulse.

c. Coder Module No. 3. Refer to coder module No. 3 logic diagram, figure 61, and schematic diagram, figure I-23. This module contains a 10-stage counter and a 10-input AND gate.

(1) 10-Stage Counter. Transistors Q1 through Q23 are NPN transistors which form a 10-stage counter that employs saturated stages and ac coupling. The last seven stages of the counter are identical, but the first three stages are slightly different in that each of the first three stages drives a buffer amplifier. The counter operates between -6 volts and PSC. The 500-kc trigger pulses are differentiated and diode-coupled to the base of the first bistable multivibrator, causing negative triggering of the first stage. The other stages are coupled and triggered in the same manner. The counter receives a dc reset pulse at the beginning of every encode or calibrate cycle. Transistors Q3, Q6, and Q9 function as buffers to isolate the 2⁰, 2¹, 2² stages from their loads.

(2) Overvoltage Circuit. The overvoltage condition is detected by a 10-input AND gate formed by diodes CR3, CR8, CR13, CR18, CR22, CR26, CR30, CR34, CR38, and CR42. Inputs to the AND gate are from the 10-stage counter. When each of the ten stages of the counter are in the ONE state (count 1023), the AND gate develops a positive pulse through diode CR44 and resistor R67 to the base of transistor Q24. The positive pulse turns on transistor Q24 to clamp the base of Q25 negative level, to turn off Q25. Zener



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Figure 61. Coder Module No. 3, Logic Diagram

diode CR45 provides DC level shifting between transistors Q24 and Q25. Diode CR44 is included in the AND gate circuit to provide an energy gap, thereby ensuring that Q24 turns off. The diode also prevents base-emitter breakdown of Q24 when the transistor is in the reverse-bias condition. The positive pulse output of the overvoltage circuit is routed through connector pins 59 and 60 to coder module No. 2.

2.3.1.6 OUTPUT REGISTER AND SPLIT-PHASE CONVERTER.

2.3.1.6.1 GENERAL. The output register and NRZ-to-split-phase converter are located in one module. Because block redundancy is employed, there are two of these modules in each PCM unit, with only one module operating at a time.

2.3.1.6.2 BLOCK DIAGRAM DESCRIPTION. Refer to the output register and split-phase converter block diagram, figure 62. The shift register receives eight parallel read-in data bits from the digital multiplexer that provides the 8-bit data word. After the parallel read-in data has been loaded by the 15-microsecond strobe command, the shift line serially shifts the data out as NRZ code at a 500-cps bit rate. The NRZ code is then converted to split-phase mark 0 such that a continuous series of ONE's appears as a square wave at bit rate, and a continuous string of ZERO's appears as a square wave at one half the bit rate. The output ZERO bits are phase-shifted, while the ONE bits are not. A transition occurs in the middle of all bits (ONE's or ZERO's) and a transition occurs at the beginning of all ONE bits (but not ZERO bits).

The split-phase converter output is applied to three output drivers. One driver routes the REAL TIME PCM data to the TME unit, and the other drivers furnish two outputs each that provide the two phases of the output data to the record amplifiers in the TME unit. The two record amplifiers are driven in parallel through separate isolation resistors so that shorting one output line to PSC will not affect data to the second recorder. In addition the five output lines are connected to the five output lines of the other output register module to achieve block redundancy while using one set of output wires. To provide fail-safe operation in event of a single failure, resistors are used for the record amplifier signals, while a diode was added to the REAL TIME driver of the PCM.

The output register and split-phase converter module also contains the 500-cps buffer amplifier for CY500 from the clock. This buffer amplifier produces both phases of the 500-cps signal. One phase is used to operate the countdown flip-flops and shift register, and both phases are used for logic gating commands to the programmer and to generate the split-phase code.

2.3.1.6.3 DETAILED DESCRIPTION. Refer to the output register and split-phase converter logic diagram, figure 63, and schematic diagram, figure I-24. The output shift register and split-phase converter module consists of the output shift register, the 500-cps buffer, and the NRZ-to-split-phase converter.

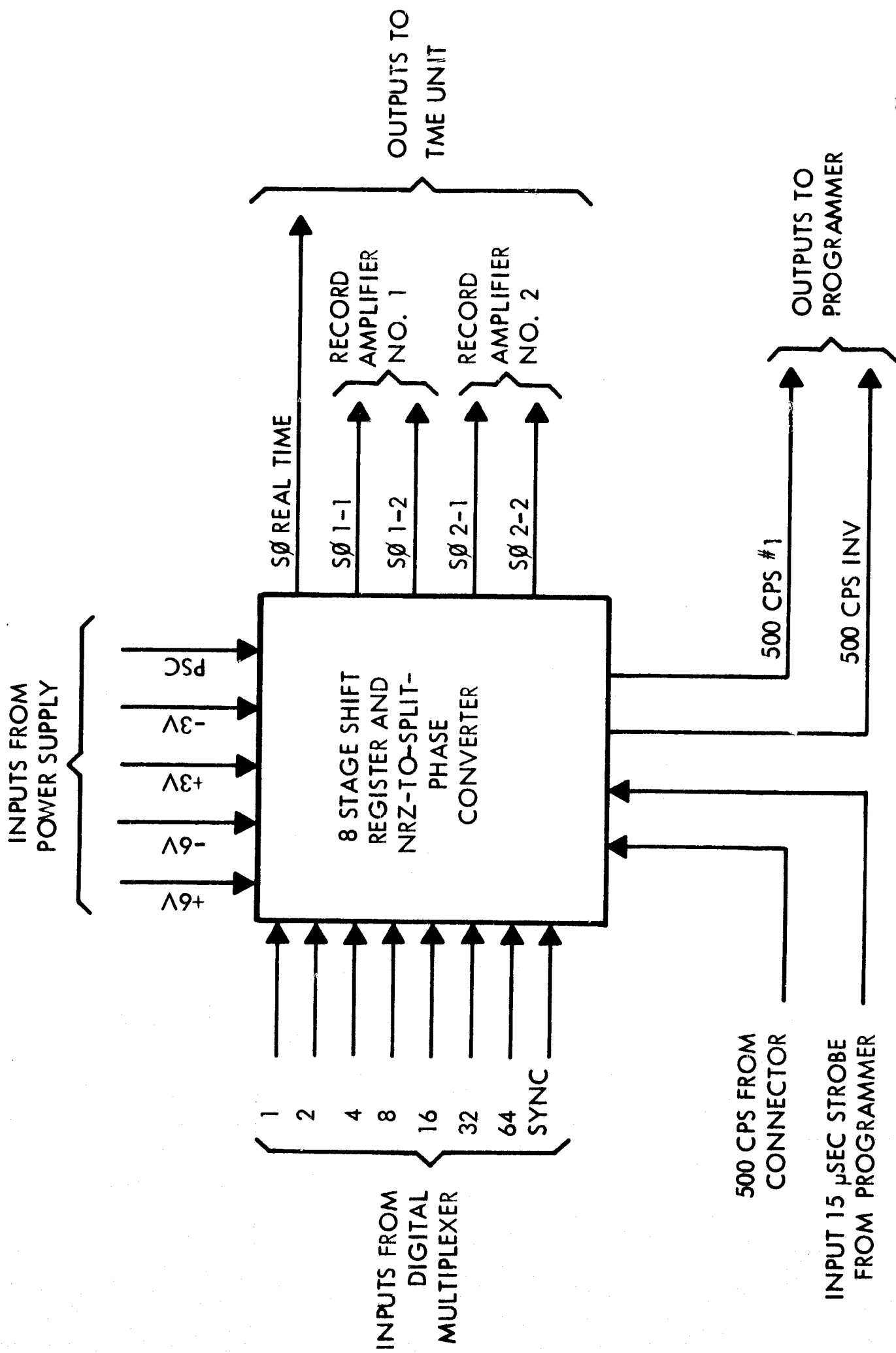


Figure 62. Output Register and Split-Phase Converter, Simplified Block Diagram

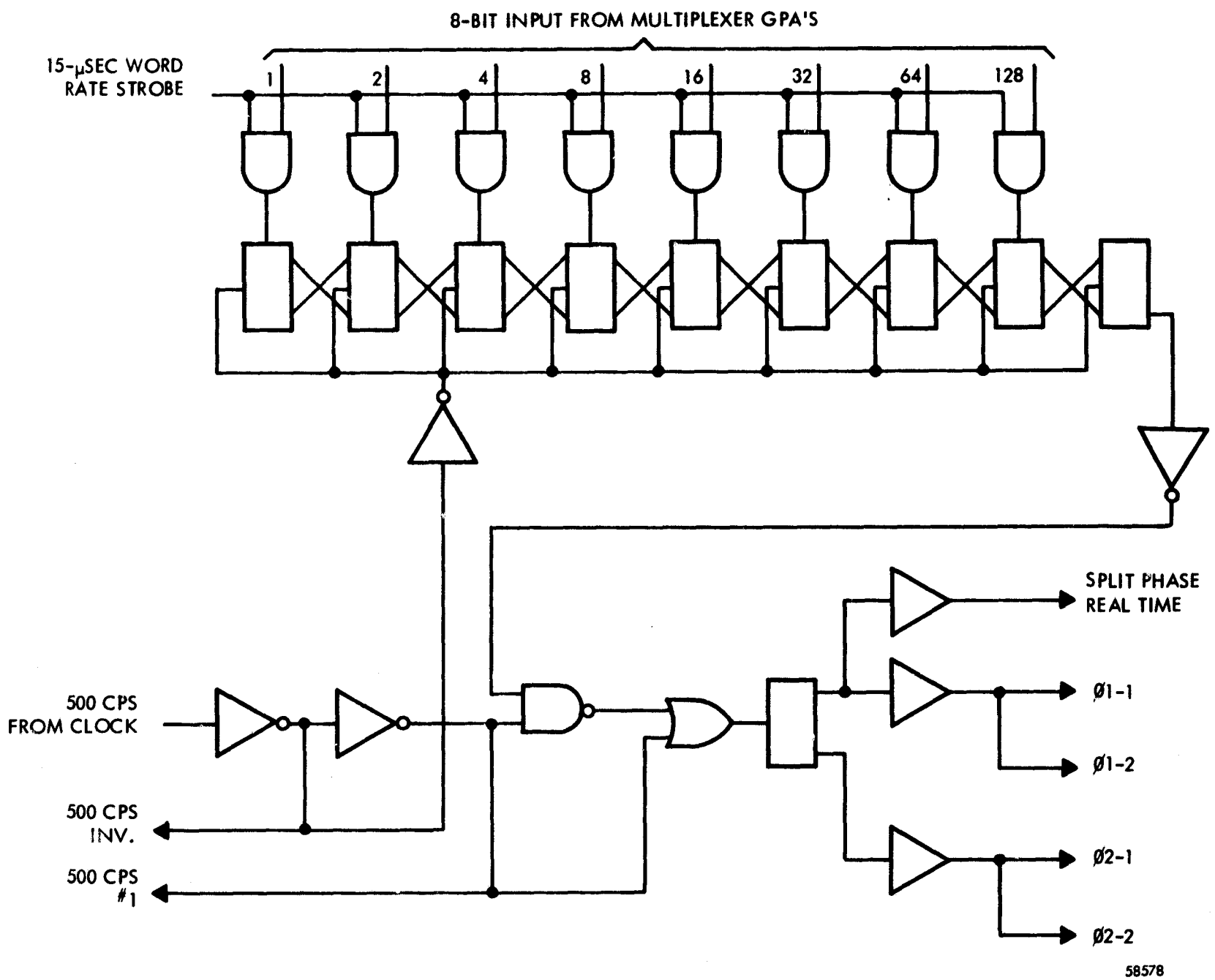


Figure 63. Output Register and Split-Phase Converter, Logic Diagram

a. Output Shift Register. The PNP type transistors, Q1 through Q16, Q26, and Q27, form a 9-stage shift register that uses saturated stages and direct-coupled transfer through steering resistors. The first eight stages of the shift register are identical. The last stage, in conjunction with transistor Q28, is designed to drive the split-phase converter. The shift register stages operate between -6 volts and -3 volts. Data is set into the shift register through diode gates CR28 through CR43. The diode gates operate only when strobed by the 15-microsecond pulse generator in the programmer. Data is shifted out of the register at a 500-cps rate.

The 500-cps shift pulses to the output shift register module from the Nimbus clock are buffered by transistors Q17, Q18, Q19, Q31, Q20, and Q21. Transistors Q17 and Q18 shift the input level and route the proper phase and amplitude of the clock signal to transistor Q31. Transistor Q31 drives transistors Q19, Q20, and Q21. The output of transistor Q19 is the 500-CPS INV. signal and the output of transistor Q20 is the 500-CPS #1 signal. Transistor Q21 is a special driver for the shift line to the shift register.

b. NRZ-To-Split-Phase Converter. The NRZ-to-split-phase converter is made up of NPN type transistors. Transistors Q23 and Q24 form the NRZ-to-split-phase bistable multivibrator, the outputs of which are routed to buffers Q25, Q29, and Q30. The 500-CPS #1 signal from transistor Q20 is differentiated and diode-coupled to the bases of the NRZ-to-split-phase bistable multivibrator transistors. The differentiating and coupling network is formed by CR21, CR22, R72, R73, C19, C20 and provides negative triggering of the bistable multivibrator. Diodes CR17, CR18, and CR23 and transistor Q22 form an AND gate and buffer that provides an output that is differentiated and diode-coupled output to the bases of the NRZ-to-split-phase bistable multivibrator transistors. The differentiation and diode-coupling is accomplished by CR20, CR19, R71, R74, C17, and C18. Inputs to the AND gate are from shift register buffer transistor Q28 and from 500-CPS #1 buffer transistor Q20. The combination of inputs to the NRZ-to-split-phase bistable multivibrator causes a change of phase at the beginning of a ZERO but not at the beginning of a ONE. In the middle of all ONE's and ZERO's, a change of state takes place. The resultant output is termed biphasic mark 0 code.

2.3.2 TELEMETRY ELECTRONICS UNIT

2.3.2.1 GENERAL. The Telemetry Electronics Unit (TME) amplifies, records, and plays back input data signals. The TME consists of two record amplifiers, two playback amplifiers, two summing amplifiers, signal monitor circuits, control relays, gain controls and Zener diode, one coaxial connector, two 61-pin connector, one 85-pin connector, and one 9-pin connector. Refer to the TME block diagram, figure I-25 and schematic, figure I-26.

When channel 1 and channel 2 are commanded off, power is removed from all circuits of the TME unit, and power is removed from the PCM unit and from both tape recorders. When either channel is commanded on, power is also applied to the selected PCM unit. Continuous power is applied to both summing amplifiers when either channel is commanded on. When channel 1 is commanded on, power is applied to record amplifier 1 and record motor 1 or to playback amplifier 1 and playback motor 1. When channel 2 is commanded on, power is applied to record amplifier 2 and record motor 2 or playback amplifier 2 and playback motor 2. During launch of the Nimbus Rocket Vehicle, both of the recorders will be operated in the record mode to record launch data.

When both channels are commanded on in the record mode, the split-phase mark zero data from the selected PCM unit will be applied through both record amplifiers to both tape recorders. At the same time, the split-phase mark zero data in real time can be mixed with the 10-kc pulse width modulated time code and then applied to the selected summing amplifier. If the PCM data is not desired, the 10-kc time code alone can be selected to modulate the transmitter. (Modulation of transmitter by PCM data only cannot be selected.) In an emergency, the time code can be selected to bypass the normal playback interlocks to mix with the playback data if either of the recorders has been commanded to the playback mode. The interlocks are present to automatically remove the 10-kc time code beacon when either recorder is commanded to playback. The recorder playback commands are interlocked so that only one recorder at a time can be commanded to play back. For example, if recorder 1 is commanded to play back data, recorder 2 cannot be commanded to play back until after recorder 1 has been commanded to the record mode (either manually or automatically). The interlock is included because the data would be lost if both recorders were to play back data at the same time.

NOTE

The playback interlock will not be included in the Nimbus B flight models.

Since there are two summing amplifiers, two record amplifiers, two playback amplifiers, two tape recorders, two transmitters (and essentially two PCM units), the entire TME electronics is completely block redundant, except for the relays. However, the relays have a high reliability number, or probability of success (very low failure rate), and a relay failure, rather than a failure in the complex electronics, is unlikely. If a relay should fail, it would, in all probability, only limit the TME to one complete channel instead of the two it normally has. Compared with the PCM electronics, the TME electronics are relatively simple and TME failure is much less likely than PCM failure. (The TME has only four electronic modules while

the PCM has 16 electronic modules plus 708 integrated circuit packages.) Even with the low probability of failure, the TME electronics have been made completely block redundant.

2.3.2.2 RECORD AMPLIFIER

The two record amplifiers are contained in separate modules with each record amplifier packaged with one of the playback amplifiers. Thus, there are two identical record/playback amplifier modules.

Refer to the record and playback amplifiers schematic diagram, figure 1-27. Each record amplifier is driven from a separate isolated source in the PCM unit to achieve maximum isolation and redundancy. The PCM output circuit contains buffer amplifiers or drivers that isolate the NRZ-to-split-phase code flip-flop from the load. Since the PCM output circuit is a flip-flop, all that is required for saturated digital recording is switching transistor gates at the output of the flip-flop to switch the current in alternate directions through the record head. The record amplifier circuit consists of two transistor switches and two transistor current sinks, with one switch and sink for each direction of current flow. The current sinks provide a constant record current of 3.8 milliamperes through the record winding. The maximum record frequency is the PCM bit rate of 500 cps and occurs when the data is all ONE's. The minimum record frequency is 1/2 bit rate or 250 cps and occurs when the data is all ZERO's.

The record amplifier receives both phases of the split-phase signal. Each phase is applied to an input gate transistor. When a gate transistor receives a negative input, that transistor saturates and supplies base drive to the associated current sink, thereby providing a current path through the record winding. When one gate transistor is saturated, the other gate transistor and current sink are held off. When the phase of the signal changes, the other gate transistor and current sink operate to switch current through the winding in the reverse direction.

2.3.2.3 PLAYBACK AMPLIFIER. Refer to the record and playback amplifiers schematic diagram, figure 1-27. Both the record and playback amplifiers use the same tape recorder head winding. The winding is relay-switched to the desired amplifier. As the winding is switched to desired amplifier, a second relay, operating in parallel, applies -24.5 volts to the desired amplifier. Thus, the unused amplifier is not connected to -24.5 volts nor to the record/playback winding. The playback amplifier data input frequency is 30 times that of the record frequency (the playback motor operates the tape 30 times faster than the record motor). Therefore, the maximum playback frequency (all ONE's) is 15 kc and the minimum frequency (all ZERO's) is 7.5 kc. The playback amplifier consists of successive gain, compensation, differentiating, and squaring stages to provide constant amplitude stable data to the summing amplifier. A gain monitor point for channel 1 is located at pin 59 of front panel connector J3. Pin 54 of J3 is the gain monitor point for channel 2. Gain adjustment potentiometer A2R4 (channel 1) and A2R5 (channel 2) are adjusted to provide 8-volt peak-to-peak signals at the monitor points. In normal operation, the record amplifier records data on the tape recorder for approximately 90 minutes and the playback amplifier then plays back this data for approximately 3 minutes. After playback, the recorder automatically switches all circuits back to the record mode.

The playback amplifier consists of a differential input stage, a variable gain stage, a differentiator, and a zero crossover detector squaring circuit. The input to the differential stage is 40 millivolts at 7.5 kc. The variable gain stage is adjusted to provide an 8-volt peak-to-peak output that is differentiated and capacitively-coupled to the detector squaring circuit. Two select-at-test resistors, R21 and R37, adjust the crossover detection point so that a symmetrical square wave is generated. A third select-at-test resistor, R39, provides a precision output level to the summing amplifier.

2.3.2.4 SUMMING AMPLIFIER. The two summing amplifiers are conventional operational amplifiers and are contained in one module. The -24.5-volt power line is connected to both amplifiers in parallel, and complete signal or redundancy isolation is achieved by relay switching both the inputs and the outputs. Thus, only one amplifier at a time can be connected between the summing junction and the coaxial cable to the transmitter. The summing junction functions under relay control to present any one of the following signals to the amplifier: (1) 10-kc modulated time code, (2) 10-kc modulated time code mixed with real time PCM split-phase data, (3) playback of recorded data from channel 1 recorder, (4) playback of recorded data from channel 2 recorder, and (5) emergency by pass 10-kc modulated time code plus playback data from either recorder if the playback mode is commanded (this function bypasses the record interlock relay contacts in the event of a relay failure).

Each of the circuits that develop the above signals includes an adjustment potentiometer to control the output signal amplitude to the transmitter. Time code emergency bypass data is controlled by A2R3, time code normal data is controlled by A2R1, PCM real time data to be mixed with the time code is controlled by A2R2, channel 1 playback data is controlled by A2R4, and channel 2 playback data is controlled by A2R5. When mixing time code and PCM real time data, the time code amplitude to the summing network is halved through relay contacts and a precision voltage divider. Thus, the time code and PCM real time data each contribute one-half of the total signal amplitude to the summing junction.

The voltage from the playback amplifiers to the summing junction is controlled by select-at-test resistors in the output circuit of the playback amplifier. These resistors are selected during module testing and cannot be changed after assembly. The playback amplifier gain control potentiometers are used to vary the gain of the playback amplifier to compensate for manufacturing tolerances in the various tape recorders used. Thus, a fixed 8-volt peak-to-peak signal can be applied to the shaping circuits to optimize the signal and minimize pulse width variations to reduce bit width jitter. The resultant jitter caused by the playback amplifier then becomes negligible compared to the tape recorder jitter, and small when compared with the possible bit-rate alternation variations between phases of the 500-cps bit-rate. The 500-cps bit-rate square wave alternations are within $50 \pm 3\%$ of the total cycle, as specified in the Nimbus C clock manual. One alternation can, therefore, have a maximum pulse width of 1 millisecond +1.5% (1,015 microseconds) and the other alternation can have a minimum pulse width of 1 millisecond -1.5% (985 microseconds). This initial unbalance of 30 microseconds is large compared to the approximately 5 microsecond jitter caused by the playback amplifiers.

The summing amplifier module contains two identical operational amplifiers (refer to the summing amplifier schematic diagram, figure I-28. Either of these amplifiers can be selected as the output summing amplifier for the TME unit. Amplifier selection is accomplished

by relay switching the input of the amplifier to the combining resistor network, and simultaneously switching the output of the amplifier to the transmitter input cable. The amplifiers, when connected to the input combining network, perform the summing function for the various input signals. The amplifiers also provide gain adjustment for each signal without affecting the gain settings of the other inputs. The gain is controlled by adjusting the resistance of the input resistor in the combining network.

The amplifier consists of a double-ended input stage, a PNP stage, and an emitter-follower output stage. The input stage is balanced and compensated for temperature variations with the current sink. The two series diodes provide compensation for the amplifier by tracking the base-emitter junction of the current sink transistor and the base-emitter junction of the PNP stage. The positive input of the amplifier is biased at -12 volts and is held at ac ground by a 22-microfarad capacitor. The negative input of the amplifier is connected to the 6.19-K feedback resistor, and with no input present, the amplifier functions as a unity-gain buffer for the voltage at the positive input. When the amplifier is connected to the combining network, the amplifier gain is determined by the ratio of the feedback resistor to the input resistor. The amplifier has an open loop gain of 3000, which begins a 20 db/decade rolloff at approximately 20 kc. The output resistance of the amplifier is less than 300 ohms.

2.3.2.5 SIGNAL MONITOR CIRCUITS. Refer to the monitor schematic diagram, figure I-29. The signal monitor circuits consist of one temperature sensor monitor circuit and four identical voltage divider circuits, all contained within a single module. The temperature sensor circuit can be connected to any one of the PCM analog channel inputs to provide TME internal temperature data. However, the circuit will provide this data only when an external supply voltage is applied to the circuit through an external relay. The four identical voltage dividers provide a 39K resistance to ground to represent a digital channel logic ZERO. A logic ONE is developed when a relay closes to apply -24.5 volts through a series 120K resistor to the 39K resistor. Thus, the ONE monitor point voltage is approximately -6 volts. The following four commands can be monitored if the four monitor points are connected to PCM digital channel inputs: (1) channel 1, power on, (2) channel 2, power on, (3) recorder 1, record mode, and (4) recorder 2, record mode.

2.3.2.6 CONTROL RELAYS. The 18 control relays are mounted on two printed circuit cards containing nine relays per card. All relay coils (or parallel relay coils) contain 2 parallel diodes in series with the input command voltage and another 2 diodes connected in series across the coil. The diodes provide isolation and reduce noise generation. All 18 relays have DPDT contacts with 14 relays having magnetic latching with two separate command coils (relay operates like a set-reset flip-flop). The remaining four relays are non-latching (standard) relays with one command coil. The non-latching relays are used to drive four parallel latching relay coils. The relays are connected in this manner to reduce the total load on the Nimbus C clock command circuits.

Refer to the TME unit schematic diagram, figure I-26. The 14 latching relays have a dc coil resistance of 230 ohms, and the four non-latching relays have a dc coil resistance of 210 ohms. All relays operate with a nominal 12 volts and the DPDT contacts are rated at 3 amperes, dc. Two parallel resistors are connected in series with the command voltage to reduce the drive to the relays that are energized directly from the -24.5-volt power line. Since the tape recorder automatically switches the relays back to the record mode after three

minutes in the playback mode, the two non-latching record command relays provide signal isolation between the Nimbus C clock record command and the tape recorder record command. The isolation is necessary for proper operation of the clock output circuits.

The following command signals control the relays and perform all TME and PCM switching functions:

- Channel No. 1 - Power ON
- Channel No. 1 - Power OFF
- Channel No. 2 - Power ON
- Channel No. 2 - Power OFF
- Recorder No. 1 - Record
- Recorder No. 1 - Playback
- Recorder No. 2 - Record
- Recorder No. 2 - Playback
- Summing Amplifier No. 1 ON - No. 2 OFF
- Summing Amplifier No. 1 OFF - No. 2 ON
- PCM Power No. 1 ON - No. 2 OFF
- PCM Power No. 1 OFF - No. 2 ON
- Time Code Normal
- Time Code Bypass
- Time Code ON - PCM Real Time OFF
- Time Code ON - PCM Real Time ON

2.3.2.7 ZENER DIODE AND GAIN CONTROLS. A power Zener diode, two 5K potentiometers, and three 10K potentiometers are mounted on the front panel of the TME unit. The potentiometers are all single-turn (270°) type with adjustment controls external to the TME unit.

The 10-watt Zener diode performs a clamping function for fault voltage protection at the outputs of the analog and digital input channel gates in the PCM unit (refer to the TME unit schematic diagram, figure I-26). The Zener voltage is approximately -17 volts which limits the input negative voltage to the multiplexer final sequencers. The limiter prevents failure of output circuits of the analog (or digital) multiplexer which could result in failure of the entire multiplexer such that an entire PCM function could be lost. Thus, the Zener diode clamp circuit provides fail-safe operation for fault voltages up to -24 volts even under worst case conditions such as an input to output short. The Zener diode operates in parallel with slightly higher-voltage Zener diodes in the PCM. Thus, the PCM unit is protected against fault voltages even when disconnected from the TME; however, the Zener located in the TME provides maximum protection with several multiplexer failures, requiring power dissipation beyond the capabilities of the small micro-zener diodes in the PCM unit.

2.3.2.8 CONNECTORS. J1 is a coaxial connector, J2 and J3 are 61-pin Deutsch connectors, J4 is an 85-pin Deutsch connector, and J5 is a 9-pin Cannon connector. J1 connects the outputs of either summing amplifier to either transmitter, through one coaxial cable. J2 is connected to the Nimbus power supply, J3 is connected to the Nimbus clock, J4 is connected to the PCM and two tape recorders, and J9 is for monitor points only.

The coaxial cable connected to J1 is not terminated in its characteristic impedance as the source impedance is approximately 300 ohms and the load impedance is approximately 75K. Thus, the coaxial cable is simply a shielded wire, with the shield connected to the TME case or chassis ground.

Extra pads are provided on the printed circuit boards inside the TME unit to provide redundant pins for connector J4. It is desirable to use the TME box for a tie point or junction box for the 100 cps signal, YB1, as this signal is used both by tape recorder 1 and the PCM. Since the tape recorders are already fabricated for the Nimbus B program, they cannot be used and the Nimbus C clock presents only a single interface pin. Thus YB1-1 is connected to the TME connector on one pin (J3-pin 45) and this pin is connected through card pads to two pins on J4. One of these pins (J4 pin 77) is connected to the PCM while another (J4 pin 83) is connected to tape recorder 1. Connector J2 has 40% spare pins, J3 has approximately 12% spare pins, J4 has approximately 7% spare pins, and J5 has 1 spare pin.

2.3.3 BENCH TEST EQUIPMENT

2.3.3.1 GENERAL. The bench test equipment (BTE) provides all of the electronics and switches necessary to simulate Nimbus C clock commands and clock frequencies for proper operation of the Nimbus Study PCM and TME, plus the 100 cps (YAI and YBI) necessary to operate the tape recorders. (Refer to the BTE tool drawings that have been supplied separately.) Closed circuit phone jacks are also provided to individually control all analog and digital channels. The BTE provides the circuits and functions listed below.

- a. 21 closed circuit jacks for prime analog channels.
- b. 63 closed circuit jacks for prime digital channels.
- c. 434 closed circuits jacks for subcom analog channels.
- d. 280 closed circuit jacks for subcom digital channels.
- e. 30 closed circuit jacks for monitor points.
- f. 20 switches to control the time code MO and MM10A.
- g. 14 switches to control the upper and lower limits for analog word accuracy.
- h. Eight switches to control the TME relays.
- i. One rotary switch to control six modes of operation.
- j. One toggle switch to provide a seventh mode of operation.
- k. Eight bit switches to route simulated word data into the TME (not required for demonstration).
- l. One toggle switch to control the test set 10kc time code to the TME.

- m. Six toggle switches to select any word out of 62.5.
- n. Four toggle switches to select any word out of 16 subframes (used in conjunction with the six word select switches).
- o. One rotary switch to select either PCM real time or test real time.
- p. One toggle switch to select PCM power on or PCM power off.
- q. One toggle switch to connect the line current monitor meter to PCM 1 or PCM 2.
- r. 500 cps (CY500), 100 cps (YAI and YBI), 10 cps (CY10), 1 cps (CY1A), and time code (MO and MM10A).
- s. One toggle switch to select manual or automatic tape recorder mode.
- t. One toggle switch to select prime or subcom rate for oscilloscope sync.

2.3.3.2 DETAILED DESCRIPTION. The BTE functions in six modes of operation. Mode 1 provides a manual check of any selected word, mode 2 provides an automatic check of all channels, mode 3 performs an automatic check on all subcom channels, mode 4 performs an automatic check on all prime channels, mode 5 provides a coder linearity check on all channels, and mode 6 performs a digital channel check.

The test set consists of a split-phase-to-NRZ converter, counters for bit, word, and subframe information, shift-registers for sync, data, and ID count, a comparator, and reset circuits. The split-phase-to-NRZ converter processes the 600-millivolt signal from the TME to develop an NRZ code usable by the test set. The input data triggers a 75-percent monostable multivibrator, which then triggers a 50-percent monostable multivibrator. The 50-percent monostable multivibrator generates bit-rate for the test set. Outputs of the two multivibrators are ANDed with incoming data to develop NRZ ONE's and ZERO's. The final output is derived from a shift-register stage which is driven by a flip-flop circuit.

The test set contains three counters and three shift registers. The first three flip-flops are connected to form an 8:1 bit counter. The next six flip-flops form a 62.5:1 word counter and the last four flip-flops form a 16:1 subframe counter. The three shift registers in the test set are a 16-stage sync shift register, an 8-stage data shift register, and a 4-stage subframe ID shift register. The serial data stream is continuously shifted through the 16-stage sync shift register. This shift-register provides parallel outputs to a 16-input AND gate which develops a half bit-period pulse upon detection of the PCM 16 bit sync code. When the sync code is detected, the counters are set to bit 5, word 2.

The 4-stage subframe ID shift-register receives four shift pulses per subframe during the last 4 bits of word 2. This shift register provides parallel outputs to an AND gate that detects the count for subframe 16. A fifth input to this AND gate is from a 200-microsecond monostable multivibrator that is triggered by the trailing edge of the output from the sync AND gate. Thus, the AND gate develops a single 200-microsecond reset pulse at the start of word 3 in subframe 16.

The 8-stage data shift-register provides outputs to the comparator circuit and to the console indicator lights. The comparator output is normally + 6 volts. If the data in the shift-register is above the upper limit or below the lower limit of the front panel switches, a 200-microsecond PSC pulse is developed by the comparator. The comparator is not strobed during sync words or digital channel time slots and no comparator outputs are developed at those times.

The last shift pulse to the data shift-register is received coincident with the beginning of the next word. Thus, the data for word 47 is not entirely in the data shift-register until the beginning of word 48. With the test set operating in one of the automatic modes with no errors, a comparator strobe is developed every eight shift pulses. New data begins to enter the register with the ninth shift pulse and the comparator strobe time must, therefore, be between the eighth and ninth bits. The strobe time was set in the middle of this time interval (1 millisecond after the beginning of each word).

During automatic modes 2, 3, and 4, the comparator strobe toggles the error flip-flop upon detection of an error. When the error flip-flop is toggled, the 500-cps signal to the PCM is interrupted to hold the PCM at the word containing the error, and bit-rate to the test set counters is interrupted. The error flip-flop is reset to the go condition when the reset push-button on the front panel is depressed.

Mode 5 is used primarily to provide a visual check of coder linearity. The error flip-flop is also functional in this mode, but is disconnected from the gate controlling bit rate to the counters. During this mode, the error flip-flop is toggled to the no-go state for the duration of a word that is in error and is then reset to the go state for the next word. Switching points are determined by observing voltage levels required to completely change bits. The red and green indicators on the front panel provide an indication of the state of the error flip-flop.

One of the commands used by the BTE in modes 5 and 6 is the overvoltage pulse produced by the PCM coder approximately 1 millisecond before the word is shifted out of the PCM output shift register. The command must be held in memory for 18 milliseconds because of the following delay times: (1) a one-millisecond delay between the time data is shifted out of the shift register and the time the data appears at the output of the split-phase-to-NRZ converter, (2) a one-millisecond delay after the beginning of the next word and after the data is in the data shift-register to occurrence of the test set strobe to the comparator, and (3) a 16-millisecond delay during the eight shift pulses required to shift a complete word into the data shift register.

During normal operation the AD flip-flop is continuously reset to the go state by pulses which occur approximately 2 milliseconds after the beginning of each word. The 2-millisecond delay is to overlap the time of the comparator strobe. If an error occurs, the leading edge of the overvoltage pulse sets the AD flip-flop to the no go state and the trailing edge triggers a four-millisecond monostable multivibrator. The resultant 4-millisecond pulse inhibits a gate to override the AD flip-flop reset pulse. However, the flip-flop is again reset to the go state at the beginning of the following word.

An inhibit gate is used when it is required to override the comparator, such as during sync words or digital channels. A gate that detects words 1 and 2 provides an inhibit output to this gate. However, the compare strobe for word 2 occurs 1 millisecond

after the start of word 3. The trailing edge of the output of the W1-W2 AND gate triggers a 2-millisecond monostable multivibrator that develops an output to override the word 2 compare strobe.

During normal operation, the error flip-flop is reset to the go state during the middle of each word by a reset pulse that is received through a gate that also has inhibit and B-O signal inputs. If the comparator detects an error, the reset pulse is inhibited. Because the compare pulse occurs 1 millisecond after the beginning of a word and the reset to the flip-flop occurs at the middle of the word (or after 5 milliseconds), an overlap is developed to prevent the reset for that one word. The C-O signal, in addition to the output of the 4-millisecond multivibrator, is applied to the inhibit line to ensure that the reset pulse occurs only during the last half of the word. At the next word, the flip-flop is again returned to the go state.

NOTE

The time code time slots are not inhibited during the automatic compare mode and the test set cycles a maximum of one major frame (16 seconds) and then stops. The Nimbus B test sets will be corrected such that continuous operation results when all channels operate within the limits set into the limit switches.

2.3.4 GROUND STATION MODIFICATION.

Modifications to PCM Ground Station System 2 include: (a) addition of a Radiation 5220A bit synchronizer to provide improved signal-to-noise performance; (b) modification of the group synchronizer to permit synchronization with a longer and more uniquely coded sync pattern and to permit operation at the revised words/frame format; (c) modification of the decommutator and incorporation of a new digital decommutator to provide on/off and time code decommutation capability; (d) addition of a time code display unit to provide visual read-out of time code data; (e) addition of an event recorder to record up to 150 channels of unitary on/off data or time code data; and (f) modification of the simulator to provide simulation of Nimbus B format, including time code, digital channels, split-phase data, revised words/frame format, and revised synchronization code format.

These modifications were accomplished through: (a) addition of cabinet 6 that contains the event recorder, digital decommutator, and time code display; (b) addition of a single card file that contains the time code generator to the simulator cabinet (cabinet 5); and (c) rework of the group synchronizer, system control, decommutator, and simulator. Figure 1-30 is a block diagram presentation of the current PCM Ground Station System 2 configuration.

2.3.4.1 BIT SYNCHRONIZER. The original bit synchronizer was removed and replaced by a Radiation 5220A bit synchronizer that was modified to handle split-phase mark zero input data. Addition of this unit provides a better signal-to-noise ratio than the original unit. The 5220A bit synchronizer is completely programmable as to data type and bit rate.

2.3.4.2 GROUP SYNCHRONIZER. Wiring and logic changes to the group synchronizer input shift register, frame synchronizer, word synchronizer, subframe ID correlator, and output shift register were required to permit synchronization with the revised format. Modifications to each unit are described in the following subparagraphs.

2.3.4.2.1 INPUT SHIFT REGISTER. The input shift register (figure 1-31) was modified to provide a DC RESET input to CSR's A99-A, A99-B, and A99-C. The DC RESET signal is derived from subframe ID correlator logic and is developed over a 5-microsecond interval immediately following the SF ID READ signal. By resetting the last three bits of the frame sync pattern after frame sync correlation, the subframe ID sync word appears in the output register in the proper form with ZERO's in the most significant three bits and subframe ID count in the least significant four bits.

2.3.4.2.2 FRAME SYNCHRONIZER. The frame synchronizer (figure 1-32) was modified to provide a 63:1 instead of a 64:1 words/frame count and to produce frame rate and bits/word counter reset pulses upon occurrence of count 0 in the words/frame counter or upon occurrence of frame sync correlation during the search mode.

The words/frame counter was short-counted by wiring differentiator A33-F between power inverter A20-B and the reset input to CSR A43-A. When the counter is advanced to count 32, the positive-going output of power inverter A20-B triggers differentiator A33-F. The resultant negative output of A33-F resets CSR A43-A to advance the counter to count 33, thereby short-counting to produce a 63:1 words/frame counter.

Since type B data is no longer used, the output of B data sync AND gate A32-B was opened to remove the AND gate from synchronizer logic. The output of AND gate A4-C was connected to OR gate A32-A, and output power inverter A20-K was connected to power inverter A29-K. These modifications provide an output from OR gate A32-A when AND gate A37-B detects words/frame count 0 or when AND gate A4-C detects sync correlation during the search mode. The output of OR gate A32-A is routed through power inverter A20-K to provide a FRAME RATE signal and (through modification) also drives power inverter A29-K to provide a BITS/WORD COUNTER RESET signal.

2.3.4.2.3 WORD SYNCHRONIZER. The word synchronizer (figure 1-33) was modified to provide a first word count of four bits, with subsequent word rate signals at 8-bit intervals. Since type B data is no longer used, the output of AND gate A64-A was opened to remove the AND gate from synchronizer logic. The pin 8 input to OR gate A57-E (the OUT contact of the WS INHIBIT switch) and the pin 21 input to AND gate A61-A were grounded. With this arrangement, a BITS/WORD COUNTER RESET signal from the frame synchronizer is routed through AND gate A61-A and OR gates A28-E and A28-F to set CSR's A52-A and A52-B. Since the bits/word counter is preset in this manner, the first word of each frame is limited to a 4-bit period.

2.3.4.2.4 SUBFRAME ID CORRELATOR. The subframe ID correlator (figure 1-34) was modified to provide a reset pulse to input shift register stages 10, 11, and 12 so that subframe ID count appears in the output register in the correct form. An additional connection was made to the output of differentiator A90-E so that input shift register stages 10, 11, and 12 are reset when the differentiator is triggered. The reset pulse is of a 5-microsecond duration and commences at the trailing edge of the SUBFRAME ID READ pulse from differentiator A90-D.

2.3.4.2.5 OUTPUT SHIFT REGISTER. The output shift register (figure 1-35) was modified to provide the additional drive capability required for outputs to the digital decommutator and the time code display. The additional drive is furnished by power inverters A88-A through A88-G that are connected in parallel with power inverters A93-A, A93-C, A93-E, A93-G, A93-J, A68-C, and A68-E.

2.3.4.3 SIMULATOR. Modifications to the simulator (figure 1-36) include: (a) incorporation of a split-phase code generator to simulate Nimbus B data signals; (b) modification of bit and word counters to comply with the 62-1/2-word frame format; (c) addition of single word insertion and selectable frame capabilities; and (d) modification to data register input circuits to permit simulator loading of time code. In addition a time code generator was assembled into a single card file and was mounted in cabinet 5 to provide simulated time code data.

2.3.4.3.1 SPLIT-PHASE CODE GENERATION. Split-phase code is generated by toggling a CSR at the leading edge of each ZERO data bit, ANDing BIT RATE with the ONE output of the CSR, ANDing BIT RATE with the ZERO output of the CSR, and OR-gating the resultant signals.

The NRZ output of the simulator data shift register is routed through power inverter A55-B to AND gate A69-A that is enabled by every ZERO bit in the data signal. The BIT RATE

signal from connector J104 is inverted through 2-NOR A34 and provides BIT RATE sample pulses to AND gates A69-A and A69-B. The applied NRZ ZERO bit enable and the BIT RATE sample signals to AND gate A69-A result in a negative-going output that is coincident with the leading edge of each NRZ data bit. Each negative-going signal from AND gate A69-A toggles CSR A19-A that alternately enables AND gates A69-B and A69-C. AND gate A69-B is sampled by the BIT RATE output of A43-E, and AND gate A69-C is sampled by the BIT RATE output of power inverter A55-H. The outputs of the AND gates are OR'ed by A69-D and are routed to video amplifier A90. Since the CSR changes state with each ZERO bit to alternately enable gating of opposite phases of bit rate, the resultant OR'ed signal changes phase with each ZERO data bit to fulfill split-phase code requirements.

2.3.4.3.2 BIT AND WORD COUNTER. Simulator bit and word counters were modified such that the first word of each minor frame is limited to four bits and the remainder of the frame is limited to sixty-two 8-bit words. This results in a minor frame length of $62\frac{1}{2}$ words, as required by the Nimbus B format.

Occurrence of the first word of each minor frame is detected by AND gates A34-D and A34-F. The resultant outputs inhibit AND gates A40-E and A40-F and are inverted by power inverter A93-C to enable AND gate A40-A during the first word of each minor frame. With these enable and inhibit signals, the word counter is advanced by the output of bit counter CSR A1-B (through AND gate A40-A and OR gate A40-D), thus removing CSR A1-C from the counter string to shorten the first word length by four counts. During all subsequent minor frame words, a ground level output from AND gates A34-D and A34-F enables AND gates A40-E and A40-C to permit the bit counter to function as a full 8-bit counter.

Count 62 of the frame counter is detected by AND gates A94-C and A94-D that produce a negative output through A78-A to monostable multivibrator A44-B. At count 63, the trailing edge of the count 62 signal triggers monostable multivibrator A44-B, and the resultant 2-microsecond output is routed through power inverters A93-H and A93-D to reset the frame counter.

2.3.4.3.3 SINGLE WORD INSERT CAPABILITY. The single word insert capability was accomplished by adding circuits for selection of word time slot and word content. Switches A20-S1 through A20-S6 and A45-S1 through A45-S4 are positioned to select the word and frame time slot and are connected to true and inverted outputs of word and frame counter CSR's. Switch A45-S6 provides enable/disable control of the single word insertion logic. Outputs from the time code select switches and the enable/disable switch are applied to a 13-input AND gate consisting of A66-F, A94-B, A94-A, A93-F, A93-G, and A94-F. AND gate A94-F also receives inhibit inputs from power inverter A93-E during sync time slots and from the time code gating time slots. If the enable/disable switch is in the enable position and a valid time slot is selected, the 13-input AND gate is enabled during the selected time slot with a resultant output through power inverter A93-B that strobes word content AND gates A92-B through A92-H. The word content AND gates are enabled or inhibited as selected by word content switches A70-S1 through A70-S7. The word thus constructed is strobed through the word content AND gates to the OR gates at the simulator data register input. The negative output of the 13-input AND gate also inhibits AND gate A94-E to prevent loading other data during the single word insertion time slot.

2.3.4.3.4 SELECTABLE SYNC WORD CAPABILITY. The selectable sync word capability was accomplished by adding circuits for selection of sync word. Switches on circuit cards A17, A42, and A67 and associated gating logic provide this capability. Switches A17-S1 through A17-S4 are positioned to select the pattern for the first four bits of the frame sync word. Outputs from these switches enable or inhibit AND gates A16-C, A66-E, A66-A, and A65-D that are strobed during word time 1 by the output from AND gates A34-D and A34-F through power inverter A93-C. The resultant gated output bits are OR'ed by A65-C, A66-C, A16-A, and A16-D and are routed through power inverters A47-F, A47-G, A47-H, and A47-J to the OR gates at the simulator data register input.

Frame sync pattern bits 5 through 12 are constructed by switches A17-S5, A17-S7 and A42-S1 through A42-S6. Outputs of these switches control AND gates A92-A, A16-F through A16-H, and A69-E through A69-H that are strobed during word time 2 by the output from AND gate A83-F through power inverter A54-D. The second portion of the frame sync word is routed from the AND gates to the OR gates at the simulator data register input.

Bits 13 through 16 of the frame sync pattern are constructed by switches A42-S6, A42-S7, A67-S1, and A67-S2. These switches control AND gates A16-E, A16-B, A66-D, and A65-E that are strobed during word time 3 by the output from AND gate A84-B through power inverter A93-A. The AND gate outputs are then OR'ed, inverted, and applied to the simulator data register input OR gates as described for frame sync pattern bits 1 through 4. Power inverter A93-A output also strobes AND gates A32-E through A32-H to gate the four ID sync bits to the simulator data register input.

2.3.4.3.5 TIME CODE INPUTS. The simulator data register input OR gates were further modified to accept four bits of time code data from the time code generator. These time code bits are received through pins BZ, BY, BX, and BW of connector J108.

2.3.4.3.6 TIME CODE GENERATION. The time code generator (figure 1-37) contains six binary-coded-decimal (BCD) up-counters that are advanced at a 1-pps rate to generate time code data comprised of units and tens of seconds, minutes, and hours.

The units of seconds up-counter is formed by CSR's A7-A through A7-C and A8-A and is advanced at a 1-pps rate by the minor frame rate signal received through power inverter A16-A. When the counter is advanced to count 10, AND gate A21-D is enabled by the $\bar{8}$ output of the CSR A8-A, the 2 output of CSR A7-B (inverted through A15-D), and the frame rate signal (inverted through A16-B). The resultant negative output of AND gate A21-D advances the tens of seconds counter and is applied through OR gate A6-A and power inverter A16-C to trigger differentiator A19-A. The output of differentiator A19-A resets the units of seconds counter to 0.

Each count 10 output from the units of seconds up-counter causes the tens of seconds up-counter to advance as discussed above. The tens of seconds counter is a 6:1 counter and is comprised of CSR's A8-B, A8-C, and A10-A. When the tens of seconds up-counter is advanced to count 6, AND gate A21-E is advanced by the $\bar{4}$ output of CSR A10-A, the 2 output of CSR A8-C (inverted through A15-F), and the inverted frame rate signal. The resultant

negative output of AND gate A21-E advances the units of minutes up-counter and is applied through OR gate A6-B and power inverter A16-D to trigger differentiator A19-B. The output of differentiator A19-B resets the tens of seconds up-counter to 0.

Operation of the units of minutes up-counter (CSR's A10-B, A10-C, A11-A, and A11-B) and the tens of minutes up-counter (CSR's A11-C, A12-A, and A12-B) is identical to the seconds up-counters described in the preceding paragraphs.

The units of hours up-counter (CSR's A12-C and A17-A through A17-C) and the tens of hours up-counter (CSR's A18-A and A18-B) operate similarly to the counters described in the preceding paragraphs except that the hours count is reset at count 24. When the counter is advanced to count 24, AND gate A22-C is enabled by the $\bar{2}$ output of CSR A18-B, the 4 output of CSR A17-B (inverted through A22-D), and the inverted frame rate signal. The resultant negative output from AND gate A22-C is applied through OR gate A6-F and power inverter A16-H to reset the tens of hours up-counter. The output of power inverter A16-H is also applied through OR gate A16-E and power inverter A16-G to trigger differentiator A19-E to reset the units of hours up-counter and through OR gates A6-A through A6-D to reset the seconds and minutes up-counters.

The FRAME GATE $\bar{T}$ signal from the decommutator provides one enable input to each of the AND gates in the word gate matrix consisting of NOR circuits on A1, A2, and A3. These circuits also receive true and inverted WORD GATE 1, 2, 4, 8, 16, and 32 signals through power inverters A13-A through A13-K, A16-J, and A16-K and A26-C. During word time 4 of each first frame, AND gates A1-A and A1-B are enabled by applied FRAME GATE $\bar{T}$ and WORD GATE 1, 2, 4, 8, 16, and 32 signals to develop an output through power inverter A4-A to strobe AND gates A23-A, A23-B, A6-G, and A6-H. These gates receive the ZERO outputs of CSR's A7-A through A7-C and A8-A and, when strobed, gate units of seconds data through OR gates A3-A, A3-C through A3-E, and A21-A through A21-C and power inverters A4-H, A4-J, A4-K, and A13-K to the simulator data register.

During word time 13 of the first frame, AND gates A1-C and A1-F are enabled to develop an output through power inverter A4-B to strobe AND gates A23-C through A23-E to gate tens of seconds data to the simulator. During word time 22, the output of AND gates A2-B and A1-D strobes AND gates A23-F through A23-H and A24-A through power inverter A4-C to gate units of minutes data; during word time 24, the output of AND gates A2-F and A1-E strobes AND gates A24-B, A24-C, and A24-D through power inverter A4-D to gate tens of minutes data; during word time 32, the output of AND gates A3-B and A2-A strobes AND gates A24-E, A24-F, A24-G, and A24-H through power inverter A4-E to gate units of hours data; and during word time 37, the output of AND gates A3-F and A2-C strobes AND gates A15-A and A15-B through power inverter A4-F to gate tens of hours data.

Each word gate matrix output is OR'ed by A2-D and A2-E and is routed through power inverter A4-G to inhibit normal simulator data loading during the word time slots. Provision is also made for a switch-controlled input through connector P108-CL to OR gate A6-F to reset all time code generator counters.

2.3.4.4 TIME CODE DISPLAY. The time code display unit (figure I-38) included in the system modification provides logic circuits for decimal display of hours, minutes, and seconds of time code data and for generation of time code plots on analog and digital recorders.

2.3.4.4.1 DECIMAL DISPLAY. The four data bits containing time code are routed from the group synchronizer output register, through the digital decommutator, to input AND gates at the time code shift register. The input AND gates are A99-A through A99-F, A100-A through A100-F, A74-A through A74-F, A75-A, and A75-C. During each first minor frame period, the FRAME GATE 1 signal from the decommutator is received through power inverter A73-E and complementary emitter-follower A95-C to enable all shift register input gates. During word time 4 of the first frame, units of seconds time code data is received and WORD GATE $\overline{4}$ signal from the decommutator is routed through complementary emitter-follower A95-K to strobe AND gates A74-B through A74-E. The strobe pulse loads CSR's A88-C and A89-A through A89-C with units of seconds time code data. During word time 12 of the first frame, tens of seconds time code data is received. The WORD GATE $\overline{12}$ signal, received through complementary emitter-follower A95-J, strobes AND gates A74-F, A75-A, and A75-C to load tens of seconds data into CSR's A90-C, A91-A, and A91-B. Similarly, WORD GATE $\overline{19}$ signal, through complementary emitter-follower A95-H, loads units of minutes data into CSR's A84-B, A84-C, A85-A, and A85-B; WORD GATE $\overline{23}$ signal, through complementary emitter-follower A95-G, loads tens of minutes data into CSR's A86-B, A86-C, and A87-A; WORD GATE $\overline{31}$ signal, through complementary emitter-follower A95-B, loads units of hours data into CSR's A80-A through A80-C, and A81-A; and WORD GATE $\overline{36}$ signal, through complementary emitter-follower A95-A, loads tens of hours data into CSR's A82-A through A82-B.

Shift register CSR outputs that contain time code data are routed to display register CSR's on A61 through A67. The FRAME GATE $\overline{1}$ output of A95-C also enables AND gate A75-E and the WORD GATE $\overline{60}$ signal, received through power inverters A73-G and A98-D samples the AND gate during word time 60 to develop a load pulse to strobe time code data into the display register. The resultant strobe pulse is routed through power inverter A98-A to load CSR's A61-B, A61-C, A62-A through A62-C, and A63-A; through power inverter A98-B to load CSR's A63-B, A63-C, A64-A through A64-C, A65-A, and A65-B; and through power inverter A98-C to load CSR's A65-C, A66-A through A66-C, and A67-A through A67-C. Display register CSR outputs are routed through power inverters on A70 and A71 to drive unitary readout indicators DS1 through DS6 that provide a decimal readout of time code data in hours, minutes, and seconds. The decimal readout is updated at the end of word time 60 during each first minor frame.

2.3.4.4.2 TIME CODE PLOTS. After the first minor frame period, the FRAME GATE 1 inhibit signal to AND gate A75-E is switched to ground and enables the AND gate. WORD GATE 20 and 40 signals from the decommutator and the WORD GATE $\overline{60}$ signal (inverted by A73-G) are OR'ed by A75-B to provide sample pulses to AND gate A68-A. The resultant output is routed through power inverter A73-F and complementary emitter-followers A95-E and A95-F to shift the time code shift register contents to the time code tracks on the analog and digital recorders. The shift register outputs through power inverters A73-J, A73-K, and A92-A through A92-D are routed to five time code tracks on the digital event recorder; and shift register outputs through power inverter A73-H and relay drivers A96-A and A96-B are routed to relays that control event pins on the analog recorders.

Shift pulses from AND gate A75-E and power inverter A73-F are also routed through complementary emitter-follower A95-D to shift the time code locator circulating shift register, consisting of CSR's A57-A through A57-C, A58-A through A58-C, A59-A through A59-C, A60-A through A60-C, and A61-A. The time code locator shift register is preset to a pattern of ONE's and ZERO's such that a ONE output is developed coincident with every time code output from the shift register. Outputs of the time code locator shift register are routed through AND gate A75-F and power inverters A98-J, A98-K, and A73-A through A73-D to the time locator tracks on the event recorder. The output of AND gate A75-F is also routed through power inverter A98-H and relay drivers A96-C and A96-D to time locator relays in the analog recorders. Time code shifting is completed during the 13th frame, and AND gate A75-F is inhibited thereafter by applied FRAME GATE 13, 14, and 15 signals from the decommutator. During word time 12 of each first minor frame, AND gate A75-D is enabled to provide outputs, through power inverters A98-E through A98-G, to preset the required pattern into the time code locator register.

2.3.4.5 DECOMMUTATOR. Modifications to the decommutator logic included addition of two power inverter circuit cards to the decommutator drawer and associated wiring changes to obtain additional word gate and frame gate outputs; wiring of patch panel hubs to an output connector to permit digital data word selection for event recording; and inclusion of a digital decommutator in the new cabinet 6.

2.3.4.5.1 DECOMMUTATOR MODIFICATIONS. Inclusion of the time code display drawer in cabinet 6 required routing additional transfer pulses from the decommutator (figure I-39). Power inverter circuit cards were installed in locations A55 and A80 to permit routing the additional transfer pulses in parallel with existing circuits. Parallel routing was used to prevent excessive loading of patch panel inputs. Table 12 identifies each power inverter circuit, specifies associated input and output connections, and lists the transfer pulse thus routed.

Table 12. Decommulator Modification (Transfer Pulses)

Modification Circuit	Input Circuit	Output Connection	Signal
A55-A	A50-D	J1-g	Word gate $\bar{4}$
A55-B	A48-D	J1-h	Word gate $\bar{12}$
A55-C, A55-D	A54-A	J1-j	Frame gate $\bar{1}$
A55-E	A45-C	J1-k	Word gate $\bar{19}$
A55-F, A55-G	A45-D	J1-n	Word gate 20
A55-H	A45-G	J1-p	Word gate $\bar{23}$
A55-J	A53-F	J1-q	Frame gate 14
A55-K	A53-G	J1-r	Frame gate 15
A80-A	A53-H	J1-t	Frame gate 16

Table 12. Decommulator Modification (Transfer Pulses) (Continued)

Modification Circuit	Input Circuit	Output Connection	Signal
A80-B	A43-G	J1-u	Word gate $\overline{31}$
A80-C	A40-D	J1-v	Word gate $\overline{36}$
A80-D, A80-E	A40-H	J1-w	Word gate 40
A80-F	A32-D	J1-x	Word gate $\overline{60}$

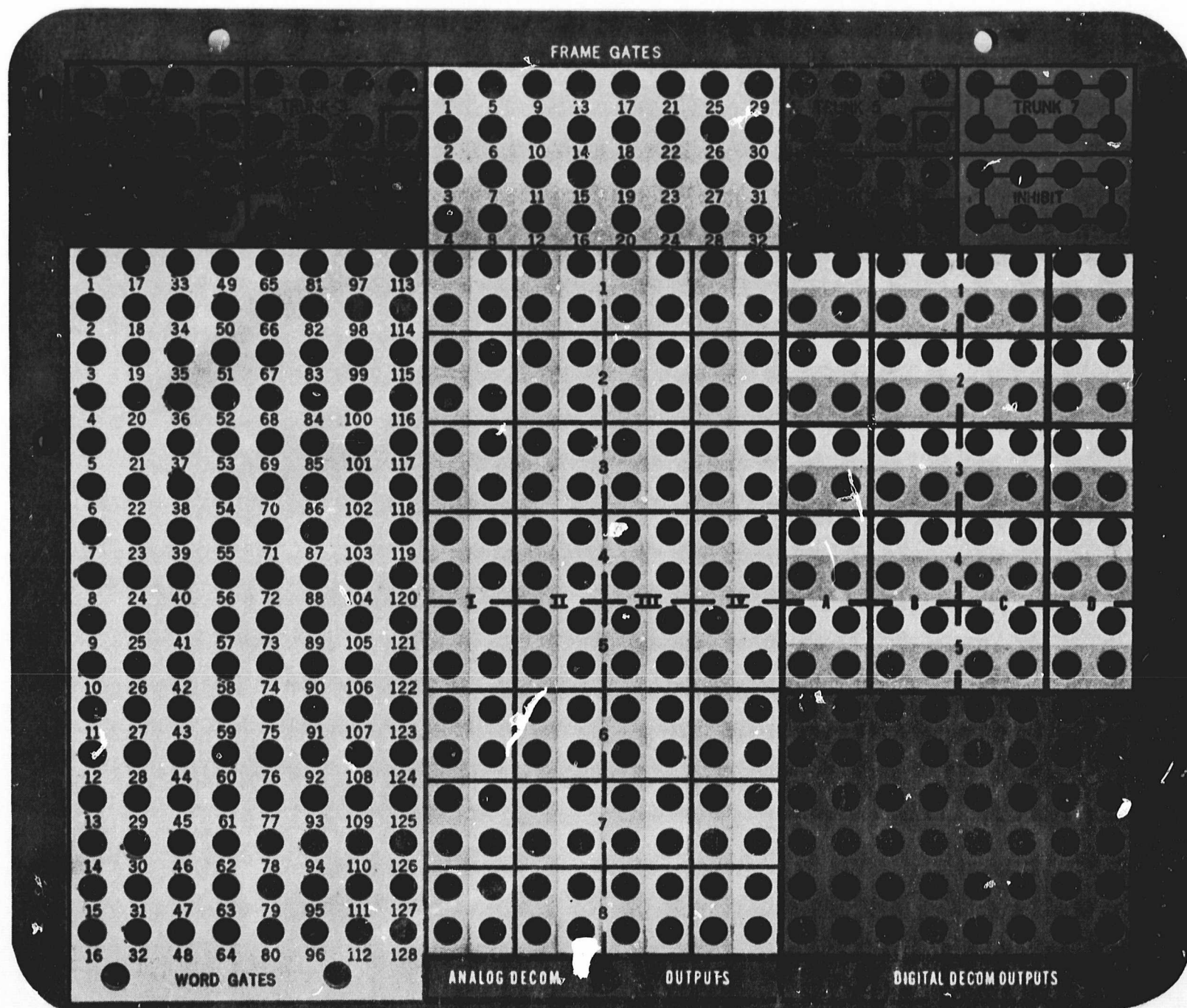
Additional wiring from previously unused patch panel hubs to connector J2 permits patch panel selection of time slots for recording digital data on the event recorder. These hubs are designated DIGITAL DECOM OUTPUTS on the modified patch panel (figure 64). Selection of data for the event recorder is accomplished in the same manner as selection of data for the analog recorders.

2.3.4.5.2 DIGITAL DECOMMUTATOR. The digital decommutator (figure 1-40), added during the modification, consists of twenty 7-bit storage registers. The unit receives the parallel 7-bit data word output from the group synchronizer output register and, dependent on patch panel programming, loads data words from the program-selected time slots into selected registers for application to the event recorder. The data is then recorded on 140 tracks (twenty 7-bit groups) of the event recorder.

The 7-bit data word output from the group synchronizer output register is received through digital decommutator power inverters on A76, A82, A88, A94, A81, and A92. True and inverted data outputs from the power inverters are applied to steering inputs of the twenty 7-bit storage register flip-flops. Word and frame gate signals, patch-selected on the decommutator patch panel are routed to 2-NOR AND gates on A98, A99, and A100. Upon coincidence of the selected frame and word time slot, the AND gate associated with selected event recorder channels is enabled to develop a trigger pulse to load the data word into the 7-bit register for these channels. When recording of supercommutated data (data sampled every frame) is required, the frame gate patch connection is left open and the AND gate is enabled every selected word time to load the supercommutated data into the selected storage register. Outputs from the storage register flip-flops are routed through power inverters to event recorder inputs.

2.3.4.6 EVENT RECORDER. An event recorder, Brush Model 14-3615-00, was added during the modification to record digital data and serial time code data. The trace is an on-off mark, i.e., presence of a trace is a ONE (negative-true logic) and absence of a trace is a ZERO. Activation of the event recorder TEST pushbutton produces traces on a channel for troubleshooting.

Event recorder inputs are hard-wired to outputs of the digital decommutator storage registers. The input trigger circuits of the 20 registers are hard-wired to the digital decommutator portion of the patch panel. Table 13 shows the correlation between patch panel areas and event recorder channels.



1210-4

Figure 64. Decommutator Patch Panel

Table 13. Event Recorder and Patch Panel Assignments

Event Recorder Channels	Patch Panel Inputs	Event Recorder Channels	Patch Panel Inputs
3 through 9	1-A	77 through 83	3-C
10 through 16	1-B	84 through 90	3-D
17 through 23	1-C	91 through 97	4-A
24 through 30	1-D	98 through 104	4-B
31 through 37	2-A	105 through 111	4-C
40 through 46	2-B	114 through 120	4-D
47 through 53	2-C	121 through 127	5-A
54 through 60	2-D	128 through 134	5-B
61 through 67	3-A	135 through 141	5-C
68 through 74	3-B	142 through 148	5-D

Channels 1, 38, 75, 112, and 149 are time code marker channels; and channels 2, 39, 76, 113, and 150 are time code channels. These channels are not patchable and are hard-wired to the time code display drawer.

2.3.4.7. SYSTEM CONTROL. Modifications to the system control unit (figure 1-41) include removal of the B-data squelch circuit, incorporation of two new squelch circuits to permit operation with split-phase data, removal of the drive signal to the B DATA indicator, and addition of logic for bit synchronizer programming.

2.3.4.7.1 REAL-TIME SQUELCH CIRCUIT. With a split-phase data input, squelch circuits are required for the half-frequency, as well as the basic frequency, because a series of ZERO's in a split-phase input appear as a signal that is one-half the frequency of a series of ONE's. Since B-type data is no longer required, the B-data squelch card was removed and a 250-cps squelch card was installed in location A98. The 250-cps and 500-cps squelch cards are adjusted for overlapping operation, i.e., a squelch output is developed by A97 or A98 for any input signal ranging from 250 to 500 cps. The outputs from A97 and A98 are inverted by A92-F and A93-F, respectively, and are OR'ed by A92-G. The resultant output from OR gate A92-G is inverted by power inverter A93-G to provide a real-time squelch signal to system control logic and to inhibit time code squelch AND gate A92-D.

2.3.4.7.2 TIME CODE SQUELCH CIRCUIT. Operation with the Nimbus B format requires time code squelch circuit operation only when the received time code is not accompanied by a real-time (500-cps) data signal. Therefore, the time code squelch signal from A99 was re-routed through AND gate A92-D and NOR A92-E to power inverter A93-E. When 500-cps data is received, the real-time squelch output of power inverter A93-G inhibits AND gate A92-D to prevent generation of a time code squelch signal.

2.3.4.7.3 PLAYBACK SQUELCH CIRCUIT. The playback squelch circuit was modified by installation of a half-frequency (7.5-kc) squelch card in location A96 and by OR-gating the outputs from the 7.5-kc and 15-kc squelch cards. The outputs from A96 and A100 are inverted by A92-A and A92-B, respectively, and are OR'ed by A92-C to develop the playback squelch signal to system control logic.

2.3.4.7.4 B DATA INDICATOR. Since operation with B-type data is no longer required, the input to indicator-driver A76-B was grounded. The resultant negative output of the circuit holds B DATA indicator DS26 deenergized.

2.3.4.7.5 BIT SYNCHRONIZER PROGRAMMING. Gates were added to the system control logic to generate the correct format for the remote portion of the bit synchronizer. These gates are triggered by the squelch circuits to program the bit synchronizer for either 500-cps or 15-kc operation.

2.4 SYSTEM MECHANICAL DESCRIPTION

The following subparagraphs provide detailed mechanical descriptions of the PCM and TME units.

2.4.1 PCM UNIT

2.4.1.1 PACKAGING CONCEPT. The packaging concept utilized for the Nimbus B PCM Telemetry Unit is based on experience gained from previous Radiation-built PCM systems for missile and spacecraft use (OAO, Telstar, Apollo, LEM, Nimbus and the Lunar Orbiter programs, among others). The technique utilized is that of placing the electronics under compression, using a lightweight polyurethane foam for a module encapsulant and spacer material to carry the compressive load. This lightweight foam encapsulant also serves to damp high frequency vibration. The resulting packaging reacts as a solid mass under dynamic environments, thus affording maximum protection to the electronics.

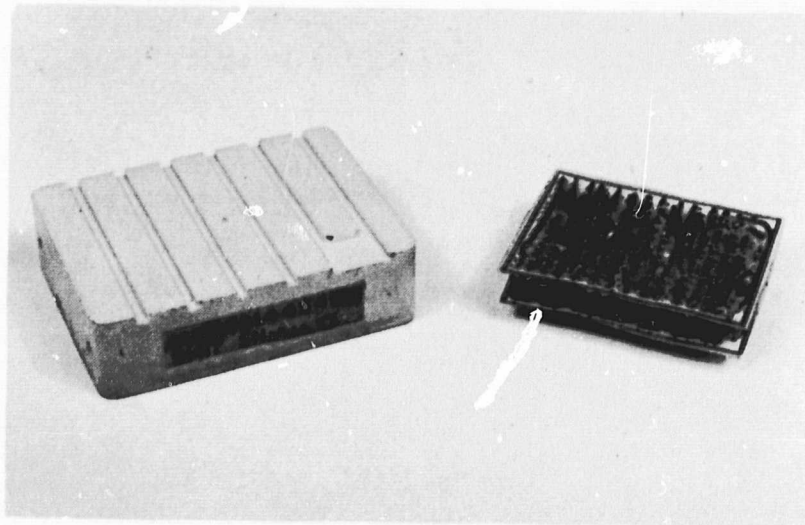
2.4.1.2 ELECTRONICS PACKAGING. A thorough evaluation of several approaches to packaging the PCM for minimum size and weight was performed early in the program. This study indicated that both planar and modular packaging techniques had to be employed to meet the system size requirements. A breakup of the electronics by circuit function showed that the power supply, programmer, A/D converter, and output register/split-phase converter circuitry all utilized conventional discrete components, while the multiplexer, timing and sequencer circuits utilized a combination of integrated circuits, microdiodes, and miniature resistors.

2.4.1.2.1 MODULAR PACKAGING TECHNIQUE. A study of the parts/unit count showed that the A/D converter, programmer, power supply, and output register circuits could be packaged in eight 2 x 2.68-inch welded cordwood modules. This is accomplished by positioning the components parallel to each other between, and normal to, two mylar sheets. The components are interconnected by resistance welding nickel ribbon to the leads (figure 65). Following electrical test, the welded field is coated with a conformal layer of epoxy to prevent stress during the foam-in-place molding operation. This molding is performed in cavities of accurate dimensions to provide modules of consistent size for the compressive loading operation.

The foamed modules are then mounted onto doublesided printed circuit cards, having plated-through holes. The modules are secured to the card by soldering the module pins to the printed wiring pads on the opposite side of the card, thereby effecting the electrical interconnections.

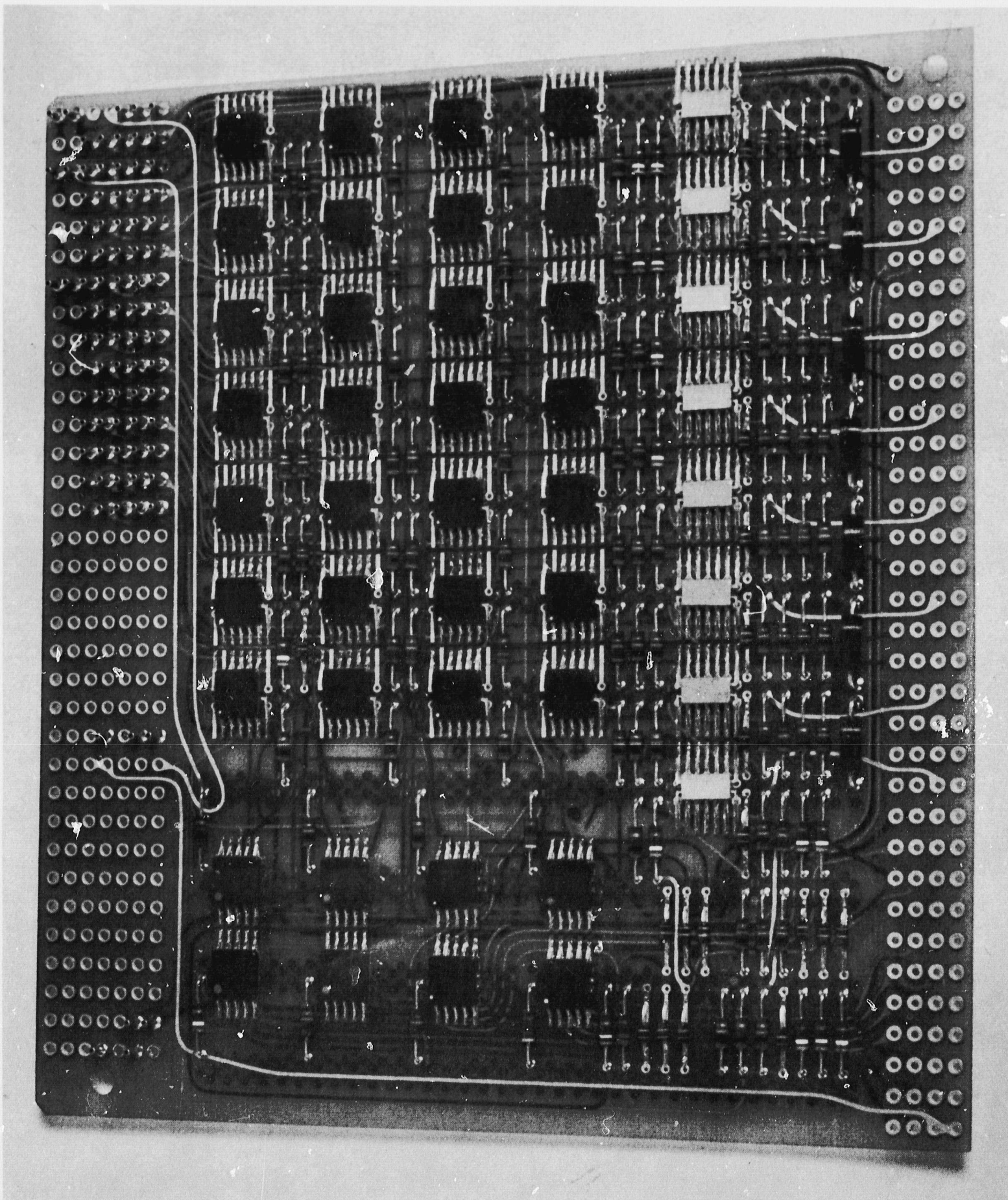
2.4.1.2.2 PLANAR PACKAGING TECHNIQUE. The multiplexer, sequencers, and timing circuits are composed of 708 flat-pack integrated circuit devices, 276 micro-zener and switching diodes, and 1,059 resistors and capacitors. The use of these various components is necessitated by the requirement that any single failure shall cause the loss of no more than eight channels of data. The majority of the resistors and diodes are utilized exclusively for the fault protection function.

The large quantity of components, along with the variety of form factors, required that a low-volume, high-density packaging technique be utilized. It was found that this requirement could be met through the use of a planar packaging technique. The circuits are packaged on 6-layer multilayered, plated-through hole, printed circuit cards, with integrated circuit, discrete, and microcomponents all mounted on the same cards (figure 66). The capacitors and resistors are mounted parallel to the card, with leads bent at a 90-degree angle and inserted through the plated-through holes for soldering. The microdiodes and integrated circuit packages are mounted flat against the multilayered card. These devices are procured with pre-tinned flat ribbon leads, which are fluxed and placed on top of their interconnecting circuit lands on the card. Interconnection is then made through the use of a temperature/time cycle controlled resistance soldering technique (figure 67).



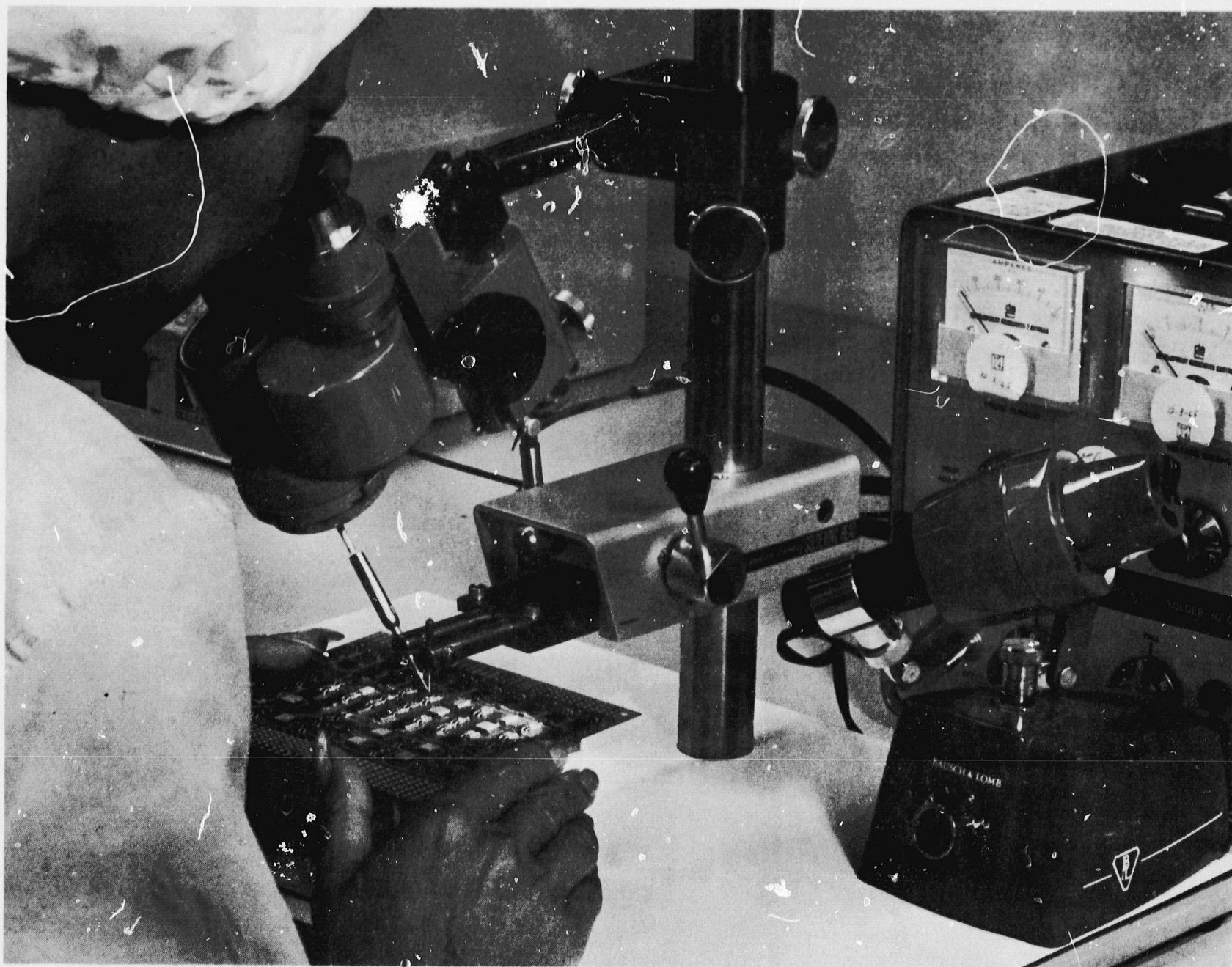
56450-4

Figure 65. Cordwood Welded Modules (Before and After Encapsulation)



1210-13

Figure 66. Planar Mounted Multiplexer Card Assembly



56450-6

Figure 67. Resistance Soldering of a Multiplexer Card Assembly

A functional breakup of these circuits showed that if analog and digital channels were packaged on the same printed circuit cards, a minimum number of different card types would be required.

This breakup resulted in the following four types of card assemblies:

- a. prime channel multiplexer card assembly
- b. subcommutated channel multiplexer card assemblies
- c. multiplexer timing circuits card assemblies
- d. multiplexer output circuits card assemblies

The prime channel multiplexer card assembly (hereafter referred to as the prime matrix card) contains all of the channel gates for the 21 prime analog and the 63 prime digital channels. The functions on this card are non-redundant, but utilize fail-safe circuit design. Thus, only one prime matrix card per PCM unit is required.

The subcommutated channel multiplexer card assemblies (hereafter referred to as submatrix cards) contain all of the subcommutated analog and digital gates on eight cards. All of these cards are identical except that the top layer is reversed on four of the cards to simplify system assembly and wiring. The circuits on these cards are nonredundant, but utilize fail-safe circuit design to minimize the propagation of any failures that might occur.

The multiplexer timing circuits card assemblies (hereafter referred to as output cards 1A and 1B) contain the timing generator for the row, column and sequencer commands to operate the analog and digital multiplexer, along with circuits to generate timing commands for the sync, ID, and time code words, and the multiplexer readout commands. These cards are identical, with one card required for each PCM unit to provide block redundancy for these functions.

The multiplexer output circuits card assemblies (hereafter referred to as output cards 2A and 2B) contain the multiplexer output circuits and sync word generators, along with the ID, time code, and analog and digital gates. These cards are identical except for differences in two resistors and differences in Zener diode values necessitated by the multiplexer timing.

2.4.1.2.3 PRINTED CIRCUIT CARDS. Two types of printed circuit cards are utilized in the system. The cordwood modules have two-sided cards with plated-through holes for mounting and interconnection, while the planar-packaged electronics have six-layer multilayered cards.

To minimize checking and rework time of the multilayered card masters, and to provide a high confidence level for card correctness prior to fabrication, a digital computer was used for checking these cards. Two sets of input sheets were independently originated from the card detail drawings, one by engineering and one by drafting. These were then entered into the computer, and the readouts checked independently against the card wiring diagram. Following this, they were crosschecked against each other. In this manner, total errors (engineering and drafting) were held to 3 out of a total of 10,031 circuit lines, with no mistakes being attributed to errors in pad identity.

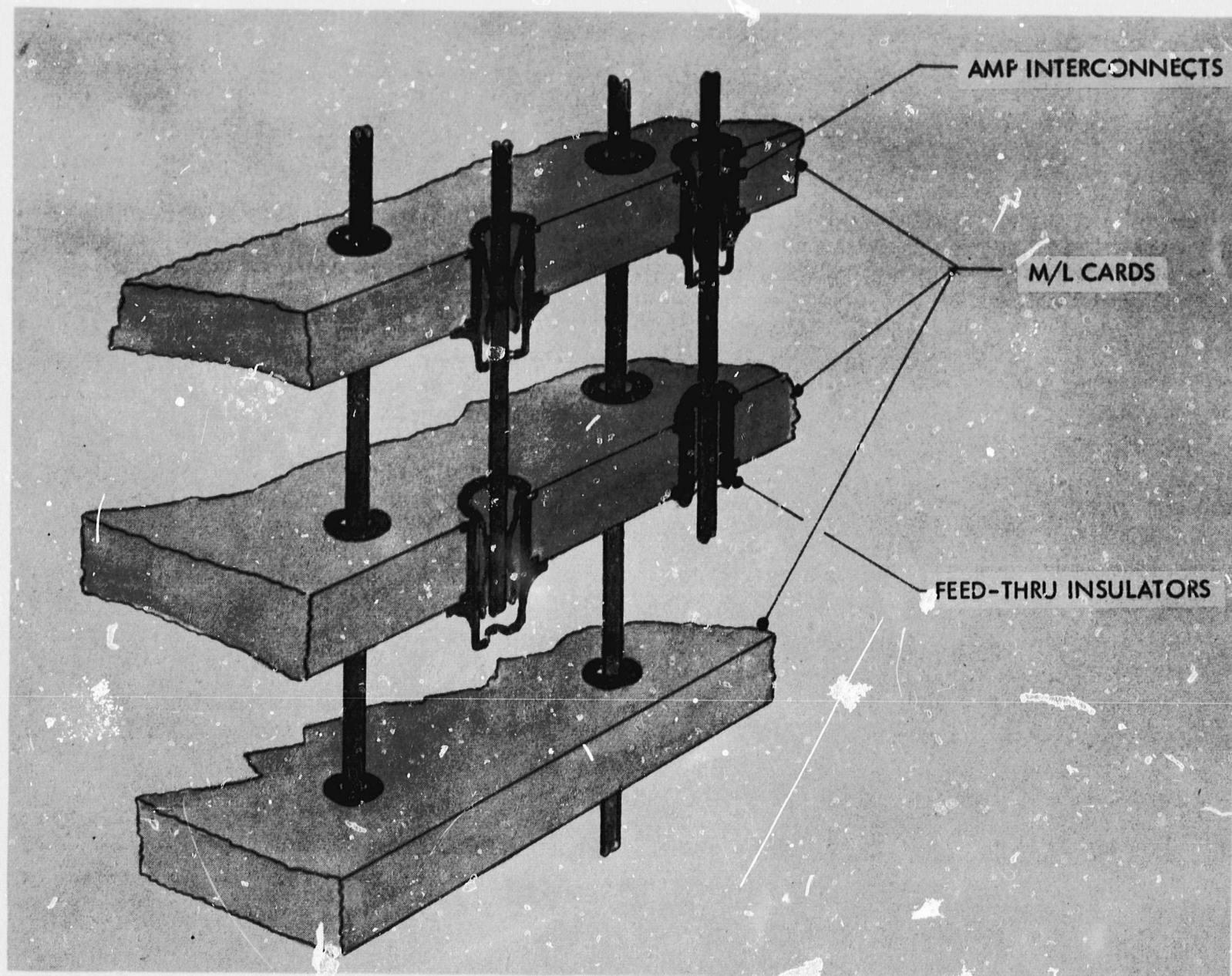
All of the printed circuit cards in the system utilized plated-through holes for interconnection between circuit layers. To comply with NASA specification NPC 200-4, redundant pads and jumper wires are also utilized for layer interconnection on the two-sided cards. Where this was not practical, such as with the multilayered cards, extensive quality control tests (which exceed the requirements of the NPC standards) are performed on test coupons attached to each card. In addition, photomicrographs are taken of etched cross-sectioned plated-through holes on the coupon and are examined as a part of the inspection process prior to release of the cards to system assembly.

2.4.1.2.4 INTERCONNECTIONS. The extreme density of the package (due to its high channel capability and redundancy/fail-safe provisions) required that a minimum volume, high capacity system be utilized for card interconnections.

In reviewing this requirement, it was determined that sufficient wiring pads were available to hard-wire the module cards together, since only 32 wires interconnected them, with an additional 23 wires from these two cards going to the external connectors. Since these two cards (which contained the power supply, programmer, A/D converter, and output register/split-phase converter modules) were connected directly to output cards 1 and 2 (which required a total of only 31 additional pads on both boards), it was decided that these would also be hard-wired together. This utilized 116 of the total 210 pads available on each of the module cards. Since the output type 1 and 2 cards had no wires going to an external connector, only 46 wires interconnected what thus became a four card group to the external connectors.

The wiring of the multiplexer was a different situation altogether. Due to the functional circuit breakup, number of channels per card assembly, quantity of timing signals required, and similarity of card layouts, over 46 pads would be required for most of the cards to provide the necessary intraconnections within the multiplexer, notwithstanding the 798 pads required for the input signals. To alleviate this situation, a unique interconnection technique was utilized (figure 68).

Interconnections among the multiplexer cards are effected through the use of miniature spring sockets, manufactured by AMP, Incorporated. These sockets are placed into the holes in the printed circuit cards and soldered onto their pads. The pads are oriented so that any interconnection from a pad on one card is directly in line with pads on other cards which must also be connected to this line. Solid bus wires are inserted through these sockets effecting electrical contact to all cards where required. On cards where connection is not required, a nylon insulator is bonded in that hole, and the wire passes through this insulator without making contact with that card.



56450-7

Figure 68. Bus Wire Interconnection Technique

This technique has many advantages. It eliminates the need for bused pads to connect wires which provide several boards with the same signal. (It reduced the requirement for 460 intraconnection pads per card to a maximum of 210.) It allows 0.085-inch diameter pads to be spaced on 0.100 by 0.150-inch centers. It allows closer spacing of card assemblies, since no additional space is required for any wiring harness. It provides the capability of minimizing crosstalk and noise problems on sensitive signal lines by separating them from power and other noise generating wires (sometimes difficult to do with hard wiring). Other advantages include savings in card layout time, simplified interconnection wire lists, elimination of potential damage to the printed circuit cards from soldering and unsoldering of wires, and ease of system assembly and disassembly. The utilization of this interconnect method can be seen in figure 69, which shows the PCM unit prior to mechanical assembly.

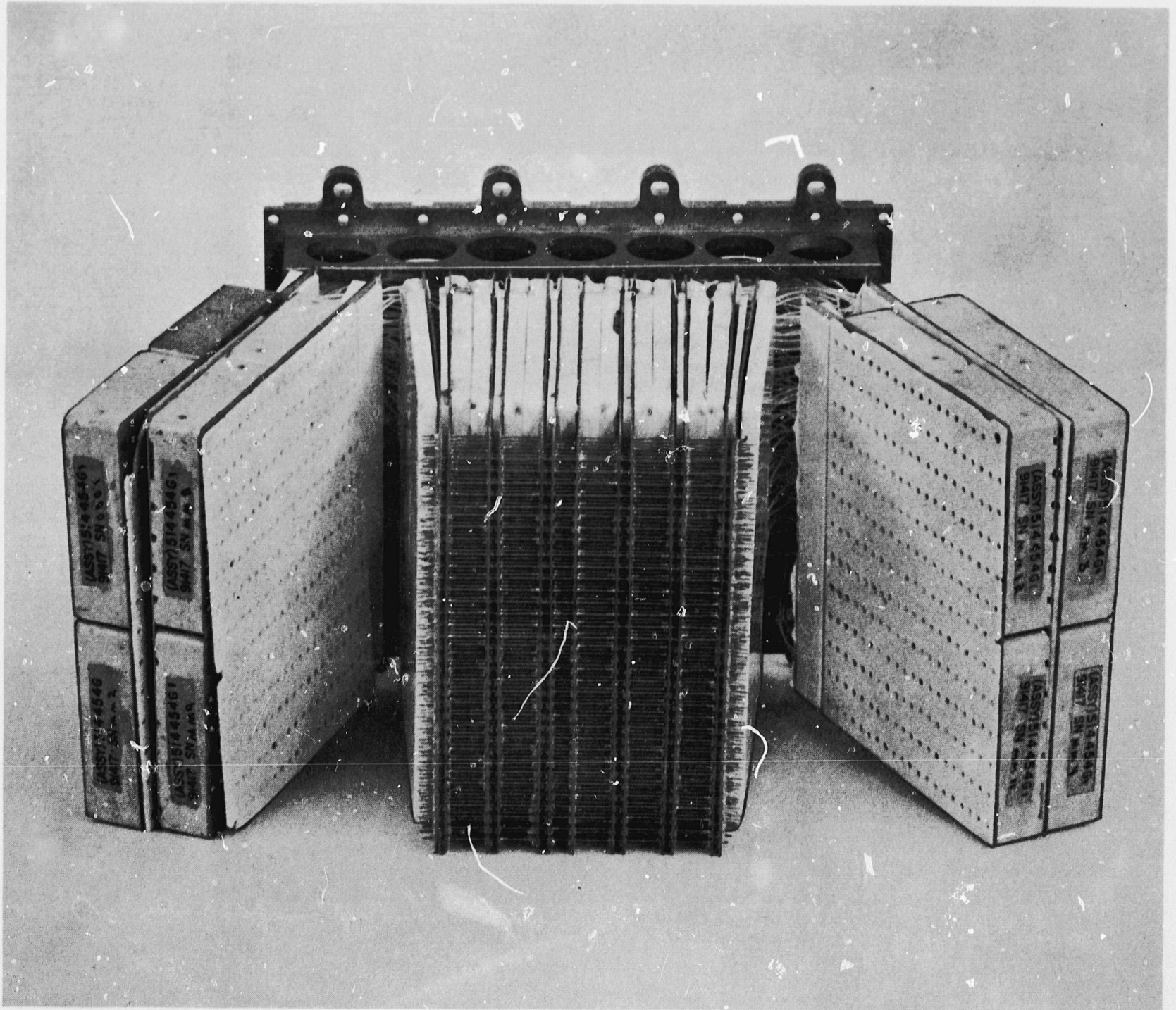
2.4.1.3 MECHANICAL PACKAGING. The mechanical integrity of the system relies upon a preloaded electronics assembly (figure 70). Utilizing this preloading technique, the electronics are integrated into what is effectively one mass, allowing a thin-walled, lightweight housing design to be utilized. This is possible since the walls of the housing are in tension only, while the bending moment is applied to the rigidized ends of the unit.

This concept was implemented through the use of an internal electronics support structure, along with a separate system housing (figure 71). The electronics support structure consists of two aluminum pressure plates connected by six columns. The electronics assembly is placed into the support structure, and a hydraulic press is used to apply the required compressive load. Fiberglass and foam loading shims ensure that the desired loads and correct displacement are achieved simultaneously.

The electronics support structure provides for proper alignment of the card assemblies and also maintains the preload on the electronics. This allows the electronics to be completely assembled before insertion into the housing. It also permits complete system test and operation prior to assembly in the housing.

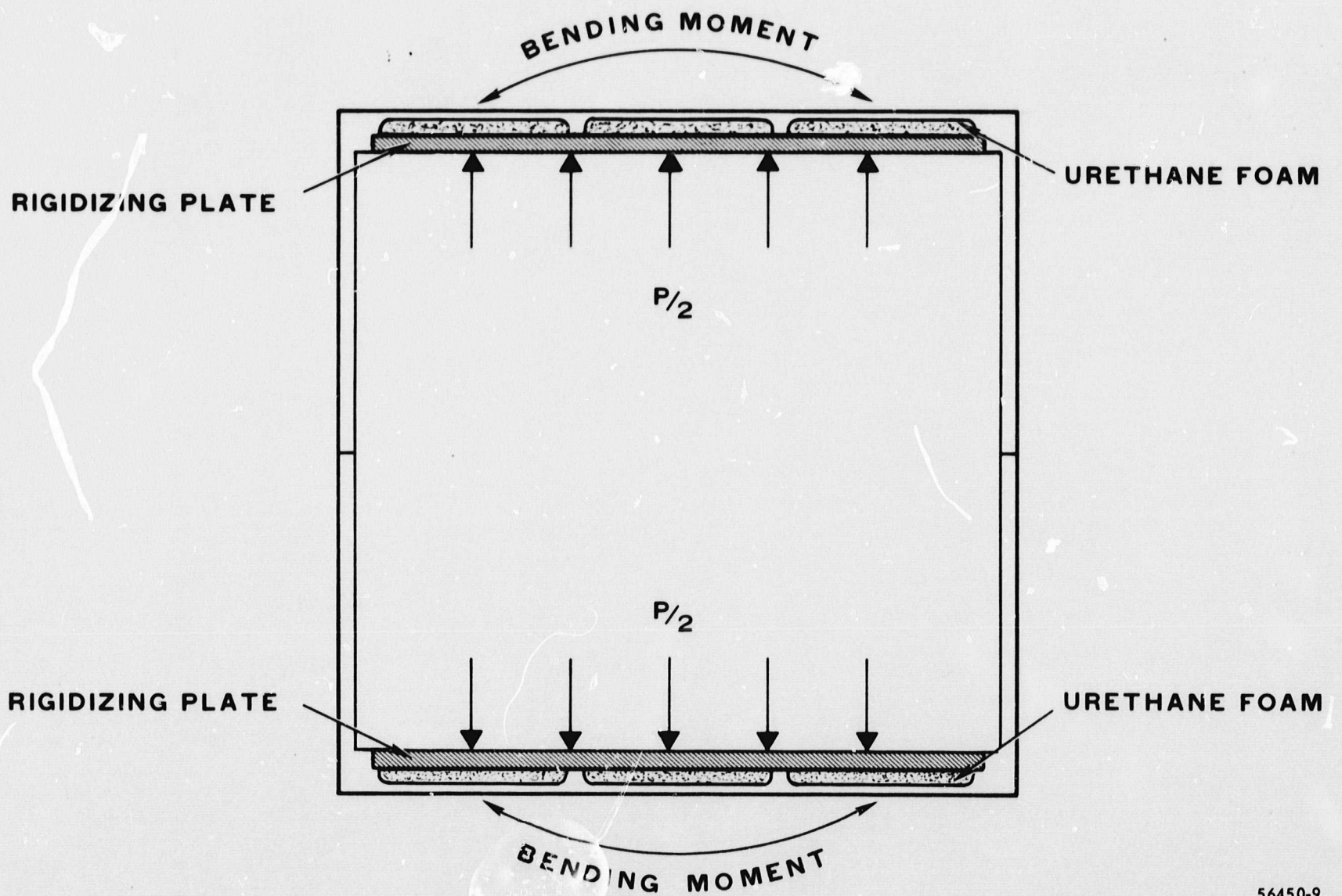
The housing consists of two machined monolithic magnesium structures. These structures, when secured together in a "clamshell" manner and with the front panel in place, provide support and protection for the electronics. The housing weight is minimized by using 0.040-inch walls wherever possible and through use of a rigid foam sandwich construction of the compression panels (ends of the housing).

When the system is assembled, the internal loading structure is separated from the housing by strips of foam silicone rubber bonded to the inside of the housing compression panels. These strips are designed primarily to provide high frequency vibration isolation, but also provide resonance control by being located around the perimeter of the compression panels. By locating the rubber strips in this manner, each of the two structures is exposed only to those areas of minimum displacement of one another when at their respective resonances. This technique has resulted in a maximum amplification factor (Q) of approximately 3.0 when vibration tested to qualification levels (sine - 10 g 0-peak maximum, 20 to 2,000 cps; random - 20 grms, 20 to 2,000 cps, 0.2 g²/cps spectral density) in all three planes (figures 72 and 73). Part of this can be attributed to the excellent damping characteristics of the rubber strips, which, being



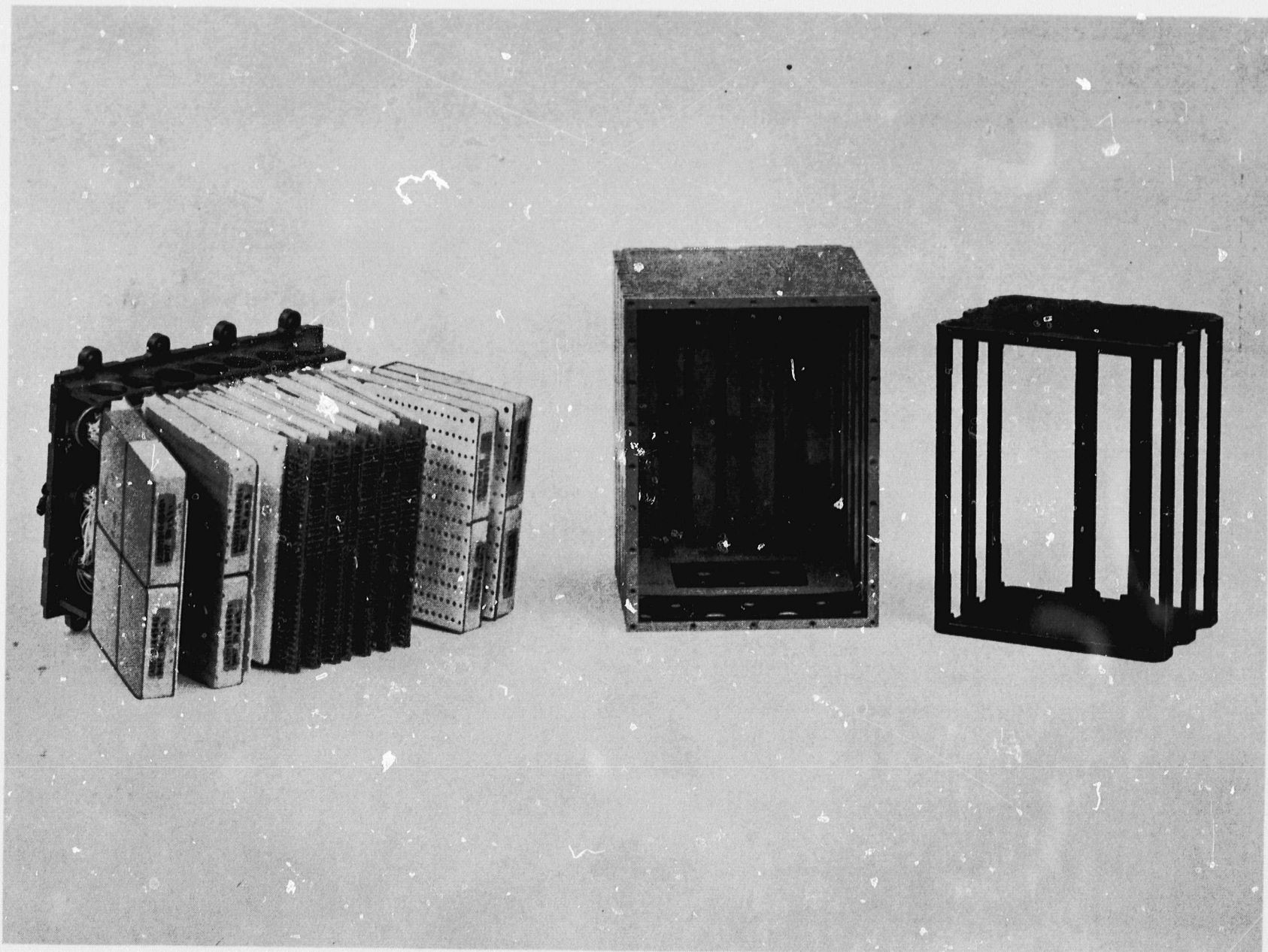
1858-15

Figure 69. Wired PCM Unit (Before Mechanical Assembly)



56450-9

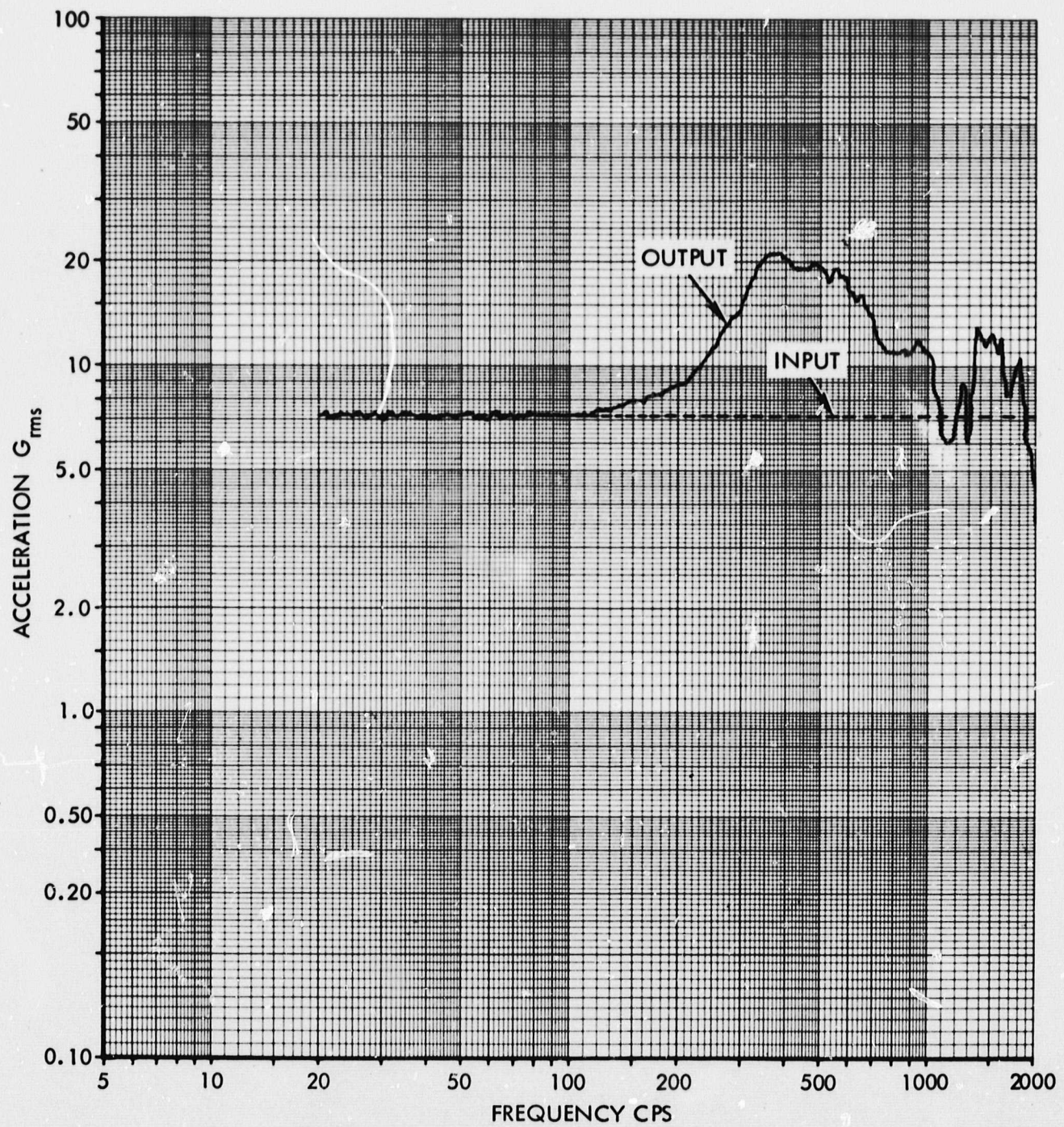
Figure 70. Housing Load Distribution



1858-16

Figure 71. PCM Electronics, Housing, and Internal Structure

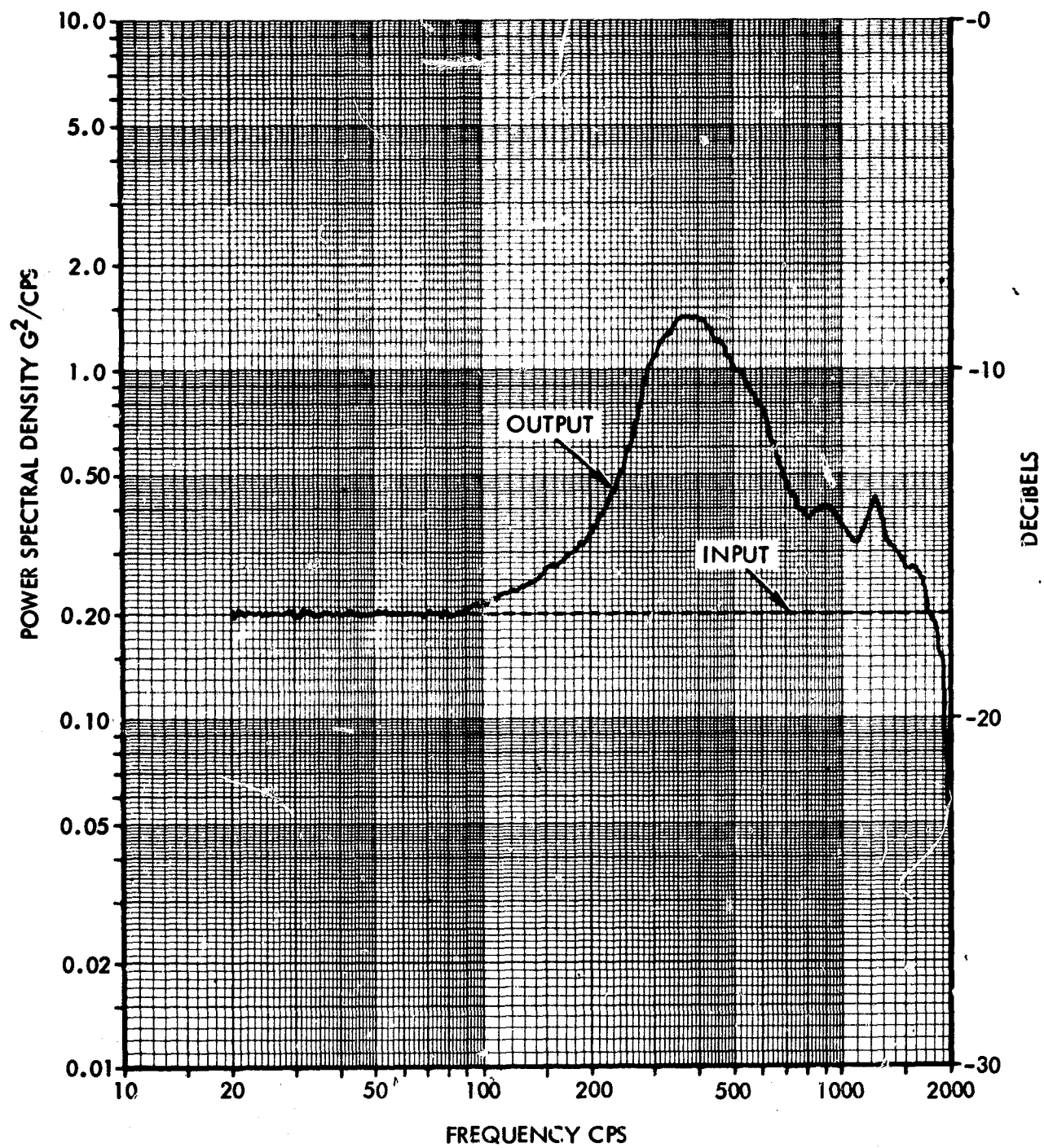
MAXIMUM AMPLIFICATION FACTOR = 3.0



56450-11

Figure 72. Maximum Response Within PCM Unit to Qualification Level Sine Vibration

TOTAL INPUT ACCELERATION: 20.0 G_{rms}
TOTAL RESPONSE ACCELERATION: 28.7 G_{rms}



56450-12

Figure 73. Maximum Response Within PCM Unit to Qualification Level Random Vibration

compressed to 35% of their free thickness, are in a high stress condition and perform with a high degree of efficiency. The success of this packaging technique is illustrated by the fact that there were only negligible differences between simultaneous readings taken at various locations in the electronic stack during the testing.

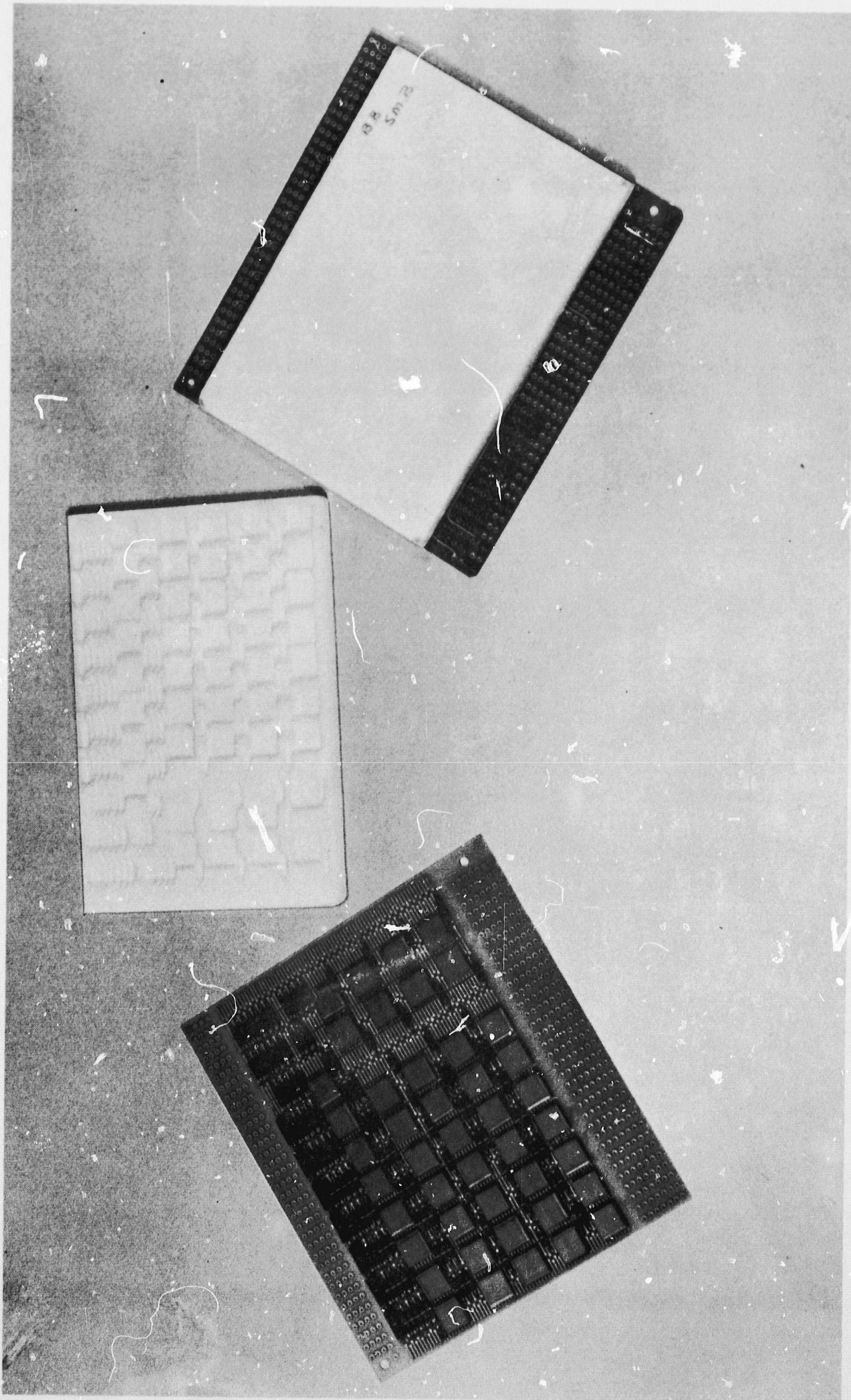
To effectively compression-load the electronics, in which conventional and integrated circuit packages are mounted on the same cards, it was necessary to attain a common height denominator for all of the assemblies. This was accomplished through the use of formed foam shims that conform to the shape of the components on the cards, while also providing a flat surface against which the next card assembly is placed (figure 74). The shims were made using tool cards for each type of planar packaged card in the system. The tool cards utilized dummy components slightly larger than those in the system to prevent loading on the actual system components. A sheet of thin latex rubber was stretched over the tool card and the card was placed in a mold. Foam was poured into the mold and cured. During the curing cycle, the foam expanded and conformed to the inside dimensions of the mold and, by stretching the rubber, assumed the contour of the tool card and its components.

Since the rubber sheet is not affected by either the foam or the curing bake, the mold was easily separated from the tool card.

The foam shim is molded to the exact form factor and component layout of the particular tool card utilized and is, therefore, keyed as to card and placement in the system.

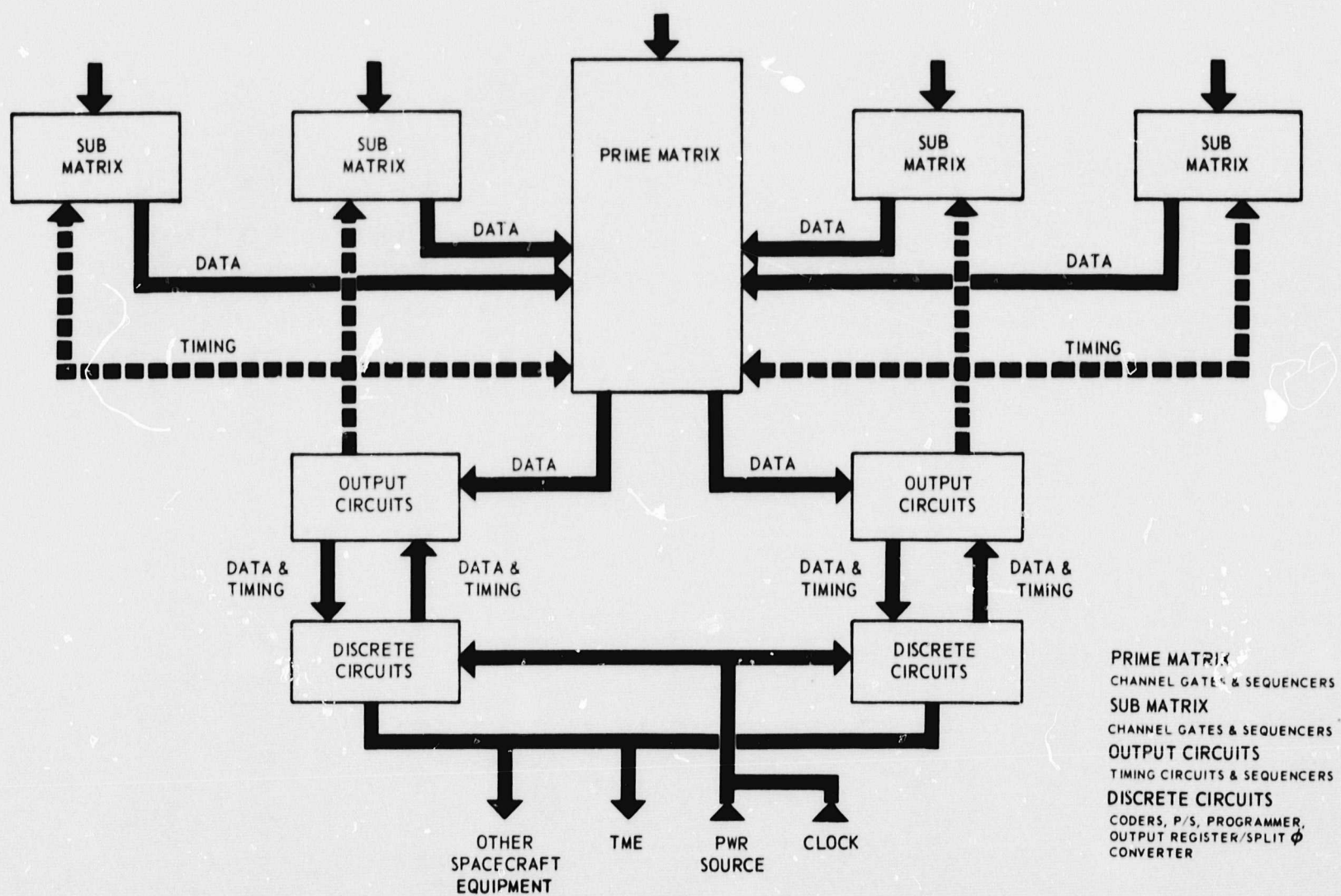
2.4.1.4 SYSTEM ASSEMBLY AND TEST. The card assemblies are wired as functional groups with each group having independent connectors. This type of wiring is possible because of bus wire interconnections in the multiplexer and because the prime and submatrix card assemblies require direct connections only to their transducer inputs (figure 75). All other inputs and outputs must pass through the modular-packaged discrete component portion of the system. Thus, except for the transducer inputs, all inputs are brought into the system through the module card assemblies, from which they are transferred to the output type 1 and 2 cards via point-to-point hard wiring. From these cards, the signals are routed to the multiplexer card assemblies via the rigid wire interconnect system. The data is multiplexed and routed through rigid wires to the output circuit and module card assemblies where it is converted, properly sequenced, and applied to the output register/split-phase converter before transmission to the ground. Power is routed from the power supply module in a similar manner.

This interconnection scheme allows the card assemblies to be wired in the following manner:



56450-13

Figure 74. Tool Card, Formed Shim, and Card/Shim Assembly



56450-14

Figure 75. Nimbus PCM Telemetry Unit Functional/Packaging Block Diagram

<u>Card Assemblies</u>	<u>Number of Connectors per Card Assembly Group</u>
Prime Matrix	1
Submatrix Type A	3
Submatrix Type B	
Output Card Type 1	1
Output Card Type 2	
A/D Converter-Output Register	
Programmer-Power Supply	

Each group of card assemblies is wired to their appropriate connectors in special fixtures (figure 76). The fixtures are designed so that card assemblies and connectors are located relative to each other in the unit, thereby eliminating excessive wire loops and unnecessary strain on the wires and solder joints.

The system is then assembled in its electrical test fixture for preliminary checkout. The card groups, with their respective connector panels, are removed and secured in the system test fixture (figure 77). Electrical contacts connected to jumper wires are then inserted into the AMP sockets to effect electrical interconnection to the cards of the multiplexer. The front panel connectors are mated to cables from the test set, which simulates the spacecraft electrical interfaces.

The complete PCM unit consists of one prime matrix card assembly (non-redundant), four submatrix A and B card assemblies (identical but non-redundant), two output type 1 card assemblies (redundant), two output type 2 card assemblies (essentially identical), two programmer-power supply card assemblies (redundant), and two A/D converter-output register/split-phase converter card assemblies. To test the complete system it would require a fixture capable of handling all 17 card assemblies (A, figure 78); however, the redundancy and similarity of the card assemblies allow the system to be checked out on a reduced system capability basis. By planning fabrication so that one of the prime matrix, submatrix A, submatrix B, output type 1, output type 2, A/D converter-output register, and programmer-power supply card assemblies are completed at the same time, the system can be electrically checked out in a reduced system test fixture (B, figure 78). Checkout of the remaining card assemblies is then accomplished by substituting the functional groups for similar groups in the fixture. This method allows initial system testing to begin when 7 of the total of 17 card subassemblies (41 percent of the system card assemblies) have completed assembly and wiring. Thus, testing can be performed continuously on a parallel path with fabrication for all subsequent systems and parts of systems, regardless of whether all functional groups for that system have completed fabrication. This technique results in substantial savings in test time and costs by allowing 100 percent utilization of test personnel and equipment, by assuring an extremely high degree of confidence in any system prior to its assembly, and by creating minimal down time due to the malfunction of any particular functional unit.

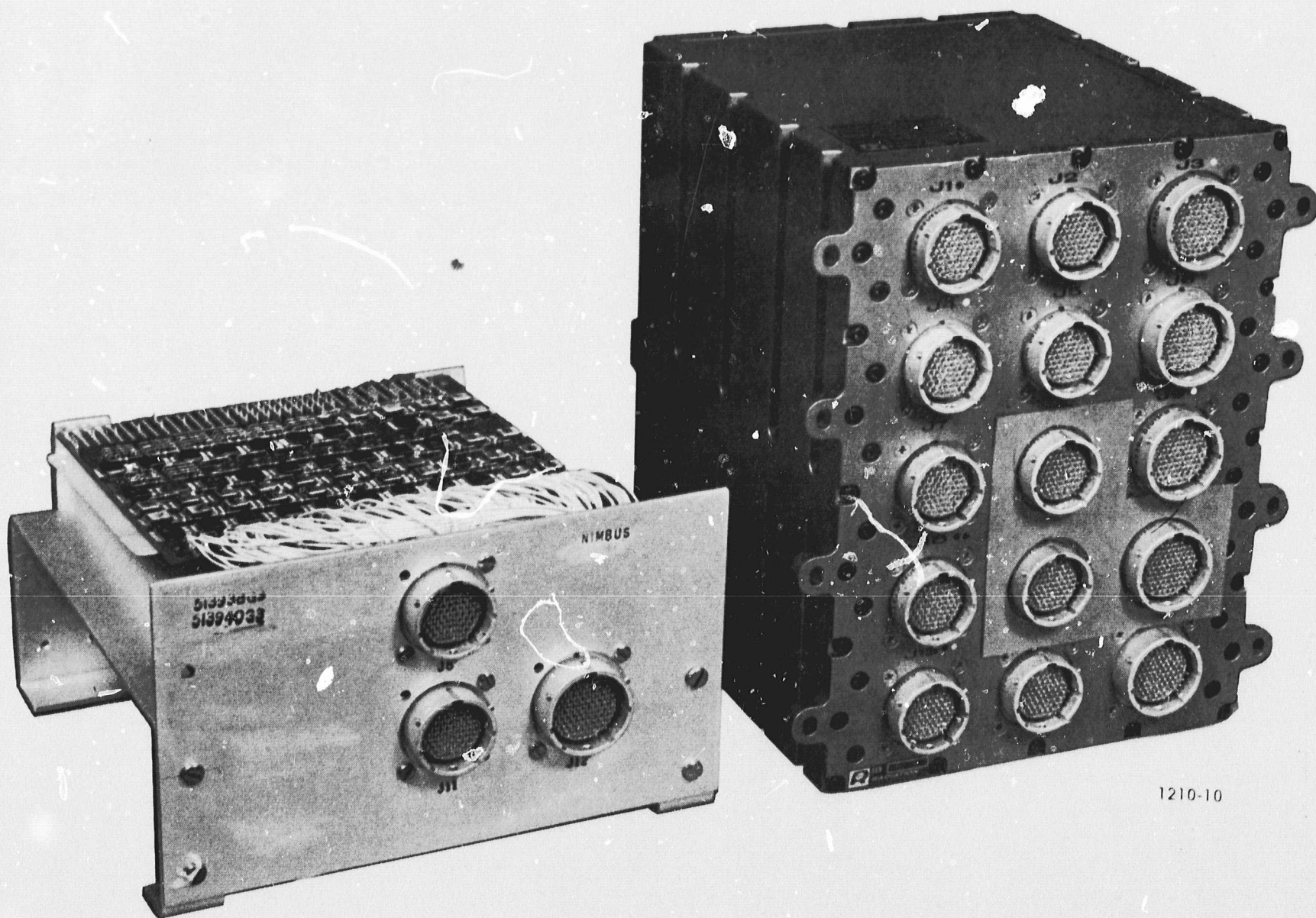
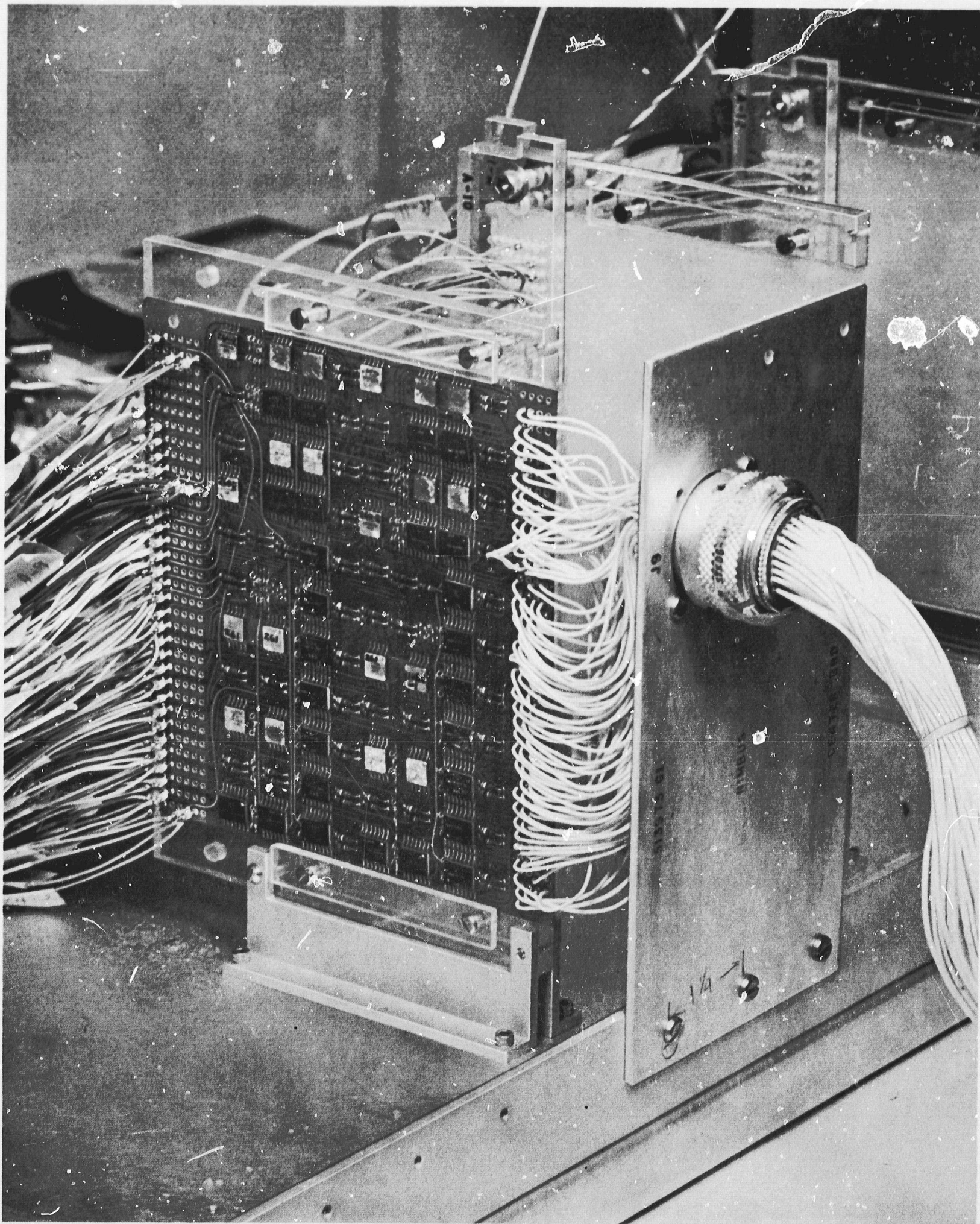
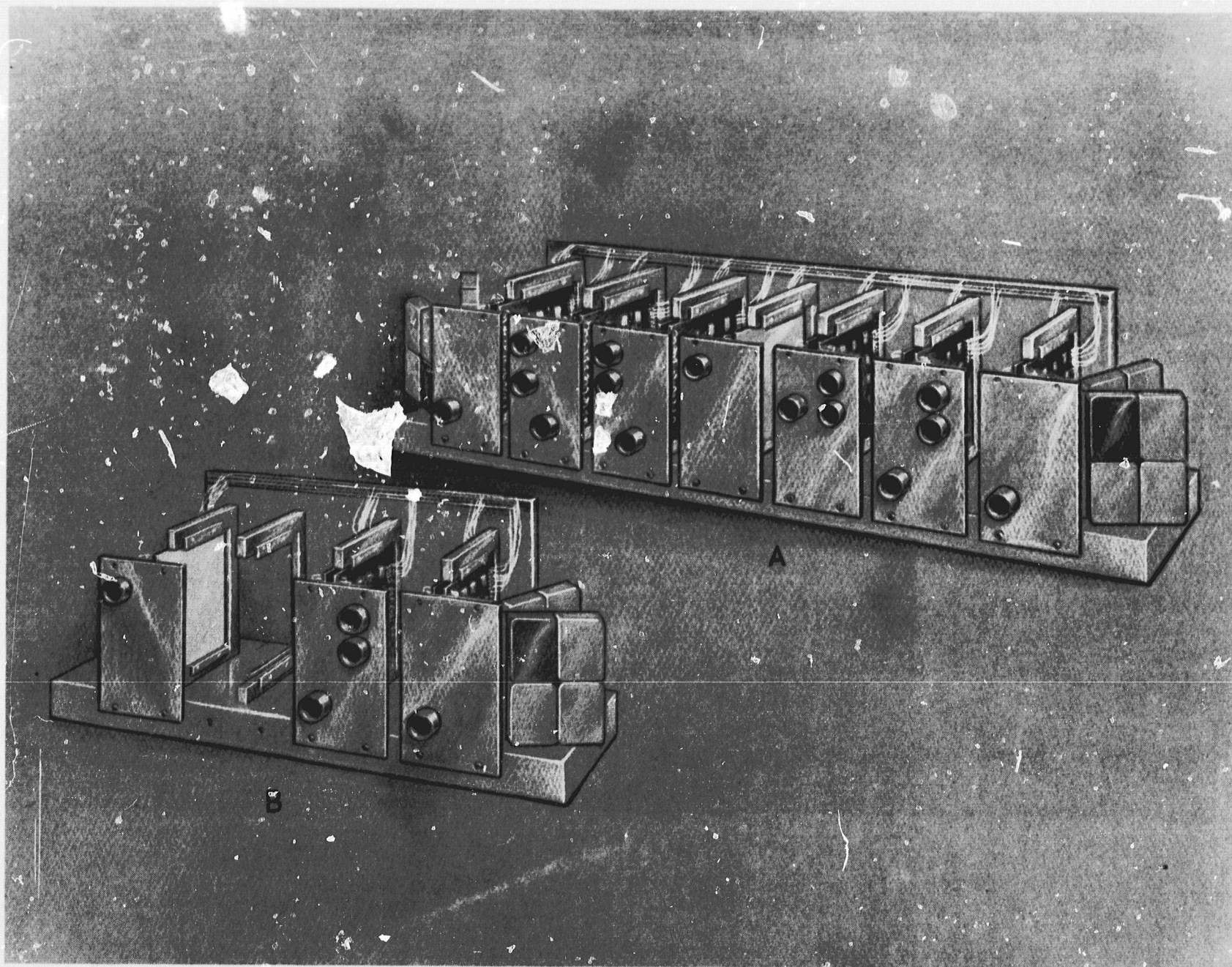


Figure 76. Functional Assembly in Wiring Fixture and Location in PCM Unit



1210-11

Figure 77. Prime Matrix Card Installed in System Test Fixture



56450-17

Figure 78. System Test Fixtures

Final assembly is accomplished when all of the card assemblies have completed electrical test. The card assemblies, with their appropriate foam shims in position, are placed in an alignment fixture. The connectors are secured to the housing front panel, which is then fastened to the front of the fixture. The rigid wires are threaded through their respective AMP sockets and insulating bushings. When the wires are completely through the multiplexer cards, they are nail-headed on both ends to prevent their working out of the contacts. This assembly is then loaded into the electronics support structure with a hydraulic press, and subsequently inserted into the mechanical housing. Following loading of the clamshell halves of the housing (to compress the internal rubber strips), the housing assembly is completed by securing the two halves and the front panel together. Since there is no soldering of wires to be done during these steps, total time for final system assembly (from insertion of the card functional group in the alignment fixture to completion of housing assembly), including inspection by Quality Assurance, is approximately six hours.

2.4.1.5 MAINTAINABILITY AND REPAIRABILITY. The system is repairable to the individual component or integrated circuit. Two levels of maintenance have been considered for the system; maintenance at field and at depot repair levels. Troubleshooting may not be practical under certain conditions; therefore, the housing is designed to be easily removed and replaced in the spacecraft without special tools or equipment.

At the repair depot, the electronics can easily be removed from the housing through use of a hydraulic press. Standard repair procedures are used for removal and replacement of the foamed modules from their card assemblies, and removal of the potting foam and components from the defective module. Component replacement on the planar packaged card assemblies can be effected by removing the malfunctioning card group from the system. This is accomplished by removing the bus wires from the multiplexer card stack and by removing the associated connector(s) from the front panel. Repair at the card level is accomplished by removing the foam shim from the card, unsoldering the defective component, and soldering the replacement component onto the card.

2.4.2 TME UNIT

2.4.2.1 PACKAGING CONCEPT. As with the PCM, the packaging concept for the TME unit utilizes a compression-loading technique that places the electronic under a load using light-weight polyurethane foam potting and spacer material. The resultant package provides protection to the electronics from the exposed dynamic environments.

2.4.2.2 ELECTRONICS PACKAGING. The circuits within the TME can be grouped into five basic functional groups. These groups are the relay and noise suppression circuits, the record amplifier, the playback amplifier, the summing circuits, and the temperature monitoring circuit. A review of this grouping, together with a study of the electrical requirements, indicated that optimum design would result from packaging the record amplifier, playback amplifier, temperature monitor circuit, and the fixed value components of the summing circuits into welded cordwood modules. These circuits are packaged into four modules as follows:

Circuit	No. of Module Types	No. of Modules Per TME
Record Amplifier	1	2
Playback Amplifier		
Monitor Circuit	1	1
Summing Circuitry	<u>1</u>	<u>1</u>
Total	3	4

Since there are two separate recorders, two sets of record/playback amplifiers are needed. For electrical reasons, record amplifier No. 1 is located in the module with playback amplifier No. 2 and record amplifier No. 2 is packaged with playback amplifier No. 1. The modules are electrically interconnected by soldering the modules to printed circuit cards. The variable resistors employed in the summing circuits are located on the front panel so that the adjustments are accessible externally.

The relays and their associated noise suppression components are mounted directly onto printed circuit cards in a planar manner. Interconnection is effected through solder connections to the cards.

The module card is a single-sided card with plated-thru holes. One such module card assembly is required in the TME.

The relay cards are four-layered M/L cards, with circuitry located on all but the top layer (the layer on which all of the components are located). One each of two types of relay card assemblies are required in the TME.

Two ground plane shield cards are used in each TME. These cards are placed between each relay card assembly and the module card assembly to block stray signals that might be emitted by the relays. The shield cards prevent such signals from adversely affecting the circuits in the module card assembly.

A fault protection diode is located on the TME front panel. This is a large, stud-mounted diode that has been mounted on the panel to provide for heat dissipation.

2.4.2.3 MECHANICAL PACKAGING. As with the PCM, the TME unit consists of a pre-loaded electronics assembly. This technique effectively integrates the electronics into one mass, allowing use of a thin-walled light-weight housing design.

The housing assembly consists of three separate parts; the housing bottom, cover, and front panel. The housing bottom is fabricated by machining of a monolithic magnesium block. The cover is a hollow magnesium panel which, when filled with foam and rigidized by a

bonded-on plate, forms a rigid light-weight structure capable of withstanding the bending moments caused by preloading. The front panel is a machined magnesium plate that provides support of the TME in the spacecraft and provides mounting for the external connectors, fault protection diode, and variable resistors.

Internally, the relay card assemblies, the shield cards, and the module card assembly are separated by both foam and Fiberglas loading shims. This grouping is isolated from the housing bottom and housing top cover by foam silicone rubber strips which provide vibration isolation. The strips also provide resonance control by contacting the perimeters of both the box and the electronic assembly, thereby minimizing vibration displacement of the electronics.

Except for the internal support structure and the differences outlined above, the mechanical packaging of the TME is nearly identical to that of the PCM.

2.4.2.4 SYSTEM ASSEMBLY AND TEST. The initial step in the assembly of the TME is preparation for unit test. The relative simplicity of this unit is such that except for the usual module tests, no subunit tests are required. To prepare the TME for unit test, the card assemblies and their associated connectors are hard-wired together, the ground plane cards are installed in the proper locations, and the assembly is mounted to the front panel. The unit is then secured to a holding fixture in which initial unit checkout is performed. Following checkout, the assembly is removed from the fixture and the appropriate compression shims are installed. The assembly is then installed in the housing, the top panel is positioned, and a hydraulic press is used to apply a predetermined load to the stack. While the load is maintained, the top and front panels are secured. The TME unit is removed from the hydraulic press and is then ready for final test.

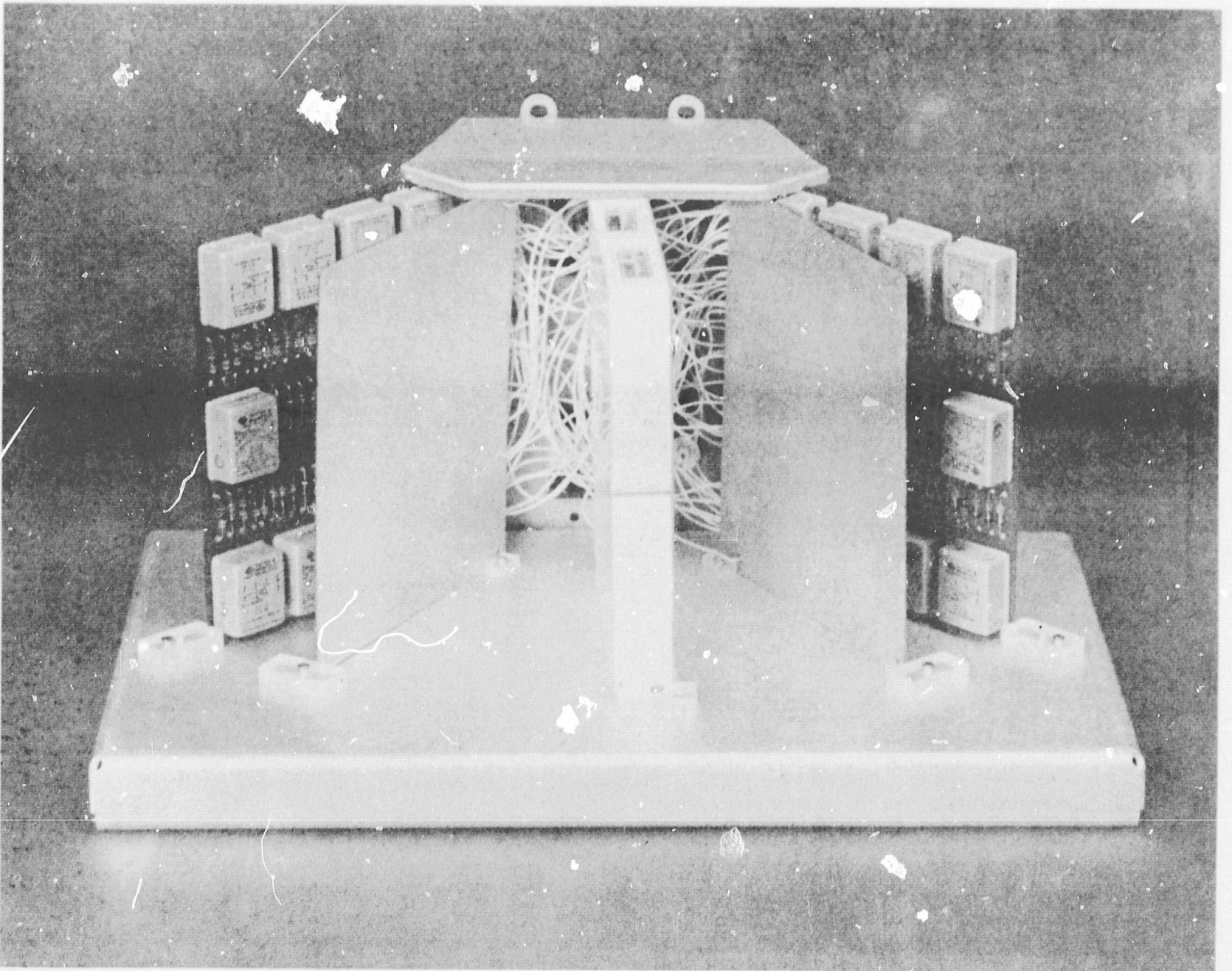
2.4.2.5 MAINTAINABILITY AND REPAIRABILITY. As with the PCM, two levels of maintenance (field and depot) are feasible to provide repairability of the TME to the component level. Since troubleshooting on the field may not be considered expedient, the unit is designed to be easily removed and replaced in the spacecraft without the use of special tools.

At depot level, the electronics are easily removed from the housing through the use of a hydraulic press. Standard repair procedures are used to remove and replace the foamed modules from their card assemblies, and to remove the potting foam and components from the defective module. Component replacement on the planar-packaged cards (relay/component cards) is effected by fanning the card stack apart (figure 79), unsoldering the defective component, and soldering the replacement onto the card.

2.5 DESIGN TESTING.

2.5.1 ELECTRICAL TEST AND DEMONSTRATION.

The Nimbus Study system testing falls into four categories: (a) breadboard design proof-testing, (b) module or functional unit testing, (c) complete system testing, and (d) problem areas encountered and retesting.



C1858-2

Figure 79. TME Card Stack

2.5.1.1 BREADBOARD DESIGN PROOF TESTS. The breadboard design proof tests include voltage variation tests and temperature tests. These tests were applied to the discrete component module breadboards and to the integrated circuit partial multiplexer breadboard. The only critical circuits involving both temperature and voltage are the analog-to-digital converter (coder), the dc-to-dc converter (power supply), the summing amplifiers, and the record/playback amplifiers. All other circuits are digital, saturated switching circuits that have a high degree of engineering confidence based upon past performance history and, therefore, do not require extensive additional testing. All circuits operated properly with ± 10 to 20% voltage variation in the temperature range of -10°C to $+65^{\circ}\text{C}$. With the voltage remaining within $\pm 5\%$ of nominal, the temperature range for proper operation can be from -20°C to $+75^{\circ}\text{C}$. The controlling factor is the analog accuracy of the coder.

2.5.1.2 MODULE OR FUNCTIONAL UNIT TESTING. All discrete component modules were tested in module test fixtures. The four fixtures listed below were built specifically to test modules and a specification was written to perform the tests and to accumulate data by module serial number.

- a. Programmer Test Fixture - checks all three programmer modules, the signal monitor module, the shift register module, and the coder 3 module.
- b. Coder Test Fixture - checks all three coder modules.
- c. Power Supply Test Fixture - checks the power supply module.
- d. Record/Playback/Summing Amplifier Test Fixture - checks the summing amplifier module and the record/playback amplifier modules.

An additional test fixture was fabricated to check all integrated circuit flat-packs except the MOSFET gates. A MOSFET flat-pack tester had been previously fabricated for another project and was made available for use in the Nimbus program.

Temperature tests, from -10°C to $+75^{\circ}\text{C}$, were run on the coder modules, summing amplifier modules, and the record/playback amplifier modules. All other discrete component modules and the integrated circuit flat packs had sufficient engineering confidence (and no select-at-test resistors) that no temperature tests were deemed necessary at this stage of fabrication.

There are no individual card test fixtures on the Nimbus Study program; however, it has been determined that they are necessary to reduce final test time. Card test fixtures will be designed, fabricated, and used on the Nimbus B program.

2.5.1.3 COMPLETED SYSTEM TESTING. The completed PCM and TME were integrated with the modified BTE and two Raymond tape recorders before the final temperature tests were conducted. The final temperature tests employed temperatures from -10°C to $+60^{\circ}\text{C}$, with the PCM and TME units being stabilized at each temperature extreme for approximately four hours. No electrical problems were encountered until the line voltage was increased to -35 volts.

In fact, all circuits functioned normally and were essentially the same at both temperature extremes as they were at room ambient. All measured data was either recorded in the system log or was directly compared with the same data taken at +25°C. (The complete test procedure has been submitted under separate cover.) All problems that were encountered during testing are discussed in the following paragraph.

2.5.1.4 PROBLEM AREAS ENCOUNTERED AND RETESTS PERFORMED.

2.5.1.4.1 PROBLEM NO. 1. When the power line voltage was increased from -24.5 volts to -35 volts, the output voltages from the PCM power supply increased, giving the appearance of regulator thermal runaway. The cause of the problem was that the RFI ground inside the power supply was returned to a -24.5-volt return which forward-biased a tantalum capacitor. As the voltage was increased, this capacitor began to leak sufficiently to completely bypass the series regulator. Thus, the output voltage was changing proportional to the input line voltage. To solve this problem, the RFI ground connection was removed so that it cannot be grounded to the -24.5-volt return.

2.5.1.4.2 PROBLEM NO. 2. Several analog and digital channels were lost during temperature changes because of faulty solder connections on several of the flat packs. The unit was disassembled and a microscope was used to examine all solder connections. The poor solder connections were resoldered and all channel gates were then 100-percent operational.

2.5.1.4.3 PROBLEM NO. 3. The coder switching points on the coder for PCM No. 2 were offset by approximately 18 millivolts. The trouble was caused by a permanent offset present in the coder calibrate circuit which may have been introduced while isolating the many multiplexer MOSFET problems. This problem was solved by reselecting the coder select-at-test resistors.

2.5.1.4.4 PROBLEM NO. 4. The overvoltage circuits did not function properly to read out all ONE's. It was then discovered that the GPA's were incorrectly wired and were not being duty-cycled. When the wiring was corrected, the input capacitors to the GPA's had to be replaced with resistors so that ONE's could be read out properly when more than -6.4 volts was placed on any analog channel. After that problem was corrected, noise (caused by the 0.2-microsecond leading edge of the GPA turn-on pulse) false-triggered the output register by setting in too many ONE's. To remove that problem, an RC filter was added to the -26-volt duty-cycle pulse line to increase the rise time to 5 to 10 microseconds.

2.5.1.4.5 PROBLEM NO. 5. After problem No. 4 was removed, the PCM was operating properly, but the unit was in the open configuration such that the cards were separated by approximately 3 inches of air space. When the cards were compressed into the final configuration, both coders had a sudden increase in full-scale voltage from approximately -6.401 volts to -6.413 volts for PCM No. 1, and -6.415 volts for PCM No. 2. The only possible cause for the full-scale voltage increase would be that the voltage calibrate reference increased. Since both coders increased and remain within ± 3 millivolts of the average straight line from minimum scale (0 volts) to the new full scale (-6.415 volts), the problem affects both coders. The only difference in the newly-compressed PCM unit is that the GPA's are duty-cycled. The duty-

cycling involves a -26 volts power switch which can produce noise in adjacent circuits that will increase as the circuits are compressed together. The PAM lines into both coders are routed through the multiplexer amplifier interconnect area close to the -26 volt power switching circuit. To solve this problem on the Nimbus B program, an analog MOSFET gate will be added inside the coder. The gate will be connected in series with the PAM line so that the PAM line to the multiplexer will be disconnected during the calibrate cycle. This will prevent multiplexer noise from affecting the full scale calibrate cycle, and will also protect the front end of the coder from accidental shorts during multiplexer preliminary check-out.

2.5.1.4.6 PROBLEM NO. 6. The last problem involved the amount of retesting required to prove out the de-bugged system. The final system was retested by repeating the demonstration test plan and by retaking the data. The PCM unit was demonstrated and delivered for integration with only one uncorrected problem (problem No. 5). The coder linearity curves are shown in the demonstration test plan supplied separately.

2.5.2 MECHANICAL TESTING

2.5.2.1 GENERAL. An analysis of the system electrical, packaging, and mechanical design indicated that the vibration environment would be the most severe condition to which the PCM and TME units would be exposed. To verify design in this area, mechanical models of the PCM and TME were built. These models simulated actual size, weight, configuration, and construction techniques. The units were subjected to vibration qualification levels in both sine and random modes. The vibration limits are listed in tables 14 and 15.

Table 14. Sine Vibration Limits

Frequency Range (CPS)	Amplitude - Zero to Peak (G's)	
	Thrust Axis	Transverse Axes
5-200	15	10
200-2000	10	10
Notes: 1. Vibration limited to 1/4" single amplitude. 2. Sweep Rate - one octave per minute.		

Table 15. Random Vibration Limits

Direction	Frequency Band (CPS)	Spectral Density (G ² /CPS)	G RMS
Thrust Axis	20-2000	0.2	20
Transverse Axes	20-2000	0.2	20
Note: Duration was 4 minutes in each direction for a total of 12 minutes.			

The test details for each unit are contained in Appendix IV . A summary of the vibration tests is contained in the following paragraphs .

2.5.2.2 PCM UNIT . Vibration testing of the PCM (figure 80) proceeded smoothly and without interruption from start to finish . At least two qualification-level input sine and random test runs were run and monitored in each of the three axes . As shown in the X-Y plots (Appendix IV), the maximum Q observed in the electronics stack was 5.5 during run No. 48, while Q's of 4 and less were the rule . Based on the mechanical test data, no problems are foreseen with regard to the ability of the PCM to successfully pass environmental testing in its present mechanical configuration .

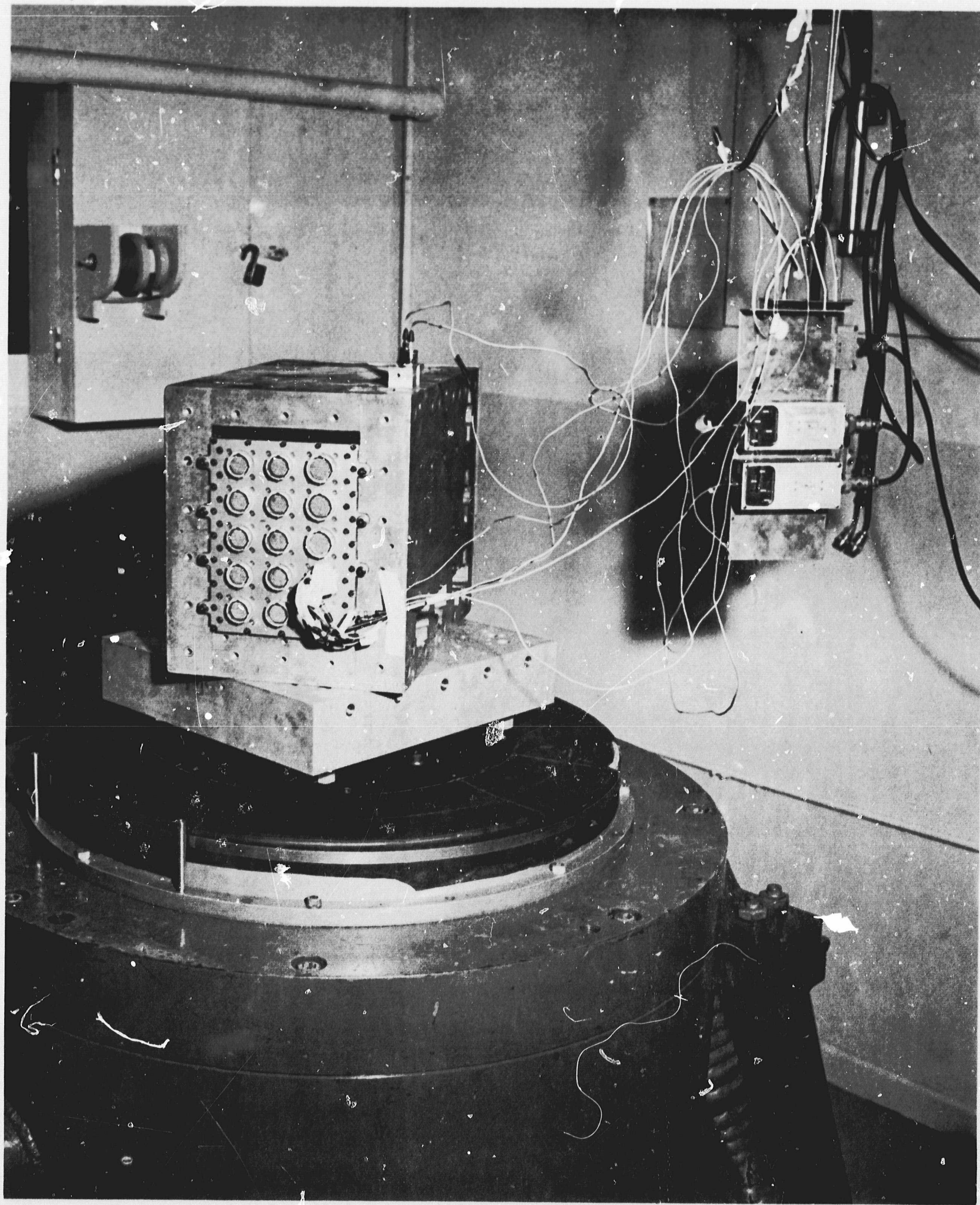
2.5.2.3 TME UNIT . The vibration testing of the TME (figure 81) was halted when an audible rattle was detected during final random qualification level test in the lateral axis . The rattle developed after the unit had successfully passed qualification level vibrations in both the vertical and longitudinal axes (refer to Appendix IV) and had been vibrated for a total of 14 runs . Disassembly of the TME disclosed that wear on the circuit board had created excessive board-to-housing clearance . The wear occurred at the contact surface where the loading feet meet the circuit board . Three factors, none of which will exist on future assemblies, were found to be responsible for this wear problem .

The first problem was that improper sizing of the boards greatly reduced their ability to withstand wear . In an effort to build a system for mechanical evaluation before the design was finalized, scheduling dictated that the boards be sized in a manner other than that normally prescribed . At the time, the sizing technique employed was not felt to be significantly detrimental to the integrity of the boards . By employing the proper sizing technique, board strength will not be affected during the sizing operation and this problem will not exist in the future .

The second problem was erroneous chamfering of the front edge of the board (A, figure 82). This increased the load pressure of the board and, correspondingly, the frictional drag at the board-to-loading feet contact surface by 33 percent . A lack of readily available replacement boards necessitated that the boards be used even though they had been erroneously chamfered . A properly sized board will not have a chamfer at the board-to-loading feet contact surface and this problem will not exist on future boards (B, figure 82).

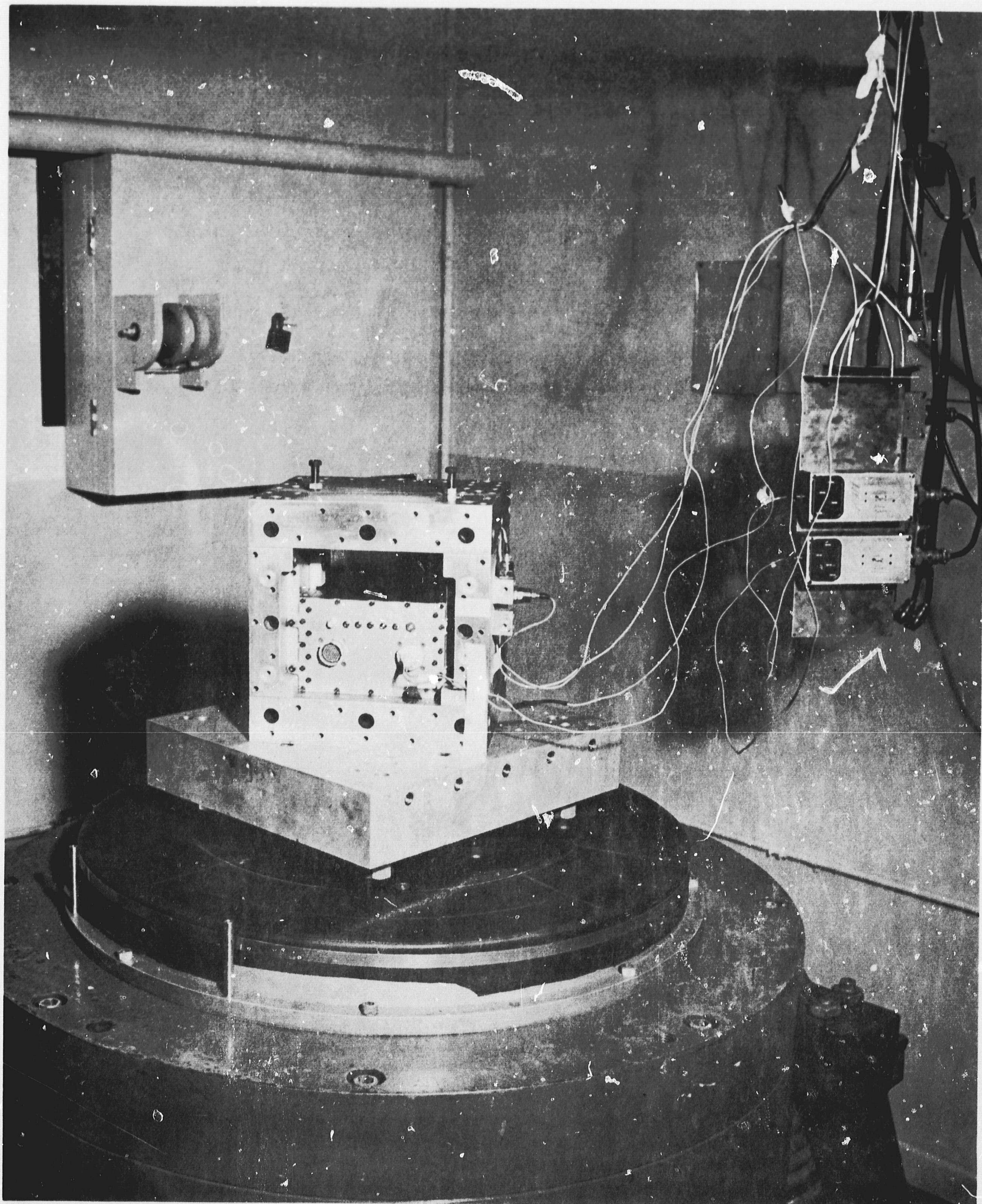
The final problem resulted from insufficient support to the frontal area of the card stack in the longitudinal axis . The lack of support in the longitudinal axis permitted excessive board movement . This problem was solved by the addition of a 1/4-inch strip of silicone rubber, located to add support to the card stack in the longitudinal axis (B, figure 82). Verification of the validity of the correction was obtained in that examination of the circuit board after a total of nine subsequent vibratory runs (refer to Appendix IV) indicated no discernible wear .

By using properly sized boards that conform to the correct board dimensions and with the addition of the rubber strip previously mentioned, no problem is expected regarding the ability of the TME to successfully pass the vibration test .



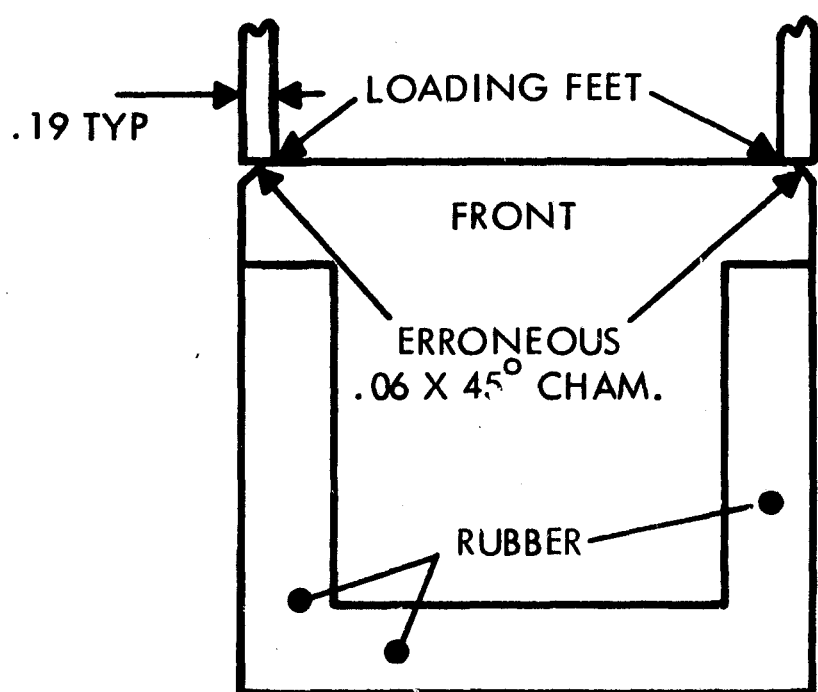
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Figure 80. PCM Vibration Testing

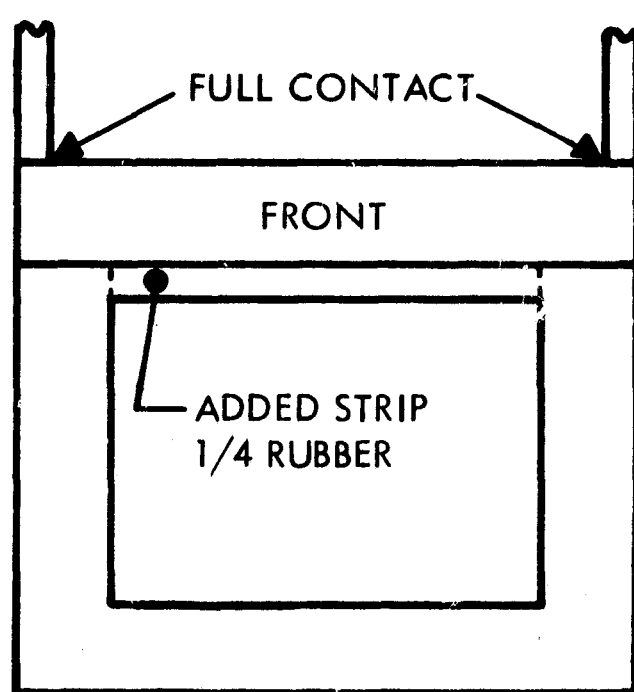


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Figure 81. TME Vibration Testing



TOP VIEW A



TOP VIEW B

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Figure 82. TME Board/Loading Feet Contact Surface

2.6 RELIABILITY.

The following paragraphs present the reliability assessment, failure effects analysis, parts selection, and failure history for the Nimbus Design Study telemetry equipment. A detailed listing of the failure rate for each subassembly is contained in Appendix III.

A summary of the probability of success for each mode of operation for the equipment, including Government-furnished equipment (GFE) recorders and transmitters, is as follows:

<u>Mode of Operation</u>	<u>Probability of Success</u>
Record/Playback	.8949
Time Code Plus Real Time	.8807
Time Code Less Real Time	.8885
Time Code Bypass	.8922

All reliability calculations are based on a 6-month (4380-hour) mission time. The probability of success as a function of mission time is shown in figure 83 for the record/playback and time code plus real time modes. The remaining modes, time code less real time and time code bypass, are not shown because the graphical presentation would become overly complicated due to closeness of the curves.

2.6.1 SUBSYSTEM RELIABILITY NUMERICAL ASSESSMENT.

The following paragraphs present mathematical techniques which, when used to form the mathematical model of the subsystem, best reflect the electrical configuration of the equipment. The diagrams graphically and numerically display the probability of success for each function performed by the equipment and are not intended to show signal flow.

2.6.1.1 NONREDUNDANT COMPONENTS. The mechanism underlying the exponential reliability function of nonredundant components is that of random or chance failures that are independent of accumulated life and are individually unpredictable. This type of "failure law" for complex systems is used because different part failure rates, varying deterioration mechanisms, varying environmental conditions, etc., result in stress-strength combinations that produce failures randomly in time.

Exponential and Poisson distributions are equivalent except for the choice of the random variable. For the exponential, the random variable is the time-to-failure; for the Poisson, the random variable is the number of failures per given time period when failure times are exponentially distributed.

The exponential reliability expression is derived from the Poisson distribution as the probability of zero failures in the interval $[0, t]$.

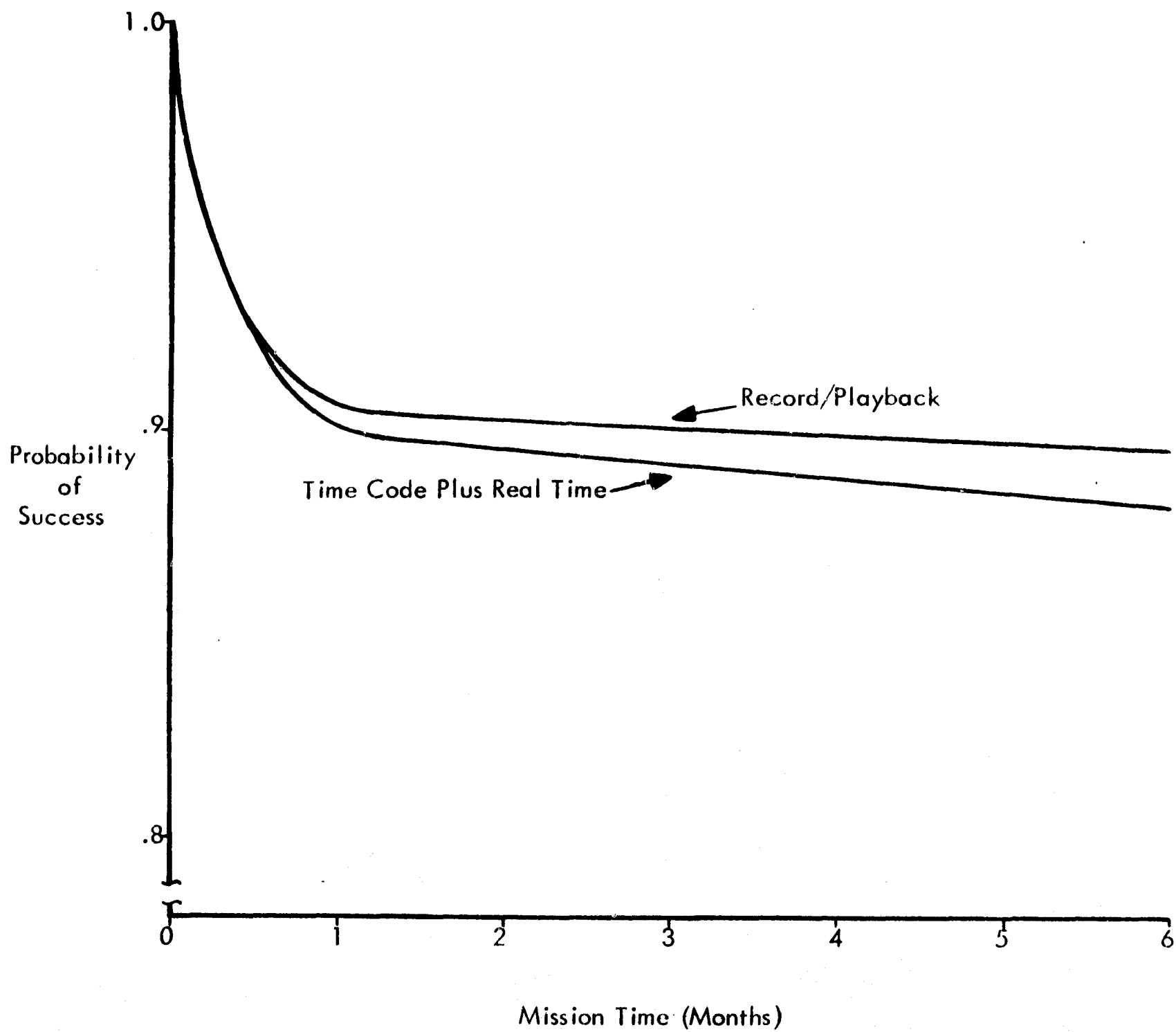


Figure 83. Probability of Success Versus Mission Time

$$R = e^{-\lambda t}$$

where R = reliability or probability of success

λ = failure rate

t = mission time

2.6.1.2 REDUNDANT COMPONENTS. The expression used to represent the probability of successful operation for redundant components, whereby the active component fails at some time (t_1) and the standby component is switched into operation for the remaining mission time, is derived as follows:

Success can be achieved in the following ways:

- Components A and B succeed to time t (mission duration).
- Component A fails at time t_1 , less than t , and component B must operate to time t . (The switch must work at time t_1 .)
- Component A succeeds to time t and the standby component B fails.

Translating the preceding three conditions of success into time independent probabilities:

$$R(t) = e^{-\lambda_A t} + \lambda_A e^{-\lambda_B t} \int_0^t e^{-(\lambda_A + \lambda_S)t_1} dt_1$$

where λ_A = failure rate of the initially active component

λ_B = failure rate of the standby component

λ_S = failure rate of the switch

Solution of the above equation yields:

$$R(t) = e^{-\lambda_A t} + \frac{\lambda_A}{\lambda_A + \lambda_S} e^{-\lambda_B t} \left[1 - e^{-(\lambda_A + \lambda_S)t} \right]$$

When redundant components A and B have the same failure rate, this equation reduces to:

$$R(t) = e^{-\lambda_A t} \left[1 + \frac{\lambda_A}{\lambda_A + \lambda_S} \left(1 - e^{-(\lambda_A + \lambda_S)t} \right) \right]$$

2.6.1.3 ALLOWABLE CHANNEL LOSS. The allowable loss of eight analog and seven digital inputs has been introduced to define mission success. With this definition of success, the binomial distribution is applicable. However, when the number of channels is large and single channel failure probability is small, the Poisson distribution is a close approximation to the binomial. The reliability expression becomes:

$$R = \sum_{r=0}^X \frac{a^r e^{-a}}{r!}$$

where R = reliability

$$a = \lambda t$$

λ = total failure rate

t = mission time

X = number of allowable failures

Where circuit configuration is such that a single failure will cause maximum allowable data loss for mission success, the expression above reduces to:

$$R = e^{-\lambda t} (1 + \lambda t)$$

2.6.1.4 PCM BLOCK ANALYSIS. For analysis purposes, the PCM subsystem is divided into nonredundant input circuits and redundant blocks, (figure 84).

2.6.1.4.1 NONREDUNDANT INPUT CIRCUITS ($P_1 = .9617$). The PCM subsystem is a block-redundant configuration except for the multiplexer submatrix input gates. These nonredundant gates are divided into the following subsections:

- a. Prime Digital ($R_{PD} = .9996$)
- b. Subcom Digital ($R_{SCD} = .9933$)
- c. Prime Analog ($R_{PA} = .9997$)
- d. Subcom Analog ($R_{SCA} = .9689$)

The mathematical model for multiplexer input gates is as follows:

$$P_1 = R_{PD} R_{SCD} R_{PA} R_{SCA}$$

where R_{PD} = reliability of prime digital gates with one allowable failure

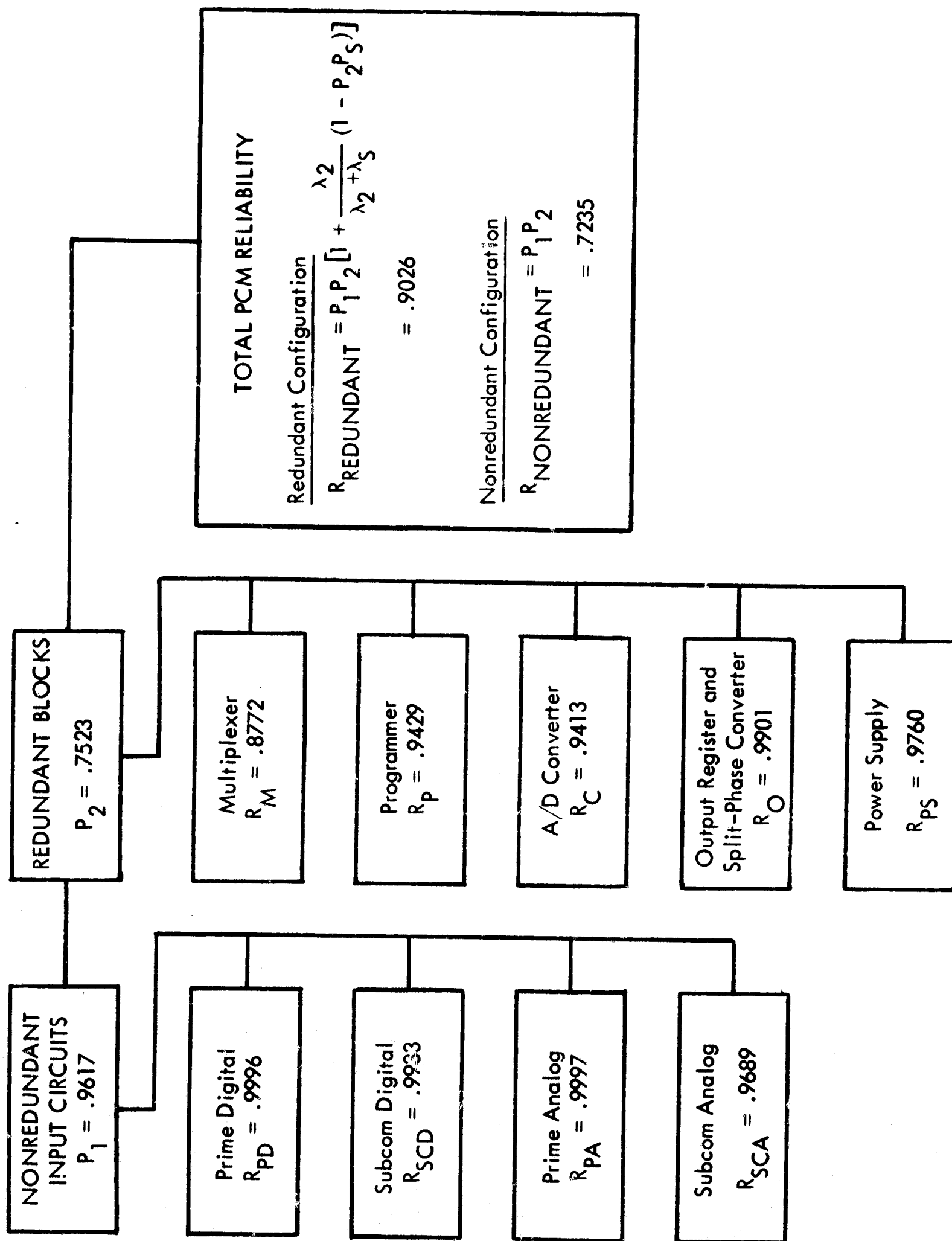


Figure 84. PCM Reliability Diagram

R_{SCD} = reliability of subcom digital gates with one allowable failure

R_{PA} = reliability of prime analog gates with one allowable failure

R_{SCA} = reliability of subcom analog gates with one allowable failure

2.6.1.4.2 REDUNDANT BLOCK ($P_2 = .7523$). PCM redundant circuits are divided into the following subsections:

a. Multiplexer ($R_M = .8772$)

b. Programmer ($R_P = .9429$)

c. A/D Converter ($R_C = .9413$)

d. Output Register and Split-Phase Converter ($R_O = .9901$)

e. Power Supply ($R_{PS} = .9760$)

The mathematical model for the redundant circuits is as follows:

$$P_2 = R_M R_P R_C R_O R_{PS}$$

where

R_M = reliability of redundant multiplexer circuits

R_P = reliability of programmer

R_C = reliability of A/D converter

R_O = reliability of output register and split-phase converter

R_{PS} = reliability of power supply

2.6.1.4.3 TOTAL PCM RELIABILITY ($R = .9026$). The mathematical model for the complete PCM subsystem is as follows:

$$\begin{aligned} R &= e^{-\lambda_1 t} \left\{ e^{-\lambda_2 t} \left[1 + \frac{\lambda_2}{\lambda_2 + \lambda_S} \left(1 - e^{-(\lambda_2 + \lambda_S) t} \right) \right] \right\} \\ &= P_1 P_2 \left[1 + \frac{\lambda_2}{\lambda_2 + \lambda_S} (1 - P_2 P_S) \right] \end{aligned}$$

where

$P_1 = e^{-\lambda_1 t}$ = probability of success of multiplexer input circuits with allowable losses

$$P_2 = e^{-\lambda_2 t} = \text{probability of success of redundant circuitry}$$

$$P_S = e^{-\lambda_S t} = \text{probability of success of switching circuitry}$$

PCM subsystem reliability, in a nonredundant configuration, is shown in the following mathematical model for comparative purposes:

$$\begin{aligned} R &= P_1 P_2 \\ &= .7235 \end{aligned}$$

2.6.1.5 TME BLOCK ANALYSIS. For analysis purposes, the TME subsystem is divided into four modes of operation, the redundant record/playback blocks and the nonredundant real time and time code circuitry (figure 85). The GFE tape recorders and transmitters that interface with the TME are included in the analysis.

2.6.1.5.1 COMMON EQUIPMENT ($P_{CE} = .9978$). The following equipment is common to all modes of operation:

a. Summing Amplifier ($P_{SA} = .9964$)

b. Transmitter ($P_T = .9527$)

The mathematical model for these redundant blocks is as follows:

$$P_{CE} = \left\{ P_{SA} \left[1 + \frac{\lambda_{SA}}{\lambda_{SA} + \lambda_{S2}} (1 - P_{SA} P_{S2}) \right] \right\} \left\{ P_T \left[1 + \frac{\lambda_T}{\lambda_T + \lambda_{S3}} (1 - P_T P_{S3}) \right] \right\}$$

where P_{SA} = probability of success of summing amplifier

P_T = probability of success of transmitter

P_{S2} = probability of success of switching circuitry for the summing amplifier

P_{S3} = probability of success of switching circuitry for the transmitter

2.6.1.5.2 RECORD/PLAYBACK ($R_{R/P} = .9915$). The mathematical model for the record/playback mode of operation is as follows:

$$R_{R/P} = P_{CE} \left\{ P_{R/P} \left[1 + \frac{\lambda_{R/P}}{\lambda_{R/P} + \lambda_{S1}} (1 - P_{R/P} P_{S1}) \right] \right\}$$

where P_{CE} = probability of success of common equipment (summing amplifiers, transmitters, and associated switching circuits)

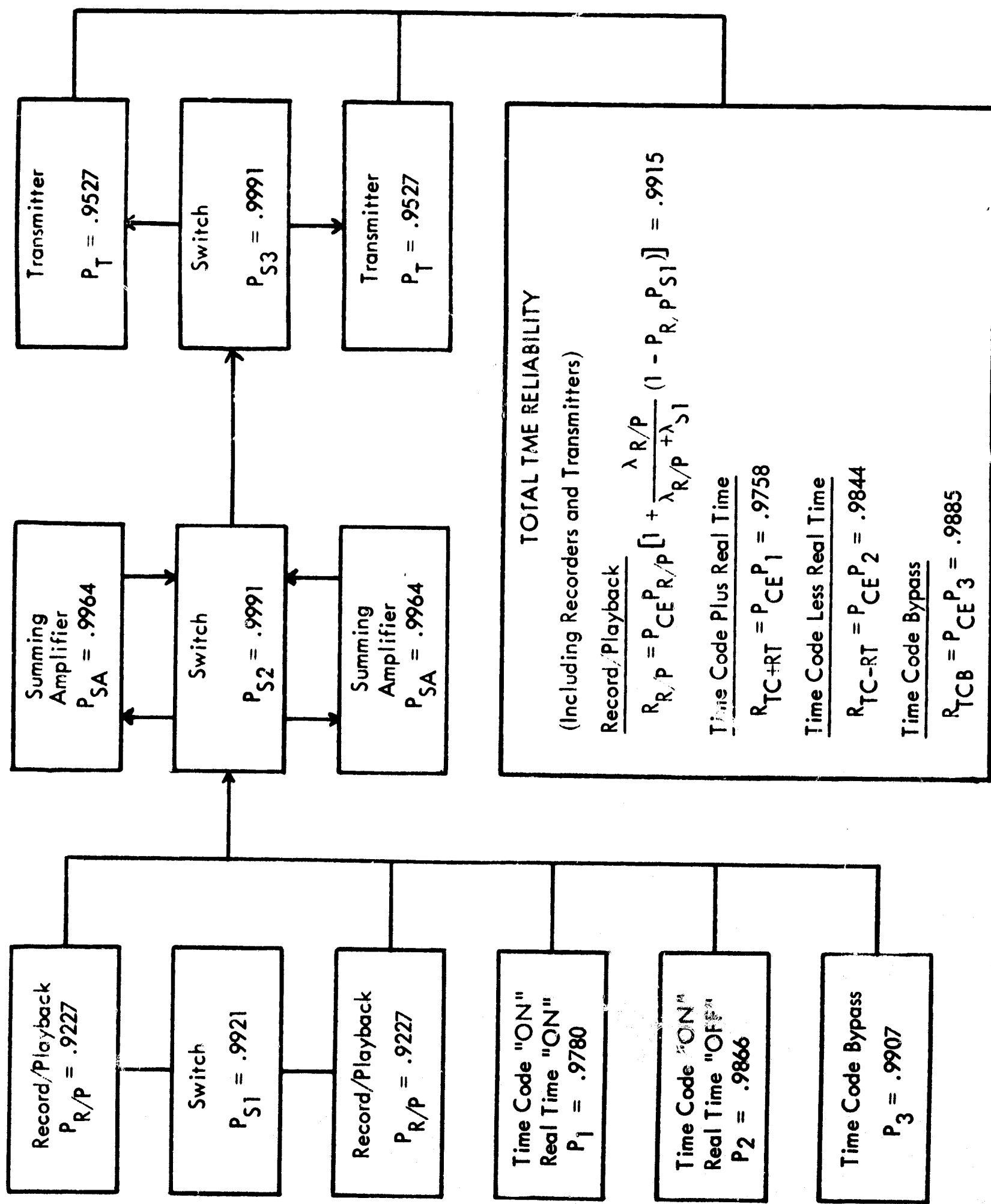


Figure 85. TME Reliability Diagram

$P_{R/P}$ = probability of success of recorder, record amplifier, and playback amplifier

P_{S1} = probability of success of record/playback switching circuits

2.6.1.5.3 TIME CODE "ON," REAL TIME "ON" ($R_{TC+RT} = .9758$). Nonredundant, internal TME components required for this mode of operation are:

<u>Component</u>	<u>N</u>	<u>$N\lambda \times 10^{-5}$</u>
Relay	4	0.080
Resistor, Variable WW	2	0.266
Resistor, Metal Film	4	0.088
Capacitor, Tantalum	2	<u>0.074</u>
Total Failure Rate		0.508

$$P_1 = e^{-N\lambda t} = .9780$$

The mathematical model for time code plus real time mode of operation is as follows:

$$R_{TC+RT} = P_1 P_{CE}$$

where P_1 = probability of success of TME nonredundant circuitry

P_{CE} = probability of success of common equipment

2.6.1.5.4 TIME CODE "ON," REAL TIME "OFF" ($R_{TC-RT} = .9844$). Nonredundant, internal TME components required for this mode of operation are:

<u>Component</u>	<u>N</u>	<u>$N\lambda \times 10^{-5}$</u>
Relay	4	0.080
Resistor, Variable WW	1	0.133
Resistor, Metal Film	1	0.022
Capacitor, Tantalum	2	<u>0.074</u>
Total Failure Rate		0.309

$$P_2 = e^{-N\lambda t} = .9866$$

follows: The mathematical model for time code less real time mode of operation is as

$$R_{TC-RT} = P_2 P_{CE}$$

where P_2 = probability of success of TME nonredundant circuitry

P_{CE} = probability of success of common equipment

2.6.1.5.5 TIME CODE BYPASS ($R_{TCB} = .9885$). Nonredundant, internal TME components required for this mode of operation are:

<u>Component</u>	<u>N</u>	<u>$N\lambda \times 10^{-5}$</u>
Relay	1	0.020
Resistor, Variable WW	1	0.133
Resistor, Metal Film	1	0.022
Capacitor, Tantalum	1	<u>0.037</u>
Total Failure Rate		0.212

$$P_3 = e^{-N\lambda t} = .9907$$

The mathematical model for time code bypass mode of operation is as follows:

$$R_{TCB} = P_3 P_{CE}$$

where P_3 = probability of success of TME nonredundant circuitry

P_{CE} = probability of success of common equipment

2.6.1.6 TOTAL SYSTEM RELIABILITY. A summary of the reliability calculations discussed in the preceding paragraphs is as follows:

$$R_{PCM} = .9026$$

$$R_{R/P} = .9915$$

$$R_{TC+RT} = .9758$$

$$R_{TC-RT} = .9844$$

$$R_{TCB} = .9885$$

Total system reliability is calculated for each mode of operation as follows:

$$\begin{aligned}
 R_{\text{EQUIPMENT}} &= R_{R/P} R_{\text{PCM}} = .8949 && \text{Record/Playback} \\
 &= R_{\text{TC}+\text{RT}} R_{\text{PCM}} = .8807 && \text{Time Code Plus Real Time} \\
 &= R_{\text{TC}-\text{RT}} R_{\text{PCM}} = .8885 && \text{Time Code Less Real Time} \\
 &= R_{\text{TCB}} R_{\text{PCM}} = .8922 && \text{Time Code Bypass}
 \end{aligned}$$

Monitor circuits are considered nonessential to mission success and are not included in the above equipment reliability calculations.

2.6.1.7 MONITOR CIRCUITS. Reliability of the components used to monitor environmental conditions within the equipment is listed below:

<u>Component</u>	<u>N</u>	<u>$N\lambda \times 10^{-5}$</u>
Monitor Module	1	0.082
Thermistors	5	0.150
Diode	1	0.001
Resistor, Carbon Comp.	1	<u>0.001</u>
Total Failure Rate		0.234

$$R_{\text{MONITOR}} = e^{-N\lambda t} = .9898$$

2.6.2 FAILURE RATE CONSIDERATIONS.

Failure rates for discrete components were selected at appropriate stress levels from MIL-HDBK-217. Failure rates for semiconductor devices were improved by a factor of 10:1 to reflect improvements realized from power aging. This improvement factor is based on data obtained from GSFC Document X-650-65-105, "A Comparison of Burn-In and Bake As Semiconductor Screening Techniques For the Nimbus Spacecraft Program," dated March 1965.

Failure rates for multiplexer components were obtained from the latest manufacturer-supplied testing information, as follows:

- a. MOSFET 0.03%/1000 hours
- b. Integrated Devices 0.016%/1000 hours
- c. Custom Device (GPA) 0.04%/1000 hours

Failure rates for record/playback and erase heads were not included in MIL-HDBK-217 and were obtained from "Failure Rate Data Handbook (FARADA)," dated 1 March 1965, that was supplied by the Bureau of Naval Weapons.

2.6.3 FAILURE EFFECTS ANALYSIS.

Failure effects analysis was conducted on a circuit function level for the PCM and by mode of operation for the TME. With the exception of PCM multiplexer input gates and the TME real time signal path, the failure effects described in the following paragraphs can be corrected by switching to the redundant subsystem. PCM multiplexer input gates were designed to allow maximum losses of seven digital or eight analog channels as a result of a single failure, and these losses prevail regardless of the redundant state in operation. The remainder of the Nimbus study telemetry system was designed such that a single failure does not cause the loss of all data, e.g., a failure in the TME real-time signal path causes loss of real-time data but the recorded data function is retained without loss.

2.6.3.1 PCM ANALYSIS. For analysis purposes only, the Nimbus "B" PCM circuitry is grouped by function for multiplexer circuits and by module for the remaining circuits (figure 86).

2.6.3.1.1 MULTIPLEXER. The multiplexer contains integrated circuits and discrete components mounted on 13 printed circuit boards. All signal paths are redundant except the input gates that interface with inputs from the spacecraft.

a. Analog Multiplexer. A total of 21 prime plus 434 subcommutated analog time slots is provided. Prime channel input gates are arranged in a 4 (column) x 8 (row) matrix, and the subcommutated input gates are arranged in four sets of 8 (column) x 8 (row) matrices. Outputs from each matrix are tied together so that a group of eight or less channels passes through a sequencer gate. Prime analog data passes through one set of sequencer gates, and subcommutated analog data passes through two sets of sequencer gates before entering the coder.

The basic analog switching gate is the metal oxide silicon field effect transistor (MOSFET); five monolithic MOS transistors are arranged in one flatpack. Conduction is achieved when an individual gate is driven negative by gate driver circuitry. Failure modes and corresponding number of channels lost are contained in table 16 for the analog input matrix and sequencer gates.

Losses that occur as a result of input matrix failures cannot be recovered by switching to the redundant PCM block.

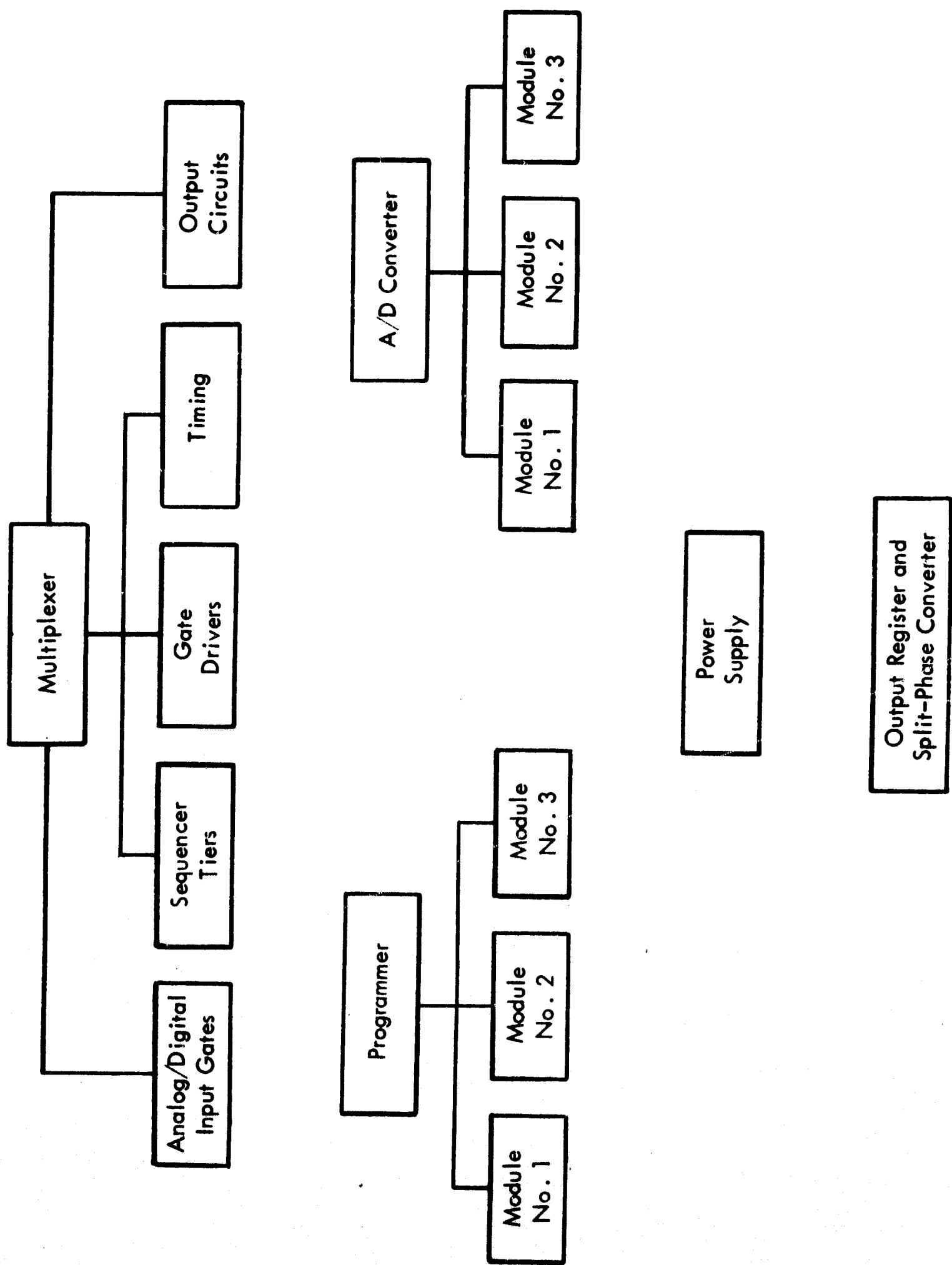


Figure 86. PCM Detailed Reliability Diagram

Table 16. Analog Input Matrix and Sequencer Gates, Failure Modes Versus Channels Lost

Failure Mode	Number of Prime (P) or Subcommutated (S) Channels Lost		
	Input Matrix	First Sequencer	Final Sequencer
Short-Source to Body	1P or 1S	Up to 8S	Up to 30S or 6P
Short-Gate to Body	1P or 1S	Up to 8S	Up to 30S or 6P
Open Source	1P or 1S	Up to 8S	Up to 30S or 6P
Open Drain	1P or 1S	Up to 8S	Up to 30S or 6P
Short-Source to Drain	Up to 6P or 8S	None	Up to 434S or 21P
Short-Body to Drain	Up to 6P or 8S	Up to 30S	Up to 434S or 21P
Short-Source to Gate	Up to 6P or 8S	Up to 8S	Up to 30S or 21P
Short-Gate to Drain	Up to 6P or 8S	Up to 30S	Up to 434S or 21P
Open Gate	1P or 1S	Up to 8S	Up to 30S or 6P
Loss of Gate Drive	1P or 1S	Up to 8S	Up to 30S or 6P
Continuous Gate Drive	Up to 6P or 8S	Up to 30S	Up to 434S or 21P

b. Digital Multiplexer. The digital multiplexer contains 63 prime and 280 sub-commutated channels. Two sets of prime digital channel input gates are arranged in 7 (row) x 4 (column) and 7 (row) x 5 (column) matrices. Subcommutated channel input gates are arranged in 7 (row) x 5 (column) matrices. Data from the digital input matrix passes through one group of sequencer gates.

Digital switching gates are identical to the MOSFET devices used in the analog multiplexer. Failure modes and corresponding number of channels lost are given in table 17 for the digital input matrix and sequencer gate.

Table 17. Digital Input Matrix and Sequencer Gates, Failure Modes Versus Channels Lost

Failure Mode	Number of Prime (P) or Subcommutated (S) Channels Lost	
	Input Matrix	Sequencer
Short-Source to Body	1P or 1S	5S or up to 5P
Short-Gate to Body	1P or 1S	5S or up to 5P
Open Source	1P or 1S	5S or up to 5P
Open Drain	1P or 1S	5S or up to 5P
Short-Source to Drain	5S or up to 5P	9P or 40S
Short-Body to Drain	5S or up to 5P	9P or 40S
Short-Source to Gate	5S or up to 5P	9P or 40S
Short-Gate to Drain	5S or up to 5P	9P or 40S
Open Gate	1P or 1S	5S or up to 5P
Loss of Gate Drive	7P or 7S	35S or up to 35P
Continuous Gate Drive	All	All

c. MOSFET Gate Drivers. Each analog gate has an individual gate driver. Gate drivers for the analog input gates generate drive to digital groups (seven input gates). Separate gate drivers are provided for each group of seven MOSFET gates in the digital sequencer and in the final digital output tier.

A failure in the gate drive circuitry causes loss, or continuous presence, of the drive signal to the MOSFET gate. The number of channels lost as a result of these failure modes is covered in the preceding analog and digital multiplexer sections. A failure in the analog input gate driver, however, causes loss of analog and digital channels. The number of channels lost is obtained by combining the losses given in tables 16 and 17.

d. Multiplexer Timing. Timing for the multiplexer is provided by a 10-stage integrated circuit counter. A failure in the timing circuitry causes the loss of all data.

e. Multiplexer Output Circuits. Coded analog data from the coder and digital data from the digital sequencer are gated with the ID and time code data in the final digital tier to a group of seven general purpose amplifiers (GPA). An additional GPA controls the sync bits. An 8-bit word is thus passed to the output shift register from the GPA outputs.

A failure in a GPA causes the data loss shown in table 18.

Table 18. General Purpose Amplifiers, Failures Versus Data Lost

GPA/Bit Number	Data Lost				
	Sync	ID	Time Code	Digital	Analog
1	X				
2	X		X	X	X
3	X		X	X	X
4	X		X	X	X
5	X	X	X	X	X
6	X	X		X	X
7	X	X		X	X
8	X	X		X	X

Failure modes and corresponding data bit losses are given in table 19 for the final digital tier.

Table 19. Multiplexer Final Digital Tier, Failure Modes Versus Data Lost

Failure Mode	Information Lost
Short-Source to Body	Time Code or ID or 1 analog bit or 9 prime plus 40 subcommutated digital bits
Short-Gate to Body	Time Code or ID or 1 analog bit or 9 prime plus 40 subcommutated digital bits
Open Source	Time Code or ID or 1 analog bit or 9 prime plus 40 subcommutated digital bits
Open Drain	Time Code or ID or 1 analog bit or 9 prime plus 40 subcommutated digital bits
Short-Body to Drain	9 prime plus 40 subcommutated digital bits and 1 analog bit and either ID or Time Code
Short-Source to Gate	9 prime plus 40 subcommutated digital bits and 1 analog bit and either ID or Time Code

Table 19 . Multiplexer Final Digital Tier, Failure Modes Versus Data Lost (Continued)

Failure Mode	Information Lost
Short-Gate to Drain	9 prime plus 40 subcommutated digital bits and 1 analog bit and either ID or Time Code
Open Gate or Loss of Gate Drive	Time Code or 1 analog bit or 9 prime plus 40 subcommutated digital bits or ID
Continuous Gate Drive	9 prime plus 40 subcommutated digital bits and 1 analog bit and either ID or Time Code
Short-Source to Drain	9 prime plus 40 subcommutated digital bits and 1 analog bit and either ID or Time Code

2.6.3.1.2 PROGRAMMER. The programmer is a block-redundant circuit and is contained in three modules .

a. Programmer Module No. 1. Programmer Module No. 1 consists of the 15-microsecond strobe for the output shift register, duty cycle pulses for the multiplexer, coder commands, and the 8:1 counter that provides bit rate .

(1) **15-Microsecond Strobe.** This strobe is used to activate the coder storage flip-flops and the shift register input gates to allow placement of digital data into the register. The programmer circuitry that generates the 15-microsecond strobe consists of a 4-input AND gate, two half-shot switching circuits and an inverter output stage .

A shorted diode in the AND gate causes an increase in the 15 micro-second strobe rate, resulting in the loss of all analog data as well as the loss of enabling commands for placement of all digital data into the output register. An open diode causes loss of timing commands to the output shift register .

A failure in the half-shot switching circuits or the output inverter causes loss, or continuous presence, of the 15-microsecond strobe to the shift register, resulting in the loss of all data .

(2) **Duty Cycle Pulses.** Two duty cycle pulses (200 microsecond and 260 microsecond) are provided to the multiplexer to preserve power consumption by limiting the active time of the driver stages. The programmer circuitry that generates these pulses consists of seven half-shot switching circuits, four 4-input AND gates, two 2-input OR gates, and two inverter stages .

A failure in any stage causes loss, or continuous presence, of the duty cycle command to the multiplexer. A loss of the duty cycle command causes complete loss of data. A continuous duty cycle command causes an increase in the active time of the multiplexer driver stages, resulting in increased power consumption which is detrimental to the power supply .

(3) **Coder Commands.** Two commands are provided to the coder for enabling the calibration or encode modes of operation. Two 2-input AND gates, two 3-input AND gates, and two buffer amplifiers generate the coder commands.

A failure in any stage causes the loss, or continuous presence, of a command to the coder. Loss of the calibration command causes degradation of coder accuracy, and a continuous calibration command causes the loss of all analog data. A continuous coder encode command causes the loss of all data, and loss of the coder encode command causes the loss of all analog data.

(4) **8:1 Counter.** A failure in any stage of the 8:1 counter causes the loss of all data.

b. **Programmer Module No. 2.** Programmer Module No. 2 consists of the 1/16-cps pulse generator, a 1-cps reset circuit, and time code circuitry.

(1) **1/16-CPS Generator.** This 250-microsecond pulse is provided at the connector to drive up to five external experiments. The programmer circuitry that generates this pulse consists of a 250-microsecond monostable and a buffer inverter stage. Any failure in the 1/16-cps generator causes loss of the 250-microsecond pulse; however, the PCM will function normally.

(2) **1-CPS Reset.** The 1-cps reset pulse is used to obtain the proper subframe length of 62.5 words per second. A 500-microsecond monostable reset pulse generator in the programmer is driven from two AND gates and an OR gate. One AND gate gates the 500-cps buffered bit rate against the 1-cps buffered clock signal. The second AND gate detects word 62.5 and provides internal reset if the Nimbus clock pulse is inhibited. These two AND gate signals activate an OR gate to drive the reset pulse generator, so that a failure in the 1-cps circuitry causes the loss of time code but the PCM data is retained.

A shorted diode in any gate or a failure in the 500-microsecond monostable causes a loss of reset to the counters, resulting in complete loss of PCM data.

(3) **Time Code Circuits.** Time code data from the Nimbus "C" clock is presented in serial form to the programmer for storage, conversion from serial to parallel data, and application to the digital multiplexer. Two monostables form a 38.5-millisecond pulse that is delayed by 16.5 milliseconds from the 10-cps clock pulse. This delayed 38.5-millisecond pulse is gated with 100-cps to provide shift pulses to the 4-stage storage shift register. A failure in any of these circuits causes complete loss of time code data but does not affect PCM data.

c. **Programmer Module No. 3.** Programmer Module No. 3 consists of subframe ID buffers, a multiplexer clamp circuit, and a 3-bit coder storage circuit.

(1) **Subframe ID Buffers.** These buffers provide the level shift required to place the binary code status of the 16:1 subframe counter into the output format. A failure in these circuits causes the loss of subframe identity in the output format.

(2) **Multiplexer Clamp Circuit.** These circuits clamp the standby block-redundant multiplexer circuits to within ± 0.5 volts from PSC to prevent improper commands to the multiplexer resulting from failures in the standby circuitry. The programmer circuitry consists of a duty cycle driver and clamping circuits. A failure in the duty cycle driver circuits inhibits power to the multiplexer resulting in loss of all data. A failure in the clamp circuitry causes one of two possible conditions: (a) supply lines to the standby multiplexer drivers are floating; or (b) supply lines to the standby multiplexer are grounded continuously. The first condition causes a loss of data from the active multiplexer if improper commands result from a failure in the standby multiplexer. The second condition inhibits operation of the standby multiplexer; however, the active multiplexer remains operative.

(3) **3-Bit Coder Storage Circuit.** The last seven stages of the 10-stage counter in the coder are hard-wired to the digital multiplexer and gated into the output register to provide the normal 7-bit words in the Nimbus format. The first three stages of the coder 10-stage counter are applied to the 3-bit storage circuit in the programmer to provide up to 10 bits of resolution (1 part in 1024) when these extra bits (bits 8, 9, and 10) are patched back into the system. A failure in the three bistables or in the timing circuitry causes a loss of the 10-bit capability but does not affect the normal 7-bit format.

2.6.3.1.3 CODER. The coder is a block-redundant circuit and is contained in three modules. Coder module 1 contains the analog circuitry, and modules 2 and 3 contain the digital circuitry.

The MOSFET input gate alternately switches the unity gain buffer amplifier between the input analog bus and the calibration reference voltage source. Three coder-calibrate correction cycles are completed during each coding period.

During the analog sampling period, the unity gain buffer amplifier output charges a capacitor to the same potential as the input voltage. At the completion of the input sampling period, the input buffer amplifier is disconnected from the capacitor, allowing the capacitor to be discharged through the constant current source. Coincident with the beginning of the capacitor discharge, a bit counter control gate is enabled, allowing the 500-kc clock pulse to trigger a 10-stage binary counter. When the ramp function reaches a 0-reference level, the bit counter control gate is inhibited, thus completing the conversion process. Since the ramp voltage is a linear function of time, a binary number that represents the analog voltage is now stored in the counter. The first three stages of the counter are applied to the 3-bit storage register in the programmer, and the remaining seven stages are connected directly to digital multiplexer gates.

During the calibration mode, the voltage reference source is switched to the input buffer amplifier and coded. The level detector and the full scale detector are enabled to permit ramp slope correction such that the 0-detect pulse is coincident with the overvoltage pulse. The necessary correction is accomplished by controlling the current used to discharge the ramp capacitor.

a. **Coder Module No. 1.** For analysis purposes, the circuitry for coder module 1 is grouped as follows: encode/calibrate switch and calibrate reference, unity gain buffer amplifier, ramp capacitor and constant current source, and level detector.

(1) Encode/Calibrate Switch and Calibrate Reference. The encode/calibrate switch is a silicon planar MOSFET and is controlled by an NPN driver on command from coder module 2. Thus any failure mode that ties the input analog bus to a voltage source causes a complete loss of analog data. These failure modes are: short-source to drain, short-base to drain, short-source to gate, short-gate to drain, short-collector to emitter (NPN driver), and a continuous command signal resulting from a failure in coder module 2. The remaining MOSFET failure modes, or any failure in the calibrate reference circuitry, causes decreased accuracy in the coding process.

(2) Unity Gain Buffer Amplifier. A failure in this circuit affects encoded analog data, ranging from partial degradation to complete loss of data.

(3) Ramp Capacitor and Constant Current Source. The effect of a failure in this circuit ranges from degradation to total loss of data.

(4) Level Detector. A failure in this circuit causes the loss of all analog data, because the 0-detect pulse that inhibits the 500-kc clock pulse at completion of the sample and encode cycles is lost.

b. Coder Module No. 2. The circuitry for coder module 2 was analyzed according to the following grouping: 500-kc oscillator, counter gate control, sync bistable, counter reset, and error correction circuits.

(1) 500-KC Oscillator. A failure that causes the loss or frequency degradation of the 500-kc signal inhibits the 10-stage counter and causes a complete loss of analog data.

(2) Counter Gate Control. Any failure in the counter gate control circuitry that causes a loss, or continuous presence, of 500-kc signal to the 10-stage counter also causes complete loss of analog data.

(3) Sync Bistable. The sync bistable controls the coder module 1 sampling switch that connects the unity gain buffer to the analog bus and ramp capacitor. Any failure that locks the bistable in the state with the buffer amplifier continuously connected to the ramp capacitor causes inaccurate coding due to nonlinear discharge of the ramp capacitor. Conversely, any failure that locks the bistable in the opposite state, i.e., with the unity gain buffer amplifier function inhibited, causes complete loss of analog data.

(4) Counter Reset. Loss of the reset signal causes the word rate to be asynchronous with the analog to digital conversion time period, resulting in degradation of all analog data. A continuous reset signal inhibits the 10-stage counter, causing the loss of all analog data.

(5) Error Correction Circuits. A failure in this circuit affects encoded analog data, ranging from partial degradation to complete loss of data.

c. Coder Module No. 3. For analysis purposes, coder module 3 circuitry is divided into two functions, a 10-stage counter and an overcode detector.

(1) 10-Stage Counter. A failure in any stage of the counter causes the loss of one or more encoded analog data bits, depending on the stage of the counter that fails, as shown in table 20.

Table 20. Ten-Stage Counter, Failures Versus Data Lost

Failure	Data Lost
Stage 1	All encoded analog data
Stage 2	All encoded analog data
Stage 3	Bits 4, 8, 16, 32, 64, 128, 256, and 512
Stage 4	Bits 8, 16, 32, 64, 128, 256, and 512
Stage 5	Bits 16, 32, 64, 128, 256, and 512
Stage 6	Bits 32, 64, 128, 256, and 512
Stage 7	Bits 64, 128, 256, and 512
Stage 8	Bits 128, 256, and 512
Stage 9	Bits 256 and 512
Stage 10	Bit 512

(2) Overcode Detector. A failure in this circuit causes the loss of all analog data as a result of losing the overvoltage pulse that signifies a count of 1023 in the ten counters.

2.6.3.1.4 OUTPUT SHIFT REGISTER AND SPLIT-PHASE CONVERTER. Circuitry for the output shift register and split-phase converter is contained in one module. Since block redundancy is employed, each PCM contains two of these modules.

a. Output Shift Register. A failure in any stage of the shift register causes loss of one or more data bits, depending on the stage of the register that fails, as shown in table 21.

Table 21. Output Shift Register, Failures Versus Data Lost

Failure	Data Lost
Stage 1	All data
Stage 2	All data
Stage 3	Bits 1, 2, 4, 8, 16, 32, and 64
Stage 4	Bits 1, 2, 4, 8, 16, and 32
Stage 5	Bits 1, 2, 4, 8, and 16
Stage 6	Bits 1, 2, 4, and 8
Stage 7	Bits 1, 2, and 4
Stage 8	Bits 1 and 2
Stage 9	Bit 1

b. 500-CPS Buffer. Loss of the 500-cps signal causes a complete loss of all data.

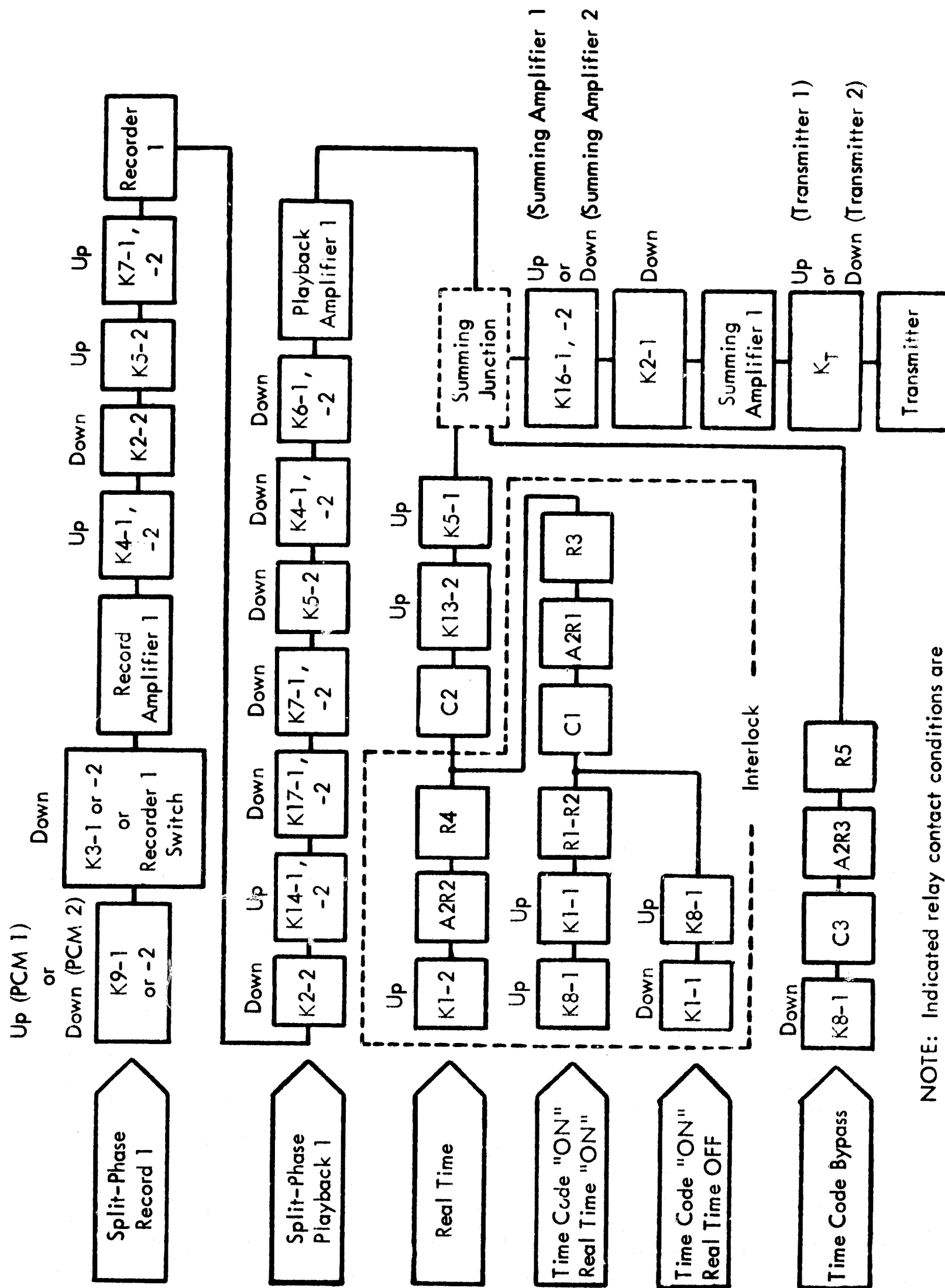
c. NRZ-To-Split-Phase Converter. Any failure that causes a loss of a split-phase signal inhibits the record or real-time function, or both, depending on where the failure occurs in the converter.

2.6.3.1.5 POWER SUPPLY. The power supply circuitry is contained in one module. Since block redundancy is employed, each PCM contains two of these modules. Any failure causing the loss of power disables the system. A failure involving loss of power regulation can cause degradation of data.

2.6.3.2 TME ANALYSIS. The Nimbus "B" TME is grouped by mode of operation, as shown in figure 87 for subsystem 1 of the block-redundant TME equipment. Figure 87 shows the electronic components and relays required, as well as the state of the relay contacts, for each mode of operation.

Table 22 lists the circuitry in figure 87 under subsystem 1 and the associated complementary circuitry for the redundant path under subsystem 2. The failure effects analysis references only the circuitry for subsystem 1, since subsystem 2 contains similar circuitry.

2.6.3.2.1 DIODES. Diodes in the TME are used as relay coil protective devices. The suppression diodes are placed across each coil to reduce noise generation and are series-redundant for short mode protection. Isolation diodes are placed in series with the coil command lines for isolation and are parallel-redundant for open mode protection. Thus, any single diode can fail in either the open or short mode without affecting relay operation.



NOTE: Indicated relay contact conditions are referenced to figure I-26.

Figure 87. TME Detailed Reliability Diagram

Table 22. TME Electronic Components and Relays

Component	Subsystem 1	Subsystem 2
Diodes	(See paragraph 2.6.3.2.1)	(See paragraph 2.6.3.2.1)
Relays	K1-1, -2 K2-1, -2 K3-1, -2 K4-1, -2 K5-1, -2 K6-1, -2 K7-1, -2 K8-1, -2 K9-1, -2 K16-1, -2 K17-1, -2	K1-1, -2 K10-1, -2 K11-1, -2 K12-1, -2 K13-1, -2 K14-1, -2 K15-1, -2 K8-1, -2 K9-1, -2 K16-1, -2 K18-1, -2
Resistors	R1 through R5 R6, R10 R7, R11 A2R1 through A2R3	R1 through R5 R8, R12 R9, R13 A2R1 through A2R3
Capacitors	C1 through C3	C1 through C3
Amplifiers	Record 1 Playback 1 Summing 1	Record 2 Playback 2 Summing 2
Recorders	Recorder 1	Recorder 2
Transmitters	Transmitter 1	Transmitter 2

2.6.3.2.2 RELAYS. Failure modes for relays are: (a) contact failure resulting in an open circuit; and (b) open coils, sticking contacts, or loss of command voltage preventing a change of state.

a. Relay K1. Failure effects are as follows:

(1) Real Time "ON" State. A contact failure causes the loss of real time data; whereas a coil failure causes a continuous real-time signal that inhibits the time code bypass mode of operation.

(2) Real-Time "OFF" State. A contact failure causes a continuous reduction to half amplitude of the time code normal data. An open coil in the real time "off" state causes complete loss of real-time data.

b. Relay K2. Failure effects are as follows:

(1) Channel No. 1 Power "ON" State. A contact failure inhibits subsystem 1 as a result of power loss. A coil failure has no effect on system operation; however, the ability to remove power from subsystem 1 is lost.

(2) Channel No. 1 Power "OFF" State. A contact failure does not affect operation of either subsystem; however, a coil failure renders subsystem 1 inoperative.

c. Relay K3 and Recorder 1 Timing Switch. Relay K3 is a standard, nonlatching type relay requiring only one command. The spring loaded contacts are automatically returned to the normally open position after removal of the command signal. The contacts for relay K3 are wired in a redundant configuration such that any contact failure has no effect on the system. A coil failure causes loss of manual control of the record function for subsystem 1.

A contact failure in the recorder timing switch precludes automatic switching to the record mode following the 3-minute playback mode; however, relay K3 provides manual control of the record mode.

d. Relay K4. A coil or contact failure renders subsystem 1 inoperative as a result of losing the record-playback function.

e. Relay K5. Failure effects are as follows:

(1) Recorder 1 "RECORD" State. A failure of contact K5-1 causes complete loss of real-time and time code data. A failure of contact K5-2 renders subsystem 1 inoperative as a result of losing the record function. A coil failure inhibits the playback function.

(2) Recorder No. 1 "PLAYBACK" State. A failure of contact K5-1 does not affect system operation; however, a failure of contact K5-2 inhibits the playback function. A coil failure inhibits the record function as well as real-time and time code data. Switching to subsystem 2 restores the record-playback function, but the real-time and time code data remains inoperative.

f. Relay K6. Failure effects are as follows:

(1) Recorder No. 1 "RECORD" State. A contact failure inhibits the playback function of subsystem 2. An open coil does not affect subsystem 1 operation.

(2) Recorder No. 1 "PLAYBACK" State. A contact failure does not affect system operation. A coil failure inhibits the playback function of subsystem 2.

g. Relay K7. Failure effects are as follows:

(1) Recorder No. 1 "RECORD" State. Failure of the contacts has no effect on system operation. An open coil inhibits subsystem 1 playback as a result of power loss to the recorder.

(2) Recorder No. 1 "PLAYBACK" State. A contact failure inhibits subsystem 1 playback as a result of power loss to the recorder. A coil failure holds the recorder for subsystem 1 in a continuous playback mode.

h. Relay K8. Failure effects are as follows:

(1) Time Code "NORMAL" State. A contact failure does not affect system operation. A coil failure causes loss of the time code bypass function.

(2) Time Code "BYPASS" State. A contact failure inhibits the time code bypass function. A coil failure inhibits the time code normal function.

i. Relay K9. A contact or coil failure inhibits PCM 1 or PCM 2, depending on the state of the relay, as a result of power loss to the PCM.

j. Relay K16. A contact or coil failure inhibits summing amplifier 1 or summing amplifier 2, depending on the state of the relay, as a result of signal loss.

k. Relay K17. Relay K17 is a standard, nonlatching type relay that requires only one command. The spring-loaded contacts are automatically returned to the open position after removal of the command signal. The contacts for K17 are wired in a redundant configuration such that any contact failure has no effect on the system. A coil failure holds the recorder for subsystem 1 in a continuous record mode.

2.6.3.2.3 RESISTORS. Composition resistors are considered to fail only in the open mode. Fixed-film and variable wirewound resistors are more likely to fail in the open mode; however, this analysis considers the possibility of a short mode failure for these two types.

a. Resistor R1. An open mode failure causes loss of the time code normal function. A short mode failure causes degradation of real-time data as a result of the continuous, full amplitude, time code normal data.

b. Resistor R2. An open mode failure causes degradation of the real-time data as a result of the continuous, full amplitude, time code normal data. A short mode failure causes loss of time code data and a decrease in real-time data amplitude.

c. Resistors R3 and A2R1. An open mode failure causes loss of time code data. A shorted resistor causes degradation of the real time data as a result of an increase in time code normal data amplitude.

d. Resistors R4 and A2R2. An open mode failure causes loss of real-time data. A short mode failure causes degradation of the time code normal data as a result of an increase in real-time data amplitude.

e. Resistors R5 and A2R3. An open mode failure causes loss of the time code bypass function. A short mode failure causes degradation of the PCM data (real-time and playback) as a result of an increase in time code bypass data amplitude.

f. Resistors R6 and R10; R7 and R11. These fixed-composition resistors are connected in a parallel redundant configuration such that any one resistors failure, in the open mode, does not affect system operation.

2.6.3.2.4 CAPACITORS. The tantalum capacitors, used for coupling time code and real-time data to the summing amplifiers, are more likely to fail in the short mode; however, short and open failure modes are considered in this analysis.

a. Capacitor C1. A shorted capacitor causes degradation of time code data as a result of the change in DC bias of the time code modulation output circuit. An open capacitor causes complete loss of the time code normal data.

b. Capacitor C2. A short mode failure causes an increased DC input voltage to the summing amplifier which clips the real time and time code normal data. An open capacitor causes complete loss of real-time and time code normal data.

c. Capacitor C3. A shorted capacitor causes an increased DC input voltage to the summing amplifier which clips the time code bypass data. An open capacitor inhibits the time code bypass function.

2.6.3.2.5 AMPLIFIERS, RECORDERS AND TRANSMITTERS. The recorder, transmitter, record amplifier, playback amplifier, and summing amplifier are all redundant. A failure of any of these units in one subsystem can be corrected by switching to the standby subsystem.

2.6.4 PARTS SELECTION AND VENDOR EVALUATION.

All part requirements and potential vendors were carefully screened to obtain the most reliable and best qualified devices. Parts that required additional effort are discussed in the following paragraphs.

2.6.4.1 RELAYS. Relays, being large components, occupy a large portion of the package volume. For packaging considerations, it was necessary to find the smallest relay that exhibited favorable reliability characteristics. Three relays were evaluated; these were Babcock (BR-17), Filtor's (Demi-J), and Potter and Brumfield (FL 11D). The Babcock and Filtor's relays were approximately one-tenth the volume of the Potter and Brumfield relay. A relay of each type was disassembled and examined for sturdiness of construction. It was noted that each type was constructed by a different method, but that each would probably pass the relay screening tests. The Babcock and Filtor's relays were preferred from a packaging standpoint; however, the Potter and Brumfield relay was chosen because of the favorable history compiled from previous Nimbus systems.

2.6.4.2 MOSFET, 5 CHANNEL MULTIPLEXER. MOSFET's presented two major problem areas. These areas can be considered as handling procedures and supply source.

MOSFET's are extremely susceptible to damage caused by static charge. Static charge generated by friction in handling is sufficient to destroy a unit. To prevent this type

of damage, a handling procedure was generated (Radiation Drawing Number 110174 (Appendix VII), Handling and Shipping Flatpack and MOSFET devices) that outlined all special requirements for the vendor and for Radiation personnel.

The major supplier, Fairchild Semiconductor, was unable to adequately protect the units as outlined in the handling procedure, and therefore had a high destruction rate. The excessive fall-out seriously threatened the production schedule, thus necessitating a search for a source better able to comply with the handling procedures.

General Instrument Corporation (G.I.) of Hicksville, Long Island, indicated promise as a potential supplier because of development work on a 5-channel MOSFET. Negotiations were inaugurated to develop a circuit that would be interchangeable with the Fairchild circuit. General Instrument's plant, production procedures, and quality control procedures were surveyed and found to be inadequate for production of aerospace components. Radiation and G.I. personnel met on several occasions to revamp production and quality control procedures so that fabrication of the circuits could begin.

After all procedural problems were resolved, Radiation released a purchase order for an evaluation lot of a hundred pieces. Radiation surveyed G.I.'s process steps at chosen phases to assure all procedures were followed precisely. At present, G.I. has adequately followed all procedures as documented; however, they have encountered many difficulties in meeting the required electrical parameters. Radiation is continuing liaison with G.I. to resolve the existing problem areas.

2.6.4.3 NAND GATE AND DIODE EXTENDER SOURCE. Fairchild Semiconductor, Philco, and Westinghouse were investigated as potential suppliers of DTL NAND gate requirements. Westinghouse was considered to be superior in plant facilities and production procedures and, after an engineering evaluation of Westinghouse circuits, was chosen as the supplier.

2.6.4.4 POLYCARBONATE CAPACITORS. Metallized polycarbonate film capacitors are available in round and rectangular hermetically-sealed cases. The rectangular case offers system packaging advantages. Round and rectangular capacitors are manufactured by the same processes, except that a rectangular capacitor is made by pressing a round capacitor flat to fit in a rectangular case. Engineering observation noted that points of high stress that can have degrading effects are generated in the crease areas of the flattened capacitors. A test was performed on samples of round and rectangular capacitors to determine any difference in performance. The tested capacitors were rated by the vendor (Marshall Industries) at 200 volts. During the tests, no dielectric breakdown was observed below a 1200-volt potential. From this and other testing it was concluded that essentially no difference in reliability could be detected between the two types.

2.6.4.5 HYBRID INTEGRATED CIRCUITS, NPN DRIVERS AND PNP DRIVERS. Sprague encountered three major problems with the hybrid integrated circuits (Radiation part numbers 110260 and 110261). The first was lead-tinning difficulties, the second was a production process, and the third was a testing problem.

The first units received with tin-dipped leads proved to have an unsatisfactory tin coat. Sprague was instructed by Radiation on the lead tinning process, and was

given the Radiation lead-tinning procedure (Drawing Number 112286). Tinning results proved satisfactory when the Radiation procedure was followed.

The second problem involved internal shorting of components. Before bonding, Sprague scraped each gold bonding pad with tweezers to provide a clean bonding surface. Gold slivers, scraped up in this manner, were sealed in the package. Combined with irregular component placement, it was possible for these gold slivers to cause intermittent shorts. Sprague has discontinued the scraping process.

Several defective units were received at Radiation. Since these units were 100 percent screened by Sprague before shipment, a question arose concerning the effectiveness of Sprague's testing. Examination of the test setup revealed that a device could be reversed in the test fixture, causing the device to be destroyed (in the same mode experienced at Radiation) and, simultaneously, indicating the device was acceptable. Radiation revised the test plan and end point limits, thereby preventing any recurrences.

2.6.4.6 SWITCHING DIODE. A switching diode in an extremely small package was required for mounting on the relay assembly board. Two types were studied; the TI-252 with round leads made by Texas Instruments, and a diode similar to 1N901 with ribbon leads made by TRW. Both types exhibited favorable electrical characteristics and poor soldering characteristics. The TI-252 was extremely hard to work with and generally had poor solder joints; the 1N901 was fairly easy to solder except the gold content of the tin coating was too high, thus forming a brittle gold-tin eutetic (Radiation Problem Bulletin #003). Ribbon lead diodes, tinned by Radiation, exhibited acceptable tin coating and formed good solder joints. The final choice was the TRW diode, tinned by Radiation.

2.6.4.7 LOW POWER FLIP-FLOP (FAIRCHILD μ C1133). A specification was generated by Radiation for the Fairchild μ C1133, a fairly straightforward low power DTL flip-flop device. Fairchild initially accepted the specification, but took several exceptions. Fairchild stopped production of these devices for each exception to await Radiation's action. In each case, negotiation with Fairchild resulted in their withdrawal of the exception and return to production.

2.6.4.8 TEMPERATURE COMPENSATED ZENER DIODE. Radiation's experience with temperature compensated (TC) zener diodes has been limited to the Fairchild FCT series which is a standard transistor with the base lead cut off. Past experience shows that the internal base bond can fly loose during vibration stress and short out portions of the diode, or even the whole diode. A short from the base to the header yields an uncompensated zener, and a short across the emitter to the collector totally shorts-out the diode. Fairchild indicated the "transistor zener" was to be phased out of the TC zener line, but did not indicate any effective date.

Continental Device Corporation (CDC) has developed a temperature compensated zener diode series (the CDT series) that is actually constructed as a zener diode rather than a transistor. CDC's facilities and diodes were surveyed and found to be acceptable; and CDC's zener is an acceptable and preferred substitute for the Fairchild zener.

2.6.5 FAILURE HISTORY.

All failures that occurred during module and card level fabrication and tests can be attributed to manufacturing or test errors. These types of failures are expected on breadboard systems where quality control standards are not as stringent compared with production units.

Although qualification tests have not started, all system level failures to date involve MOSFET devices. Analysis of MOSFET failures is incomplete and conclusions cannot be made concerning the failure mode.

2.6.6 SUMMARY OF RESULTS AND RECOMMENDATIONS.

The probability of success of the Nimbus B study system as a function of mission time is shown in figure 83 for the record/playback and time code plus real time modes of operation. These two operating modes represent the upper and lower limits of the four reliability assessments calculated in this report. It appears that complexity of the record/playback circuitry in the TME renders this mode of operation less reliable than the real-time and time code modes. However, complete redundancy is employed for the record/playback functions, whereas the remaining operating modes contain nonredundant signal paths. The probability of success of the time code plus real time mode of operation, for example, increases to .9001 for a six months mission time by providing redundant signal paths in the TME.

There is only one fused power line to both summing amplifiers. Since a failure in this power line would cause the loss of all data, system reliability would be enhanced by providing separate power lines to each summing amplifier.

The 500-cps signal from the clock passes through the TME to the PCM via single connector pins. Discontinuity of this signal path would cause the loss of all data. However, the reliability of connectors is high enough that redundant pin connections for the 500-cps signal is probably not necessary.

SECTION III

NEW TECHNOLOGY

3.0 INTRODUCTION.

This section contains a description of electrical and mechanical new technology encountered in the Nimbus Design Study Extension Program.

3.1 AIRBORNE EQUIPMENT.

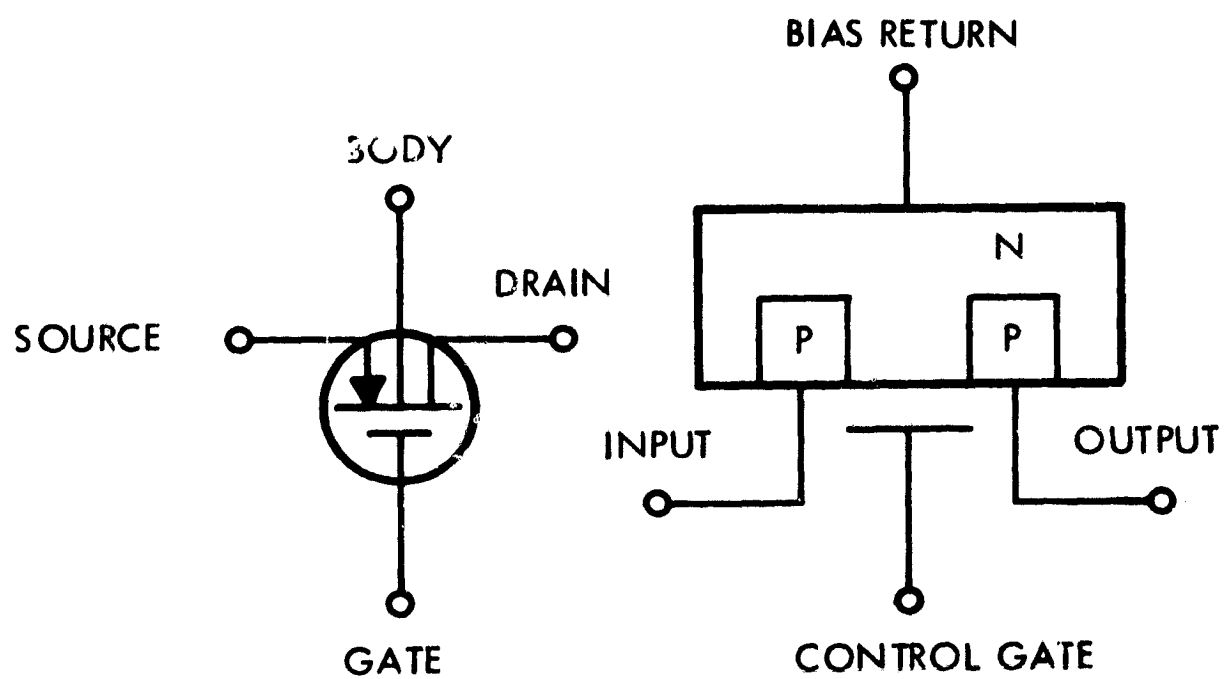
3.1.1 ELECTRICAL.

3.1.1.1 GENERAL. The Nimbus Design Study Extension Program was involved with only one circuit element in the category of new technology. This circuit element is the MOSFET flat pack that contains five individual channel gates.

The previous design study discussed the following types of gates: (a) optoelectronic gate, (b) dual emitter chopper gate, (c) P-channel unipolar field effect transistor, and (d) metal oxide semiconductor field effect transistor. The metal oxide semiconductor field effect transistor (MOSFET) was highly recommended and was used in the new program. A detailed description of the MOSFET device is contained in the following paragraphs.

3.1.1.2 MOSFET CHARACTERISTICS. A schematic diagram of the MOSFET is shown in figure 88. To obtain source-to-drain conduction, a negative voltage is applied to the metallic gate which directs the resulting field through the oxide insulation to the "N" substrate, thereby attracting holes to the semiconductor surface under the gate. The net result is a conduction path formed between the source and drain "P" diffused areas. When the negative gate voltage is removed, the "P" channel disappears and the source and drain junctions are back-biased by the more positive body voltage. Absolute isolation is assured for the gate terminal and the always back-biased source and drain junction leakages can be maintained in the nanoampere range. The resulting drive circuits are simple, since the isolated gate need only be voltage-switched for the on and off conditions. Therefore, drive currents are minimal and power consumption is low. The offset of the MOSFET is zero. Present junction breakdown voltages of 30 volts (General Instruments) to 40 volts (Fairchild) are realized. Future increases are anticipated that will make possible a wide range of input voltages. Capacitance to ground is comparable to the integrated chopper, and crosstalk is minimized because the source-to-drain capacity is less than 1 picofarad. Gate on resistance is less than 2.2K in the present design, and could be decreased to less than 1K at the expense of more capacitance to ground.

3.1.1.3 SELECTION OF MOSFET FOR ANALOG GATE. The general gating requirements for future systems, as well as all present Nimbus analog signal input specifications, can be met with the MOSFET. The simplicity of drive circuits and the open circuit feature of all gates when system power is turned off provide significant advantages over the conventional FET. The basic advantage of the MOSFET over the transformer-driven matched chopper transistor gate is the



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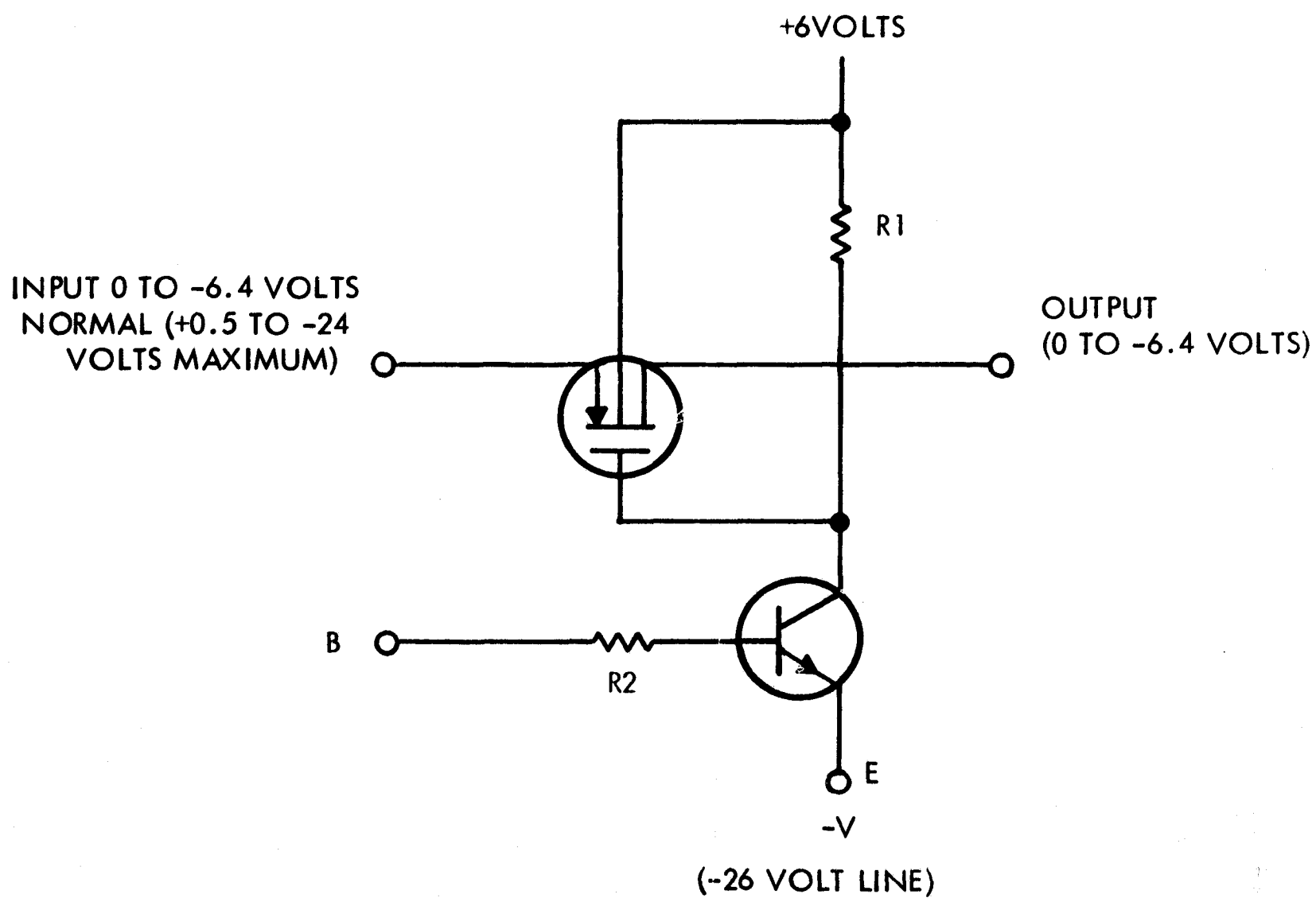
Figure 88. P-Channel Metal Oxide Silicon Field Effect Transistor

elimination of the bulky, relatively unreliable transformer. Not only are most parameters of the MOSFET superior to those of the optoelectronic chopper, but future development will probably favor the MOSFET. Another advantage of the MOSFET over the optoelectronic chopper is simplicity of drive circuits and physical construction. Since the MOSFET can be built by similar planar techniques used for normal transistor integrated circuits, a complete microelectronic analog commutator is possible.

3.1.1.4 ANALOG GATE DRIVE REQUIREMENTS. A basic MOSFET drive circuit is shown in figure 89. Since the input signal voltage is always more negative than +0.5 volts, the source-to-body junction will remain back-biased if the body is returned to +6 volts. The drain-to-body junction is similarly reverse-biased. The P-channel MOSFET will remain off as long as the insulated control gate potential is equal to or greater than the source or drain voltage. With the MOSFET off, the only conduction will be the body junction leakage currents to +6 volts. The control gate is, therefore, returned to +6 volts through a resistor to ensure that it is normally off. If the NPN transistor is saturated, the analog gate will conduct. The -26-volt power input line provides a convenient voltage to bias the control gate for conduction. The minimum gate-to-source voltage during normal signal conduction will then be approximately 19 volts (26 volts - 6.4 volts) which is more than sufficient to form a conducting channel from source to drain. During overvoltage, the minimum gate-to-source voltage is reduced to 11 volts (26 volts - 15 volts). When the NPN transistor stops conducting, the control gate recharges to +6 volts and the analog input gate is effectively open. An inherent immunity to cracking (temporary closing) of the analog gate due to system noise is provided since the control gate requires at least a 2-volt threshold to the source before any source-to-drain conduction takes place.

Protection against negative overvoltage input signals is provided by the MOSFET gates since the basic body junctions are capable of withstanding 30 volts without breakdown, damage, or excessive leakage. Thus, protection is provided for any analog input voltage from +0.5 volts to -24 volts. With a small modification in the buffer amplifier, the system would then be able to withstand these overvoltages without damage. The MOSFET can be operated with the source and drain interchanged. The drain is connected to the analog gate output (rather than the input) to reduce feedback current and line capacity, since the drain body junction is physically smaller than the source body junction. C_{leak} / leakage and capacitance is most important at the drain or analog gate output because the grouping of the analog switches is such that any analog signal path is connected to many more analog gate outputs than inputs. The turn-on and turn-off transient current in the input and output lines caused by the source and drain capacity to the control gate must also be considered. For a 25-volt switching gate transient and 10 picofarads capacity, 250 picocoulombs must be supplied from the analog signal source for each series conducting MOSFET in the signal path. A simple solution to this problem is to allow sufficient settling time before starting the coding process. Presently, settling time is provided by a 170-microsecond delay in the coder. Thus, for an 11 time constant settling time, a maximum 10-microsecond RC time constant could be allowed. For a maximum 3.3K source impedance, approximately 3,000K picofarads capacity would be allowable at the analog input. Another solution would be to provide a sufficiently large parallel capacitor at the analog source such that the transferred charge and leakage currents would have negligible effect upon the input voltage during the sample period.

Detailed information on MOSFET specifications are included in Radiation Part Specifications 106510 and 110245.



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Figure 89. Basic MOSFET Drive Circuit

3.1.1.5 PREVENTION OF CATASTROPHIC SYSTEM FAILURE. Since the system contains a large number of analog gates, a considerable increase in overall reliability was obtained by limiting failures to a small number of gates. The MOSFET failures are limited by grouping analog inputs into tiers of eight or less inputs per sequencer (figure 90). The effect of failure of any input MOSFET gate disables only the individual gate or disables all eight of the tiered group. Failure of a single input will occur with points S-B or G-B shorted or S or D open. A tier of gates will fail if points S-D, B-D, S-G, and G-D are shorted or G is open. All gates outside of a tier are protected, since any gate can withstand up to -24 volts and the circuit is clamped to provide protection to -35 volts. The output of one tier of input gates is connected to the input of a second tier, referred to as the sequencer gates. The effect of failures in a tier of sequencer gates is similar to that of failures in the tier of input gates, except that a sequencer failure causes loss of all channels in an input tier or all channels in the sequencer tier. Loss of all channels in the sequencer tier may be an undesirably large number of channels; however, the probability of this type of failure is reduced by driving an input gate only when its sequencer is driven. Thus, a shorted gate in the sequencer will not interfere with the other gates in the sequencer tier. When this drive limitation is used, the only failures in the sequencer gates that can affect more than a single input tier are shorts on points B-D and G-D. The B-D short could be avoided by leaving the body terminal in the sequencer MOSFET gates open, but the +0.5-volt fault voltage upper limit requires that the body be returned to a voltage more positive than +0.5 volts (+6 volts was used). The body connection serves as a bias return and, if left open, would allow gate junction leakage current to flow from input to output separately and would also increase the gate and drain capacity to the source. (Refer to paragraph 3.2.)

The MOSFET gate has been used in the Nimbus Study Extension PCM unit for both the analog channel gates and the digital channel gates. Thus, the same fault voltage limits and feedback currents apply to both analog and digital channels. The major difference between analog and digital gates is in input impedance. The input impedance is greater than 10 megohms for analog channels and is greater than 500 kilohms for digital channels.

3.1.2 MECHANICAL.

3.1.2.1 GENERAL. Foam shims have been used to absorb the load resulting from application of a compressive preload that is applied to the system electronics to protect the components from imposed dynamic environments. The compressive preload results in a plastic deformation of the foam, which maintains the load throughout the system.

To avoid placing excessive forces on planar-mounted components and their solder joints, the foam shims are designed such that there is clearance between the deflected shim and all portions of the components and their leads. The machining of grooves in a shim could result in only a few contact points between the shim and its associated printed circuit card. Machining would also result in loss of strength due to the removal of the "skin" from the foam which could cause collapse of the shim when the required preload is applied to the system. A technique has been developed for forming the shims such that maximum contact areas between the shim and the card is assured, and the foam "skin" strength is maintained. This technique is described in the following paragraph.

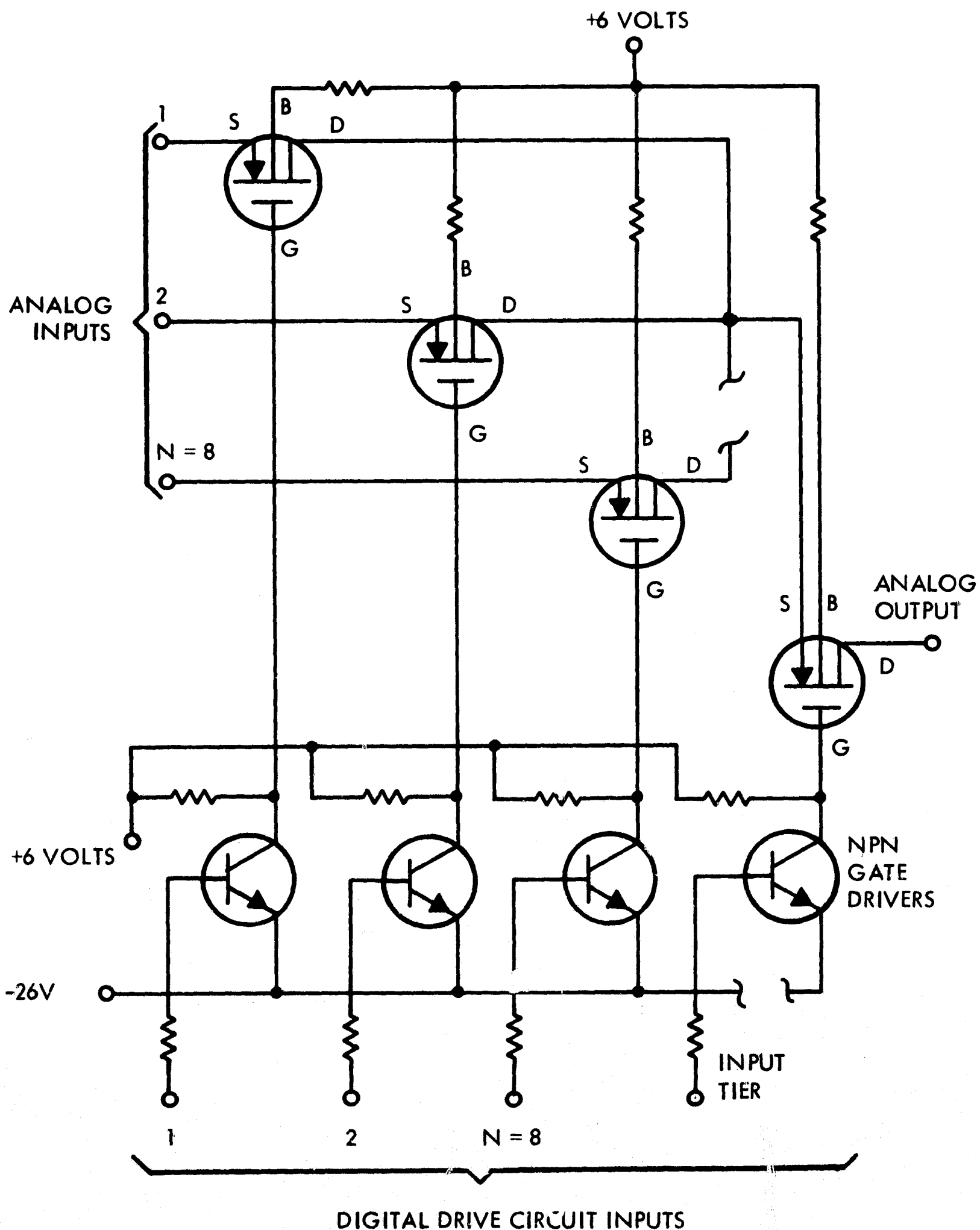


Figure 90. Typical N-Tiered Analog Gate Circuit

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3.1.2.2 SHIM FABRICATION. The first step in the shim fabrication process is the making of tool cards for each type of card assembly in the system. These tool cards use dummy components that are slightly larger than the system components so that there will be no load on the actual system components or their leads. The dummy components are bonded in place in locations corresponding to the actual system components. A 0.002-inch sheet of latex rubber is then placed over the tool card and the assembly is installed in a mold of accurate dimensions. A polyurethane foam is poured into the mold and allowed to cure. During the curing cycle, the foam expands and conforms to the inside dimensions of the mold. The foam stretches the rubber and assumes the contour of the tool card and its components. After curing, the tool card and shim are removed from the mold and separated from each other. Since the rubber is not affected by either the foam or the curing bake, the tool card and the shim are readily separated. The foam shim is thus molded to the exact form factor and component layout of the particular tool card utilized and is keyed as to card placement in the live system.

3.2 SUMMARY.

The only problems encountered with the MOSFET gate were feedback noise to the transducer caused by the MOSFET channel gate drivers, and feedback noise to the coder and time code shift register caused by the power switching of the GPA's. If the MOSFET body were directly returned to ground, the feedback capacity would be minimum (approximately 2 picofarads), and the feedback noise caused by the switching time transitions would be minimized. However, this solution for the problem of feedback noise to the transducer cannot be effected because of the input +0.5-volt fault requirement and because of the fail safe design criteria. A 100-K ohm resistor to +6 volts was installed in the body leads of all MOSFET gate flat packs, but this allowed the MOSFET to operate as a capacity amplifier when the gate lead was suddenly switched to the negative supply that enabled the gate. This capacity allowed a negative voltage noise spike of 4 to 8 volts to appear at the input transducer. To solve this problem, a capacitor should be placed across the resistor in the body lead; however, because of physical problems this correction was not accomplished in the Nimbus Study PCM. Instead, the resistors to +6 volts were replaced with 6-volt Zener diodes connected to PSC. With the diodes installed, the noise at the input is reduced to less than 0.5 volts. The Nimbus B system will use RC networks to reduce this noise to the very low millivolt region. There will then be minimum noise across the minimum source impedance such that a 10-K ohm source impedance would have nearly three times the peak noise of a 3.3-K ohm source impedance.

The second feedback noise problem was caused by the large turn-on transient feedback to the inputs of the final sequencers when the 260-microsecond power pulse was applied to the GPA's. The turn-on -26 volt transient was capacitively-coupled through the off MOSFET gate and collector-reset coder counters and time code shift register circuits. The off MOSFET gate had sufficient capacity (with the body lead returned through 100-K ohms to +6 volts) to appear as a 4:1 attenuator. Thus, the collector-reset pulse appeared as a noise spike of approximately -6 volts and would randomly (depending upon the circuit parameters of the coder counter and the time code shift register circuits) reset the input bistable multivibrator circuits. This problem was solved by the same corrective action as described above, i.e., a diode in the study PCM and an RC network in the Nimbus B PCM.

These two problems, the corrective actions, and tradeoffs are described in further detail in the next paragraph.

3.3 CONCLUSIONS AND RECOMMENDATIONS.

The two interface problems encountered in the Nimbus B study multiplexer were both solved through a single corrective action. The first problem was that a pulse that was generated when the duty-cycled GPA's turned on was being routed back through an off MOSFET gate (in the final sequencers) and collector-triggering the coder and time code shift register flip-flops. Because the GPA's turn on 30 microseconds before the MOSFET gates, the pulse was capacitively-coupled through the gate, thereby creating a condition wherein the source terminal was forward-biased by the negative-going, -24 volt, GPA turn-on pulse. This pulse was capacitively-coupled from drain to body to forward-bias the body to source junction. In this condition, the MOSFET gate was caused to function as a transistor which became a capacitor multiplier (figure 91). This effect is worse with the final sequencers in which only two of the five MOS gates are used. The unused MOSFET gate terminals in a flatpack (gate and source terminals) are tied to the common body terminal. This connection adds parallel capacitance from the drain to body terminals as shown in figure 91, resulting in a negative-going 6- to 8-volt, 5-microsecond (approximately) pulse on the source terminal of the MOSFET gate.

The second problem is similar to the first except that the pulse on the source terminal occurs when the MOSFET gate turns on (figure 92). This condition was caused by a negative pulse being capacitively-coupled from gate to body when the gate was strobed on (from +5 volts to -26 volts). The pulse caused the source-to-body junction to be forward-biased and the MOSFET gate again functioned as a capacitor multiplier. A negative pulse, from 1 to 2 volts in amplitude and about 1/2 microsecond in duration, appeared at the source terminal. In this case, the pulse at the source terminal is smaller in amplitude because the gate-to-body capacitance is small (2 to 3 picofarads).

Another problem that could be caused by this action is illustrated in figure 93. Figure 93-A shows a typical MOSFET flatpack (it makes no difference whether the channel is analog or digital). As can be seen, all bodies and all drains are common. The several approaches taken to solve the problem are shown at the top of the illustration. In the original configuration (100-K ohm resistor in the body lead to +6 volts) and with a -7 volt signal on the input to the top MOS gate and a 0-volt on the input to the bottom MOS gate (input A), operation of the circuit is such that when the top MOSFET gate is strobed on, the negative signal on the drain terminal of all MOSFET gates in the flatpack is coupled to the source terminal of the bottom MOSFET gate by the method described previously. The magnitude of this feedback pulse depends upon the difference between the two input terminals. This pulse to the input transducer appears as feedback current which, although it may not affect the user, is an undesirable characteristic.

Several approaches to this problem were examined. A Zener diode in the body lead of the MOSFET gates protects against positive overvoltages; however, when operating near ground potential the problem of the pulse feeding back through the MOSFET gate is still present. With PSC tied directly to the body lead of MOSFET gate, there would be no problem if the input voltage never went above ground (specification requires -24 volts to +0.5 volt). A positive voltage would, however, forward bias the source-to-body junction, making the MOSFET gate function as a transistor (B, figure 93) and placing a positive voltage on the drain terminal of

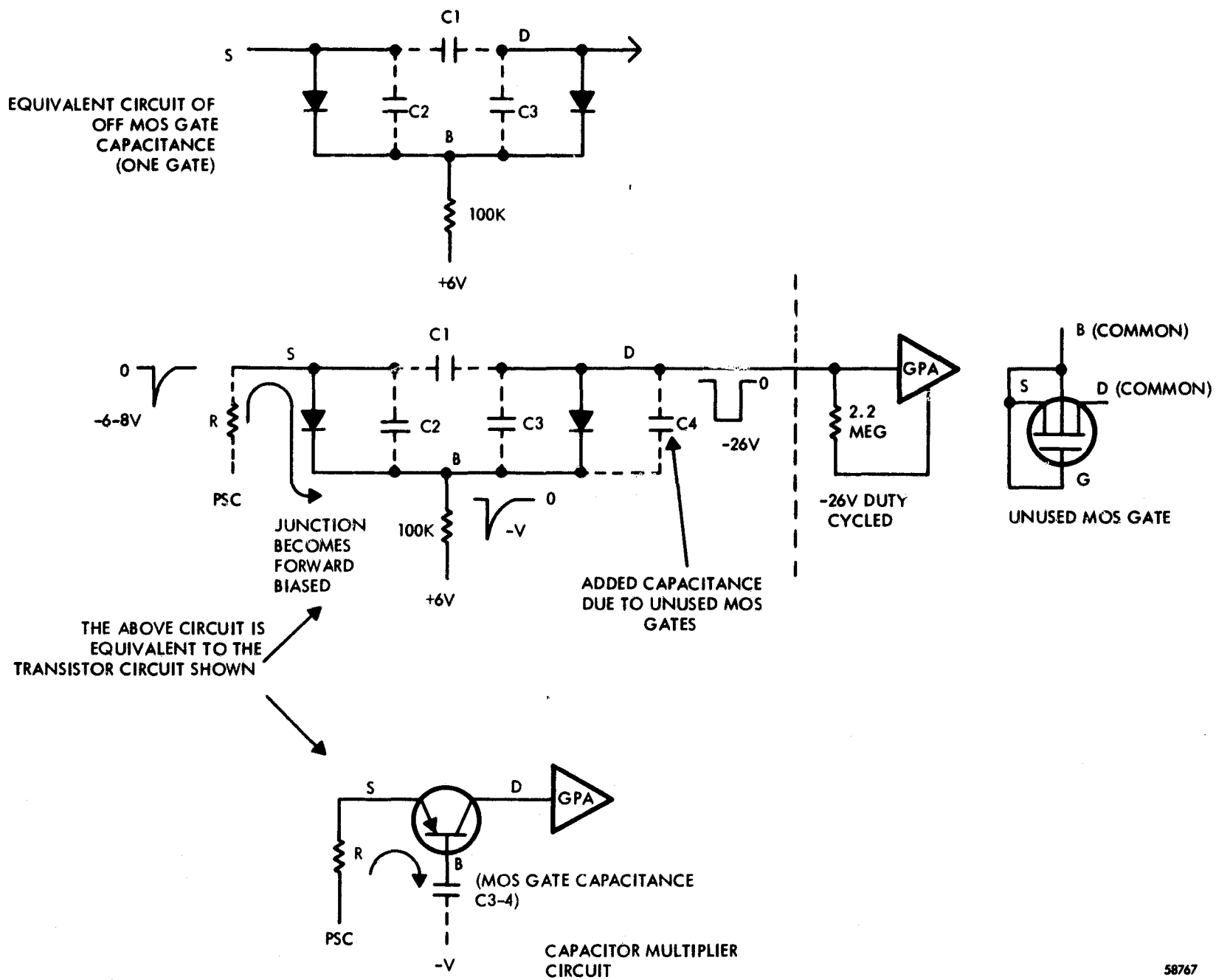
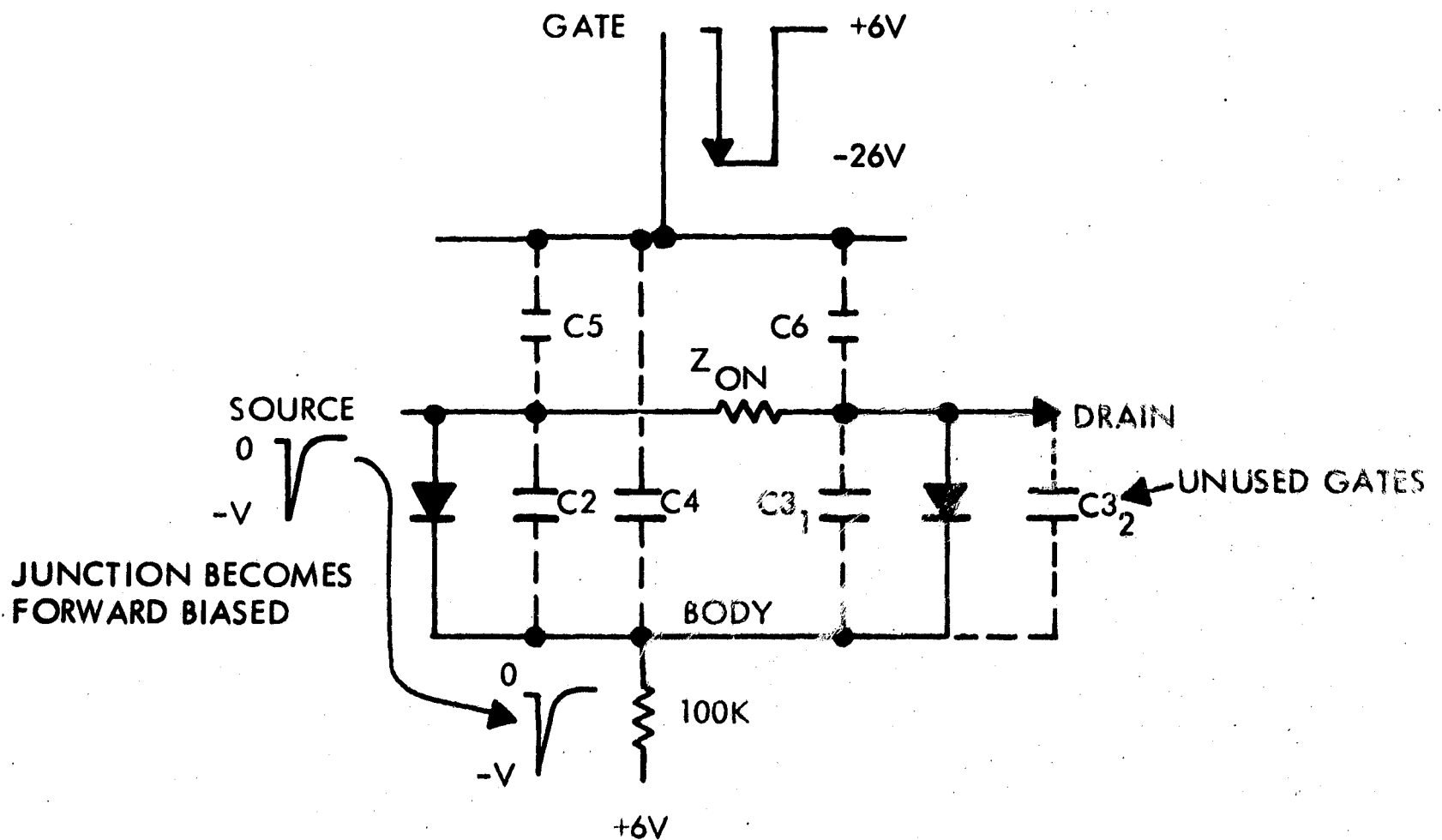
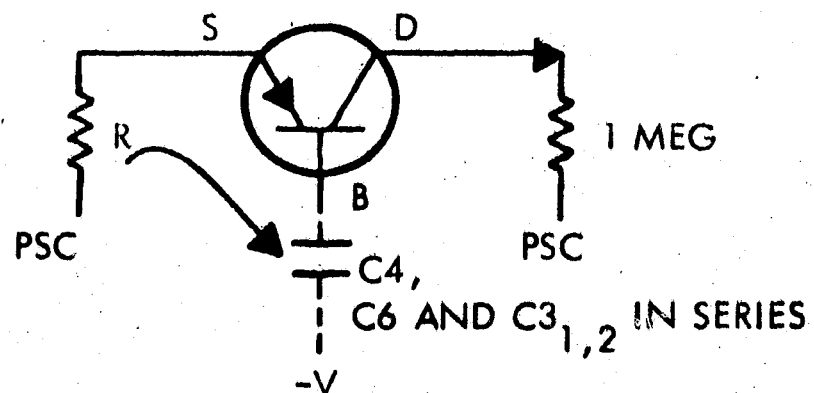


Figure 91. MOSFET Gate Equivalent Circuit



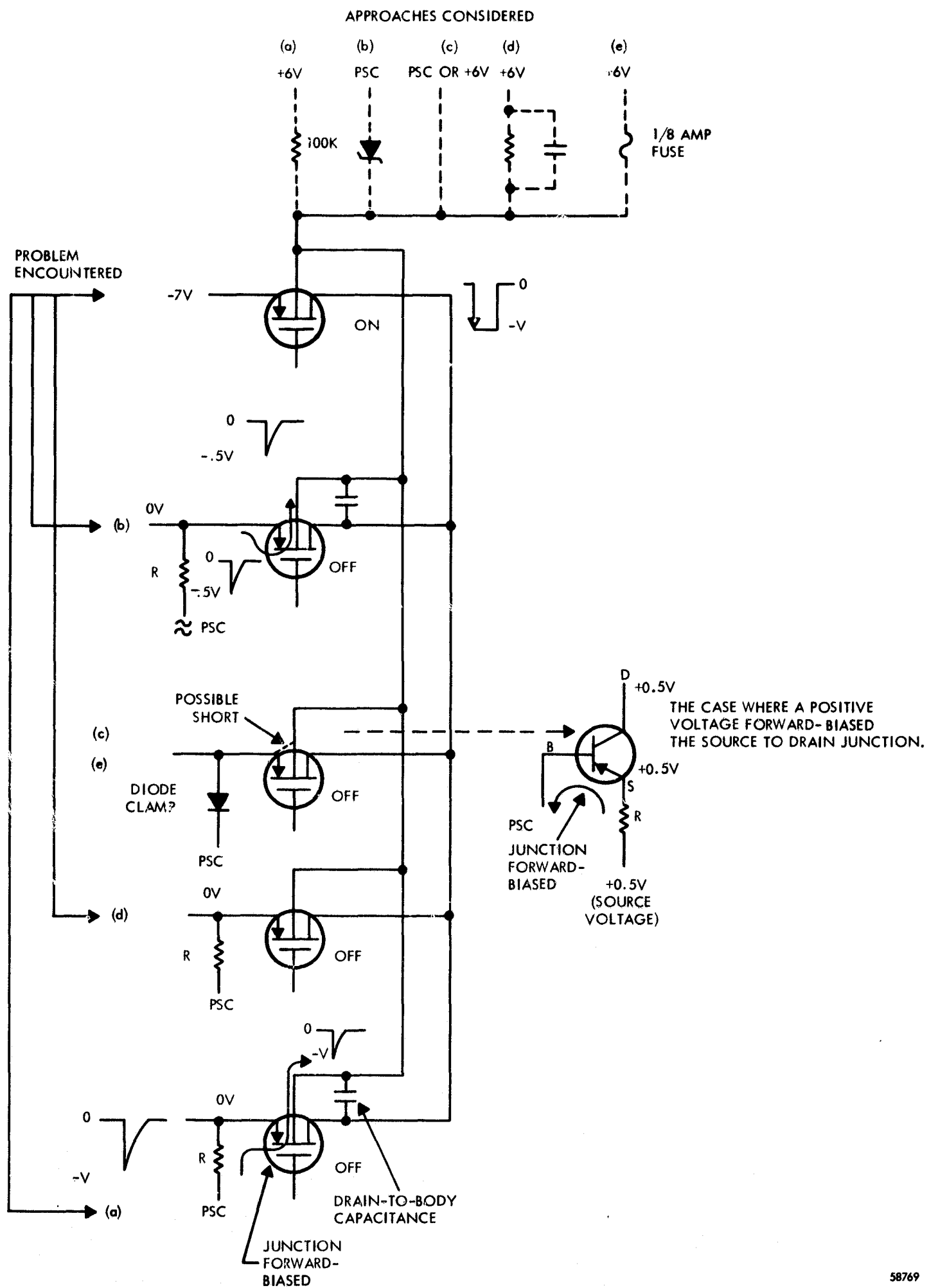
(A) EQUIVALENT CIRCUIT OF "ON" MOS GATE CAPACITANCE



(B) EQUIVALENT TRANSISTOR CAPACITOR MULTIPLIER CIRCUIT

Figure 92. MOSFET Gate Capacity

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Figure 93. Typical MOSFET Flatpack

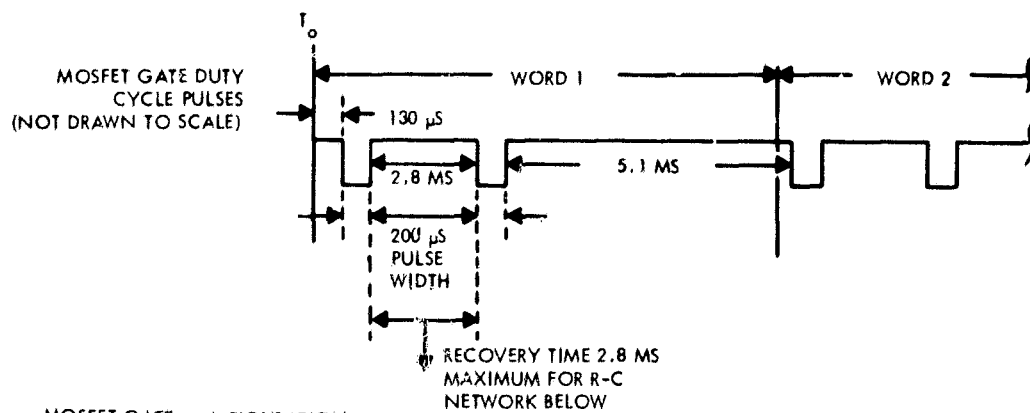
the gate. The positive voltage would remain on the drain terminal while the positive voltage was present on the source terminal, and the rest of the channels attached to this line would be inoperative. Another undesirable effect of grounding the body terminal is that a source-to-body short would cause the transducer at the input to that channel to be shorted to ground and possibly destroyed. If +6 volts were tied directly to the body lead of the MOSFET gate, the body would be tied to a low impedance point and protected from positive fault voltages up to +6 volts. However, a source-to-body short could then not only destroy the transducer but could also destroy the PCM power supply. A fuse between the body terminal of the MOSFET gate and +6 volts would probably provide the required protection to the PCM power supply. However, the only fuse that could be obtained at this time that would fit into the system was rated at 1/8 ampere. Because there was a possibility that the fuse would not blow even if a source-to-body short should occur (due to the transducer resistance, etc.), it was decided that this was not an ideal solution.

An R-C network between the body terminal of the MOSFET gate and +6 volts provides the required positive overvoltage protection and also provides a low impedance reference point for the body. The R-C network was decided upon as the best solution to the problem, with the only drawback being the addition of several capacitors to the system. An analysis of the R-C network is contained in the following paragraph.

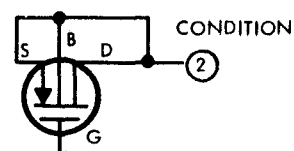
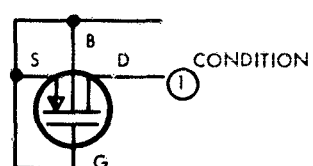
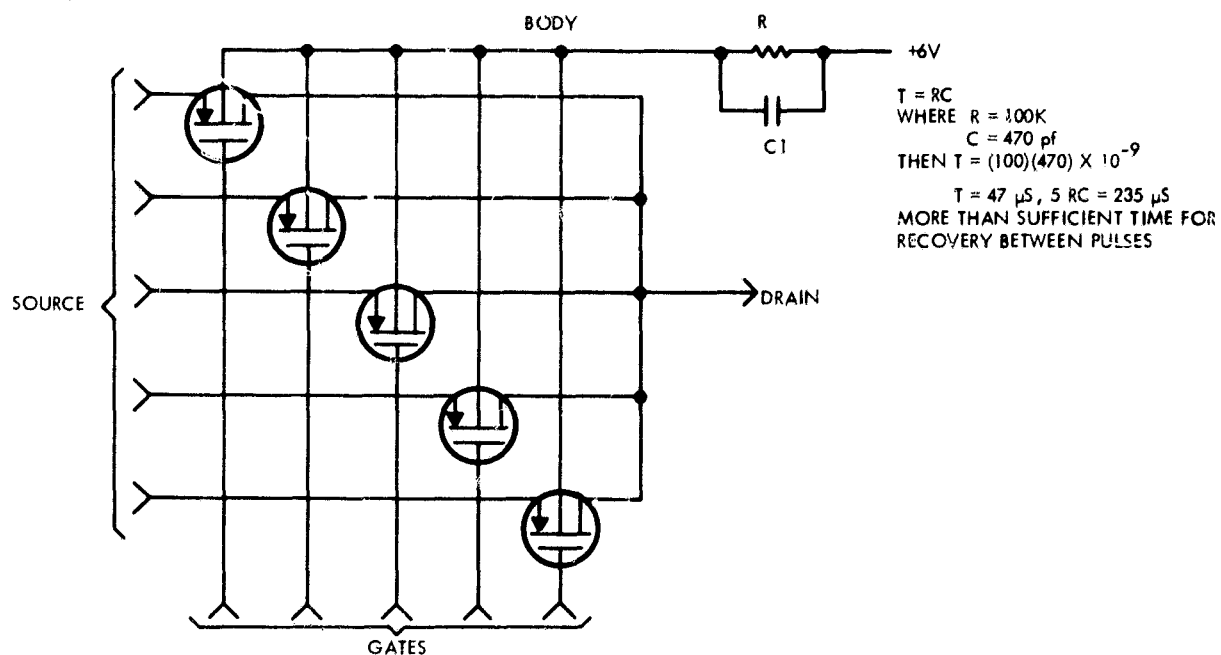
The R-C network should contain a resistance large enough so that if the body terminal shorts to another element in the gate, the increased load on the +6-volt power supply would be negligible. This value of resistance was chosen to be 100K ohms. As shown in figure 94, the minimum time between MOSFET gate duty cycle pulses is 2.8 milliseconds. The value of C_1 must be chosen such that $T = 5RC$ is less than 2.8 milliseconds, and such that the body terminal of the MOSFET gate never goes below ground under either of the conditions described previously. The MOSFET gate specification states that the maximum capacitance between the drain terminal and all other elements of the gate is 2 picofarads. The maximum capacitance between the gate terminal and all other elements of the gate is 3 picofarads. Since each flatpack contains five gates, the total capacitance is 10 and 15 picofarads for these two cases. Using the worst-case capacitance of 15 picofarads for C_2 (figure 94), C_1 should be no less than 65 picofarads to keep the body terminal of the MOSFET gate above ground. To ensure that the body terminal stays above ground (over temperature range, etc.), a value of 470 picofarads was chosen for C_1 . With $T = 5RC$ using a 470-picofarad capacitor and a 100-K ohm resistor, a time of 235 microseconds is obtained which is well within the 2.8 milliseconds allotted for recovery time of C_2 .

Figures 95 and 96 illustrate the different multiplexer arrangements between the analog and digital channels. These figures also show how the R-C networks will be installed in Nimbus B.

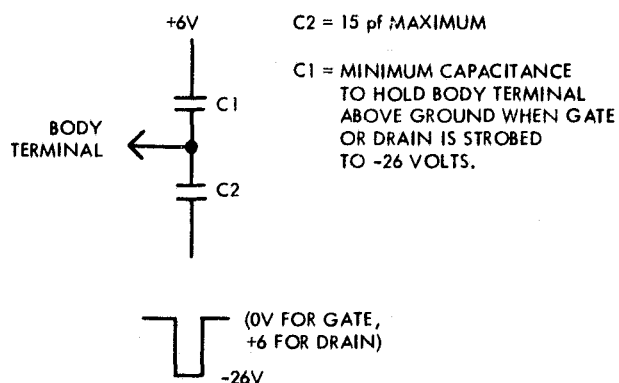
The final solution to both feedback noise problems provides for connection of the selected R-C network in all body connections of all MOSFET flatpacks for both the analog and digital channel gates, first sequencers, and final sequencers. With this problem solved (the only multiplexer problem), the new Nimbus study system multiplexer provides significant improvement over the old Nimbus system multiplexer. The advantages and disadvantages of the Nimbus study system are listed below.



MOSFET GATE CONFIGURATION IN FLAT PACK



USING WORSE CASE CAPACITANCE FOR C2 OF 15 pf THEN



$$C1 = \frac{(26V)(15) \times 10^{-12}}{6}$$

C1 = 65 pf MINIMUM
C1 WILL BE A 470 pf IN THE SYSTEM TO ENSURE THAT THE BODY IS HELD WELL ABOVE GROUND.

Figure 94. R-C Network Analysis

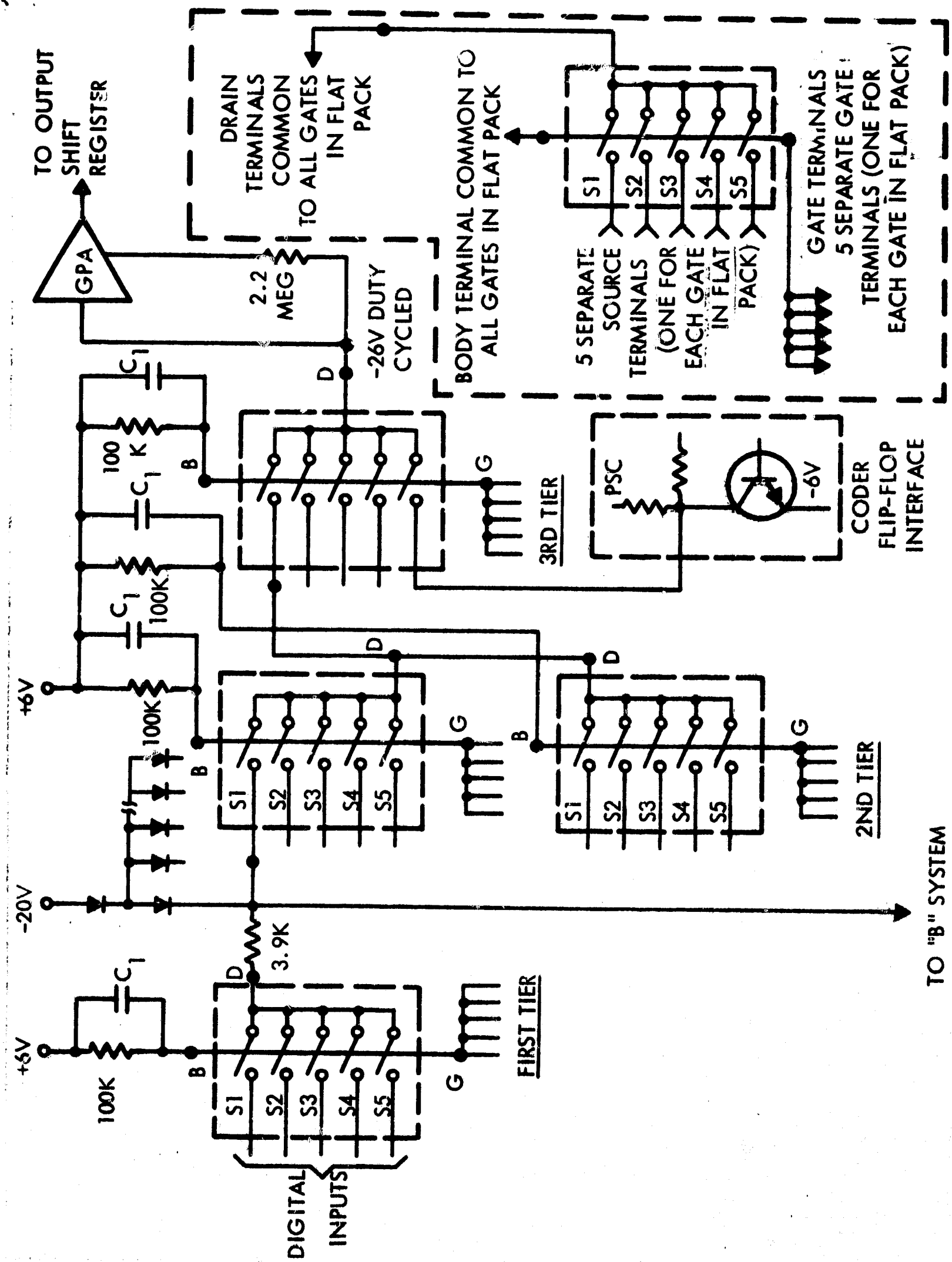


Figure 95. Prime and Subcommutated Digital Multiplexer Channels

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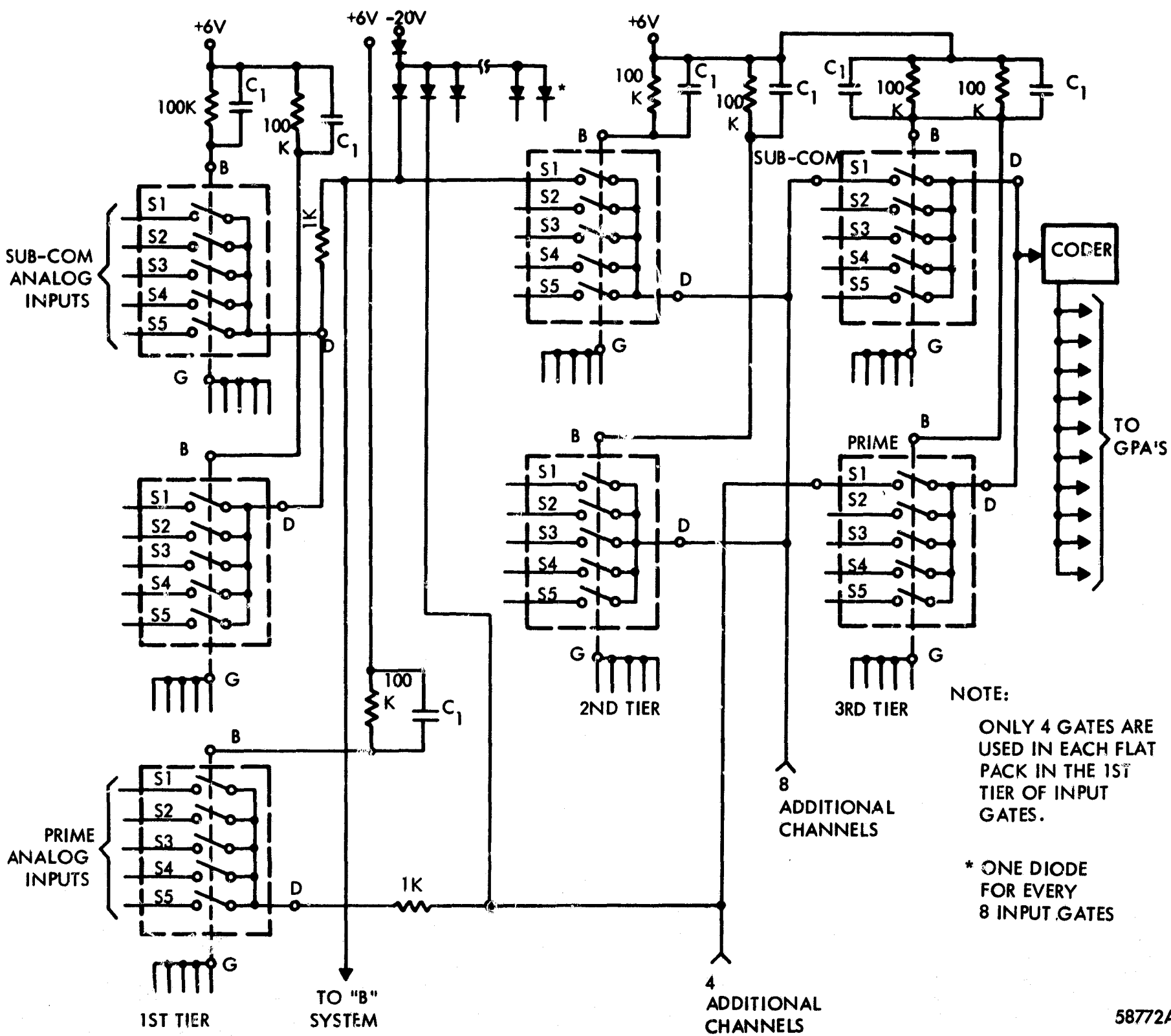


Figure 96. Prime and Subcommutated Analog Multiplexer Channels

- Advantages:**
- a. No droop in output sample to coder.
 - b. Less feedback current.
 - c. Higher fault voltage breakdown.
 - d. Smaller physical size.
 - e. More reliable operation.
 - f. More flexible design.
 - g. Has digital channel capability.
 - h. Can withstand wider temperature variations.
 - i. Less expensive future production.

- Disadvantages:**
- a. In present configuration, uses more power.
 - b. At present time, component parts require a longer delivery time from vendor.
 - c. Requires careful handling in receiving, inspection, and during fabrication because of susceptibility to static electricity.