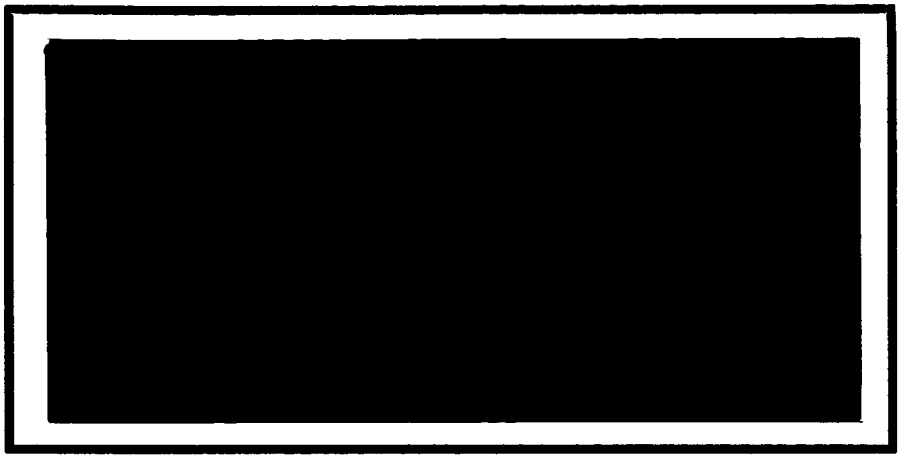

ELECTRONIC MATERIALS RESEARCH LABORATORY

THE UNIVERSITY OF TEXAS

COLLEGE OF ENGINEERING

AUSTIN

801

FIRST SEMIANNUAL REPORT

RESEARCH ON DIGITAL TRANSDUCER PRINCIPLES

to the

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

GRANT NGR 44-012-043

Covering the Period

July 1, 1966 - December 31, 1966

by

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I. INTRODUCTION

A transducer which feeds analog information to a digital data processor requires an analog-to-digital converter. The possibility of eliminating the converter by utilizing a digital transducer is an attractive one. This project originated from a conviction that such a concept is sound in a limited but useful way. This report describes theories and measurements which form the basis of a family of digital transducer principles.

A digital transducer is a device which initiates a discontinuous signal when the quantity sensed passes through a threshold value. Many discontinuous phenomena exist in nature which reflect a change-of-state at some threshold condition. The change in dielectric constant of $BaTiO_2$ with temperature is an example. Its performance would be limited by the hysteretic nature of the domain-flipping mechanism, however. More suitable mechanisms exist which are essentially reversible and can be exploited. From this point one asserts a digital transducer can be conceived which initiates a set of digital or stairstep responses to suitably spaced thresholds within the range of the quantity sensed.

Devices which meet the definition of an ordinary transducer may either generate a suitable signal or modulate a signal being generated elsewhere. Examples of these are the thermocouple and resistance wire thermometer respectively. A digital transducer can also be placed in either of these categories. A transducer would also qualify as being digital if it initiates a positive pulse each time the input rises through the next higher threshold, and initiates a negative pulse at each threshold on the way down. Fig. 1 illustrates typical input-output characteristics to be sought. The primary test for a true digital transducer, then, is its freedom from a separate analog-to-digital converter.

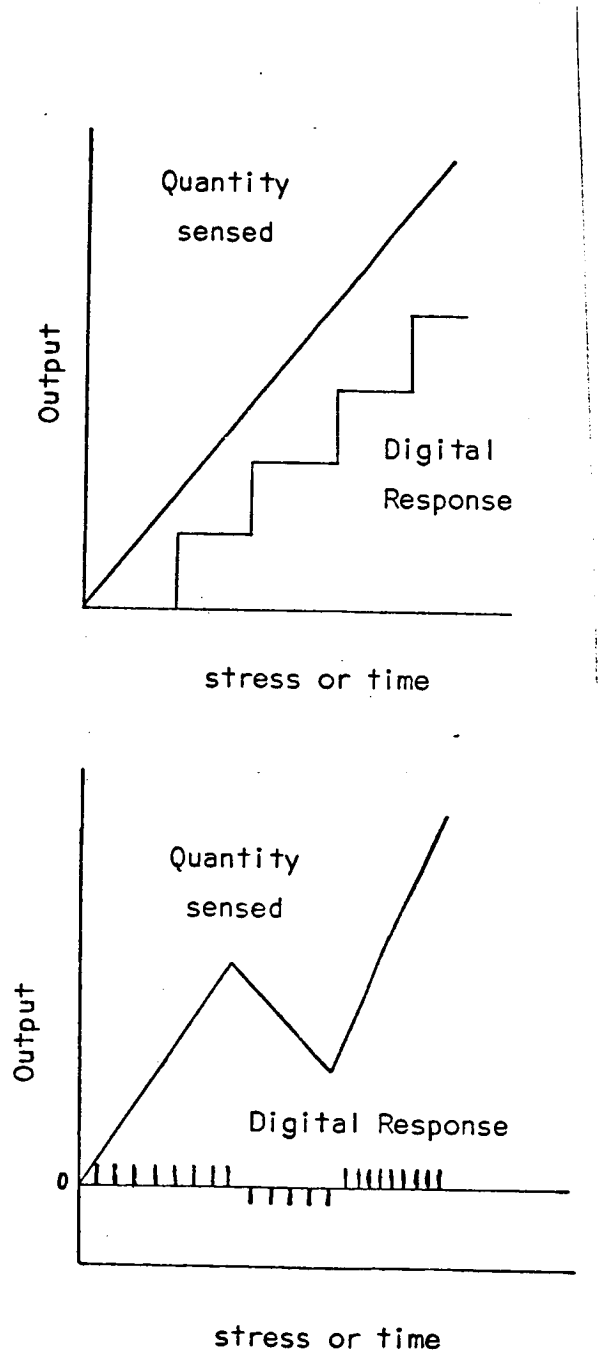


Figure 2 Digital Transducer Concept

II. PHYSICAL PHENOMENA OF POTENTIAL VALUE

A. A CATALOG OF PHYSICAL PHENOMENA

At this early stage in the program only an incomplete list of phenomena can be presented. It is not clear how completely this can ever be done since ingenuity and unexpected discovery will continue to be unbounded variables. An organized and documented body of knowledge, compartmented into recognizable segments for classification must be set up. Terms must be defined which facilitate discussion and analysis. This section is offered with the realization that the subject will eventually mature and a start has been made.

1. Cooperative Phenomena--This class includes those threshold phenomena which have a quality of coherence. A Q-switched laser is one example in which the transducer output is a light pulse when a reflecting mirror or prism has reached a chosen position. The similar statement can be made about the less sophisticated toy cap pistol. In both these examples the "transducer" needs to be "loaded" after each digital pulse response.

The condensation of normal electrons into superconducting pairs with opposite spins is a true digital behavior which can lead to cryogenic digital transducers for measuring temperature or magnetic field. Because it is a nearly ideal physical phenomenon, section II B describes workable devices in some detail.

Its applicability would be limited to temperatures less than 20°K since all known superconducting materials have critical temperatures below this value.

Another aspect of superconductivity ideally suited to digital transducer action is Josephsen tunneling. The effect is a zero voltage transport of charge across a very thin insulating film between two superconducting films. This component of current flows in addition to the familiar tunneling current consisting of single electrons. This effect is the basis of a new class of cryotrons, as recently shown by Matisoo (1). The Josephsen tunneling current is exceedingly rapid, with switching times well below a nanosecond. The transition is the removal of the Josephsen component with a magnetic field generated by a control current in an adjacent superconductor. There is no transition from the superconducting to normal states in this mechanism. In a digital transducer the device would consist of several junctions in series or parallel, with each one switched at a preset value of an external magnetic field. The transitions are sharp and reproducible but the entire concept is limited by the low temperature requirement.

2. Exhaustion Phenomena--This class includes those phenomena which cause a discontinuity due to exhaustion of stored charge. The exhaustion of space charge in thermionic diodes is a familiar example. As plate voltage is raised the plate current tends to saturate at a value set by the cathode temperature.

A less familiar example is the exhaustion of surface charge

states in semiconductors. This effect has been studied in thin-film tunneling configurations and is sufficiently promising to merit closer investigation. The theory of digital transducers using this phenomenon is described in the next chapters.

3. Unstable Phenomena--This class includes avalanche effects which have a threshold. Zener breakdown in P-N junctions is an example. Multiple discontinuities in the voltage-current characteristics have been observed and may become a digital transducer mechanism if the external influence is sufficiently developed.

4. Geometry-Limited Phenomena--There are numerous examples of discontinuous behavior determined by a moving boundary reaching a discontinuity in a device. An example would be a depletion zone in a semiconductor crystal widening until it encountered a surface with higher or lower conductivity. This effect may prove to be a means of building a multiple-step transducer in which the first step would terminate by a depletion zone reaching its limit and other steps continuing until they are successively terminated.

This concept is a possible means of commutation of several transducers in addition to being the basis for digital response. This is being considered in conjunction with the surface state exhaustion studies.

5. Ordering and Phase Transformations in Metals--This is a broad and complex class of phenomena in solids which may include some of the others in this list. We refer here to a restricted group

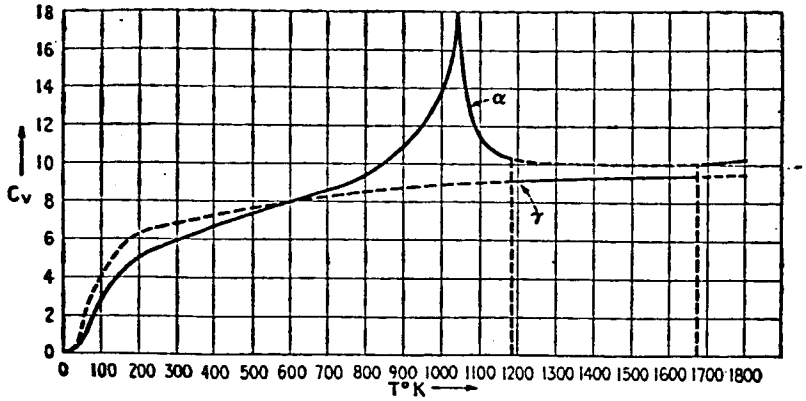
of behaviors in metals which are reflected in their specific heat, magnetic and resistive behavior with temperature and pressure. The subject is covered by Seitz (2) and many more recent texts. It is a class of behavior which is hysteretic and slow in going to completion. The figures on the next page are taken from Seitz's examples. In general a rearrangement of atom positions, such as the α - γ phase transition in iron, or the change from disorder to order in the arrangement of atoms of CuPd or Fe_3Al, is not a phenomenon which would give reversible characteristics. While the discontinuities are evident, they are well known and do not seem particularily attractive for digital transducers.

The antiferromagnetic and ferrimagnetic effects are different from ferromagnetism in the alignment of electron spins. Antiferromagnetism is displayed in crystals of compounds like MnO in which the Mn ions are arranged with antiparallel spins. At some sufficiently high temperature, called the Ne'el Temperature, the paired spin configuration breaks down completely. Above this temperature they behave as normal paramagnetic materials.

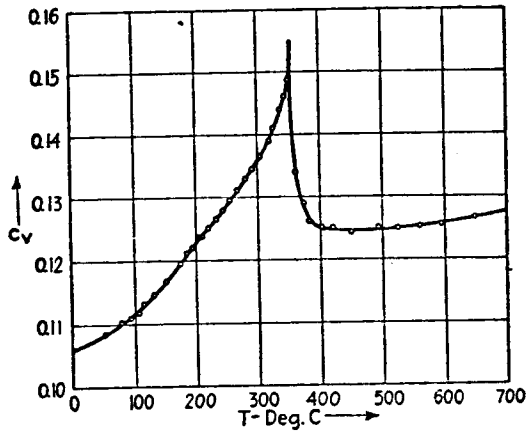
Ferrites are a special group, being ionic crystals of metal atoms plus Fe and O; $MeFe_2O_4$. The unit cell has 24 Fe atoms, 16 trivalent and 8 divalent. The 8 divalent atoms have aligned moments which gives the crystal a net moment and an incomplete antiferromagnetic spin arrangement.

While these materials are extremely interesting, no obvious application to a novel digital transducer is seen at this time.

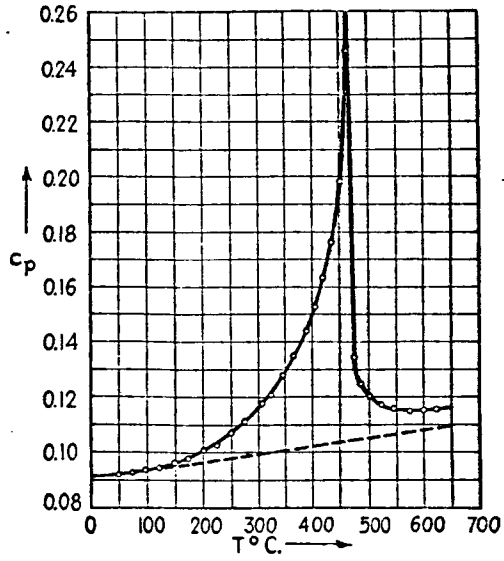
Figure 2. Examples of Order-Disorder and Phase Transformations in Metals (See Seitz, Reference 2)



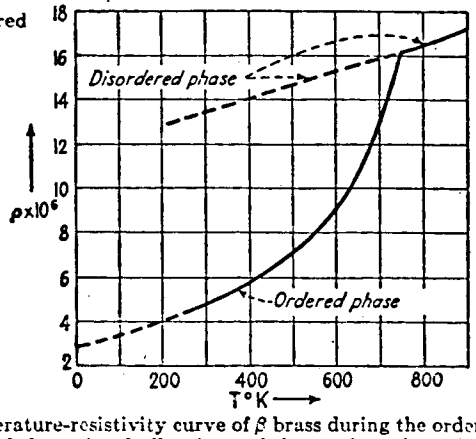
—The atomic-heat curves of α and γ iron. The ordinates are cal/mol. (*After Austin.*)



—The specific heat of nickel in the vicinity of the Curie temperature. (*After Moser.*)



—The specific heat of β brass during the transition from the ordered to a disordered structure. (*After Moser.*)



—The temperature-resistivity curve of β brass during the ordering transition. The residual resistivity of the ordered alloy is much lower than that of the disordered phase.

6. Resonance and Relaxation Phenomena--There is a variety of natural resonance and relaxation phenomena which would have true digital response of a pulse type. Magnetic resonance is an example of numerous frequency dependent magnetic effects in solids. These include paramagnetic relaxation effects and nuclear resonance which reflect a complex susceptibility. In a high frequency magnetic field Gorter (3) observed the build-up of magnetization could be represented by the equation

$$dM/dt = (M_e - M)/\tau$$

where M_e is the equilibrium value and τ is an equivalent relaxation time. This phenomenon has an analog in dielectrics which leads to a complex permittivity. In each behavior the relaxation time is best represented by a distribution of relaxation times.

The paramagnetic phenomena are best understood by considering a material which contains a randomly oriented group of free magnetic dipoles. If a uniform external magnetic field is applied the dipoles will precess about the H vector but not orient themselves. The only way in which they will add to the magnetization is by exchanging energy with their surroundings. The relaxation occurs as a spin-lattice or spin-spin mechanism. The essential difference between them is seen by comparing the size of the applied field, H_a, and the local field set up by neighboring dipoles, H_i. For $H_a \ll H_i$ precession about the H_i vector is shifted to a slightly different direction. There is an energy exchange between each dipole and the field but not with the lattice.

Spin-lattice relaxation occurs when $H_a >> H_i$ and the field direction is determined by H_a. If the value of H_a is changed the number of dipoles in parallel and antiparallel orientations is shifted toward a new equilibrium value by exchange of energy with the lattice.

Since atomic nuclei have a magnetic moment associated with their angular momentum, there is a nuclear analog to the paramagnetic relaxation. Nuclear Magnetic Resonance is well known and is the basis for numerous measuring instruments. The sharp response as frequency and magnetic field are tuned to their proper values for the material in the measurement suggests this as an attractive digital transducer phenomenon.

7. Dipole Orientation--Dielectric materials display a wide variety of behavior which make them attractive for digital transducer applications. Orientation of dipoles, electrostriction, piezoelectricity, ferroelectricity, optical and electro-optical phenomena, and tunneling are some of the properties which are not found in metals.

Dipole orientation in an external electric field is found in some materials at their freezing points and in others below their freezing points. Fig. 3 is taken from Wert and Thomson, Physics of Solids, McGraw-Hill, 1964 which shows an example of each kind. Molecules with permanent dipoles become oriented with the E vector just above critical temperature and rotation is hindered below this.

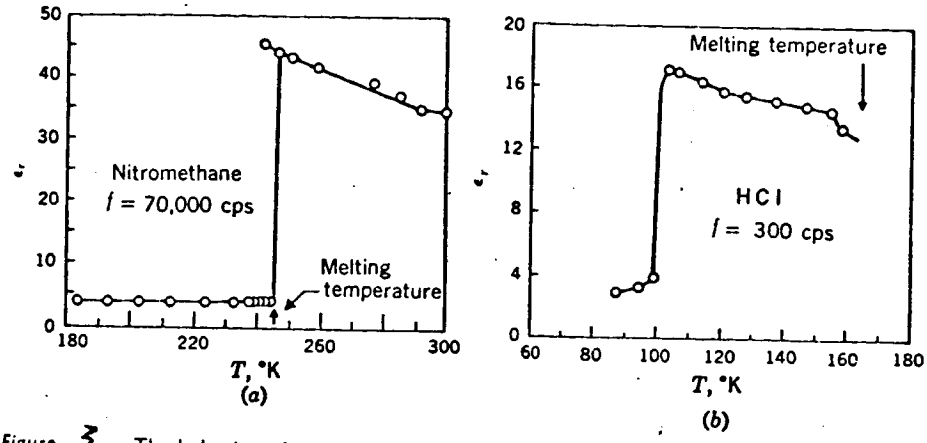


Figure 3 The behavior of ϵ_r versus T for completely hindered (*a*) and partly hindered (*b*) rotation of dipoles in the solid. (*a*) Nitromethane. [*Data of C. Smyth and W. Walls, J. Chem. Phys.*, **3**: 557 (1935).]; (*b*) Hydrogen chloride. [*Data of C. Smyth and C. Hitchcock, J. Am. Chem. Soc.*, **55**: 1830 (1933), *by permission of the American Chemical Society.*]

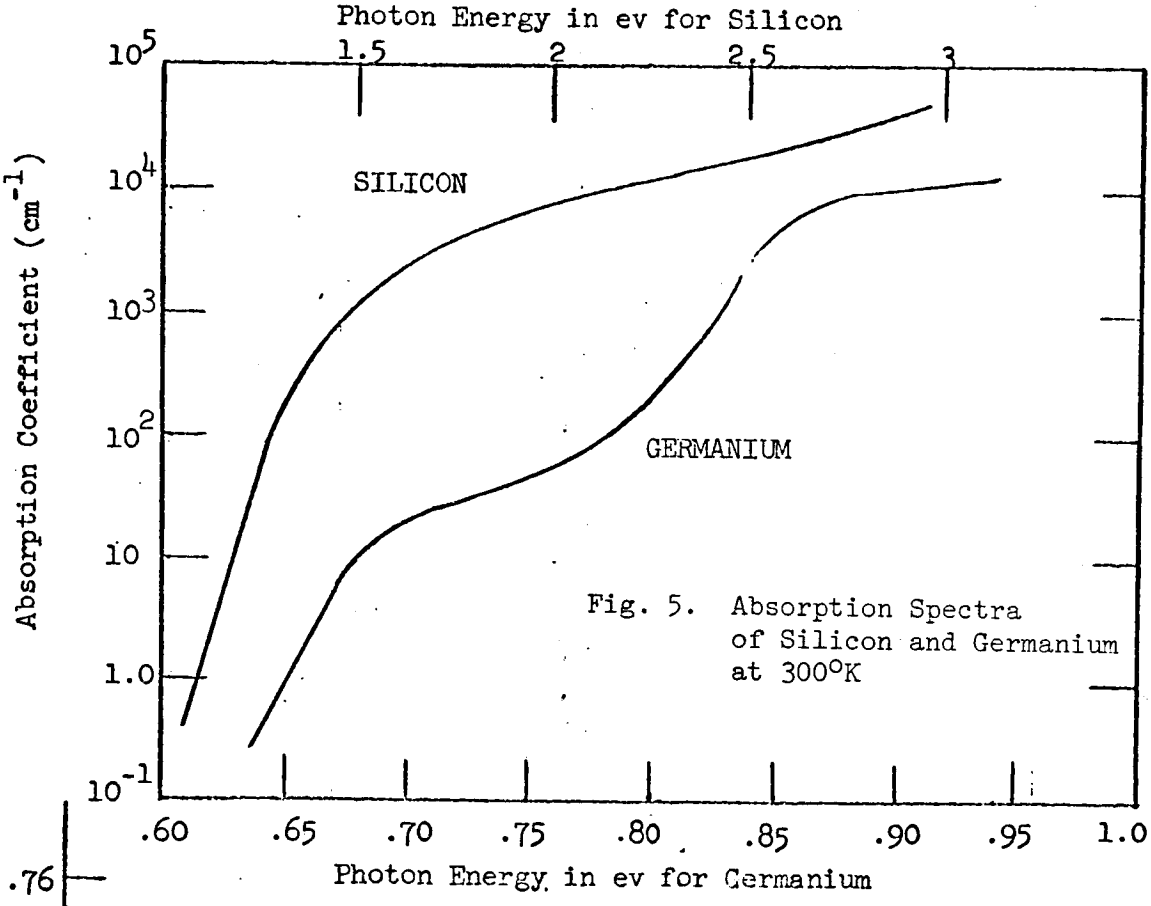


Fig. 5. Absorption Spectra of Silicon and Germanium at 300°K

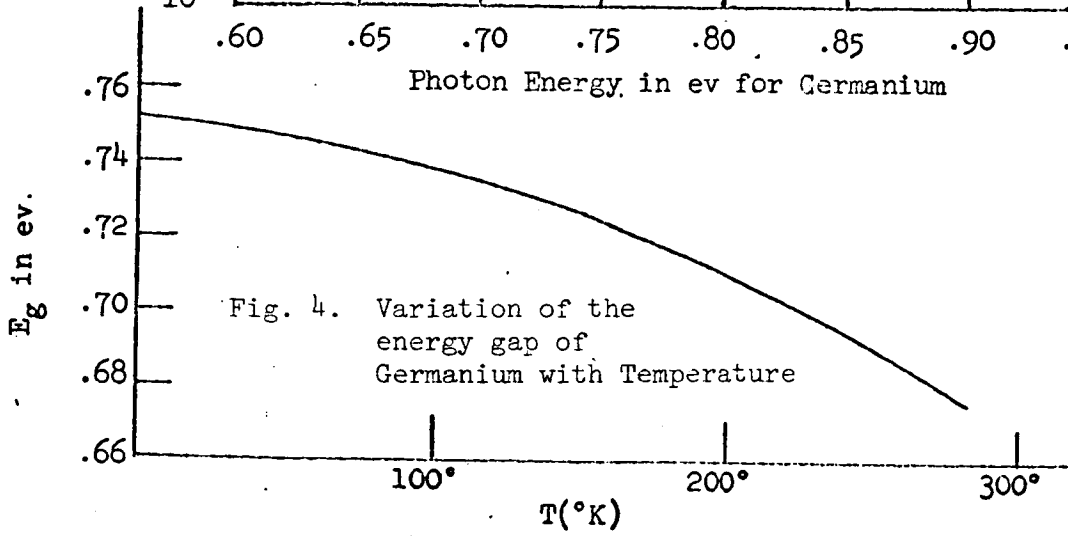


Fig. 4. Variation of the energy gap of Germanium with Temperature

Electrostriction and piezoelectricity are properties of numerous crystalline solids such as quartz, Rochelle salts, ammonium dihydrogen phosphate and potassium dihydrogen phosphate. These materials have low crystalline symmetry, as contrasted with NaCl. They display a polarization-strain behavior which is the basis for numerous analog digital transducers.

Ferroelectric materials, such as barium titanate, and potassium niobate have a spontaneous polarization when subject to strain. The polarization is propagated by domain-flipping similar to ferromagnetism in iron. There is a nearly complete analogy, in fact, because the ferroelectrics have hysteresis and a Curie temperature above which the effect disappears.

A digital transducer is readily conceived using the discontinuities in dielectric constant of several materials. A capacitor which would have discontinuous changes in capacity with temperature can be constructed with this effect. This has been studied by the author and the result leaves much to be desired. The discontinuities are evident, but so is hysteresis and an intolerable analog drift between discontinuities.

The successful use of dielectric materials is felt to depend upon using combinations of properties. Chapter IV describes such a concept. The transducer action is provided by one effect and the discontinuities are injected by another.

8. Band Gap Effects and Optical Transparency--Semiconductors are transparent to wavelengths longer than hc/Eg where Eg is the band gap energy, and opaque to much shorter wavelengths (4) (5). The transition region is fairly abrupt, as shown in Fig. 4. The optical transparency changes two decades for a change of less than 8% in the wavelength of light falling on germanium at 300°K.

The band gap itself is a function of temperature as shown in Fig. 5. It is also a function of temperature and pressure, in fact the piezoresistance of homogeneous semiconductors has been studied quite extensively by Keyes (6). Furthermore, Rindner and Braum studying shallow p-n junctions (7) showed anisotropic elastic stress caused completely reversible resistance decreases by several orders of magnitude. Considerable reduction of the breakdown voltage can be observed. The digital transducer concepts which are suggested involve strain or temperature modulation of the band gaps of selected semiconductors.

II. B. EXAMPLES OF PRACTICAL DIGITAL TRANSDUCERS

1. Digital Temperature Transducer Using Superconducting Transitions

The best example of a proven high-speed reversible effect which could be used as a digital transducer is the superconducting transistion with temperature and/or magnetic field. No difficulty would be experienced in constructing a transducer which would produce sharp reversible steps in resistance over the range 0-20°K (or over the range 0-100,000 gauss). A series of resistors,

each made from a different metal, would have a discontinuous change in total resistance at each transition temperature. The device pictured in Fig. 6 has 18 steps between 0.14°K and 18.2°K. No essential technological limitations prevent the fabrication of such a transducer. The actual transducer would be built to have uniform steps in resistance by adjusting the length and cross-sectional area of each leg. Some adjustment in the transition temperature is possible to space the steps on the temperature axis. The transition temperature of a thin film of metal A can be shifted toward that of metal B if a thin film of B is deposited on top of it.

Such a digital cryogenic temperature transducer would have crisp transitions between the steps. For example the onset to superconductivity in tin occurs within a few millidegrees.

2. Digital Cryogenic Magnetic Field Transducer--A completely separate application of this transducer would be its stepwise response to an external magnetic field at constant temperature. At any given temperature each metal which is in the superconducting state can be switched reversibly into the normal state in some critical value of B. For example, at 3°K a digital cryogenic magnetic field transducer with series elements of Sn, Hg, Ta, Pb, V, and Nb would have discontinuous responses at .010, .020, .045, .068, .082, and .175 webers/m^2 respectively. Fig. 7 is taken from Applied Superconductivity by Vernon L. Newhouse, John Wiley and Sons, New York, 1964.

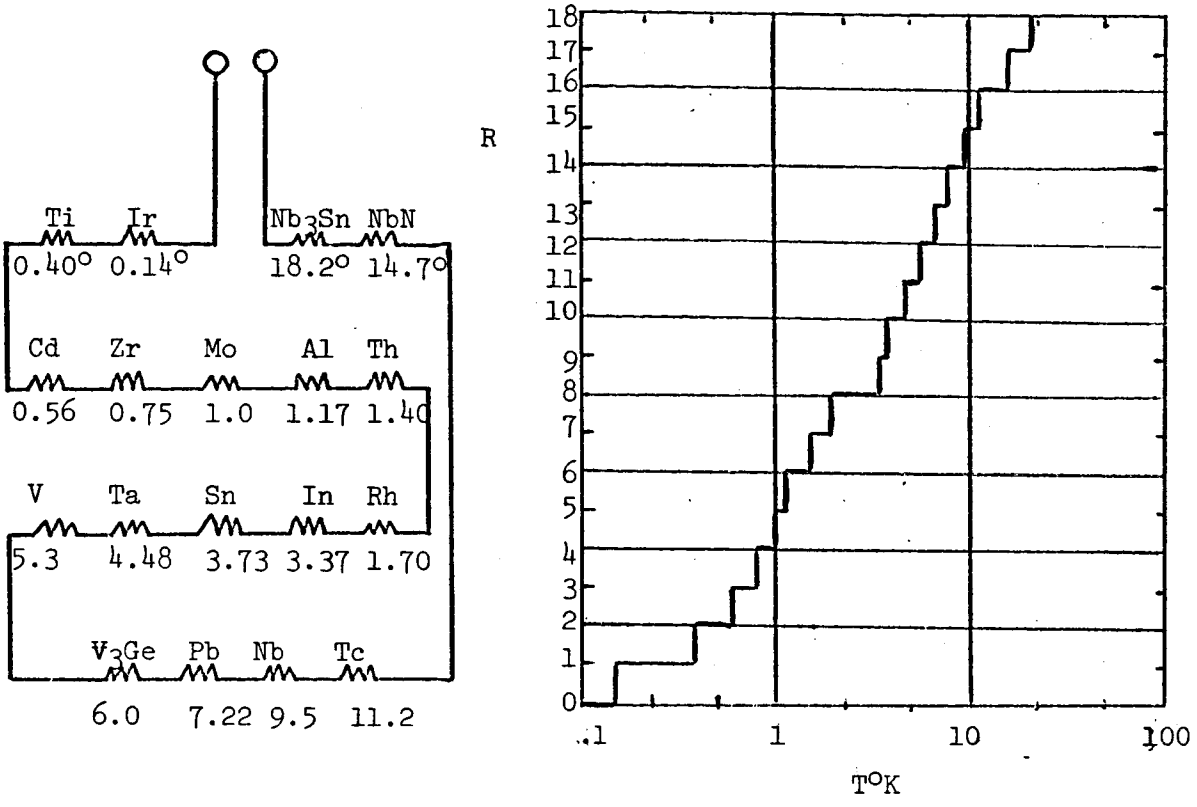


Fig. 6 Cryogenic Digital Resistance - Temperature Transducer

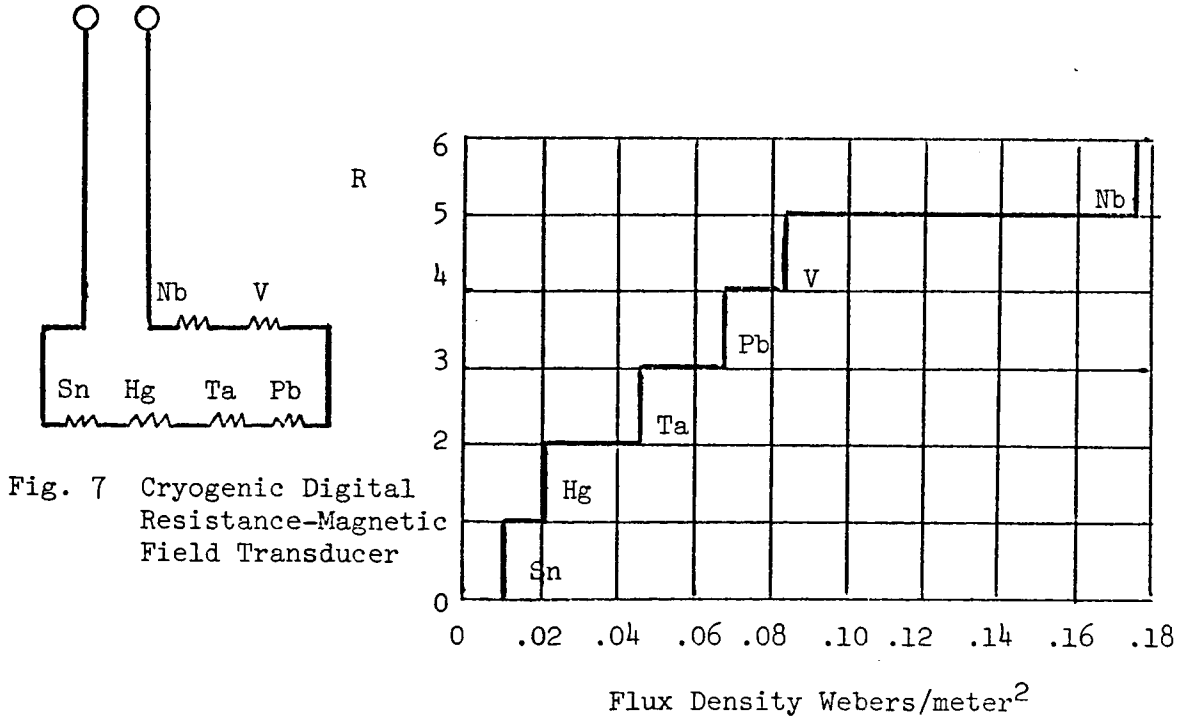


Fig. 7 Cryogenic Digital Resistance-Magnetic Field Transducer

These examples of true digital transducers are practical in every respect; they can be fabricated without extensive new technology, they display crisp discontinuities which are reversible and repeatable, no large amount of external circuitry is involved, the application itself insures the presence of the cryogenic environment, and the transducer should be able to withstand repeated cycling if properly designed and fabricated. We plan to demonstrate this transducer at a convenient date.

3. Commercial Digital Transducers--There are a few digital transducers on the commercial market, but from the survey made so far, they do not operate on a basis which clearly meets the objectives of this program. They involve legitimate phenomena, such as the frequency dependence of "water-hammer" upon liquid flow parameters, or the number of interference fringes in an optical system, but require considerable sensing apparatus.

III. TUNNELING THEORY FOR MIS DIGITAL TRANSDUCERS

A. TUNNELING BEHAVIOR IN MIS STRUCTURES

A promising effect which is classified as an exhaustion phenomenon is seen in tunneling between metal and silicon separated by a thin insulator. A theoretical model describing the tunneling is presented along with experimental data on both metal- metal and metal- silicon tunneling. The insulator for the experimental devices was formed by polymerizing diffusion pump oil with 350 volt electrons by the process described by Christy (8) and Mann (9).

Metal - metal tunneling was studied first in order to establish the properties of tunneling through the polymer film. The room temperature current-voltage characteristics of a metal-polymer-metal sample are shown in Fig. 8 . This device was constructed by vapor depositing a stripe of aluminum on a glass substrate. A polymer film is formed over part of the stripe. A cross strip of aluminum is then vapor deposited to form a tunneling junction. The current is in mμA and the voltage in volts. The small circles are experimental points. The X's are a fit of Stratton's Metal- Metal tunneling equation (10). The polymer of this sample is 80Å thick. Fig. 9 illustrates the room temperature current-voltage characteristics of a Metal - insulator - N type silicon tunneling junction. This device was constructed by forming the polymer insulator on a chemically cleaned 60 ohm cm N-type silicon wafer.

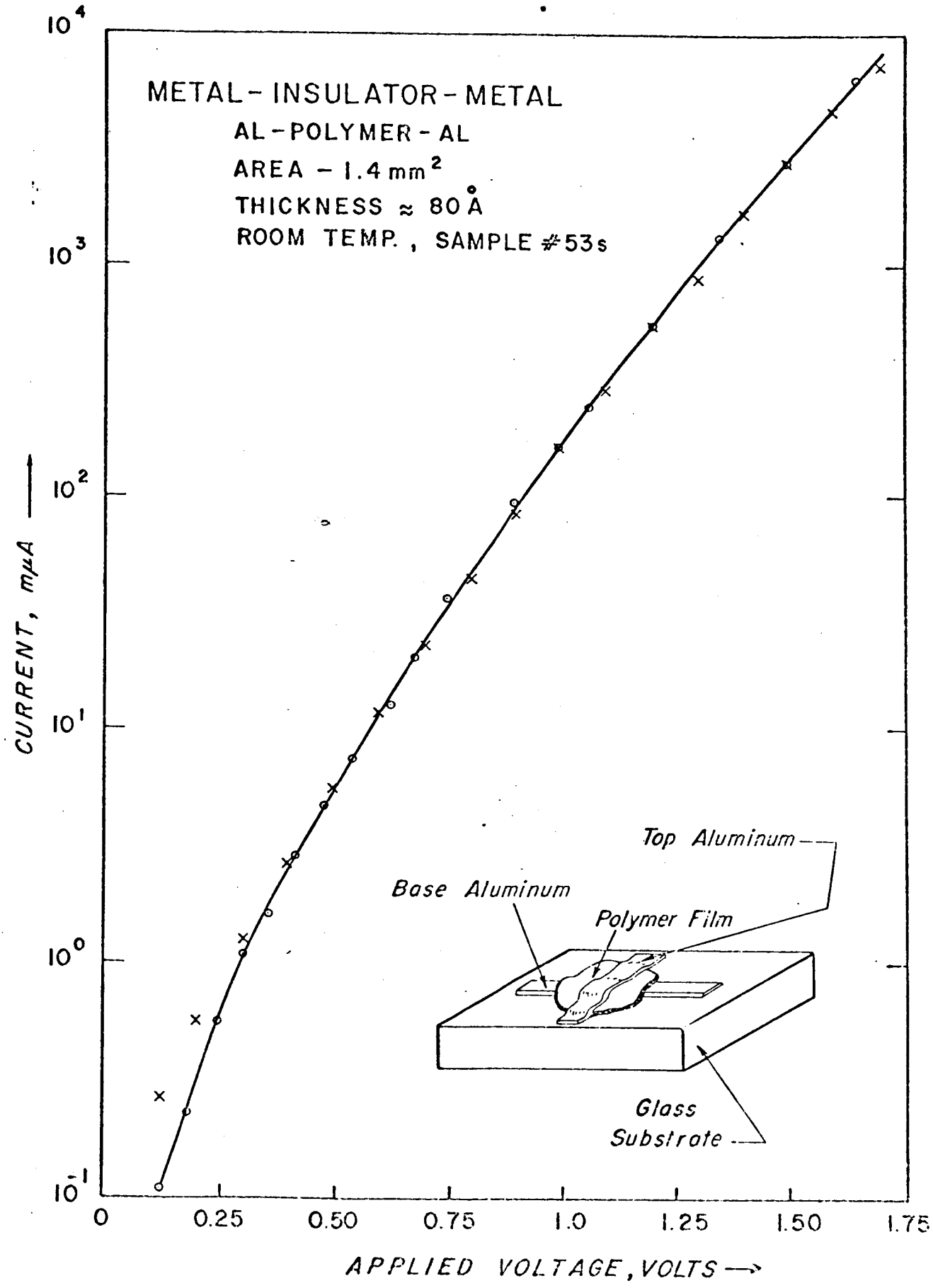
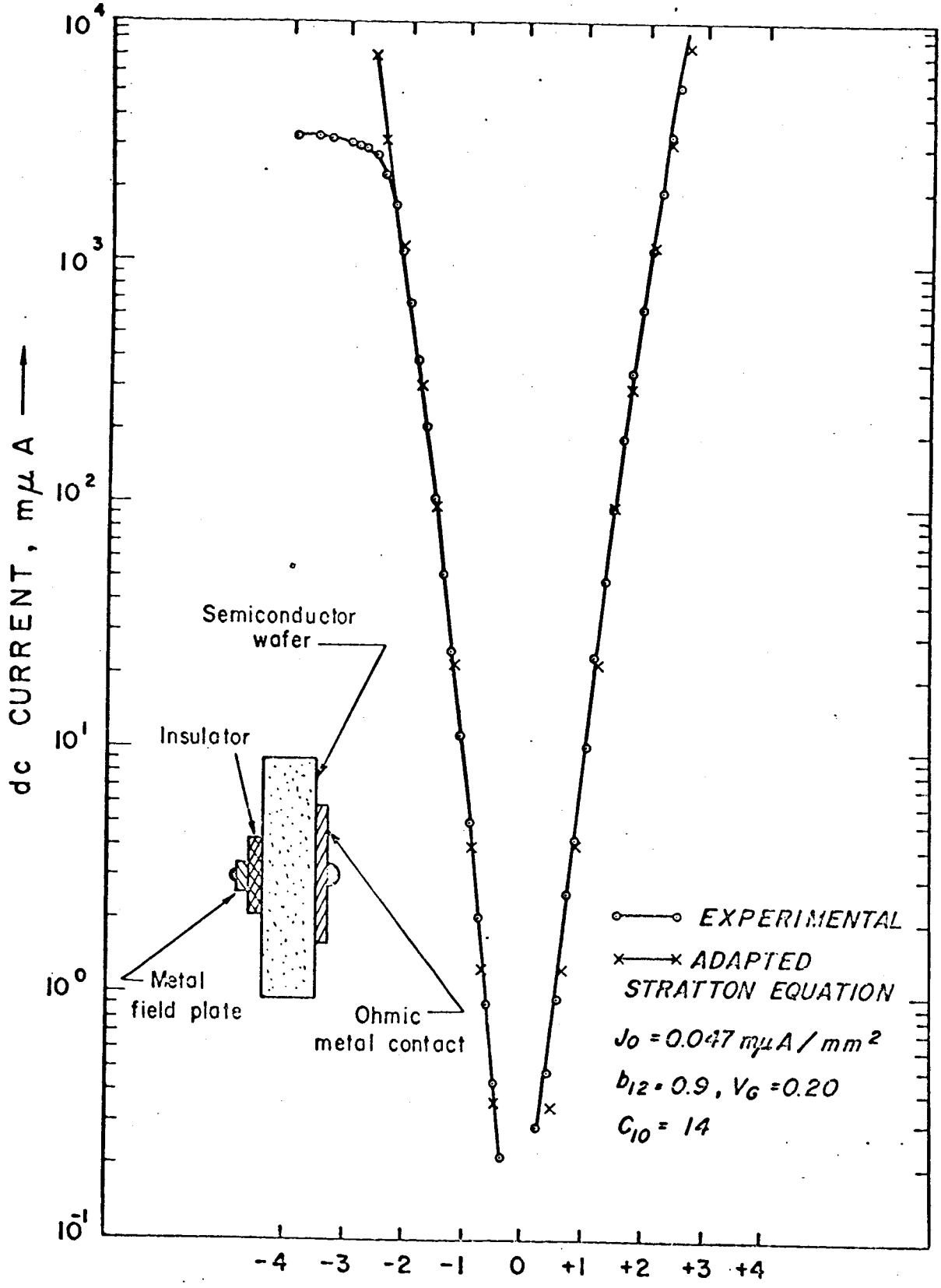

METAL-INSULATOR-METAL
AL-POLYMER-AL
AREA - 1.4 mm²
THICKNESS ≈ 80 Å
ROOM TEMP., SAMPLE #53s
CURRENT, mμA
APPLIED VOLTAGE, VOLTS
Top Aluminum
Base Aluminum
Polymer Film
Glass Substrate

Figure 8



CURRENT-VOLTAGE CHARACTERISTICS

N-TYPE SILICON #30si

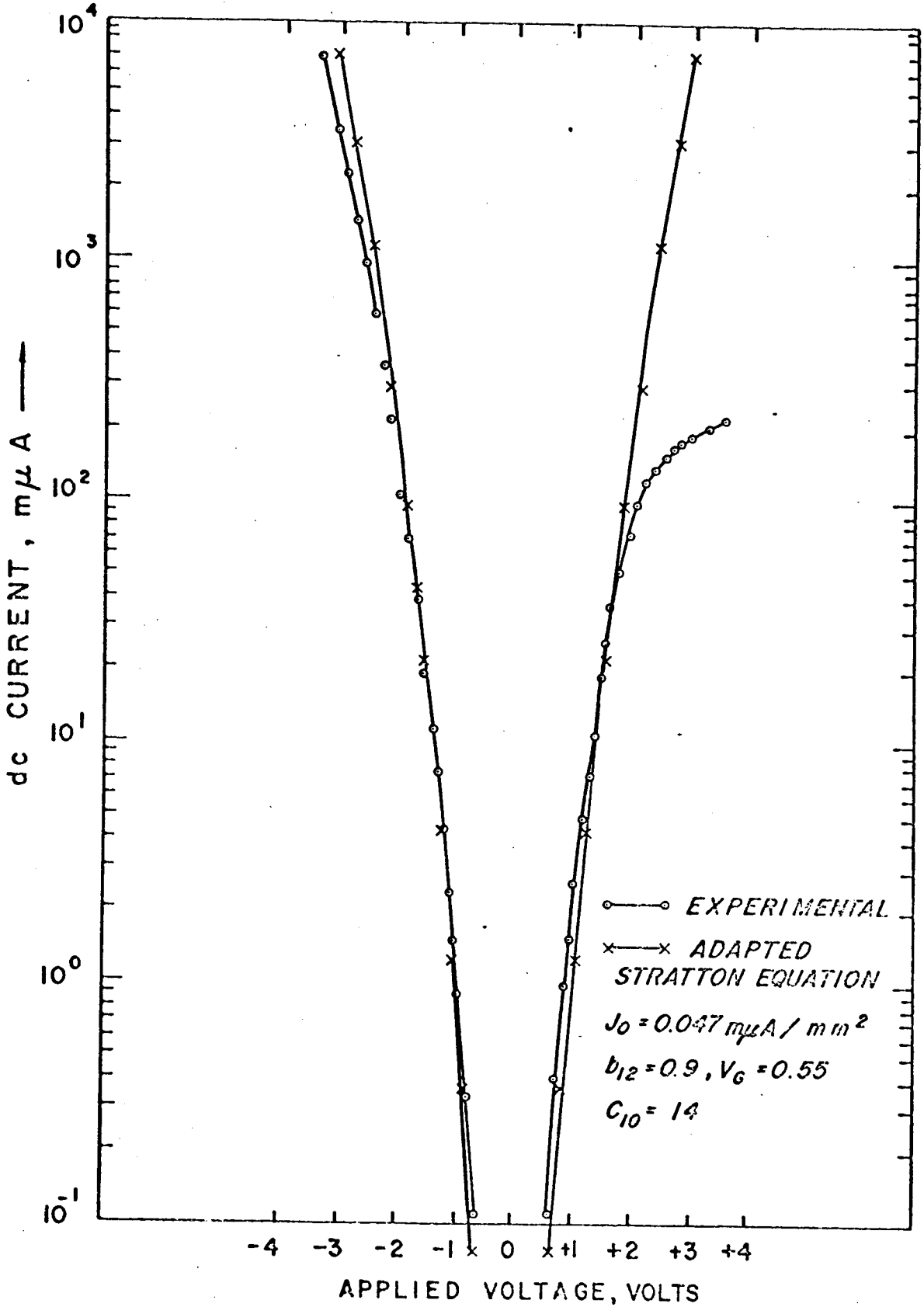
60 Ω CM - ROOM TEMP, INSULATOR THICKNESS ≈ 80 Å°

Figure 9

A small metal dot field plate was then vapor deposited on the polymer. The insulator thickness is 80 Å as was the Metal - Metal sample. (The current is in mμA and the voltage in volts as before. The small circles are experimental points. The X's are points calculated with Stratton's equation with the constants reduced approximately 10% from the metal-metal fit. To account for the modulation of the forbidden band the applied voltage is replaced by $V_A - V_G$, where V_G is taken to be 0.2 volts. The agreement is remarkable. A saturation of the current for negative voltage occurs. Note that the experimental curve follows the modified metal - metal equation up to the point of current saturation. The theory of tunneling as developed by Stratton and modified to fit MIS data are given in Section C.

Fig. 10 illustrates the results with a 100 ohm-cm P-type silicon substrate. The X's are calculated with the same constants as with N-type silicon, but the voltage, V_G, required to align tunneling states, is increased from 0.2 to 0.55 volts. The current saturation now occurs with positive voltage. The current and voltage scales are the same as on the previous N-type silicon slide. When plotted on a linear scale these curves have the same shape as those reported by Gray (11) (12).

The saturation behavior of reverse-biased metal - silicon tunneling can be explained in terms of exhaustion of the surface states of the silicon. The high density of surface states give the semiconductor a metal-like surface. When an external voltage is applied, charge accumulates in



CURRENT-VOLTAGE CHARACTERISTICS

P-TYPE SILICON $\sim 17\,\Omega$-cm - ROOM TEMP, INSULATOR THICKNESS $\approx 80\,\text{Å}$

Figure 10

the surface states. The electric field lines terminate on this accumulated surface charge, therefore, the insulator field is proportional to the applied voltage. As the external bias is increased the charging of the surface continues until the surface states are exhausted. Further increase in the applied voltage creates either an accumulation layer or a depletion layer in the silicon depending upon the conductivity type of the silicon and polarity of the applied voltage. If an accumulation layer forms, then the insulator field does not penetrate the semiconductor bulk and continues to increase. Therefore tunneling current increases in an exponential manner as before. If a depletion layer forms, then the field lines terminate on ionized dopant states in the bulk. The field now penetrates the bulk and the field in the insulator levels off and approaches a constant. As a result the tunneling current also levels off. The field penetration occurs with positive voltage on P-type and negative voltage on N-type.

To verify this theory, we examined the effect of insulator thickness upon the current saturation. The insulator field at saturation is related by Gauss' law to the maximum charge that can collect at the surface. The charge, Q, is dependent upon the insulator thickness since the field plate metal and the silicon transfer charge in order to align the Fermi level. However, for small thickness changes, the maximum field is approximately constant. Tunneling current is dependent upon the insulator field, therefore, the value of the current

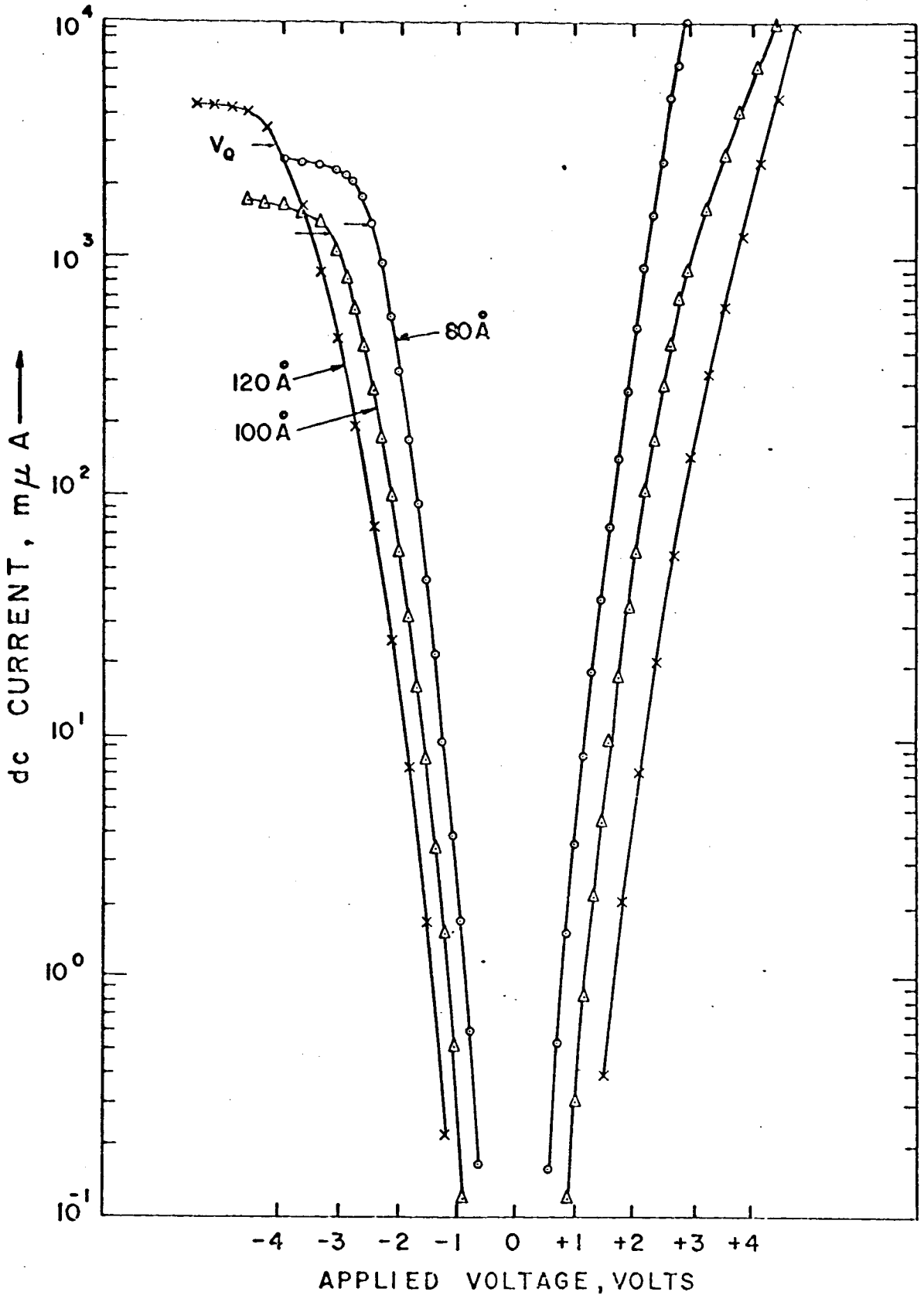
at saturation is approximately independent of insulator thickness since the maximum insulator field is constant.

To experimentally test this property three samples with different insulator thickness were constructed on N-type silicon with an aluminum field plate. The insulator thickness of the samples are 80, 100, and 120 Å. Fig. 11 shows the V-I characteristics of the three samples. The tunneling currents are reduced due to the reduced field but the current level at saturation is approximately constant. This is in agreement with the model. To assign a point of saturation, the V-I curves are extrapolated beyond saturation. The difference in the extrapolated and experimental curves is taken to be the voltage drop across the depleted layer of the semiconductor. This voltage is plotted versus applied voltage for the three samples in Fig. 12. The voltage, V, is then taken to be the applied voltage at which the extrapolated V_s line is equal to zero. The field calculated with this V_Q is found to be approximately independent of insulator thickness as shown in Fig. 13.

This is taken as strong evidence in support of the proposed metal - insulator - silicon tunneling model. Experiments involving the variation of temperature and work function of the field plate metal also provide verifying evidence.

B. SIGNIFICANCE OF MIS TUNNELING SATURATION

This phenomenon has several features which make it attractive. The behavior is reversible, that is there is no hysteresis



MIS TUNNELING

N-TYPE SILICON, 60Ω CM, ROOM TEMP, AREA = 0.85 mm²

THICKNESS ≈ 80 Å - #32si

≈ 100 Å - #33si

≈ 120 Å - #36si

Figure 11

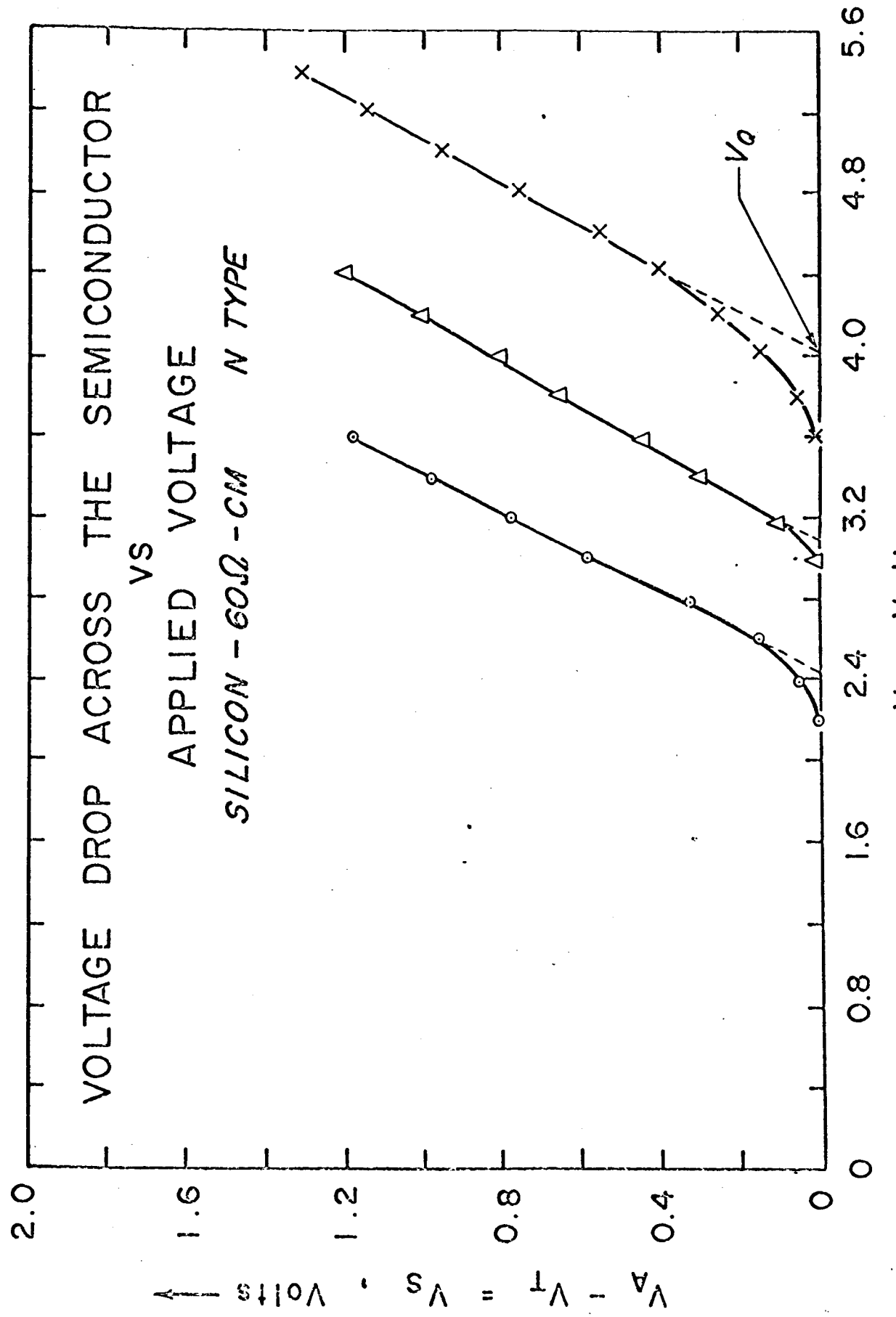

VOLTAGE DROP ACROSS THE SEMICONDUCTOR
VS
APPLIED VOLTAGE
SILICON - 60Ω - CM N TYPE
V_o
$V_A - V_T = V_S$, Volts
V_A , Volts
0
0.4
0.8
1.2
1.6
2.0
0
0.8
1.6
2.4
3.2
4.0
4.8
5.6

Figure 12

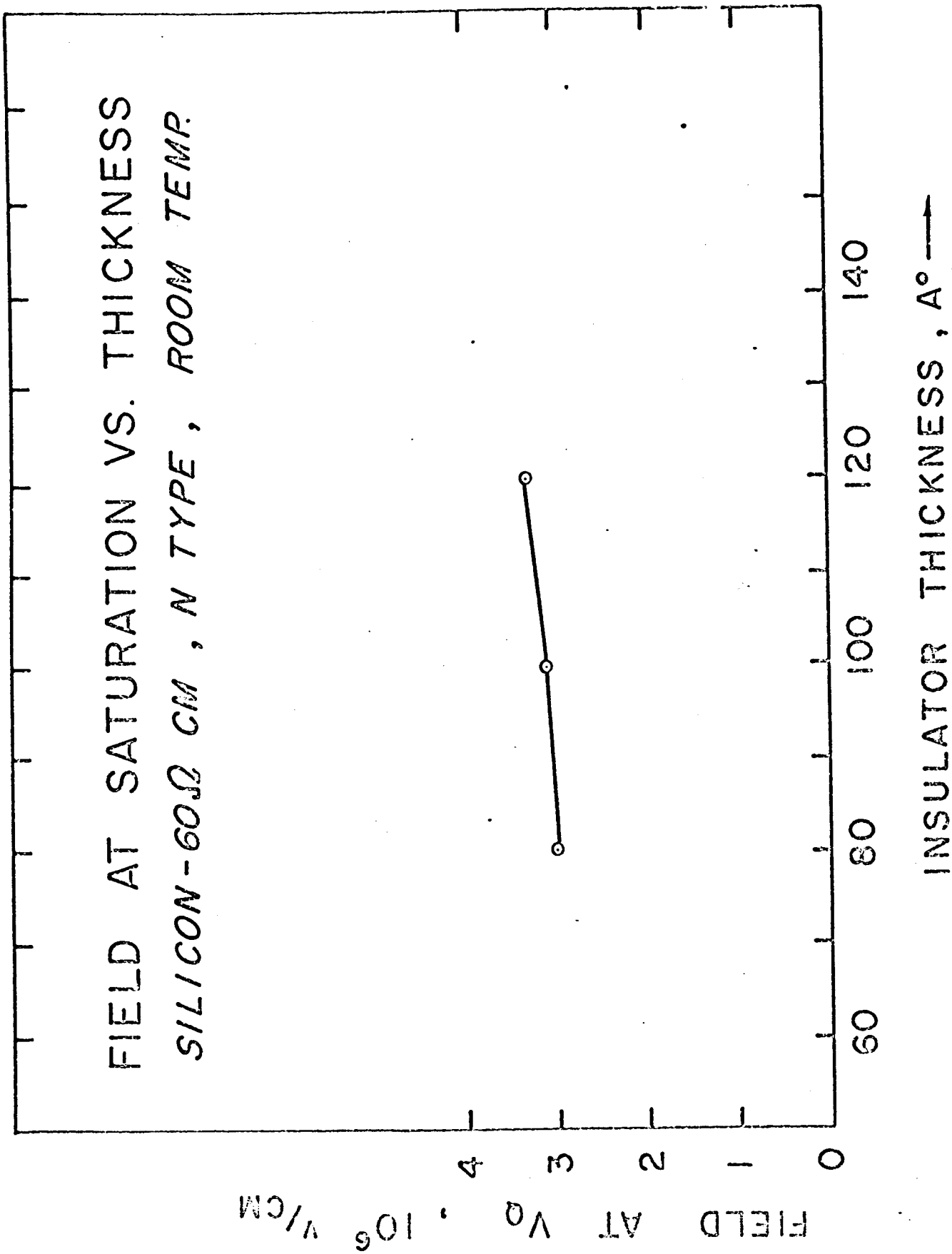

FIELD AT SATURATION VS. THICKNESS
SILICON - 60Ω CM , N TYPE , ROOM TEMP.
FIELD AT V_0 , 10^6 V/CM
0
1
2
3
4
60
80
100
120
140
INSULATOR THICKNESS , A° ——

Figure 13

effect, at least in the range of frequencies measured. There is a frequency dependence, however, which is discussed in the next chapter.

The discontinuity in the I-V curve is polarity sensitive and is subject to several external parameters. Several of these parameters are susceptible of being a "sensed" quantity in the transducer application including temperature and light intensity. Other internal parameters can provide the step location; for example, work function of the field plate area or thickness of the dielectric and doping level of the semiconductor. The exact shape of the discontinuity is not yet completely understood, but it clearly is a function of the surface properties of the semiconductor.

C. TUNNELING THEORY

1. Metal-Insulator-Metal Tunneling--Electrons can pass between two metals separated by an insulating film by at least two processes, Schottky emission or tunneling. While there are other mechanisms which invoke atomic scale properties of the insulator, these two are well known in electron device theory.

Normal emission is the process which allows thermionic or photocathodes to give off electrons in vacuum or gas tubes. The electron must gain enough energy to leave its positively charged nucleus in the metal surface. For the thermionic emitter, where the temperature is high enough, a significant number of electrons can exceed the work function. The emission can be enhanced by an electric field normal to the surface. The increase in emission is called the Schottky Effect and is an exponential function of the square-root of the field.

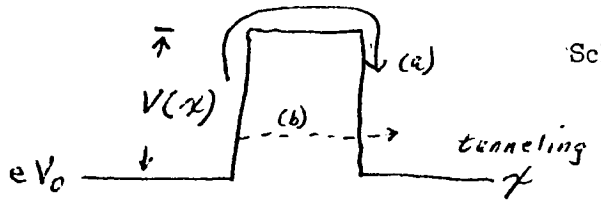
$$J_s = C\epsilon^{\alpha E^{1/2}}$$

This mechanism will be important in explaining some of the charge transport through thin insulating films between metals. It is represented by path (a) in Fig. 14.

Of more immediate interest, however, is a quantum-mechanical process whereby an electron can pass through the insulating film without overcoming a potential barrier. This phenomenon is best understood in terms of the wave properties of the

electron. Theories have been derived by Simmons (13) and Stratton (14) which are similar in their results for MIM tunneling. We have made an empirical approach to MIS tunneling by modifying their expressions.

2. Metal-Metal Tunneling Theory



Schottky Emission

Figure 14

The time independent wave equation is

$$1. \qquad \frac{d^2\psi}{dx^2} + K[E - eV(x)]\psi = 0$$

where E is the expectation value of total energy, and eV(x) is the shape of the potential barrier.

Case I $V(x) = V_B$ = constant --This has a solution.

$$2. \qquad \psi \propto \varepsilon^{\alpha(E - eV_B)^{1/2} x} \qquad eV_B > E$$

Case II. When V(x) is not a constant, which occurs when an electric field is present in a solid dielectric, no closed solution is possible. A WKB approximation assumes a solution of the form

$$3. \qquad \psi = A(x)\varepsilon^{iS(x)/\hbar} = \varepsilon^{iw/\hbar}$$

This form is differentiated and substituted into the wave-equation and real and imaginary parts separated.

$$4. \qquad \dot{S}^2 - 2m(E - eV(x)) = \hbar^2 \ddot{A}/A$$

$$5. \qquad 2\dot{A}\dot{S} + A\ddot{S} = 0$$

which in turn leads to

$$6.\quad \dot{S}^2 = 2m[E - eV(x)] + \hbar^2\left[\frac{3}{4}\left(\frac{\dot{S}'}{\dot{S}}\right)^2 - \frac{1}{2}\frac{\dddot{S}}{\dot{S}}\right]$$

Eq 3. is a solution only if 6. is satisfield. So far there is no approximation. To proceed from here the WKB approximation is made for S in a power series in $\hbar^2$

$$7.\quad \begin{aligned} S &= S_o + \hbar^2 S_i + \hbar^4 S_2 + \ldots \\ \dot{S} &= S_o' + \hbar^2 S_1' + \ldots \\ \ddot{S} &= S_o'' + \hbar^2 S_1'' + \ldots \end{aligned}$$

By dropping enough terms (those in $\hbar^2$ and higher) one gets

$$8.\quad (\dot{S}) \simeq (\dot{S}_o) = 2m[(E-eV(x)]$$

$$9.\quad S = S_o = \pm\int\sqrt{2m[E-eV(x)]}\,dx$$

Substituting 9. into 3. gives the solution inside the barrier.

$$10.\quad \psi \simeq K\ exp\left[-\frac{1}{\hbar}\int\sqrt{2m[eV(x)-E_x]}\,dx\right] = KD(E_x)$$

The exponential term is the <u>transmission coefficient</u> D(Ex).

The current tunneling from one side of the barrier is the number of electrons which impinge upon the barrier per second times the transmission coefficient.

$$11.\quad dJ_x = ev_x\, D(E_x)n(v_x)dv_x$$

where $n(v_x)dv_x$ = density of electrons with velocities between

$$v_x \text{ and } v_x + dv_x$$

and in terms of the Fermi distribution, f(E);

$$n(v_x) = \frac{4\pi m^2}{\hbar^3}\int_0^{\infty} f(E)dE \text{ where } E = \text{total K.E.},$$

$$E = 1/2\ mv^2$$

Thus

$$12.\quad J_x = \frac{4\pi em}{\hbar^3}\int D(E_x)dE_x\int f(E)dE$$

Since current can tunnel from both sides, the net current is

$$13.\quad J_x = \frac{4\pi em}{h^3}\int_0^{E_{max}} D(E_x)dE_x\int_0^{\infty}[f(E) - f(E + eV)]dE$$

where the energy of electrons in the second electrode has been shifted by a bias voltage to eV.

13 is a starting point for most authors in the derivation of MIM tunneling. The significant differences appear in the approximation of the transmission coefficient D(Ex). The principle methods have been given by Simmons and Stratton

Both equations of Simmons and Stratton adequately describe tunneling through thin oxide films.

Stratton's Equation is used, which starts with

$$14.\quad J = \frac{4\pi em}{h^3}\int_0^{\infty}[f_1(E) - f_2(E)]dE\int_0^{E} D(E_x)dE_x$$

assuming

$$15.\quad D(E_x) = \exp\left[-\int_{x_1}^{x_2}[\phi(x,V) + E_F - E_x]^{1/2}dx\right.$$

where x_1 and x_2 are the values of x where $\phi(x) = E_x$ (classical turning points)

$\phi(x,V)$ = the barrier energy profile measured above E_F

E_F = fermi energy above the bottom of valence band

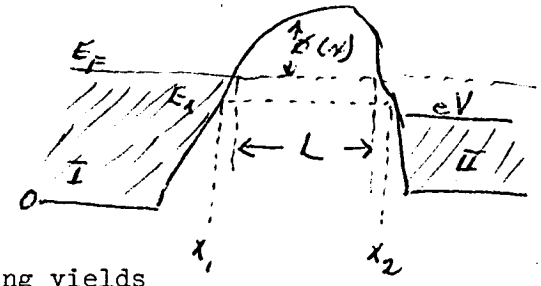


Figure 15

Integrating yields

16. $$J_x = \frac{4\pi em}{h^3} kT \int_0^\infty D(E_x) \ell n \left\{ \frac{1 + \exp\left(\frac{E_F - E_x}{kT}\right)}{1 + \exp\left(\frac{E_F - E_x - eV}{kT}\right)} \right\} dE_x$$

Simmons and Stratton agree to here.

The barrier profile with external bias goes from $\phi_o(x)$ for zero bias to $\phi(x,V) = \phi_o + \frac{eVx}{L}$

Stratton assumes electrons near the Fermi level dominate the tunneling transport, so he expands the coefficient of $D(E_x)$ in powers of $e_x = E_F - E_x$, or

17. $$\ell n\, D(E_x) = b_1 + c_1 E_x + \text{---}$$

and only the first two terms are kept.

This yields

18. $$J_x = \frac{B\pi c_1 kT}{(c_1 kT)^2 \sin(\pi c_1 kT)} \varepsilon^{(-b_1)(1-\exp(-c_1 V))}$$

$$B = 4\pi em(kT)^2/h^3$$

Since b_1 and c_1 are functions of applied voltage, they are expanded in a power series in V.

$$b_1(V) = b_{10} - b_{11}V + b_{12}V^2 + \text{---}$$
$$c_1(V) = c_{10} - c_{11}V + c_{12}V^2 + \text{---} \qquad 19.$$

Stratton keeps the first 3 terms of $b_1(V)$ and only c_{10}. This leads to

$$20. \quad J_x \approx J_o\left(\frac{2\pi c_{10}kT}{\sin(\pi c_{10}kT)}\right) \exp[(b_{11}V - b_{12}V^2)(1-\varepsilon^{-c_{10}V})$$

This can be further simplified for symmetrical barriers; $x = L/2$, $b_{11} = 1/2\ c_{10}$, thus

$$21. \quad J_x = J_o\left(\frac{2\pi c_{10}kT}{\sin(\pi c_{10}kT)}\right) \exp\left[-b_{12}V^2 \sinh \frac{c_{10}V}{2}\right]$$

Temperature dependence

Since b_{10}, c_{10} and J_0 are independent of temperature 21 can be written

$$J_x\Big|_{V = \text{const.}} = J(T) = J(0)\frac{\pi c_{10}kT}{\sin(\pi c_{10}kT)} \qquad 22$$

where $J_o \neq J(0)$. Expanding the sine as a power series

$$J_x(T) \approx J(0) + \gamma T^2 + \text{---} \qquad 23$$

Simmons results for $J_x(T)$ agree with this.

3. Tunneling into a Semiconductor

Basically one expects at least two major effects, 1, the presence of the forbidden band would influence the voltage scale to higher values, and 2, conservation of momentum requirements would influence the magnitude of the current to reduce it.

An emperical expression is taken from Stratton

$$J_x = J_o\left(\frac{2\pi c_{10}' kT}{\sin(\pi c_{10}' kT)}\right) \exp\left[- b_{12}'(V_A - V_G)^2\right]\sinh\left[\frac{c_{10}'}{2}(V_A - V_G)\right]$$

where $c_{10}' < c_{10}$ and $b_{12}' > b_{12}$ and would be fitted experimentally at first. V_A = applied voltage and V_G is the voltage required to adjust for the relative positions of the Fermi levels in the silicon and metal.

The data can be made to fit the curve which gives the emperical expression some utility. The present state of knowledge on the tunneling between a metal and a semiconductor does not permit much more to be done for the present. The data is very precise but the range of voltages and thickness can take the curves into regions where the theories may not be valid. The effort which is now required should be directed toward more basic understanding of the mechanisms governing the transport of charge through thin insulating films.

IV. TUNNELING DIGITAL TRANSDUCER CONCEPTS

A. PRELIMINARY DESIGN AND ANALYSIS

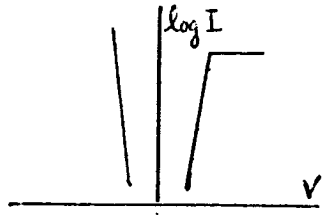


Figure 16

The volt-ampere characteristics of a tunneling MIS device is shown in the sketch. From the experiments conducted so far we can say this is but one member of each of several families of curves. For a family in which work function is a parameter the second sketch is typical, while the third shows a family

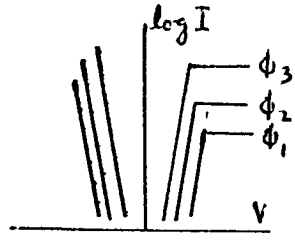


Figure 17

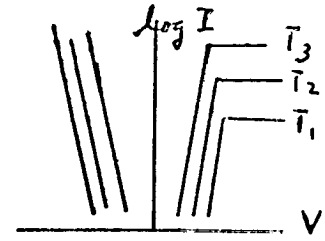


Figure 18

with temperature as a parameter. There are other families with parameters such as thickness, doping level and dielectric constant. The digital transducers which will attract the greatest interest are those with some parameter controlled by an external stimulus. We are exploring those parameters to determine how the solid state properties govern the detailed shape of the characteristics.

The first generation digital transducer action is possible by several approaches having one feature in common, it will have a bias current or voltage, such as does an analog resistance strain gage. The second generation of digital transducer

action may not require a bias, a piezoelectric strain gage is an analog example of such a device. The number of variables in this investigation is large and a rich field of possible new electron devices seems to be open to development.

Several versions of MIS tunneling arrays could be constructed to demonstrate digital action. A voltage-to-current or current-to-voltage A-D converter is planned as the first multiple-step device. While it is a very elementary form of transducer, it has digital response and may have some utility as just an A-D converter. While the development of digital transducer concepts is the stated goal of the grant, a new form of A-D converter which is compatible with integrated circuit technology would seem a welcome bonus.

The design of a three-step device is planned and may appear in several forms as described below.

1. PRELIMINARY DESIGN

The tunneling curves shown in the previous chapter have coordinates of log I and V, amperes and volts. An independent group of parameters are; area, thickness of the polymer insulating film, work function of the metal field plate and several parameters characteristic of the semiconductor.

Area of these devices could readily vary over a range of 10^4 to 1, with some adjustment possible after fabrication. No doubt field plates 3 cm. in diameter could be deposited, and 0.3mm is not regarded as a minimum. The fabrication problems are similar to the state-of-the-art in integrated circuit technology.

The polymer insulating film is formed at a rate which permits thickness control to close tolerances. More experience will be needed before questions of uniformity and yield can be posed and answered. At present no problems have appeared which suggest any difficulty. Since tunneling current density is an exponential function of the electric field, this is a very sensitive method to scale the current level of the device. Transducer action will depend upon the volume or thickness of the dielectric film, so it is expected there must be some compromising done here by the designer.

The field plate work function is a very sensitive parameter in determining current levels. Wilmsen (15) shows the peak value of conductance is a linear function of the difference in metal and semiconductor work function. Some technological problems may arise in depositing the various metals because of the high temperatures needed to evaporate them. The work function can be adjusted, however, by depositing two or more metals simultaneously. This technique is not yet worked out in sufficient detail to predict the effect on the current and voltage characteristics. The number of pure metals which can be used to achieve different work functions without causing fabrication problems appears to be adequate for now.

The semiconductor substrate is the most complex material in the device, giving the designer opportunities as well as problems. Due to the low conductance of the tunneling process, semiconductor doping levels will determine the current level largely through the effect on the Fermi level. The amount of information available

on this phase of the program is very large but not yet fully analysed.

The finished device will be characterized by its high internal resistance, of the order of ten megohms. The range could be several decades on either side. This will mea- it would be operated as a digital current source. The equivalent circuits and circuit sysbols to be used will reflect this basic property. In applying tunneling digital devices, their compatibility as current sources in integrated circuits is considered to be an advantage.

Configurations for a three-step A-D converter must incorporate a feature to set the daturation current at three different and definite values. The parameters mentioned above can be used separately or in combination. In the examples discussed below the devices are assumed to operate at constant and uniform temperature. The analog quantity is voltage and the digital quantity is current.

a. Constant Thickness Configuration

A common substrate of (N-type) silicon is coated with a uniform film of dielectric. Field plates of metals with different work functions are deposited. The areas are determined to give the desired current scale. They are connected in parallel to form the output current terminal. An ohmic connection on the reverse face of the silicon wafer is the second terminal.

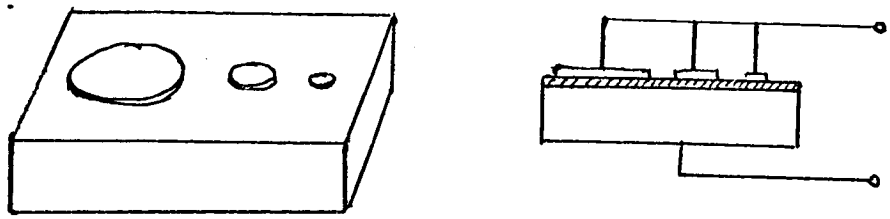


Figure 19

b. Stairstep Configuration

By forming the dielectric film in a different thickness for each element a different behavior is expected. The point at which the tunneling current saturates is dependent upon the maximum charge collected in the surface states. The field in the insulator also saturates, so the value of the saturation current should be nearly independent of the dielectric film thickness. With identical field plates the characteristics would look like the figure.

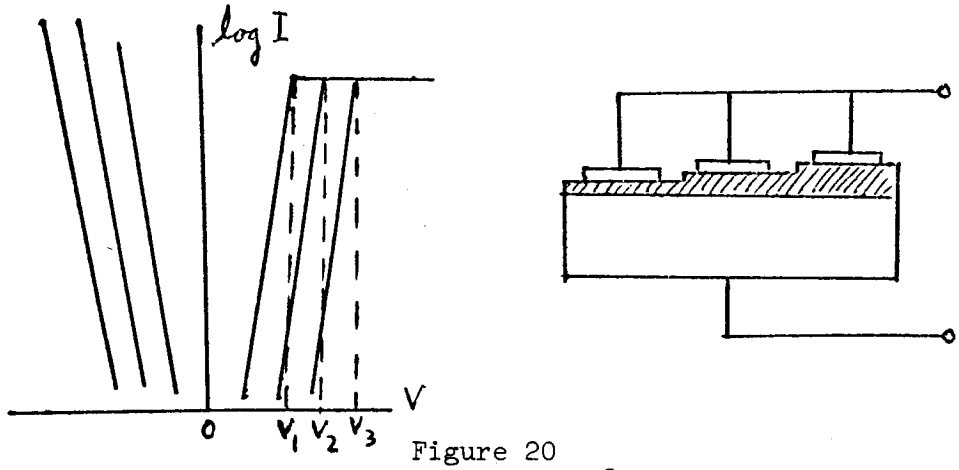


Figure 20

This configuration may prove difficult to build, but has the advantage of producing uniform current steps. Since the field is proportional to the thickness of the insulator, the device will saturate from left to right with an increase in the external voltage. The resolution of the device depends on the number of stages included. The technology of this "pyramiding" of insula-

tion most likely would make this device difficult to build.

c. Isolated Devices with Different Biases

Construct several separate MIS devices, i.e. several units, each with its own Si substrate, insulator and field plate. All the units are of identical construction and similar electrical properties. The units are ganged together by an external bias network. The number of units and the construction of the external network determine the resolution and range of the device.

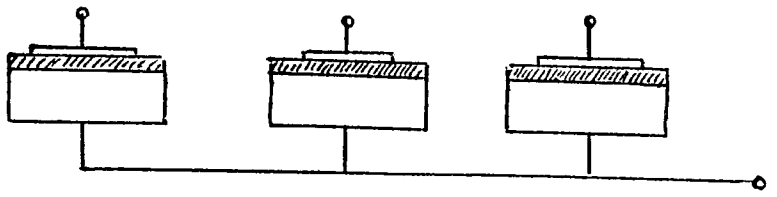


Figure 21

d. Isolated Devices on Common Substrate with Different Biases

This device would be an improvement on (c). A single substrate will hold a uniform polymer film. Several field plates of the same metal are deposited on the surface of the insulator. These elements are then ganged together by an external bias network as in (c). This particular configuration is appealing due to its simple construction, size and ultimately, the ability to build the external network into the device through thin film component deposition techniques.

The construction of a device like (4) will determine whether the depletion layer remains localized below the metal field plate or spreads in the "oil spot" fashion. If the latter is the case it may be contained by etching grooves between units

to reduce lateral current, by wide interspacing of the field plates on the substrate or by other methods.

2. PRELIMINARY ANALYSIS

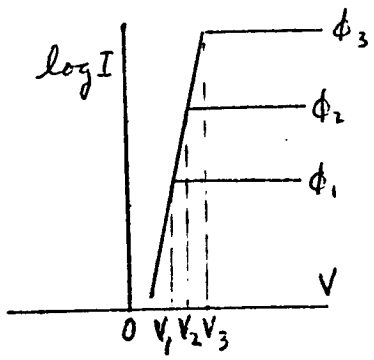


Figure 22

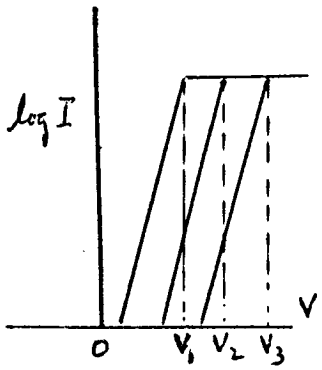


Figure 23

The low frequency analysis of a tunneling A-D converter is a straight forward graphical procedure. We simplify the preliminary analysis by selecting an example which is conceptually possible with either a device using three work-functions with constant thickness or three thicknesses with constant work function. The linearized characteristics each give three saturation voltages.

These devices connected in parallel would display a step response in current as shown by the diagrams below.

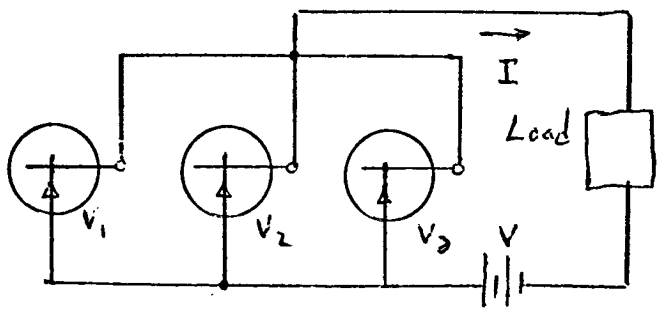


Figure 24

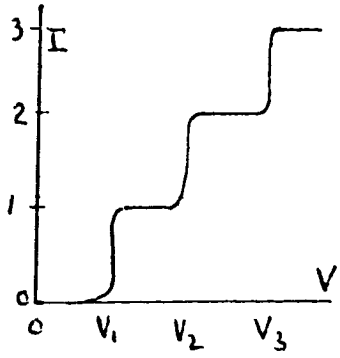


Figure 25

Attention is called to the change in current scale, which would be the reason the steps of current on the linear I-V characteristic

appear to break more sharply.

The tunneling device has a high internal impedance so the load would be a device which is suited to a current input, such as a bipolar transistor.

While much more remains to be done in this area, the results of the analysis so far have been encouraging.

IV. B. Voltage and Frequency Dependence of Metal-Polymer-Silicon Thin Film Capacitors

The technique for studying the silicon-silicon oxide interface with differential capacitance vs. dc bias data has been extensively utilized (16). The band structure of the silicon at this interface is effected by the oxygen present in the oxide. If the oxide is replaced by a chemically inert dielectric, then the MOS technique should reveal information more directly related to the undisturbed silicon surface. If a suitable dielectric could be found, the MOS technique could be extended to other semiconductors and serve as a method of studying semiconductor surface preparation. One dielectric which holds promise of fulfilling these goals is a thin polymer film as reported by R. W. Christy (8) and H. T. Mann(9).

This paper discusses some of the properties that these polymer films have been found to possess and presents some differential capacitance vs. dc bias data taken on aluminum-polymer-silicon samples. The silicon was 60 ohm-cm n-type; the same as used in the MOS studies presented by J. R. Yeargan (17) of this laboratory. It was chosen in order that a comparison with his data could be made. The results of these are not conclusive, but indicate that it is feasible to utilize the polymer film in semiconductor surface studies.

The polymer film is formed by introducing a partial pressure of diffusion pump oil into a vacuum containing the silicon or other substrate. The oil molecules are adsorbed on the substrate and are broken up into free radicals by a beam of low energy electrons, Fig. (26). The free radicals then recombine into long interweaving

chains to form a solid (18,19). The polymer film strongly adheres to the glass and silicon substrates used in this study. It is thought that the film either forms a bond with the surface layer of adsorbed molecules or that the process is self cleaning since the electron beam will break the bonds between radical of most adsorbed organic molecules.

The properties of the polymer film were determined by forming metal-polymer-metal capacitors on optically flat glass substrates. A base strip of aluminum is first vapor deposited on the glass. Then a polymer film was formed over part of the strip. A cross strip of aluminum was then deposited as shown in Fig. (27). The dielectric constant was determined by measuring the area, capacitance and thickness of polymer film between the two aluminum strips. The thickness of the films were measured with an interferometer using a sodium lamp. The thickness measurement introduced error into the dielectric constant determination; therefore capacitors with film thicknesses ranging from 1000 to 4000 Å were constructed and the capacitance per unit area plotted against reciprocal film thickness as shown in Fig. (28). From this plot the dielectric constant was found to be 2.8 which is independent of voltage and only slightly dependent upon frequency and temperature. The field strength of the films was found to be in excess of 5×10^6 volts/cm.

One of the most important properties of a thin dielectric is continuity. Since the polymer film is formed slowly, it should be more uniform and continuous than vapor deposited dielectrics such SiO_x. To determine if the polymer film contains any gross defects or pin holes, capacitors with polymer thicknesses of 67 to 200 Å were constructed and the variation of current with applied voltage was analyzed. The current as shown in Fig. (29) was found

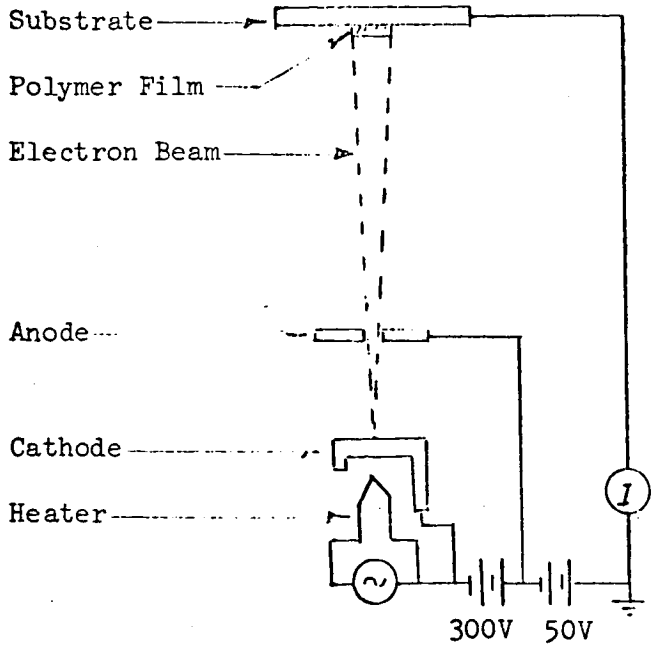


Fig.26 Electron Gun Used to Form Polymer Film

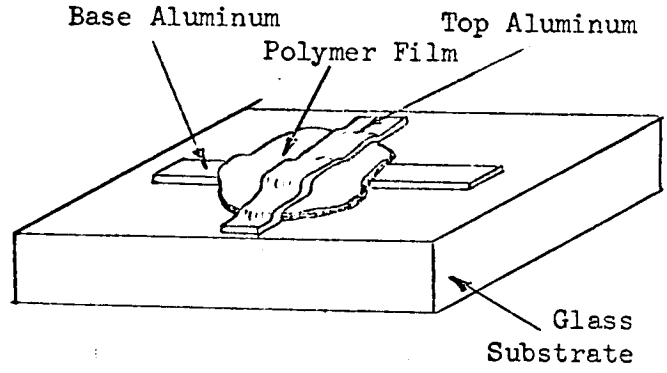


Fig. 27

Metal-Polymer-Metal Capacitor

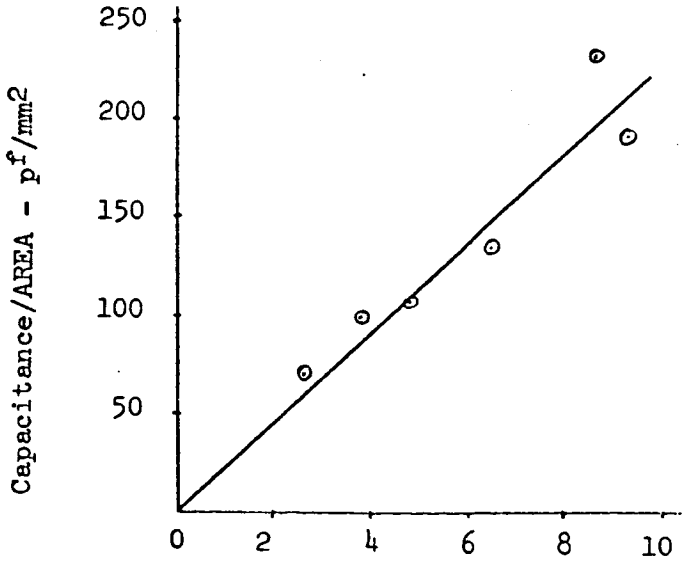


Fig. 28 Determination of Polymer Dielectric Constant

to increase exponentially with voltage which is characteristic of tunneling current. This indicates that ohmic currents which would flow through any pin holes in the film are small. An electron microscope picture of one of the films shows that a few pin holes do exist but their size and number are small.

Metal-Polymer-Silicon Capacitor

To investigate the MOS technique with the polymer film termed MPS, a film of the polymer was formed on 60 ohm-cm n-type silicon wafers which had been lapped, etched with CP-4, and boiled in trichloraethylene and concentrated nitric acid. An aluminum dot was deposited on the polymer film to serve as the metal electrode in the MPS structure. To prevent mechanical disturbance of the polymer film under the aluminum dot, a ball of indium-gallium paste was placed on the dot and a probe point dipped into the paste as shown in Fig. (30). The capacity measurements could then be made. The capacity vs. dc bias curves on the MPS structure have been found to be of two types. The first type is shown in Fig. (31). The curves indicate a slight p shift in the surface potential which is considerably different from the strong n shift which is found with a grown oxide dielectric. This is not surprising considering the differences in the polymer and the SiO_2 dielectrics. Other researchers have reported changes in the surface potential when the ambient is changed. Buck and McKinn (20) using a surface conductivity technique found that the surface of silicon is quite sensitive to surface preparation. They found widely different surface potentials after soaking the silicon in either sodium dichromate, boiling

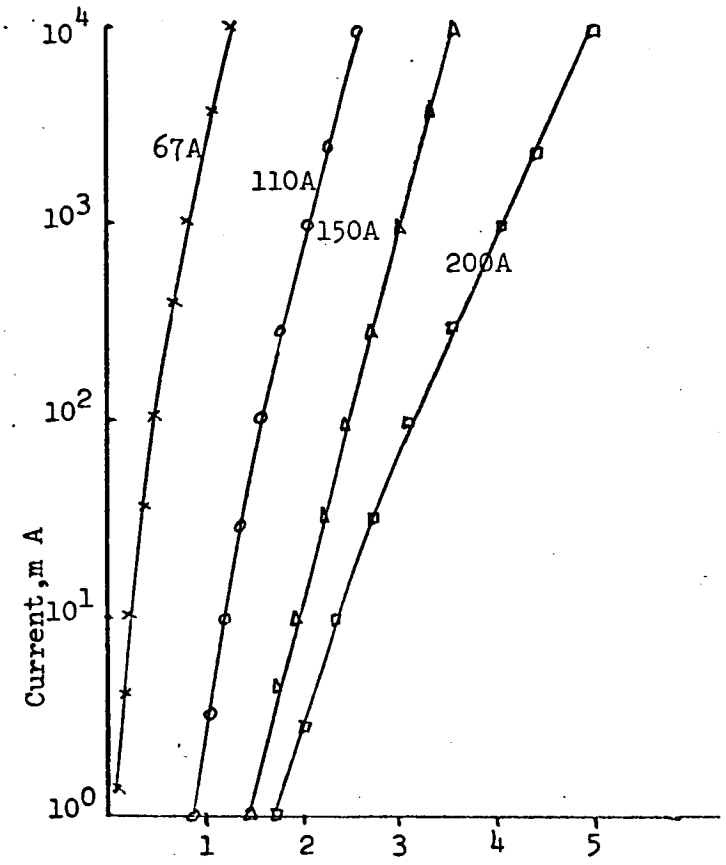


Fig. 29 Applied Voltage

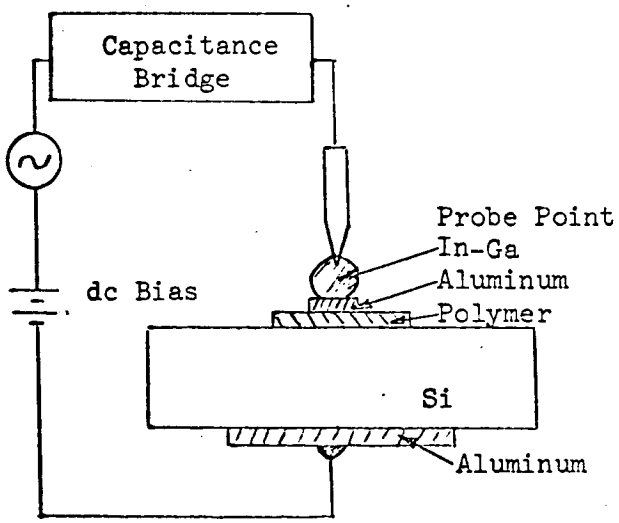
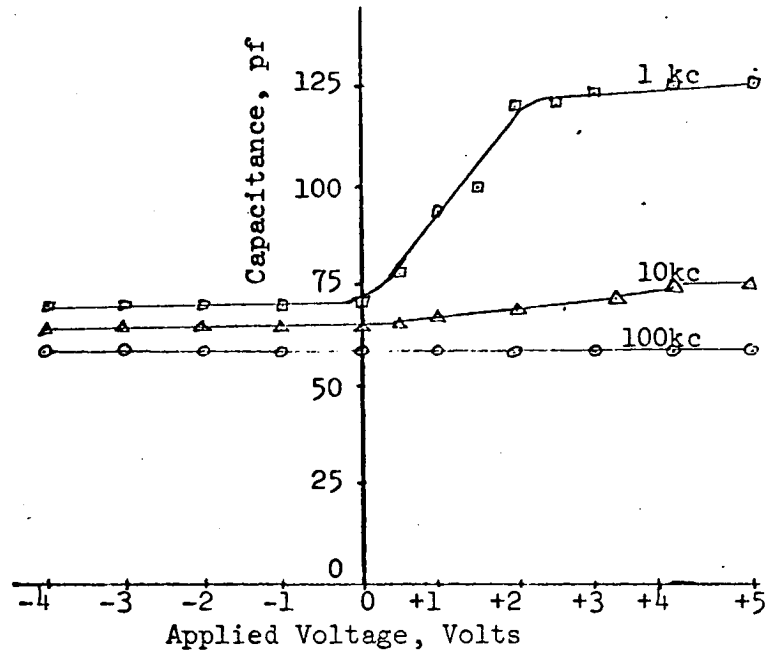
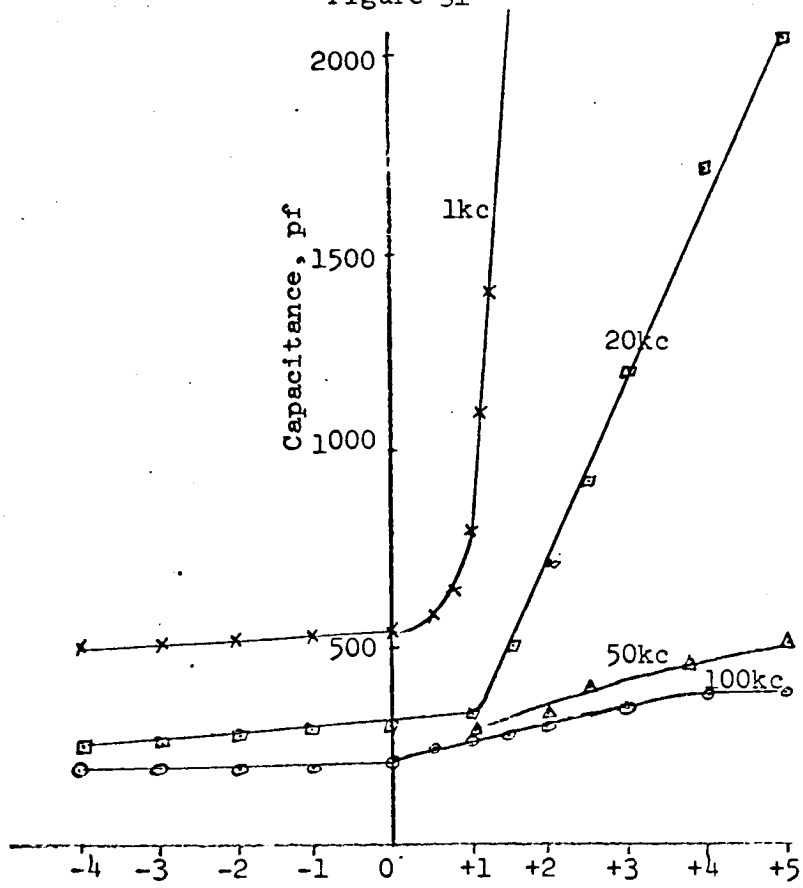


Fig. 30 Metal-Polymer-Semiconductor (MPS) Construction



Variation of Capacitance with Voltage, Type I
Figure 31

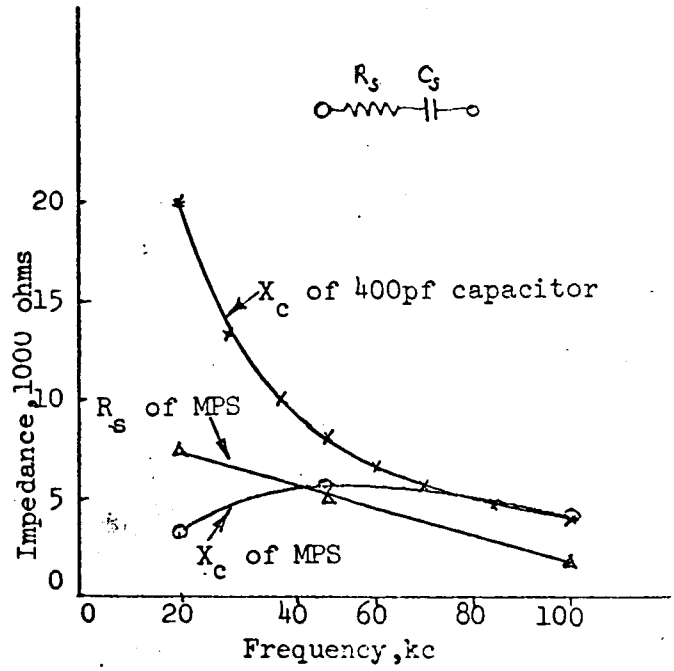


Variation of Capacitance with Voltage, Type I
Figure 32

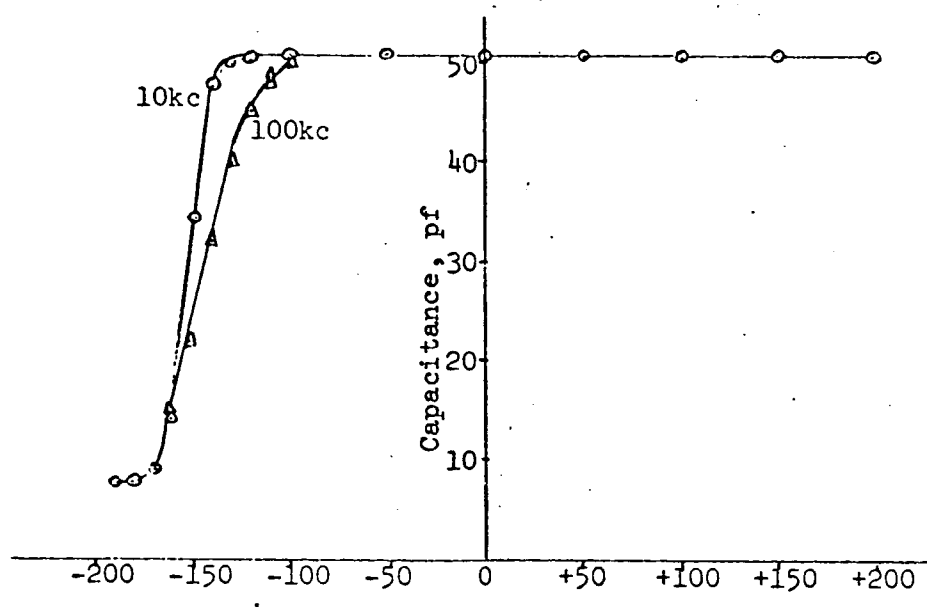
deionized water, HF or 10/1 - HNO_3/HF.

Moore and Nelson (21) also found that adsorbed films of sodium dichromate produced changes in the surface potential. The curves in Fig. (32) show a strong dependence of capacitance upon frequency. This frequency dependence is even stronger at liquid nitrogen temperature. If the capacitive reactance is calculated at a positive voltage of 6 volts, it is found that the capacitive reactance is nearly constant with frequency as shown in Fig. (33). The reactance of a 400 pf capacitor is also plotted on the graph for comparison. This frequency independence could be utilized in some interesting new types of filters. Series capacitance and resistance were measured with a GR1615A capacitance bridge. The series resistance decreased with frequency and the resulting impedance over the narrow frequency range shown in Fig. (33) is $Z_{eq} \simeq R_o/\omega - jR$. Several other samples had similar frequency dependence.

The second type of capacitance vs. dc bias curve on MPS structures that has been observed is shown in Fig. (34) and indicates a strong n shift in the surface potential. These curves are more typical of the Si-SiO_2 structure. The Type II curves do not have strong frequency dependence as do the Type I. The change in the surface states at zero surface potential varied between 2×10^{12} and 6×10^{12} cm^{-2} for the different samples. This is only slightly higher than the 0.5×10^{12} to 1×10^{12} cm^{-2} surface states change reported by Yeargan (17) for grown oxides.



Frequency Dependance of MPS, Type I
Figure 33



Capacitance vs dc Bias, Type II
Figure 34

IV. C. Surface States, Trapping and MOS Capacitance

1. Introduction

The discussion in the preceding section is the results of an experimental investigation on the circuit properties. The extraordinary behavior of MOS capacitors leads them to have an unexpected and very useful role in digital transducer systems. The explanation of the frequency dependence is not yet available, but a reasonable start has been made.

The "dangling bonds" appearing at the silicon oxide-silicon interface will serve as "trapping centers" which have the tendency to catch the electrons or make the moving electrons immobilized. The residing charges and the associated surface potential will affect the MOS capacitance in the following extent: a) Let C = total capacitance per unit area of the MOS structure, Q_{ss} and Q_{sc} are charges per unit area residing in surface states and silicon respectively, V = bias voltage, ψ_s = surface potential then,

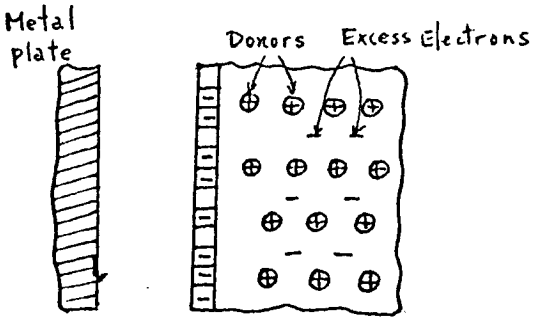
$$C = \frac{d(Q_{ss} + Q_{sc})}{dV} = C_{ox}\left(1 - \frac{d\psi_s}{dV}\right). \qquad 24$$

From the above equation we can see that the capacitance is completely determined by the ability of the surface potential to follow the applied voltage or is a function of bias voltage. b) Associating with the charging and discharging process of those surface states we can define a time constant τ. For low frequencies ($\omega\tau<<1$) the surface states are able to give up and accept charge in response to applied signal. The toal capacitance of the device is the surface-state capacitance in parallel with the depletion capacitance. For high frequencies ($\omega\tau>>1$) the time constant is too long to permit

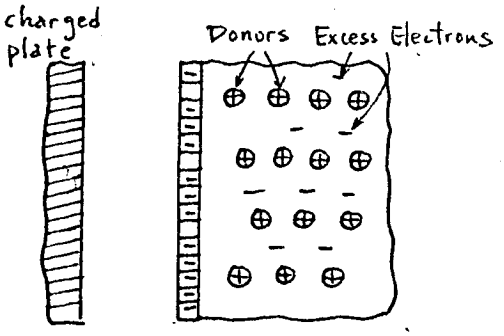
charge to move in and out of the states in response to an applied signal. The total capacitance is the oxide and depletion capacitances in series. Therefore, generally the capacitance of the MOS device will decrease as the frequency increases. Physically, we can explain that the increase in capacitance is due to the fact that surface states act as a source of charge are located closer to the metal layer than the charge in the depletion region. The second effect serves a main reason to explain the frequency independent phenomenon of MPS structure. Other considerations which may affect the value of capacitance will be mentioned in the discussion of this report.

2. BARDEEN'S THEORY OF SURFACE STATES

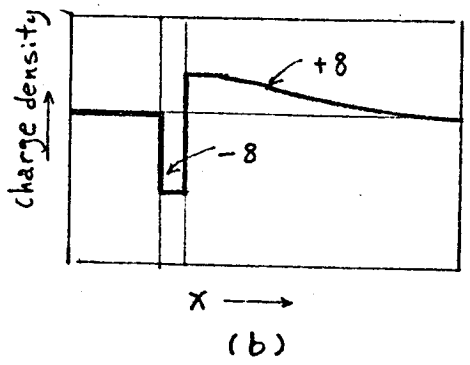
The theory of surface states was first proposed by J. Bardeen [22]. According to Bardeen's theory, the binding structure of semiconductor at the surface is different from the bulk. In the bulk of silicon or germanium crystals the four valence electrons of an atom share the electrons of the neighboring atoms and form the covalent bands which bind the crystal together. Yet, the atoms at the surface, where the crystal structure ends, will have some unused valences or "dangling bonds." These unused valences have a tendency to "catch" electrons which may pass by it in order to form a complete covalent bond. The energy states introduced by these unused valences electrons are the surface states and the tendency to catch an electron is so called "trapping." Thus, trapping can make electrons which move in the body of the semi-conductor immobilized. Fig. 35 shows Bardeen's theory of the Role of Surface States in Trapping Induced Charge. In part a) eight electrons were shown being trapped in the surface states. Note that an accumulation of layer of electrons was formed below the surface. This layer induces an equal amount of positive charge (the space-charge layer) inside of the semi-conductor so that there is an over all charge neutrality. In parts b) and c) the charge density and energy distribution diagram were shown. When

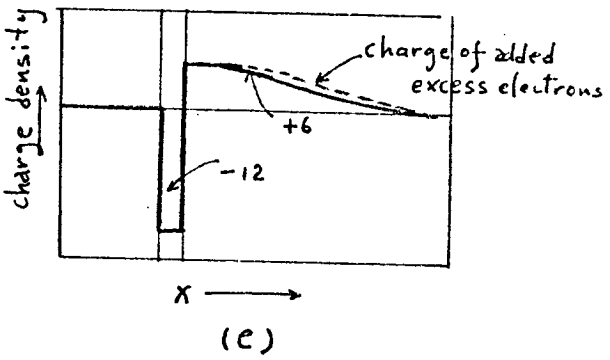


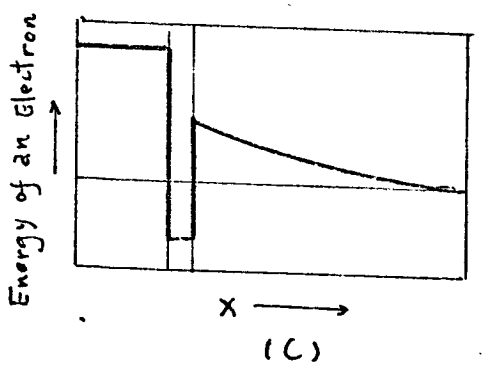
Distribution of charge
(a)

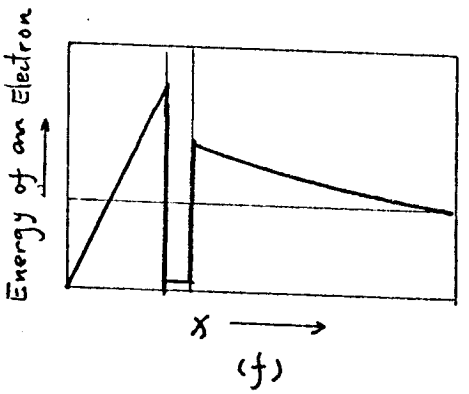


Charges induced at surface
(d)









Distance into semi conductor

Distance into semi conductor

Fig.35 Surface States Diagram, showing Bardeen's Theory of the Role of Surface States in Immobilizing Induced Charge.

the metal plate is charged positively, more electrons, coming from the bulk of semi-conductor through the charging circuit will be trapped by the surface states. In part d) we can see four of these electrons go into the surface states. Parts e) and f) are charge density and energy distribution diagrams for the modified system.

3. SURFACE-STATE DISTRIBUTION

The surface state can only exist in certain energy levels (or regions). Figure 2 shows the surface state distribution observed for n- and p-type surface [23]. It can be noted that the surface states observed on n-type material are quite different from those of p-type material. This suggests that the background of doping is playing a significant role in determining the nature of the surface states.

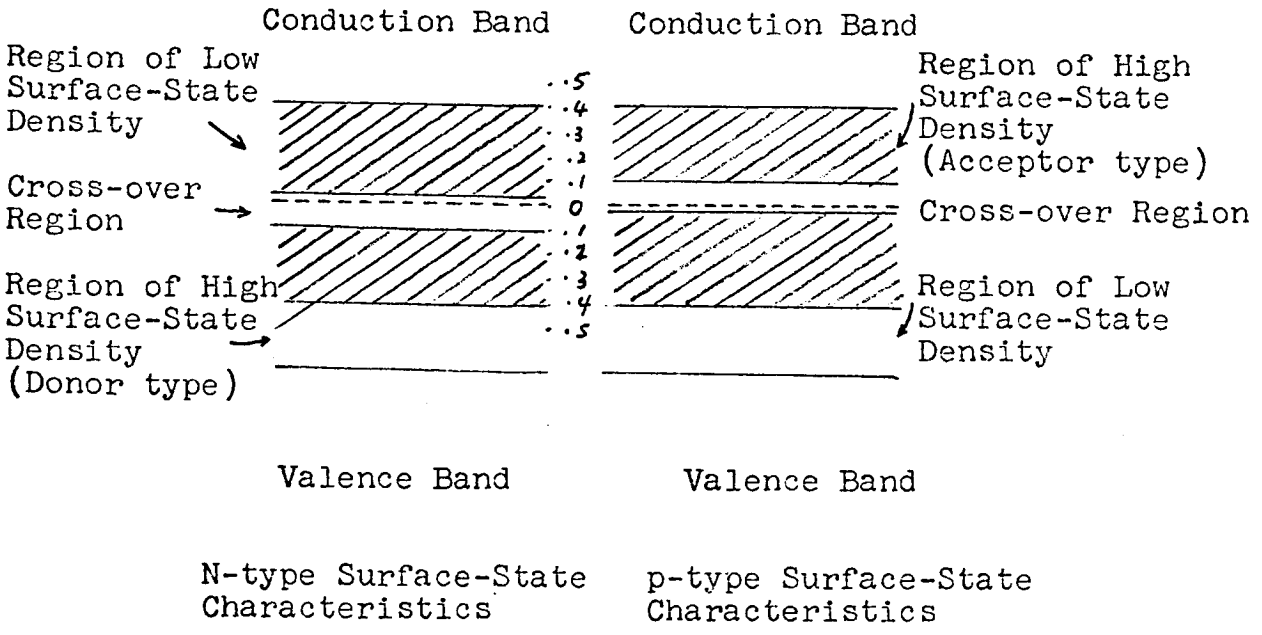


Fig. 36 Surface-State Distribution

From Fig. 36 we can see "the n-type surfaces exhibited donor levels lying in the range of $\sim$ 0.15 to $\sim$ 0.45

above the valence band; their density was found to vary from $\sim 5 \times 10^{12}$ to $\sim 5 \times 10^{13}$ states/cm^2/eV . The p-type surfaces exhibited acceptor levels lying $\sim$ 0.15 to $\sim$ 0.45 eV below the conduction band; their density was comparable with those observed on n-type surfaces."

4. OXIDIZED SURFACE

It has been found that the surface states are of great importance in determining the reliability of semiconductor devices [24]. The idea of using insulators on the surface was generated with two major reasons: a) to study the surface phenomena, b) to control the surface conditions--this also means to control the stability and reliability of semiconductor devices.

A fundamental approach is the growth of an oxide (insulator) over the semiconductor surface. Lindmayer and Wrigley have listed three advantages of this oxidized surface and explained why it has been widely used. Since it is not related to the main purpose of this report the author will not discuss those advantages. Although the growth of dioxide over the semi-conductor surface is a pretty involved problem; for example, there are directions of motions of donors and acceptors and also there is disturbance of the interface due to the potential difference between two dissimilar materials. Yet, the author does want to point out that the surface states or traps still exist in the oxide or interface. This is also the reason why the author can tie together the surface states, trapping and MOS capacitance in a single report.

The following figure will show the energy diagram of an oxidized, intrinsic silicon crystal.

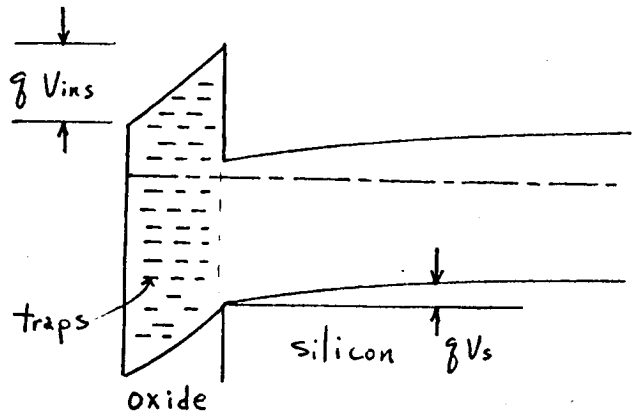


Fig. 37. An Interface Between A Polycrystalline Oxide and A Semiconductor Crystal.

It is worth noting here that the MOS structures which will be discussed later all refer to a growth of oxide on the surface of N-type silicon crystal.

5. STATISTICS OF RECOMBINATION OF HOLES AND ELECTRONS

Bardeen's surface states theory emphasized the trapping as electron capture of surface states. Shockley and Read showed that electron emission, hole capture as well as hole emission were also basic processes involved in recombination by trapping [25]. The following Figure shows the way in which holes and electrons may be recombined through the traps.

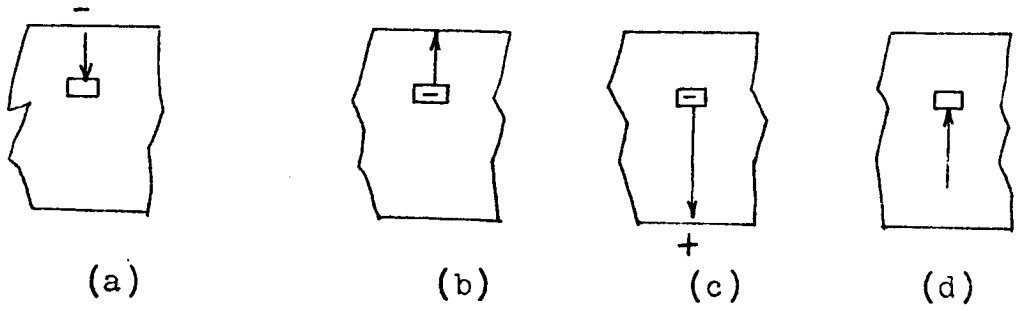


Fig.38. The basic processes involved in recombination by trapping; (a) electron capture, (b) electron emission, (c) hole capture, (d) hole emission.

The basic formulas associated with the above process also had been derived by Shockley and Read.

a) Electron capture process.

It can be easily understood that such factors as the probability that a trap is empty, the number of trapping centers per unit volume, the probability of available electrons passing by a trap, etc., will surely affect the rate of electron capturing.

Let N_t = the number of trapping centers per unit volume

f_{pt} = the probability that a trap is empty

$N(E)dE$ = total quantum states per unit volume in the energy range dE.

$f(E)$ = the probability that a state of energy E being occupied.

v = the speed of the electron

A = the cross section for capture by a trap

Then $C_n(E)$ = average of

= the average probability per unit time that an electron in the range dE be captured by an empty trap.

Then, the rate of capture will be

$$f_{pt} N_t C_n(E) f(E) N(E) dE.$$

b) Electron emission process.

Let f_p = the probability that a state is empty

f_t = fraction of traps occupied by electrons

e_n = emission constant corresponding to

=

E_t = effective energy level of traps

$= E_t(true) + KT \ln(\omega_p/\omega)$

where ω_p and ω are the degeneracies of an empty and full trap respectively.

Then, the probability that an electron been emitted from the trap is

$$f_t N_t e_n f_p(E) N(E) dE.$$

The net rate of capture (that is capture minus emission) for the energy interval dE is

$$d U_{cn} = [f_{pt} f(E) - (e_n/c_n) f_t f_p(E)] N_t C_n(E) N(E) dE . \quad 25$$

The total rate of electron captured is

$$U_{cn} = [1 - \exp\{(F_t - F_n)/KT\}] f_{pt} N_t \times \int_{E_c}^{\infty} f(E) N(E) C_n(E) dE . \quad 26$$

where E_c is the bottom of conduction band.

An entirely similar expression may be derived for U_{cp}, the net rate of hole capture.

Applying the above principles Shockley and Read showed that for the nondegenerate semi-conductors

$$U_{cn} = G_n f_{pt} n - G'_n f_t n_1 \quad 27$$

where $G'_n = N_t \langle C_n \rangle$

n = density of electrons in conduction band

N_c = effective density of levels for conduction band

$$n_1 = N_c \cdot \exp(E_t - E_c)/KT \quad 28$$

similarly

$$U_{cp} = G'_p f_t p - G'_p f_{pt} p_1 . \quad 29$$

6. CAPTURE CROSS-SECTION ESTIMATE

From the Shockley and Read statistics previously discussed we understood the capture cross section of a trap A, played an important role in determining the rate of capture (or recombination) of electrons and holes. Laurence L. Rosier showed that this capture cross section A could be expressed as

$$A = \frac{2 n_i S_{max}(N)}{V_t n_o \int_{V_1}^{U_2} \frac{(-\frac{dN_{ss}}{dY}) dV}{\sqrt{\Delta p/p_o + \cosh V}}} \qquad [30]$$

where n_i = intrinsic carrier density

Y = surface potential relative to the bulk in units of

N_{ss} = surface state density

V_t = thermal velocity of electrons and holes.

S_{max} = max. surface recombination velocity.

n_o = bulk doping in the n-type epitaxial layer, cm^{-3}.

p_o = the equilibrium hole concentration in the bulk of semiconductor

Δ_p = the injected carrier density in the bulk of the semiconductor.

By a $C-V$ measurement technique Rosier found out $S_{max} = 4.3 \times 10^3 \, cm/s$ and the capture cross section had been estimated $\sim 4 \times 10^{-17} \, cm^2$.

Instead of using C-V measurement technique Heiman and Warfield, by a quantum mechanical theory approach, proved that the effective capture cross section of an oxide trap viewed by a carrier at the semiconductor surface is a function of location of the trap from the interface [26].

From the equation derived by Heiman and Warfield,

$$A(x) = A_o e^{-2K_o x} \qquad 31$$

where A_o = the capture cross section of a trap at $x = 0$.

K_o = reciprocal of penetration depth of the electron

We understand the capture cross section of a trap located a distance x from the interface into the oxide is reduced by the factor $e^{-2K_o x}$.

7. A PSEUDO-FERMI FUNCTION AND FIELD DEPENDENCE OF SURFACE STATE DENSITY

A so-called pseudo-Fermi function in the variable was derived by Heiman and Warfield. This equation gives the probability that a trap will be filled in a measurement time, Tm. The following is the equation,

$$f_t(x, E_t) = N_t f(E) g(x, E_t) \qquad 32$$

where $f_t(x, E_t)$ = the probability that a trap will be filled or the average fraction of traps occupied by electrons.

N_t = the number of trapping centers per unit Volume or the number of available (empty) traps.

$f(E)$ = Fermi Function

E_t = effective energy level of traps

$$g(x, E_t) = 1 - \exp\left[-e^{-2K_0(x - x_m)}\right] \qquad 33$$

x_m = a distance from the interface associated with measurement time, Tm.

$$= \frac{1}{2K_0} \ln\left[T_m A \langle v \rangle (n_s + p_1)\right] \qquad 34$$

$\langle v \rangle$ = average thermal velocity of the electron

n_s = the electron density at the surface

$$p_1 = N_v e^{-\beta(E_t - E_{v0})}$$

E_{v0} = top of valence band at $x = 0$

$$\beta = (KT)^{-1}$$

Heiman and Warfield also showed that the density of surface states depends upon the electric field E_{ox} in the oxide.

$$\mathcal{N}_{ss} = \frac{N_t}{e\,E_{ox}} \qquad 35$$

where E_{ox} = electric field in the oxide and will be discussed later in this report.

8. CAPACITANCE OF AN MOS STRUCTURE

After we have investigated the surface states and trapping associated with the MOS structure we will be able to discuss the frequency and bias voltage dependence characteristics of the MOS capacitor. Before proceeding with the details of the discussion the student would like to introduce two equations derived by Heiman and Warfield [26]. These two equations will give us a general idea about the MOS capacitance.

$$C = \frac{dQ_{tot}}{dV} = \frac{d(Q_{ss}+Q_{sc})}{dV} = C_{ox}\left(1 - \frac{d\psi_s}{dV}\right) \qquad (1) \quad 36$$

$$\frac{dV_{ss}}{d\psi_s} = \left(\frac{e}{C_{ox}}\right)\frac{dN_{ss}}{d\psi_s} \qquad \text{----------} \quad (2) \quad 37$$

where Q_{ss} is the charges per unit area residing in surface states or charges been trapped by the oxide traps.

Q_{sc} = the charge per unit area in the silicon.

C = total capacitance per unit area of the MOS structure.

V = applied bias voltage across the structure.

ψ_s = surface potential it depends upon the charge surface distribution.

N_{ss} = the total number of filled traps per unit surface area.

Cox = the oxide capacitance per unit area.

Vss = voltage equivalents of Qss is a function of ψs and V. From first equation we see that the capacitance is completely determined by the ability of the surface potential to follow the applied voltage, or is a function of bias voltage. Since the quantity dVss/d s will depend on frequency, then Cox as well as C all become frequency dependent. Although it is impossible to eliminate the surface states at the silicon silicon-oxide interface, it will be easeir to understand the effect of surface states on the MOS capacitance by first assuming that there are no surface states existing between the $Si-SiO_2$ interface. The development will follow L.M. Terman (27) to establish the capacitance and its equivalent circuits with and without surface states involving.

a. Surface States Absent

An energy levels diagram between the metal, silicon oxide and silicon with zero bias voltage can be shown as follows (we also assume the work function of the silicon, $\emptyset s$ is larger than the work function of metal, $\emptyset m$).

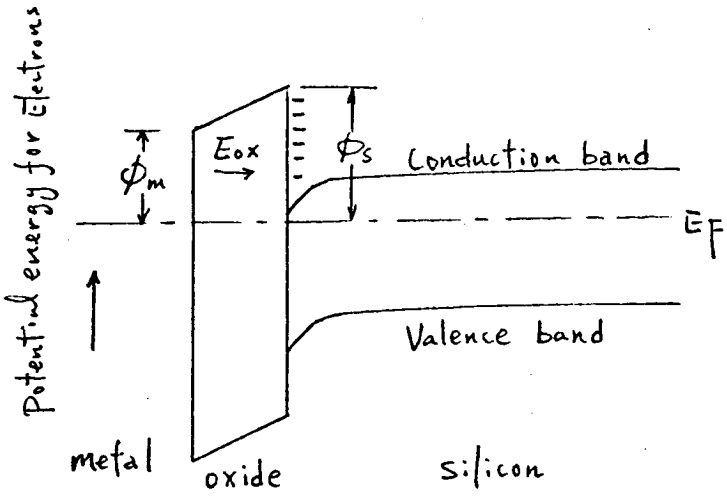


Fig. 39 Energy-band picture of MOS capacitance, for $\phi_s > \phi_m$, zero applied voltage.

As mentioned before, the thermal oxide on ordinary silicon produced sufficient donors at the silicon, silicon-oxide interface to make the surface n -type. Thus an accumulation of negative charge in the silicon at the interface appears. As a result, a field, E_{ox}, must exist in the oxide which terminates on this negative charge.

From the above diagram it also can be easily understood that the total differential capacitance of the MOS device will consist of two capacitances in series; that of the oxide layer, and that of the silicon surface. The oxide capacitance may be determined solely from geometry, and is given by

$$C_{ox} = \frac{\epsilon_{ox}}{W_{ox}}$$

where ϵ_{ox} is the dielectric constant of silicon oxide and W_{ox} is the thickness of the silicon oxide. The

capacitance of the silicon surface depends upon the distribution of net charge at the silicon surface as a function of the voltage drop across the silicon. It can be calculated from the expression,

$$C_D = \frac{dQ_{net}}{dV_s}$$

where Q_{net} is the net excess charge at the silicon surface and V_s is the voltage drop across the silicon.

At room temperature and by assuming a) all impurity atoms are ionized everywhere b) the silicon is not degenerate Garrett and Brattain had found,

$$C_D = \sqrt{\frac{q\epsilon_s n_i \beta}{2}} \frac{\exp(\beta\Delta\psi) - 1}{[\exp(\beta\Delta\psi) - \beta\Delta\psi - 1]^{1/2}} \qquad [38]$$

where $\beta = \frac{q}{kT}$

n_i = the electron concentration in the silicon at room temperature.

$\Delta\psi$ = the potential drop across the silicon.

b. Effect of surface states.

The existence of surface states complicates the theory for the MOS capacitance. The space-charge densities and displacement current distributions appear as in Fig. 40.

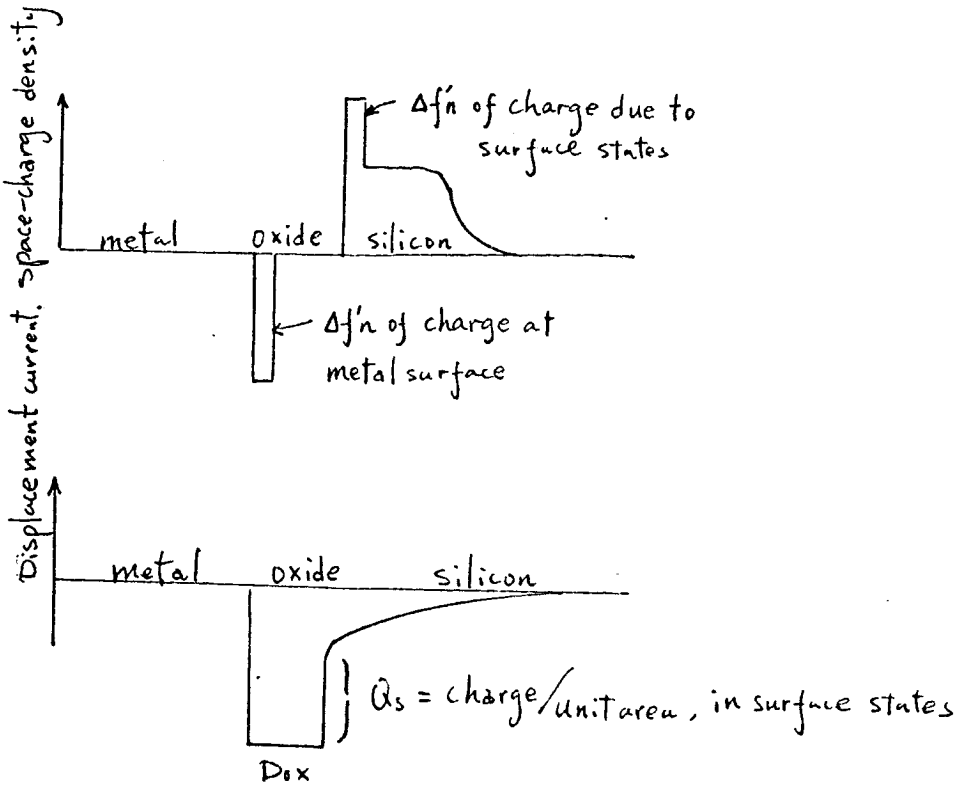


Fig. 40 Space-change density and displacement current displacement current distributions for the MOS capacitor.

With charging and discharging those states a time constant τ can be defined. Let $Q_{s(t)}$ as the charge in the surface states at time t. and $Q_{so(t)}$ as the charge that would be in the states at time t if equilibrium conditions were reached then the time constant is defined as

$$\frac{dQ_s}{dt} = \frac{Q_{s(t)} - Q_{so(t)}}{\tau} \qquad 39$$

Note, if the surface potential of the silicon varies with time, then Q_{so} will also be a function of time.

When the potential at the surface of the silicon is disturbed, the total charging current to the surface of the silicon will be the sum of the current which charges the depletion region in the silicon, and the current which

charges the surface states. Thus

$$C_{total} = \left.\frac{dQ}{dV_s}\right|_{silicon} + \left.\frac{dQ_s}{dV_s}\right|_{states}$$

The admittance of the first term is just the admittance of the capacitance of the depletion region which has been calculated previously. The admittance of second term can be obtained by making the usual small-signal approximations for quantities varying sinusoidally in time. After doing this, Terman derived the admittance per unit area of the whole MOS device would be

$$Y = jw \Big/ \left\{ \frac{w_{ox}}{\epsilon_{ox}} + \left[C_D + \left|\frac{dQ_s}{dV_s}\right| \frac{1}{1+jw\tau} \right]^{-1} \right\} \qquad 40$$

The equivalent circuit corresponding to the above equation is given in Fig. 7.

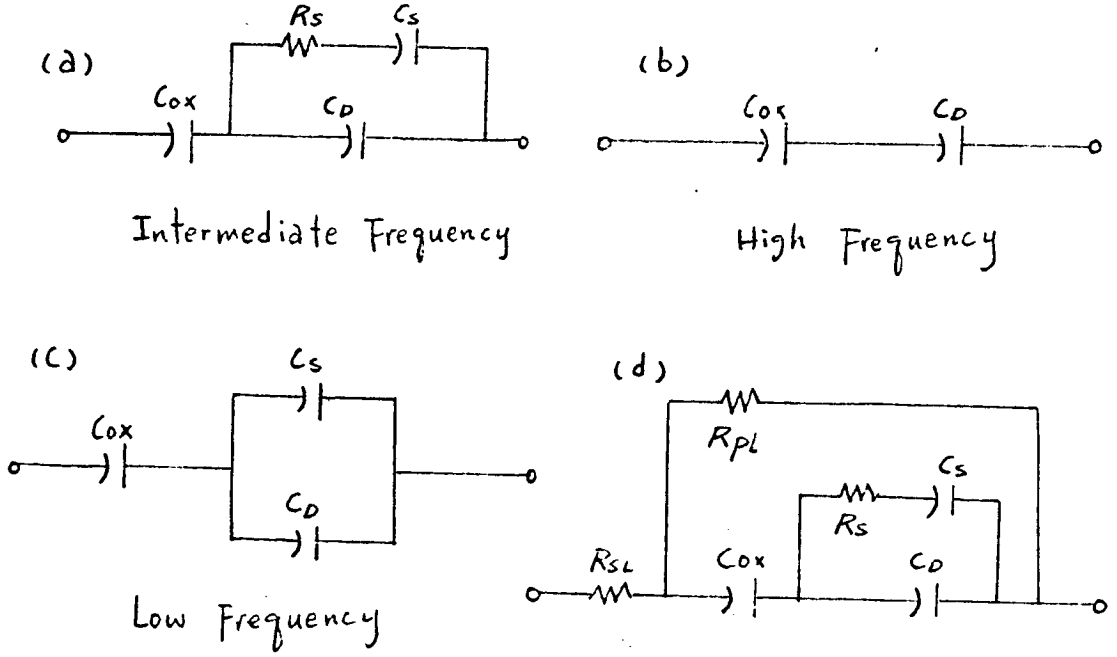


Fig. 41. Equivalent circuits for the MOS Capacitor.

In Fig. 41 (b) it shows the high frequencies ($\omega\tau >> 1$) equivalent circuit it is just the oxide and depletion capacitances in series. This happens when the time constant is too long to permit charge to move in and out of the states in response to an applied signal. The small signal equivalent circuit will be one as if there were no surface states present. Fig. 41 (c) shows the low frequencies ($\omega\tau << 1$) equivalent circuit. Here all the surface states are able to give up and accept charge in response to the applied signal. The total capacitance of the device is increased as the surface-state capacitance is in parallel with the depletion capacitance. At intermediate frequencies ($\omega\tau \approx 1$) part of the surface state charge will contribute to a small-signal measurement, and the observed value of capacitance will lay between the low and high frequency values. Therefore, in general at a given applied voltage the capacitance will decrease as the frequency increases. Physically, we can explain that the increase in capacitance is due to the fact that surface states acting as source of charges which are located closer to the metal layer than the charge in the depletion region.

The equivalent circuit of Fig. 41 (a) corresponds to the ideal device. An equivalent circuit which includes the effect of series losses in the bulk resistivity of the silicon and the d.c. leakage through the oxide and depletion region is shown in Fig. 41 (d).

The depletion capacitance, C_D will vary directly with bias voltage. The resistance and capacitance due to surface states may vary indirectly in the following way. Consider Fig.42; at room temperature for a good approximation we can assume that all the states above the Fermi level will be empty; all those below will be occupied. Defined as shown in Fig. 42. Then for a small signal measurement only those states at the neighborhood of $E_{F(S)}$ will be affected by the applied signal and will hence contribute to the values of R_S and C_S measured. By varying the bias it will shift the value of $E_{F(S)}$ and then, affect the distribution of surface states and their time constants.

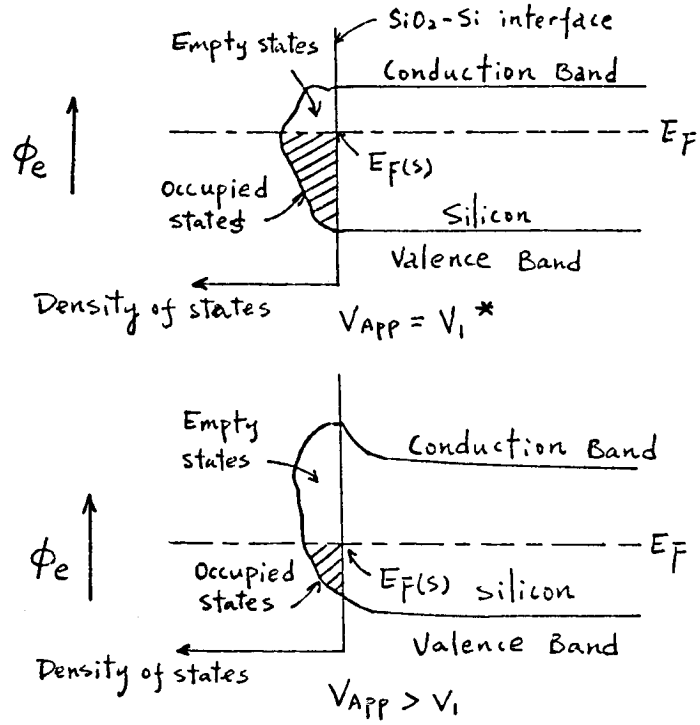


Fig. 42 Effect of bias voltage on Surface-states Occupancy.

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* is defined as the value of applied voltage which will straight out the energy bands in the silicon to the surface.

Following along the line of Terman's work Lehovec and Slobodskoy have also derived equivalent circuits for the MOS device. In their equivalent circuits the Boltzmann distributions of carriers in the space-charge layer at current flow, the loss angle, the extreme cases of negligible and infinite recombination rates as well as frequencies and bias voltages are taken into account [29]. A simple physical model which gives excellent agreement with the experimental observations at high measurement is also presented by Grove, Snow, Deal, and Sah [30].

9. Discussion

From the above studies about surface states and trapping we can understand qualitively the frequency independent nature of the MOS impedance. Yet, we must point out the thickness of the silicon-oxide layer of the MOS device we have observed is greater than 200 Å. For the silicon-oxide layer less than 200 Å the tunneling between silicon and the metal will play an important role in the V-I (Voltage vs. current) characteristic as well as impedance of this MOS device. The surface of silicon is also quite sensitive to surface preparation. Buck and McKinn (20) found widely different surface potentials after soaking the silicon in either sodium dichromate, boiling deionized water, HF or 10/1 - HNO_3/HF. Moore and Nelson also found the changing of surface potential due to adsorbed films of sodium dichromate(21). Clearly the detailed understanding of the tunneling digital transducer will not be complete until more work is done in this area.

D. Impurity Distribution at the Silicon Surface

The variation of the depletion layer capacitance with voltage is dependent upon the impurity and defect distribution in the semiconductor as illustrated in Fig. 43 for an abrubt junction diode. A semiconductor surface is disturbed by many defects which penetrate a finite

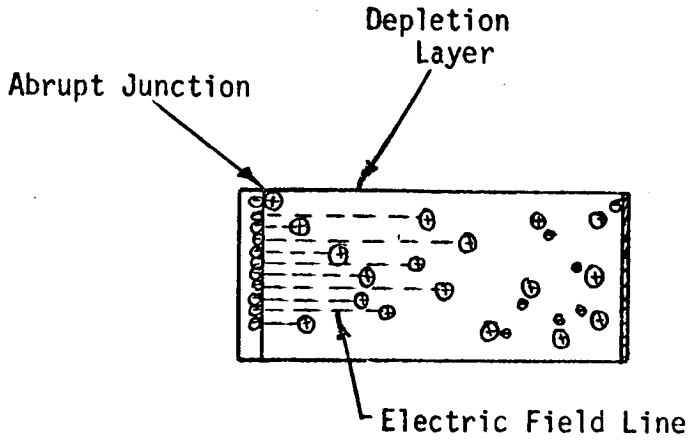
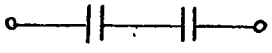


Figure 43 Impurity-defect distribution in a semiconductor.

depth into the semiconductor bulk. These defects may cause a non-homogeneous distribution of localized states in the bulk near the surface. The MIS tunneling junction offers a possible experimental method of determining this distribution. The analysis which follows first discusses abrupt PN junctions and thick insulator MIS structures. This is followed by an analysis of thin MIS structures which utilizes the point of tunneling saturation to determine the voltage at which the surface states are completely filled.

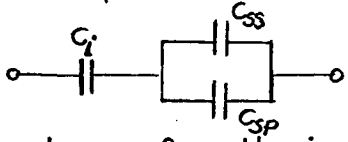
For an abrupt junction PN diode, Schottky[31] found that the reciprocal depletion layer capacitance increased linearly with the square root of the voltage across the layer. This square root

relationship has been verified many times, e.g. Giacoletto.[32] Garrett and Brattain[33] point out that the assumptions which produce the square root dependence are clearly met by a reversed biased PN junction but not completely by the surface of a semiconductor. Fig. 45 is a plot of $(1/C_{sp})^2$ versus applied voltage for the N-type MIS capacitance-voltage curve of Fig. 44 . C_{sp} is the space charge (depletion) capacitance calculated from the measured capacitance using the following equivalent circuit:



C_i C_{sp} , C_i = Insulator capacitance.

If the depletion layer followed a square root relationship, as does an abrupt PN junction, then the curve of Fig. would be a straight line. Lehovec, et al[34] and Terman[35] reason that the depletion layer capacitance of an MIS structure follows the square law relationship but the charge which collects in the surface states prevents the manifestation of this fact in a simple $(1/C_{sp})^2$ versus applied voltage plot. In a back-biased PN junction all of the applied voltage appears across the depletion region. In the MIS structure, however, the applied voltage is divided between the insulator and the depletion layer. How the voltage divides depends upon how the charge collects in the surface states. Lehovec assumes the MIS equivalent circuit to be:



where: C_i = the insulator capacitance

C_{sp} = the space charge capacitance

C_{ss} = the capacitance associated with the charge collected in the surface states.

If the total capacitance is measured at a high frequency, the charge in

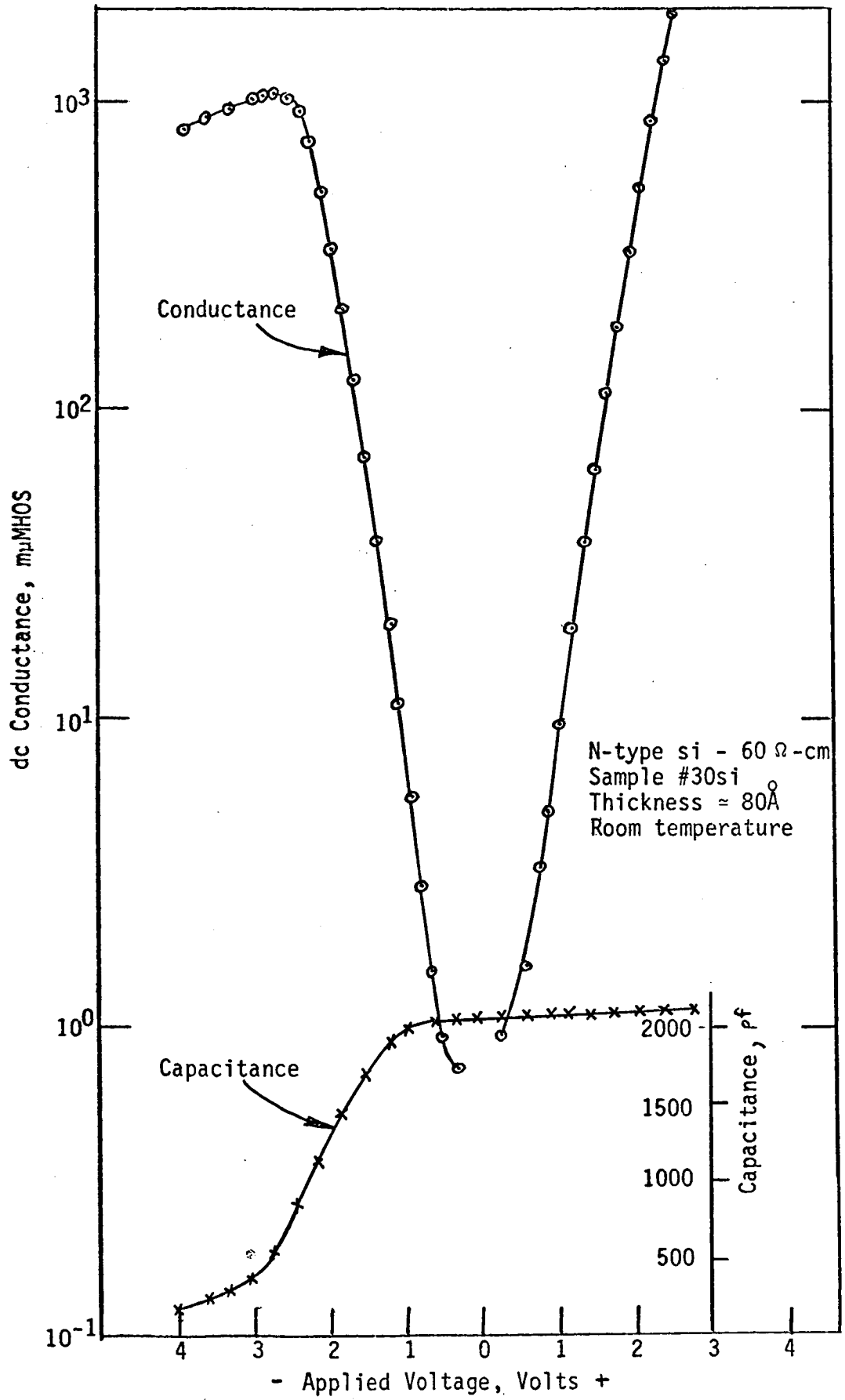


Figure 44 Depletion layer formation on N-type Silicon. Negative voltage indicates semiconductor reverse bias.

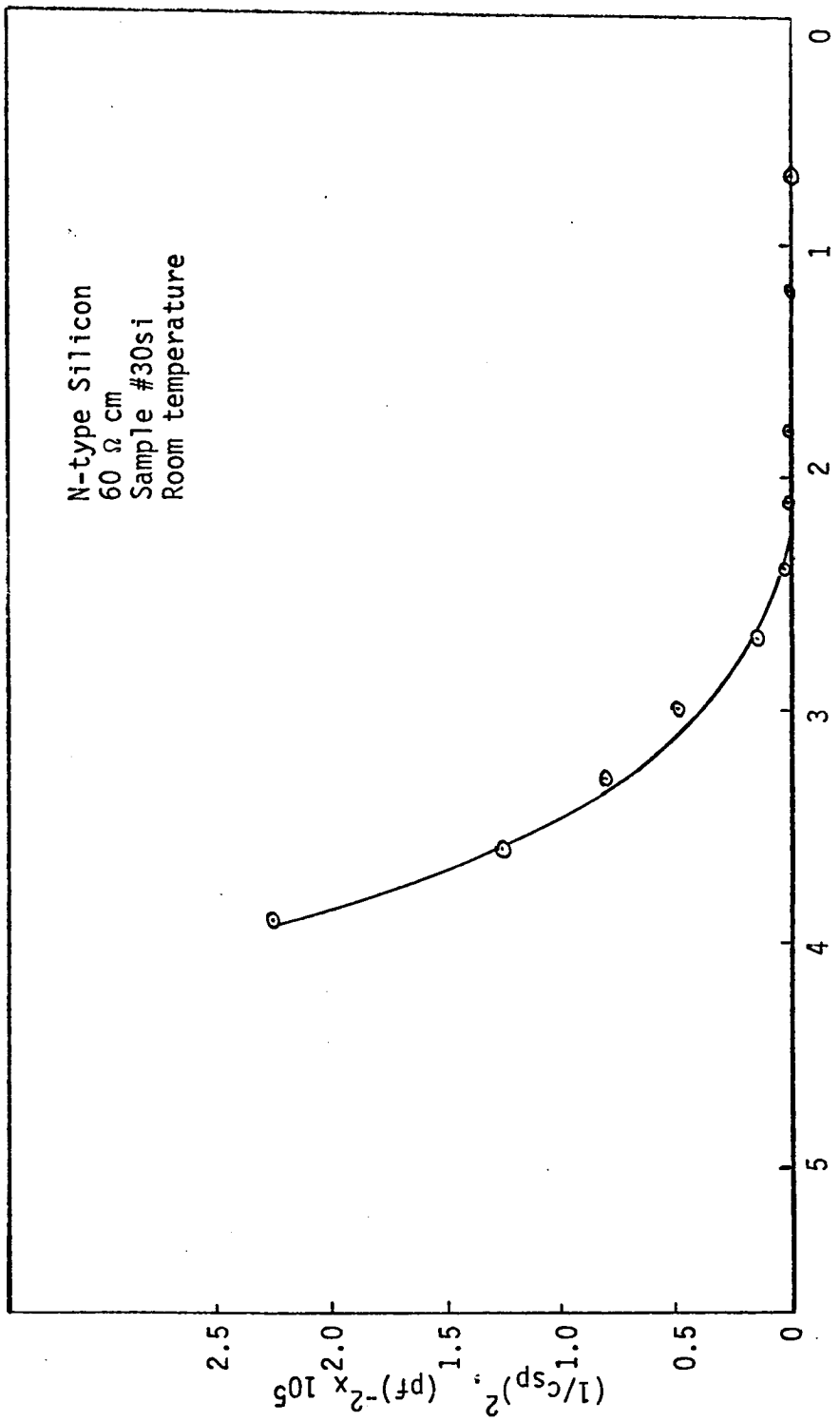
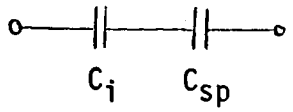


Figure 45. Square of the reciprocal depletion layer capacitance versus applied voltage.

the surface states cannot follow the ac field, hence the contribution of the surface state to the total capacitance is not known with confidence. However, Lehovec assumes the high frequency equivalent circuit to be:



The measured capacitance, C_m, is:

(41) $$\frac{1}{C_m} = \frac{1}{C_i} + \frac{1}{C_{sp}} \quad \text{and} \quad C_{sp} = \frac{C_m C_i}{C_i - C_m}$$

Lehovec then assumes a form of the Garrett and Brattain square root equation (which assumes a homogeneous distribution of impurities).

(42) $$C_{sp} = \left(\frac{\varepsilon n_o e^2}{2kT}\right)^{1/2} \left\{ \frac{1 - \exp\left(\frac{eV_{sp}}{kT}\right)}{\left[\frac{-eV_{sp}}{kT} - 1 + \exp\left(\frac{eV_{sp}}{kT}\right)\right]^{1/2}} \right\}$$

where: V_{sp} = voltage across the space charge region

n_o = bulk electron concentration

e = electronic charge

ε = the dielectric constant.

Note that V_{sp} is negative which leads to Eq. (41) for $\frac{eV_{sp}}{kT} >> 1$.

(43) $$C_{sp} = \left(\frac{\varepsilon n_o e}{2}\right)^{1/2} V_{sp}^{-1/2}$$

From Eqs. (39) and (40) the voltage drop across the depletion layer can be calculated. With V_{sp} known, the space charge, Q_{sp}, can be subtracted from the total charge. This difference is attributed to the charge collected in the surface states.

Since the square root depletion layer equation is known to be valid for depletion layers within the bulk silicon, Lehovec's formulation

seems reasonable for a depletion layer which has penetrated the bulk. This permits calculation of the surface state charge as a function of applied voltage. However, surface defects may penetrate the bulk silicon and create a non-homogeneous distribution of localized states which will give rise to a non-square root C-V relationship. At low voltage the impurity distribution analysis is complicated by the collection of charge in surface states. At higher voltage the surface states are filled and the C-V relationship is directly related to the impurity and defect distribution. The dc voltage at which the surface states are fully charged can be obtained for thin insulator MIS structures from a tunneling current curve for the same sample. The point of current saturation corresponds to the point of filled surface states and can be found by the method of Fig. 12a. For sample #30si, the voltage at saturation, V_s, is 2.4 volts. Subtracting V_s from the applied voltage, V_A, and plotting (V_A-V_s) versus $1/C_{sp}$ on a log-log scale (Fig. 52) yields the relation:

$$\frac{1}{C_{sp}} = B(V_A-V_s)^{0.8}$$

where: B = constant

V_A = applied voltage

V_s = saturation voltage

C_{sp} = depletion layer capacitance

Giacoletto [36] analyzed the C-V relationship for abrupt junction diodes with an arbitrary impurity distribution. Using Giacoletto's results, the impurity-defect distribution at the silicon surface of the MIS structure can be found. The analysis proceeds as follows:

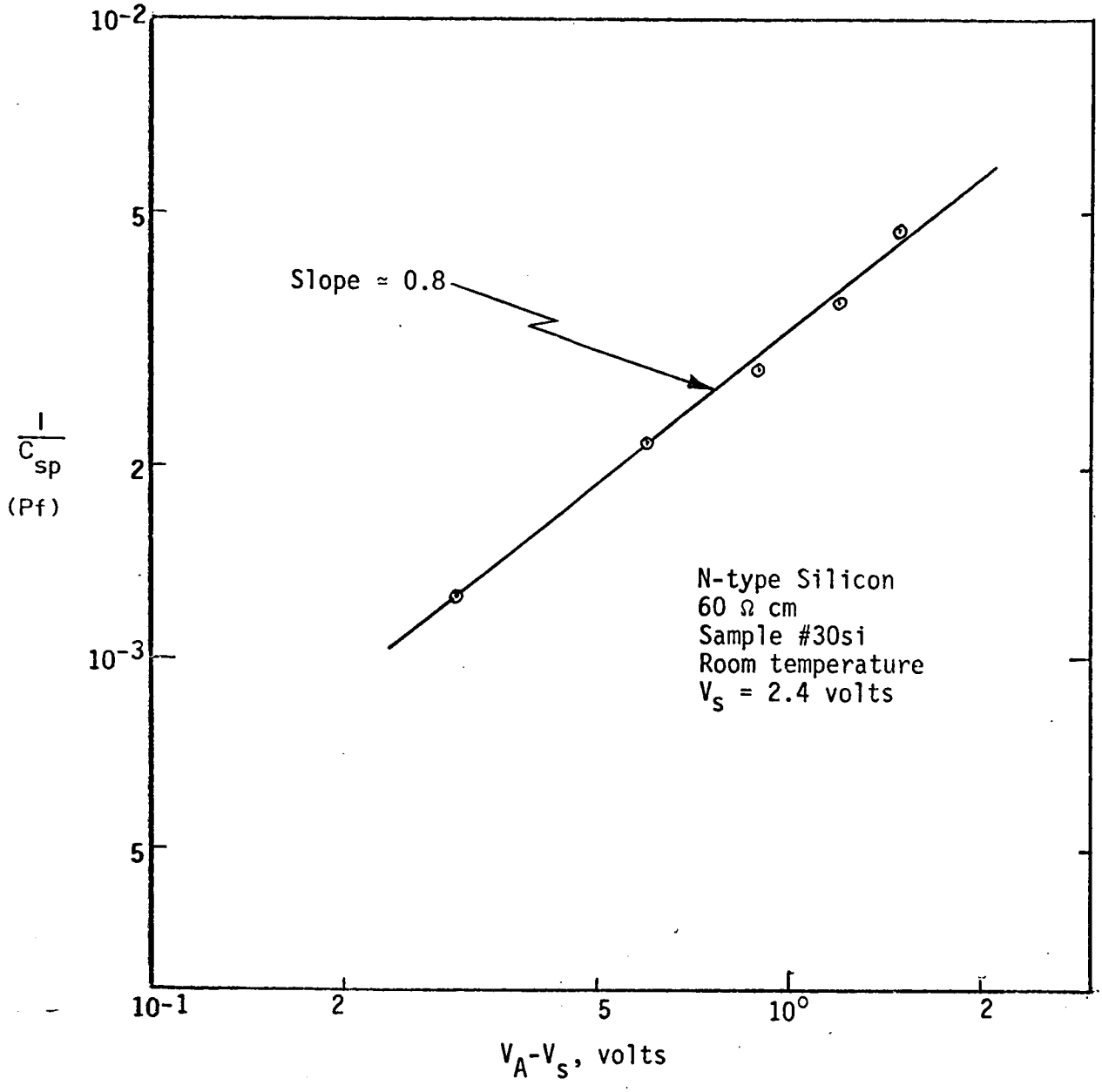


Figure 46 Reciprocal depletion layer capacitance versus depletion layer voltage.

$$\frac{1}{C_{sp}} = B(V_A - V_S)^{\alpha} = \frac{W}{A\epsilon}$$

where: W = depletion layer width

A = area

ϵ = dielectric constant

α = slope of the log-log C-V curve.

Thus

$$(44) \qquad V_A - V_S = \left(\frac{W}{BA\epsilon}\right)^{1/\alpha}$$

Giacoletto's expression for the impurity distribution, I(x), in the x direction is:

$$(45) \qquad I(x) = \frac{\epsilon}{en_i} \left.\frac{d(V_A - V_S)}{dW}\right|_{W = x}$$

where: e = electronic charge

n_i = intrinsic electron density.

Substituting Eq. (44) into Eq. (45) yields:

$$(46) \qquad I(x) = \frac{\epsilon}{en_i}\left(\frac{1}{BA\epsilon}\right)^{1/\alpha}(x)^{1/\alpha - 2} = \text{constant}\,(x)^{1/\alpha - 2}$$

From Fig. 46, $\alpha = 0.8$. Therefore the impurity-defect distribution for sample #30si is, $I(x) = \text{constant}\ x^{-0.75}$, which is sketched in Fig. 47.

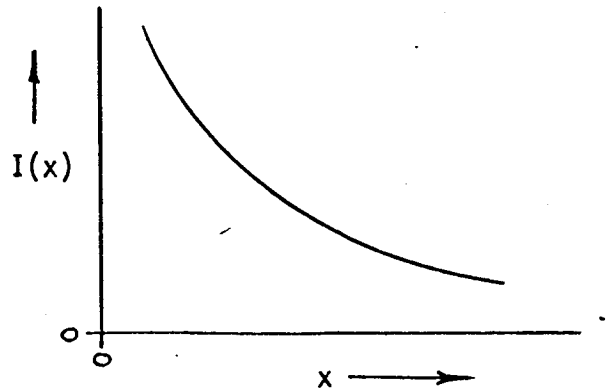


Figure 47. Impurity distribution of sample #30si.

The surface is shown to have a high impurity-defect density. This density decreases with penetration into the bulk. It is expected that I(x) would approach a constant at a sufficient distance from the surface where $\alpha = 1/2$ and $I(x) = \text{cont.} x^{\frac{1}{1/2}-2} = \text{const.}$

The above solution is dependent upon the choice of V_s which determines the exponent α. Also the location of $x = 0$ is not known. However, the above method seems to be valid and opens the door to a means of investigating impurity-defect distributions at a semiconductor surface. The method may be particularly useful in examining the MIS system with a thermally grown oxide since the oxidation process can change the surface doping density by diffusion redistribution of the impurities and by impurity rejection from the oxide.[37] It may also be possible to determine the depth of surface damage by correlating the voltage at which the capacitance begins to follow the square root law relation.

V. THIN FILM RESEARCH

To insure an adequate back-up to the effort on MIS tunneling a broader program of basic thin-film research has been undertaken. The objectives are to develop digital transducer technology, to get a more fundamental understanding of the physical and chemical processes, and to increase the number of useful phenomena which may be exploited for digital transducer action. The progress along several lines is described in this section.

A. Deposition of Silicon Nitride on Metal-Coated Substrates

A metal-insulator-metal structure, using the dielectric to be studied as the insulator, offers the best method of studying the electrical properties of thin dielectric films. This silicon nitride study included films of thickness varying from 500 to 4000 Angstroms on molybdenum-coated quartz plates. The reaction of silane and ammonia in a hydrogen atmosphere at temperatures from 600 to 900°C deposits the Si_3N_4. The apparatus materials include only teflon, stainless steel, graphite and quartz. A resistive graphite substrate holder heats the substrate. Typical flowrates are 2000 std. cm^3/min for hydrogen, 150 std. cm^3/min for ammonia, and 10 std. cm^3/min for silane. Deposition rates range from 100 Å/min depending on temperature and flowrates, to 1000 Å/min. The resulting films exhibit resistivities of the conduction component at high fields which are stable and reproducible.

B. I-V Characteristics of Mo-Si_3N_4-Metal Structures

I-V data form a straight line over as much as four decades on a Schottky plot for thin films of vapor deposited silicon nitride in a metal-insulator-metal configuration. Thickness variations, activation energies, and different metals for electrodes indicate a bulk limited process. Current

variation with temperature is typical of thermal emission processes. These considerations suggest a transport mechanism similar to the Poole-Frenkel effect.

C. Theoretical Program on Exotic Dielectrics

The search for natural phenomena related to the digital transducer necessitates concurrent research into exotic dielectrics. Chemical vapor deposition (CVD) provides an efficient means of obtaining such exotic dielectrics. Controlling parameters in an atom-by-atom deposition process yields tailor-made materials having desired combinations of physical, thermal, and electrical properties. In order to be useful in this project the film must be thin, uniform, reproducible, virtually pin-hole free, homogenous, and must passivate the surface of the semiconductor, possess high stability, high breakdown voltage, and low dissipation or loss mechanisms. In particular, freedom from hysteresis effects would make it a welcome transducer material.

One of the immediate aims of this research is the production of an insulator with a high dielectric constant. In addition to the great value of such a material in microcircuits for higher capacitances in integrated circuits and higher gain in field-effect-transistors, such a material would provide much more responsive transducer action since the high dielectric constant would cause more current for greater tunneling. The pyrolysis of metal alkoxides constitute one basis for the CVD technique yielding thin film insulators with high dielectric constants. Thin films of titanium compounds offer desirable dielectric properties; i.e. TiO_2, $\varepsilon = 100$; $BaTiO_3$, $\varepsilon > 1000$.

Clevite Research Corporation in working with Sandia Corporation (38) has concentrated almost entirely on lead titanate zirconate polycrystalline materials in their research on piezoelectric materials. Barium titanate was the first piezoelectric ceramic. It is capable of attaining permanent or nearly permanent polarization. Other forms of this may have stronger distortion, larger electric moment, and may be capable of being mistreated in a variety of ways and still remain strongly ferroelectric.

The digital transducer requires a dielectric that reacts to ambient stimuli such as light, radiation, pressure, or temperature. Barium titanate exhibits a marked discontinuous change with temperature. The insulator for the digital transducer need not exhibit such a discontinuity but may react to external stimuli in an analog fashion. Stress-strain changes would also be important. A purer dielectric should also make the step in current versus applied voltage much sharper. In addition such exotic dielectrics should exhibit different optical properties. Light might cause discontinuties or changes in the dielectric constant or in the current.

Chemical vapor deposition offers a technique for depositing films with the above properties which has several advantages over other techniques. Much versatility is possible since films can be deposited on metals or semiconductors. The dielectric film should be very homogenous since the reactant emanates from a source with preservable integrity. A sharper, cleaner interface can be expected since inter-diffusion is not necessary. The composition of the film can be controlled independently of the composition of the substrate. The processes involved generally can be carried out at lower temperatures than those required for deposition from inorganic

systems. The reactant and product vapors of the organic systems are usually less reactive and corrosive than those of the inorganic systems. The organic reactions may be more suitable for the preparation of high-purity oxides. Anisotropy of properties (thermal, mechanical, and electrical) are possible in materials that achieve a preferred orientation. In CVD advantage is taken of the formation of the deposits in atomic or molecular steps to obtain strong anisotropy of properties. This characteristic of CVD offers a tremendous potential for forming materials with specific properties and it can also give rise to useful and unique nonlinear effects. In addition, layer structures could be formed to take advantage of their unique electrical properties due to surface and composite layered characteristics.

Thus through chemical vapor deposition exotic dielectrics can be prepared with useful transducer properties.

D. Ionic Diffusion in the Al-Al_2O_3-Al Structure

The behavior of thin film devices is expected to be very sensitive to the interface between the dielectric film and a metal overlaying layer. Diffusion of metal atoms or ions into a dielectric film could have a significant impact upon the characteristics of thin film digital transducers.

Wortman and Burger (39)studied the Al-Al_2O_3-Au system at elevated temperatures. Air ambient supplied gaseous oxygen for diffusion through the gold electrode. They observed an open-circuit oxygen ion current in the microampere range. In this study of ionic diffusion in the Al-Al_2O_3-Al system, the aluminum concentration gradient that exists at the upper interface produces the diffusion potential. The Al-Al_2O_3-Al structure

forms from vacuum deposition of the lower electrode, thermal formation of the oxide, then deposition of the upper electrode.

After cleaning a soda lime glass substrate by vapor degreasing and ultrasonic washing in deionized water, contact pads of DuPont silver paste are baked on. Placing the substrates in the Varian Associates vacuum system precedes pumping to 10^{-11} torr range by sorption, sublimation and ion pumping. Electron gun evaporation produces the aluminum lower electrode. The aluminum oxide forms thermally from dry oxygen admitted to a pressure of 40 to 50 torr while infrared quartz lamps heat the substrate to 550°K. Pumping to low pressure precedes a second evaporation which forms the upper electrode at room temperature. A rotating specimen mount holds substrates in six sequential positions during the various steps of the process. The resulting sandwich structure forms an electrochemical cell of $0.4cm^2$ area with the bottom electrode positive. A Keithley millimicrovolt meter measures the short-circuit current by indicating the voltage across a 100 ohm shorting resistor.

After the structure has been formed, four atomic concentration gradients exist; an oxygen and an aluminum gradient at both the upper and lower Al-Al_2O_3 interfaces. The lower interface is thermally grown and both the aluminum and oxygen concentration gradients are near equilibrium. At the upper interface, an abrupt concentration change exists for both oxygen and aluminum. Barrer (40) and Smithells (41) show no measurable oxygen diffusion through aluminum because oxygen is insoluble in aluminum. Figure 48 shows the one remaining aluminum gradient of importance at X = 0.

Because of the abrupt aluminum concentration gradient at X = 0, gradient induced diffusion will occur if left unimpeded. Jost (42) points

out that the conditions are much more favorable for ionic rather than atomic diffusion. Ions moving through an insulator produce a current which determines the nature of the diffusion process.

When the two electrodes are short-circuited, electron current flows to balance the movement of the ions. Any charge attempting to accumulate on the electrodes drains off through the external circuit. Since no charge builds up on the electrodes, the ionic diffusion proceeds unimpeded by an electric field.

The diffusion process must follow Fick's second law. A useful solution to Fick's law is:

$$C(X,t) = C_o + \{(C_s - C_o)/2\} \quad \{1 - \mathrm{erf}[x/2(D_x t)^{1/2}]\} \qquad 47$$

C - Concentration

C_o - Concentration of Al in Aluminum oxide

C_s - Concentration of Al in upper Al electrode

X - Distance

t - Time

D_x - Diffusion coefficient in X direction (assumed constant)

This is a standard Gaussian error-function-form solution for this particular problem. Writing equation (V-1) in the form of a Taylor series, taking the derivative with respect to X, and evaluating at X = 0, gives the solution to Fick's law and yields the short-circuit current of the cell:

$$I_{sc} = -[Q_i A/\pi] \; [(C_s - C_o)/2] \; [D_x/t]^{1/2} \qquad 48$$

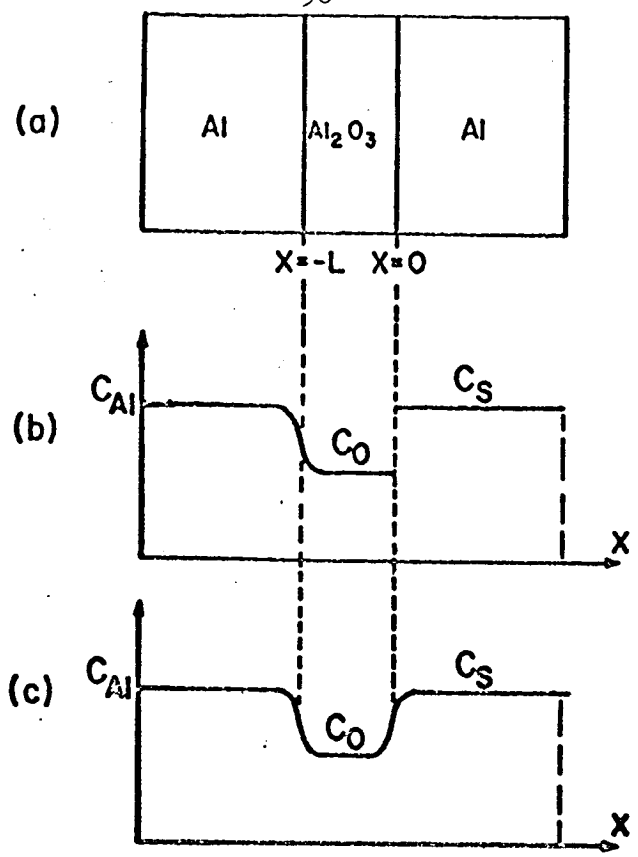


Fig. 48 Specimen cross section and concentration distribution profile.

a) Cross Section of Metal-Insulator-Metal Structure.

b) Concentration profile for the metal at t = 0.

c) Concentration profile for the metal at t>>0.

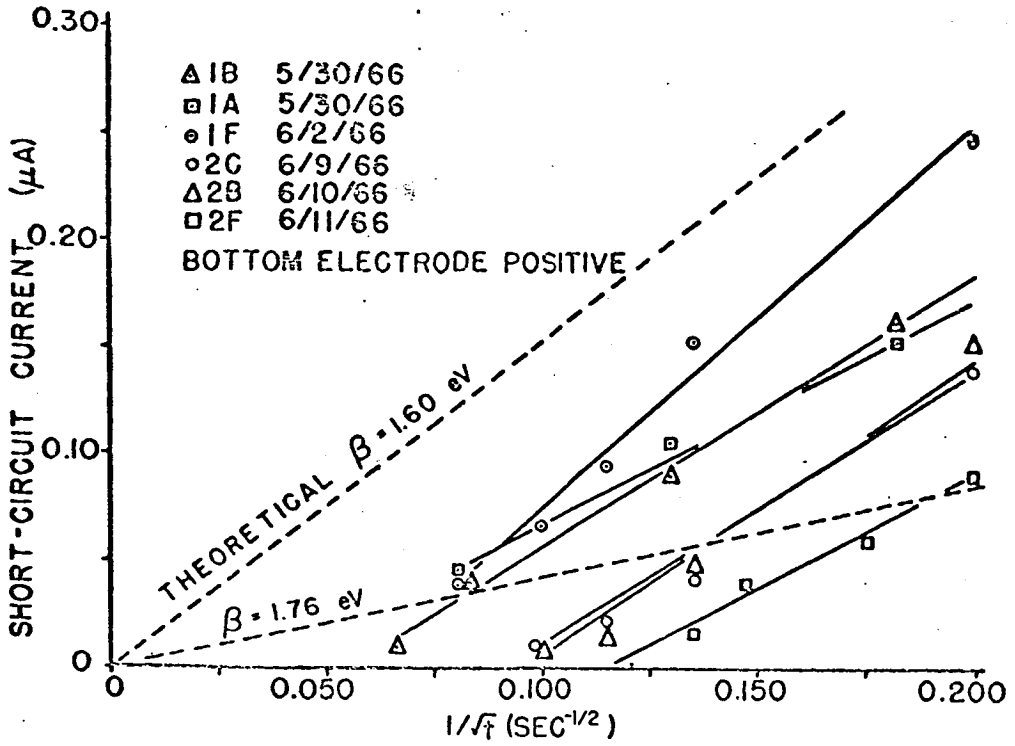


Fig. 49 Specimen short-circuit current versus the inverse root of time:

Solid lines for experimental data and dashed lines for theoretical calculations.

Where:

I_{sc} = Short-circuit current

Q_i = Charge of diffusion particle

A = Active area of cell

Jost (42) derived the following expression for the diffusion coefficient of the vacancy diffusion mechanism.

$$D_x = (d/3)\ (kT/2\pi m)^{1/2} \exp\ (-\beta/RT) \qquad 49$$

Where:

d - Interatomic distance

k - Boltzmann constant

m - Mass of diffusing ion

β - Activation energy

R - Universal gas constant

T - Absolute temperature

Equations 48 and 49 define the short-circuit current. Required quantities are absolute temperature, ionic mass, nearest neighbor distance, ionic valence, and activation energy.

All of these quantities are fairly well known except the activation energy. Dignam (43) determines the activation energy for Al_2O_3 by anodic polarization measurements. In the model presented here initial calculations use his value of 1.76eV. See Figure 49 Dignam's value does not accurately describe the present study because he employs anodic measurements in aqueous solution causing the presence of water as well as high electric fields in the oxide.

Figure 49 shows the short-circuit current plotted against $t^{-1/2}$ for

the six samples measured and two theoretical curves for an activation energy of 1.76 and 1.60eV. Note the points describe straight lines to support the $t^{-1/2}$ time dependence predicted by equation (48). However, both slope and intercept differ from the 1.76eV curve. The slope discrepancy is corrected by using a new activation energy of 1.60eV to an accuracy of $\pm$ .02eV. The difference of this value and the value determined by Dignam arises from the different fabrication and measurement techniques employed. The nonzero intercept appears to result from "aging" of the samples during heating and while measuring adjacent specimens, and from thermal voltages due to small temperature gradients in the specimen substrate.

This work demonstrates the technique of observing interface diffusion by simple electrical measurements. The experiment yielded an activation energy for the diffusion of aluminum into aluminum oxide of 1.60eV $\pm$ .02eV. The technique should apply to any system where both contacts can be made of the same metal to avoid thermal potentials. Extension of the technique to include the time variation of electrode potential and the thermal potential from different electrode metals requires additional study. The existence of ion diffusion effects at room temperature can now be expected to occur at a very low rate, but additional work will be needed to assess the importance of this phenomenon upon digital transducer action.

VI. PROGRAM FOR THE SECOND SIX MONTHS

A. PHYSICAL PHENOMENA

Developments in solid state physics in recent years have shown an increasing number of new phenomena. These include the Knight Shift, the Gunn Effect, Josephsen Tunneling and several others which are not yet identified by a popular name. These will be added to phenomena presently being studied to determine how they might be exploited for digital transducer effects.

B. TUNNELING THEORY

The analysis of the tunneling digital transducer is still deeply rooted in fundamental understanding of the transport of charge through thin insulating films. Our particular program is only a small part of the total national effort in thin film and surface properties of solids. A large fraction of our effort will be in monitoring the latest research results and contributing to them as the need for new knowledge is felt. Specifically, we will be analyzing charge transport through films from 50 Å to 5000 Å.

C. TUNNELING DIGITAL TRANSDUCER CONCEPTS.

The greatest effort will be in the search for properties of materials which will make them suitable to be incorporated in tunneling digital transducers. In particular we will be separating semiconductors and metals by dielectric materials with characteristics which are influenced by external effects and give the TDT the desired discontinuous input-output characteristics. We will continue our studies with polymer films

and vapor deposited Si_3N_4, and consider the use of more exotic dielectrics.

Fabrication of a three step analog-to-digital V-I device will be attempted during the second six months of the grant. Each element in the device will be examined as a thin film capacitor to learn more about the frequency dependence of tunneling structures. It is felt the future use of tunneling digital transducers as part of the integrated circuit technology will provide the digital system designer with some new tools.

VII. ATTENDANCE AT MEETINGS, PAPERS AND PUBLICATIONS

A. ATTENDANCE AT MEETINGS

The project director attended the Research Conference on Thin Films and Sensors, 8-9 September 1966 at the Research Triangle Park, Durham, N. C. This meeting was co-sponsored by the Langley Research Center of NASA. Project Director and J. L. Stone attented the International Electron Devices Meeting in Washington, D.C. While there, we visited the Goddard Space Flight Center to discuss research progress and applications of results to other NASA problems with Mr. Nelson McAvoy. Mr. J. R. Yeargan attended the Electro Chemical Society Meeting in Philadelphia, Pa. which had a session devoted to silicon nitride thin films.

B. PUBLICATIONS AND PAPERS

The following pages are abstracts of published papers, papers presented at meetings and theses and dissertations which were produced by the members of the laboratory staff. Most of them were supported, fully or in part by the NASA Grant NGR-44-012-043 and all are pertinent to the research project.

"Tunneling Between a Metal and Silicon Separated by a Polymer Insulator*", Carl W. Wilmsen, Ph.D. Dissertation, January 1967, The University of Texas, Austin, Texas.

ABSTRACT

This research investigates tunneling between a metal and silicon separated by an insulator (MIS structure) and develops a model describing the MIS current-voltage characteristics. Analysis shows that any model for MIS tunneling must consider the density of surface states and the formation of a depletion or accumulation layer in the silicon. The model shows that the electric field in the insulator controls the MIS current while the charge distribution in the silicon determines the insulator field.

For the experimental results presented in this paper a polymerized silicone film formed the insulator. After establishing the technique of forming the polymer, metal-insulator-metal (MIM) junctions enabled study of the electrical properties of the polymer and characterization of MIM tunneling currents. The MIM characteristics permitted comparative analysis with MIS structures.

The experimental MIS curves on both N and P type silicon show the exponential dependence of current on voltage and they indicate that the mechanisms for MIM and MIS tunneling are quite similar. An asymmetric saturation of the MIS tunneling occurs. This is shown to be caused by the formation of a depletion layer on the semiconductor which forms after completely charging the surface states. Experimental evidence verifies this model. The distinct roles played by the surface states, the depletion layer, insulator thickness, temperature and the work function of the field plate metal appears in the analysis.

* Work done under the sponsorship of NASA Grant 8-11235, NSF/URP and the Joint Services Electronics Program.

"Tunneling Between Silicon and a Metal Separated by a Thin Insulator*", C. W. Wilmsen, W. H. Hartwig and G. L. Neely, Bull. Am. Phys. Soc., Ser. II, vol. 11, no. 5, p. 740, July 1966.

ABSTRACT

Tunneling between silicon and a metal separated by a thin polymer insulator has been observed. The variation of dc conductance with applied voltage has been measured. These measurements are compared with previously reported tunneling in Si-SiO_2 -metal (MOS) structures[1] and with the tunneling in metal-polymer-metal junctions. The results of the tests performed on the silicon-polymer-metal (MPS) are similar to that reported for MOS samples. The MPS conductance curves clearly demonstrate the exponential nature of tunneling, which is similar to that found for metal-polymer-metal junctions. For positive voltage on P-type silicon, however, the conductance of the MPS structure was found to level off after the exponential rise as observed by Gray[1] for MOS structures. With N-type silicon, we observed that the conductance leveled off with negative voltage. This saturation of the conductance is shown to be related to the formation of a depletion region at the silicon surface, which is an essential factor in correctly interpreting the experimental results. The MPS tunneling junctions were constructed on chemically polished N- and P-type silicon wafers. The insulating polymer films were formed in a vacuum by polymerizing adsorbed diffusion pump oil on the silicon surface with 350-V electrons. The top metal electrode was vapor-deposited on the polymer to complete the MPS structure.

* Research supported by the Joint Services Electronics Program and the National Science Foundation Undergraduate Research Participation Program.

1. P. V. Gray, Phys. Rev. Letters 9, 302 (1962; Phys. Rev. A140, 179 (1965).

Presented at the American Physical Society Meeting, Summer 1966, Mexico City, August 29-31, 1966.

"Aluminum Diffusion into Aluminum Oxide" C.A. Snell, J.H. Christian, and H.L. Taylor, Bull. Am. Phys. Soc., Ser. II, Vol. 12, No. 2, p. 205, 1967

ABSTRACT

A study of aluminum-aluminum oxide-aluminum structures fabricated to achieve a net concentration gradient across the oxide yields the ionic diffusion coefficient and activation energy. The fabrication process involves an aluminum evaporation on glass followed by thermal oxidation and then another evaporation of aluminum. Elevated temperature ionic diffusion at an abrupt interface produces a current in an external short circuit. The theoretical short-circuit current expression fits quantitatively the slope of the experimental data which follows a $(\text{time})^{-1/2}$ dependence. The ionic motion becomes very small in about 5 min as indicated by the short-circuit current decreasing to 0. In the open circuit case, the fact that electrons effectively accumulate on the electrode where the ions diffuse into the oxide causes an open-circuit voltage. Analysis and observation of the open-circuit voltages vs time can further illuminate the ionic and electronic transport near a metal-dielectric interface.

"Deposition of Silicon Nitride on Metal-Coated Substrates" by J.R. Yeargan and H.L. Taylor, Presented at the Spring 1967 SWIEEECO meeting, Southwestern IEEE Conference Record, R.L. Carrel, Editor, Collins Radio Company, Dallas, Texas, April, 1967.

ABSTRACT

A metal-insulator-metal structure, using the dielectric to be studied as the insulator, offers the best method of studying the electrical properties of thin dielectric films. This silicon nitride study included films of thickness varying from 500 to 4000 Ångstroms on molybdenum-coated quartz plates. The reaction of silane and ammonia in a hydrogen atmosphere at temperatures from 600 to 900°C deposits the Si_3N_4. The apparatus materials include only teflon, stainless steel, graphite and quartz. A resistive graphite substrate holder heats the substrate. Typical flowrates are 2000 std. cm^3/min for hydrogen, 150 std. cm^3/min for ammonia, and 10 std. cm^3/min for silane. Deposition rates range from 100 Å/min depending on temperature and flowrates, to 1000 Å min. The resulting films exhibit resistivities of the conduction component at high fields which is stable and reproducible.

The research was supported by NASA Grant NGR 44-012-043 and the Air Force Joint Services Electronics Program under Grants AF-AFOSR-766-66 and AF-AFOSR 766-67.

"I-V Characteristics of Mo-Si_3N_4-Metal Structures" by J.R. Yeargan and H.L. Taylor, To be presented at the Electro Chemical Society Meeting, Dallas, Texas, May, 1967.

ABSTRACT

I-V data form a straight line over as much as four decades on a Schottky plot for thin films of vapor deposited silicon nitride in a metal-insulator-metal configuration. Thickness variations, activation energies, and different metals for electrodes indicate a bulk limited process. Current variation with temperature is typical of thermal emission processes. These considerations suggest a transport mechanism similar to the Poole-Frenkel effect.

This work supported by NASA Grant NGR 44-012-043 and the Joint Services Electronics Program under Grant AF-AFOSR-766-66 and AF-AFOSR-766-67.

A Wide Band Optical Detector Using the Photodielectric Effect in Cooled Semiconductors

by

W. H. Hartwig, G. D. Arndt and J. L. Stone

ABSTRACT

An AM-FM detector is described which makes use of the photodielectric effect to optically tune a microwave oscillator. The device operates at cryogenic temperatures where the photodielectric effect dominates the photoconductive effect in semiconductors such as germanium and silicon. The change in dielectric polarization due to photoexcitation of free charge is derived in the same manner as the complex photoconductivity. The device is an improvement over photoconductive detectors in several respects.

The device consists of an amplifier and a superconducting resonant cavity having a quarter-wave stub terminated in a semiconductor wafer. The unloaded cavities have Qs in excess of 10^7 which provides the oscillator with exceptional short-term stability. The bandwidth is limited by the lifetime of carriers which is typically one nanosecond. Other factors limiting the frequency response are the loaded Q and the time required for a disturbance to propagate around the oscillator loop. The sensitivity is proportional to lifetime. Response of 20 cps per microwatt of light on a high resistivity germanium sample illuminated by a GaAs laser is typical, with the operating frequency at 787 Mc/sec. The photodielectric detector is shown to surpass those operating in the absorption mode over a wide frequency range.

Abstract for IEEE 1966 International Electron Devices Meeting, October 25 - 28, 1966.

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