System Reliability Technology

Technical Report No. 5

PRELIMINARY DESIGN REVIEW ANALYSIS OF A 250-VOLT-AMPERE STATIC INVERTER

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RESEARCH TRIANGLE INSTITUTE · DURHAM, NORTH CAROLINA

FOREWORD

This report is one of a series of technical reports issued by RTI (Research Triangle Institute), Durham, North Carolina, under NASA (National Aeronautics and Space Administration) Contract NASw-905, "Development of Reliability Methodology for Systems Engineering". The contract is administered under the direction of J. E. Condon, Director, ORQA (Office of Reliability and Quality Assurance) NASA Headquarters, Washington, D. C.

The major objective of this contract is to apply probabilistic modeling techniques developed at RTI under a previous NASA contract to a NASA in-house R and D system and to conduct research necessary to further develop techniques appropriate to probabilistic modeling. A complex 250 volt-ampere static inverter under design and development by the Astrionics Laboratory of MSFC (Marshall Space Flight Center) was selected as a representative NASA system for application and demonstration of the techniques, and the majority of the technical reports in this series are devoted to documenting results of this effort. The additional research, both basic and applied in nature, on general probabilistic modeling is documented in several specific reports also included in this series.

The effort under this contract began in April 1964, and will continue for a period of approximately two years. The studies are being performed jointly in the Institute's Solid State Laboratory and Statistics Research Division under the general direction of Dr. R. M. Burger with W. S. Thompson serving as project leader.

PREFACE

This report is the fifth technical report of the series to be issued under Contract NASw-905. The text of this report is devoted solely to a preliminary design review analysis of the MSFC 250 volt-ampere static inverter which is being analyzed for reliability by modeling procedures under this contract. In addition to promoting sound engineering practices to enhance reliability, the complete inverter analysis under the contract is concerned primarily with both performance and life.

The analysis herein is not a complete reliability analysis of the inverter but is presented as one type of analysis that is performed by the designer at an early stage of the design process. The analysis is limited primarily to relatively simple hand calculations for comparing worst case operating requirements of components to their rated conditions. Such an analysis is not usually documented in this formal manner, but since it is used in this case as a basis for identifying the need for more detailed analysis for certain portions of the circuit, it is presented for future reference to demonstrate this role.

The major portion of the study leading to this report was conducted during an earlier phase of the contract. The major contributor in this effort was C. D. Parker.

ACKNOWLEDGMENT

The static inverter described in this report is being developed in the Applied Research Branch, Astrionics Laboratory, George C. Marshall Space Flight Center, NASA, Huntsville, Alabama 35812. Appreciation is extended to this group for permission to use the static inverter in this contract study. Special thanks are due to Astrionics engineers, R. F. Harwell, W. J. Kreider, and A. E. Willis for their helpful discussions on the inverter operation which contributed greatly to this report.

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1. Introduction

The functional operation of a complex static inverter was described in detail in Reference 1. This inverter is under development in the Astrionics Laboratory at George C. Marshall Space Flight Center and is designed as a space borne ac power supply to convert 28 vdc into a three-phase, 115 vac, 400 cps, sinusoidal output with a load capacity of 250 va. The inverter design is being used as a test vehicle under this contract effort for application of the reliability methodology being developed.

In the design and development of a space equipment the eventual goal is an equipment design providing adequate performance capability and having sufficient life to perform the intended functions for the duration of the mission. Thus reliability as an important design criteria is well established.

In a thorough analysis of equipment for reliability, certain procedures are inherent. Having established an initial circuit configuration as a basis for performing certain functions, the circuit designer proceeds with an iterative review process of the circuit with emphasis on performance and life. This process entails computation of certain component requirements and comparison with component ratings to assure that the component capabilities are not exceeded. Such an analysis serves to identify needed improvements in the design, and results may lead to actions such as; selection of better components, change in component purchase specifications, circuit redesign or modification, special qualification testing, negotiation of change in interface characteristics with other equipments, and identification of limitations in the circuit application. Seldom are analyses at this stage of the design documented in a manner more formal than the designer's notebook.

A preliminary design review of this type has been performed for the static inverter circuitry. The purpose of this report is to present this analysis primarily to illustrate the contributions such a review can make toward the design of reliable equipment. It also serves as a basis for identifying more detailed analyses to be performed within the framework of the reliability methodology being developed. It is emphasized that this review is not presented as a complete reliability analysis; however, the analysis was performed with the reliability as the principle criterion for a successful design. Principally, the design review is based upon the inverter specifications and the component parts characteristics as published by the component manufacturers. Often these are inadequate and other criteria are used as a basis for evaluating the design; for example, measured

component characteristics. Design decisions are also questioned freely throughout the analysis without knowing for certain that design criteria unknown to the reviewer influenced or even dictated certain decisions. To consider the questions raised by a design review such as this; however, can only enhance and not detract from a reliable equipment design. The calculations in this analysis are simple and will be obvious to most readers. In some cases units may be haphazardly presented, but also will be obvious. For each element reviewed, worst-case loads and inputs are usually assumed without considering possible negative correlations, and all but the most obvious considerations are included. Also, worst-case parameter values are used when the expected variation is significant. Extensive use has been made of the static inverter breadboard in that voltage and current levels determined from the review were compared with observed values.

Each functional circuit or major element of the inverter is discussed separately in Section 2 along with some additional factors that are considered pertinent to the reliability. For example, some circuit configuration changes are suggested for the purpose of improving the reliability of the inverter. Section 3 is devoted to more detail discussion of an observed failure mode of considerable interest that was predicted by the design review and later observed with the breadboard circuit. Section 4 presents, for reference, a summary of observed performance with the breadboard circuit. Finally, section 5 includes a summary of the findings of this design review and identification of more detailed analyses to be performed within the framework of the reliability methodology under development. With the publication of this report some of the additional analyses are being performed while some are already complete. These will be published in future technical reports or the final report.

2. Element Analyses

2.1 Six-Volt Power Supply

A schematic diagram of the six-volt power supply is presented in Figure 1. The six-volt power supply functions to provide regulated dc to elements of the timing section as illustrated in Fig. 2.2 of Reference 1.

(1) Required External Load

Estimates of maximum loads for the various elements supplied by the six-volt supply are as follows. The output voltage for these calculations is assumed to be 6.5 vdc as derived from the 7.5 v zener voltage of CR145 or CR139 through diodes CR140 or CR146 having approximately a 1 v forward drop.

(a) Closed Electronic Switch (see Fig. 5)

$$\frac{(6.5v)^2}{2K\Omega} = 21 \text{ mw.}$$

(b) Open Electronic Switch (see Fig. 5)

Q22 Base Circuit:

$$\frac{(18v)^2}{4K\Omega} = 81 \text{ mw.}$$

Q24 and Q25 Base Circuits:

$$\frac{(4.5v)^2}{4K\Omega} = 10 \text{ mw.}$$

(c) Primary Oscillator (see Fig. 6)

$$\frac{(6.5v)^2}{5.6K\Omega} = 7.5 \text{ mw.}$$

(d) Dissipation in 12 T. I. Integrated Circuits at 7 mw each (from T. I. data)

$$7 \text{ mw} \times 12 = 84 \text{ mw.}$$

(e) Clock Pulse Amplifier (see Fig. 9)

Collector Circuit:

$$\frac{(6.5v)^2}{1.5K\Omega} = 28 \text{ mw.}$$

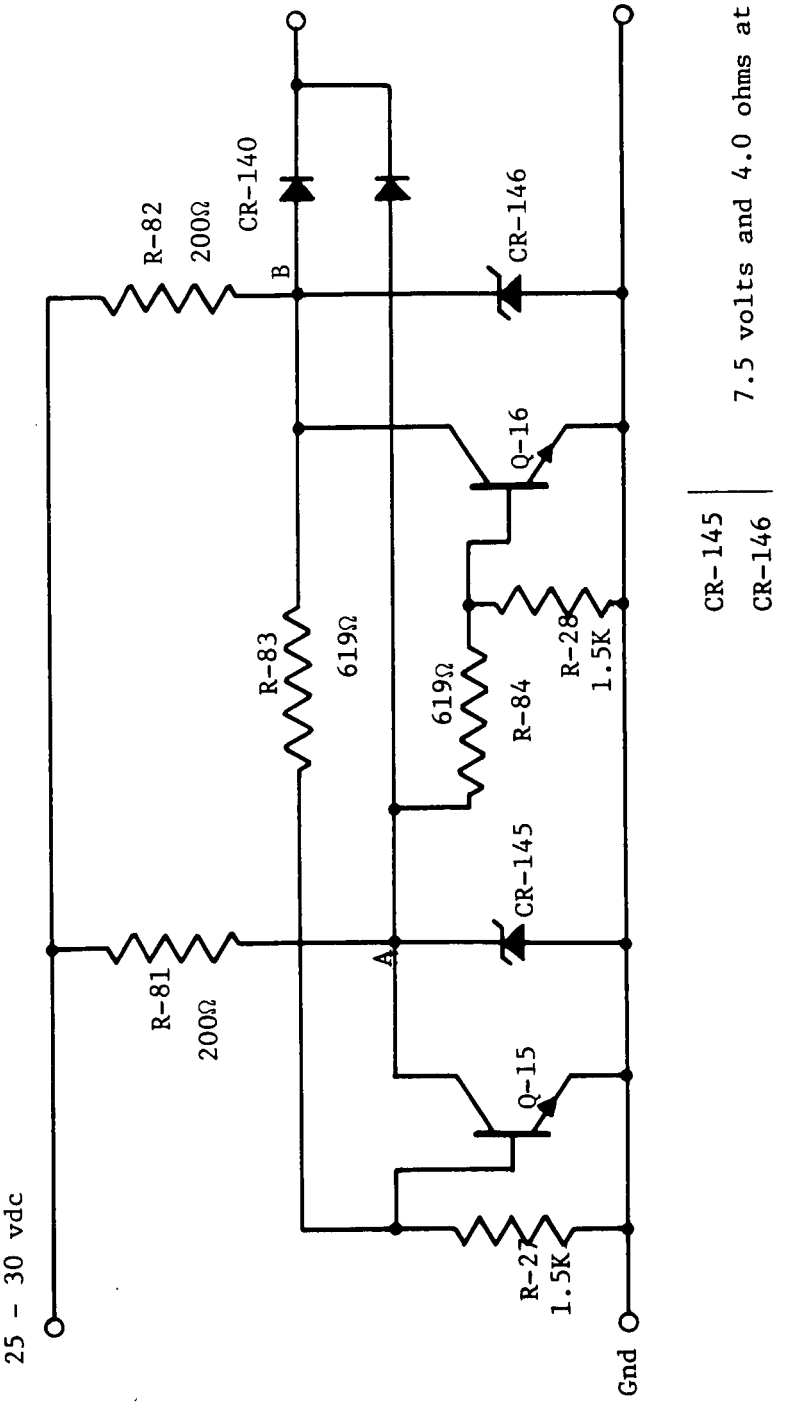


Figure 1. Schematic of the Six-Volt Power Supply

Base Circuit:

$$\frac{1}{2} \times \frac{(4.5v)^2}{1K\Omega} = 10 \text{ mw.}$$

(f) Magnetic amplifier drive (see Fig. 17)

$$\frac{(4.5v)^2}{301 \text{ ohm}} = 67 \text{ mw.}$$

(g) Timing pulse amplifier drive (see Fig. 11)

Diodes: $\frac{(4.5-2)v}{619 \text{ ohm}} \times 1.5v \times 6 = 36 \text{ mw.}$

Resistors: $\frac{(2.5v)^2}{619 \text{ ohm}} \times 6 = 60 \text{ mw.}$

Total external load $\cong$ 405 mw;

at 6.5 volts, the load current is

$$\frac{405 \text{ mw}}{6.5 \text{ v}} \cong 62 \text{ ma.}$$

Measured 6V supply current $\cong$ 65 ma.

(2) Internal Part Requirements

The following estimates of internal power dissipation are based primarily on worst-case conditions and, therefore, are conservative. Due to the internal redundancy there is a duality of components, and the power dissipation depends on the mode of operation with regard to redundancy.

(a) Resistors R83, R84 [$\frac{1}{4}$ watt, derated to $\frac{1}{10}$ watt @ 100°C]

Bias Circuit for the Inactive Channel;

$$P_{max} = \frac{(7.5v)^2}{619 \text{ ohm}} = 91\text{mw.}$$

This represents an additional load on the active channel of

$$\frac{91 \text{ mw}}{7.5 \text{ v}} = 12 \text{ ma.}$$

Bias Circuit for the active channel; power dissipation is negligible

(b) Resistors R81, R82 [200 ohm, 10 watt, derates to 7 watts at 100°C]

Inactive channel:

$$P_{max} = \frac{V^2}{R} = \frac{(30 - 0)^2}{200} = 4.5 \text{ watts.}$$

Active channel:

$$P_{max} = \frac{(30-7.5)^2}{200} = \frac{(22.5)^2}{200} = 2.53 \text{ watts}.$$

The power rating is adequate. R81 and R82 must be sufficiently low in value to allow the desired load current to flow without reducing the voltage at the zener diode (CR145, CR146) below the zener voltage. The total load current (both external and internal) is, from (1) and (a) above, (62 + 12) ma = 74 ma. Using the low input voltage requirement,

$$I_L = 74 \text{ ma} \leq I_{min} = \frac{(25 - 7.5)\text{v}}{200 \text{ ohm}},$$

$$74 \text{ ma} \leq 87 \text{ ma}.$$

The resistors are thus adequate for this purpose.

(c) Zener Diodes CR 145, CR 146 [1 watt; 7.5v @ I_{ZT} = 34 ma]
Using the upper input voltage extreme of 30 vdc

$$I_{ZT} = \frac{(30 - 7.5)\text{v}}{200 \text{ ohm}} = 38 \text{ ma}.$$

$$P_{max} = 7.5\text{v} \times 38 \text{ ma} = 285 \text{ mw}.$$

The power rating is adequate.

(d) Transistors Q15, Q16 [S2N2034A]
Rated I_C = 3 amps
Min. rated P_{diss} = 600 mw @ T_a = 100°C

Collector (ON transistor):

$$I_C = \frac{30}{200} = 150 \text{ ma}.$$

$$P_{max} = 1\text{v} \times 150 \text{ ma} = 150 \text{ mw}.$$

Base (ON transistor):

$$I_B = \frac{7.5\text{v}}{619 \text{ ohm}} = 12 \text{ ma}.$$

Based on manufacturer's data this base current is adequate for saturation.

$$P_{max} = 1\text{v} \times 12 \text{ ma} = 12 \text{ mw}.$$

The collector emitter breakdown voltage rating (BV_{CEO} = 80v min) is more than adequate for the OFF transistor.

(e) Diodes CR139, CR140 [400 ma, $V_f < 1$ volt]

The diodes are adequate to conduct the load current of 71 ma.

$$P_{max} = 1v \times 71 \text{ ma} = 71 \text{ mw}.$$

(f) Resistors R27, R28 [$\frac{1}{4}$ watt, derated to $\frac{1}{10}$ watt @ 100° C]

The power dissipation is negligible.

Total internal power dissipation $\approx$ 7.6 watts.

(3) Conclusions

From the preliminary observations it is generally concluded that the six-volt power supply is adequately designed to supply the six-volt load under all conditions of time, load, inputs, and temperature extremes. However, the circuit does dissipate more power than is necessary, and it appears that the redundancy scheme can be duplicated less expensively. The efficiency of the six-volt supply can be estimated to be as low as

$$\eta = \frac{P_o}{P_{in}} \times 100\% \cong \frac{405 \text{ mw}}{405 + 7600} \times 100\% \cong 5.3\%.$$

The redundancy assures that the six-volt supply will not fail if CR145 or CR146 short circuit or if R81 or R82 open. If CR146 or CR147 open circuit or if R81 or R82 short circuit, then the six-volt supply will be abnormally high and the system will fail.

It is suggested that the same redundancy can be achieved by simply removing the transistors and their biasing circuits. This will reduce the component count but cause both zener diodes to conduct continuously. Unless the zener diode failure probability is significantly increased in the zener breakdown region, it will not significantly increase the probability of failure of the system. If the circuit is further modified by paralleling the zener diodes as illustrated in Fig. 2, additional protection will be gained in that any one of the zener diodes can open or short without causing the circuit to fail. It is easily shown that the configuration illustrated in Fig. 2 will dissipate less power than the circuit of Fig. 1.

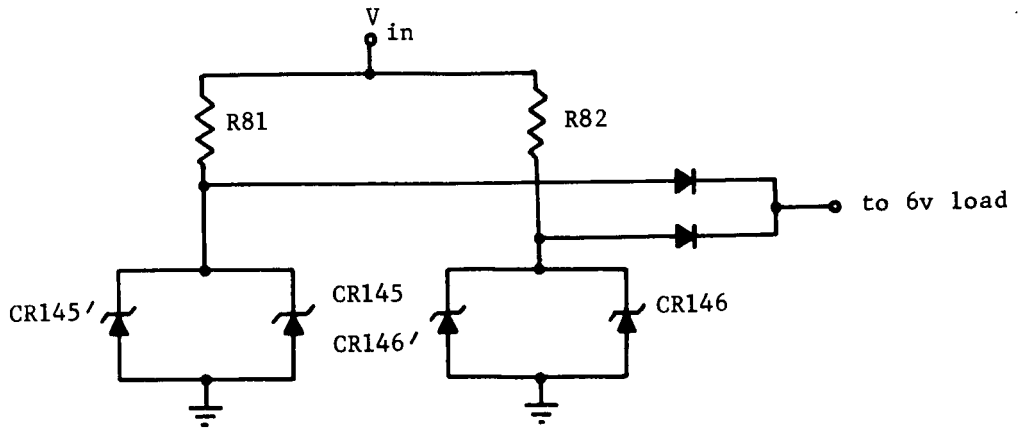


Figure 2. A Modified Six-Volt Supply

(4) Circuit Modifications

Since the preceding review was completed, the six-volt supply has been redesigned to provide for an anticipated increase in load. The new system arrangement, illustrated in Figure 3 provides for a non-redundant six-volt circuit in each of the two timing channels, and the electronic switches have been redesigned to control the unregulated dc supplied to the two timing channels rather than the 6 vdc.

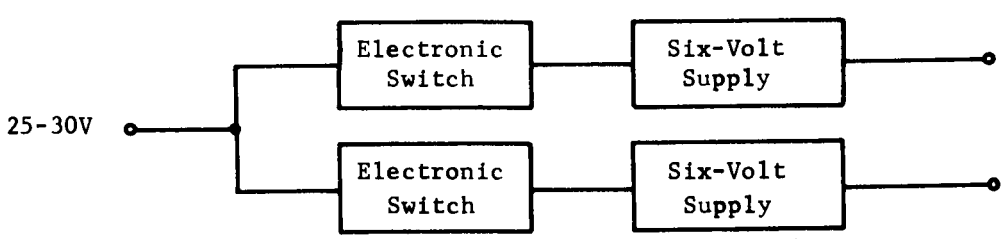


Figure 3. The Modified Timing Circuit

The redesigned six-volt supply circuit is illustrated in Figure 4. The circuit is expected to supply a total external load of 305 ma. At the 6.8 vdc zener voltage the output power is

$$6.8 \times 305 \text{ ma} = 2.08 \text{ watts.}$$

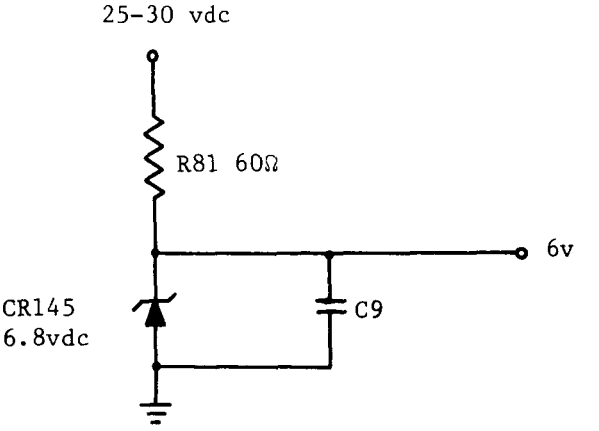


Figure 4. The Non-Redundant Six-Volt Supply

The internal part requirements are considered below.

(a) Resistor R81 [15 watts, derated to 10.5 watts at 100°C]

$$I_{max} = \frac{(30 - 6.8)v}{60 \text{ ohm}} = 386 \text{ ma.}$$

$$P_{max} = \frac{(30v - 6.8v)^2}{60 \text{ ohm}} = 9 \text{ watts.}$$

Using the lower input voltage requirement to compare the minimum available current with the required load current,

$$I_L = 305 \text{ ma} \overset{?}{\leq} I_{min} = \frac{(25 - 6.8)v}{60 \text{ ohm}} = 304 \text{ ma,}$$

$$305 \text{ ma} > 304 \text{ ma.}$$

This computation indicates that the circuit is marginal in that a larger load current will cause the output voltage to drop below the design value of 6.8 vdc.

(b) Zener diode, CR145 [10 watt; 6.8 volts]

$$I_{ZT,max} = (386 - 305)ma = 81\ ma.$$

$$P_{max} = 6.8 \times 81\ ma \approx 550\ mw.$$

(c) Capacitor C9

Since the ripple on the output is expected to be small, the power dissipation in the capacitor is considered negligible.

Total internal power dissipation $\simeq$ 9.55 watts.

From the above analysis the circuit is concluded to be marginal in its ability to deliver the required output current at the design voltage under low input voltage conditions. If the design of the new electronic switch as illustrated in Fig. 3 is essentially the same, an additional drop of 0.5 to 1.0 vdc, i.e., the V_{CE} drop of the electronic switch, will aggravate the situation even more. The resistance of R81 should therefore be decreased to

$$\frac{(25 - 1 - 6.8)v}{300\ ma} = \frac{17.2v}{300\ ma} \approx 57\ ohm.$$

This, of course, will increase the internal power dissipation slightly.

For the design as shown in Fig. 4 the efficiency at maximum power output is

$$\eta = \frac{2.08\ w}{(2.08 + 9.55)w} \times 100 = 17.8\%$$

which is an improvement in this regard over the original design.

With the appropriate modification in the resistance of R81 the circuit is considered of sound design and adequate for serving its intended function.

2.2 The Electronic Switch

(1) Closed Switch Operation

The electronic switch is shown schematically in Fig. 5. When the switch is closed, inputs q5 and $\bar{q}5$ and the six-volt supply to the primary of T9 are missing. Transistor Q22 is forward biased through R57, connecting the six-volt supply to the load.

(a) Transistor Q22, S2N1132

Rated I_c = 600 ma,

Rated P_{diss} = 600 mw,

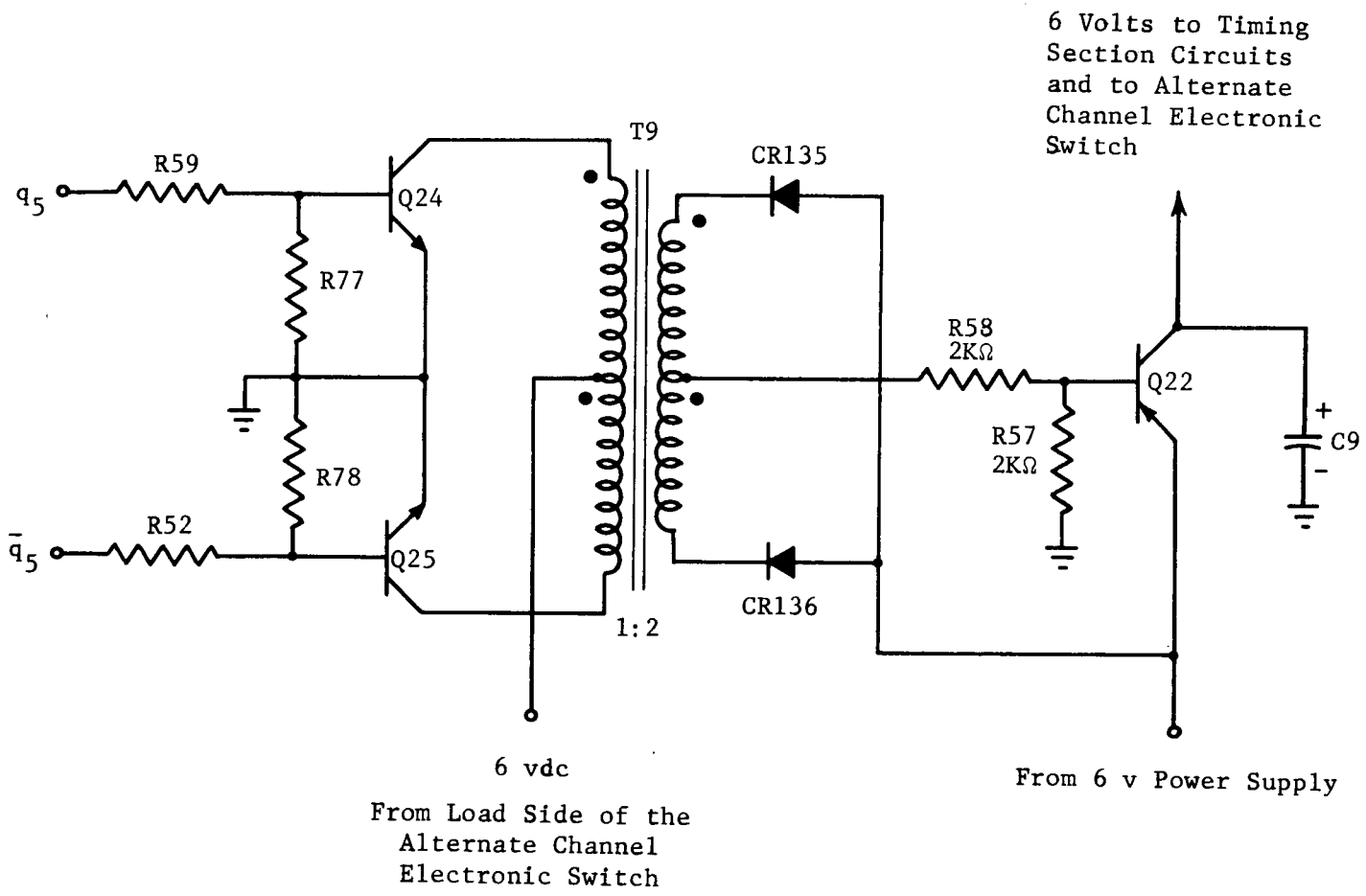


Figure 5. Timing Subsystem Electronic Switches

I_c requirement $\approx$ 65 ma (estimated load current),

The base current is estimated to be

$$I_B = \frac{(6 - 1)v}{2K\Omega} = 2.5 \text{ ma.}$$

From manufacturer's data, it is concluded that I_B = 2.5 ma is an adequate base drive for maintaining saturation.

Q22 operates as a closed or an open switch for long periods. Therefore, the power dissipation is negligible.

(2) Open Switch Operation

The inputs q5 and $\bar{q}5$ in Fig. 5 are complimentary squarewave signals. As determined in Section 2.6, the high and low voltage levels are approximately 3.5 and zero volts, respectively.

(a) Transistor Q22 (2N718A)

The required collector current is

$$I_c = \frac{6v}{4K\Omega \times (\frac{1}{2})^2} = 6 \text{ ma.}$$

For this collector current, the base current required for saturation is

$$I_B = \frac{6ma}{20} = 0.3 \text{ ma (from worst-case } h_{FE}),$$

$$I_B = 0.12 \text{ ma (from measured characteristics).}$$

The estimated base current is

$$I_B = \frac{(3.5 - 0.8)v}{2K\Omega} - \frac{.8v}{7.5K\Omega} = 1.2 \text{ ma,}$$

and is more than adequate.

(b) Transformer T9, MSFC #R1191 (core; Magnetics, Inc., Orthonal, 51056-2A)

N_p = 700 turns

$A_{fe} = 4.3 \times 10^{-6} \text{ m}^2$

$\Phi_s = A_{fe}B_s = 4.3 \times 10^{-6} \text{ m}^2 \times 1.45 \text{ web/m}$

$= 6.24 \times 10^{-6}$ web.

$\Delta\Phi_{max} = 2\Phi_s = 12.5 \times 10^{-6}$ web

For the 400 cps. operations,

$$\Delta T = \frac{1}{2} \times \frac{1}{400} = 1.25 \times 10^{-3} \text{ sec, and}$$

$$\Delta\Phi = \frac{e}{N}\Delta T = \frac{6}{700} \times 1.25 \times 10^{-3} = 10.8\mu \text{ web} < 12.5\mu \text{ web} = \Delta\Phi_{max}$$

Thus the transformer core is adequate.

(c) Resistors R52, R59[$\frac{1}{4}$ watts, derated to $\frac{1}{10}$ @ 100°C]

Maximum dissipation is $\frac{V^2}{R} \leq \frac{(4.5v)^2}{2K\Omega} \approx .01$ watts.

(d) Capacitor C9 [15v, 150μf.]

This capacitor is essential in that it removes the 400 cps spikes introduced by the alternate channel switch and the 4.8 kc ripple from the six-volt bus. Its capacitance and voltage ratings are adequate.

2.3 The Primary Oscillator

The primary oscillator is shown schematically in Fig. 6.

(1) Transistors Q30, Q31 (2N718A)

(a) Required $I_c = \frac{6v}{5.62K\Omega} = 1.1$ ma.

Required $BV_{CEO} = 6$ volts.

These requirements are adequately provided for.

(b) The rated power dissipation is

$P_d \gg (1.1 \text{ ma})\ (6v) = 6.6$ mw.

(c) $f_\beta \gg 10 \times 76.8$ kc = 768 kc.

(2) Resistors

Maximum power dissipated by any resistor is

$P_d = \frac{(6v)^2}{5.62\Omega} = 6.4$ mw $< \frac{1}{10}$ watt, the derated value for 100°C operation.

(3) The frequency stability of the output is determined by the stability of the crystal.

2.4 The Frequency Countdown Circuit

The frequency countdown circuit is a simple ripple-through counter constructed entirely of five Texas Instruments' series 51 integrated circuits, the SN511A R-S flip flop. A schematic of the frequency countdown circuit is shown in Fig. 7. The series 51 integrated networks are designed for use with other series 51 networks. The manufacturer states that any series 51 network will drive any

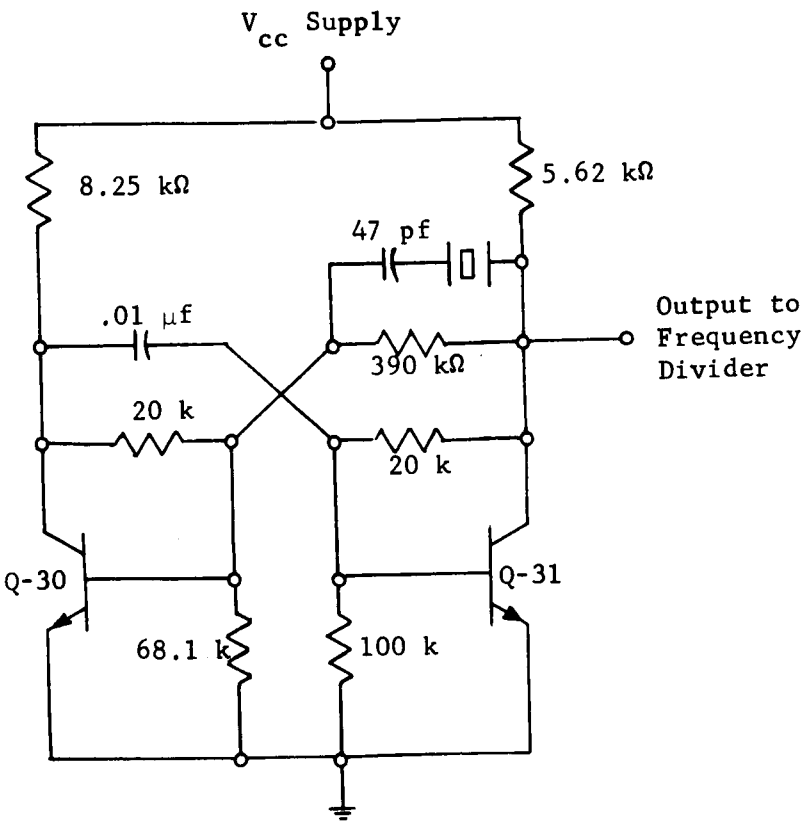


Figure 6. 76.8 kc Primary Oscillator

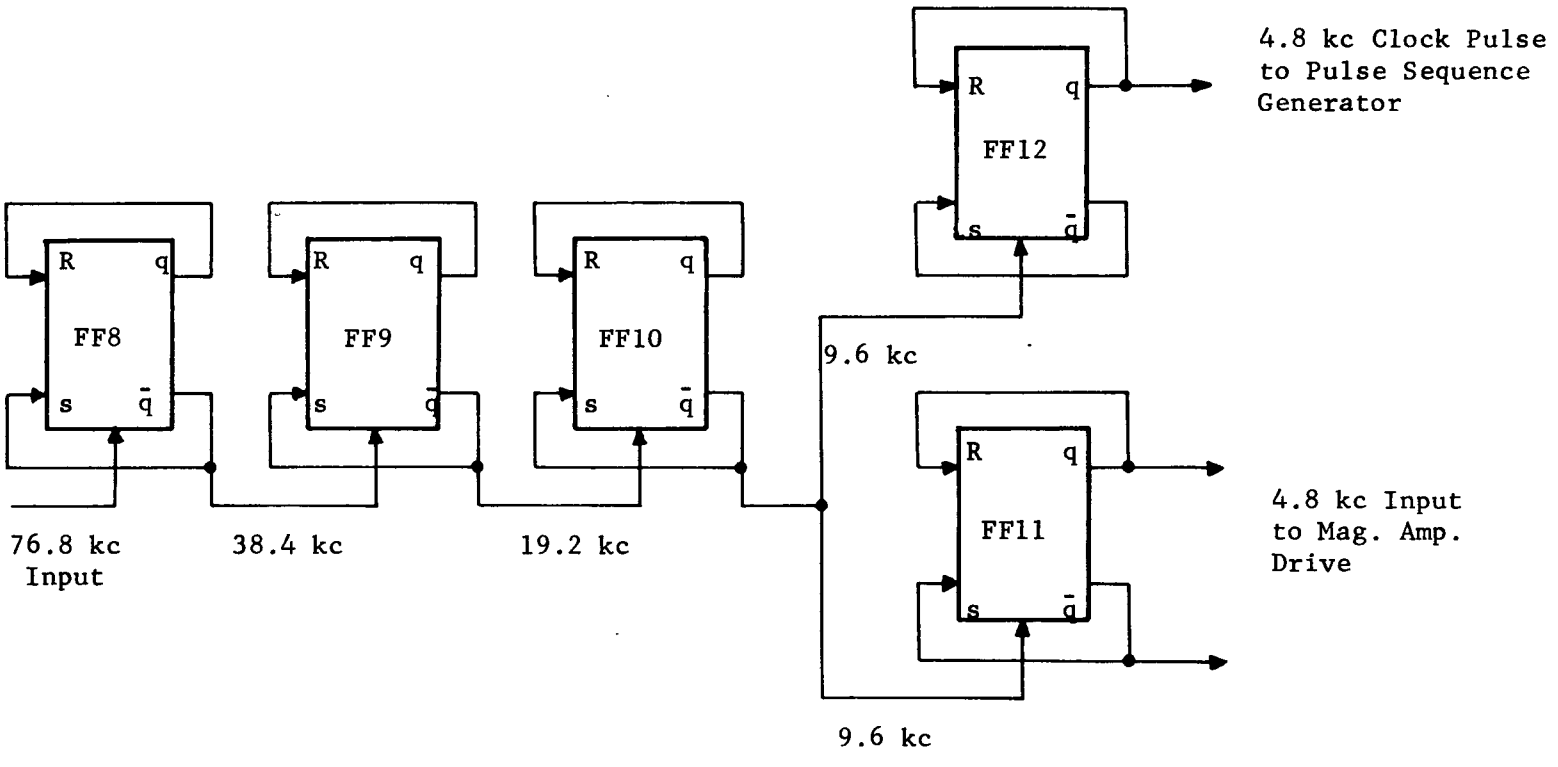


Figure 7. Frequency Countdown Circuit

other network in the series, and further cites in reference 2 the ripple-through counter used in the static inverter as a typical application. Unless a study is made of the integrated networks, a design review of equipment using the networks is limited to establishing that the design conforms to certain application rules, and that inputs and output to other equipment are within the range of values stated by the manufacturer to be satisfactory.

The application rules established by the manufacturer are concerned only with interconnections between the series 51 integrated networks. Input and output characteristics are given in reference 3 and these characteristics are used to assess the compatibility of non-series 51 inputs and outputs. The SN511A emitter-follower output characteristics published in reference 3 are reproduced in Fig. 8 along with the output characteristics of several units measured in the laboratory. All of the units exhibited a lower output impedance than that claimed by the manufacturer. In the following sections of this report, the output characteristics from reference 3 are used for worst-case analyses. Because of the low switching frequencies involved, switching transient times are considered of no concern in the frequency divider circuit.

One other concern is the power dissipation capabilities of the SN511A. At +25°C the units are rated to dissipate 50 mw and actually dissipate approximately 7 mw with zero fan out. When driving a timing pulse amplifier (TPA), as described in section 2.7, at 25°C and zero frequency (with the 28 volts removed from the TPA), the SN511A dissipates approximately 20 mw (from laboratory measurements). The application rules are stated for the -55°C to +125°C temperature range, but it is not known how the dissipation capability derates with increasing temperature. For the purposes of this review, it is assumed that rated power dissipation will not be exceeded at any temperature if the q and $\bar{q}$ outputs are a minimum, i.e., a DC fan out of 1, and the emitter follower outputs, q* and $\bar{q}$* operate in the lower half of the output characteristics defined in reference 3, i.e., below point "A" in Fig. 8.

As was pointed out in an earlier paragraph, the frequency countdown circuit conforms to all the series 51 application rules. The input from the primary oscillator is safely within the wide range of satisfactory inputs both in frequency (76.8kc) and pulse amplitude (6 volts maximum). The outputs from the frequency countdown circuit drive the magnetic amplifier drive circuit and the clock pulse amplifier, and these outputs will be considered in paragraphs discussing these two elements.

2.5 The Clock Pulse Amplifier

The clock pulse amplifier (CPA) and its position relative to the

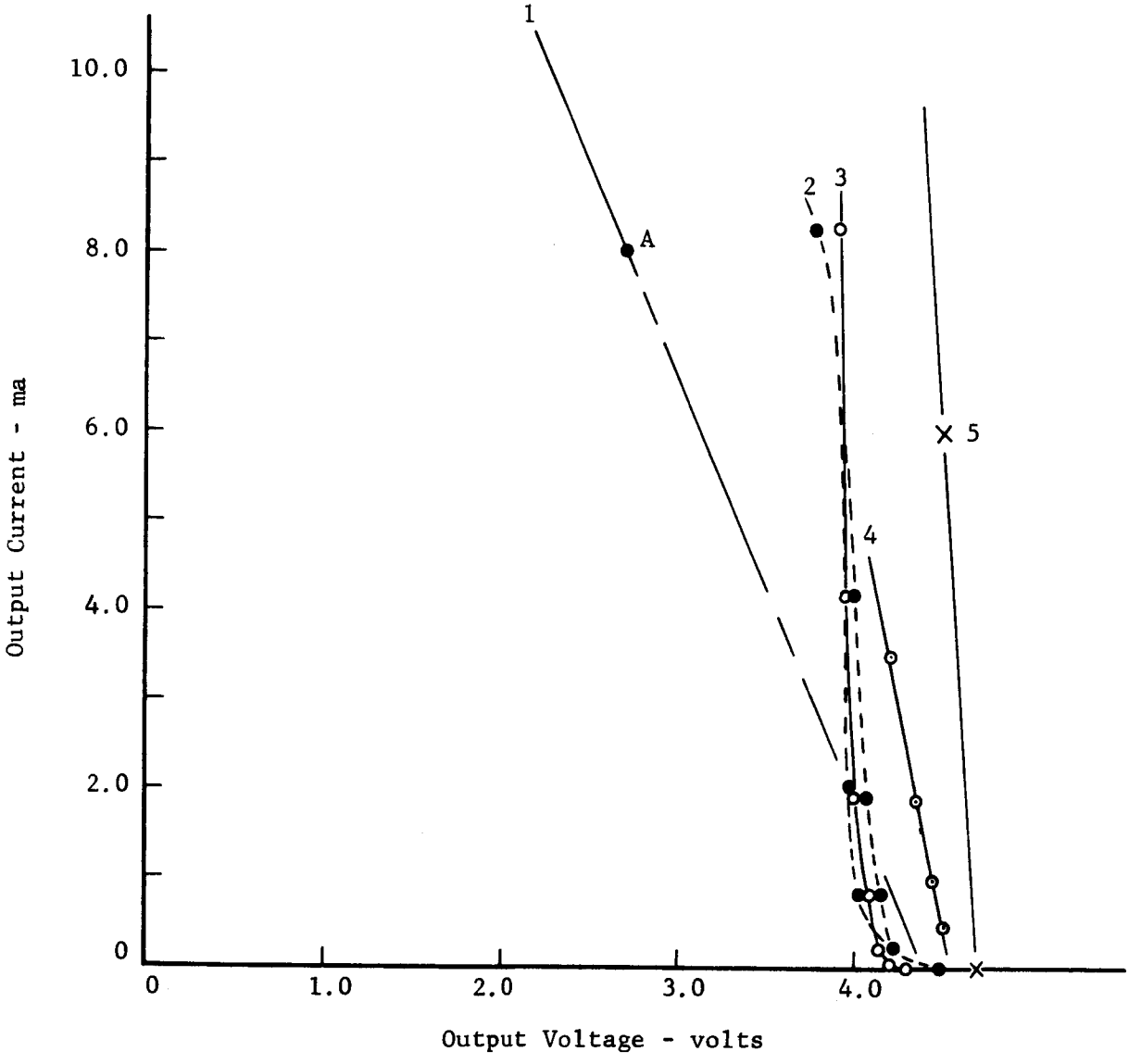


Figure 8. Output Characteristics of SN511A

1. Manufacturer published data. 2. 4.8 kc operation at 125°C--spread in data results from changing load on alternate emitter follower from no-load to equal load. 3. 4.8 kc operation--room temperature. 4. "d-c" characteristic obtained from transistor curve tracer. 5. "d-c" characteristics from a second unit.

frequency countdown circuit and the pulse sequence generator (PSG) are shown in Figure 9. This common emitter amplifier has an input impedance of approximately 1 K ohm and an output impedance of approximately 360 ohms. Its input is the 4.8 kc output of the frequency countdown circuit, and it supplies a 4.8 kc clock pulse to the PSG at approximately 1.5 volts. A consideration of the CPA design follows.

(1) Transistor Q28 (2N718A)

Required BV_{CEO} = 6 volts.

Rated BV_{CEO} = 50 volts.

Required $I_C \approx 6v/1.5K\Omega = 4$ ma $\ll$ Rated I_C.

Required Power Dissipation $\approx 1/8 \times 6v \times 4$ ma ≈ 3 mw.

Required $f_B \approx 10 \times 4.8$ kc = 48 kc.

Rated f_T = 80 mc.

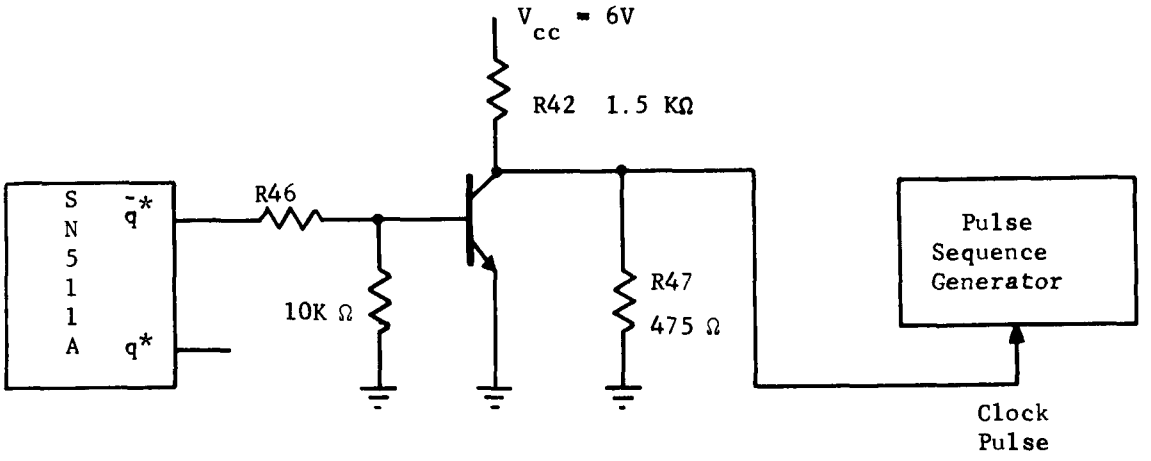


Figure 9. Clock Pulse Amplifier

From measured 2N718A collector characteristics, the base current required for saturation is

$$I_B = 0.08 \text{ ma} ;$$

from a worst-case h_{FE} computation, the required base current is

$$I_B = 4 \text{ ma}/20 = 0.2 \text{ ma}.$$

The estimated base current is

$$I_B > \frac{(3.5 - 1)v}{1K\Omega} = 2.5 \text{ ma}$$

(2) Resistors [All $\frac{1}{4}$ watt, derated to $\frac{1}{10}$ watt @ 100°C]

The maximum power dissipated by any resistor is

$$\frac{V^2}{R} = \frac{(6v)^2}{1K\Omega} = 36 \text{ mw} < \frac{1}{10} \text{ watt.}$$

(3) The output voltage amplitude is determined by the voltage divider formed by R42 and R47 and the load. Its maximum value is

$$V_{out} = \frac{6v \times .475}{1.97} \approx 1.44 \text{ volts.}$$

There have been unpublished reports of difficulties experienced with the SN511A units when the clock pulse input amplitude is too high, and the CPA is apparently, in part, a response to such experiences. It does perform the function of reducing the clock pulse input to the SN511A units in the pulse sequence generator (PSG) from 4.5 volts to 1.5 volts, approximately. It seems clear that, if the clock pulse input to an R-S flip flop is high with respect to the R and S terminations, the resulting state of the flip flop will be indeterminate. Such a condition is not likely to exist in the static inverter, however, since all flip flops are supplied from the same bus, and the R and S terminations are connected to SN511A outputs and the clock pulse inputs to SN511A emitter follower outputs.

In the absence of any specific written reports of unsatisfactory performance of the series 51 integrated circuits due to the amplitude of the clock pulse input, consideration was given to the elimination of the clock pulse amplifier. If the CPA output supplied the clock pulse input to the PSG directly, the application rules would be violated in that the fan out of the CPA SN511A network would be six. The application rules specify a maximum ac fan out of five, but this load is permitted over a temperature range from -55°C to +125°C and at clock frequencies greated than 500 kc. A study of the SN511A networks may illustrate that an ac fan out of 6 is not excessive at 400 cps and at the lower temperature extremes.

Experimentally, the clock pulse amplifier has been removed from one of the two timing channels in the static inverter, and the input signal to the amplifier connected directly to the amplifier load, i.e., the six SN511A flip flops of the PSG.

The static inverter breadboard has subsequently been caused to operate on the altered channel for extended periods of time and under all input, load and temperature extremes. No difficulties have been experienced with the timing channel during this period and the inverter has not switched from this channel to the redundant channel during operation. Consequently, it is concluded that the CPA may be unnecessary. This problem must be investigated further before a firm recommendation can be made for its removal from the circuit.

It is noted that in an earlier version of the static inverter, the present clock pulse amplifier was probably required for pulse shaping. In the earlier model, the 4.8 kc output of the frequency countdown circuit supplied the inputs to the magnetic amplifier drive circuit just as it does in the present model, but the 4.8 kc input to the PSG was supplied from a secondary winding on the magnetic amplifier drive transformer. The clock pulse winding supplied a six volt P-P, 4.8 kc square wave voltage that was symmetrical about zero. The CPA was necessary to eliminate the negative portion of the square wave and reduce the peak amplitude.

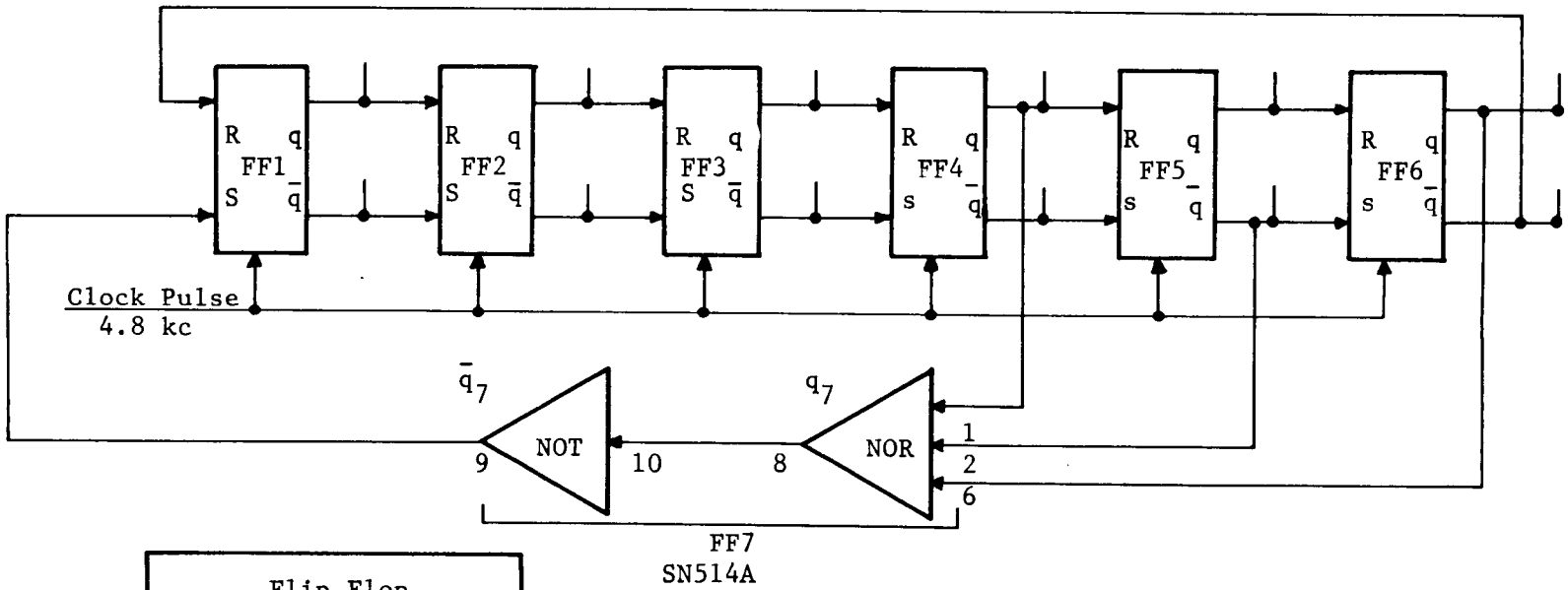
2.6 The Pulse Sequence Generator

The pulse sequence generator (PSG) is a Johnson Counter logic circuit consisting entirely of six Texas Instruments' SN511A networks and a Texas Instruments' SN514A network to reset the counter. The interconnection of these units is illustrated in Figure 10. The PSG is also used as an example application of the series 51 units by the manufacturer in reference 2 and the design of the PSG is in accord with the application rules stated in that reference.

The input to the clock pulse terminals of the PSG SN511A networks is within the range of values given by the manufacturer as satisfactory from both the frequency divider circuit and the CPA. The low frequency 400 cps clock pulse rate eliminates switching time as a performance consideration. The output of the PSG will be considered in the next section discussing the timing pulse amplifiers.

2.7 The Timing Pulse Amplifier

A schematic diagram of a timing pulse amplifier is shown in Figure 11. The inputs, q_i and $\bar{q}_i$, are complementary 400 cps. squarewaves provided by one of the series 51 integrated circuits in the PSG. The primary function of the TPA is to amplify these timing pulses to provide adequate base drive for power switching transistors Q36 and Q37 in the power converter stages. The operation is push-pull with transistors Q1 and Q2 being alternately turned ON and OFF at the 400 cps rate.



Flip Flop Truth Table			
T_n		T_{n+1}	
R	s	q	q
1	1	q_n	$\bar{q}_n$
1	0	0	1
0	1	1	0
0	0	Indeterminate	

Positive Logic

Emitter-follower outputs, q^* and $\bar{q}^*$, of FF1-FF6 drive the PSG loads

Figure 10. Block Diagram of the Pulse Sequence Generator

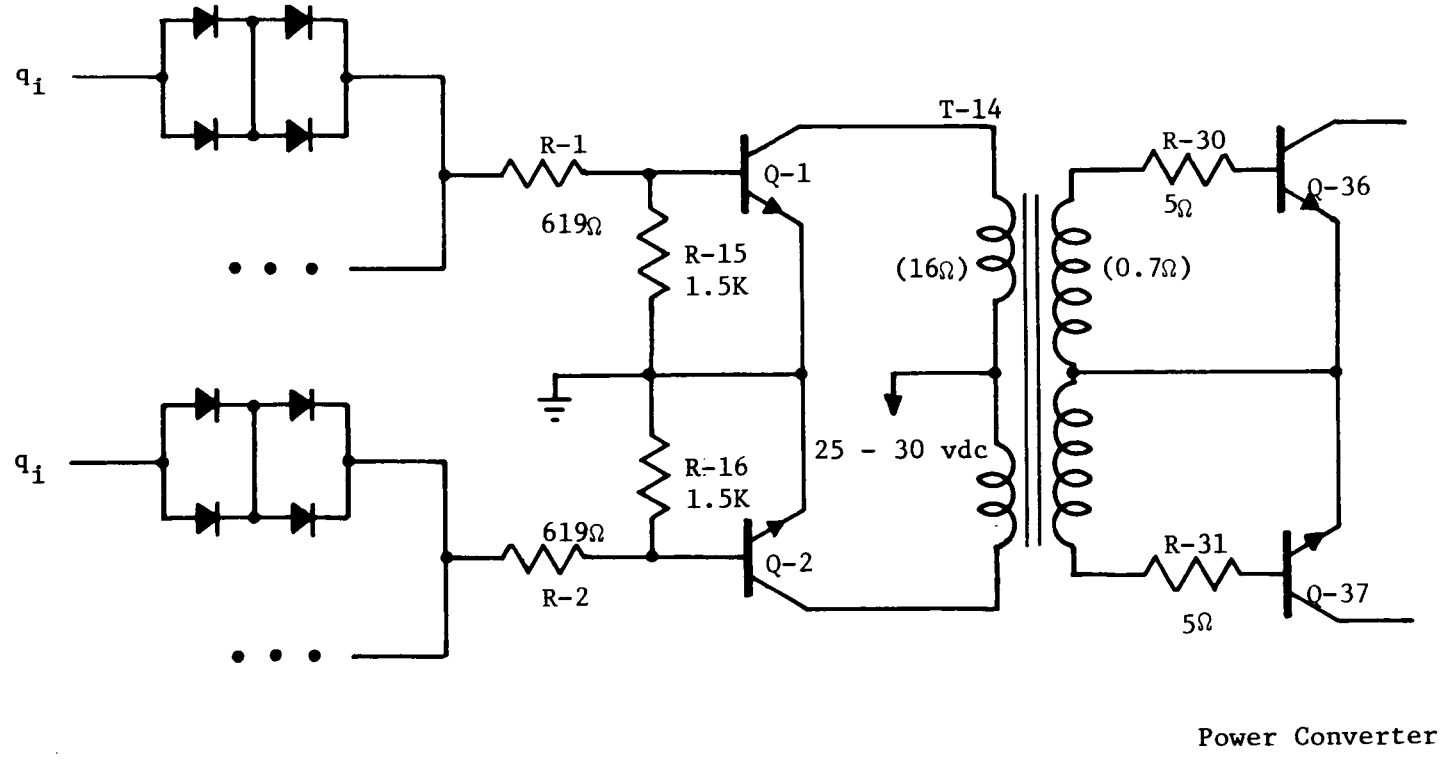


Figure 11. Timing Pulse Amplifier with Load

(1) Transistors Q1, Q2 (2N2034A)

(a) Maximum collector current requirement is

$$I_{c\ max} = \frac{30v}{16\Omega + 5.7\ (\frac{340}{54})^2\ \Omega} \cong 125\ ma,$$

$$I_{c\ max} < \text{Rated } I_c = 3\ \text{amps.}$$

(b) Using a 20% safety factor, it is required that $BV_{CER} > 1.2 \times 2 \times 30v = 72v.$

($R = 1.5k\Omega$)

Rated $BV_{CEO} = 70$ volts,

Rated $BV_{CES} = 120$ volts.

The actual BV_{CER} for $R = 1.5\ k\Omega$ is probably nearer the rated BV_{CES} than the rated BV_{CEO}. Also, if a 16% safety factor was used rather than 20%, the required breakdown voltage computed would have been 70 volts. There is considerable uncertainty in the 20% safety factor used above. It is a factor frequently used to provide for switching transients in saturable oscillator circuits and is probably excessive in this case since switching is not dependent on the transformer cores saturating. Switching transients have not been observed in the laboratory and the breadboard model has been operated successfully with a supply voltage in excess of 32 volts.

(c) For power dissipation considerations a generally accepted application rule is that transistors can switch approximately eight times the Class A power rating. The power dissipation requirements are

$$P_d = \frac{1}{8} \frac{(30v)^2}{16\Omega + 5.7(\frac{340}{54})\Omega} = 0.5\ \text{watts}$$

Rated P_d = 8.5 watts @ case temperature, $T_c = 25°C$,
= 5 watts @ $T_c = 100°C$,
= 0.6 watts @ ambient temperature, $T_A = 100°C$.

(d) Frequency requirements are considered adequate if the transistor gain corner frequency f_β (i.e., the frequency at which the gain $i_c(j\omega)/i_b(j\omega)$ yields 3 db attenuation from the β or dc value) is

$$f_\beta = 10 \times 400\ \text{cps} = 4\ \text{kc.}$$

The frequency for unity gain f_T of the 2N2034A is specified by the manufacturer as

$$\text{rated } f_T = 1 \text{ mc minimum.}$$

This is known to be several octaves, say 6, higher than f_β; therefore,

$$f_\beta \gg 4\text{kc}.$$

(e) Base current required to saturate the 2N2034A with I_c = 125 ma is

(i) $I_B < 5$ ma (from STC data bulletin),

(ii) I_B = 125 ma/20 = 6.25 ma (from worst-case h_{FE}),

(iii) I_B = 1.8 ma (from laboratory measured collector characteristics).

The worst-case h_{FE} is extremely pessimistic. The units measured in the laboratory proved to be uniform and to have higher gains. In the following analyses, the I_B = 1.8 ma determined from lab measurements will be used as criteria for successful performance.

A worst-case estimate of base drive current available is determined as follows.

The base drive source is the SN511A integrated circuits in the PSG. The linear output characteristics given by the manufacturer are included in Figure 8 as curve 1. Since the output characteristics are linear, the output can be represented by the Thevenin's equivalent shown below in Figure 12.

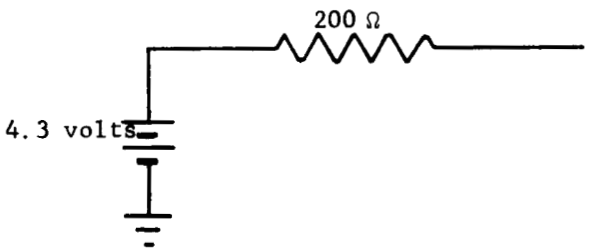


Figure 12. Equivalent circuit of the SN511A output characteristics.

The diode-quad shown in Figure 11 in the base circuit drops 1.4 volts at worst-case temperatures (T = 0°C) and the 2N2034A base-emitter junction drops 0.9 volts at I_B = 5 ma (mfg. data). Therefore,

$$I_{R1} = \frac{(4.3 - 1.4 - .9)\ v}{(619 + 200)\Omega} = 2.4 \text{ ma, and}$$

$$I_B = 2.4 \text{ ma} - 0.6 \text{ ma} = 1.8 \text{ ma.}$$

The base current available to the 2N2034A as determined from the preceding analysis is marginal at best. This analysis is realistic except for one modifying influence. The published output characteristics for the SN511A are pessimistic compared to the output characteristics of some SN511A units measured in the laboratory. However, some measured units did compare closely with the published data in the region of interest (see Figure 8).

The marginal drive conditions discussed in this section can be modified to a satisfactory situation by either reducing the resistance of R1 and R2 or by removing one parallel pair of diodes in the diode coupling to yield only a single diode drop. The cognizant design group has already resorted to the former method by reducing the resistance of R1 and R2 to 392Ω. Repeating the preceding calculation using this value for resistance,

$$I_{R1} = \frac{(4.3 - 1.4 - 0.9)v}{(392 + 200)\Omega} = 3.4 \text{ ma,}$$

and

$$I_B = (3.4 - 0.6) \text{ ma} = 2.8 \text{ ma}$$

which is adjudged adequate on the basis measured characteristics of the 2N2034A.

The other method of removing one parallel pair of diodes results in a base current estimated as before to be

$$I_{R1} = \frac{(4.3 - 0.7 - 0.9)v}{(619 + 200)\Omega} = 3.3 \text{ ma,}$$

and

$$I_B = (3.3 - 0.6) \text{ ma} = 2.7 \text{ ma}$$

which is also adequate. The use of a diode-quad vs. a single diode parallel pair in the base circuit is a point of contention from the point of view of reliability. Considering the predominant mode of failure to be "opens" and the primary function of the diode coupling to be isolation of the redundant timing channels, the single diode parallel pair has been shown to be more reliable. However, other modes of

failure and the effects on circuit performance must be appropriately considered before the question is finally resolved. This problem is currently being investigated with breadboard experimentation being used to compare the relative performance of different circuit configurations.

The circuit modifications as discussed above for obtaining the adequate base drive and the resulting current assumes that the power dissipation of the SN511A unit is not exceeded. The power dissipation capabilities of the SN511A were discussed in Section 2.4, and for purposes of analysis, point A in Figure 8 was assumed to represent the rated power dissipation.

(2) Resistors, R1, R2, R15, R16 [$\frac{1}{4}$ watt, derated to $\frac{1}{10}$ watt @ 100°C]

The maximum power dissipated by any resistor is

$$P_d < \frac{(4.3v)^2}{392} \approx 47 \text{ mw} < \frac{1}{10} \text{ w.}$$

(3) Diodes 1N645

Rated I_{ave} = 150 ma @ 150°C (.7v threshold devices).

The diode is more than adequate for the currents computed in (1) above.

(4) Transformer T14 [Core: CARP 49; -]

It is required that

$$\Delta B = \frac{E\Delta T}{NA_{fe}} < 2B_{sat},$$

where

E = 30 volts,

$\Delta T = \frac{1}{800\text{cps}}$ = 1.25 m sec,

N = 340 turns, and

B_{sat} = 10 k gauss (from core manufacturer's data).

A_{fe} is unknown for the computation above; however, experimental observations reveal that the transformer is adequate for the intended function.

(5) Other Considerations

One of the SN511A units in the PSG is required to drive a 2KΩ load, i.e., an electronic switch, in addition to the timing pulse amplifier, a very significant load compared to the TPA load. Consequently, the preceding estimates of available

base current must be modified for the one unit in question. Using an interative procedure, it is estimated that

$$I_{R1} = \frac{(3.5 - 1.4 - 0.9)v}{619\Omega} = 2.1 \text{ ma},$$

$$I_B = (2.1 - 6) \text{ ma} = 1.5 \text{ ma},$$

$$I_{sw} = \frac{3.6v}{2K\Omega} = 1.8 \text{ ma, and}$$

$$I_{FF} = I_{R1} + I_{sw} = (2.1 + 1.8)\text{ma} = 3.9 \text{ ma}.$$

which corresponds to 3.6 volts out of the driving flip-flop. From this analysis, it is concluded that the base drive current is not adequate (based on the 1.8 ma required). In the region of 3.6 volts, all of the SN511A measured characteristics are more optimistic than the output characteristics published by the manufacturer and used in the preceding analysis. Without a more extensive study of the SN511A, there is no strong justification for assuming the more optimistic, measured characteristics.

Still using the manufacturer's published SN511A output characteristics, the following estimate is made assuming one of the diode parallel pairs is removed from the circuit.

$$I_{R1} = \frac{(3.4 - 0.7 - 0.9)v}{619\Omega} = 2.9 \text{ ma},$$

$$I_B = (2.9 - .6)\text{ma} = 2.3 \text{ ma},$$

$$I_{sw} = \frac{3.4v}{2K\Omega} = 1.7 \text{ ma, and}$$

$$I_{FF} = (2.9 + 1.7) \text{ ma} = 4.6 \text{ ma}.$$

Consequently, based on the required 1.8 ma base current the removal of one parallel pair of diodes will render the timing pulse amplifier satisfactory since the SN511A will adequately saturate the 2N2034A transistors with the additional load of the electronic switch.

An additional estimate of the 2N2034A base current is computed below assuming that R1 and R2 are changed to 392Ω.

$$I_{R1} = \frac{(3.4 - 1.4 - 0.9)v}{392\Omega} = 2.8 \text{ ma},$$

$$I_B = (2.8 - .6) \text{ ma} = 2.2 \text{ ma},$$

$$I_{sw} = \frac{3.4v}{2K\Omega} = 1.7 \text{ ma, and}$$

$$I_{FF} = (2.8 + 1.7) \text{ ma} = 4.5 \text{ ma}.$$

Based on the 1.8 ma required base current, this modification is also adequate.

(6) Conclusions

From the preceding considerations, it is concluded that either of the modifications in the TPA design is adequate to provide sufficient base current to saturate the 2N2034A transistors. The original design was marginal at best for the TPA units that were driven as the only load from an SN511A network, and inadequate in the single case in which the driving SN511A network was also loaded by the electronic switch. The preference of the two modifications considering both performance and life is being investigated.

It is assumed here that the added load represented by removing a diode pair or reducing R1 and R2 will not cause the driving SN511A units to exceed their rated dissipation, since the operating point is below "A" in Figure 8.

2.8 Power Converter Stage

Figure 13 is a schematic diagram of one of the six power converter stages. Each stage must convert an equal amount of power and, if an efficiency of 80% is assumed for the power section of the inverter, each stage must convert approximately

$$\frac{250 \text{ va}}{6 \times 0.8} = 52 \text{ va}.$$

(1) Transistors Q36, Q37 (2N1016D)

(a) Transistors Q36 and Q37 must block twice the maximum controlled dc supply voltage. Adding a 20% safety factor, it is required that

$$BV_{CEO} = 2 \times 23 \times 1.2 = 55 \text{ volts}.$$

$$\text{Rated } BV_{CEO} > 200 \text{ volts to } 150°C.$$

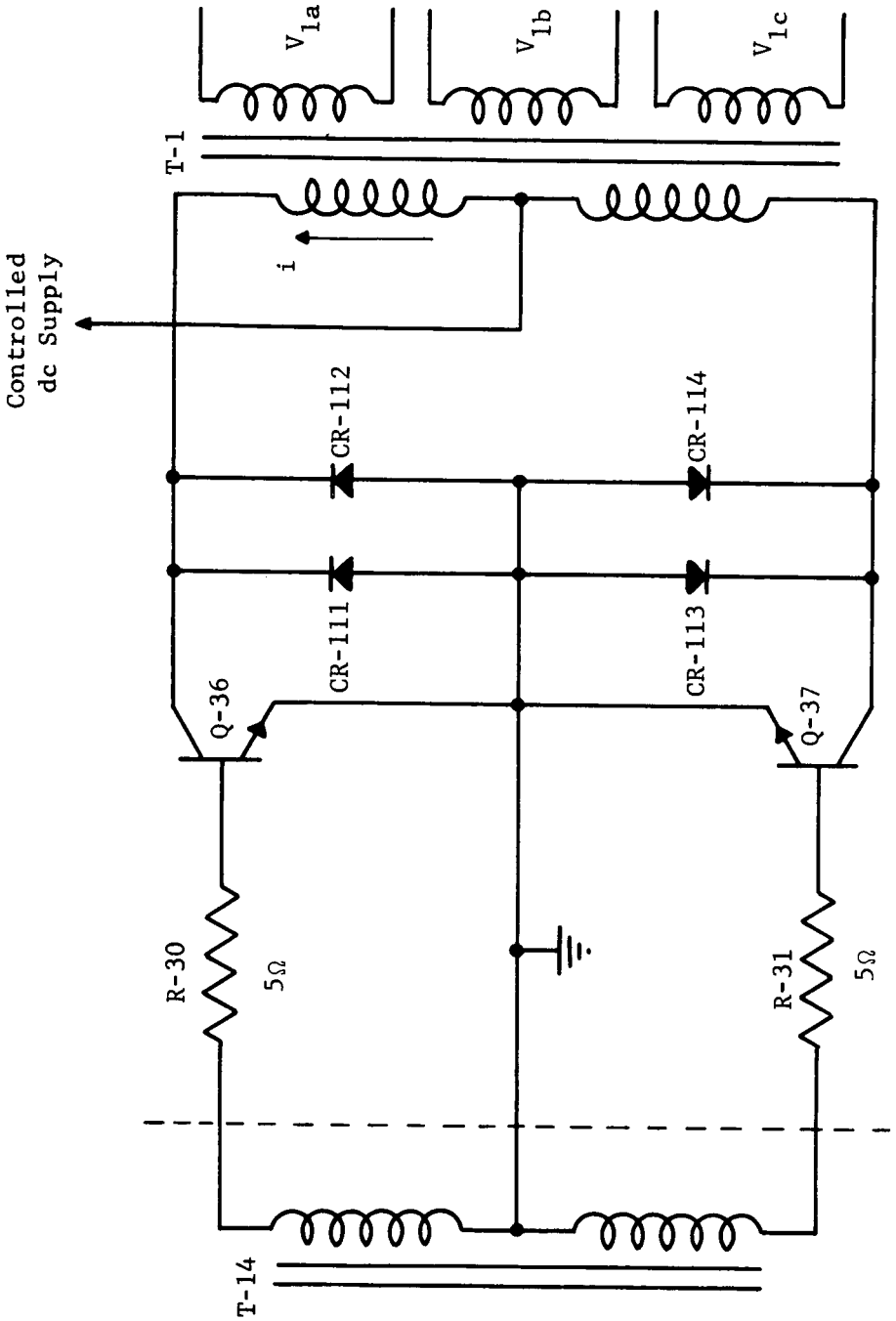


Figure 13. Power Converter Stage

(b) Using the criteria that a transistor can switch 8 times its Class A power rating, the transistor power rating must be

$$P_d \geq \frac{52}{8} \approx 6.5 \text{ watts.}$$

The 2N1016D power ratings are

$$P_d = 150 \text{ watts at } 45°C,$$

$$= 10 \text{ watts at } 140°C.$$

(c) The power transistors are switching at 400 cps. Consequently, it is desirable that

$$f_\beta = 10 \times 400 \text{ cps} = 4\text{kc.}$$

$$\text{Rated } f_\beta = 30 \text{ kc.}$$

(d) Collector current requirements are

$$I_c = \frac{52 \text{ va}}{19\text{v} \times 2} \approx 1.4 \text{ amps average/transistor.}$$

The major component of each of the three secondary currents is a 400 cps sinusoid current. These three currents seem to provide a net mmf in the secondary of each output transformer that is also sinusoidal. Consequently, the primary mmf is also sinusoidal and the peak collector current is estimated as

$$I_{C \text{ peak}} = \frac{52 \text{ va}}{19\text{v}} \times \frac{1}{.637} = 4.3 \text{ amps peak.}$$

This estimated is improved by considering the saturation voltage. At $I_c = 4.3$ amps, $V_{CE(sat)} = 0.8$ volts (from mfg. bulletin) and

$$I_{C \text{ peak}} = \frac{52 \text{ va}}{(18.2\text{v})\ (.637)} \approx 4.5 \text{ amps peak.}$$

$$\text{2N1016D rated } I_C = 7.5 \text{ amperes average.}$$

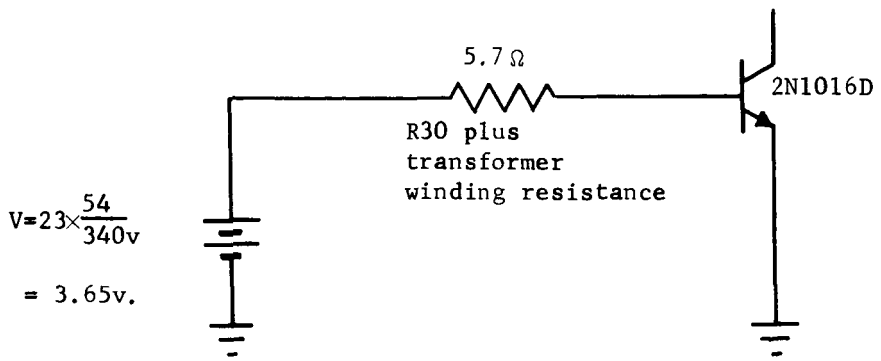
It is concluded from the preceding considerations that the 2N1016D transistors are more than adequate for the power converter application. The excess BV_{CEO}

rating also contributes to an increased $V_{CE(sat)}$ and, consequently, increased power loss, but the increase is considered insignificant.

(e) Consider the 2N1016D base drive circuit. The minimum $N \frac{d\Phi}{dt}$ in the R1020 primary is

$$25v - V_{CE(sat)} - I_c R_{R1020} \approx 23v,$$

where $V_{CE(sat)}$ and I_c refer to Q1 and Q2 in the TPA unit. Consequently, the Q36 base drive circuit can be represented as shown below.



Using a worst-case value for V_{BE} of 1.1 volts,

$$I_B = \frac{(3.65 - 1.1)v}{5.7\Omega} = 450 \text{ ma.}$$

From the 2N1016D collector characteristics the base current required to saturate the 2N1016D for a collector current of 4.5 amps is

$$I_B \approx 300 \text{ ma.}$$

The available base drive is more than adequate. The power dissipated in the 5Ω resistors, R30 and R31, can be reduced, however, without reducing the base drive current. For example, if the criterion is used that the voltage drop in the base current-limiting resistor should be approximately equal to the base-emitter voltage drop, the secondary turns on R1020 and the 5Ω resistors could be reduced without changing the base current.

(2) Diodes, CR111, CR114, (1N645)

For a given inverter load, the approximate relationship between the output transformer primary current and voltage is illustrated in Figure 14. This assumes that the current is sinusoidal resulting from sinusoidal currents in the secondary windings as previously described under (d) above. Under worst-case, zero power factor load conditions for the individual converter stages, the reactive diodes are required to conduct for 1/2 of each switching cycle as illustrated in Figure 14, conducting the peak primary currents. (The angle θ in Figure 14 cannot be interpreted as the power factor angle defined by the inverter external load.) Under these conditions, the peak current in each parallel-pair of 1N645 diodes is the same as the $I_{C\ peak}$ for the transistor, and as computed above

$$I_{peak} = I_{C\ peak} = 4.5 \text{ amps.}$$

The average current is the time average of the current conducted over the full cycle.

$$I_{ave} = \frac{1}{2\pi} \int_{\circ}^{\pi/2} I_{peak} \sin x \, dx \cong 700 \text{ ma.}$$

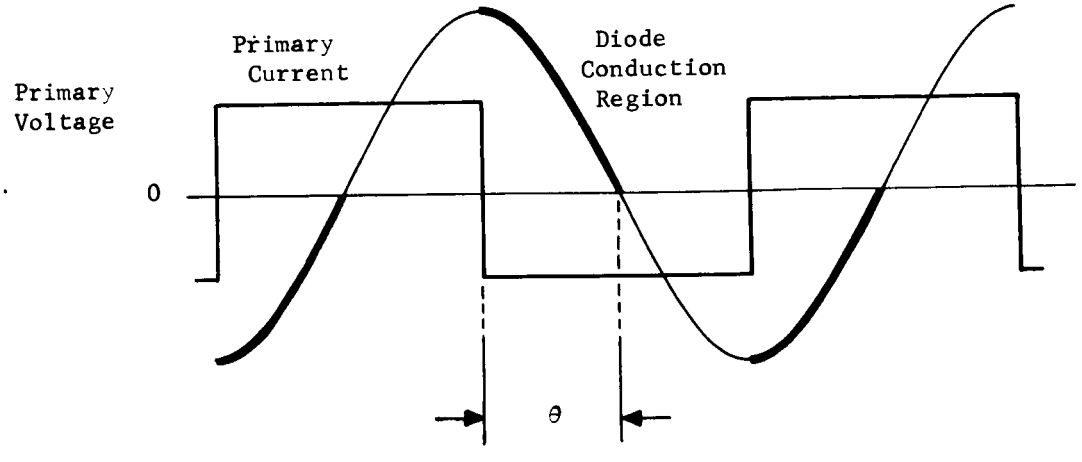


Figure 14. V-I relationship in the output transformer primary

With no inverter external load the output filter (see section 2.9) is highly capacitive. Experimentally observed values of parallel-pair diode currents at these low power factor conditions are

$$I_{peak} = 1.2 \text{ amps, and}$$

$$I_{ave} = 680 \text{ ma.}$$

For these conditions the current waveforms are not truly sinusoidal as previously considered. For other external load conditions, i.e., capacitive loads, the diode currents have been observed to peak at 3 amps while the average decreased

The 1N645 diode is rated as follows:

$$I_{peak} = 1.25 \text{ amps recurrent,}$$

$$I_{surge} = 3 \text{ amps, and}$$

$$I_{ave} = 400 \text{ ma @ } 25°C;$$
$$= 250 \text{ ma @ } 100°C.$$

It is concluded that, based on the manufacturer's ratings, the two paralleled diodes are not adequately rated for the power converter stage application. An obvious recommendation is to replace the paralleled diodes with a single diode of the required capacity. Otherwise, the failure of one diode will cause the probability of failure of the parallel unit to approach unity. Extended operation of the inverter breadboard under specified conditions has yet to produce a failure in these diodes.

(3) Resistors, R30, R31 (5 watts, derated to 3.5 watts at 100°C)

The maximum power dissipated is

$$P_d \leq \frac{(30 \cdot \frac{54}{340} v)^2}{5.7\Omega} = 3.7 \text{ watts.}$$

(4) Transformer, T1

Since information on the transformers is currently unavailable some comments follow. The equation of significance in the design of T1 is

$$V_{dc} = N_p \frac{d\Phi}{dt} = N_p A_{fe} \frac{\Delta B}{\Delta T}$$

where V_{dc} is the controlled dc supplied to the power converter stage. For maximum efficiency, the value of V_{dc} should be as large as possible. The power converted by the converter varies with $V_{dc} I_C$, and increasing V_{dc} permits a corresponding

decrease in I_C. The power dissipated in Q35 and Q36 is independent of V_{dc}, but varies directly with I_C. The base drive requirements can also be reduced with I_C. In practice, V_{dc} must be less than 25 volts because the specifications permit the input voltage to reduce to 25 volts and the switching mode regulator will reduce this value further when operating at its maximum output (the magnetic amplifier cannot be 100% modulated because of roundness in the mag amp cores). A realistic estimate of the maximum V_{dc} is 22 volts, and this value will occur at maximum inverter external load. ΔT is fixed by the frequency of operation of the inverter, and is equal to

$$\frac{1}{2} \times \frac{1}{400} = 1.25 \text{ m sec.}$$

ΔB is limited to a value less than $2 \times B_{sat}$, the saturation flux density of the core material. By increasing ΔB, the area of the core, A_{fe}, and/or the number of primary turns, N_p, can be reduced. The material used in this application is Magnetics' Orthonal. There are other materials with equivalent loop widths and larger values of B_{sat}, e.g., Magnetics' Supermendure with $B_{sat} > 20$ kilogausses, but the use of Orthonal does not detract from the reliability of the converter stage.

Over a large range of values, $N_p A_{fe}$ does not contain uniquely optimum values for N_p and A_{fe}. Large values of N have the negative effects of increasing winding capacitance and resistance, and the positive effect of decreasing the magnetizing current. At 400 cps, experience has indicated that $N_p < 1000$ turns is a good empirical rule.

The Magnetics Inc., tape wound core No. 51078-2A used in the power converter stage application is not listed in the Magnetics' Catalogue (TWC-300). Laboratory observations show the core to be of adequate size.

2.9 The Output Circuit

A simplified schematic diagram of the output circuit is shown in Figure 15. The three-phase delta connection on the left represents the interconnection of the eighteen secondary windings of the output transformers. This interconnection is illustrated in more detail in Figure 2.4 of reference 1.

(1) Inductors; L1, L2, and L3

Core: Pwd. iron, D-082168-3

100 turns, #20 wire

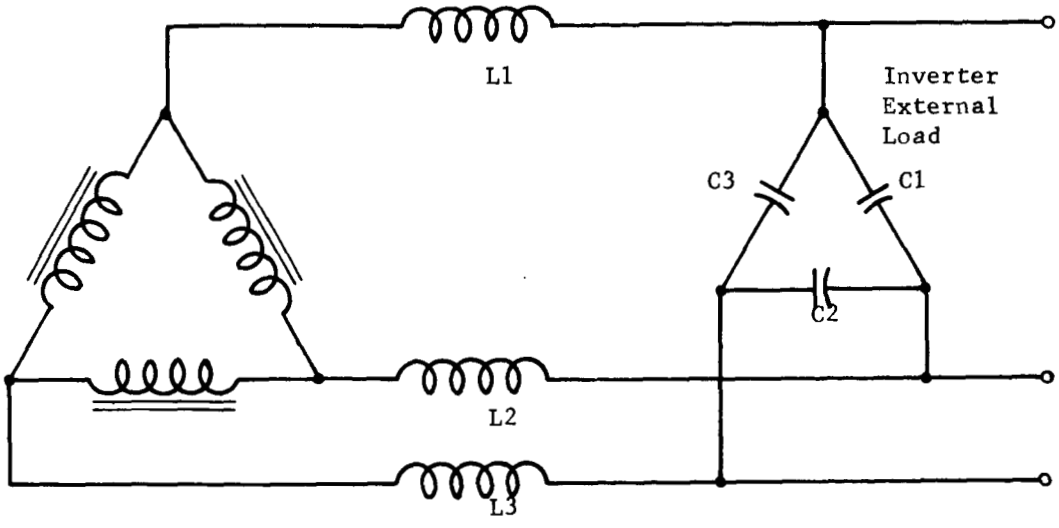


Figure 15. The Output Circuit

From Arnold Bulletin No. 6C-106C,

O.D. = 1.57 in

I.D. = 0.95 in $\qquad \mu = 125$

H = 0.57 in $\qquad$ L = 168 mh/1000 turn winding

$$L = 168 \text{ mh } \left(\frac{100}{1000}\right)^2 = 1.68 \text{ mh.}$$

In order that the cores not saturate, it is important that the mmf not exceed 100 oersteds, where the mmf of the cores is represented by

$$H = \frac{0.4\pi \text{ NI}}{\ell} .$$

From the above dimensions ℓ is computed as follows. The average radius of the core is

$$r = \frac{(1.57 + 0.95) \text{ in}}{4} = 0.63 \text{ in} = 1.6 \text{ cm.}$$

Then

$$\ell = 2\pi r \cong 10 \text{ cm.}$$

Therefore, the line current must not exceed

$$I = \frac{(100)\ (10)}{0.4\pi\ (100)} \simeq 8 \text{ amperes.}$$

At the inverter rated load of 250 va the line currents for a balanced resistive load are

$$I = \frac{250 \text{ va}}{\sqrt{3} \times 115\text{v}} = 1.25 \text{ amps.}$$

(2) Capacitors: C1, C2, C3; 400 volts, 2μF ± 10% (Sprague 118P20594T4). Peak voltage across these capacitors is

$$V_{peak} = \sqrt{2} \times 115 \text{ vac} = 163 \text{ v.}$$

(3) The LC Filter.

Inductors L1, L2, L3 and capacitors C1, C2, C3 connected as illustrated in Figure 15 form a three-phase filter which serves to attenuate the harmonics of the 400 cps fundamental component contained in the output waveforms. This filtering action was discussed in detail in the Appendix of Reference 1. For the balanced circuit with $L_1 = L_2 = L_3 = L$ and $C_1 = C_2 = C_3 = C$ with either no load or a balanced resistive load the filter transfer function was shown to be quadratic with the resonant frequency nominally

$$f_R = \frac{1}{2\pi} \frac{1}{\sqrt{3LC}} \approx 1600 \text{ cps.}$$

The relative distortion of the nominal stepped voltage waveform from the power transformers was computed in Reference 1 as 15.25%. At rated balanced, resistive load conditions the filter was shown to reduce the distortion to approximately 1.7%. Inverter specifications require that the relative distortion be less than 5%. At these load conditions the output filter is more than adequate. The filter operation at other load conditions including reactive loads and unbalanced loads is currently being extensively investigated by a computer program for handling the more complicated expressions.

The loads which the inverter will drive are anticipated to be inductive. The output filter is purposely designed as a capacitive output impedance to provide a power factor correction when the inverter is driving inductive loads. For example, calculations have shown that for a rated load of 250 va with the current leading the voltage by 45 degrees the power factor of the combined filter and load is

approximately unity. Thus, at these conditions the inverter operates more efficiently as a power source.

2.10 The 20-volt Regulated Supply

A schematic diagram of the 20-volt regulated supply is shown in Figure 16. During normal operation of the inverter the 20-volt regulated supply supplies current to only the center tap of transformer T7 as illustrated in Figure 17. The secondary turns of T7 serve as the voltage source for the gate voltage of the magnetic amplifier as further illustrated in Figure 18. The worst-case load to the 20-volt regulated supply occurs when the magnetic amplifier is 100% modulated and is just the maximum equivalent resistance of the magnetic amplifier gate circuit reflected back through T7. This is

$$\frac{R67 \quad R69}{R67 + R69} \left(\frac{100}{60}\right)^2 = \frac{(100\Omega) \quad (150\Omega)}{(100 + 150)\ \Omega} \left(\frac{100}{60}\right)^2 = 167\Omega \ .$$

The maximum load current is then

$$I_{max} = \frac{20\ v}{167\Omega} = 120\ ma.$$

During the over-current protection mode of inverter operation the magnetic amplifier modulation is reduced to near zero by the over current protection circuit. The load on the 20-volt regulated supply as provided by the magnetic amplifier gate circuit is negligible in comparison to that computed above. During this mode of operation; however, the 20-volt regulated supply is required to deliver current to the over-current protection circuit via the magnetic amplifier control winding as shown in Figure 19, page . The measured resistance of the magnetic amplifier control winding is 100Ω ; therefore, current during the over-current protection mode is

$$I_{ocp} = \frac{20\ v}{1.1k\Omega} = 18.2\ ma.$$

(1) Zener diode CR152, (20v, 10 watt)

The maximum power dissipation is

$$P_{max} = V_z I_z = 20\ v\ \frac{(30 - 20)v}{33\Omega} \simeq 6\ watts.$$

The diode is thus adequate.

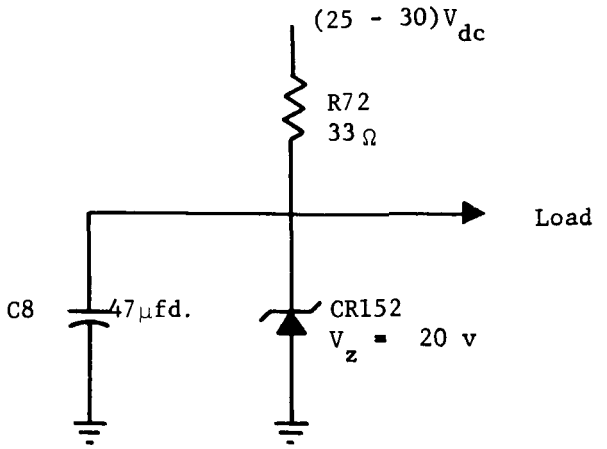


Figure 16. The 20-volt Regulated Supply

(2) Resistor R72 (33Ω, 15 watts derated to 9 watts at 125°C)

The maximum power dissipation is

$$P_{max} = \frac{(30v - 20v)^2}{33\Omega} \simeq 3 \text{ watts.}$$

Using the lower input voltage requirement of 25 vdc to determine if the minimum available current is adequate to supply the required load current,

$$I_L = 120 \text{ ma} < I_{min} = \frac{(25 - 20)v}{33\ \Omega} = 152 \text{ ma;}$$

$$120 \text{ ma} < 152 \text{ ma.}$$

(3) Capacitor C8 (47 μf, 35 v)

Some filtering is required on the 20-volt supply output because of the periodic (9.6kc) demand of the normal load. The voltage rating is adequate and, from experimental observations, the capacitance is also adequate.

2.11 Magnetic Amplifier Driver

A schematic of the magnetic amplifier driver stage is shown in Figure 17. This circuit functions to supply the gate excitation required for magnetic amplifier operation.

(1) Transistors Q17, Q18 (RCA S2N2102)

(a) Maximum collector current requirement is 120 ma as computed in Section 2.10 above.

$$\text{Rated } I_C = 1 \text{ amp.}$$

(b) Using a safety factor of 20% it is required that

$$BV_{CER} > 1.2 \times 2 \times 20 = 48v.$$

$$\text{Rated } BV_{CEO} = 65v.$$

(c) Using the application rule that a transistor can switch eight times its Class A power rating, the power dissipation requirements are

$$P_d = \frac{1}{8} (20 \text{ v}) (120 \text{ ma}) = 300 \text{ mw.}$$

$$\text{Rated } P_d = 500 \text{ mw at } 100°C.$$

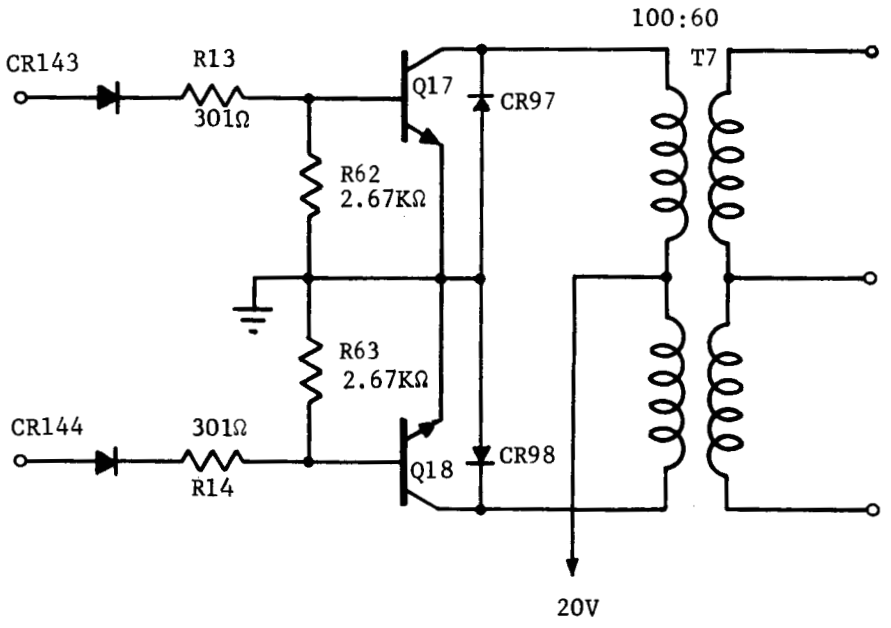


Figure 17. The Magnetic Amplifier Drive Stage

(d) Using the same argument for frequency requirements as presented in Section 2.7, the required f_β is

$$f_\beta = 10 \times 4.8 \text{ kc} = 48 \text{ kc.}$$

$$\text{Rated } f_\alpha = 60 \text{ mcs.}$$

Since $f_\beta \approx f_\alpha/100$, the frequency requirements are adequately met.

(e) The base current required to saturate the 2N2102 for the 120 ma collector current is

(i) I_B = 5 ma at 100°C (manufacturer's typical collector characteristics).

(ii) I_B = 4 ma (from laboratory measured collector characteristics).

The base of transistors Q17 and Q18 are driven by an SN511A unit in the frequency countdown circuit. Using the manufacturer's SN511A output characteristics as shown in Figure 8, page , and assuming 0.7 volts for the forward drop of the diodes and the transistor base emitter junction the actual base current is estimated as follows.

$$I_{R13} = \frac{(4.3 - 1.4)v}{(301 + 200)\ \Omega} = 5.8 \text{ ma, and}$$

$$I_B = 6 \text{ ma} - \frac{0.7 \text{ v}}{2.67 \text{ K}\Omega} = 5.54 \text{ ma.}$$

Based on the manufacturer's published characteristics the base current as computed above is marginal. However, the measured characteristics at high temperature show the transistors to have higher gains than claimed by the manufacturer and the available current to be adequate. From manufacturer's characteristic curves, a base current as low as 4 ma can be tolerated without any significant increase in V_{CE} above $V_{CE\ sat}$. These transistors should be screened to insure that they have higher gains than the minimum claimed by the manufacturer, and it is probable that this is done through the S-type specification.

(2) Diodes CR143, CR144 (1N645 - 400 v PIV, 150 ma at 150°C).

These diodes are more than adequate for the currents computed in (1) above.

(3) Resistors R13, R14, R62, R63 (1/4 watt derated to 1/10 watt at 125°C).

The maximum power dissipated by any of these resistors is

$$P_d < \frac{(4.3)^2}{301\Omega} \simeq 62 \text{ mw} < \frac{1}{10} \text{ watt.}$$

(4) Diodes CR97, CR98 (1N645, 400 v PIV, 150 ma at 150°C)

The current conducted by these diodes will be less than the 120 ma maximum collector current computed for the transistor; therefore, the diodes are adequate.

(5) Transformer T7

For the transformer application it is required that

$$\Delta B = \frac{E\Delta t}{NA_{fe}} < 2B_{sat},$$

where

$E = 30$ volts,

$\Delta T = 1/4.8\text{kc} = 0.2083$ msec,

$N = 100$ turns, and

$B_{sat} = 10^4$ gauss.

A_{fe} is unknown for the computation above; however, experimental observations reveal that the transformer is adequate for the intended function.

2.12 Magnetic Amplifier Circuit

A schematic diagram of the magnetic amplifier circuit is shown in Figure 18. The operation of the circuit is described in detail in Reference 1.

(1) Transistors Q13, Q14 (2N2034A)

(a) The maximum collector current requirement is estimated as follows. Assuming 0.6v for each of the forward drops in diodes CR149 and CR150 and transistor Q19 base to emitter junction, the maximum output current to the primary voltage regulator is

$$I_{max} = \frac{30v(\frac{13}{100}) - 1.2v}{1\Omega} = 2.7 \text{ amp.}$$

The corresponding collector current in Q13 and Q14 is

$$I_C = 2.7 \text{ amp} \times \frac{13}{100} \simeq 350 \text{ ma.}$$

$$\text{Rated } I_C = 3 \text{ amps.}$$

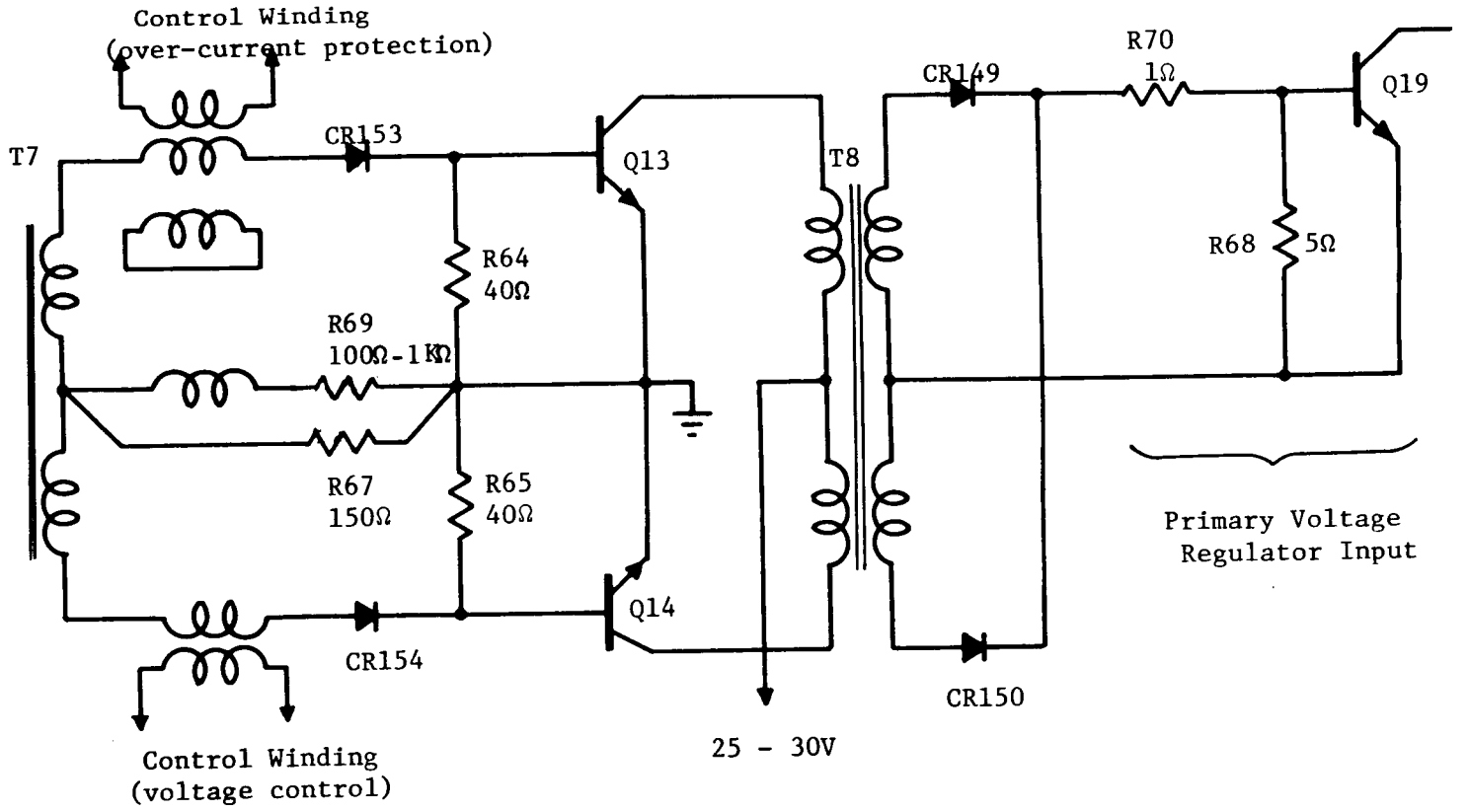


Figure 18. Magnetic Amplifier Circuit

(b) Assuming a safety factor of 20%,

Required $BV_{CER} = 2 \times 30 \times 1.2 = 72v$,

Rated $BV_{CEO} = 70v$, and

Rated $BV_{CES} = 80v$.

The comparison above appears unsatisfactory. The following considerations favorably modify the conclusion of (b). BV_{CEO} is a worst-case rating for the application considered here. The actual parameter of interest is BV_{CER} for an emitter-base resistance of 40 ohms. BV_{CER} will be greater than BV_{CEO} and less than BV_{CES}. Also, the 20% safety factor used in determining the required BV_{CEO} is a factor frequently used to provide for switching transients in saturating oscillator circuits. Some safety factor is desirable, but 20% is probably excessive since this is not a saturating application. It is concluded that the transistors have an adequate voltage rating.

(c) Using the application rule that a transistor can switch eight times its Class A power rating, the power dissipation requirements are

$$P_d = \frac{1}{8} \frac{(30v)^2}{(\frac{100}{13})^2 \times 1\Omega} = 1.9 \text{ watts}$$

$$\text{Rated } P_d = 5 \text{ watts}, \; T_c = 100°C$$

$$= 0.3 \text{ watts}, \; T_A = 100°C$$

The comparison in (c) is also unfavorable, and a thermal analysis of the completed system is required to estimate the actual thermal operating point of the transistor. A more rigorous estimate of the power dissipation required of the transistor will be made in subsequent analyses. On the basis of the above analysis, however, it must be concluded that the transistor power rating is inadequate. The design should be justified on some other basis, e.g., an experimental study.

At high ambient temperatures, Q13 and Q14 have been observed to consistently fail through "thermal run-away" as the average current through the transistors approaches a maximum, i.e., the magnetic amplifier approaches 100% modulation. This reflects the inadequate power rating at high temperatures. A subsequent section of this memorandum will discuss this observed failure mode.

(d) Using the same argument for frequency requirements as presented in Section 2.7,

Required $f_\beta = 10 \times 4.8$ kc = 48 kc.

Rated $f_T = 1$ mc minimum,

and the frequency requirements are met.

(e) The base drive requirement for Q13 and Q14 as determined from the manufacturers' data bulletin is

$$I_B < 10 \text{ ma.}$$

The base drive current is estimated from an analysis of Figure 18 as follows. The total resistance in the base circuit during magnetic amplifier saturation is

$$R_T < 150\Omega + 100\Omega + 1.3\Omega \simeq 250\Omega .$$

An estimate of base current is then determined as

$$I_B > \frac{(12 - 1.5)v}{250\Omega} - \frac{0.8\ v}{40\Omega} \approx 22 \text{ ma.}$$

It is also required that the base drive current be negligible prior to the magnetic amplifier "turn-on" time. As a first approximation, the "off-time" base current is limited to the magnetizing current in the gate winding of the magnetic amplifier.

$$I_B \approx I_{mag} = \frac{H_c \ell}{N} = \frac{8 \times 4.5}{250} \times 10^{-2} \text{ amperes, or}$$

$$I_B < 1.4 \text{ ma.}$$

From the manufacturer's data it is established that the transistor conduction for this base current is negligible.

(2) Diodes CR153, CR154 [1N3730]

From manufacturer's ratings, at 100°C

$$I_f/V_f = 750 \text{ ma}/.9\text{v}$$

$$\text{PIV} = 100 \text{ volts.}$$

These characteristics are more than adequate.

(3) Resistors [minimum power rating is 3 watts]

The maximum power dissipated by any resistor is

$$P_d \ll \frac{(12v)^2}{2 \times 40} = 1.8 \text{ watts} < 3 \text{ watts}.$$

2.13 Voltage Error Detection Circuit

A schematic of the voltage error detection circuit is presented in Figure 19. The three-phase voltage detection process yields the ripple dc voltage at the bottom of the figure. The average value of the dc is computed by

$$V_{ave} = \frac{3V_m}{\pi} \int_{\frac{\pi}{3}}^{\frac{2\pi}{3}} \sin x \, dx = \frac{3}{\pi} V_m$$

and, for the nominal output inverter voltage of 115 vac rms V_{ave} becomes

$$V_{ave} = \frac{3 \cdot \sqrt{2} \cdot 115 \text{ v}}{\pi} = 156 \text{ v}.$$

(1) Resistors R73 [3 watts]

Assuming that R74 is set at its midpoint, the resistor currents indicated in Figure 19 can be estimated from the loop voltage equations as follows:

$$20100i_1 + 1200(i_1 - i_2) = 156, \text{ and}$$

$$100\, i_2 + 1200(i_2 - i_1) = -8.4$$

which yield

$$i_1 = 7.3 \text{ ma, and}$$

$$i_2 = -\, 0.31 \text{ ma}.$$

The power dissipation in R73 is

$$P_d = (7.3 \text{ ma} + 0.3 \text{ ma})^2 \, (1.1\text{k}\Omega) = 63.5 \text{ mw}.$$

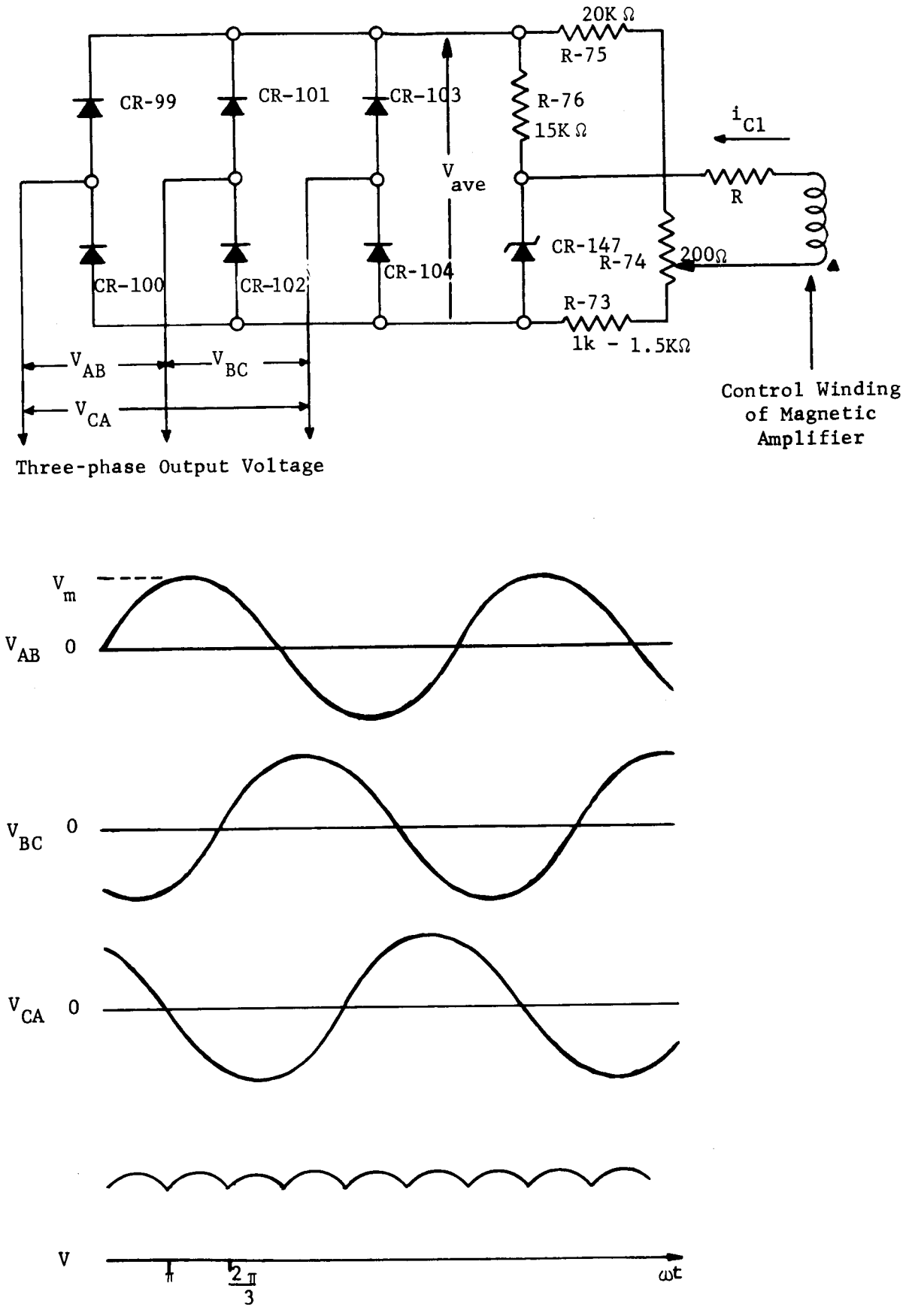


Figure 19. Voltage Error Detection Circuit and Associated Waveforms

(2) Resistor R75 [5 watt]

Using the currents computed in (1) above, the power dissipation in R75 is

$$P_d = (7.3 \text{ ma})^2 \ (20K\Omega) = 1.07 \text{ watt.}$$

(3) Potentiometer R74 [1.5 watt]

Assuming a worst-case condition when $i_2 = 0$, the maximum power dissipated in R74 is

$$P_d = (7.3 \text{ ma})^2 \ (200 \text{ ohms}) = 11 \text{ mw.}$$

(4) Resistor R76 [5 watt]

The power dissipation in R76 is

$$P_d = \frac{(156v - 8.4v)^2}{15K\Omega} = 1.4 \text{ watt.}$$

(5) Zener diode CR147[$V_z = 8.4v$]

The power dissipation is

$$P_d \approx 8.4 \text{ v } [\frac{(156 - 8.4)v}{15K\Omega} + 0.3 \text{ ma}] = 86.5 \text{ mw.}$$

(6) Diodes CR99 - CR104 [1N645]

Since the diodes share the current, the average current in any diode is

$$I_{ave} < \frac{1}{3} [\frac{156}{\frac{(15 \times 20)K\Omega^2}{35K\Omega}}] \approx 6 \text{ ma.}$$

The rated average current is 250 ma @ 100°C; therefore, the diodes are adequate.

2.14 Over-current Protection Circuit

A schematic diagram of the over-current detection circuit is presented in Figure 20. This circuit functions to detect high output currents that may potentially damage the inverter and provides a control signal to the magnetic amplifier to reduce the inverter output. The output currents are sensed by transformers T11, T12 and T13 the primary windings of which are located in the inverter output buses. Through the transformer turns ratio the low voltage drop

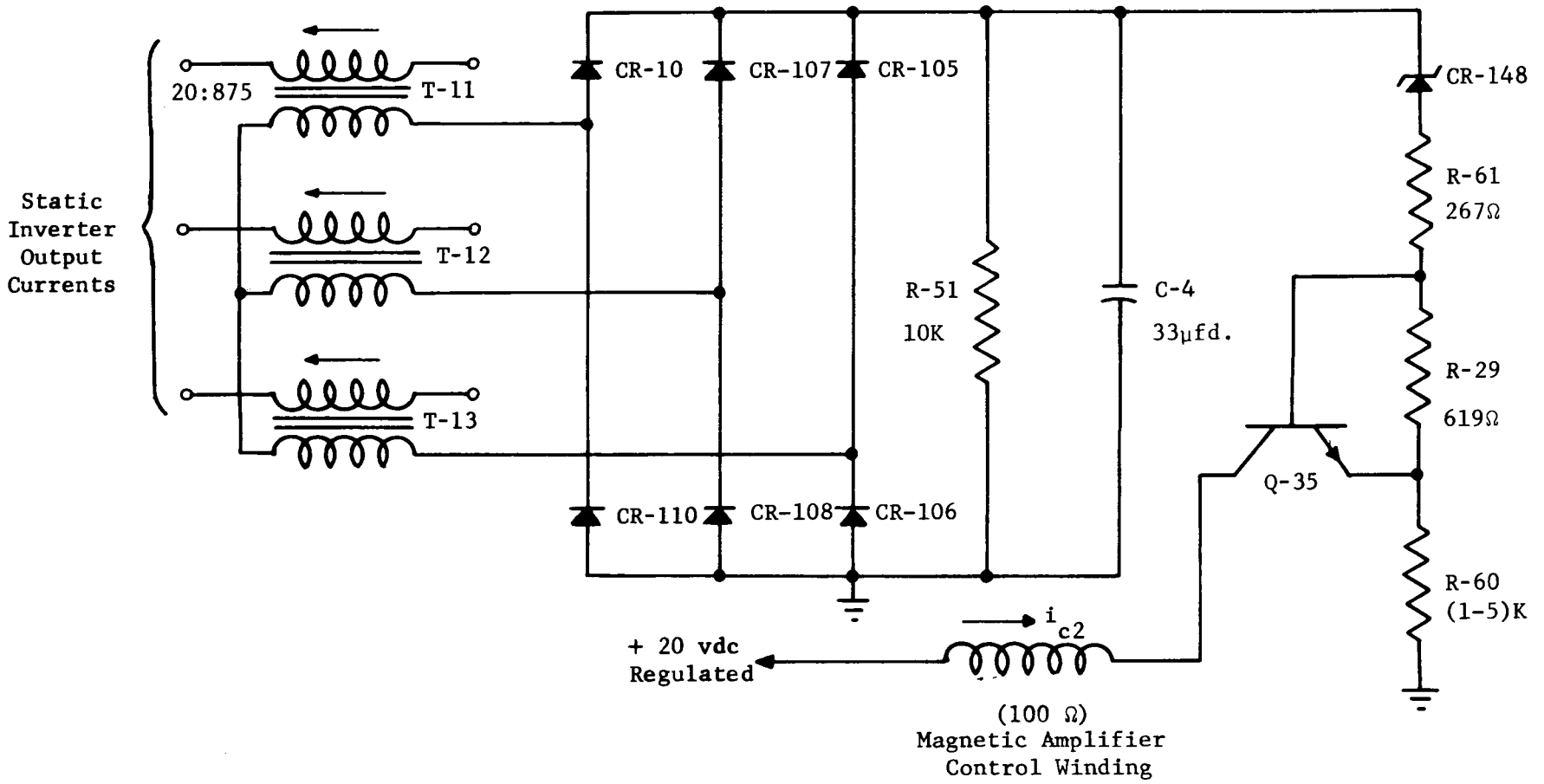


Figure 20. Over-current Detection Circuit

across the primary winding (which is proportional to the line current) is stepped up to a high voltage which is rectified in the three-phase rectifier circuit. The impedance of the primaries of these transformers is very low, as shown in (2) below, and negligible in comparison to the output filter chokes L1, L2 and L3; therefore, it was omitted from consideration in the output circuit of Section 2.9.

(1) Some initial considerations

(a) The C4 - R51 time constant is

$$\tau = 33 \times 10^{-6} \times 10^{4} = 330 \text{ msec.}$$

(b) The period of the ripple across the three-phase rectifier is

$$\tau_{3\Phi} = \frac{1}{6} \times \frac{1}{400} = 0.417 \text{ msec.}$$

(c) The period of a single phase ripple is

$$\tau_{1\Phi} = \frac{1}{400} = 2.5 \text{ msec.}$$

Since the C4-R51 time constant is long with respect to the three-phase rectifier ripple period for a single phase overload, the over-current detection circuit also functions as a protective circuit if only one line is overloaded. This is not too important, however, since the currents in the three output lines must sum to zero. It is sufficient to consider only the balanced overload case.

(2) Transformers T11, T12, T13 [MSFC 1158]

From manufacturer's data the core material provides for an inductance of 0.056 henries/10^3 turns. Therefore, the inductance of the primary winding is

$$L_p = .056 \text{ h } \left(\frac{20}{1000}\right)^2 = 22.4 \ \mu\text{h},$$

yielding an impedance of

$$Z_p = \omega L_p = 2\pi(400)\ (22.4 \times 10^{-6}\text{h}) = 56.3 \times 10^{-3} \text{ ohms.}$$

Thus the transformer primary voltage will be

$$V_p = 56.3 \times 10^{-3} \text{ volts/amp,}$$

and the transformer secondary voltage will be

$$V_s = (56.3 \times 10^{-3}) \left(\frac{875}{20}\right) = 2.46 \text{ volts/amp of line current.}$$

(3) Three-phase rectifier

The three-phase rectifier output voltage is equal to the maximum instantaneous difference between the maximum and minimum input voltages. The individual input voltages from the secondary windings of T11, T12 and T13 have the same phase relationship as the three voltage waveforms in Figure 19. The maximum instantaneous voltage difference can be obtained by considering the voltage in the interval $\frac{\pi}{6} < \omega t < \frac{\pi}{2}$, or

$$V_{ocp} = \sqrt{2}\, V_s \left[\sin\ \omega t - \sin\left(\omega t - \frac{2\pi}{3}\right)\right].$$

The maximum occurs when $\frac{dv}{dt} = 0$, or

$$\cos\ \omega t - \cos\left(\omega t - \frac{2\pi}{3}\right) = 0$$

which is only true at $\omega t = \pi/3$. Therefore,

$$V_{ocp} = \sqrt{2}\, V_s \left[\sin\frac{\pi}{3} - \sin\left(-\frac{\pi}{3}\right)\right]$$

$$= 2\sqrt{2}\, V_s \sin\frac{\pi}{3}$$

$$= 2\sqrt{2}\ (2.46 \text{ volt/amp}) \sin\frac{\pi}{3}$$

$$= 6.05 \text{ vdc/rms amp of line current.}$$

Experimentally, the output line currents have never been observed to exceed 2 amps. Accepting this as a worst-case value, the maximum three-phase rectifier output voltage is

$$V_{ocp} = (6.05 \text{ v/amp})\ (2 \text{ amp}) = 12.10 \text{ v.}$$

(4) Zener diode CR148 [1N3156A, V_z = 8.4 v, 400 mw.]

Since CR148 is an 8.4 volt zener, the threshold line current value for the over-current detection circuit is

$$I = \frac{8.4\ v}{6.05\ v/amp} = 1.39 \text{ rms amp of line current.}$$

The observed value of threshold current is 1.4 amps.
The maximum current through CR-148 is

$$I_z = \frac{(12.10 - 8.4)v}{(1K\Omega + 267)\ ohm} = 2.92 \text{ ma,}$$

and the maximum power dissipation is

$$P_d = V_z I_z = (8.4v)\ (2.92 \text{ ma}) = 24.5 \text{ mw.}$$

The power and current ratings are more than adequate.

(5) Resistors R29, R60, R61 [$\frac{1}{4}$ watt, derates to $\frac{1}{10}$ watt]

The maximum power dissipated in either of these resistors is determined by computing for R60

$$P_d = (2.92 \text{ ma})^2\ (5K\Omega) = 43 \text{ mw.}$$

Thus the $\frac{1}{4}$ watt rating for all resistors is adequate.

(6) Resistor R51[$\frac{1}{4}$ watt, derates to $\frac{1}{10}$ watt]

Using the maximum rectifier output voltage of 12.10 v, the power dissipation is

$$P_d = \frac{(12.10\ v)^2}{10K\Omega} = 14.6 \text{ mw.}$$

(7) Capacitor C4 [35 vdc]

For the maximum rectifier output voltage of 12.10 the voltage rating is adequate.

From the initial consideration in (1) above, the capacitance is adequate.

(8) Diodes CR105 - CR110 [1N645]

The maximum average current conducted by any diode is one-third the total output current from the bridge or

$$I_{ave} = \frac{1}{3}\ (\frac{12.10v}{10K\Omega} + 2.92 \text{ ma}) = 1.4 \text{ ma.}$$

Rated I_{ave} = 150 ma at 150°C.

(9) Transistor, Q35 [2N718A]

(a) The maximum collector current requirement was computed in section 2.10 to be 18.2 ma.

Rated I_C = 150 ma.

(b) Required BV_{CEO} = 20 volts.

Rated BV_{CEO} = 32 volts.

(c) The maximum possible power dissipation is

$$P_d = (18.2 \text{ ma})\ (20 \text{ volts}) = 364 \text{ mw}.$$

Rated dissipation at a case temperature of 100°C is

$$P_d = 1.0 \text{ watt}.$$

2.15 Primary Voltage Regulator

A schematic diagram of the primary voltage regulator is shown in Figure 21. The output of the magnetic amplifier circuit is supplied as base drive to the parallel transistor switches Q19, Q20 and Q21 which share the high current required by the output converters.

(1) Input filter

The input filter is composed of choke L4 and capacitor C5 and serves the primary purpose of isolating the input primary voltage bus from current transients induced by the heavy current switching at the 9.6 kc rate. Formal specifications for the inverter include no requirements pertaining to the amount of filtering to be included; however, it is obvious that some filtering is necessary to isolate the input bus from the 9.6 kcps.

(a) Inductor L4

Core Data; MoPerm B-070127-3 (Arnold Eng.)

μ = 125

OD = 1.3 in

ID = 0.785 in

h = 0.420 in (height)

A_{fe} = 0.666 cm^2

ℓ = 8.3 cm(mean magnetic path)

L = 127 mh/10^3 turns

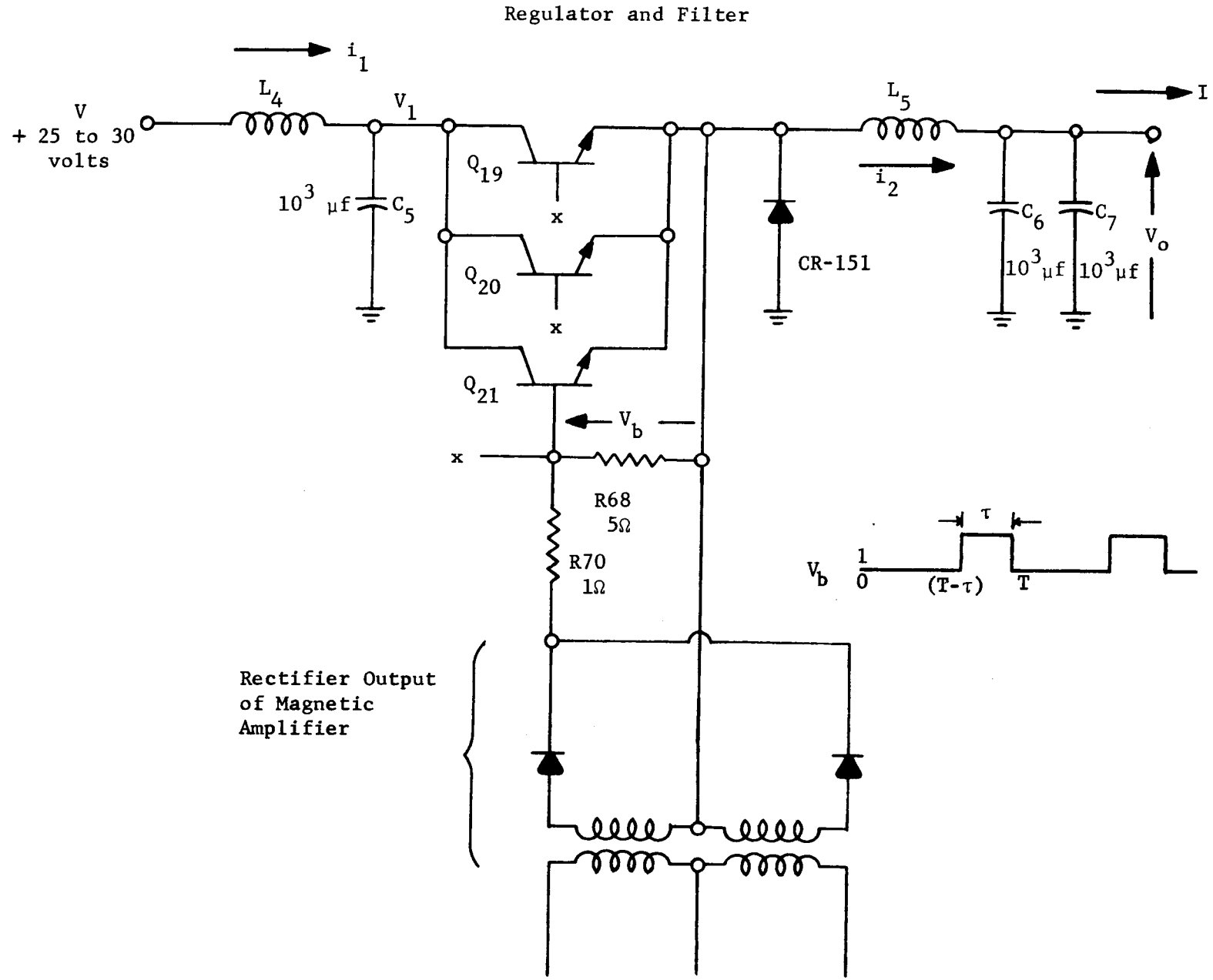


Figure 21. Voltage Regulator and Filter

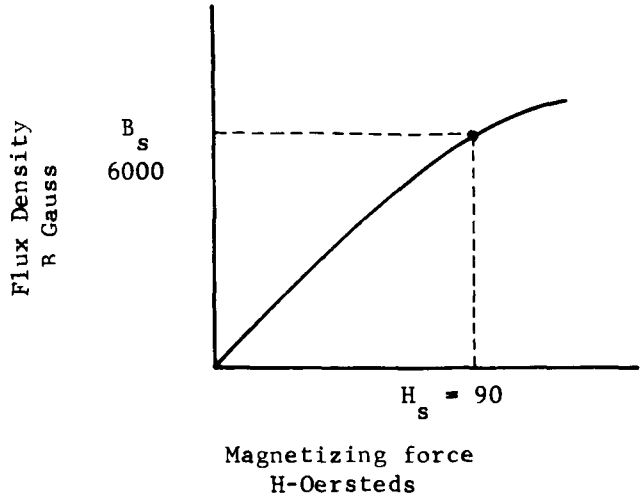


Figure 22. dc Magnetization Curve for MoPerm Material with μ = 125.

L_4 has 16 turns, therefore

$$L_4 = 127 \text{ mh } (\frac{16}{1000})^2 = 32.5 \ \mu\text{h}.$$

Assuming an efficiency of 75% for the inverter, the maximum operating point corresponds to a current of

$$I_o = \frac{250 \text{ va}}{25\text{v} \times 0.75} = 13.3 \text{ amps, and}$$

$$H_o = \frac{0.4 \text{ NI}}{\ell} = \frac{1.26 \times 16 \times 13.3}{8.3} = 32.10 \text{ Oersteds,}$$

or

$$H_o < 90 \text{ Oersteds (see Figure 22)}$$

(b) Capacitor C5

Sprague 202D108X9045A4

1000 μf, 45 volts

At 9.6 kc, a 1000 μf capacitor has a reactance of

$$X_c = 0.065 \text{ ohms.}$$

The capacitor is rated to withstand a 120 cycle ripple current of 1.8 amps rms.

Again assuming an efficiency of 75% with the input voltage at 30 volts an average current of

$$I_{ave} = \frac{250 \text{ va}}{30\text{v} \times .75} \approx 11 \text{ amperes}$$

flows through L4.

Under these conditions, the switching mode regulator is "ON" approximately 75% of the time, and the peak current through the switch (assuming I_{L4} a constant) is

$$I_{peak} = \frac{11}{.75} \approx 14.7 \text{ amperes.}$$

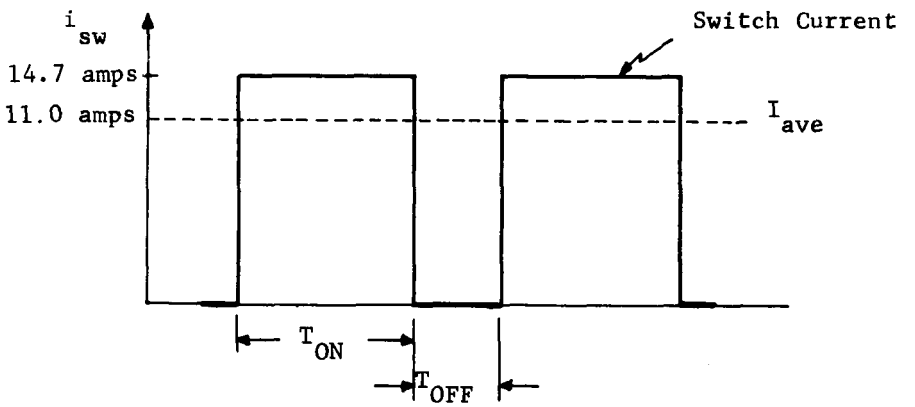
The switching period is

$$T = \frac{1}{9.6 \text{ kc}} = 104 \ \mu \text{ sec. and}$$

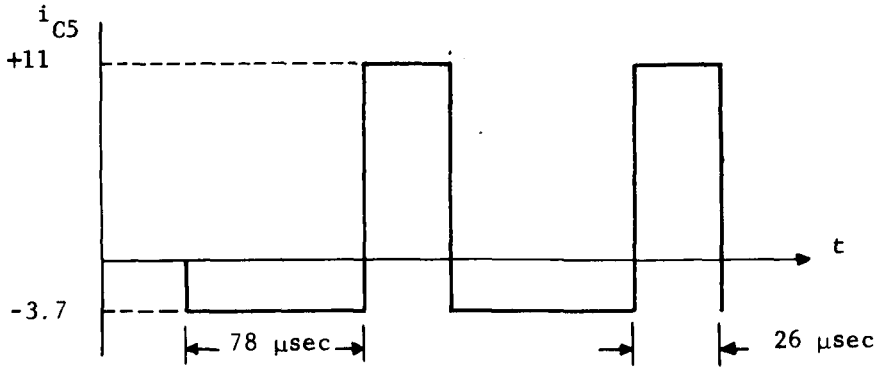
the ON period is

$$t_{ON} = .75 \times 104 = 78 \ \mu \text{ sec.}$$

The switch current is illustrated below, and, to a first approximation, the C5 capacitor current is the difference between the peak switch current and the average



L4 current. The current into C5 is thus as illustrated below.



Consequently, the rms ripple current in C5 is

$$I_{rms} = \frac{1}{104\ \mu\ sec}\ [(3.7\ amp)^2 \times 78\ \mu sec + (11\ amp)^2 \times 26\ \mu sec]^{1/2}$$

$$= 6.4\ amps.$$

This estimate of rms ripple current in C5 is pessimistic, principally because of the assumption of constant current in L4. It does indicate, however, that the ripple current in C5 is considerably more than the 1.8 amperes considered safe by the manufacturer. It seems advisable to replace C5 with a similar capacitor in a different case that has a higher ripple current rating. Such capacitors are available in the same Sprague type.

The measured rms ripple current in C5 is 5.3 amps. The ripple current is not independent of the source voltage characteristics, however.

If L4 has a constant current of 11 amperes, the voltage across C5 will increase above V_{in} by

$$V = \frac{1}{C} \int idt$$

$$= \frac{1}{10^{-3}} (11)\ \frac{1}{4}\ (104 \times 10^{-6})$$

$$= 0.286\ volts.$$

This is a negligible rise and illustrates that C5 can be considerably reduced. The principle mode of failure recognized for electrolytic capacitors is shorting, and furthermore, it is known empirically that the probability of failure of capacitors

is proportional to the capacitance. Therefore, potentially a significant contribution can be realized by reducing the capacitance of C5. This cannot be done independently of ripple current considerations, however.

The input filter attenuates frequencies above

$$f_r = \frac{1}{2\pi\sqrt{LC}} \approx 900 \text{ cps}$$

at about 12 db/oct.

(2) The Output Filter

The output filter smooths the pulse-width modulated input voltage to a near dc potential on the controlled dc bus (regulator output). A following section of this report will discuss the controlled dc bus in more detail.

(a) Inductor; L5

Core Data; MoPerm D-082168-3 (Arnold Engr.)

$\mu = 125$

OD = 1.57 in

ID = 0.950 in

h = 0.570 in (height)

$A_{fe} = 1.06 \text{ cm}^2$

$\ell = 10.1$ cm (mean magnetic path)

L = 168 mh/10^3 turns

L5 has 37 turns, therefore

$$L5 = 168 \left(\frac{37}{1000}\right)^2 \text{ mh} = 230 \ \mu\text{h}.$$

Assuming an inverter efficiency of 75%, the maximum operating point is estimated as follows.

$$I_o = \frac{250 \text{ va}}{20\text{v} \times .75} = 16.7 \text{ amps, and}$$

$$H_o = \frac{0.4 \ NI}{\ell} = \frac{1.26 \times 37 \times 16.7}{10.11} = 72 \text{ Oersteds,}$$

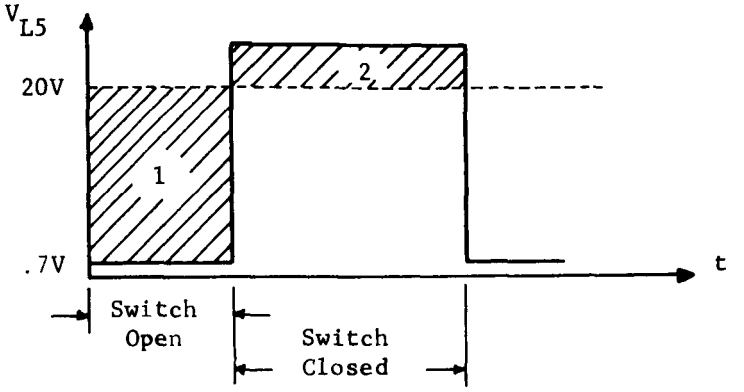
or

$$H_o < 90 \text{ Oersteds (see Figure 22).}$$

A critical consideration for L5 is that the inductor not "bottom", i.e., H become zero, at minimum loads. If L5 does bottom the output filter will cease to be an averaging filter and high inductive transients could appear across CR151.

It is also desirable that L5 not saturate.

Assuming a constant 20 v on the controlled dc bus, the voltage across L5 is approximately as illustrated below. The "swing" of L5 can be estimated by noting that Area 1 must equal Area 2, and



$$\Delta\Phi_1 = \Delta\Phi_2$$

$$= \frac{E_1}{N} \Delta T_1, \text{ where}$$

$$E_1 \approx 20v, \text{ and}$$

$$\Delta T_1 \approx 10\ \mu \text{ sec.}$$

Therefore,

$$\Delta\Phi_1 = \frac{20}{37} 10^{-5}$$

$$= 5.4 \times 10^{-6} \text{ webers.}$$

$$\Phi_{sat} = 6.30 \times 10^{-5} \text{ webers.}$$

Therefore, the core of L5 swings through approximately

$$\frac{\Delta\Phi}{\Phi_{sat}} \times 100\% = \frac{540}{63.6} = 8.5\%$$

of its capacity, and it is concluded that L5 will not saturate since

$$72 \text{ Oersteds} + (.085)\ (90) \text{ Oersteds} < 90 \text{ Oersteds}.$$

From the manufacturer's dc magnetization curve, it is estimated that the core would not bottom if the minimum operating point was such that

$$H_{min} > 10 \text{ Oersteds}.$$

This corresponds to a minimum current of

$$I = \frac{10 \times 10.11}{37 \times 1.26} = 2.6 \text{ amp}.$$

At zero external load, L5 has been observed to bottom. The transients observed, however, are insignificant.

(b) Capacitors C6, C7

Sprague 202D108x9045A4

1000 μf, 45 v.

If it is assumed that the current in L5 is a constant, then the ripple current in C_o (C_o is the parallel combination of C6 and C7) will be near zero. There will be some ripple on the controlled dc bus and some ripple current through C_o since the current in L5 is not a constant and C_o also serves to store energy returned to the controlled dc bus by the power converter stages. The worst-case measured ripple current in C_o is

$$I_{rms} = 2.2 \text{ amperes}.$$

Since C6 and C7 are each rated for 1.8 amperes of rms ripple current, this filter is considered safe.

The output filter attenuates frequencies above its 230 cps resonant frequency at 12 db/oct.

(3) Diode CR151 (HF3C)

CR151 is required to be a fast recovery diode that provides a path of current flow through L5 when the transistor regulator switch is opened. It must block approximately 30 volts, and carry an average current of approximately 4 amperes. No data is currently available descriptive of the HF3C.

(4) Regulator switch Q19, Q20, Q21

The regulator switch consist of three paralleled 2N1937 transistors.

(a) The switch, in an OFF mode, must block 30 volts. Therefore;

Required BV_{CEO} = 30 volts

Rated BV_{CEO} = 80 volts

(b) Assuming 75% efficiency, the maximum average current the switch is required to conduct is

$$I_{c\ ave} = \frac{250\ va}{25v \times .75} = 13.5\ amps.$$

The measured average current at rated load and an input voltage of 25 volts is approximately 14 amps. Assuming the switch is ON 75% of the period at full load, the peak current is

$$I_{c\ peak} = \frac{13.5}{.75} = 18\ amps.$$

Each transistor has a rated current of I_c = 20 amps, continuous at 25°C.

(c) Power dissipation:

If case temperature does not exceed 100°C and switching on a resistive load line is assumed, a single 2N1937 will always be far inside a safe, continuous operating region. Some derating is required for higher case temperatures, and a thorough analysis of power dissipation requires consideration of mounting and heat sink conditions. Assuming an efficiency of 70%, the switch is required to control

$$250\ va/.7 \approx 360\ watts.$$

If the 2N1937 can continuously dissipate

$$P_d > \frac{360\ watts}{8} = 45\ watts,$$

a single transistor could be considered for the switch.

$$\text{Rated } P_d = 150\ watts \text{ at } T_c = 100°C.$$

In an overload condition, the switch can be required to conduct more than 20 amperes average and has been observed in the laboratory to conduct approximately 24 amperes average. From (c) above, two 2N1937 transistors are required to perform the switching function, and two are adequate from power dissipation considerations.

(d) The switch is required to operate at 9.6 kc. Since f_T for the transistor is 18 mc, it is concluded that $f_\beta > 10 \times 9.6$ kc and the switching requirements are met.

(e) From laboratory measurements of the 2N1937 characteristics, a base current of

$$I_B \approx 2.5 \text{ amperes}$$

is required to saturate a single transistor switch at rated load and at room temperature. The minimum base current available is estimated below.

$$I_{R70} \approx \frac{25v(\frac{13}{100}) - 1.4v}{1\Omega} = 1.85 \text{ amp., and}$$

$$I_B \approx 1.85 \text{ amp.} - \frac{.75v}{5\Omega} = 1.7 \text{ amps.}$$

The minimum base current is not sufficient to saturate a single transistor switch. If three transistors are matched, the collector current in each will be

$$I_{ave} = \frac{13.5}{3} = 4.5 \text{ amps, and}$$

$$I_{peak} = \frac{18}{3} = 6 \text{ amps.}$$

Under these conditions, each transistor will require a base current of

$$I_B = 300 \text{ ma,}$$

and the base drive supplied is

$$I_B = \frac{1.7}{3} \approx 570 \text{ ma.}$$

It is concluded, therefore, that the base drive is sufficient for the three transistors in parallel, assuming that the transistors are reasonably matched. If they are not well matched, the use of individual base resistances to replace R70 will improve base current sharing in the transistors.

A preceding paragraph indicated that two paralleled transistors would be an improvement over three. One component would be eliminated that could cause the inverter to fail by failing in a shorted mode. The present, minimum base drive is

nearly sufficient to drive two transistors into saturation, and only a small increase in base drive would be required. The magnetic amplifier output, however, is operating above rated capacity and would have to be considered in any change in the switching mode regulator.

The curves in Figure 23 represent the switching mode regulator's closed switch voltage as a function of current through the one ohm resistor, R70. Curves 1, 2 and 3 represent the number of 2N1937 transistors paralleled to make up the switch. For these curves, V_{dc} = 30 volts, T = 28°C and the balanced load is 250 watts.

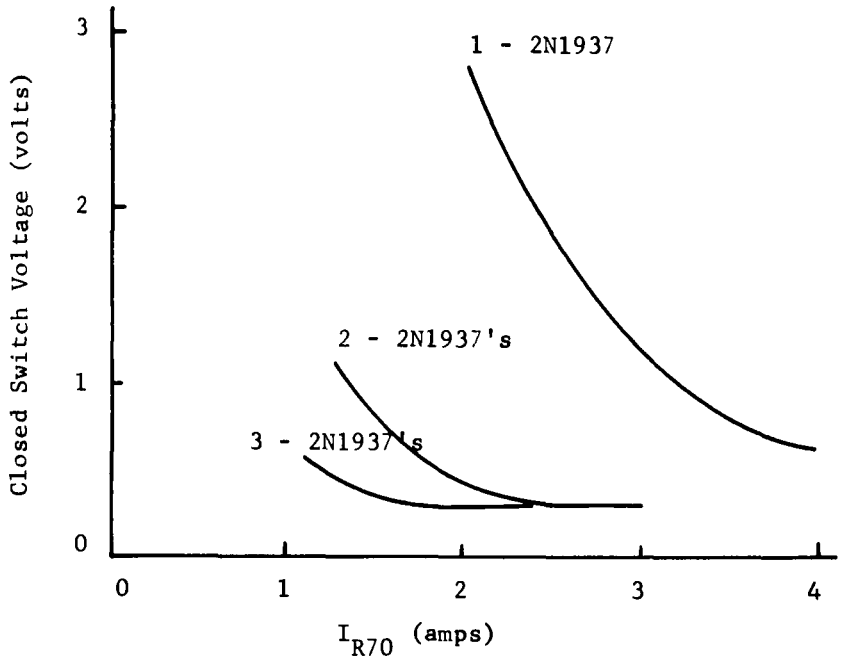


Figure 23. Regulator switch voltage as a function of the number of 2N1937 transistors in the switch and total magnetic amplifier output current.

(5) Other considerations

It has been pointed out that the output filter smooths the voltage on the controlled dc bus and that C6 and C7 provide the energy storage required by the power converter stages. The total capacitance can be reduced provided the expected ripple current can be tolerated. Using the same argument as under (1), (b) above, a decrease in capacitance will increase the reliability of the system. With these objectives in mind, more detailed studies will be made of the switching mode regulator.

3.0 AN OBSERVED FAILURE MODE

The static inverter has an over current protection system to protect the inverter from overload conditions, and it does function to protect the static inverter from extreme overloads, e.g., a short circuited output. Efforts to load the inverter with a steadily increasing load, however, has resulted in the failure of transistor Q13 and/or Q14 and, consequently, R1029 and the inverter itself. The failure mechanism has been identified as thermal run-away in Q13 and Q14, indicating inadequate power dissipation capabilities. An earlier section of this memorandum illustrated the inadequate power capabilities of Q13 and Q14 (See Section 2.12). This failure has been observed repeatedly at room temperatures and at 100° C. It has not been observed at 0° C, but it obviously will occur at temperatures below room temperature.

The region of failure is defined in Figure 24 in terms of the dc supply voltage and average, three-phase line current. The power dissipated by Q13 and Q14 is proportional to $V_{CE(sat)}$ and I_C The former is essentially constant, and the

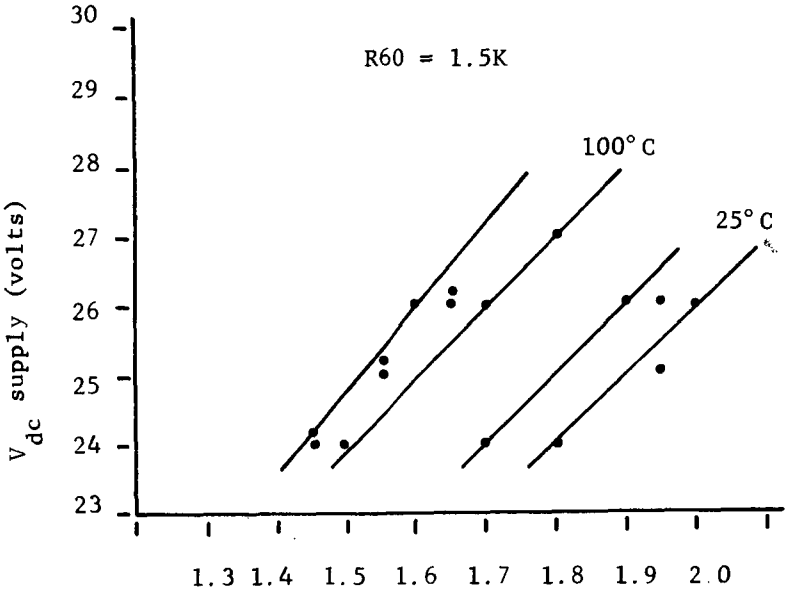


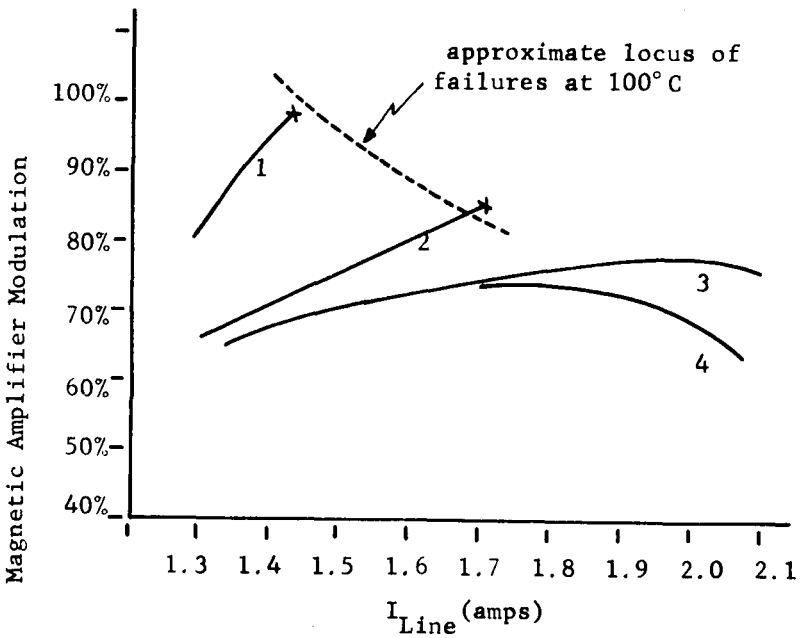
Figure 24. Static inverter failure regions

average value of I_C varies directly with the magnetic amplifier "ON" period, i.e., inversely with the supply voltage.

Figure 25 will further illustrate the observed failure. At a line current of approximately 1.4 amperes, the OCP circuit rectifier voltage reaches the threshold value that corresponds to the breakdown of zener diode CR148 and begins to

supply base current to Q35. The line current has to increase significantly, however, before enough base current is supplied to Q35 to permit a significant Q35 collector current, i.e., magnetic amplifier control current, to flow. At some value of current, the OCP circuit becomes effective and quickly turns off the inverter. Figure 25 also illustrates the effect of controlling the gain of the OCP circuit, i.e., controlling R60. By reducing R60 from 1.5 KΩ to 1KΩ, the OCP circuit influenced the inverter at a lower value of line current and prevented the inverter from entering a failure zone, c.f., the two curves for 28 V_{dc} in Figure 25. In Figure 24 no failures are indicated above 1.8 amperes and 26 volts at 100°C. Increasing R60 would probably result in failures at higher currents and voltages in the region.

This failure mode can be eleminated by increasing the power dissipation capacity of Q13 and Q14, or increasing the gain of the OCP circuit. At 1KΩ, R60 is at its minimum design value. With R60 at 1KΩ and T = 100°C, failures have



1 V_{dc} = 23V, R60 = 1.5 K T = 100°C

2 V_{dc} = 26V R60 = 1.5 K , T = 100°C

3 V_{dc} = 28V R60 = 1.5 k , T = 28°C

4 V_{dc} = 28V R60 = 1k , T = 28°C

Figure 25. Magnetic Amplifier Modulation versus Line Current

been observed at V_{dc} = 26 volts, and not observed at V_{dc} = 27 volts. To further illustrate the effect of R60 Figure 26 shows value of line current for which the OCP circuit just begins to influence the magnetic amplifier as a function of R60.

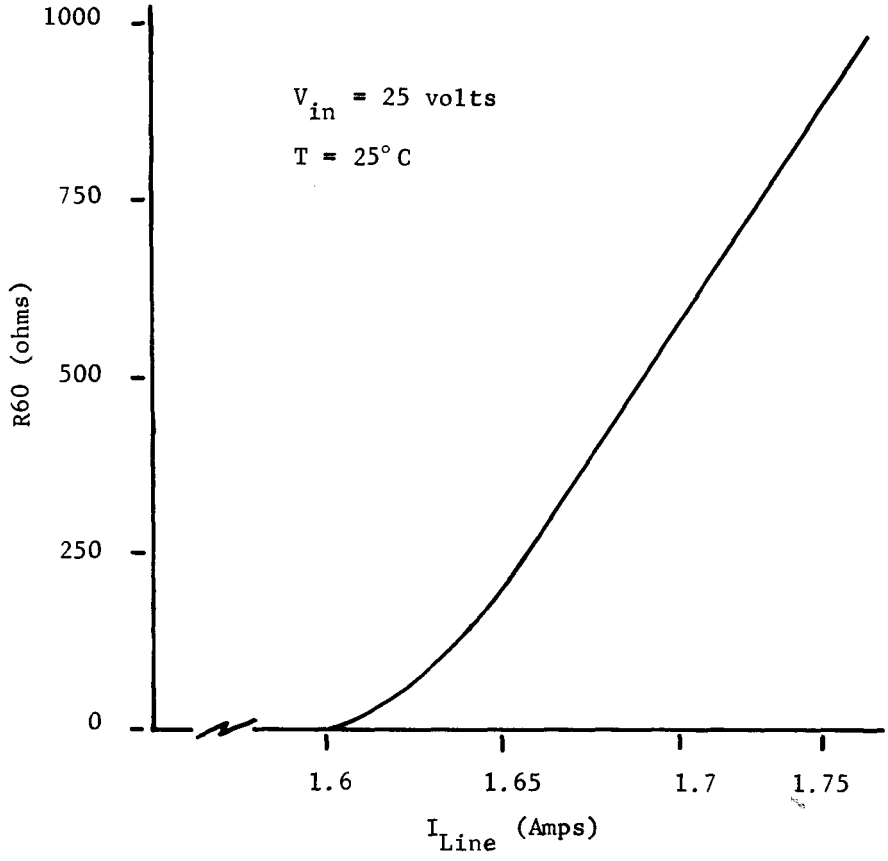


Figure 26. Effect of R60 on the threshold level of the OCP circuit.

All of the failures observed occurred within seconds or, at most, within a few minutes. Regions that would be considered "safe" from this analysis are likely to become failure regions if longer period of time are considered.

4.0 SOME OBSERVED PERFORMANCES

The performance curves in this section are included only to illustrate the voltage regulation potential of the breadboard model of the inverter. The voltage regulation characteristics can be controlled and made either positive or negative by controlling the magnetic amplifier feedback, and the output voltage level can be readily adjusted to any value within several volts of 115 volts without changing the regulation characteristics. Subsequent reports will discuss the static inverter performance and demonstrate conformance to specifications.

Figures 27A, 27B and 27C show the average 3-phase output voltage as a function of load, i.e., average line current to a balanced, resistive load, and the dc supply voltage is a parameter. Each figure corresponds to a different, constant temperature. Some of these data are also shown in Figures 27D and 27E where each figure is for a constant dc supply voltage and the ambient temperature is a parameter.

The values of the variable parameters during the period of these observations are tabulated below.

N_f = 3 turns

R60 = 1K Ω,

R69 = 125Ω, and

R73 = 1.1 KΩ.

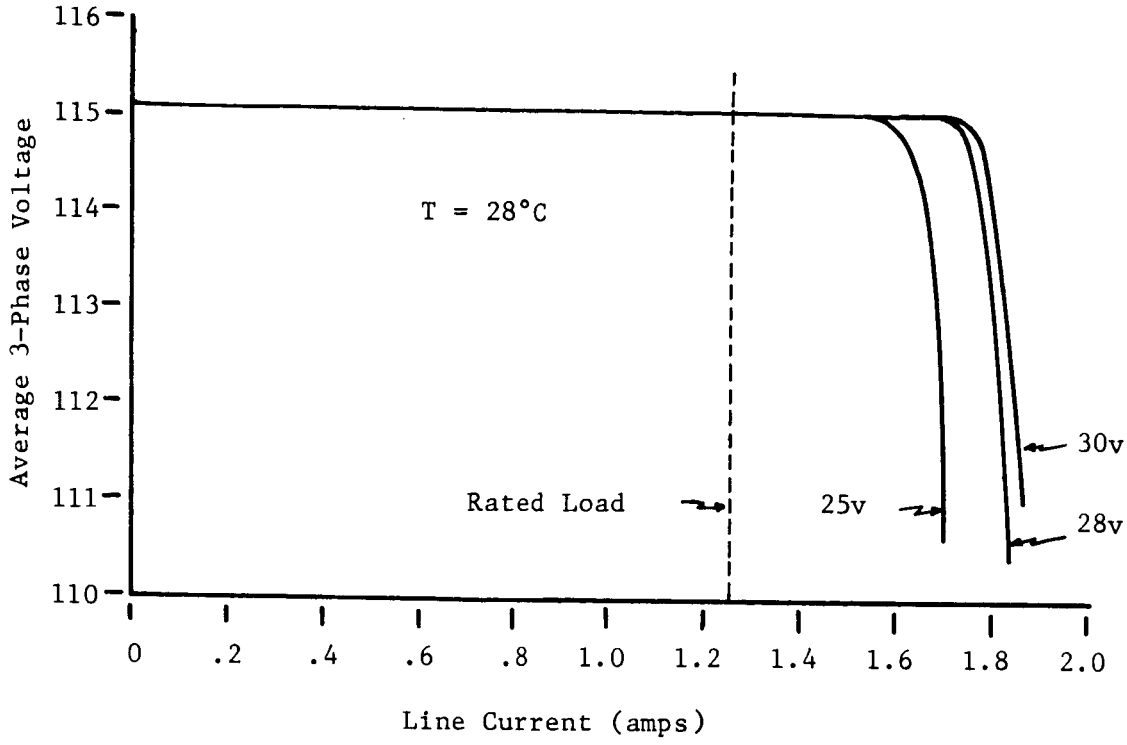


Figure 27A. Average 3-Phase Voltage Versus Line Current, T = 28°C

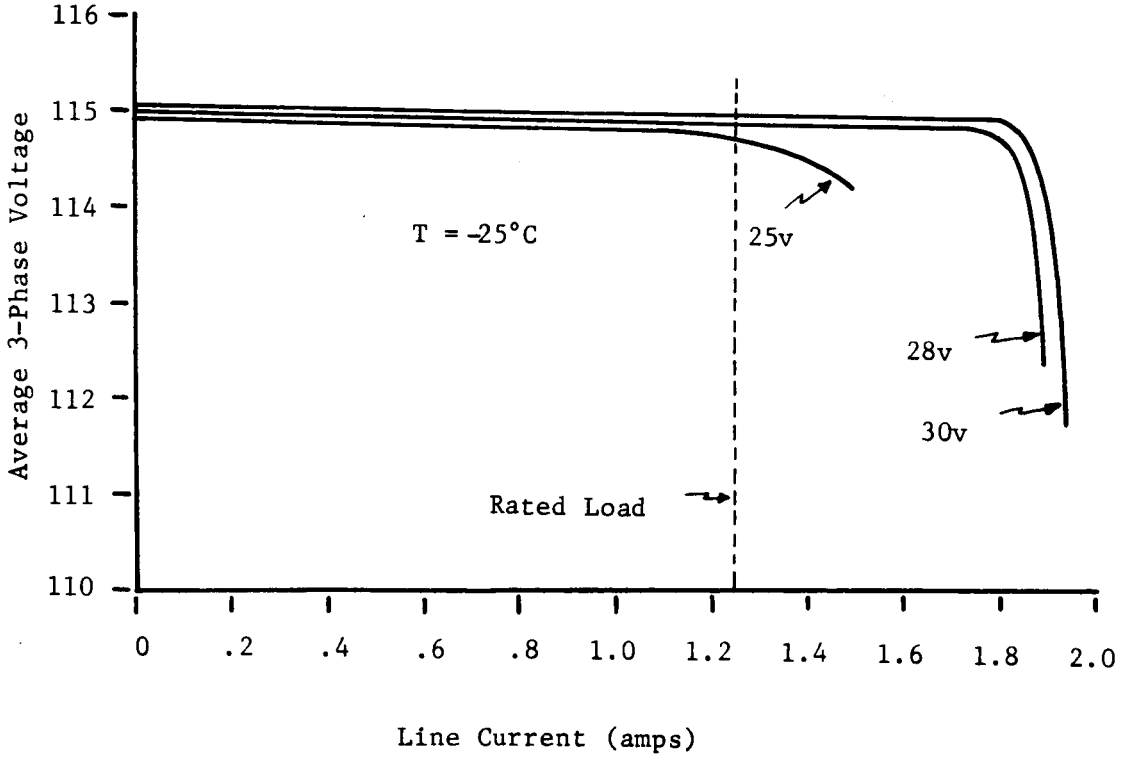


Figure 27B. Average 3-Phase Voltage Versus Line Current, T = -25°C

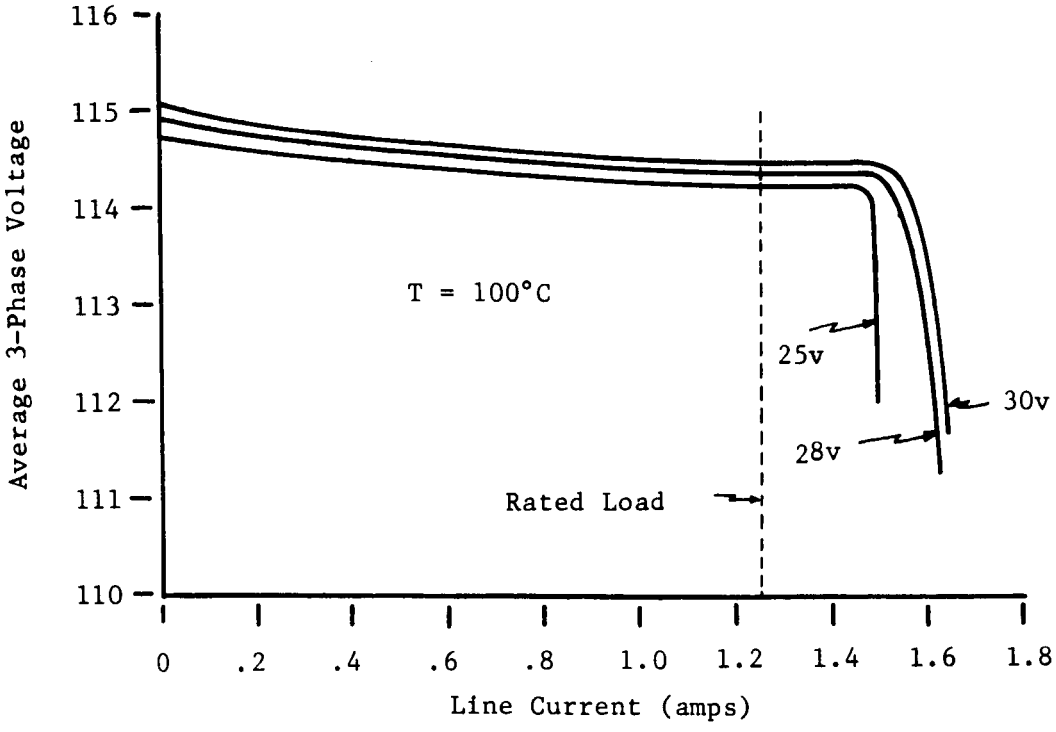


Figure 27C. Average 3-Phase Voltage Versus Line Current, T = 100°C

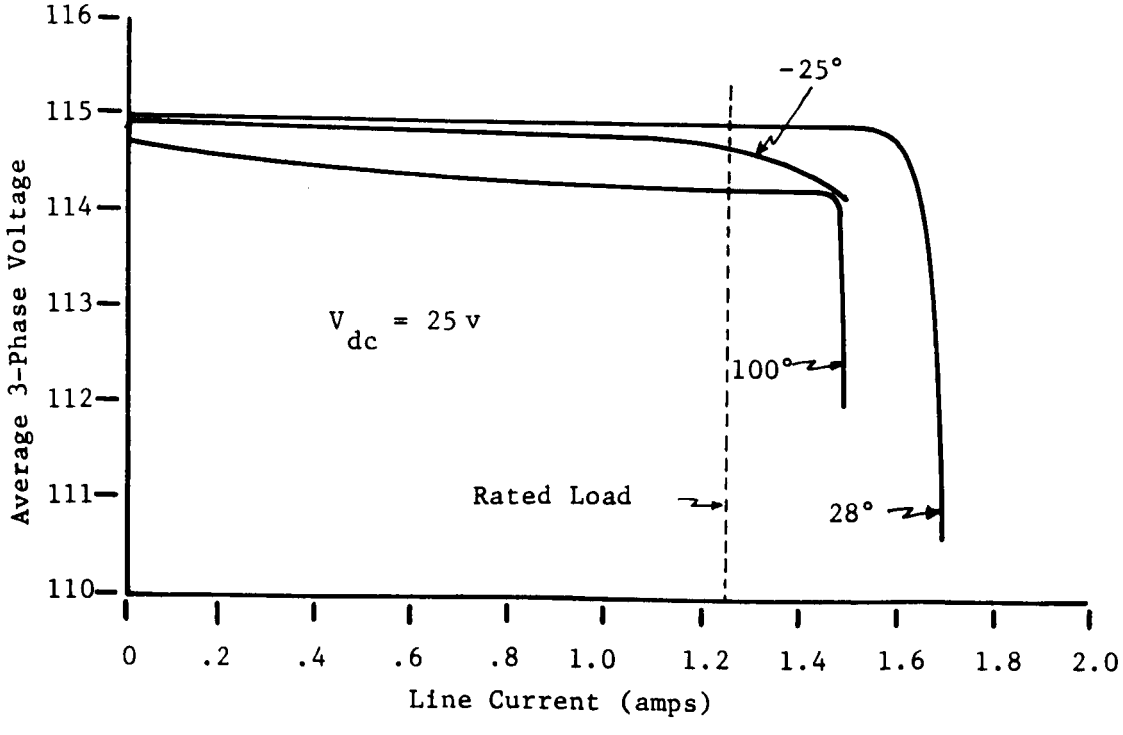


Figure 27D. Average 3-Phase Voltage Versus Line Current, V_{dc} = 25v

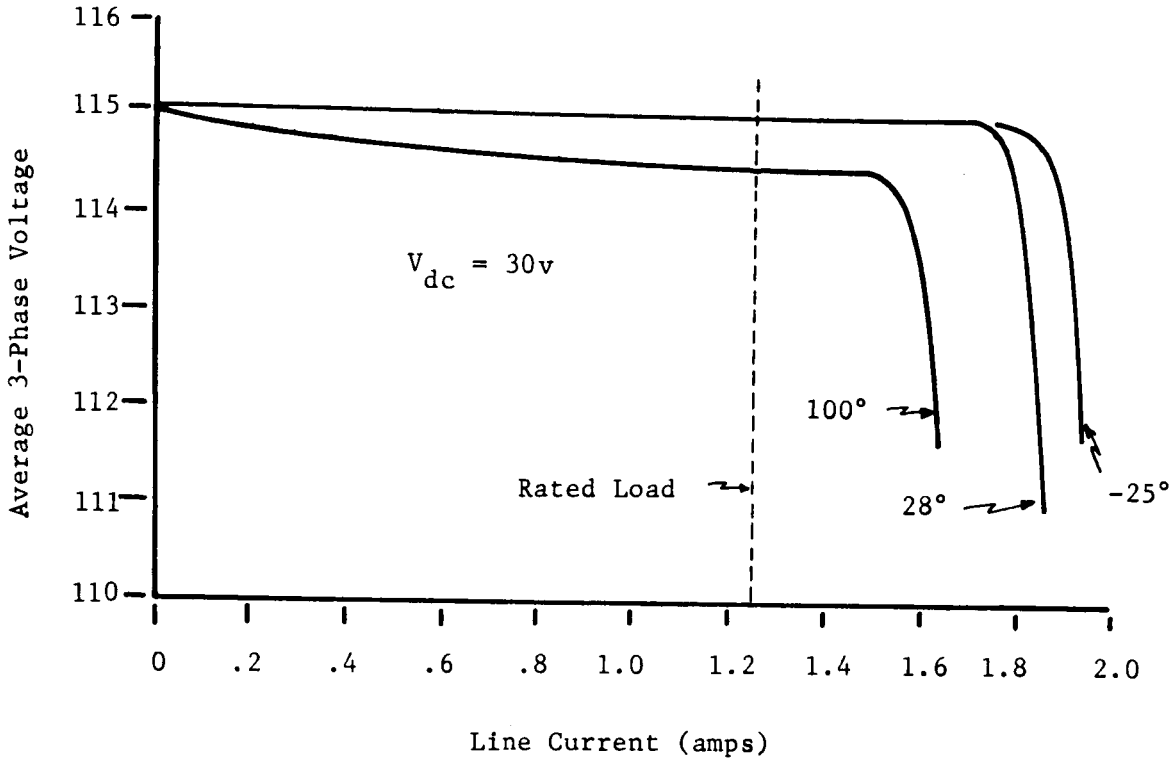


Figure 27E. Average 3-Phase Voltage Versus Line Current, V_{dc} = 30v

5. A SUMMARY OF CONCLUSIONS

The experimental performance curves shown in the preceding section illustrate the actual performance of the static inverter over a wide range of ambient temperature and input voltage for a balanced resistive load condition. This was the only attempt in the analysis presented in this report to observe the overall behavior of the inverter. Under the stated operating conditions the inverter does supply its rated load well within voltage specification, providing excellent t = 0 performance. The major portion of the analysis presented in this report was concerned primarily with reviewing the circuit for design adequacy with considerations extended to long term performance.

The preceding analyses permit certain conclusions to be drawn with respect to design adequacy and serve as the basis for identifying the need for more detailed analyses for various portions of the circuit. The conclusions drawn from the preceding analyses are summarized below.

(1) The only failure observed in the static inverter directly traceable to components is the magnetic amplifier output circuit; that is, the thermal run-away of Q13 and Q14 considered in Sect. 2.12. This mode of failure occurs only when the inverter is operating at an intermediate load condition between rated load and a load sufficiently great to cause the overcurrent protection circuit to function. This failure is predictable and can be caused to occur at any time by simply loading the inverter accordingly. Even though this overload condition is not one that may be considered to occur during the operational profile of the inverter, remedial changes are recommended to eliminate this mode of failure. It is felt that the inverter was intended to be self protecting and this mode of failure reflects a potential wekaness in the circuit design. The transistors Q13 and Q14 are inadequate for the power dissipation required of them during these overload conditions. Transistors with a high power capability are available and should be employed, or the OCP circuit should be redesigned to turn the inverter off nearer the rated load.

(2) The six-volt power supply is considered to dissipate more power than was necessary. A simplier design having fewer components and the same output power capability is proposed that extends the redundancy features of the original design. It developed, however, that the cognizant design group has already modified the design of the six-volt supply in order to

supply the higher power requirements resulting from redesign of portions of the timing section. Further consideration of the six-volt supply in this contract study will be assigned low priority because of the flexibility in the power requirements.

(3) The original design of the electronic switch is deemed adequate. This circuit, too, has been modified in connection with the modification of portions of the timing section and any further analyses will be assigned low priority.

(4) Only limited consideration was extended to the primary oscillator in the analysis. From the point of view of component ratings the design is adequate; however, the major concern with this circuit is the frequency stability. The cognizant design group is considering different designs with temperature compensation. This modification is posing the additional power requirements for the six-volt supply. Further consideration of this circuit is also assigned low priority.

(5) The design of the frequency countdown circuit appears to be adequate. Since it is likely that this circuit may be eliminated in connection with the redesign of portions of the timing section, further consideration of this circuit will be also assigned low priority.

(6) The design of the clock pulse amplifier is adequate, but the need to include this element in the system has been questioned. There is an ambiguity in the SN511A manufacturer's data bulletin concerning the acceptable levels of the clock pulse amplitude and one could conclude on the basis of this data that the frequency countdown circuit could feed the PSG directly, bypassing the CPA. Experimentally, this has been done, as was noted in Section 2.5, without any difficulties. There are, however, reports of difficulties with the SN511A flip flops when the clock pulse amplitudes are as high as typical SN511A emitter follower outputs, and similar difficulties have been observed in laboratory experiments to determine the electrical characteristics of the SN511A. Additional investigations will be made concerning the clock pulse amplifier and reported at a later date.

(7) The design of the pulse sequence generator is adequate.

(8) The original design of the timing pulse amplifier was deemed marginal. The conclusion resulted from consideration of the available base drive for the switching transistors in the circuit. The cognizant design group, however, has solved the problem of inadequate base drive by

reducing the resistance in base circuit. Other alternatives proposed in the analysis consisted of removing one of the parallel pair of diodes in each of the diode coupling units between the pulse sequence generator and timing pulse amplifier or removing the diode coupling altogether and relying strictly on resistive coupling. With the publication of this report an extensive investigation of this portion of the circuit is in progress from the point of view of failure modes and their effects. It can already be stated that eliminating a parallel pair of diodes in the diode coupling is preferable to the diode quad arrangement in the original configuration. The analysis is also considering the removal of the diode coupling and relying on resistive coupling. This requires confirming that the diodes are not needed as threshold devices. Experimentation is being conducted to verify this.

(9) The power converters can be made more efficient by reducing the input voltage and the resistance in the base circuit of the switching transistors. This can be easily accomplished by reducing the secondary winding on the coupling transformer between the timing pulse amplifier and the power converters.

The 1N645 reactive diodes in the power converter stages are obviously inadequate and should be replaced. A single diode with adequate capability should be selected to replace the parallel diodes. It is understood that the cognizant design group has such plans when a qualified component with this capability can be made available.

Since the power converter stage is a functional element of the voltage regulation loop the performance characteristics are being studied in considerably more detail in connection with the voltage regulation loop. Variations within this circuit and how they may contribute to the harmonic distortion of the output waveform will also be considered.

(10) The original configuration of the output circuit and its design parameters were deemed adequate. Further considerations of the output circuit will be made in connection with the voltage regulation loop analysis, and analyses for the output voltage balance, the output phase balance and the output distortion.

(11) The twenty-volt regulator supply was deemed adequate for supplying the required load during normal inverter operating conditions and conditions when the overload protection circuit was functioning. Further considerations

of the twenty-volt regulated supply are being made in connection with the analyses of the voltage regulation loop.

(12) The design of the magnetic amplifier driver stage was deemed adequate.

(13) The magnetic amplifier circuit was deemed adequate on the basis of the component ratings. Further studies of the magnetic amplifier are being conducted in connection with the analysis of the voltage regulation loop. The associated magnetic amplifier output circuit was considered under item (1) above for a particular failure mode that was predicted on the basis of the analysis and observed later in the breadboard circuit.

(14) The voltage error detection circuit was deemed adequate. Further considerations of this circuit are being made in connection with the voltage regulation loop analysis.

(15) The design of the overcurrent protection circuit was deemed adequate. Experimental observations reveal that it functions adequately to protect the inverter circuit during overload conditions above 2 amperes output line current. It is possible to circumvent the failure mode observed in item (1) above by lowering the load condition at which the overload protection functions, but it is concluded that a more direct means is advisable, e.g., providing for more power dissipation capability in the magnetic amplifier output circuit.

(16) In the primary voltage regulator, it was concluded that capacitor C5 in the input filter conducts excessive ripple current, that is, approximately 200% above rated ripple current. A significant improvement can be made by using the same capacitor that is available in a larger can. With this exception, the design of the primary voltage regulator is adequate.

It is recommended, however, that the following modifications be considered.

(a) Load sharing among the parallel switching transistors can be enhanced by using individual base resistors for each transistor. A speed-up capacitor in each base lead may also prove to be desirable.

(b) The use of two transistors in the switch rather than three would increase the reliability of the system provided sufficient base drive was made available. This problem cannot be resolved, however, without joint consideration of the problems discussed in item (1) above.

These recommendations will be investigated further as the project progresses.

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