SERVO CONTROL

AND

DATA SYNCHRONIZATION STUDY

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No new technology has been discovered to date of this report as a result of this study.

SYNOPSIS

Maximum usage of magnetic tape storage for digital recording requires that data rate be constant. When data rate is variable, specialized equipment must be used to achieve constant rate recordings. Such equipment changes tape speed to equalize desired recording rate with incoming data rate. Because tape speed cannot be changed instantaneously to match a data rate change, a buffer storage system is used between data input and the recording head.

Tape speed changes are controlled by a closed-loop electromechanical servo system. Error signal for the servo is derived from the incoming data rate and the amount of data in buffer storage. Speed is adjusted so that incoming data never overflows buffer storage capacity and gaps are not recorded on the tape.

For data retrieval, the process is somewhat reversed. Data are read from the tape into buffer storage. Data output from buffer storage is synchronized to a master clock. And tape speed is derived from data output rate requirements and the amount of data in buffer storage.

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SERVO CONTROL AND DATA SYNCHRONIZATION STUDY

INTRODUCTION

Investigating the feasibility of a magnetic tape recorder-reproducer capable of (1) accepting data pulses at varying rates, (2) making maximum usage of storage space by recording data at a constant rate, and (3) retrieving the recorded data at a rate synchronized to an external clock is the objective of the study. This report gives a theoretical description of such a "recorder".

GENERAL DESCRIPTION

Basically, system operation will follow this scheme. Incoming data are stored in a buffer register. Data are clocked out of the register onto the tape at a rate compatible with the chosen packing density. A voltage analogous to the incoming data rate is used as the error signal in a closed-loop servo, controlling tape speed. Because a motor is incapable of making instantaneous speed changes, tape speed cannot immediately follow changes in input data rate. Therefore, register capacity is made large enough to accommodate great data influxes without overflowing, and sufficient data level is maintained to prevent blank spaces on the tape.

For retrieval, an increase or decrease in data output rate is reflected through register data level as an increase or decrease in tape speed. Again, register capacity and optimum data level are chosen to prevent output data rate changes from depleting or overflowing the register. Data output is synchronized to a master clock, giving bit dejittering* as an incidental but very important byproduct.

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*Dejittering is the term applied to Borg-Warner Controls method of providing crystal clock steady digital output from a magnetic tape recorder-reproducer. A patent application, 555 189, Data Transfer System, covering the method has been filed.

DETAILED DESCRIPTION

A detailed description of the buffer register and servo system is given in the following paragraphs. Figure 1 is a simplified block diagram of the recorder; figures 2 and 3 show the recorder in the write (record) and read (playback) modes, respectively.

BUFFER REGISTER

The buffer register collects and transmits bits as required to obtain constant density recording with a variable, data transfer rate. Instantaneous change of the data transfer rate may be as much as 1000 bits per second (bps) between the rates of 300 to 9000 bps. Since the recorder mechanism has a finite inertia, its data rate cannot change instantaneously. Therefore, temporary storage must be provided until the tape speed is commensurate with the data rate. Calculations deriving the maximum storage requirement for this recorder are appended.

There are many configurations of buffer storage systems which will provide the necessary storage required for the recorder. One is a shift register with input data inserted at one end and output data transmitted from a particular bit position. Write operation of this system will be explained; read operation is very similar, with some additional gating required.

Basic System

Seven essential elements are comprised in the basic system (see figure 4). Data are stored in the shift register, the input flip-flop, and the output flip-flop. The shift register is always filled from the left, and the output flip-flop is filled from the shift register position specified by the current address register (CAR). CAR is incremented for each shift to the right and is decremented after each output to the output flip-flop. F_o (output empty), F_{in} (input full), and sync (read/write synchronizer) are used to control the data transfers and synchronize the operation logically.

Operating States

Basic operating states of the system are indicated in figure 5; normal resting point of the system is input flip-flop empty, and the output flip-flop full. This is illustrated as the bottom state of the diagram. Other combinations of the settings of the control flip-flops are illustrated as the other blocks. Arrows indicate the path in which a change in state may occur; the labels indicate what caused the state change.

The sync flip-flop prevents attempts to read and write simultaneously. Since the inputting and outputting of the data are asynchronous to one another, some method must be provided for synchronization of the data transfer to ensure that no bits are lost or generated. A method of synchronizing is illustrated in figure 6, along with appropriate timing diagram. A similar system is used to synchronize the spacecraft clock to the recorder oscillator (not shown).

Figure 7 illustrates the complete state diagram that includes the synchronization flip-flop. Since there are three flip-flops, there are eight logical control states. The falling edge of the oscillator clocks all operations except setting and clearing the F_o flip-flop.

Logical Equations

Logical equations in the list below describe how the hardware must be implemented from a logical standpoint in order to perform the function acting as a buffer storage unit. It should be noticed that only one clock is used to control data transfers. Inputting or outputting is determined by the status of the read/write line (see figure 1). Only the source and destination of the data changes from write to read; all operations remain the same.

Underlined terms (____) indicate the dynamic change clocks the event.

s D_{in} = Clock· write data

r D_{in} = Clock· write $\overline{\text{data}}$

s F_{in} = Clock·

r F_{in} = $\overline{\text{Sync}}$· Osc· F_{in}

Shift R_T = Osc· $\overline{\text{Sync}}$· F_{in}

Inc CAR = Osc· $\overline{\text{Sync}}$· F_{in}

Dec CAR = Osc· Sync

s Sync = F_o· Osc

r Sync = $\overline{F_o}$· Osc

dc Set F_o = Tach

dc Reset F_o = Osc· Sync

$_J CAR_1$ = $_K CAR_1$ = Osc· (Sync + F_{in})

$_T CAR_2$ = $\overline{\underline{CAR}}_1$· $\overline{\text{Sync}}$ + $\underline{CAR}_1$· Sync

$_T CAR_3$ = $\overline{\underline{CAR}}_2$· $\overline{\text{Sync}}$ + $\underline{CAR}_2$· Sync

$_T CAR_4$ = $\overline{\underline{CAR}}_3$· $\overline{\text{Sync}}$ + $\underline{CAR}_3$· Sync

$_T CAR_5$ = $\underline{CAR}_4$· Sync + $\underline{CAR}_4$ Sync

CAR is a basic count up-count down binary counter

$s\ D_o$ $= (Osc \cdot Sync\ Write + Clock \cdot Read)$

$(\overline{CAR}_5\ \overline{CAR}_4\ \overline{CAR}_3\ \overline{CAR}_2\ \overline{CAR}_1\ S_o +$

$\overline{CAR}_5\ \overline{CAR}_4\ \overline{CAR}_3\ \overline{CAR}_2\ \overline{CAR}_1\ S_1 +$ Setting of D_o directed by current contents of the CAR.

$\overline{CAR}_5$ etc.

$CAR_5\ CAR_4\ CAR_3\ CAR_2\ CAR_1\ S_{31})$

Shift Register

$s\ S_o = \overline{Sync} \cdot F_{in} \cdot Osc\ D_{in}$

$r\ S_o = \overline{Sync} \cdot F_{in} \cdot Osc\ D_{in}$

$s\ S_1 = \overline{Sync} \cdot F_{in} \cdot Osc\ S_o$

$r\ S_1 = \overline{Sync} \cdot F_{in} \cdot Osc\ \overline{S_o}$

$s\ S_2 = \overline{Sync} \cdot F_{in} \cdot Osc\ S_1$

$r\ S_2 = \overline{Sync} \cdot F_{in} \cdot Osc\ \overline{S_1}$

etc.

$s\ S_N = \overline{Sync} \cdot F_{in} \cdot Osc\ \overline{S_{N-1}}$

$r\ S_N = \overline{Sync} \cdot F_{in} \cdot Osc\ \overline{S_{N-1}}$

Hardware Estimate

Hardware estimated for accomplishing the function described and for implementing the logic equations breaks down as follows:

	Flip-flop	Gate	Inverter
Current Address Register	5	10	-
Sync	1	2	-
Shift Register	32	64	-
Data Out	1	12	-
Date In	1	-	1
Input Full	1	-	1
Total	42	89	2

Digital-to-Analog (D/A) Converter

One possible configuration for the D/A converter is shown in figure 8. The converter is required to provide an analog signal to the servo system which is proportional to the contents of the CAR. One-half full is treated as nominal.

SERVO SYSTEM

Describing the servo system includes showing how the open-loop transfer function is synthesized and discussing a phase-lock loop with comparison of communication type voltage control oscillators (VCO) with electromechanical VCOs.

Frequency Response

Synthesis used at Borg-Warner Controls involves the methods of Bode plots or templates and the Nichols chart. With the fixed plant established, the phase equalizing network is selected to provide maximum phase lead at the estimated natural frequency of the closed-loop system. Complete open-loop transfer function is calculated (using the Boonshaft and Fuchs response slide rule, or by computer).

A template relating decibels and phase angle is made and superimposed on the Nichols chart. Such a chart is a complex variable transformation of the open-loop transfer function to the closed-loop transfer function in the frequency domain; i.e., KG to KG/(1 + KG), where KG is the open-loop polynomial in S and KG/(1 + KG) is the closed-loop polynomial.

While not particularly elegant, the method is straightforward and requires only a short time to accomplish. While the natural frequency (and bandwidth) must still be estimated, the method does establish damping ratio and gain variation sensitivity quickly.

If the initial results are not satisfactory, insight is provided to make a second or third calculation yield satisfactory results. In this manner, all filtering functions can be synthesized.

Phase Lock Loops (PLL)

A paper by Jaffee and Rechtin of JPL* describes the use of the phase loop for detection and tracking of narrow band signals in the presence of wideband noise.

Communications Systems (PLL). While tape recorder capstan servo system PLLs generally are not used as detectors nor are required to operate in the presence of wideband noise, it is still useful to study the PLLs of communications systems for these reasons:

A. There is very little published data concerning PLLs used for purposes other than communications.

B. Many concepts of the communication system are applicable to the electromechanical system.

Similarities and Differences. Similarities and differences of these two types of PLLs are now described. Referring to figure 11 of the Jaffee and Rechtin paper, and to Borg-Warner Controls figure 9, the following similarities and differences are noted:

A. The communications system VCO is replaced by an electromechanical VCO consisting of the motor; a frequency generating tachometer consisting, perhaps, of a toothed-wheel and sensor; a frequency discriminator; a ripple filter; and a d-c amplifier. These are connected in a closed-loop configuration commonly called a velocity servo or the coarse speed control. Such a configuration is entirely analogous to the all electronic VCO with the basic difference that there is a time constant associated with the electromechanical VCO. This time constant is essentially that of the motor and its inertia load reduced by the gain and feedback factors of the

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*Jaffee and Rechtin, "Design and Performance of Phase Lock Circuits Capable of Near Optimum Performance Over a Wide Range of Input and Signal and Noise Levels," Information Theory, IRE Transactions, March 1955.

closed-loop system. (This concept is no different than that of a feedback amplifier in which the bandwidth increases as the amount of feedback increases. Similarly, the closed-loop gain of such an amplifier configuration decreases as the bandwidth increases, preserving the original open-loop gain-bandwidth product.)

B. A bistable multivibrator (flip-flop) is used by the electromechanical servo system as a phase detector rather than the bridge multiplier (balanced modulator) referenced by Jaffee and Rechtin. The flip-flop phase detector* is also used in communications system PLL, however.

C. The loop filter in the communications system PLL functions both to phase equalize the low frequency signals and to attenuate the high frequency term assumed negligible in the Jaffee and Rechtin analysis. A different type of loop filter is used in the electromechanical system primarily because of the added time constant of the electromechanical VCO. Good transient response and minimum error (flutter) are design goals. Generally speaking, capstan motor PLLs are not subject to reference frequency spurious bandpassed noise (Jaffee and Rechtin), but instead are exposed to spurious torques on the motor shaft caused by motor cogging, bearing irregularities, etc., which produce phase error. Such filters do not necessarily provide adequate carrier frequency attenuation. Such attenuation is essential in order that linear operations such as amplification be achieved. A separate ripple filter is therefore required.

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*C. J. Byrne, "Phase Controlled Oscillator with a Sawtooth Comparator," BSTJ, March 1962

A linear system greatly improves synchronization. Use of such a system is a basic assumption of the Byrne paper which deals heavily with synchronization analysis.

Nonlinearities

Extensive nonlinearities exist with the electromechanical PLL which do not occur with the communications PLL. These consist of:

A. Current limiting of the motor system (a typical tape recorder specification) which limits the accelerating torque of the motor and can be viewed as a saturation type of nonlinearity (figure 10).

B. Error output saturation is a fundamental nonlinearity for both types of PLL. Such saturation occurs in amplifiers when the output voltage approaches the amplifier power supply voltage. It is graphically shown in figure 11.

C. A very important nonlinearity inherent to simple implementation is the use of a single-ended power amplifier as the motor driver. Such amplifiers cannot provide negative current. When the load is a d-c motor possessing back emf, the output transistor operates only over a reduced voltage range, namely E_{supply} minus E_{BEMV}. In practice, for constant or slowly varying speed applications, this circuit does not become nonlinear. For large negative-going commands to reduce speed, however, the nonlinearity will be introduced and friction alone will slow the tape transport. Graphically, this single-ended amplifier nonlinearity is shown in figure 12.

For the motor to slow down, the transistor operating point goes from A to B as indicated by the arrows. A push-pull amplifier will correct this nonlinearity when using a d-c motor. With the inverter/a-c motor

equivalent to the d-c motor, it is not possible to supply negative current to the inverter. This arrangement thus is compatible with the single-ended amplifier. Fortunately, the a-c motor does not provide a back emf as does the d-c motor. With the present configuration braking torque can be provided by switching the phase angle of one of the 2-phase power supplies.

D. The phase detector of the communications PLL is the principal nonlinearity of such systems. In the Jaffe and Rechtin paper, the asynchronous output is a sinusoid, inherently unstable over 50 percent of its range, which hinders synchronization. Later papers such as Byrne, discuss the linear phase detector approach also used in capstan motor PLL. These nonlinearities are shown in figure 13.

Synchronization studies of PLL include only this phase detector nonlinearity. In practice it is necessary to include all nonlinearities in order to design for predictable synchronization.

In addition to nonlinearities, other important factors affect performance and must be considered. These include amplifier drift power supply, drive supply voltage variation ac and dc, the previously mentioned spurious motor torques, and resonances such as caused by reel inertia/tape compliance.

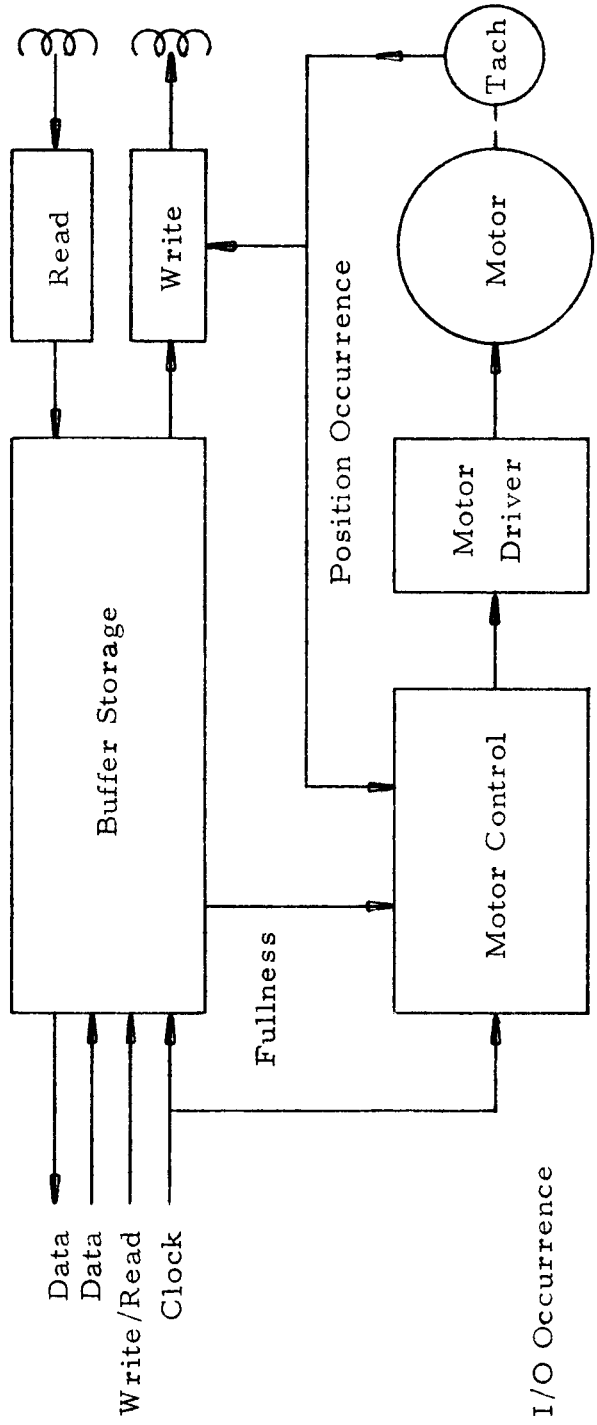

Figure 1. Basic Constant Density - Variable Data Rate System

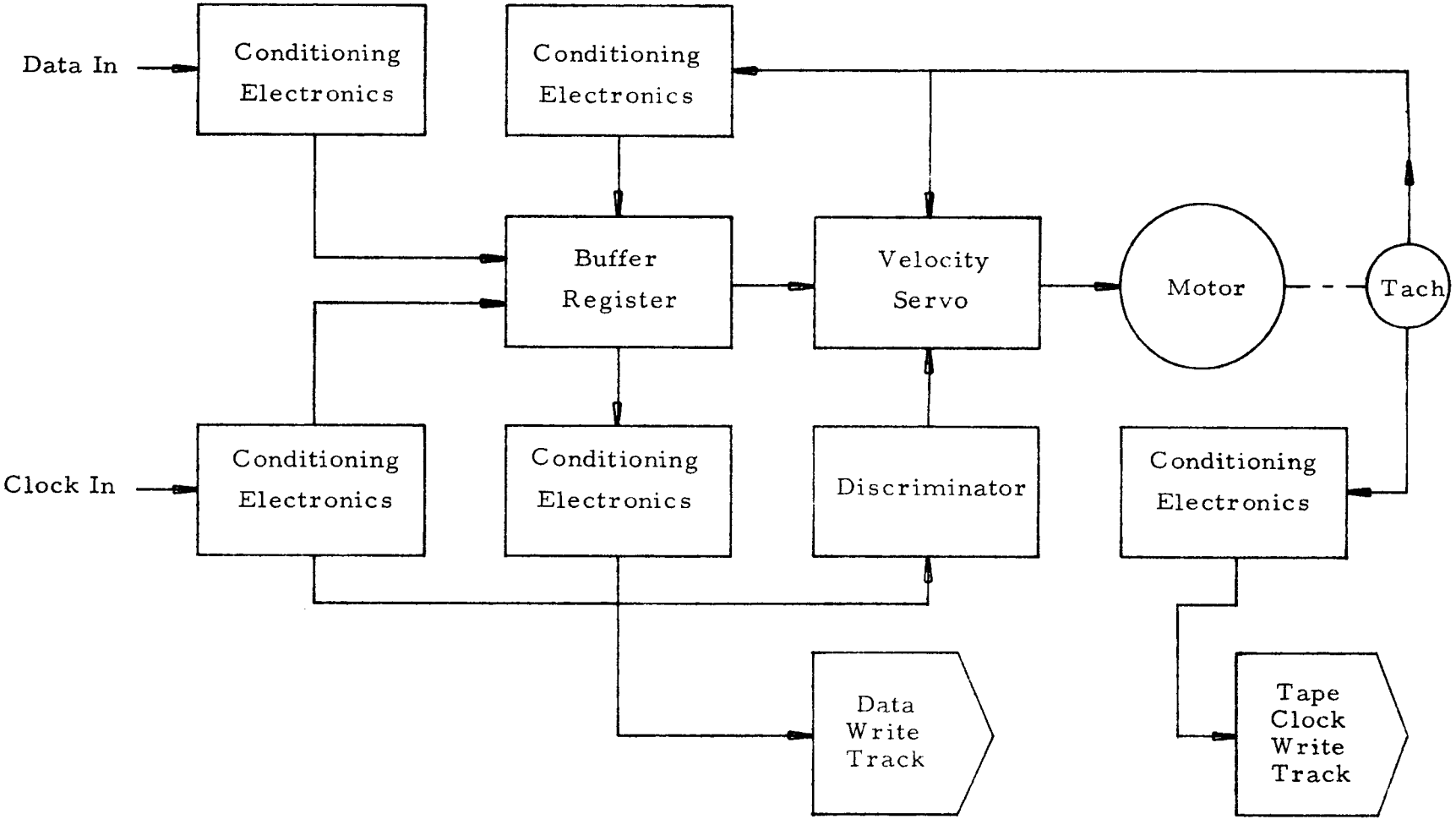

Figure 2. Recorder in the Write Mode

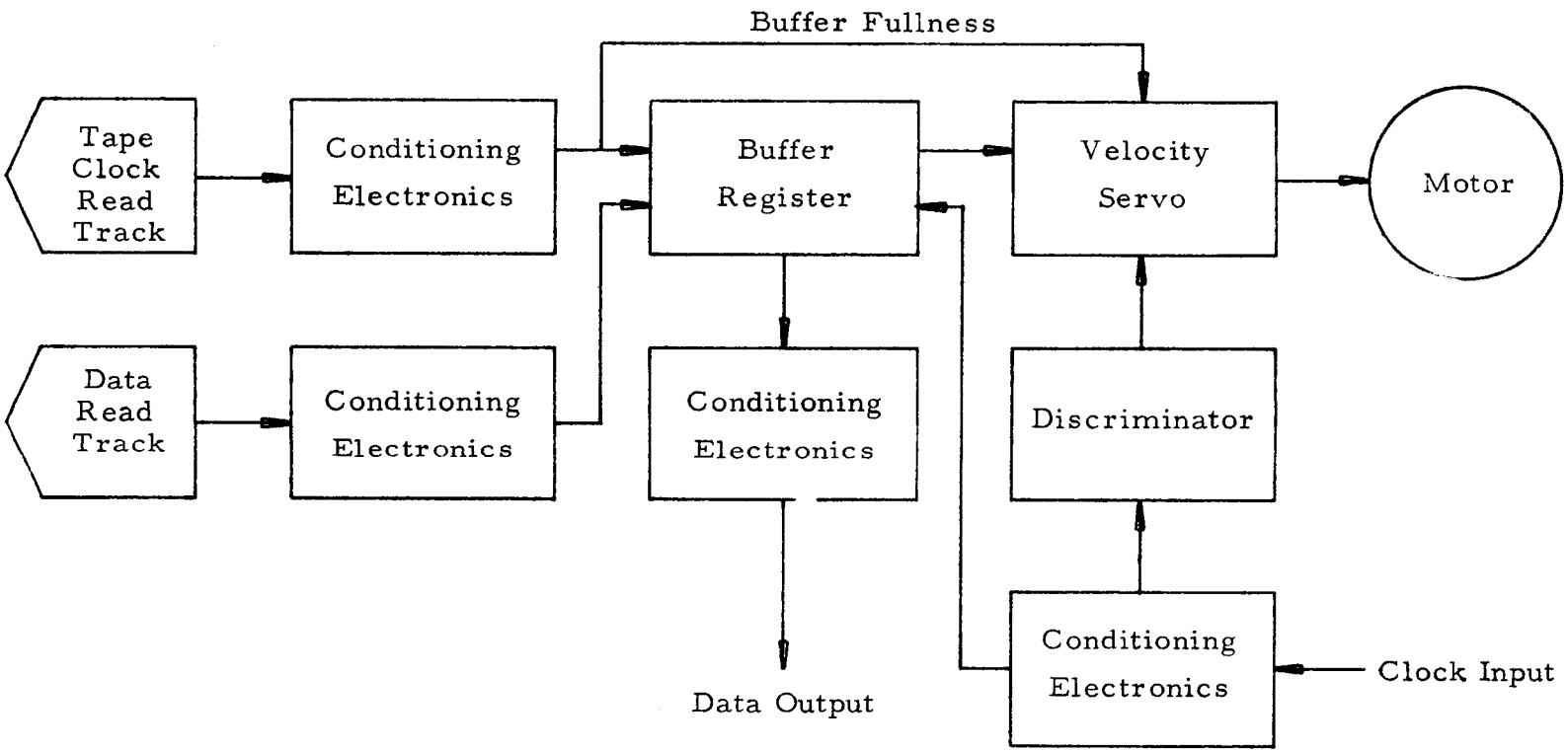

Figure 3. Recorder in the Read Mode

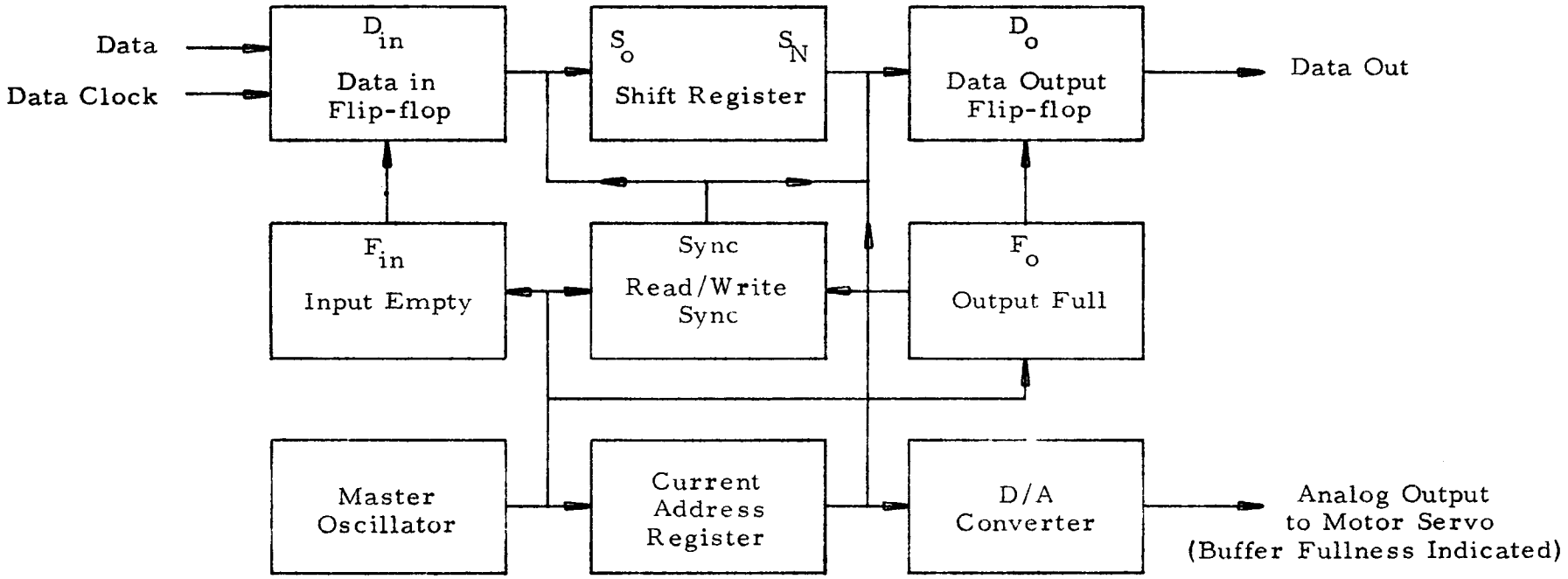

Figure 4. Basic Shift Type Buffer Register

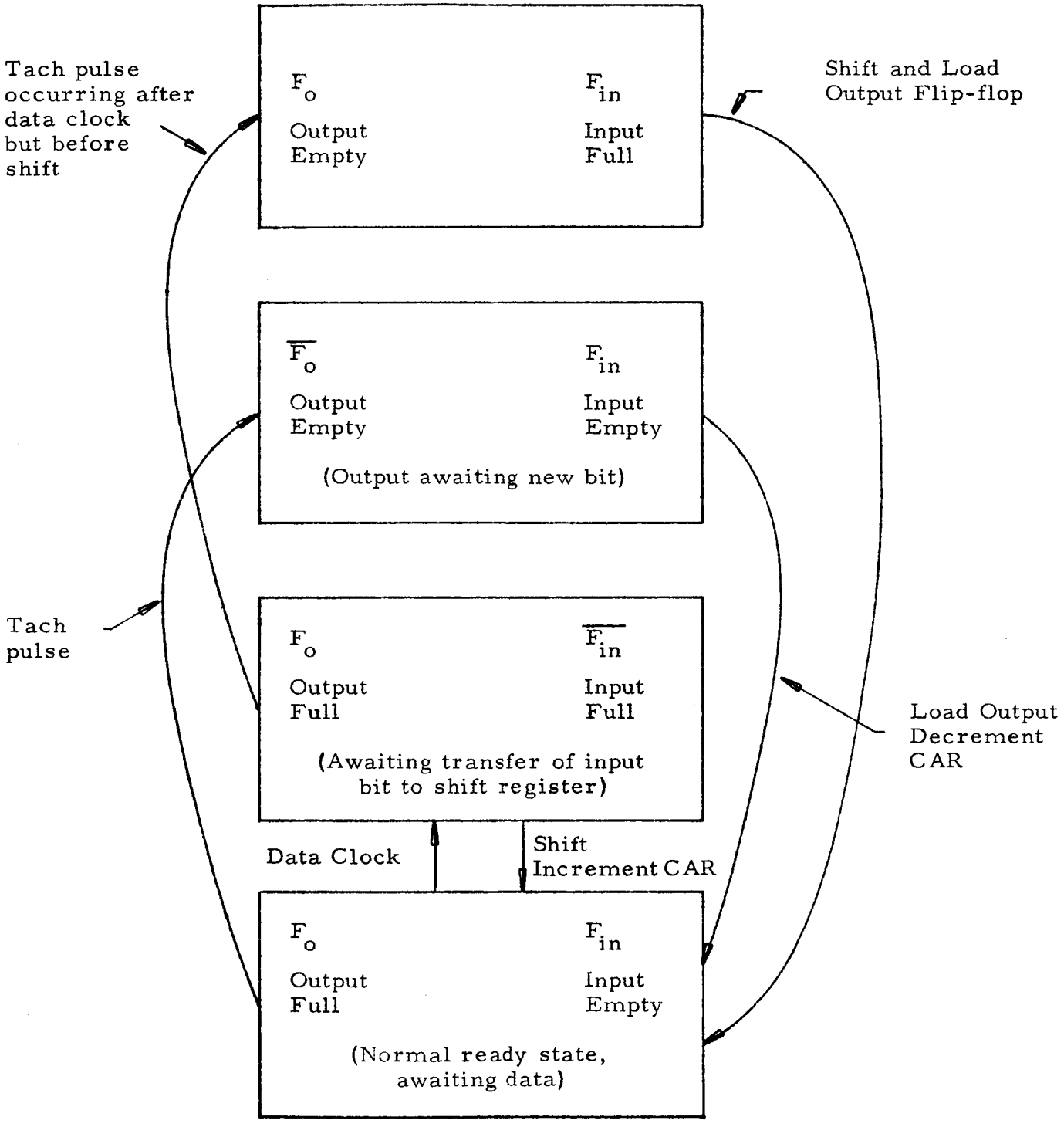

Figure 5. Basic System Control State Diagram
(Write Mode)

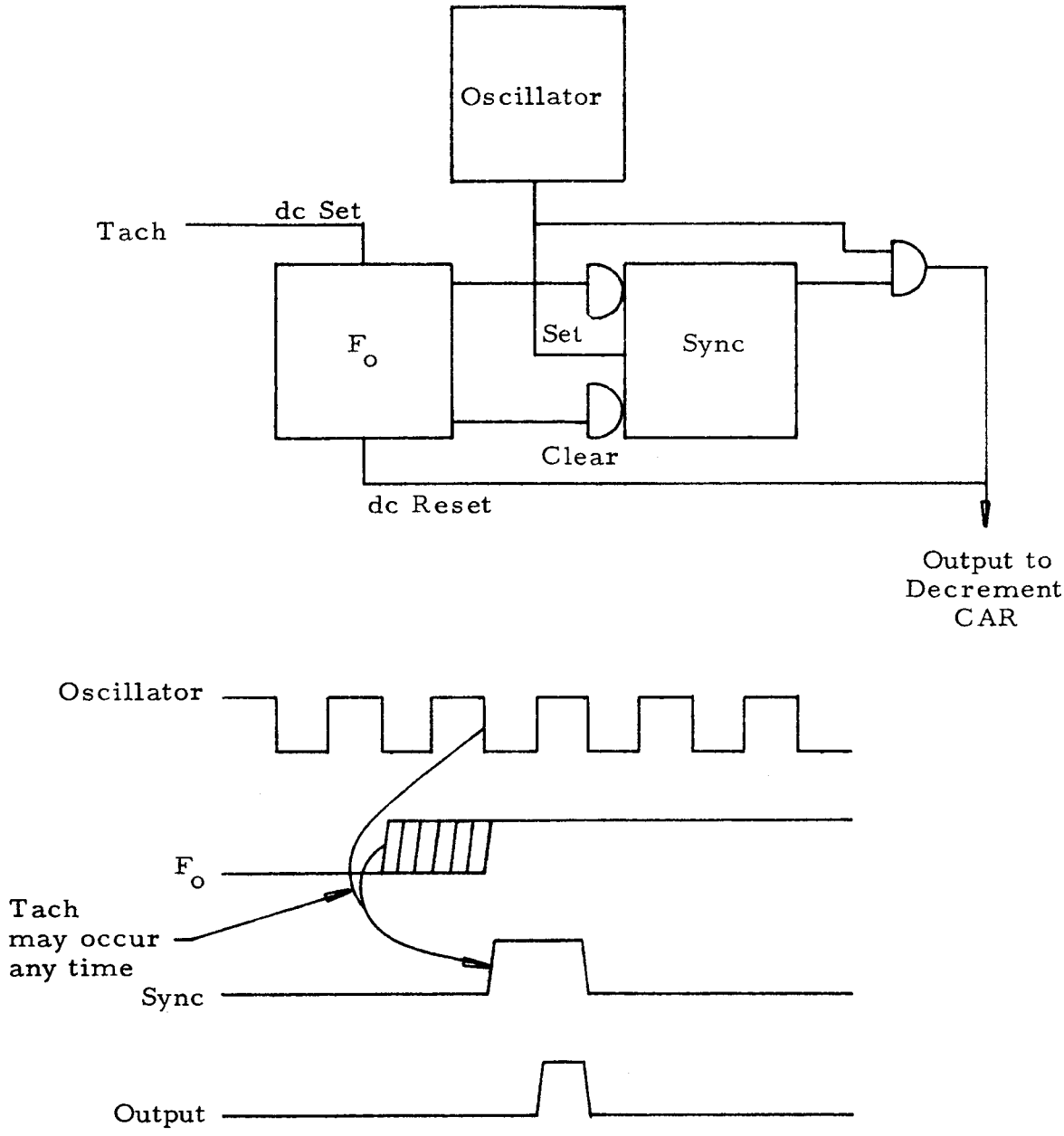

Figure 6. Synchronization Logic (Record Mode)

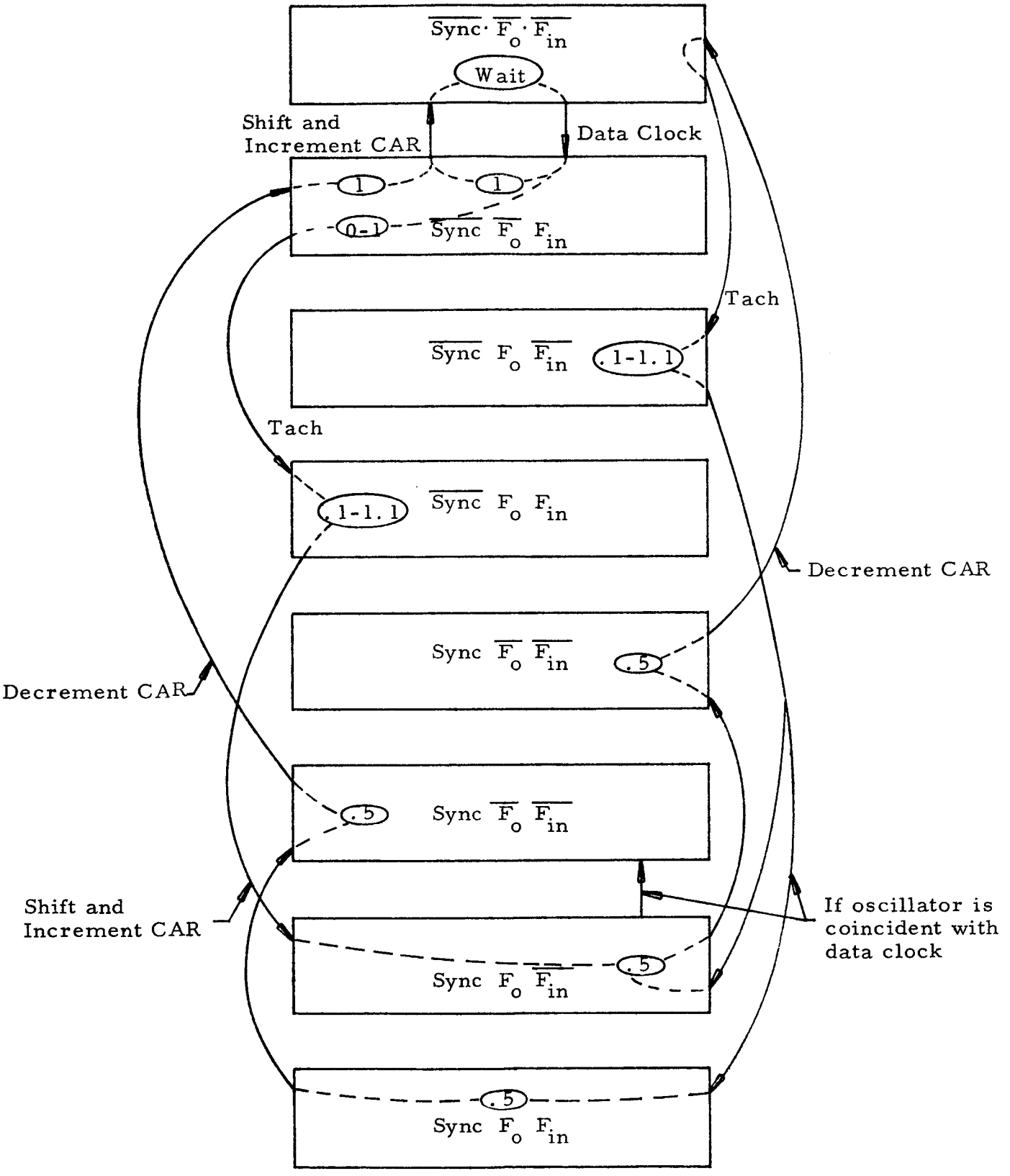

Figure 7. Shift Buffer System State Diagram
(Write Mode)

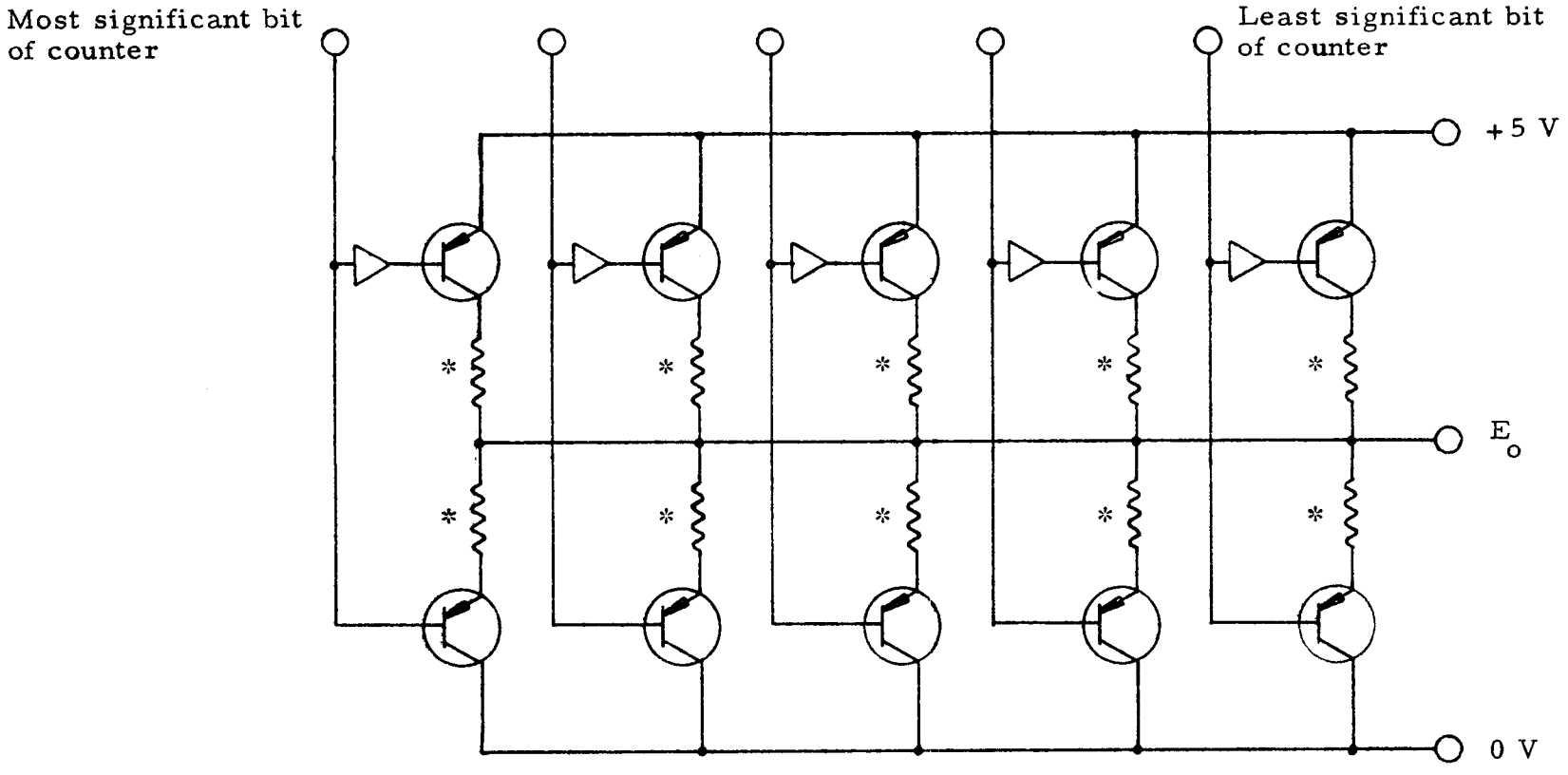

Figure 8. Digital-to-Analog Converter

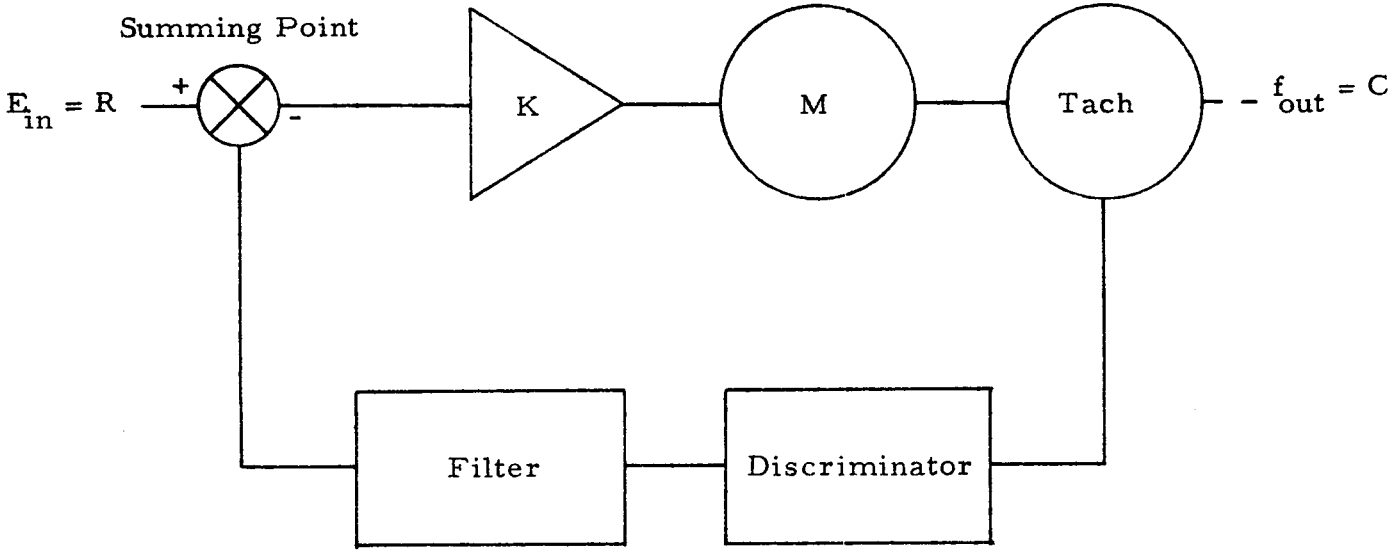

Figure 9. Velocity Servo or "VCO"

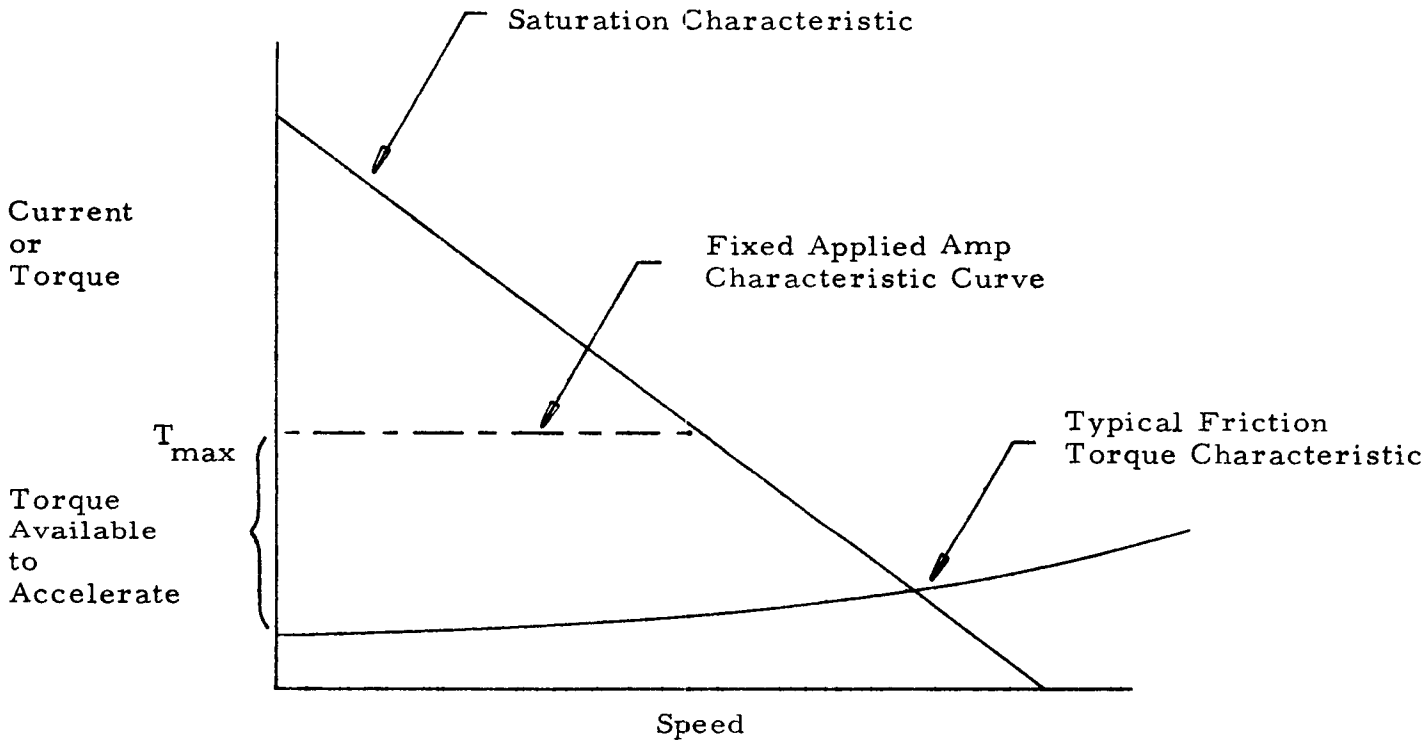

Figure 10. Current or Torque Saturation
(DC Shunt Motor Illustrated)

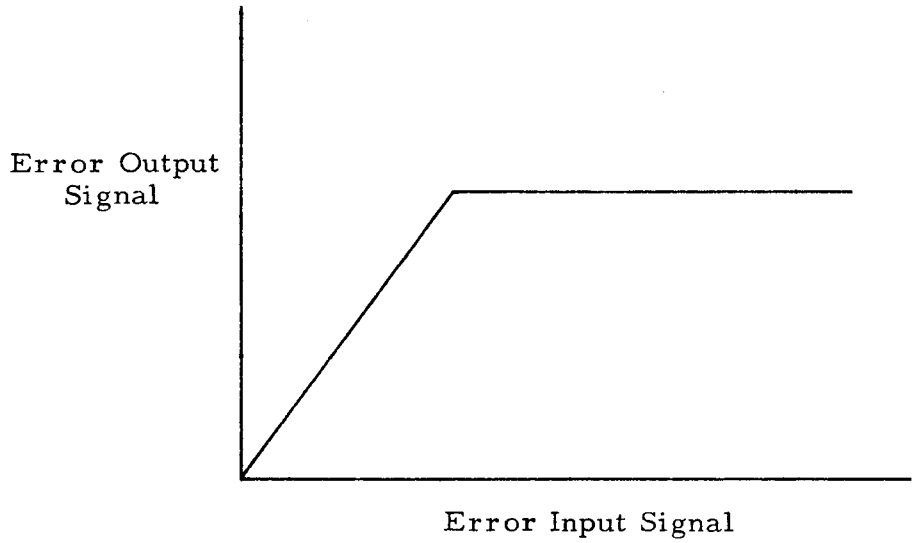

Figure 11. Error Output Saturation Characteristic

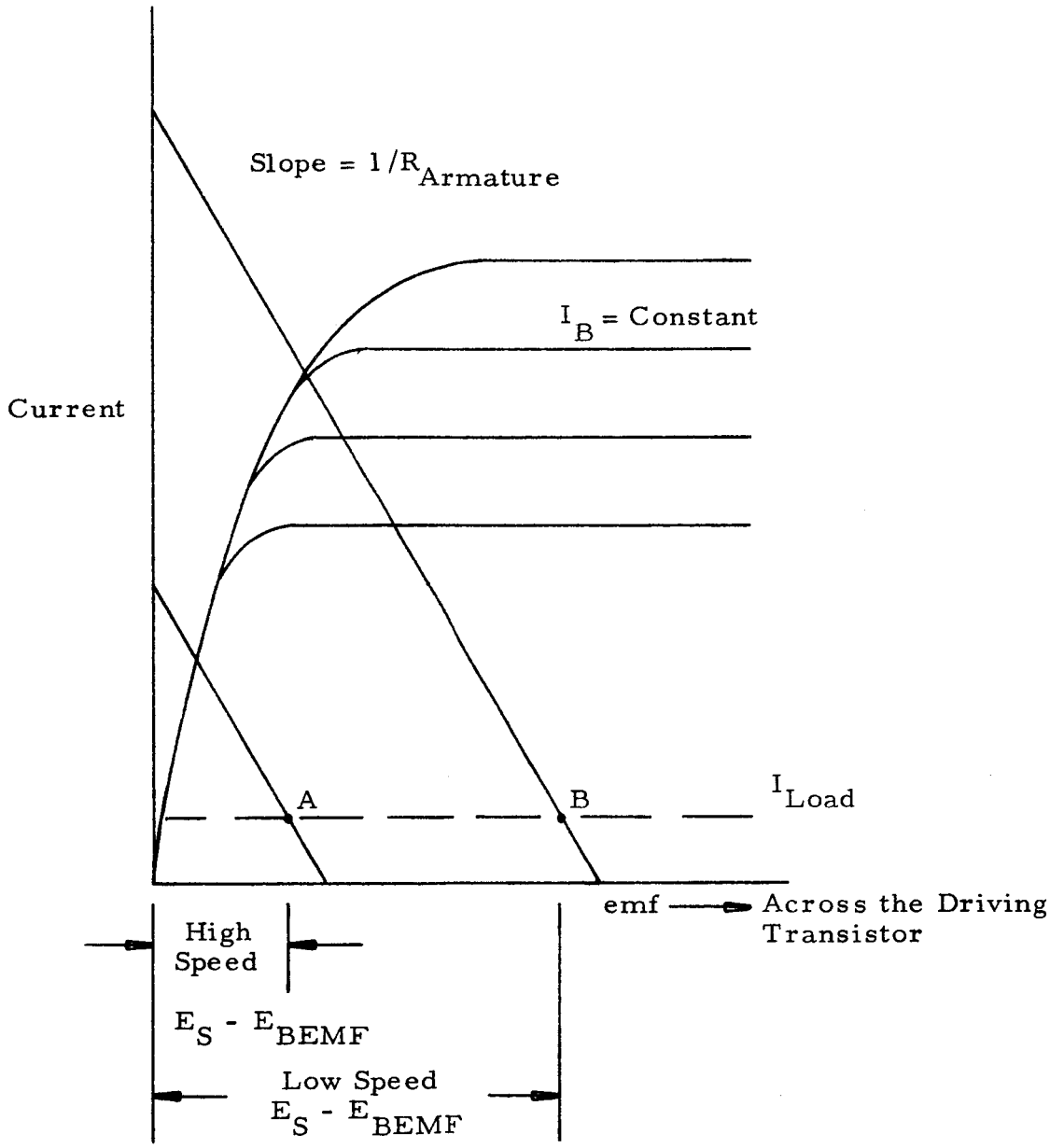

Figure 12. Drive Circuit Current-emf Characteristics

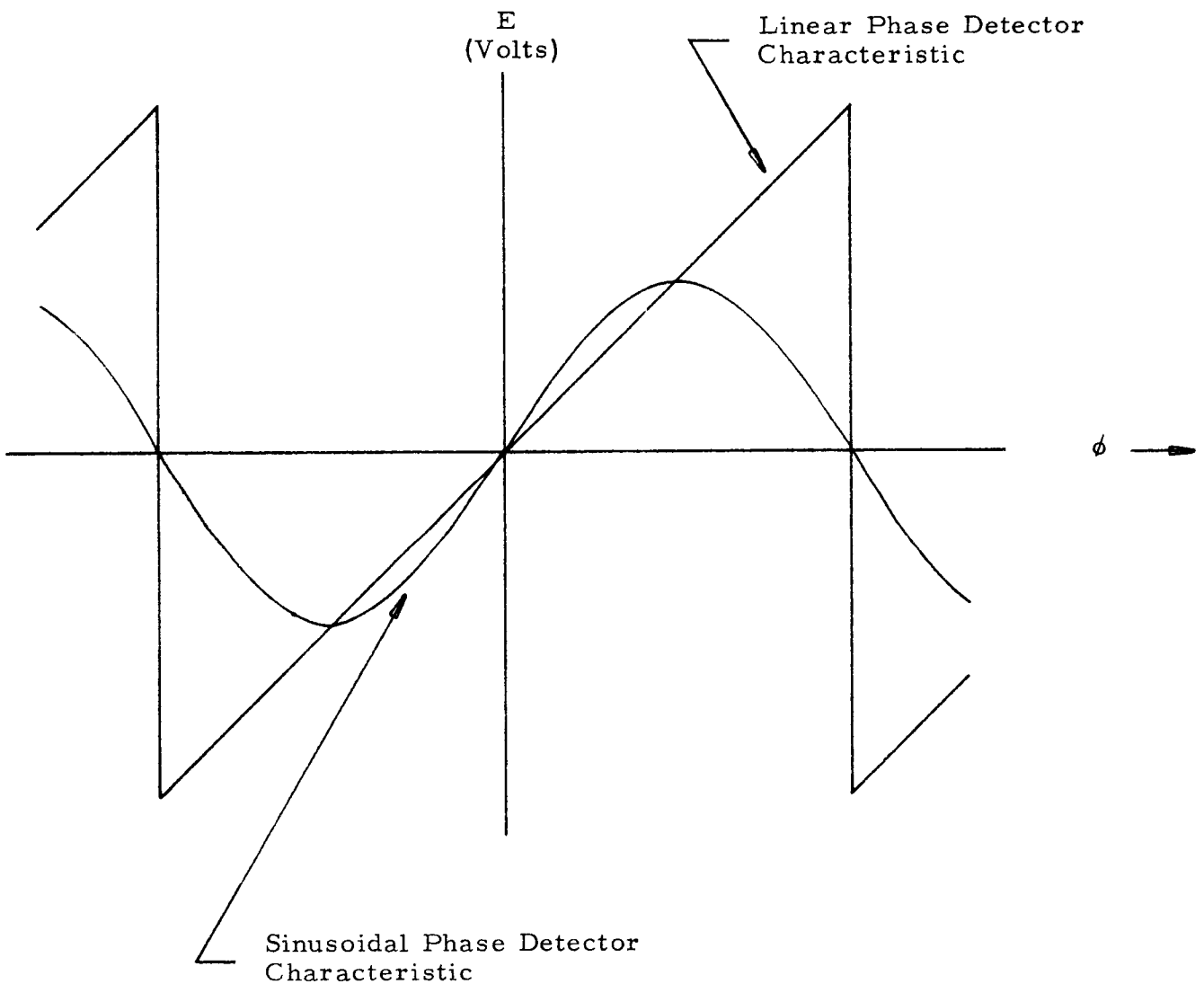

Figure 13. Phase Detector Characteristics

APPENDIX

DERIVATION OF MAXIMUM STORAGE REQUIREMENTS

DERIVATION OF MAXIMUM STORAGE REQUIREMENTS

Storage requirement (in bits) is approximately:

$$\text{storage} = \frac{(\text{data rate})(\text{time to change speed})}{2}$$

Time to change speed (to a first approximation) is:

$$\text{time} = \frac{\text{speed}}{\text{acceleration}}$$

$$= \frac{\text{speed}}{\frac{\text{minimum mean torque of motor - maximum friction torque}}{\text{maximum moment of inertia at the motor}}}$$

$$= \frac{(V)(J_s)}{T_M - T_F}$$

$$\text{storage} = \frac{(\text{data rate})(V)(J_s)}{(2)(T_M - T_F)}$$

The requirements are for a maximum

$$\text{data rate} = 1000 \text{ bps}$$

and the speed reduction is:

$$\text{rad of tape motion} = \frac{2 \text{ rad}}{\text{rev}} \frac{3000 \text{ rev}}{\text{min}} \frac{\text{sec}}{4 \text{ in.}} \frac{\text{min}}{60 \text{ sec}}$$

$$= 25$$

Thus:

$$\text{storage} = \frac{\frac{1000 \text{ bits}}{\text{sec}} \frac{25 \text{ rad}}{\text{in.}} \frac{1 \text{ in.}}{\text{sec}} J_s \frac{\text{gm cm sec}^2}{\text{rad}}}{(2)(T_M - T_F) \text{ gm cm}}$$

$$\text{storage} = 12,500 \frac{J_s}{T_M - T_F}$$

An estimate of the maximum storage requirement may be obtained by looking at a worst case situation. Assume:

$$\text{Accelerating Torque} = 10 \text{ g cm}$$

$$\text{Effective Inertia} = 0.003 \text{ g cm sec}^2$$

Then

Estimated Maximum Storage Requirement

$$= \frac{(12,500)(0.003)}{10}$$

$$= 13 \text{ bits}^*$$

Since the data rate may increase or decrease ± 13 bits are required or 26 bits total.

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*During this development, about double this capacity will be provided to be sure that no bit loss occurs.