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TEN-BIT ANALOG-TO-DIGITAL CONVERTER

by Robert S. Lee

Goddard Space Flight Center
Greenbelt, Md.

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ABSTRACT

The electronic circuits used in a 10-bit analog-to-digital converter are described; also discussed is the method used for analog-to-digital conversion by "sampling and quantizing," in which the digital counts of a data clock are measured in coincidence with a count gate of fixed width, with the input analog voltage controlling the frequency of the data clock. The accuracy achieved with basically standard logic circuits as a major feature of the method is pointed out, as well as the advantages and unusual features of the sampling method.

CONTENTS

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INTRODUCTION

A 10-bit analog-to-digital converter, accurate to within ±1 bit of the least significant digit, has been made possible by a novel use of standard electronic circuits. The analog-to-digital conversion is done by "sampling and quantizing" (Reference 1), in which the digital counts of a data clock are measured in coincidence with a count gate of fixed width, while the frequency of the data clock is controlled by the input analog voltage. The accuracy thus achieved with basically standard logic circuits was heretofore considered impossible.

This A/D converter, installed in NASA Aerobee 4.145 (launched from White Sands Missile Range, New Mexico, on December 2, 1965) was successfully used to monitor the temperature of a temperature-sensitive optical birefringent filter with the temperature being controlled to ±0.1°C (Reference 2). The accuracy of the analog data channels available on this type of rocket was insufficient to permit transmission of this temperature data back to the ground station.

BLOCK DIAGRAM DESCRIPTION

Figure 1 shows a block diagram of the A/D converter. The word gate command triggers on the count gate one-shot for a period consistent with the RC time constant chosen. The pulses from the data clock are allowed to flow through a two-transistor NAND gate to fill the 10-stage binary counter in coincidence with the count gate one-shot. The NAND gate cuts off the count at the end of this count gate period, and the trailing edge of the count gate wave form is used to set a set-reset flip-flop, which unclamps the unijunction transistor readout clock. NAND-AND logic is then used to read out sequentially the counts stored in the 10-stage flip-flop counter.

When all stages of the 10-stage counter are read out, the set-reset flip-flop is reset to clamp the readout clock. At the same time, all the flip-flop counters are reset to zero, and the converter is ready for the next word gate command.

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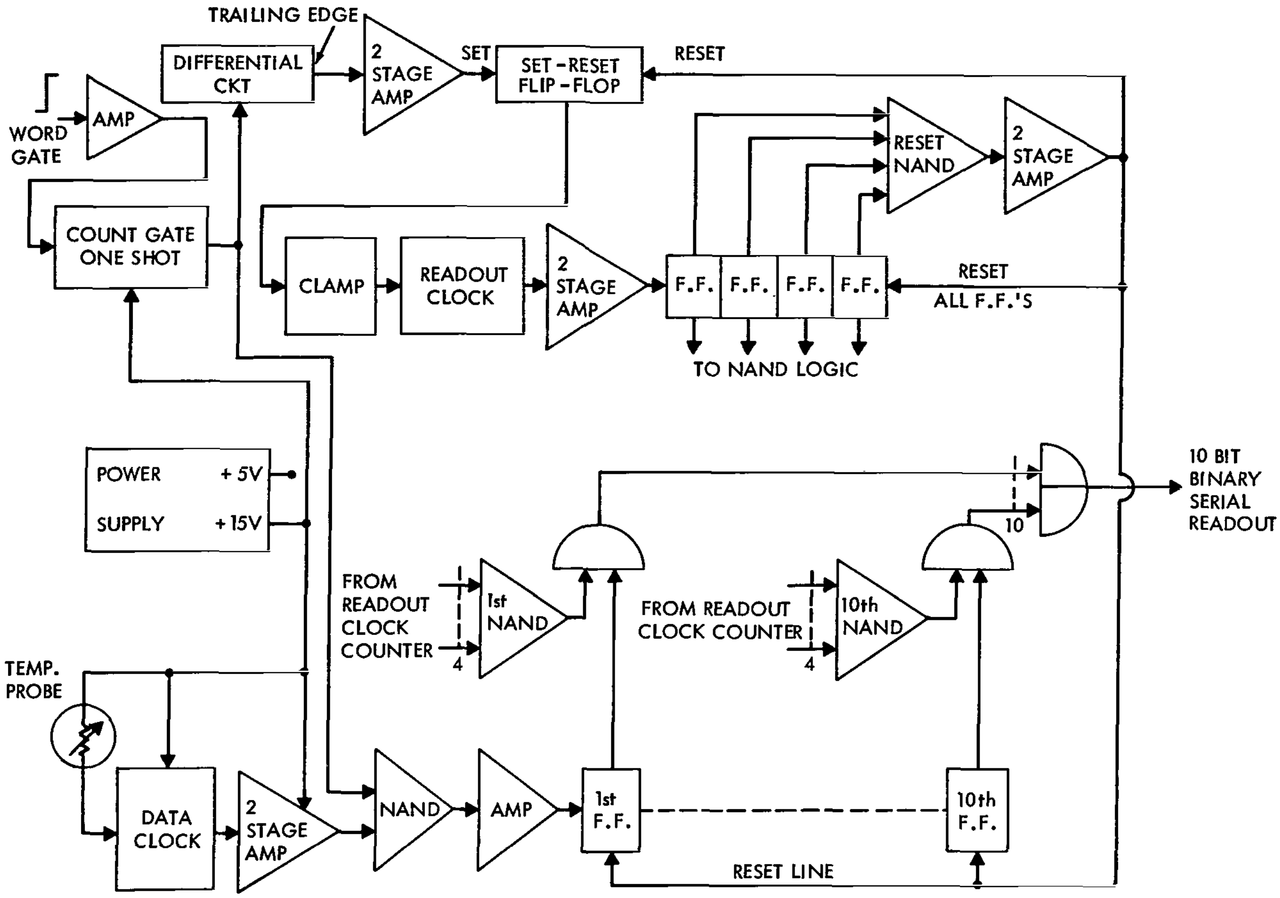

Figure 1—The A/D converter block diagram.

DATA CLOCK AND COUNT GATE

The heart of this A/D converter is a unijunction transistor clock used in conjunction with a one-shot count gate. Temperature compensation in these two circuits is critical. The clock frequency can be changed only by the input analog voltage, while the width of the count gate must remain stable throughout the designed temperature range. In these two circuits, metal film resistors and silver mica or mylar capacitors must be used in places where the RC time constant might be affected by value changes of the components because of ambient temperature change. Temperature compensation must be made with the two circuits treated as a unit.

The schematic diagram (Figure 2) shows that both positive and negative temperature coefficient resistors were used in the data clock circuit to achieve the temperature stability necessary. The results of temperature compensations are shown in Table 1.

A careful study of the schematic diagram (Figure 2) will reveal obvious limitations in this system. The data clock will not work with an analog signal less than the threshold of the unijunction transistor. Unless a linear amplifier is added in front of the data clock, an analog signal of less than one volt would make the operation of the data clock uncertain.

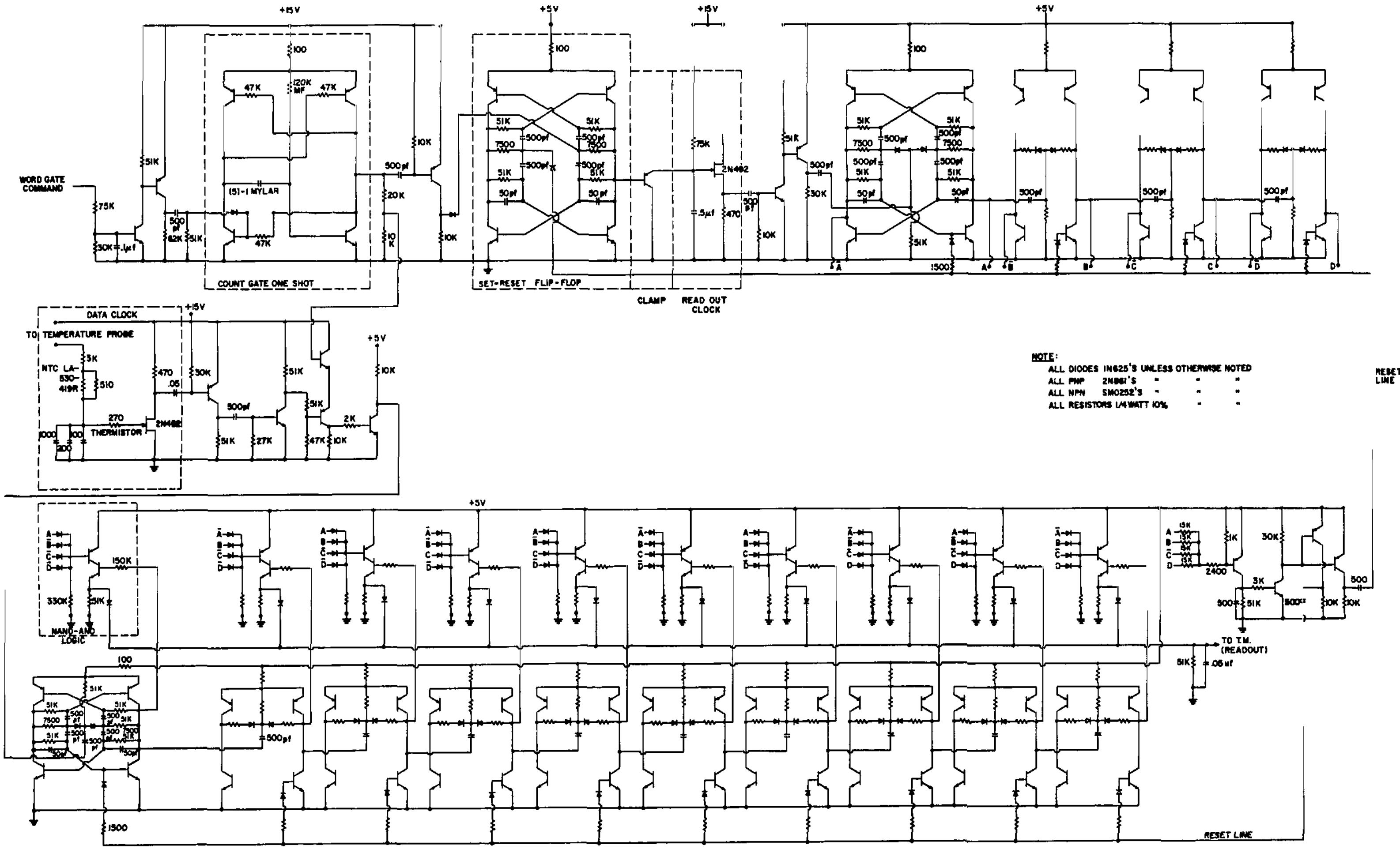

Figure 2—Schematic diagram of the analog-to-digital converter.

These limitations should not appreciably affect the adaptability of the A/D converter, since the expected signal is predictable in the majority of satellite and rocket experiments.

An alternate application of the data clock and count gate to digitize the analog signal would be to use a fixed frequency clock and to control the width of the count gate by the analog signal.

The calibration of the unit herein presented was such that approximately 3.0V input filled the counter (1023 counts), so that the least significant bit represented 3 mV. Final calibration of the flight temperature probe (temperature in °C versus digital count) is shown in Figure 3.

NAND-AND READOUT GATES

A NAND-AND logic shift register was used to read out sequentially the counts stored in the 10-stage counter. This shift register saved six flip-flop stages, inasmuch as a conventional flip-flop shift register requires 10 flip-flop stages to read out 10 bits.

As can be seen from Figure 2, if +5V is applied to the anode of one or more of the four diodes in the first NAND gate, the PNP transistor is biased off. However, when all the anodes of the four diodes are clamped to ground (the 4-stage counter of the readout clock is in the state of A, $\overline{B}$, $\overline{C}$, and $\overline{D}$), the 330k resistor will bias the PNP transistor on. Whether readout will occur then depends on the state of the first flip-flop in the 10-stage counter. If there is a count, the first flip-flop is on (+5V), turning the NPN transistor on, and readout occurs.

The remaining nine NAND-AND gates are connected to the 4-stage readout clock, as shown in Table 2.

Table 1

Data Clock and Count Gate Temperature Compensation.

Supply Voltage (V)	Temperature (°F)	Counts
+27	+74	1005
+30	+74	1005
+35	+74	1005
+27	+30	1004
+30	+30	1005
+35	+30	1005
+27	+120	1006
+30	+120	1006
+35	+120	1006

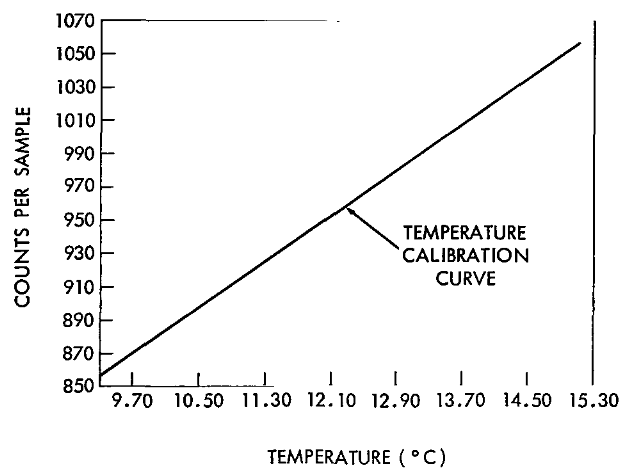

Figure 3—Final calibration of the flight temperature probe.

Table 2

Logic Truth Table for the NAND-AND Readout Gates.

Flip-Flop	NAND Gate 0	1	2	3	4	5	6	7	8	9	10	Reset NAND
1	0	1	0	1	0	1	0	1	0	1	0	1
2	0	0	1	1	0	0	1	1	0	0	1	1
3	0	0	0	0	1	1	1	1	0	0	0	0
4	0	0	0	0	0	0	0	0	1	1	1	1

The counts stored in the 10-stage flip-flop are read out sequentially by the 10 NAND-AND gates, and the outputs of the NAND-AND gates are OR'd together to the telemetry input line. The 11th pulse of the readout clock resets all the flip-flops to zero, at the same time resetting the set-reset flip-flop, and clamps the readout clock by clamping the emitter of the unijunction transistor to ground through the PNP transistor.

POWER REQUIREMENTS

As is shown in the schematic diagram (Figure 2), the circuit requires +15V and +5V. The power supply requirements are +15V at 4.1 ma, +5V at 6.7 ma.

The +15V must be highly regulated. The output voltage of this supply should change less than ±0.50 percent under any combination of the following conditions: input voltage change from +25V to +35V, ambient temperature change from +30°F to +120°F, and load change. Any significant change in the +15V will change the frequency of the data clock and the width of the count gate. For the sake of good regulation and efficiency a pulse-rate-modulated regulator was used in the circuit described.

A fair amount of voltage change (±10 percent) in the +5V supply would not affect the accuracy of the circuit; therefore, a simple zener-regulated supply was used.

Total power consumption of this circuit is 212 mw (28V at 7.6 ma.).

SPECIFICATIONS

Mechanical

(a) Size: 12.5 cubic inches. (The unit used was packaged in an L-shape box because of space limitation.)

(b) Weight: 420 grams.

(c) Circuit boards dipped in commercially available epoxy.

(d) Vibration: 10 G, 5-2000 cps, sine and random on all three axes.

Electrical

(a) Power supply voltage:

(1) ±15V ±0.5 percent at 4.1 ma for all conditions of input voltage and temperature change.

(2) ±5V ±10 percent at 6.7 ma for all conditions stated above.

(b) Temperature: +30°F to +120°F.

(c) Word gate command: +28V, rise time 1 micro-second.

(d) Word rate: one per second.

(e) Readout: 51k output impedance, least significant bit first.

CONCLUSIONS

The final version of this circuit has many novel features. The writer is not aware of any other A/D converter qualified for spaceflight use that is capable of more than 9-bit resolution.

One of the methods most commonly used for A/D conversion is "successive approximation," in which an extremely stable reference voltage is necessary. For A/D converters using the successive approximation technique with resolution better than 8 bits, an oven is necessary for the reference voltage circuit, resulting in increased overall size, weight, and power consumption.

Another advantage of the sampling method is the ease with which the range of the input analog voltage may be changed. A simple change in clock frequency and/or adjustment of the width of the count gate will accomplish this, whereas to change the range of the input analog voltage in circuits using the successive approximation method would be a sizable task.

To conserve power, complementary four-transistor flip-flops were used instead of standard two-transistor flip-flops. Should package size and weight have higher priority than power consumption, then micro-electronics chips can be used for all flip-flops, one shots, and NAND gates.

ACKNOWLEDGMENTS

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National Aeronautics and Space Administration
Greenbelt, Maryland, April 14, 1966
879-10-03-01-51

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NASA-Langley, 1967 —— 9

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