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06988-6001-R000

TEMPERATURE CONTROL FLUX MONITOR FOR MARINER MARS 1969

DEFINITION STUDY REPORT

CONTRACT NO. 951726

DECEMBER 9, 1966

Prepared for

JET PROPULSION LABORATORY

TRW SYSTEMS
AN OPERATING GROUP OF TRW INC.

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0. INTRODUCTION

This report presents the design of the Temperature Control Flux Monitor (TCFM), which has been developed during the Phase I Study of the requirements for the flight adaptation of the JPL Absolute Cavity Radiometer concept.

The major effort during this study has been appropriately directed toward obtaining a timely and detailed definition of the control and measurement circuitry necessary to meet specified Mariner Mars 1969 spacecraft interface requirements.

Of the several approaches considered during the study, the one which has been selected, and which is described in this report, is judged to be best capable of meeting the major requirements of long term stability, telemetered accuracy and reduced packaging volume.

The design for the TCFM Electronic Control Assembly presented herein is based on circuit techniques which are well founded in digital computer design and technology.

To assure that the temperature control approach utilized in the TCFM Electronic System is basically sound, a cursory dynamic analysis has been performed. The results of this preliminary analysis are included in this report.

Comparatively less effort has been directed in the study toward detailed definition of the transducer since it has been recognized that the design of this portion of the system is relatively well established. Sufficient study and consideration have been devoted to this area, however, to assure overall compatibility of the TCFM system.

1.1 SYSTEM DESCRIPTION

The Temperature Control Flux Monitor (TCFM) for Mariner Mars 1969 will be used for measurements of thermal radiation incident on the spacecraft in its transit from the near Earth environment to the near Mars environment. To accomplish the measurements to the degree of absolute accuracy desired and necessary to advance the state of the art in this regard, a comprehensive instrument system development program is proposed.

The basis for the study development effort is the guarded conical cavity thermal radiation detector concept. The essential aspects of this concept have been the subject of a pioneering development effort by JPL which has resulted in laboratory models of the instrument. Tests of these prototypes have proved the practicability of the concept and have demonstrated that the basic approach is capable of a new order of measurement accuracy.

This study describes the development of the flight adaptation of this instrument concept. The adaptation to space vehicle application imposes physical and electrical constraints not demanded for ground or laboratory applications. In particular, consideration was given to a new order of volume, weight, power, reliability, telemetry, and environmental requirements as well as to the compatability with the Mariner Mars 1969 spacecraft system.

In light of these requirements and interfaces, a TCFM system has been devised during this preliminary study and definition effort. The devised system is capable of achieving the performance characteristics and as such it complies with the design guidelines set forth in Exhibits I, II and III of the subject contract.

Basically the TCFM System consists of a transducer, an electronic control and instrumentation unit, and compatible operational support equipment for ground test and operation of the system.

The electronic system accurately controls the temperatures of the transducer's thermal guard and conical element, provides for in-flight measurements of conical element power, for in-flight measurement of set point temperature of the thermal guards, and for measurement of the cone/

guard temperature unbalance (error). Provisions are also included for spacecraft system ground test measurement of additional parameters which may be required.

The approach selected is entirely compatible with the use of integrated circuits throughout the system. There appears to be no reason why volume and weight targets cannot be met.

The electronic control system effectively duplicates the desirable functions of the control and auxiliary equipment utilized in the JPL extensive laboratory TCFM experiments. The approach is essentially digital, to achieve and maintain the required accuracy of measurements. The measured data will be continuously available for transmission to the ground over two seven-bit digital telemetry channels, upon receipt of proper commands from the TM system.

The TM data must be digital in form to preserve the desired accuracy of measurement of 0.5% of cone power. An analog approach to the control of the guard and cone temperatures would be considerably more complex than the approach proposed for systems of the same measurement accuracy. The complexity would accrue from the requirement for an analog to digital converter to convert the cone heater voltage to the required 10 bit binary number. Furthermore, the proposed digital approach makes use of common circuitry in the two servo loops which would not be possible to perform in an analog system.

It is believed that the studied digital approach is the optimum within the specified constraints of weight, power consumption and accuracy.

1.2 TRANSDUCERS

The design of the transducer for the spacecraft operational TCFM retains the essential features of the JPL Absolute Cavity Radiometer described in exhibits furnished by JPL. The guarded conical cavity sensing concept embodied in this design is capable of providing a high order of accuracy in the measurement of total radiation. Modifications to the original design may be required, however, in order (1) to meet Mariner 1969 system requirements; (2) to improve detailed performance aspects; (3) to be compatible with the flight version TCFM control electronics system; and (4) to alleviate minor fabrication and assembly difficulties that have been brought to light through JPL's in-house experience in producing current prototypes. The modifications presently studied in no way degrade the inherent measurement capability of the transducer.

The most significant modification under consideration involves the use of a light metal for the transducer's thermal guard structure to effect a lower overall unit weight. Such a weight reduction is desirable to minimize launch load deflection of the antenna ground plane structure which supports the transducer on the spacecraft. A preliminary thermal analysis of the inner guard indicates that the direct substitution of 6061 aluminum alloy for the existent copper (without dimensional change) will result in a temperature gradient of only $0.2^{\circ}K$ longitudinally along the guard. This would effect a 50% reduction in the transducer weight to approximately 0.18 lb. A further reduction in weight can be realized by the use of magnesium alloy which would effect a temperature gradient in the order of $0.3^{\circ}K$ along the guard and a transducer weight of 0.14 lb.

There appears to be no substantial basis for reduction of the dimensions of the conical receiver (23° cone angle and 0.435 in. aperture diameter). In fact, assessment of the parasitic thermal losses from the guarded cavity indicates that a higher absolute accuracy may be achieved by a cone of larger aperture, specifically in consideration of annular gap radiant losses, and cone support and electrical lead wire conduction losses.

For example, radiation to or from the cone through the aperture annular gap results in some ambiguity in the effective area of the receiver. A gap of 0.001 inch (0.025 mm) appears to be the minimum width which can be practically controlled, yet this represents an area which is 0.8% of the design area of the conical cavity. While the uncertainty in effective aperture area, due to radiation through the gap, is not as great as 0.8%, it nevertheless results in an undesirable reduction in the absolute accuracy of the instrument. To reduce this uncertainty by a significant amount, say one half, it would be necessary to increase the aperture of the cone by a factor of two. This would result in an increase in transducer weight of 50% and an increase in guard power of 100%, both of which are undesirable.

In this regard, consideration has been given to the incorporation of a small rim at the guard aperture opening which would act as a radiation stop in front of the annular gap. In effect, this would recess the rim of the cone by some amount. For on-axis collimated radiation no error would be introduced by the limiting aperture stop. For hemispherical radiation, however, the cone recess would introduce an error since the receiver would no longer have a 2π solid view angle.

The amount of this error is proportional to the difference between the actual reception angle and the ideal or hemispheric view angle. A projecting rim whose thickness is 0.008 inch would limit the reception angle of the cone to 176°. This would result in an error of 0.3% in the instrument's response when subjected to hemispherical radiation. However since the magnitude and direction of the error is known, a correction can be applied for conditions of incident hemispherical radiation.

In order to minimize the electrical power required to control the transducer guard temperature (since this reflects on the capacity and size of the electronic components) and to minimize variations in the required heater power, it is desirable to decouple the transducer from the environment to a practical extent. The Mariner antenna structure to which the TCFM transducer is attached is expected to undergo a 70°C change in temperature in the transit from Earth to Mars. Similarly, the incident flux (solar) varies through a range of 3 to 1. Both of these conditions impose a varying thermal load on the guard controller which is undesirable.

It is desirable to minimize the electrical power required to control the transducer guard temperature since this reflects on the capacity and size of the electronic components. Ideally, since two power control systems are required, it would be convenient if both were of identical design and capacity.

A radiometer cone of 1 cm^2 aperture operating in the range of 420°K requires a steady electrical power of about 0.18 watt when viewing cold space. This sets the nominal power capability of the system. For the guard power requirements to also be of this order will require effective control of the radiometer losses. It will be necessary to decouple the transducer from those components of the thermal environment which undergo a wide change, i.e., conduction losses to the structural attachment and the solar input at the frontal area of the radiometer.

While it is desirable to isolate the transducer, some losses from the system are necessary so that electrical power must always be applied to retain positive temperature control of the guard.

Analyses and assessment of the losses from the system indicate that, by appropriate design of the mount and the selection of an exterior finish with the proper thermal radiation properties, the power capacity requirements of both sections of the electronic control unit can be made similar.

Figure 1.2-1 shows the essential features of the transducer. The conical element is to be electroformed silver, machined to the final dimensions. The cone will contain two independent bifilar windings: one of constant resistance wire to be used as the electrical cone heater, and the other of platinum wire to be used as a resistance thermometer for sensing the temperature of the cone.

The thermal guard is expected to be fabricated from aluminum or magnesium alloy. The thermal guard temperature sensor assembly will contain three independent windings used for the following purposes:

- Guard Set point temperature control sensor
- Guard Set point temperature measurement sensor
- Guard Cone differential temperature control sensor

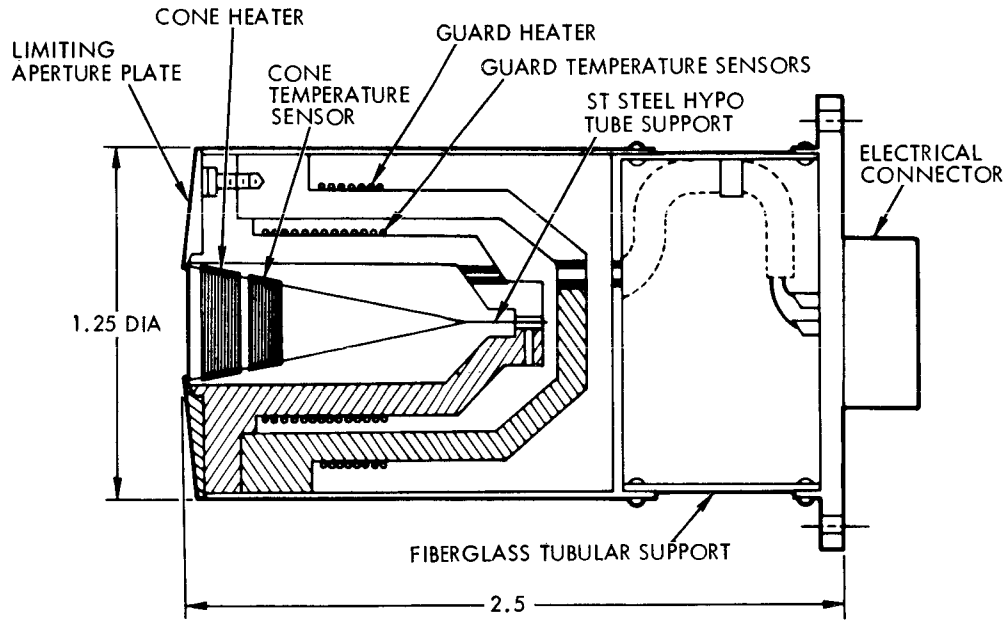


Figure 1.2-1 Transducer Configuration

Independent windings are utilized for each function to preclude the necessity for electronic switching of a single sensor to each of the necessary functions. It is planned to utilize one mil diameter Pt wire (60 ohms/ft) for all temperature sensors. Thus, relatively few turns will be required to obtain sufficient sensitivity. It is not anticipated that physical dimensions will pose a problem in accommodating the necessary sensor or heater windings in the transducer if small wire diameters are used.

Figure 1.2-1 illustrates certain design features of the transducer which may be considered in the detailed design of the instrument and which deviate somewhat from the existing JPL prototype.

The thermal guard structure is joined at the thermal interface of the two sections. A joint filler of about one mil thickness is used to reduce the resistance at the interface. If a silver filled epoxy is used the differential temperature across the joint will be less that $0.1^{\circ}K$ at maximum heat flux. The construction shown allows winding the guard temperature sensor windings directly on the guard structure.

An aperture limiting stop secured to the front face of the radiometer is shown. The advantage in using a separate plate for this stop, over incorporating it into the inner guard structure, is that the alignment and clearances of the cone in the guard may be verified before the stop is applied. Here again a joint filler would be used to lower the interface resistance. At a flux of 0.140 watts/cm^2 incident on the front face of the radiometer, the temperature differential across the stop/guard interface is less than $0.01^{\circ}K$.

1.3 TCFM ELECTRONIC CONTROL SYSTEM

1.3.1 Technical Approach

It is desired to maintain the TCFM sensor guard and the cone at a constant temperature and to provide telemetry data which accurately represent the amount of power required to maintain the cone at this temperature. The described system will control the guard and the cone temperature and will provide telemetry data representing cone power to an accuracy of better than 0.5%.

Although both analog and digital telemetry channels are available, digital channels are chosen because of the accuracy requirement. It is therefore necessary to develop digital data that accurately represents the required cone heater power. This could be done by holding the cone temperature constant by means of a servo control loop and digitizing either the voltage across, or the current through, the heater element (provided the heater resistance is accurately known). If the heater resistance is not accurately known, both the voltage and the current must be measured.

The accuracy requirement suggests a control loop with reset (integration). The reset feature reduces the system loop gain required by about 60 db and eases the error amplifier drift requirement.

The studied system effectively incorporates an A-D converter in the control loop. This element contains a 10 bit binary register. With the control loop at equilibrium this register contains a number which accurately represents heater power. This number will remain unaltered until an error signal dictates a change. The register, therefore, provides the reset (integration) function. Two control loops are required since the guard and cone heaters must be controlled separately. In the proposed system, the two control loops time share a number of common elements to reduce the required number of components. The cone register number and the error magnitude are transferred to the TM data register every 0.213 minute as two words of 7 bits each. The data in the two 7-bit TM registers are always available upon receipt of alert commands from the TM system. The two channels can be shifted out to the TM system with no constraint on the time between successive alert commands.

No new data will be transferred into the TM data registers while the shift operation is in progress. The voltage and impedance levels and the rise and fall times of the output signals are compatible with the TM system.

The studied system effectively duplicates the functions of the laboratory type 3 mode controllers and auxiliary equipment used in the TCFM laboratory experiments at the Jet Propulsion Laboratories and, in addition, provides for high accuracy digital readout.

The electronic system will be contained in two 1-3/16 inch wide standard Mariner subchassis. There will be unused space in one of the modules that could be used for some form of analog data multiplexer if desired.

1.3.2 Theory of Operation

1.3.2.1 General

A simplified block diagram of the studied system is shown in Figure 1.3-1.

The power to the heater is determined by a form of duty cycle control. The duty cycle is varied by varying the number of constant width constant peak voltage pulses in a given interval of time. The number of pulses can be varied from 0 to 1023 in a 0.213 second period (frame) in one pulse increments. These pulses are generated by counting down the 2400 pps spacecraft clock with a 9 stage binary divider chain and combining the various binary outputs in logic gates.

The width of one pulse is the width of 1/2 cycle of the 2400 pps clock. The duty cycle gates are controlled by a 10-bit register (termed data register) in such a way that the number of heater pulses per frame time is precisely equal to the number in the data register. In this manner, the number in the data register both controls and represents the power being delivered to the heater. A difference in the amount of power being supplied and the amount of power required to maintain the heated element (cone or guard) at a constant and predetermined temperature will cause an imbalance in the AC excited temperature sensing bridge. The signal resulting from this imbalance is amplified and analyzed by the error detector.

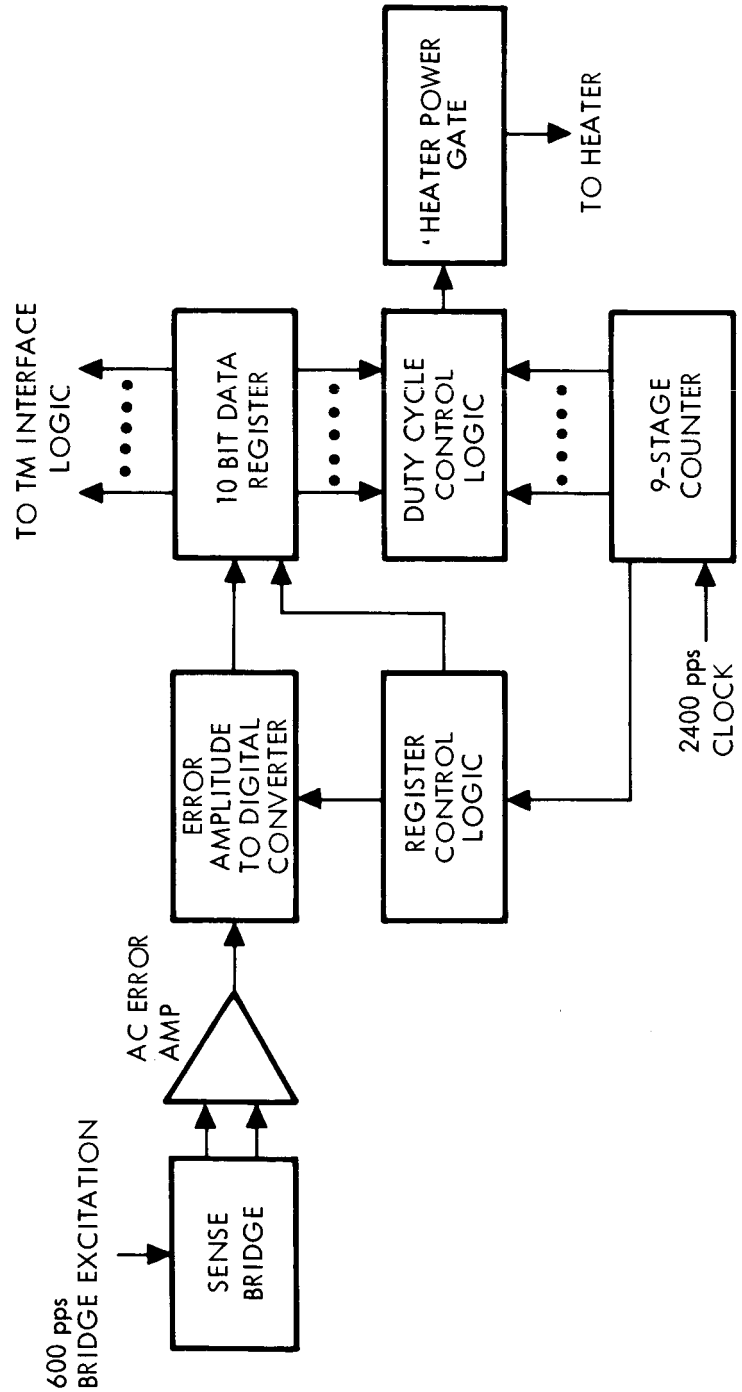


Figure 1.3-1 Simplified Block Diagram Digital Heater Control

The error detector determines the magnitude and direction of the error once each frame time (every 0.213 second) and causes a correction to be made in the number contained in the data register. The error magnitude is quantized into eight levels and the data register number is therefore changed by one of eight discrete amounts each frame time. The direction of the error determines whether the register count is increased or decreased. The system acts to reduce the error at the input of the error detector to zero.

The number in the data register represents the integrated error signal and constitutes reset. The control loop is, by definition, a Type 1 servo system in that a steady state change in required heater power will not result in an error in supplied heater power.

The more complete block diagram of Figure 1.3-2 shows the telemetry interface logic and the means of controlling both the guard and cone heaters by using common elements in the two control loops. The use of a number of the elements to control both servo loops is possible because each data register is updated once each frame time and the updating only requires a few milliseconds out of the frame time of 0.213 second. The error detection and register control circuitry can be used for both the guard and cone loops simply by updating the two data registers at different times.

There are 1024 pulses during each frame time. It is necessary to omit one of these pulses to provide the one-to-one correspondence between the data register count and the number of heater pulses per frame time. This provides a convenient time to update the data registers since altering the register count during this time will not introduce a transient in the heater power waveform. The system is organized to cause the unused pulse times to occur at different times for the cone and guard control loops. The mechanization of this approach is discussed in detail in subsequent paragraphs.

1.3.2.2 System Details

The following paragraphs discuss the various functional blocks comprising the system in detail. Block diagrams and timing diagrams

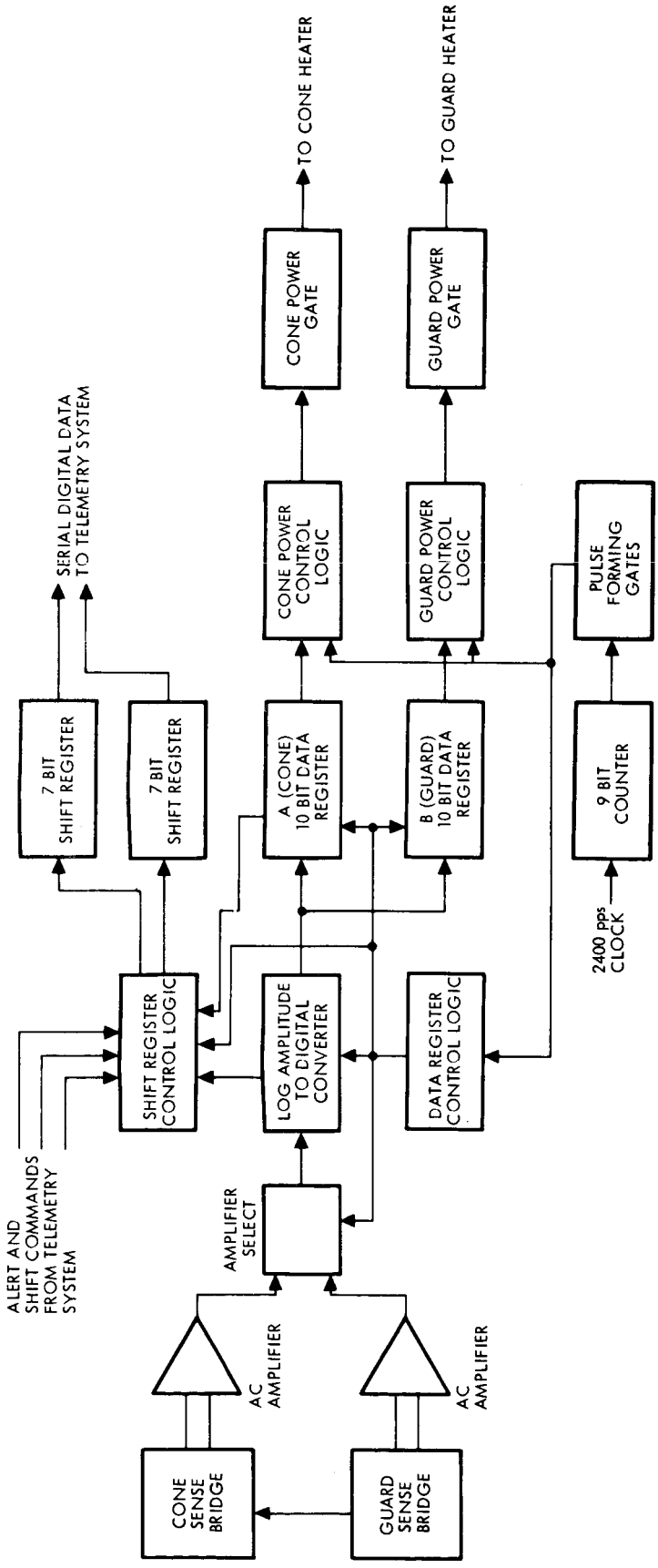


Figure 1.3-2 TCFM Logic Block Diagram

are included where deemed desirable to convey a full understanding of the system.

The functions discussed in detail are the 9 stage divider chain and associated duty cycle gates, the heater power gate details, the configuration and operation of the error sensing bridges and associated error amplifiers, the error detection and analysis section, the data register and logic control section, and the TM interface section. In addition, the provision for calibration and the signals available for verification of proper equipment operation are also discussed.

The primary logic elements employed in the studied system are the NAND gate and the RST flip-flop which are defined in Figure 1.3-3.

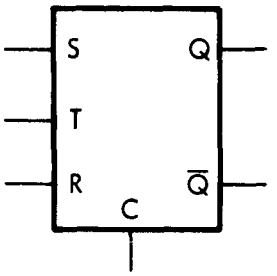
Nine-Bit Divider Chain and Duty Cycle Gates

The nine-bit divider chain is used to divide down the 2400 pps spacecraft clock to generate master timing signals and to develop the necessary logic combinations to provide variable duty cycle waveforms to power the cone and guard heaters. It appears that the spacecraft 2400 pps clock cannot be used directly because of possible variations in symmetry. It is desired that the clock input to the 9-stage divider be symmetrical within 0.1% or better as any lack of symmetry will result in an error between the number contained in the data register(s) and the power delivered to the heater(s). It is, therefore, proposed that the spacecraft clock be multiplied by a harmonic multiplier (quadrupler), then shaped and divided by four to yield a suitably symmetrical clock.

The 2400 pps clock is termed X0 and the successive stages of the divider are termed X1 through X9. The output of X1 will have a 1200 pps rate, X2 a 600 pps rate, and so on, with X9 having a rate of 75/16 pps for a wave form period of approximately 0.213 second. It is the period of X9 that determines the previously discussed frame time.

A logic block diagram of the 9-stage divider and the associated duty cycle gates is shown in Figure 1.3-4. The X0 through X9 are logically combined in two sets of gates that are controlled respectively by the A0 through A9 outputs of the cone data register and B0 through B9 outputs of the guard data register.

RST FLIP FLOP

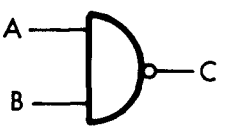


TRUTH TABLE

INPUTS AT tn		OUTPUTS AT tn		AT tn + 1	
R	S	$\overline{Q}$	Q	$\overline{Q}$	Q
0	0	0	1	0	1
0	1	1	0	0	1
1	0	0	1	1	0
1	1	INDETERMINATE			

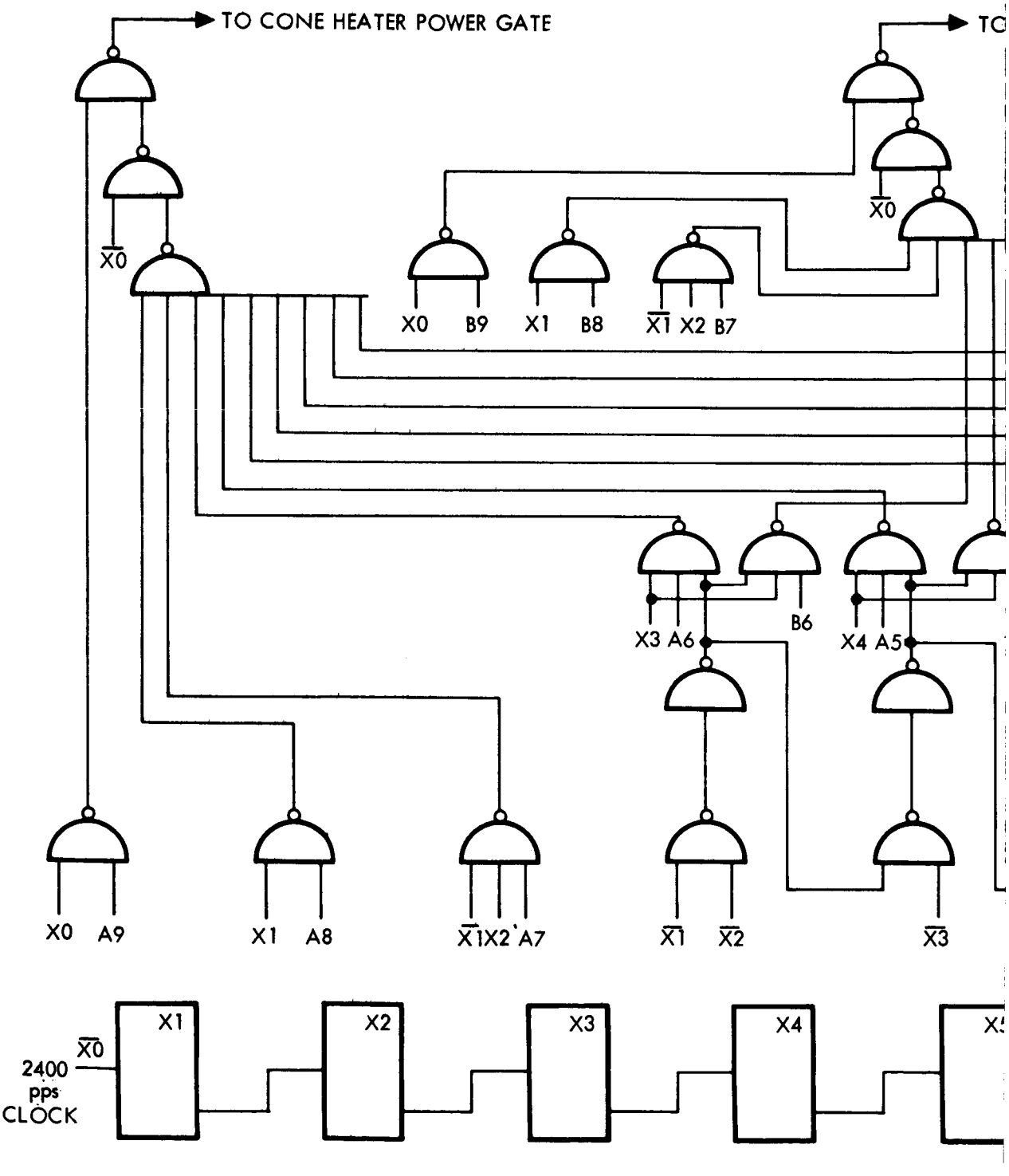
T IS CLOCK PULSE INPUT
C IS CLEAR INPUT
TRUE INPUT AT C WILL CAUSE
$\overline{Q}$ TO BECOME TRUE

NAND GATE



$C = \overline{A \cdot B} = \overline{A} + \overline{B}$

Figure 1.3-3 Logic Symbol Definitions


TO CONE HEATER POWER GATE
TO
X0
X0
X0 B9
X1 B8
X1 X2 B7
B6
X3 A6
X4 A5
X0 A9
X1 A8
X1X2 A7
X1
X2
X3
2400 pps CLOCK
X0
X1
X2
X3
X4

GUARD HEATER POWER GATE

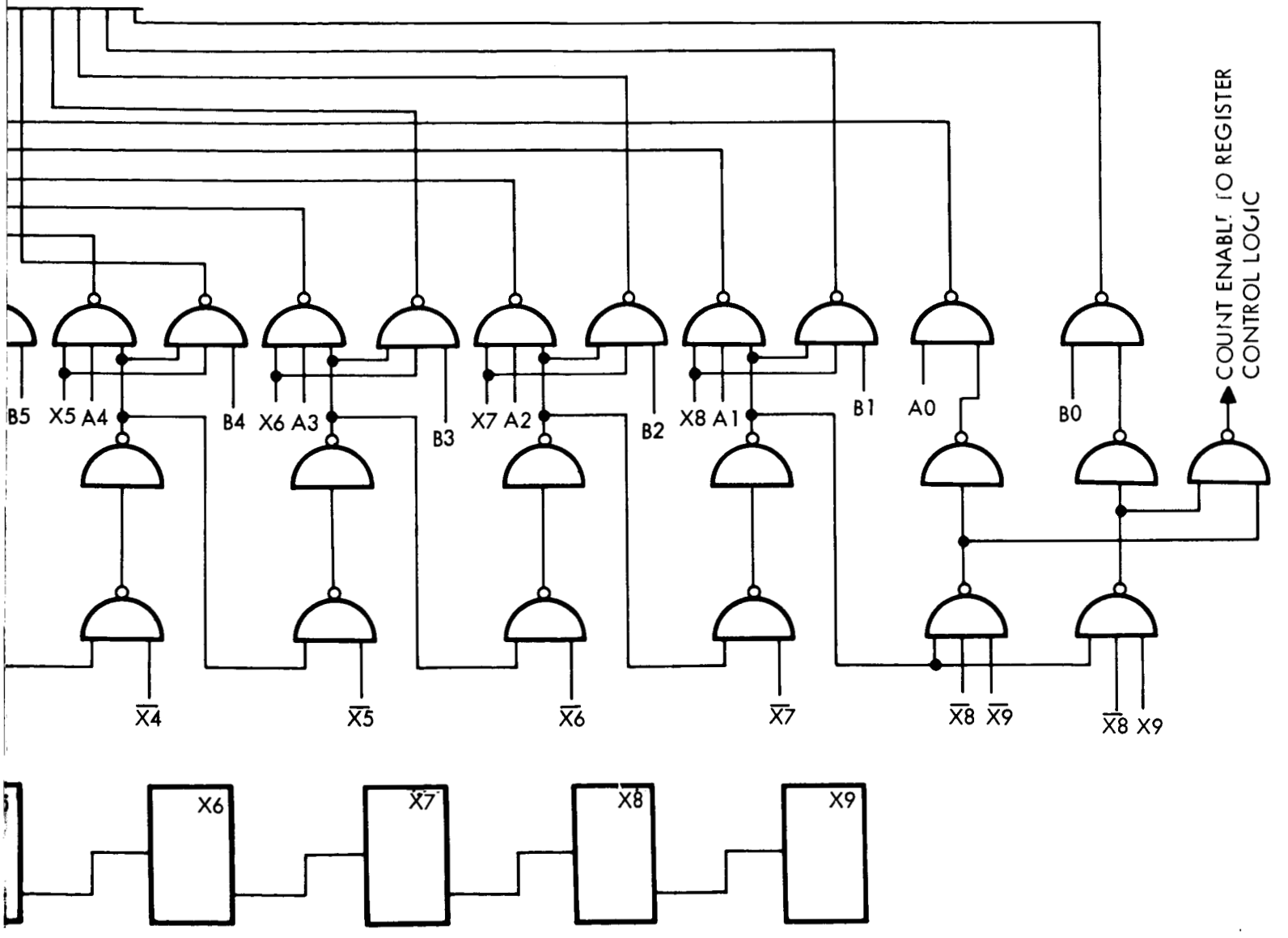


Figure 1.3-4 Nine Stage Counter and Duty Cycle Control Logic

Each gate, when enabled by its A or B control signal, contributes a precise number of power pulses to its corresponding heater element during each 0.213 second frame time. The width (time duration) of each of these pulses is equal to one-half the period of the clock X0. There are 10 contributing terms each for the cone and guard channels that allow any number of pulses from 0 to 1023 in one-pulse steps to be delivered to the heater(s) during each frame time. The terms, their logic equations, and the number of pulses per frame time contributed by each are as follows:

A. (Cone) Gate Terms

TERM	EXPRESSION	PULSES PER FRAME TIME
1A	$X0\ A9$	512
2A	$\overline{X0}\ X1\ A8$	256
3A	$\overline{X0}\ \overline{X1}\ X2\ A7$	128
4A	$\overline{X0}\ \overline{X1}\ \overline{X2}\ X3\ A6$	64
5A	$\overline{X0}\ \overline{X1}\ \overline{X2}\ \overline{X3}\ X4\ A5$	32
6A	$\overline{X0}\ \overline{X1}\ \overline{X2}\ \overline{X3}\ \overline{X4}\ X5\ A4$	16
7A	$\overline{X0}\ \overline{X1}\ \overline{X2}\ \overline{X3}\ \overline{X4}\ \overline{X5}\ X6\ A3$	8
8A	$\overline{X0}\ \overline{X1}\ \overline{X2}\ \overline{X3}\ \overline{X4}\ \overline{X5}\ \overline{X6}\ X7\ A2$	4
9A	$\overline{X0}\ \overline{X1}\ \overline{X2}\ \overline{X3}\ \overline{X4}\ \overline{X5}\ \overline{X6}\ \overline{X7}\ X8\ A1$	2
10A	$\overline{X0}\ \overline{X1}\ \overline{X2}\ \overline{X3}\ \overline{X4}\ \overline{X5}\ \overline{X6}\ \overline{X7}\ \overline{X8}\ \overline{X9}\ A0$	1

B. (Guard) Gate Terms

TERM	EXPRESSION	PULSES PER FRAME TIME
1B	$X0\ B9$	512
2B	$\overline{X0}\ X1\ B8$	256
3B	$\overline{X0}\ \overline{X1}\ X2\ B7$	128
4B	$\overline{X0}\ \overline{X1}\ \overline{X2}\ X3\ B6$	64
5B	$\overline{X0}\ \overline{X1}\ \overline{X2}\ \overline{X3}\ X4\ B5$	32
6B	$\overline{X0}\ \overline{X1}\ \overline{X2}\ \overline{X3}\ \overline{X4}\ X5\ B4$	16
7B	$\overline{X0}\ \overline{X1}\ \overline{X2}\ \overline{X3}\ \overline{X4}\ \overline{X5}\ X6\ B3$	8
8B	$\overline{X0}\ \overline{X1}\ \overline{X2}\ \overline{X3}\ \overline{X4}\ \overline{X5}\ \overline{X6}\ X7\ B2$	4
9B	$\overline{X0}\ \overline{X1}\ \overline{X2}\ \overline{X3}\ \overline{X4}\ \overline{X5}\ \overline{X6}\ \overline{X7}\ X8\ B1$	2
10B	$\overline{X0}\ \overline{X1}\ \overline{X2}\ \overline{X3}\ \overline{X4}\ \overline{X5}\ \overline{X6}\ \overline{X7}\ \overline{X8}\ X9\ B0$	1

It is seen that the differences between the corresponding A and B terms are the A and B qualifier and that the 10A term contains $\overline{X9}$ while the 10B term contains X9. Therefore, of the 1024 X0 plus $\overline{X0}$ pulses that occur during each pulse time, there will be one pulse missing from each of the heater waveforms when all terms are present. The missing pulse in the A (cone) waveform will be at a time when X0 through X8 are false and X9 is true. The missing pulse in the B (guard) waveform will be at a time when X0 through X9 are false. It is necessary that one pulse be missing from each waveform in order to establish the one-to-one correspondence between the data register counts and the number of pulses per frame time for each heater circuit.

The missing pulses for the two circuits occur one-half frame time apart. This amounts to a "dead time" in each of the channels and is a convenient time to update the corresponding data registers since the state of the data register can have no effect on the heater waveform during this time. The dead times are staggered for the two channels to allow alternate channel updating and the attendant time sharing of common elements.

An example will serve to demonstrate how the data register count and the number of pulses per frame correspond.

Assume that A0, A1 and A9 are true and all other flip-flops in the data register are false. The heater power waveform will consist of terms 1, 9 and 10, with all other terms absent. The number of pulses per frame time will be 512 + 2 + 1, or 515. If the data register is now increased by one count, A2 and A9 will be true and all other flip-flops will be false. The number of pulses per frame time will now be 512 + 4, or 516. It is seen that the number in the data register precisely controls and represents the number of pulses delivered to the heater during each frame time. If the resistance of the heater and the peak voltage of the heater waveform are both held constant, the number in the data register represents the power delivered to the heater.

Heater Power Gates

The function of the heater power gates is to convert the logic signals from the duty cycle gates to heater drive waveforms which

have a constant peak amplitude across the heater elements. Since there will be about 10 feet of wire between the power gates and the transducer heater elements, it becomes necessary to compensate for the power loss (voltage drop) in the lines. This is accomplished by sensing the peak voltage at the heaters and controlling the power gate supply voltages to provide heater voltage levels which are constant to within about $\pm 0.05\%$. It may be desirable to provide for a slight adjustment in this voltage to compensate for slight differences in heater resistance from unit to unit.

The heater power gates will be constructed of discrete components because integrated circuits are probably not available to perform this particular function.

Error Sense Bridges and Error Amplifiers

The error sense bridges will be constructed similar to those previously constructed at JPL. The temperature dependent arms will be constructed of platinum wire wound on the guard and cone and will each have a nominal cold (room temperature) resistance of 600 ohms. AC excitation will be used to eliminate the drift problems associated with DC error amplifiers. The bridges will be transformer coupled to integrated circuit AC error amplifiers to reduce the common mode signal. The AC excitation will be a 600 Hz square wave derived from the output of the second binary (X2) of the 9-stage divider chain. The AC voltage gain from the bridge(s) takeoff point to the output of the error amplifier(s) will be about 1000. (If reset were not provided, the gain would need to be between 25,000 and 100,000 to maintain the same measurement accuracy.) Feedback is provided around the error amplifiers to tailor their frequency response and to reduce the DC amplification to a low value. The outputs of the two errors are routed through a linear gate. This gate causes the cone amplifier output to be selected during $\overline{X9}$ time and the guard amplifier output to be selected during X9 time. The selected amplifier output is applied to the input of the error detection circuitry.

Thus, the error detection circuitry and associated logic elements are used for both control loops on a time shared basis. The linear gate is a relatively simple circuit and is constructed of discrete components (2 transistors and 8 resistors). The sense bridges, the error amplifiers,

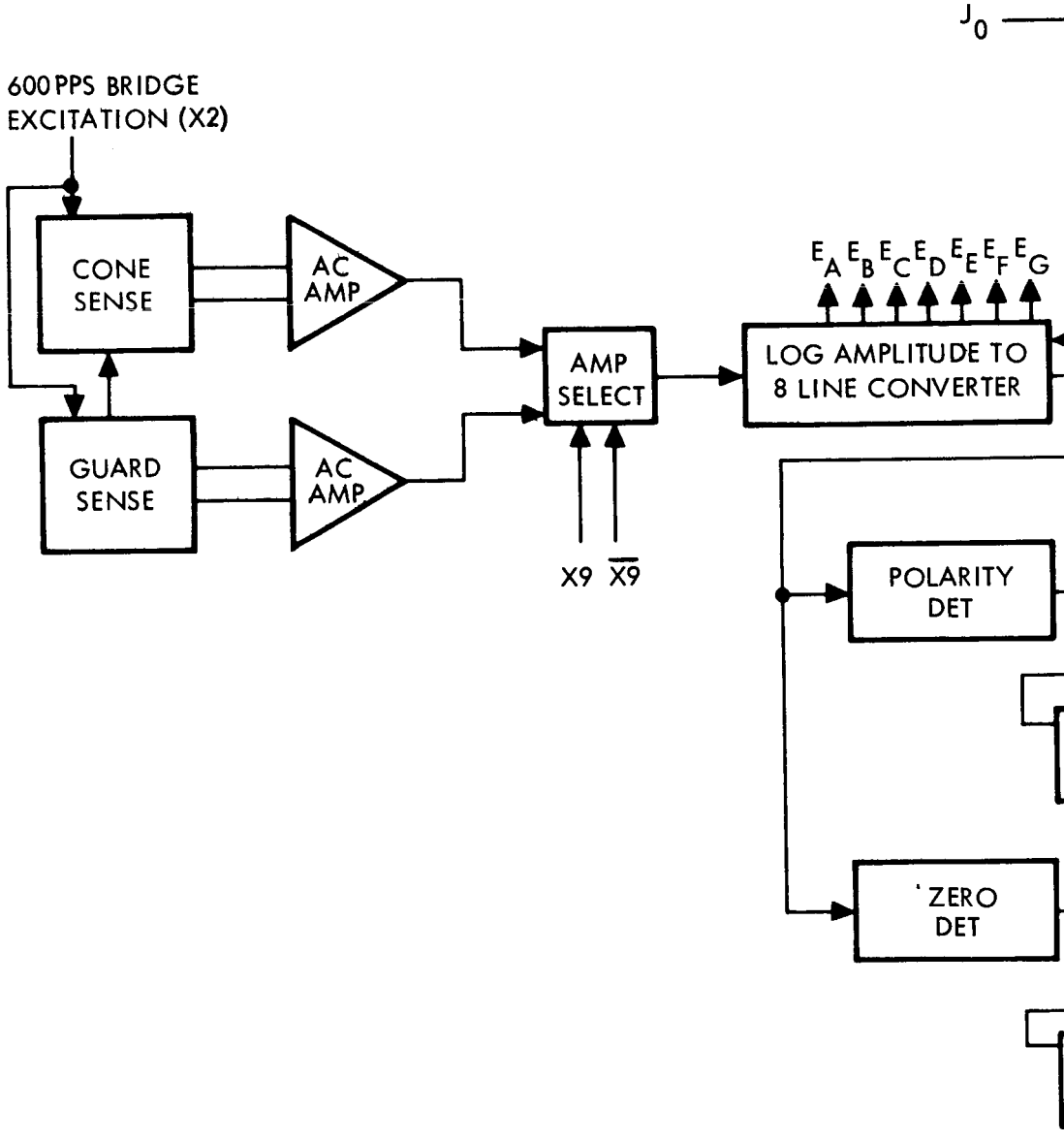
and the linear gate are shown in block diagram form in the overall block diagram of Figure 1.3-1.

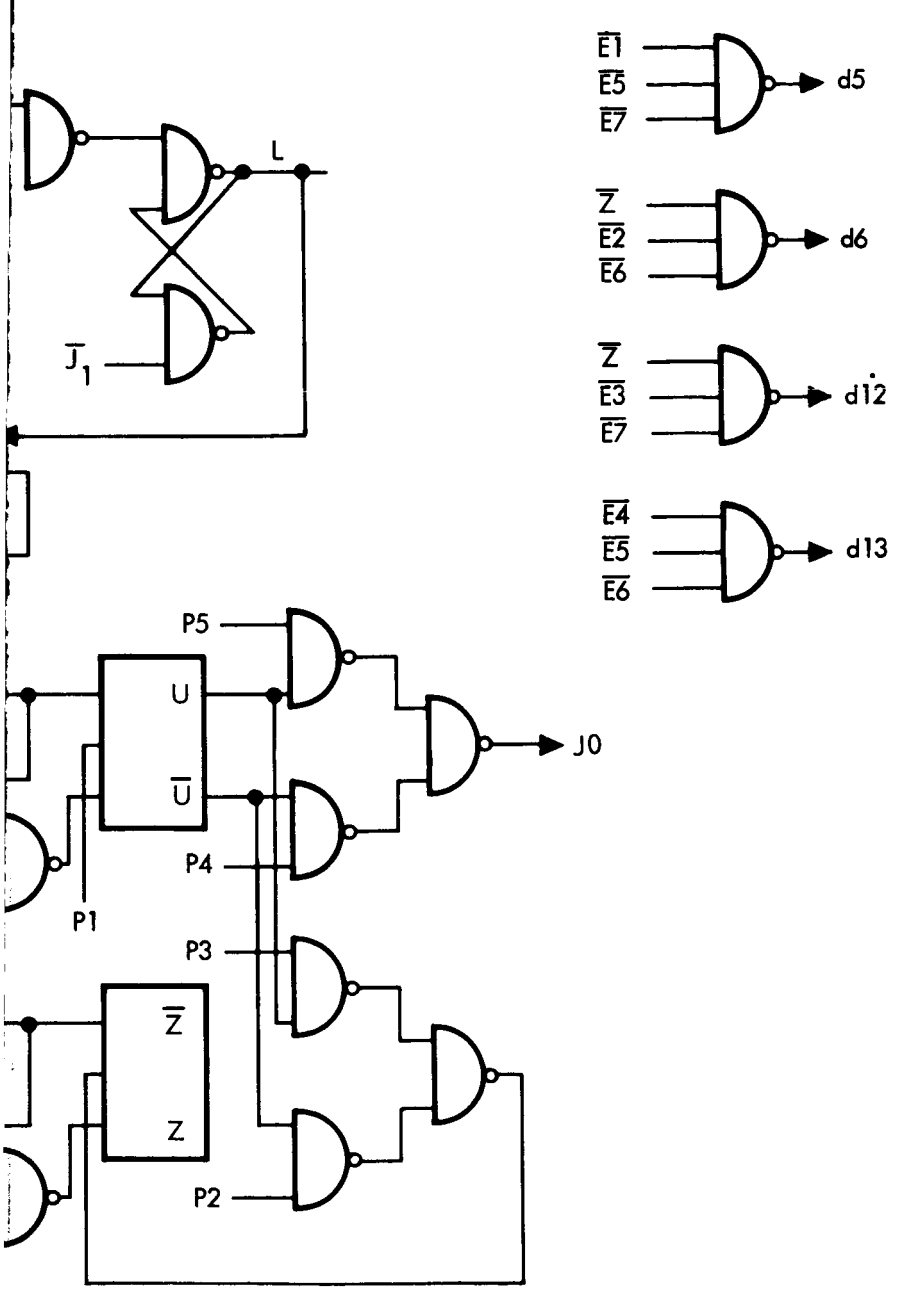
Error Detection Logic

A block diagram of the error detection logic is shown in Figure 1.3-5. The waveforms which control the operating sequence of the error detector are shown in the timing diagram of Figure 1.3-6. Referring to the timing diagram, XA is a clock at twice the rate of X0 (4800 pps), X1 through X5 are the outputs of the first five stages of the 9-stage (X) divider, X9 is the output of the last stage and P1 through P5 are error detection control signals. The times T0 and T1 are the start of the cone and guard heater power dead times, respectively. Each dead time lasts for one half period of the X0 clock, or about 210 microseconds. The term 10, or least significant heater power bit previously discussed, also occurs during the dead times. However, the cone heater term 10A occurs during the guard heater dead time and the guard heater term 10B occurs during the cone heater dead time. It is desirable to update each of the data registers during the dead time for that channel. This arrangement allows the registers to be updated on alternate half frames or 0.107 second apart.

It is seen that the logic levels P1 through P5 each occur twice during a frame time. The first pulse of each of these pulse pairs is used in the analysis of the cone bridge error and the second is used in the analysis of the guard bridge error. Each set of pulses occurs just prior to the dead time for the channel. These pulses set up conditions such that during the dead time the registers are directed to update in a prescribed manner dictated by the direction and magnitude of the error.

It is seen that the signal X9 is false during the first half of the group and true during the second half. The X9 signal causes selection of the proper error amplifier output from the amplifier select linear gate. The signal P1 is used to determine the phase of the error signal. It should be noted that the error signal at the output of the error amplifier will either be in phase or out of phase with X4, depending on the direction of the error. If the error signal is positive during P1 time, the U flip-flop is set true. If the error signal is negative, the U flip-flop


J0
600 PPS BRIDGE
EXCITATION (X2)
CONE
SENSE
GUARD
SENSE
AC
AMP
AC
AMP
AMP
SELECT
X9
X9
E A E B E C E D E E E F E G
LOG AMPLITUDE TO
8 LINE CONVERTER
POLARITY
DET
ZERO
DET



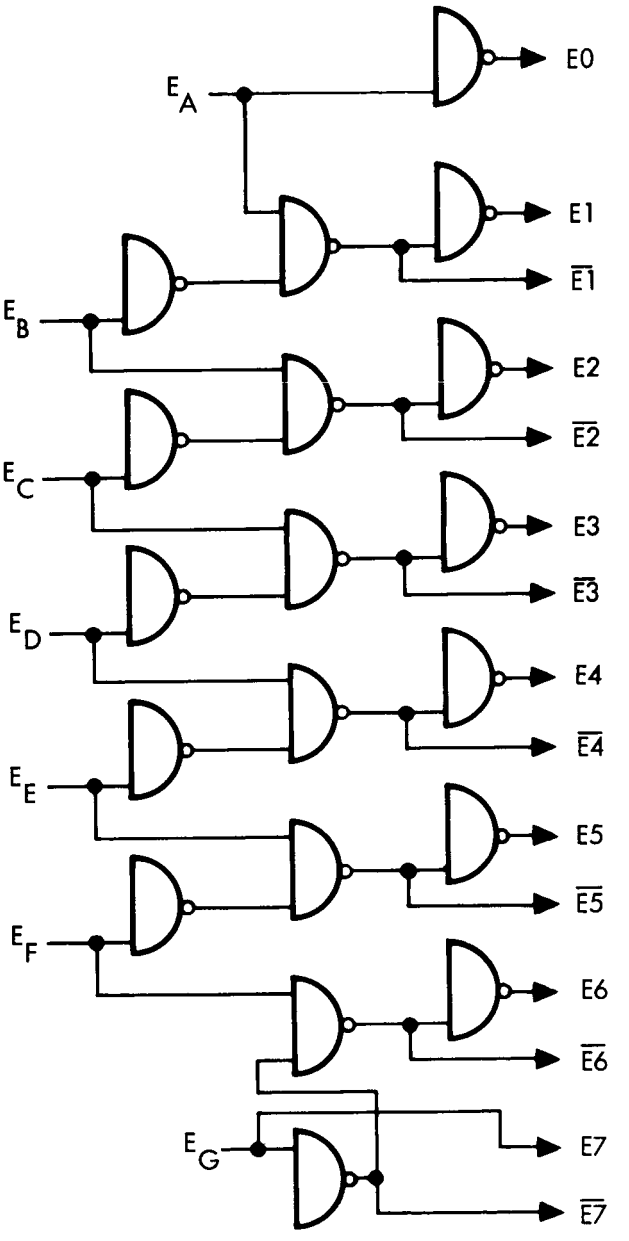
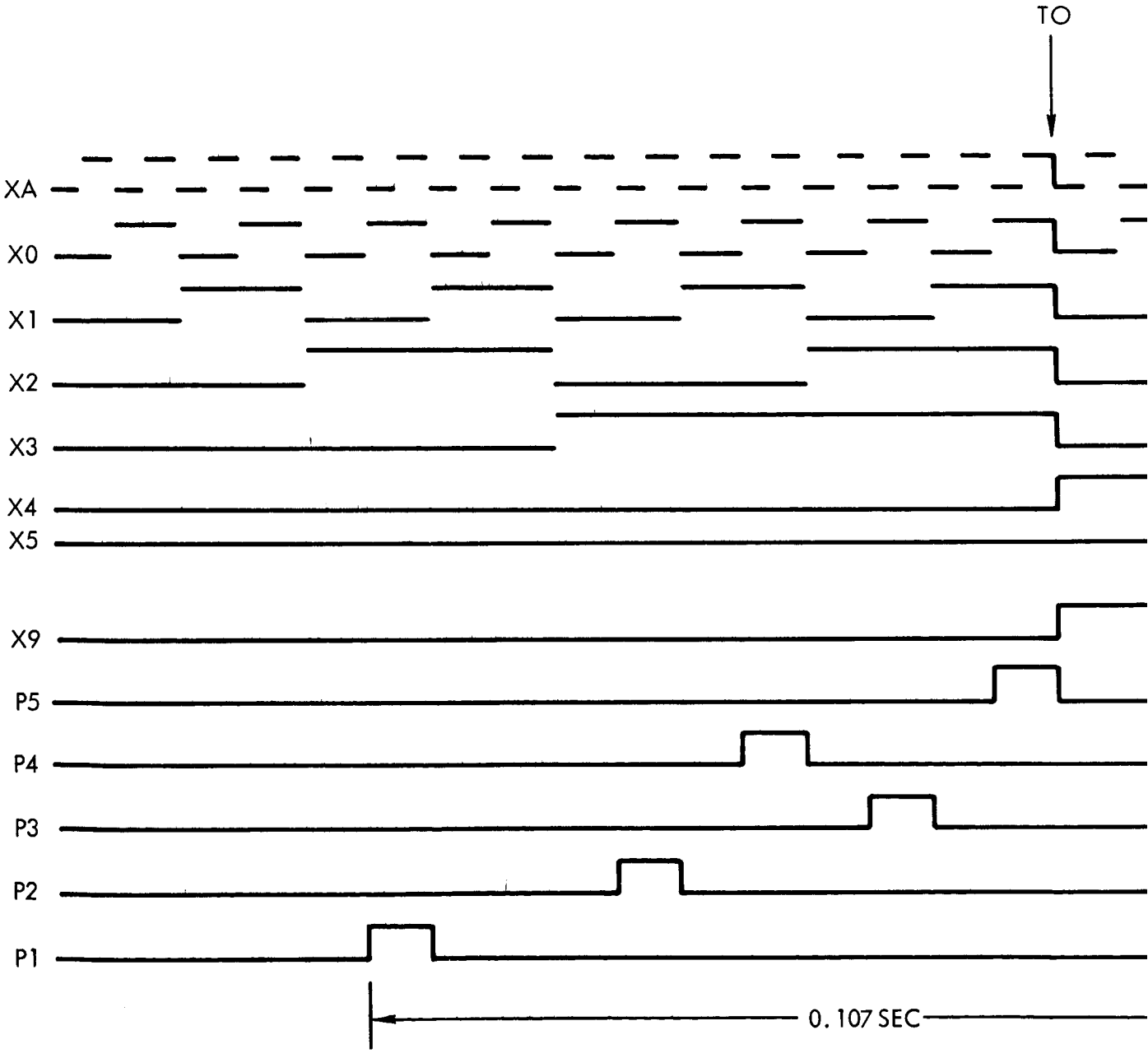


Figure 1.3-5 Error Detection Logic


TO
XA
X0
X1
X2
X3
X4
X5
X9
P5
P4
P3
P2
P1
0.107 SEC

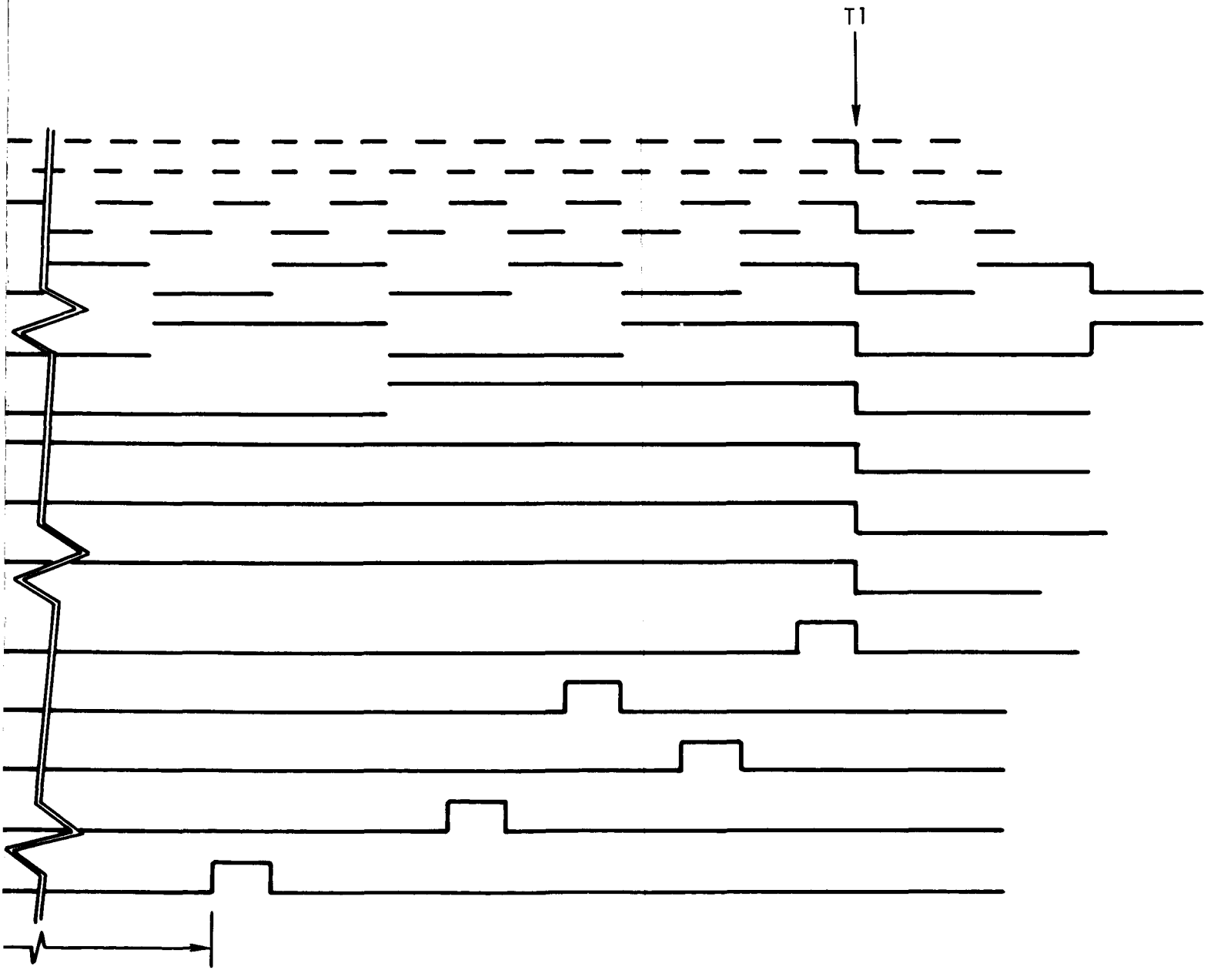


Figure 1.3-6 Timing Diagram Error Detection Control

is reset. If the error signal is below some preassigned amplitude, it is considered to be zero. This test is controlled by either P2 or P3, as determined by the state of the U flip-flop. If the U flip-flop is true P3 is selected, and if it is false P2 is selected. In this manner the measurement is always made on a positive polarity signal.

A zero detector output level above the minimum value will cause the Z flip-flop to assume the $\overline{Z}$ state indicating that the error signal is not zero. Either P4 or P5 is used to freeze the log amplitude-to-8 line converter, depending on the state of the U flip-flop.

The log amplitude-to-8 line converter has the characteristic that it generates logic levels E_a through E_g in various combinations, depending on the error signal amplitude. If E_a through E_g are false, the error is at or below a predesignated minimum value termed E_{min}. If the error is twice (2^1 times) E_{min}, E_a will be true and E_b will be false. If the error is four (2^2) times E_{min}, both E_a and E_b will be true and all other lines will be false. Each successive true line indicates a successive power of two error signal magnitude compared with an adjacent line of lesser significance. If all lines are true, the error signal is equal to or greater than 128 (2^7) times E_{min}.

E_a through E_g are decoded to produce the logic signals E_o through E_7 and their complements. Only one of these signals will be true at a time. The true bit indicates the logarithmic significance of the error signal magnitude as compared with E_{min}. Since only one clock pulse per data register is generated during each frame time, about 3-1/2 minutes would be required for a full scale heater power change if the data register count were only changed one count per frame.

The E_0 through E_7 signals establish the significance of the clock pulse that varies from 1 to 128 counts. This is done by controlling the point in the register where the clock pulse is inserted. In this manner it should be possible to accomplish a full scale change in about 3.2 seconds.

Data Storage Registers

The 10 bit data storage registers are used as the system integrating (reset) elements. They control the amount of power delivered to the heaters, and they contain numbers which accurately represent the power delivered to the heaters at a given time.

The data storage registers (termed A for the cone register and B for the guard register) must be capable of having their count increased or decreased as determined by the direction of the error; they must be capable of having their count increased or decreased each frame time by a number of counts as determined by the E logic levels. The presence of E0 shall cause a register to change by one count, E1 by two counts, E2 by four counts, etc., with E7 causing a 128 count change.

The counters must be inhibited from over-(or under) flowing since this condition would most certainly be detrimental to proper control loop operation. These registers could be configured as ripple counters with gating to provide the up-down bit weight assignment and over (under) flow prevention. However, 82 or 83 input gates would be required per stage and result in considerable register complexity.

The proposed method uses recirculating shift registers with a one bit adder/subtracter in the recirculation loop. Figure 1.3-7 shows the registers and part of the register control logic in block diagram form. The remainder of the register control logic is shown in Figure 1.3-8.

The manner in which the shift registers are employed is best explained by referring to the rules for the addition of 1 bit to, and the subtraction of 1 bit from a binary word.

The rule for the addition of one bit to a binary word is as follows: Starting with the least significant bit, complement all bits until the first 0 bit is reached; complement it and leave all remaining bits unchanged.

The rule for the subtraction of one bit from a binary word is as follows: Starting with the least significant bit, complement all bits until the first 1 bit is reached; complement it and leave all remaining bits unchanged.

These two rules are limited in that they restrict the addition or subtraction of the bit to the least significant position of the word.

The rules can be generalized to cover the addition or subtraction of a bit at any position in the word. The rule for addition of the bit now

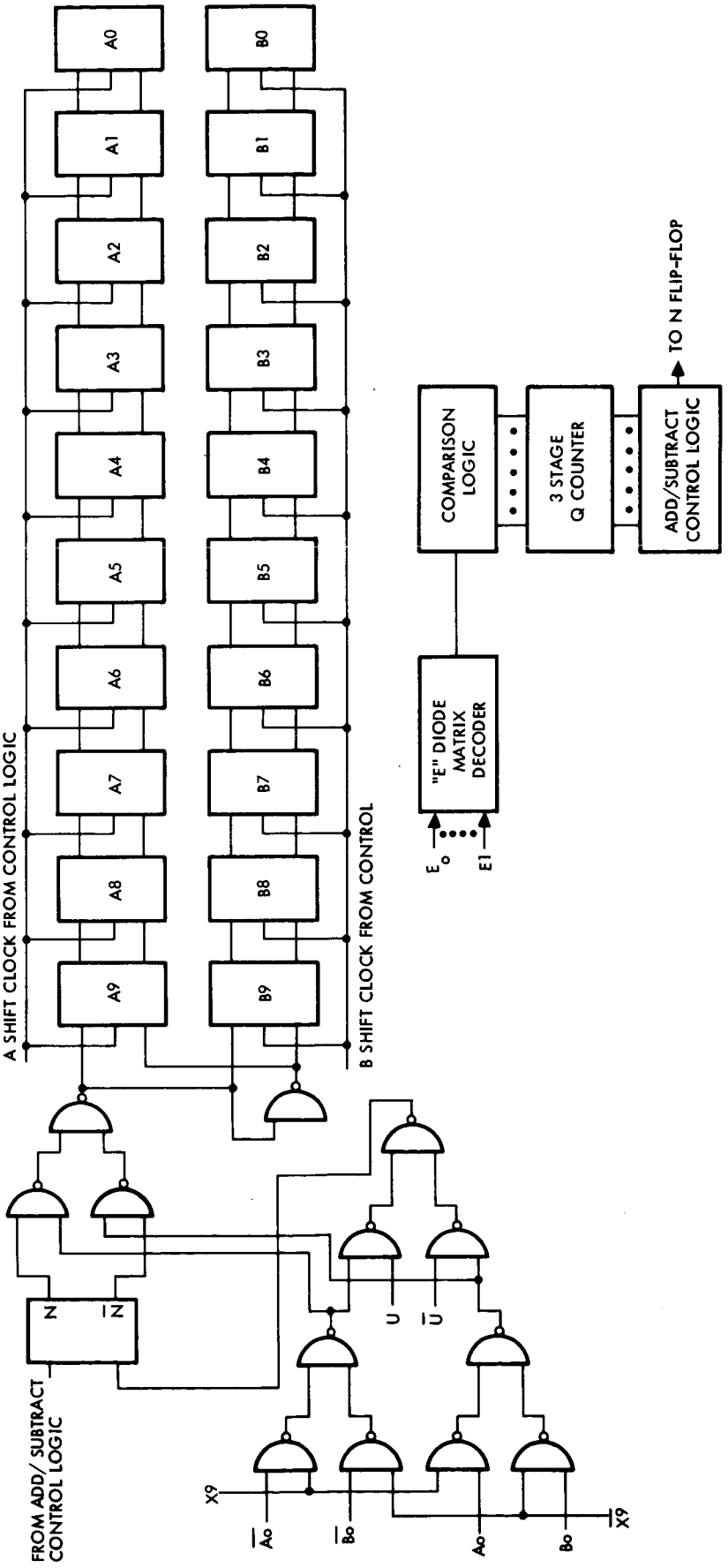


Figure 1.3-7 Data Registers and Control Logic

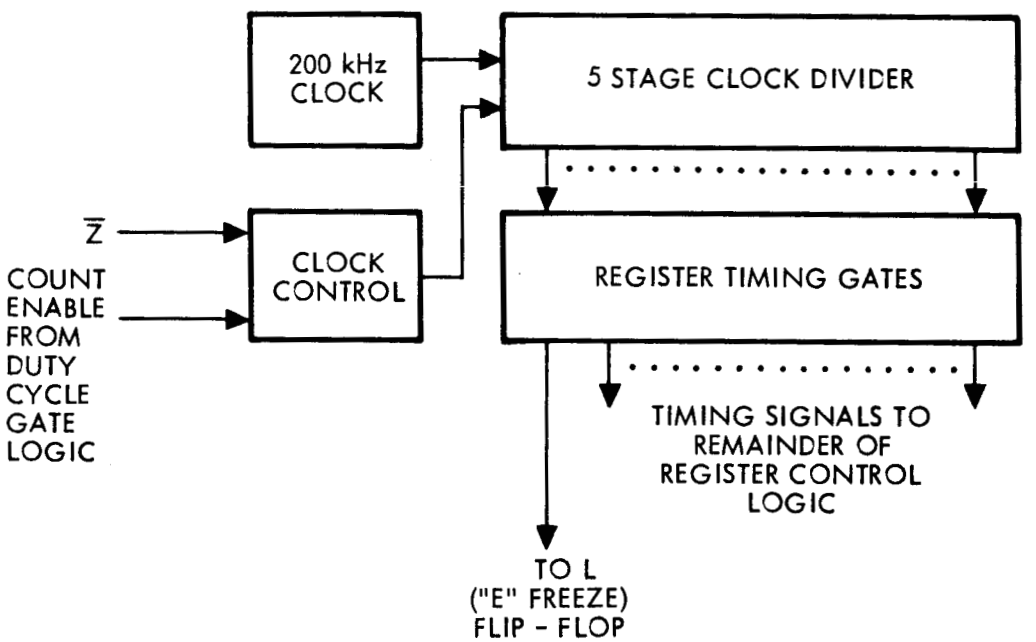


Figure 1.3-8 Data Register Timing Control Logic

becomes: Starting with the least significant bit, leave all bits unchanged until the bit position is reached where the bit is to be added, complement all successive bits until the first 0 bit is reached; complement it and leave all remaining bits unchanged.

With "1" substituted for "0," the generalized subtraction rule is obtained.

As shown in Figure 1.3-7, one adder/subtracter can be used for both data registers. The inputs to the two registers can be in parallel because the input has no effect on the register contents unless clock pulses are applied. The clock pulses are only applied to a register when it is desired to change the count in that register. The state of X9 determines which register output is routed through the adder/subtracter and which register receives clock pulses. The state of the U flip-flop determines whether a bit is to be added or subtracted. The state of the N flip-flop determines which bits are to be complemented. The control of this flip-flop will be explained in the succeeding paragraphs.

To provide the various clocking functions required, 32 clock pulses are generated during the 210μ sec dead time. This requires a minimum clock frequency of 156 kHz. To provide a safety margin, a nominal shift clock frequency of 200 kHz is selected. The clock oscillator will be a free running multivibrator probably constructed of integrated circuits. The frequency stability of this clock (CR) is unimportant.

There are four separate sets of actions that take place each time a register is updated. These actions and the number of clock pulses associated with each are as follows:

a) Recirculate the word in the selected data register once to determine the most significant position in which a bit can be added or subtracted without causing register overflow or underflow. This recirculation takes place during the first 10 CR clock pulses. At the 10th clock pulse the word has returned to its original position in the register, unchanged The Q 3-bit counter is used to determine the state of the register in the following manner:

Assume that the U flip-flop is true, indicating the data register count is to be increased. Starting with the register LSB, all one bits are totalized in the Q counter. Each time a zero bit is encountered, the Q counter is reset to the all zero state. One bits at the ninth and tenth clock times will not cause an increase in the count. However, zero bits at these times will cause the Q counter to be reset. At the end of the tenth clock pulse the state of the Q counter indicates the number of consecutive ones in the data register starting at the third most significant bit (A7 or B7) and counting toward the least significant bit. (Note that for the third most significant bit to be considered true, the two most significant bits must also be true.) Consider, for example, the case where A4 is false and all more significant bits are true. The Q counter would total 3 counts and indicate that a bit added in the A5 or higher order positions would cause register overflow. A count of 7 in the Q counter indicates that all register positions except the LSB are true. The register is considered to be full and no counts will be added to the register.

The maximum count that can ever be attained in the data registers is 1022. To allow 1023 counts would require an additional flip-flop in the Q register and additional gates to represent 8 consecutive one bits. The one bit additional register capacity does not warrant the additional circuits that would be required. When $\overline{U}$ is true, the number in the register is to be reduced. In this case, the number of consecutive zeros is counted. Otherwise, the Q counter operation is identical for up and down operation.

b) The second action that takes place is the comparison of a three bit binary number representing the true E value and the number represented in the Q register. The E values are decoded in a 12 diode decoder matrix to form the binary number. The E values and their corresponding 3 bit numbers are:

E_0	111
E_1	110
E_2	101
E_3	100
E_4	011
E_5	010
E_6	001
E_7	000

This comparison is completed in 3 clock times. If the number in the Q register is larger than the decoded E number, the position of the E ( ) indicates that the bit that should be added (subtracted) will cause overflow (underflow) of the data register. In this case, the Q register determines the position of the added bit. If the number in the Q register is smaller than the decoded E number, the next action will take place.

c) The third action takes place during the next seven clock times if the number in the Q register is smaller than the decoded E number. In this case, the Q counter is stepped until the the E and Q numbers agree. This will take a maximum of 7 clock pulses. The E number will now be contained in the Q register.

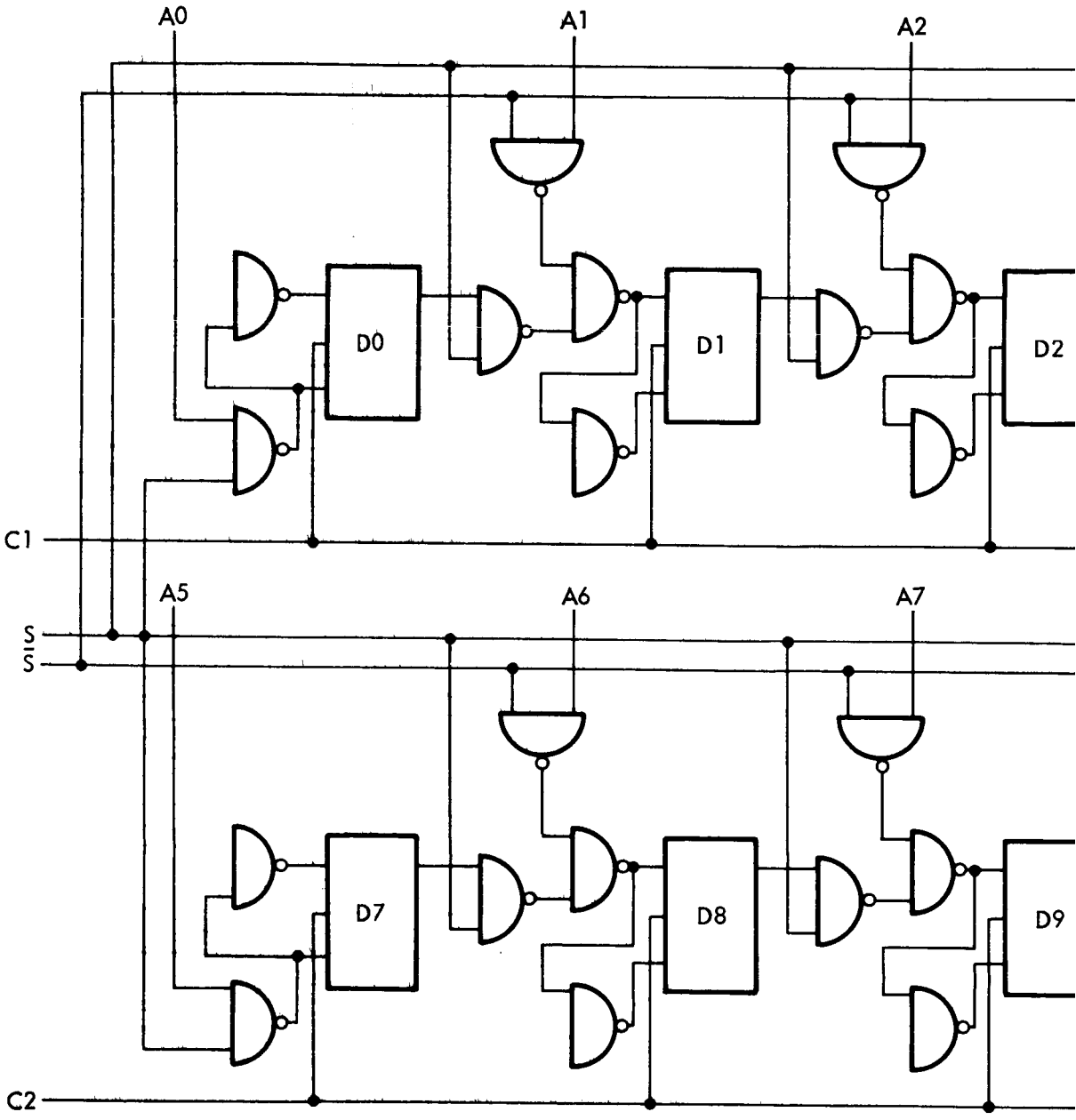
d) The final action is the altering of the data register count during the next ten clock pulses. The data word is shifted and clock pulses are simultaneously applied to the Q counter. The data are shifted, unaltered, until the Q counter reaches the all one state. At this time, the N flip-flop becomes true and subsequent data bits are complemented until the next 0 or 1 is encountered, depending on whether the bit is to be added or subtracted. This bit is complemented and all remaining bits are left unchanged. At the tenth clock pulse the new data word is in its proper position in the register and the updating process is complete. Figure 1.3-8 shows some of the control logic in block diagram form. Some of the blocks are not shown in detail because they are primarily repetitive pulse forming gates.

The counter control logic is not necessarily minimal as far as the number of logic elements is concerned. This is discussed in a later paragraph.

TM Interface Logic

The telemetry interface logic details are shown in block diagram form in Figures 1.3-9 and 1.3-10, and the pertinent timing waveforms are shown in Figure 1.3-11. Every J time that X9 is false, the contents of the A data register and a number representing the error magnitudes are transferred into the TM register unless the data are being shifted out to the TM system.

The TM register consists of two 7-bit registers. Data bits A_0 through A_4 are transferred into the 5 least significant positions of the D_0 through D_6 register, and data bits A5 and A9 are transferred into the 5 least significant positions of the D7 through D13 register. The D5, D6, D12 and D13 register positions are used to hold a 4 bit binary number which represents the last measured state of E0 through E7 and


A0
A1
A2
D0
D1
D2
C1
A5
A6
A7
S
S̄
D7
D8
D9
C2

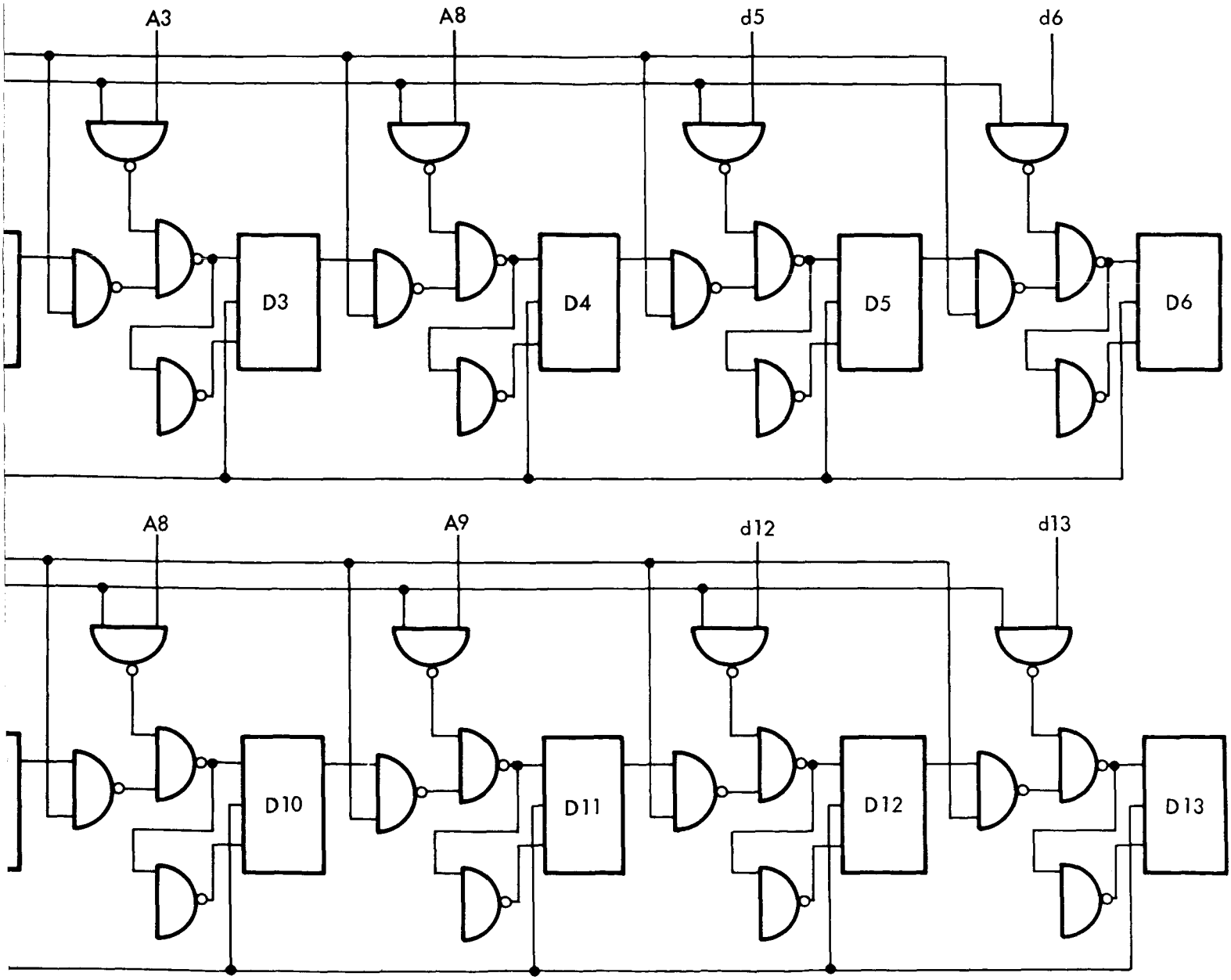


Figure 1.3-9 TM Register Logic Diagram

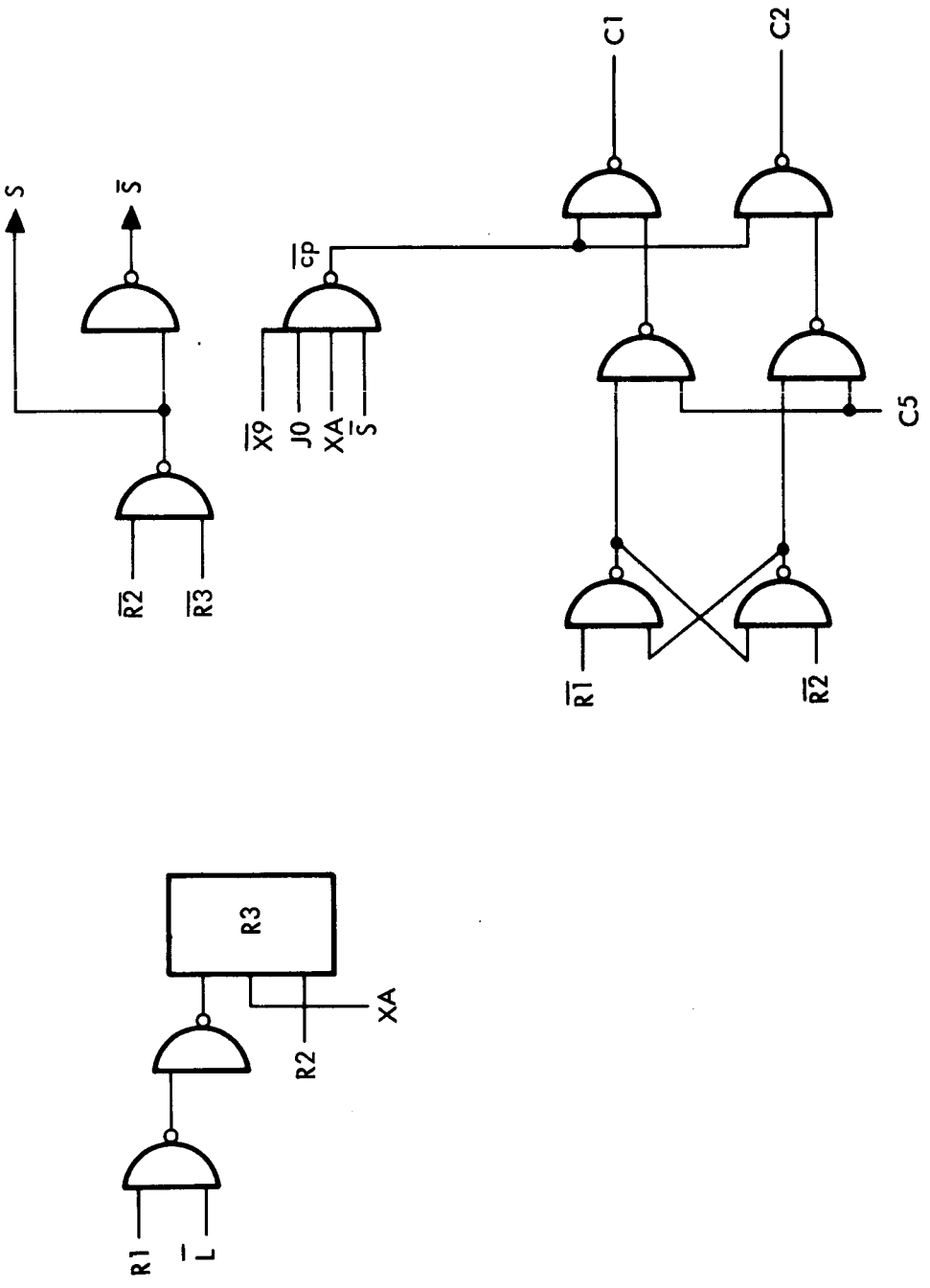


Figure 1.3-10 TM Register Control Logic

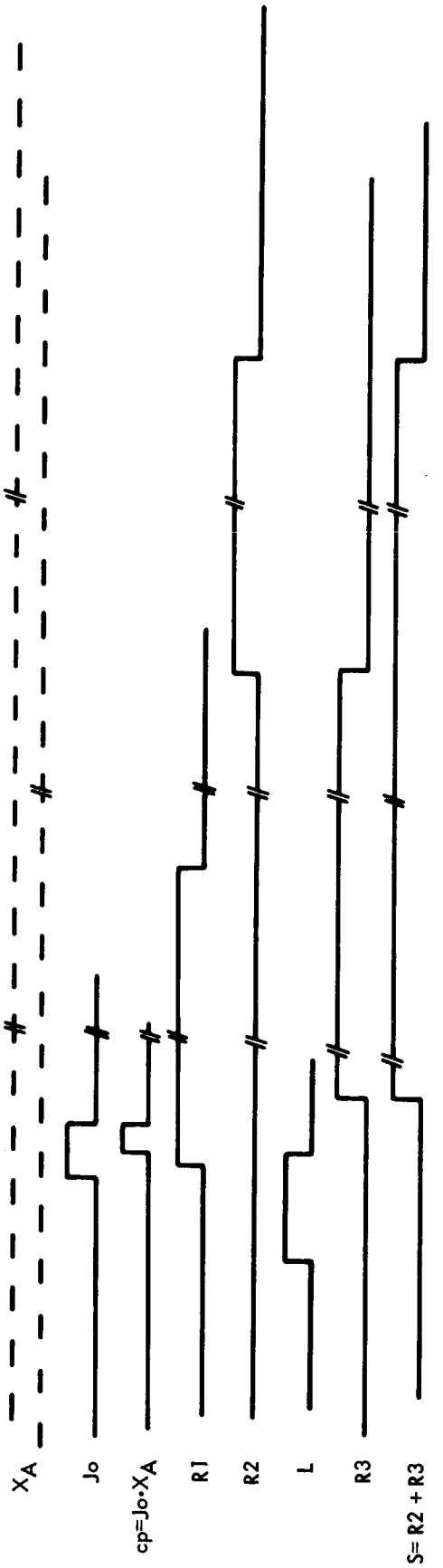


Figure 1.3-11 Timing Diagram TM Register Control

the Z flip-flop. The combinations of these signals are decoded into a 4 bit binary word by gates shown in Figure 1.3-6. The 4 bits are identified as d_5, d_6, d_{12}, and d_{13}. Of the 16 possible combinations, of these 4 bits only 9 are required. In the 9 used combinations, d_5 or d_6 is always zero and d_{12} or d_{13} is always zero. This is consistent with the requirement that each of the 7 bit telemetry words must always contain at least one zero bit.

The following assumptions are made concerning the TM alert and shift commands:

- The alert commands occur at least 0.83 millisecond prior to the first shift pulse.
- Seven shift pulses are supplied following the start of each alert command.
- The 7 shift pulses are bracketed by their respective shift commands.

The TM register control logic is shown in Figure 1.3-10. The two TM alert commands are designated as R1 and R2 and the TM shift pulses are designated as CS.

The TM registers are controlled to accept parallel transfer of data until an R1 alert command is presented by the TM system. If the L logic level is false at this time, the next XA clock pulse (XA is a clock with a 4800 pps rate) will cause the R3 flip-flop to become true, which will cause the serial shift command S to be true. S will remain true until the channel 2 alert command R2 has become true and again become false regardless of the amount of time between the R1 and R2 alert commands.

If L is true when the alert command R1 is received, the generation of the S signal will be delayed until the first XA clock pulse after J becomes false or a maximum delay time of 0.83 millisecond. This precaution is necessary to prevent the serial shift command from occurring while data is being parallel transferred into the TM data registers. S also inhibits the parallel transfer clock CP. The serial shift pulses are gated to either the D0 - D6 register or the D7 - D13 register, depending on which one of the two alert commands is present. If the R2 does not bracket its associated 7 shift pulses, it will be necessary to count the pulses to prevent the shift command S from becoming false until after the last shift pulse.

Auxiliary Circuits and Functions

A power supply of the transformer-rectifier DC regulator type is incorporated to provide the +12, -12, +5 and -5 volt DC power to operate the electronic circuitry and heaters. The 5 watt maximum input power requirement is considered to be realistic and should be attainable.

Provision is made to allow OSE monitoring of the cone heater power and error digital measurements and monitoring of the guard temperature. The guard temperature is monitored by means of a temperature dependent resistance winding (platinum wire) on the guard. A number of other functions can be made available through the direct access connectors. The number and type of such functions will be decided on the basis of the number of available connector pins. Because of the digital nature of the equipment it is anticipated that the number of desired accessible functions will outnumber the available connector pins.

1.3.3 Possible Simplifications of the System

Certain simplifications in the system can probably be made depending on the results of the final dynamic analysis. These simplifications would result in some reduction in the total number of components required. As an example, the analysis may show that the number of "E" levels can be reduced from the presently planned 8 to 4. This would simplify the log amplitude-to-logic converter and would allow some reduction in the number of logic elements elsewhere in the system.

A final review of the system logic design will undoubtedly disclose some redundant elements that can be eliminated.

1.3.4 Preliminary Dynamic Analysis of Proposed System

A brief dynamic analysis was performed on a simplified linear model of the studied system. The objective was to determine dynamic stability and to uncover any basic conceptual problems leading to steady-state measurement errors. The details of this analysis are presented in Appendix A.

The analysis was performed by making two major simplifying assumptions:

a) Instead of digital integration with a 0.213 second sample period, continuous integration was assumed.

b) The system equations were linearized such that only the performance in the vicinity of the quiescent temperature level was described.

The results of the analysis, based on the foregoing assumptions, lead to the conclusions that:

- The studied system is conceptually sound.
- The cone temperature control loop will be stable.
- The guard temperature control loop is underdamped and will be marginally stable.

The damping of the guard control loop must be increased to provide unconditionally stable operation. One straightforward way of increasing the damping would be to increase the guard energy loss by radiation and reduce the thermal mass of the guard.

Fortunately, both of these modifications are already being contemplated for other reasons. (It is presently planned to change the guard material from copper to aluminum or magnesium to reduce the weight.)

Other methods of increasing the guard control loop damping are presently being considered.

Also it is presently planned to construct a more complete sampled data mathematical model and analyze the system in terms of the total non-linear equations.

1.4 OPERATIONAL SUPPORT EQUIPMENT

1.4.1 General

The Operational Support Equipment (OSE) is designed to provide for an easy determination of the TCFM operational status. The OSE will allow any degree of performance verification from overall system operation down to the sub-function and component levels.

The equipment provides all the necessary functions to prepare the TCFM for flight at both the System Test Complex (STC) and at the Launch Complex (LC). The following functions are required at both complexes:

At the System Test Complex (STC)

- o Verification of the TCFM Design
- o Calibration
- o Provision for TCFM Operating Power
- o Trouble Shooting
- o Direct Access Monitoring of System Functions

At the Launch Complex (LC)

- o Monitoring of TCFM Telemetry Data
- o Data Display
- o Go/No-Go Indications for Operational Status
- o Data Recording
- o Data Processing

The following are required and proposed functions:

- o Readout, display and recording of cone heater power and cone error digital registers
- o Method for monitoring guard temperature
- o Provision for flux input stimulus to transducer
- o Go/No-Go indications for proper TCFM operation
- o Monitoring, through the direct access connections, of the guard heater power register and other functions necessary to determine proper operation of the equipment at the sub-system level

- o Provision for the necessary test equipment, as a part of the OSE, to accurately measure the monitored functions
- o Provision of the operating power for the TCFM
- o Conversion of the cone heater power reading to read directly in incident thermal flux units and display in decimal form
- o Display of the guard heater power in decimal form

1.4.2 Operational Ground Support Equipment Details

The OSE will be of rack mount construction. The construction details, shown in block diagram form in Figure 1.4-1, are discussed in the packaging section of this study.

The OSE consists of two sections, one containing the necessary circuitry and displays required to acquire, convert and display the digital and analog signals from the TCFM; and the other consisting of a paper strip recorder and commercial test equipment, which is to be used for detailed inspection and test of the various TCFM subsystem functions and components. The test equipment will include a digital voltmeter, an oscilloscope, a resistance bridge and power supplies.

Direct access lines from the TCFM will monitor the guard power register by reading out the number in parallel to a register in the OSE. This information will be shifted out serially to a multichannel paper strip recorder. The number will also be displayed on a lamp array. In addition, the strip recorder will also record the cone power which can be monitored from the telemetry registers or the registers from the direct access lines. The guard heater has an auxiliary platinum resistance winding provided as a temperature sensor to allow measurement of the guard temperature. The guard resistor will be measured directly, using three lines, to determine the guard temperature set point.

During checkout, a telemetry exerciser consisting of a clock oscillator counter and associated logic, will develop cone TM data register shift pulses and the cone alert pulse. A converter will supply the 50 v RMS 2400 Hz square wave to the TCFM during the checkout. A separate voltage is required for the lamp used to stimulate the sensor.

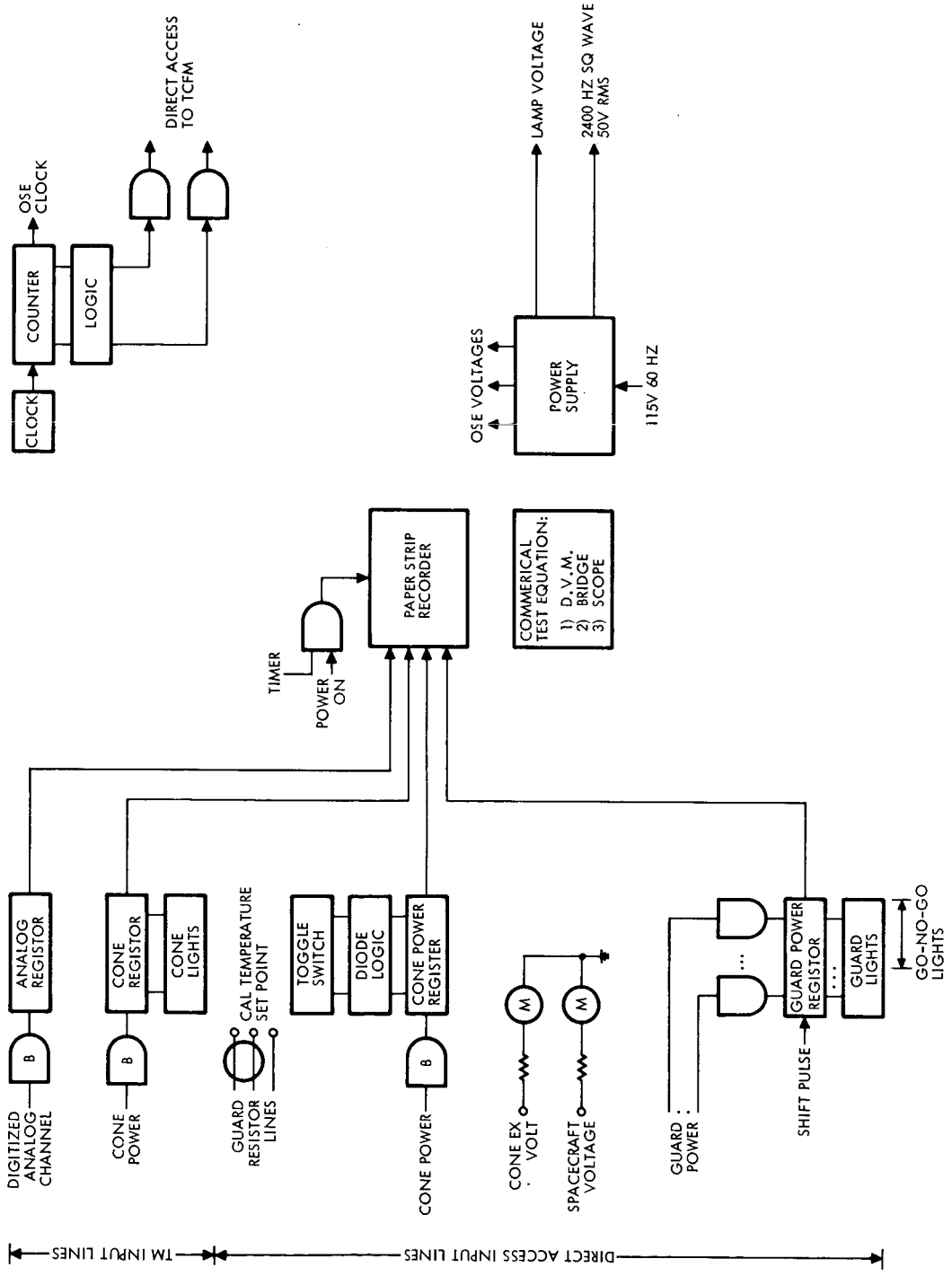


Figure 1.4-1. OSE Block Diagram

1.5 MECHANICAL DESIGN

1.5.1 Circuit Grouping and Arrangement

The arrangement of the circuits is organized to minimize the number of interconnections from one to the other of the two standard chassis subassemblies. The control monitor circuits are organized to minimize noise susceptibility of the sensitive balanced bridges. The two subassemblies are arranged such that all the analog circuits associated with the guard and cone heaters are on one chassis and the power supply, and all the digital logic circuits are on another chassis.

1.5.1.1 Circuit Types and Description of Interconnections

The analog input/output circuits associated with the cone and guard bridge balancing and power output gates are composed of a combination of close tolerance discrete parts and integrated power control logic gates and output transistors. These components are mounted and interconnected by means of etched wiring boards which are in turn bonded to the center wall of the standard 1-3/16-inch thick subchassis. Figure 1.5-1 identifies this assembly as the "A1" circuit board arrangement comprised of one A1-TB1 and one A1-TB2 circuit. The A1-TB1 circuit contains the analog bridge circuit channels for the cone and guard heaters. Included in it are the cone and guard error amplifier, error detector, channel selector and ground support buffer circuits. The A1-TB2 circuit contains the analog cone and guard power controls, power gates and power regulator circuits for the output of the heater power for each channel.

The second subassembly identified as the "A2" circuit board, Figure 1.5-1, is arranged on a modified H frame chassis having the center web off-set. This off-set allows maximum depth on one side for the higher component association with the power supply while at the same time minimizes the otherwise wasted volume over the flat pack logic circuit array which is mounted to the opposite side of the A2 circuit board. The A2 circuit board consists of one A2-TB3 containing the power supply and the clock pulse generator circuits and one A2-TB4 containing the entire logic circuitry such as shift registers, data register and counter logic circuits.

1.5.1.2 Shielding Considerations

A sheet metal cover will be used to provide protection from the

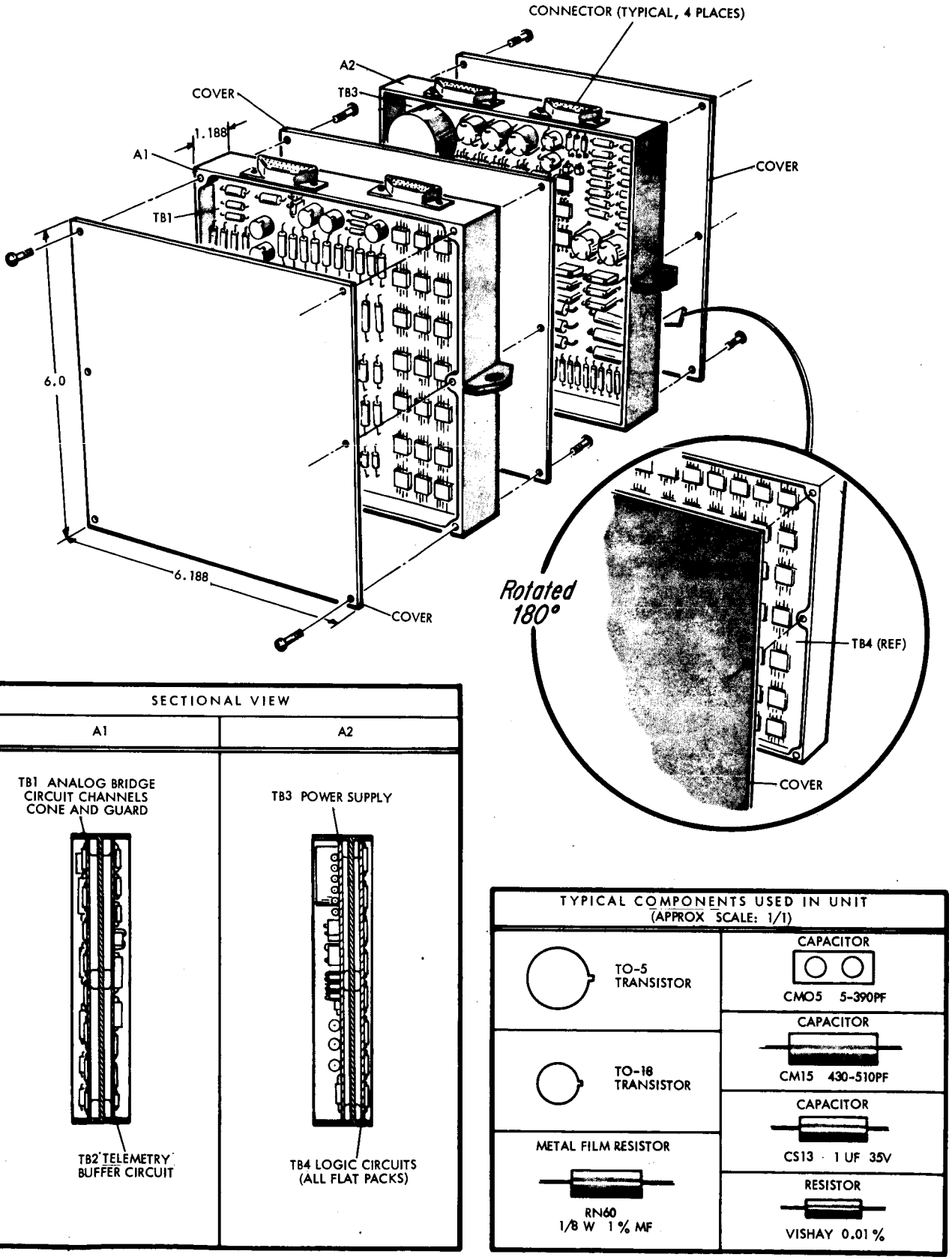


Figure 1.5-1 TCFM Mechanical Configuration

radio frequency interference on the sensitive balanced bridge circuit inputs. As shown in Figure 1.5-1, both sides of the analog subassembly A1 will be enclosed by sheet metal covers, and only one cover is expected over the logic circuits of the A2 subassembly. The power supply facing the A1 chassis being insensitive to radio frequency noise will remain uncovered. The noise generated by the power supply is expected to be at a low level and of low frequency.

1.5.1.3 Interconnection Technique

The two subassemblies of the TCFM electronics will use fired wiring, etched circuit boards as the primary means of interconnection of the circuit components. A combination of both the 2 layer and the multiple layer circuit boards is required to implement the wiring of discrete parts and approximately 120 integrated flat pack circuits. The means of lead attachment to the circuit boards will be by soldering the leads to terminals and to pads. Point-to-point wiring will be used to pick up the terminals which wire into the chassis mounted connectors. Interconnection between the two subassemblies will be made through the external connectors.

APPENDIX

DYNAMIC ANALYSIS OF LINEAR MODEL OF PROPOSED CONTROL SYSTEM

1. SIMPLIFIED LINEAR DYNAMIC ANALYSIS

In order to obtain an indication of the stability and dynamic performance of the complete radiometer system a highly simplified mathematical model was developed and studied. Since this is a first look at the system dynamics, continuous performance was assumed rather than the discontinuous action dictated by the digital electronics. First, a brief summary will be given of the basic system operation. Next, the continuous nonlinear equations will be presented. In the following section, the linearized equations will be derived in conjunction with the corresponding block diagram. In the last section, the results are shown in for form of root locus diagrams and recommendations for improving the response are made.

2. SYSTEM DESCRIPTION

Figure A-1 is a simplified presentation of the assumed radiometer geometry. The basic element of the device is the radiometer cone (hereafter simply called cone) which absorbs the unknown energy flow $\dot{Q}_i$. Energy radiated out from the cone is labled $\dot{Q}_o$. In order to assure that radiant energy is only exchanged through the cone aperture, the cone is surrounded by the thermal guard (hereafter simply called guard) which is nominally kept at the same temperature as the cone. The heat loss (undesired) of the guard due to radiation is labeled $\dot{Q}_{20}$. The rate of heat flow from the guard to the cone (undesirable) is represented by $\dot{q}_{21}$. This energy transfer is zero when the temperature of the cone and guard are identical. Both the cone and guard are provided with electrical heater elements which have resistance value R_{1H} and R_{2H} respectively. Two temperature sensitive resistance elements R_{1T} and R_{2T} are used to determine the temperatures of the cone and the guard.

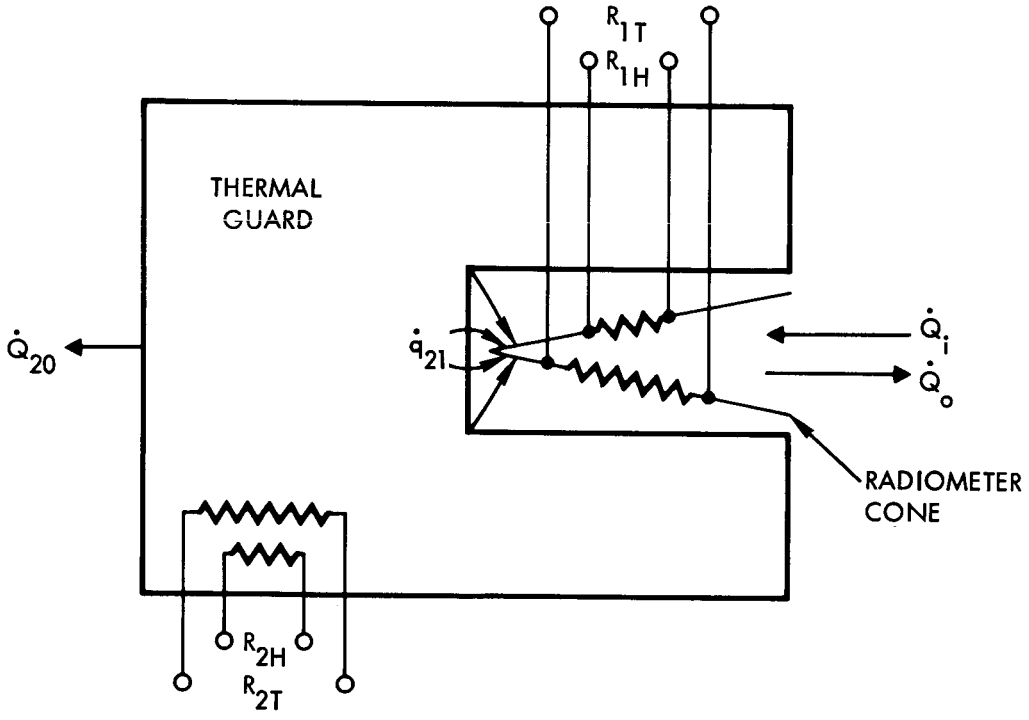


Figure A-1 Radiometer Geometry

Figure A-2 is a functional diagram of the complete radiometer system. The system consists of a guard temperature control loop and a cone temperature control loop. The two loops are only thermally coupled. The guard bridge generates an error voltage E_G which is proportional to the difference between the actual guard temperature T_G and the nominal operating temperature T_o. An error signal exists whenever the guard temperature sensing resistance R_{2T} is not equal to the reference resistance R_{2R}. The digital electronics effectively integrates the error signal E_G and activates the guard heater with a duty cycle that is proportional to the output signal E_2. Finally, the guard heater temperature T_G adjusts itself according to the energy balance equations applicable to the guard and thereby readjust the resistance R_{2T}.

The cone temperature control loop operates in a similar manner. The cone bridge has a reference resistance, R_{2T} which is a function of the guard temperature. Whenever the cone temperature T_c is not equal to the guard temperature the resistance $R_{1T} \neq R_{2T}$ and an error voltage E_c is generated. Thus the cone temperature is slaved to the guard temperature. Two separate but identical temperature sensitive resistances R_{2T} are used in the guard and cone bridge, respectively, to avoid electrical coupling. The digital electronics and heater of the cone circuit function the same as those of the guard circuit. Finally, the cone temperature T_c is adjusted according to the energy balance equations of the cone and the control loop is then closed through the temperature sensitive resistance R_{1T}.

3. CONTINUOUS SYSTEM EQUATIONS

The equations for both the guard bridge and the cone bridge errors are derived by making the following assumptions.

- The supply voltage V_2 and V_1 are constant.
- The current through the bridge does not cause resistance changes.
- The bridge output is independent of the load.

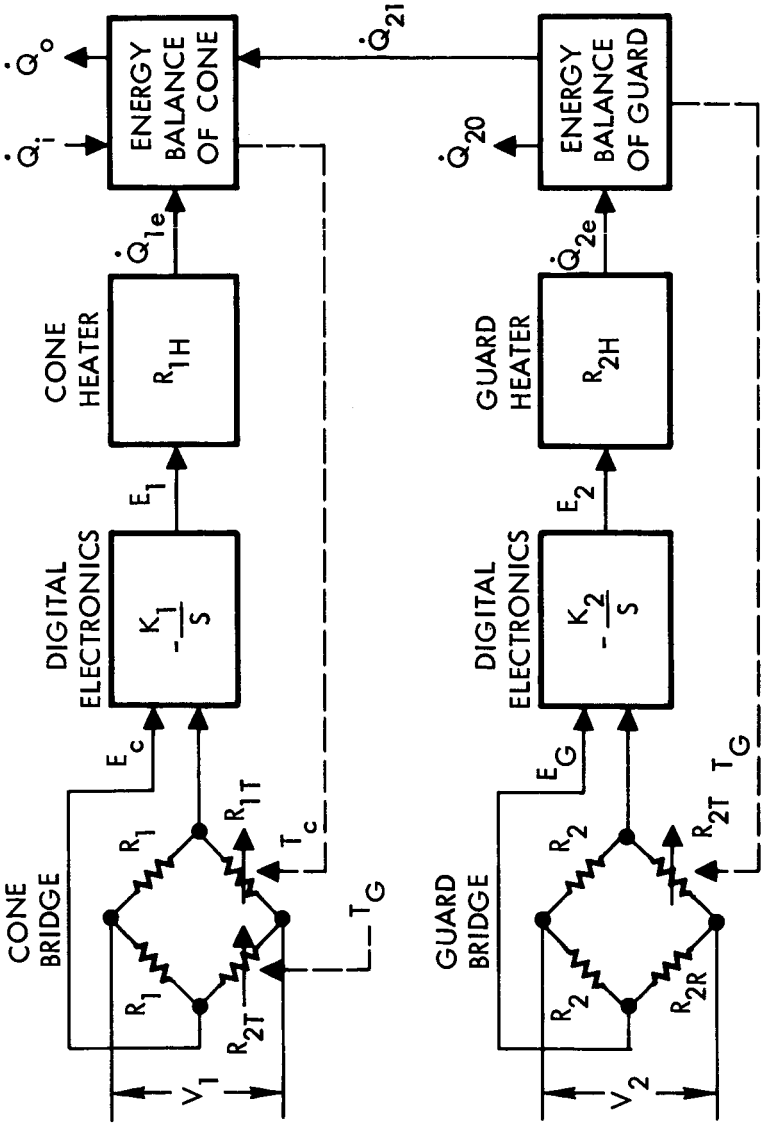


Figure A-2 Radiometer System Functional Diagram

Referring to Figure A-3 we obtain:

$$i_1 = \frac{V_2}{R_2 + R_{2R}}$$

$$i_2 = \frac{V_2}{R_2 + R_{2T}}$$

$$E_G = R_2 V_2 \left(\frac{1}{R_2 + R_{2R}} - \frac{1}{R_2 + R_{2T}}\right) \quad (1)$$

The guard temperature sensing resistance R_{2T} is given by:

$$R_{2T} = R_{20} + k_t t_G \quad (2)$$

where:

R_{20} = the resistance value of R_{2T} at the nominal guard temperature T_o

k_t = thermal coefficient of the resistance, R_{2T}

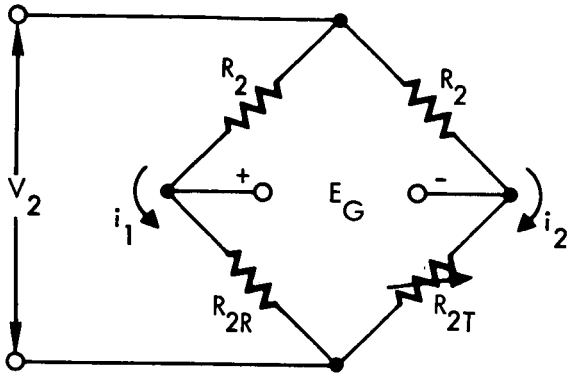
t_G = guard temperature deviation from nominal

The cone bridge error equation is obtained in a similar manner with reference to Figure A-4.

$$i_1 = \frac{V_1}{R_1 + R_{2T}}$$

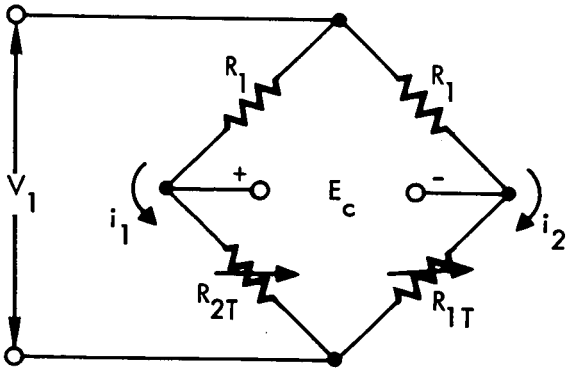
$$i_2 = \frac{V_2}{R_1 + R_{1T}}$$

$$E_c = R_1 V_1 \left(\frac{1}{R_1 + R_{2T}} - \frac{1}{R_1 + R_{1T}}\right) \quad (3)$$



GUARD BRIDGE

Figure A-3 Guard Bridge



CONE BRIDGE

Figure A-4 Cone Bridge

The resistance R_{2T} is defined in Equation (2). The cone temperature sensing resistance R_{1T} is given by

$$R_{1T} = R_{10} + k_t t_c \tag{4}$$

where:

R_{10} = the resistance value of R_{1T} at the nominal cone temperature T_o

t_c = cone temperature deviation from nominal

The digital electronics in both the guard loop and the cone loop generate fixed pulses at a rate that is proportional to the integral of the input. The sampling period of this integration is 0.213 sec. For the purpose of the present linear analysis, the following assumptions are made:

- The diginal electronics integrate continuously.
- The output signal E_1 and E_2 are continuous rather than pulse frequency modulated.

With these assumptions we obtain

$$E_2 = - K_2 \int E_G \, dt \tag{5}$$

$$E_1 = - K_1 \int E_c \, dt \tag{6}$$

where:

K_1, K_2 = the equivalent integration gain of the cone and guard electronics respectively

The negative sign is used to assure negative feedback.

If it is assumed that both the cone heater and the guard heater are energized by a constant supply voltage V_{1H} and V_{2H} and that the duty cycle is proportional to E_1 and E_2, respectively, then the rate of energy supplied by the guard heater

$$\dot{Q}_{2e} = \left[\frac{V_{2H}^{\,2} k_e}{R_{2H}} \right] E_2 \tag{7}$$

and for the cone heater

$$\dot{Q}_{1e} = \left[\frac{V_{1H}^{2} k_e}{R_{1H}}\right] \tag{8}$$

where:

k_c = proportionality constant

The rate at which heat energy is stored in a given material is proportional to the rate of change of the applied temperature. We obtain, therefore, for the guard

$$\dot{Q}_G = m_2 C_2 \, d T_G/d\tau \tag{9}$$

and for the cone

$$\dot{Q}_c = m_1 C_1 \, d T_c/d\tau \tag{10}$$

where:

$\dot{Q}_G$, $\dot{Q}_c$ = the rate of heat storage in the guard and cone

m_2, m_1 = the guard and cone mass

C_2, C_1 = the specific heat capacity of the guard and cone

τ = time

Next, the equations expressing energy loss due to radiation will be presented. The flow of radiant energy between two bodies is proportional to the fourth power of their absolute temperatures. The rate of radiant energy flow from the guard to the cone is, therefore, given by

$$\dot{Q}_{21} = A_1 e_1 \sigma (T_G^{4} - T_c^{4}) \tag{11}$$

where

A_1 = the surface area of the cone

e_1 = emisivity of the outside cone surface

σ = a physical constant $\left(0.174 \times 10^{-8} \frac{\text{Btu}}{\text{hr-ft}^2 - {}^{o}\text{R}^4}\right)$

T_G = absolute guard temperature

T_c = absolute cone temperature

The loss of heat from the guard due to radiation into space is very small since the guard surface is highly reflective. This energy loss is given by

$$\dot{Q}_{20} = K_L T_G^4 \tag{12}$$

where K_L is a small proportional constant which must be obtained experimentally.

Assuming that the cone aperture has the characteristics of a black body, the rate of energy radiated through the cone aperture into space is

$$\dot{Q}_o = A \sigma T_c^4 \tag{13}$$

where

A = the cone aperture cross sectional area

All equations are now available to write the energy balance equations for the guard and the cone respectively. The energy balance for the guard is

$$\dot{Q}_{2e} = \dot{Q}_G + \dot{Q}_{21} + \dot{Q}_{20} \tag{14}$$

Substituting Equations (7), (9), (11) and (12) into (14)

$$\frac{d T_G}{d\tau} = \frac{1}{m_2 C_2}\left[E_2\left(\frac{V_{2H}^2 K_e}{R_{2H}}\right) - A_1 e_1 \sigma (T_G^4 - T_c^4) - K_L T_G^4\right] \tag{15}$$

Similarly, the energy balance for the cone is

$$\dot{Q}_{1e} + \dot{Q}_i + \dot{Q}_{21} = \dot{Q}_o + \dot{Q}_c \tag{16}$$

Substituting Equations (8), (10), (11) and (13) into (16)

$$\frac{d T_c}{d\tau} = \frac{1}{m_1 C_1} \left[E_1 \left(\frac{V_{1H}^2 K_e}{R_{1H}} \right) + A_1 e_1 \quad (T_G^4 - T_c^4) - A\sigma T_c^4 + \dot{Q}_i \right] \tag{17}$$

Equations (1) to (13) are the complete, continuous system equations.

4. LINEARIZED SYSTEM EQUATIONS

In order to study system performance under normal operating conditions, the equations presented in the previous section will be linearized to reflect perturbations from the nominal operating temperature. This is done by making a Taylor series expansion about the nominal operating temperature and retaining only the first two terms. In general

$$F(T) \doteq F(T_o) + t\, d\, F(T_o)/d\, T_o + \ldots \tag{18}$$

where

T_o = nominal temperature

$t = T - T_o$ = the perturbed temperature

Rewriting Equation (18)

$$f(t) \doteq t\, d\, f(T_o) d\, T_o \tag{19}$$

where

$$f(t) = F(T) - F(T_o) \tag{20}$$

The resultant linearized equations are presented below. From Equation (1)

$$e_G = t_G \frac{K_t R_2 V_2}{(R_2 + R_{20})^2} \tag{21}$$

where

$$t_G = T_G - T_o = \text{the perturbed guard temperature}$$

From Equation (3)

$$e_c = (t_c - t_G) \frac{K_t R_1 V_1}{R_1 + R_{10}} \tag{22}$$

where

$$t_c = T_c - T_o = \text{the perturbed cone temperature}$$

Equations (5) to (10) are linear as given. The total variables in these equations are simply replaced by the corresponding perturbation variables. Equation (11) is linearized to

$$\dot{q}_{21} = 4 A_1 e \sigma T_o^3 (t_G - t_c) \tag{23}$$

where

$$T_o = \text{the absolute nominal system temperature}$$

From Equation (12)

$$\dot{q}_{20} = t_G (4 K_L T_o^3) \tag{24}$$

From Equation (13)

$$\dot{q}_o = t_c (r A \sigma T_o^3) \tag{25}$$

The energy balance for the guard is, therefore, in linearized form

$$\frac{d t_G}{d\tau} = \frac{1}{m_2 C_2}\left[e_2\left(\frac{V_{2H}^2 K_e}{R_{2H}}\right) - (t_G - t_c)(4 A_1 e_1 \sigma T_o^3) - t_G(4 K_L T_o^3)\right] \tag{26}$$

The energy balance for the cone in linearized form is given by

$$\frac{d\,t_c}{d\tau} = \frac{1}{m_1\,C_1}\left[e_1\left(\frac{V_{1H}^{\,2}\,K_e}{R_{1H}}\right) + (t_G - t_c)(4\,A_1\,e_1\,\sigma\,T_o^{\,3}) - t_c\,(4\,A\,\sigma\,T_o^{\,3}) + \dot{q}_i\right] \qquad (27)$$

Equations (5) to (9), (10) and (21) to (27) are combined to form the system block diagram given in Figure A-5.

5. STABILITY ANALYSIS

In order to make a stability analysis of the system presented in Figure A-5, it is convenient to assume the two control loops to be uncoupled. The system can then be represented by the two independent block diagrams of Figure A-6. The coefficients are as given below

$$G_1 = \frac{1}{m_1\,C_1}$$

$$G_2 = \frac{K_t\,R_1\,V_1\,K_1\,V_{1H}^{\,2}\,K_e}{(R_1 + R_{10})^2\,R_{1H}}$$

$$G_3 = 4\,T_o^{\,3}\,\sigma\,(A + A_1\,e_1)$$

$$H_1 = \frac{1}{m_2\,C_2}$$

$$H_2 = \frac{K_t\,R_2\,V_2\,K_2\,V_{2H}^{\,2}\,K_e}{(R_2 + R_{20})^2\,R_{2H}}$$

$$H_3 = 4\,K_L\,T_o^{\,3}$$

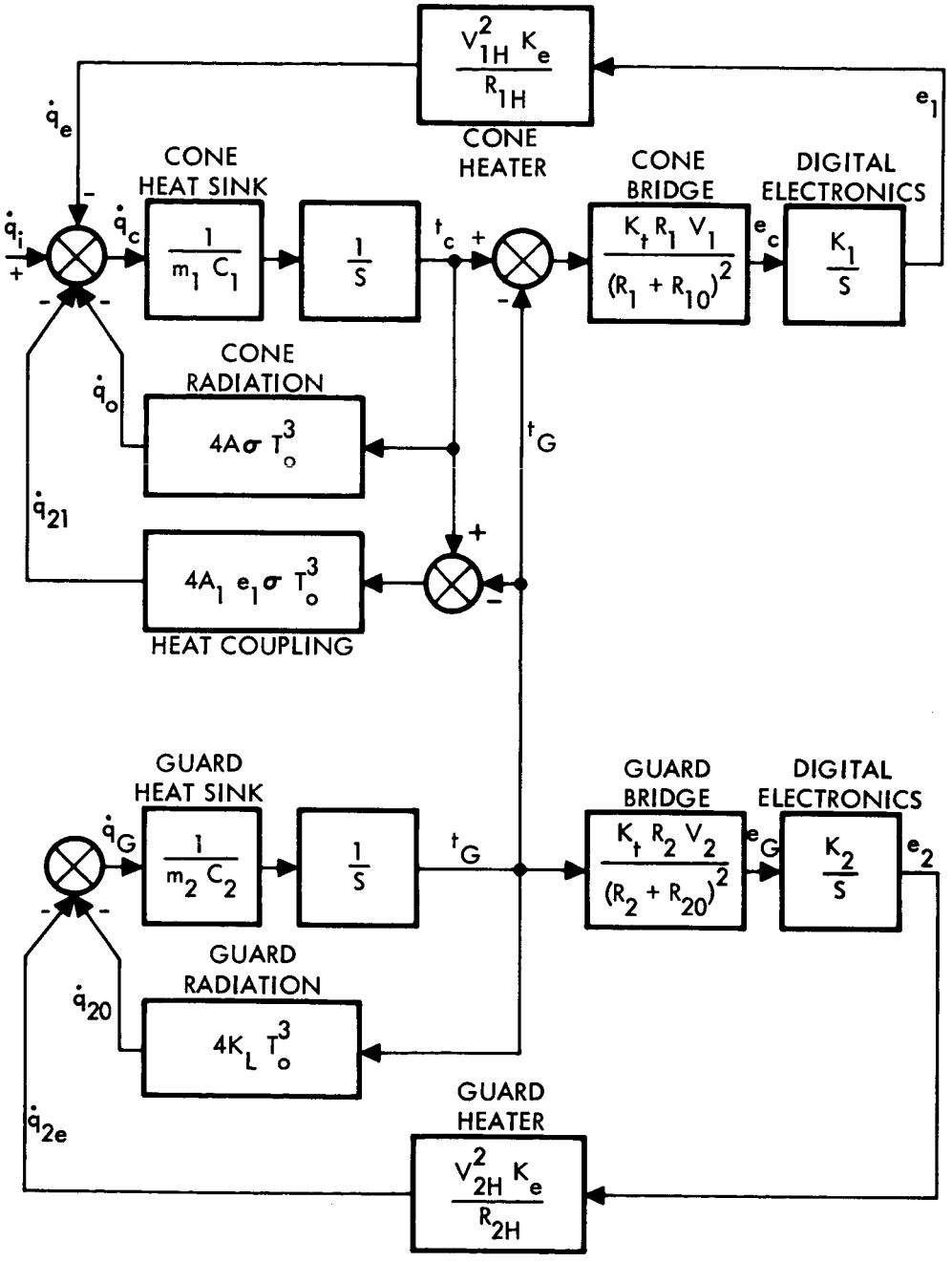


Figure A-5 Block Diagram of Linearized System

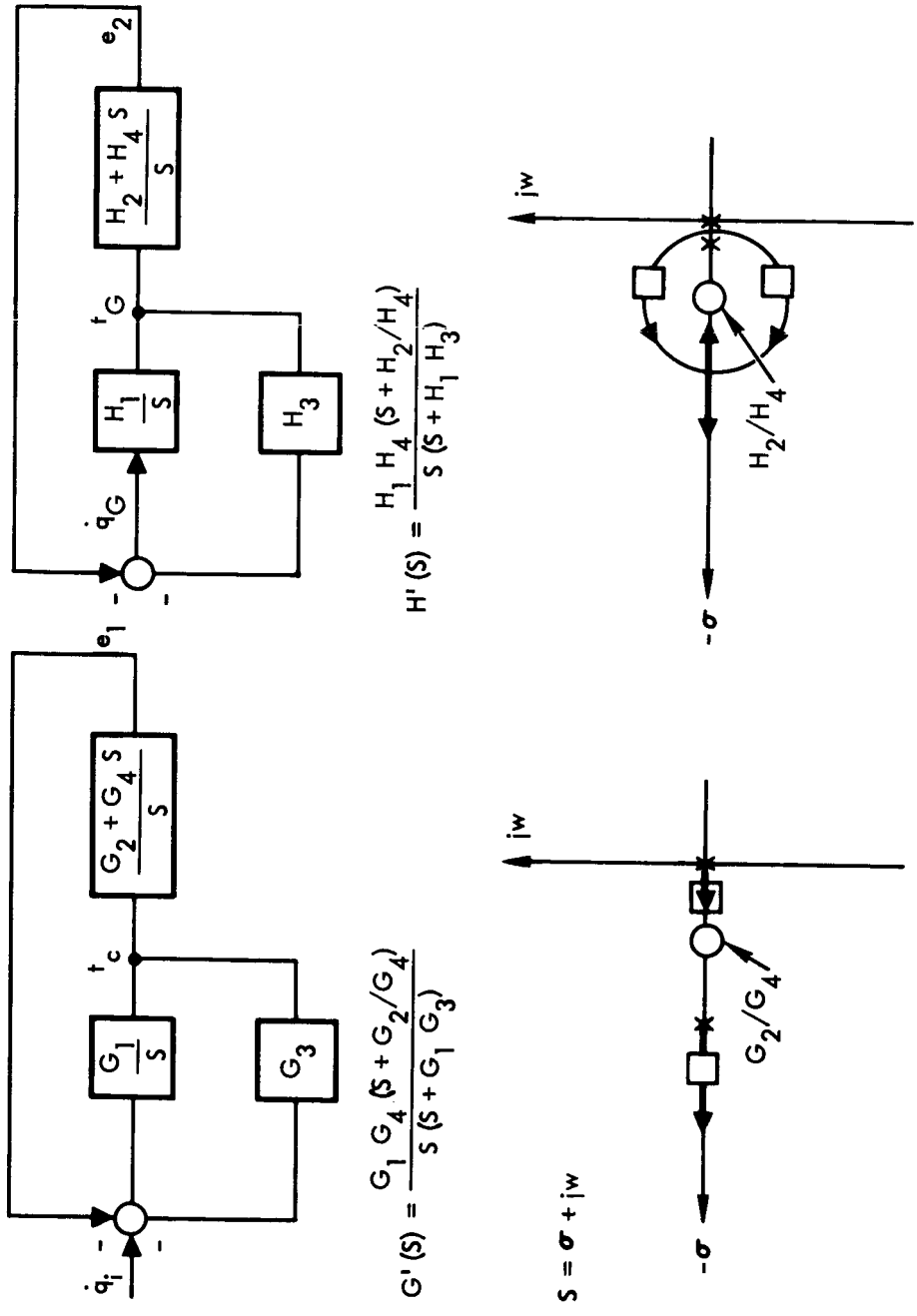
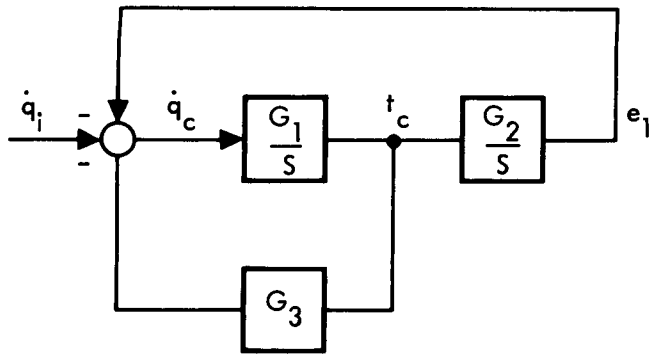


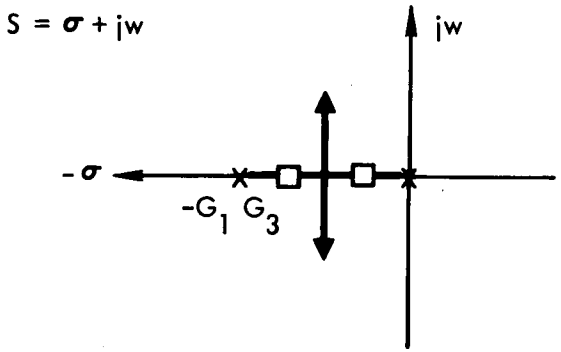
Figure A-6 Simplified Uncompensated System

Referring to the root-locus of the cone control loop, it is seen that this circuit is well stabilized. The open loop pole $-G_1 G_3$ has a large negative value because the cone represents a small heat sink (G_1 large) when compared to the cone radiation (G_3 large). The guard control loop, however, is barely stable as shown. The stability problem is actually more severe than shown since the digital electronics introduce additional phase lag into the circuit (sampling, transport delay). The closed loop pole of the actual system will, therefore, probably lie in the right hand side of the s-plane. Note that the pole $-H_1 H_3$ is non zero only because the guard has a small undesired heat loss due to radiation into space (H_3 small). It follows that causing an increase of the guard heat loss due to radiation will move the pole $-H_1 H_3$ to the left and improve the stability of the guard loop. An alternate method of obtaining improved performance is depicted in Figure A-7.

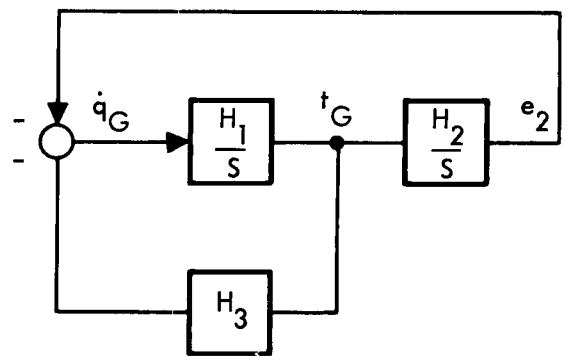
Figure A-7 shows the system with integral plus proportional compensation. G_4 and H_4 represent the gain of the proportional circuitry for the cone and the guard loop, respectively. It is seen that by proper adjustment of the gain ratio H_2/H_4 any degree of stability can be obtained.



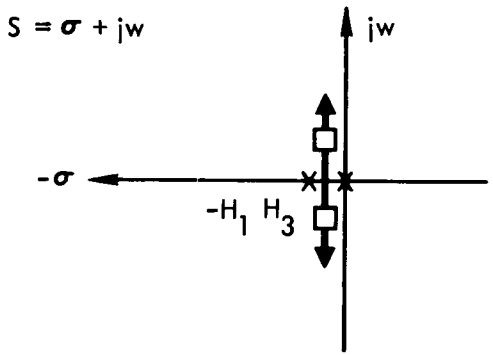
$$G(S) = \frac{G_1 G_2}{S(S + G_1 G_3)}$$



a) CONE CONTROL LOOP



$$H(S) = \frac{H_1 H_2}{S(S + H_1 H_3)}$$



b) GUARD CONTROL LOOP

Figure A-7 Simplified Compensated System