GER 13198

DEVELOPMENT OF FLIGHT CHECK-OUT SYSTEM

By J.M. Bowyer and D.P. Bickel

28 March 1967

Final Report

Prepared under Contract NAS-20598, Request No. 1-6-40-60591, by

GOODYEAR AEROSPACE CORPORATION
Akron, Ohio

for

GEORGE C. MARSHALL SPACE FLIGHT CENTER
Huntsville, Alabama

ABSTRACT

Two operating Flight Check-Out System breadboards were designed, constructed, and tested. Using a combination of analog and digital techniques, circuitry was developed that will evaluate the response of a guidance servo loop to a given forcing function. During an evaluation the Flight Check-Out System generates a programmed function that is compared to the actual response and yields an error evaluation that is indicative of the actual loop state of readiness. Two plug-in cards were constructed for each breadboard to evaluate a typical output response curve supplied by the MSFC Astrionics Laboratory. Although the circuitry was designed for microminiature packaging techniques, it was delivered on conventional printed circuit boards to facilitate experimentation at MSFC.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

SECTION I. INTRODUCTION

This report was prepared by Goodyear Aerospace Corporation under Contract NAS 8-20598, and is the final report on that contract. Flight check-out system circuitry was developed based on analog concepts that are compatible with micro-miniaturized packing techniques. Two identical sets of hardware were built, tested, and delivered to the George C. Marshall Space Flight Center (MSFC), Huntsville, Alabama. By agreement with MSFC personnel, the circuitry was not reduced to microminiature form, but was packaged on conventional printed circuit board layouts to facilitate experimentation at MSFC. The report describes the circuit design techniques and the test and evaluation procedures. Recommendations are made for improvements to be considered for future models. The procedure for calculating resistor values for the pluggable function boards is covered in an appendix.

SECTION II. CIRCUIT DESCRIPTIONS

A. FUNCTIONAL DESCRIPTION OF THE SYSTEM

Figure 1 presents a signal and control flow diagram of the flight check-out system. (A complete drawing list is contained in Appendix B). The check-out test is performed by disturbing the loop under test with a known pulse, and at the same time keying a function generator containing the normal loop response function. The time-synchronized outputs of the function generator and the loop under test are fed into a differencing circuit with the reference function inverted so that the output of the differencing circuit represents the instantaneous difference or "error-in-match" at any given point in time. This continuous-distributed error is converted to absolute values of error and integrated over the period of the test. The analog voltage output to the error evaluation and hold circuitry thus represents a total of all the incremental errors of mismatch between the loop response and the reference function. Comparison of this accumulated error voltage with a stored preset reference level determines the "go" or "no-go" output. The analog voltage error is also available as an output.

The test cycle is initiated by a "start test command" pulse to the control circuitry. The control circuitry is gated by "clear" signals from the set initial condition, function generation, and hold data circuits. Clear signals from all three must be present before the test cycle can be initiated.

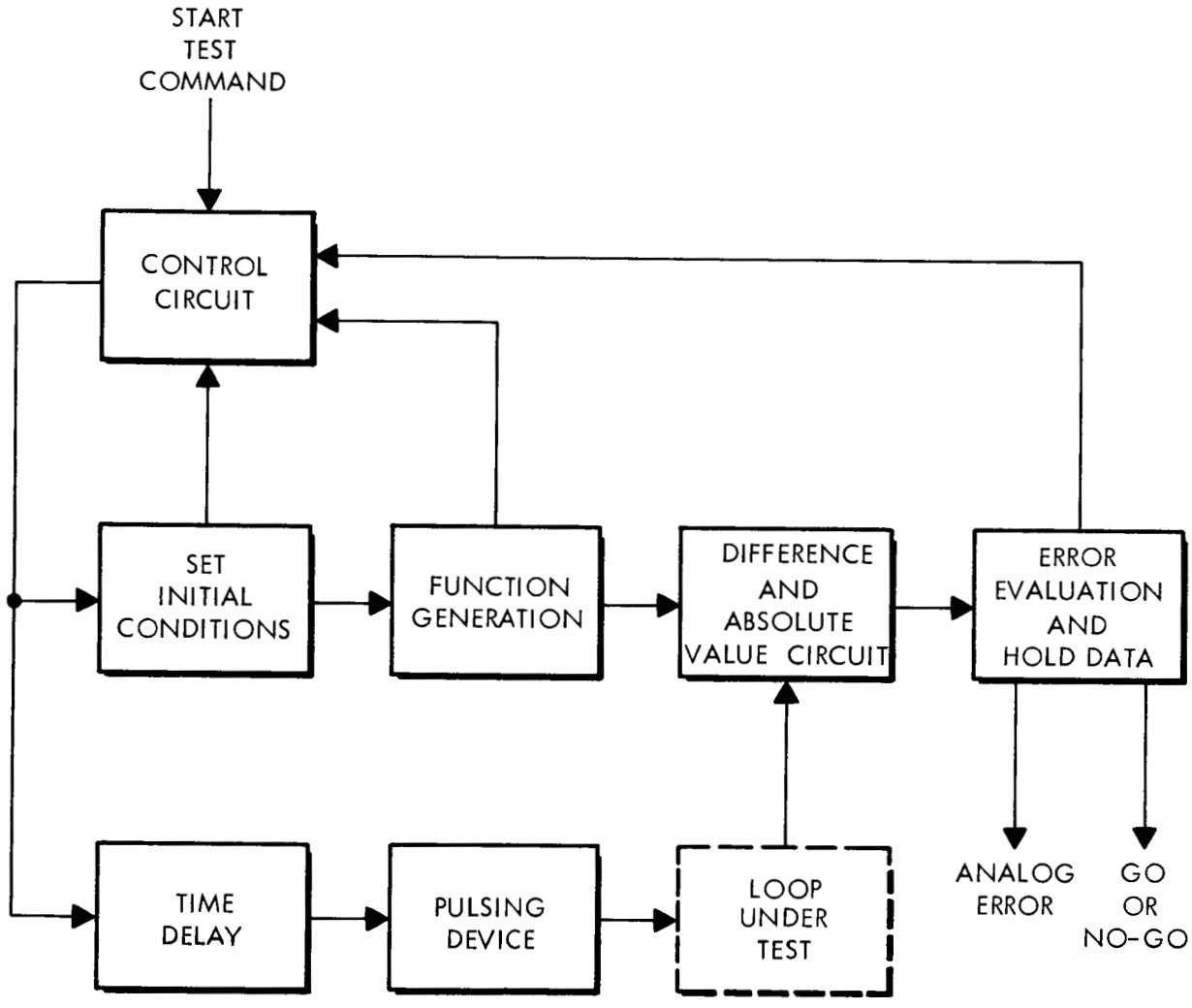


Figure 1. Function Flow Diagram

B. CONTROL CIRCUITRY

1. General

The control network establishes initial conditions prior to each test cycle and monitors the state of the circuitry during the evaluation period to prevent retriggering of the test cycle. Elements of the control circuitry are distributed throughout the system. The main control circuits are the input gating circuits, the input buffer circuit, and the timing and sequencing circuit.

2. Input Gating Circuits

Figure 2 shows the input gating logic circuitry in functional form. The gating circuits prevent retriggering of the system while a test cycle is in progress. The

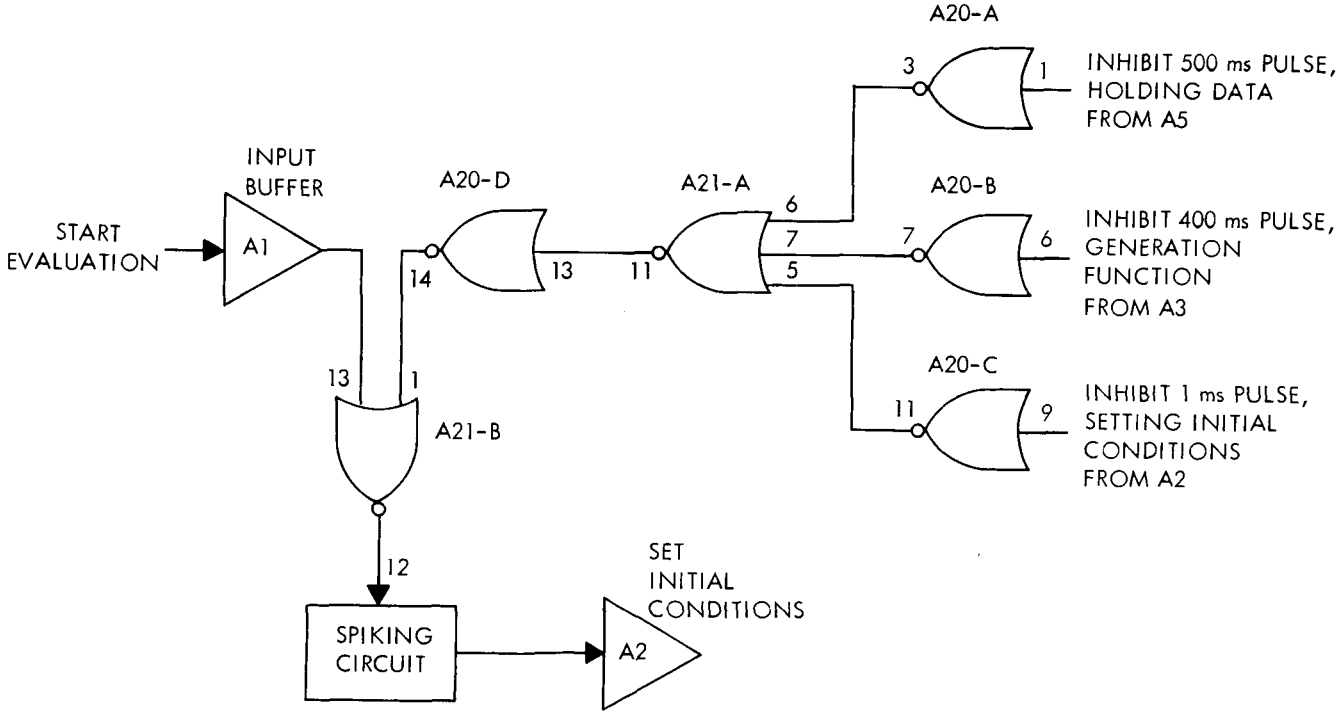


Figure 2. Gating Logic

devices marked A20 are dual gating circuits, all contained in one package. The A21 devices are quad input gates, and are also contained in one package. The start evaluation pulses (output of input buffer A1) are gated through A21-B, which requires a positive pulse ("1" level) on both inputs to yield the required negative pulse ("0" level) at its outputs. If a "1" level pulse (+3 volts) appears on the inputs to A20-A, -B, and -C, then outputs will be at "0" level, resulting in the output of A21-A going to "1" level and the output of A20-B going to "0" level. Since the output of A20-D drives A21-B, the output of A21-B will be inhibited from going to "0" level until the inputs to A20-A, -B, and -C have been cleared. Thus, no start evaluation pulse can be passed on to initiate the test until the system is ready to receive it.

3. Input Buffer

The input buffer stage A1 is a monostable multivibrator that buffers the start evaluation pulse to the control logic circuitry. Figure 3 shows a simplified schematic of the circuit, which is typical of a number of monostable multivibrators used throughout the system. The series resistor string (R1, R7, and R2) holds the quiescent input levels of the Fairchild μA 709 integrated operational amplifier within the common mode range. R7 provides approximately 150 millivolts of reference between the two inputs, thereby holding the amplifier output to ground and acting as the recharging drive level. R13 and R14 isolate the input and feedback signals from the reference sink and from each other. Capacitor C1 differentiates the input square wave pulse (10 milliseconds, approximately 5 to 10 volts positive). The resulting negative-going spike starts the amplifier output going in a positive direction until, with the aid of positive feedback network R36 and C6, the amplifier is driven to the positive stop. Once the amplifier output hits the positive stop (at approximately the supply voltage), capacitor C6 begins to discharge, essentially through R36 and R14. When the feedback current falls to a value where it and the current through R14 do not exceed the quiescent current drive through R13, the

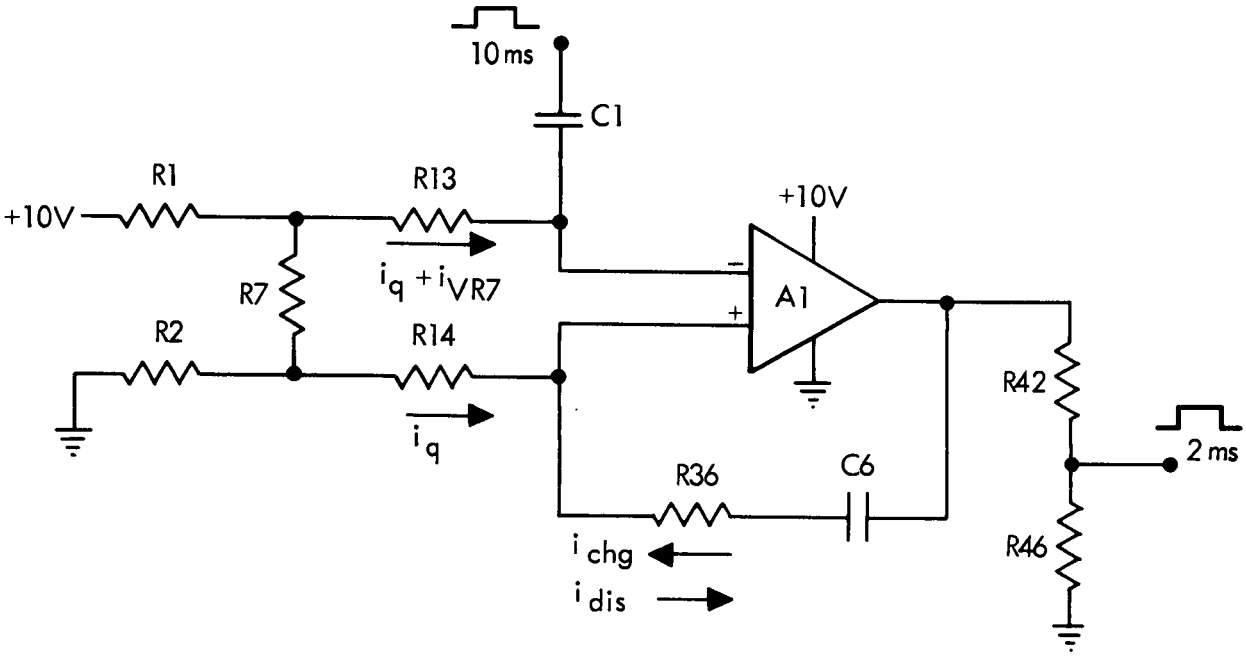


Figure 3. Input Buffer

amplifier output starts going in a negative direction and is driven with the aid of regenerative feedback through R36 and C6 to the full negative stop, where it is clamped by the voltage across R7. With a μA 709 integrated amplifier and a 10-volt supply, a pulse amplitude of approximately 9.5 volts is developed. Attenuator network R42 and R46 reduce this to the level of the logic circuits.

4. Timing and Sequencing

The timing and sequencing of the tester is established by a series of monostable multivibrators essentially identical in circuit configuration to input buffer A1.

Monostable multivibrator A2 is designed to give a 1-millisecond pulse which is used to set up the initial start conditions throughout the tester. A2 receives its

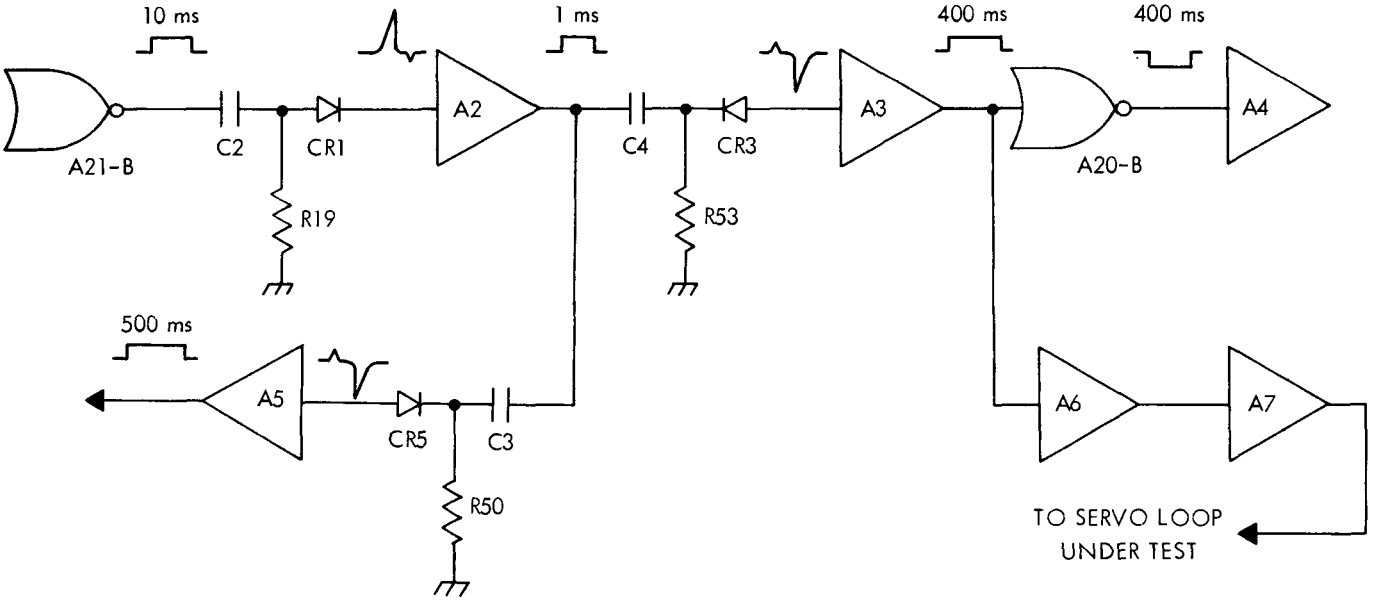


Figure 4. Timing and Sequencing

input from A21-B through a spiking circuit formed by C2, R19, and CR1 as shown in Figure 4. The output of A2 is also fed to gate A20-C to prevent retriggering of the test cycle during the initial conditions period.

Multivibrator A3 is programmed to generate a 400-millisecond pulse that establishes the range used in the function generator. A3 is fed by a spiking circuit formed by C4, R53, and CR3, which triggers A3 on the trailing edge of the output pulse fall time of A2, as shown in Figure 4. The output of A3 provides an inhibit pulse to gate A20-B to prevent retriggering of the test cycle during the function

generation period. The output of A20-B, which is a negative 400-millisecond pulse, is also used to drive ramp generator A4. In addition, the direct output of A3 drives A6 in the pulsing circuit of the servo loop under test.

Multivibrator A5 is programmed to generate a 500-millisecond pulse that holds the error voltage output of the error evaluation circuit while a readout is being taken. A5 output also provides an inhibit pulse to gate A20-A to prevent retriggering of the test cycle during the error evaluation period. A5 is triggered by the spiking circuit formed by C3, R50, and CR5, which operates on the trailing edge of the square wave output of A3.

A6 and A7 are two monostable multivibrators used to sequence the triggering of the actual servo loop under test. A6 is driven by the leading edge of the 400-millisecond pulse from A3, and its delay sets the time for the triggering of A7. The time constant for A6 is selected at test, to ensure that a correct time relationship between the actual response loop under test and the function generator occurs for arrival at the differencing circuit.

C. FUNCTION GENERATION CIRCUITS

The function generation portion of the system is composed of the ramp generator, the function generator, and the summing circuits. The operation of each is discussed below.

1. Ramp Generator

The ramp generator develops a linear voltage ramp from approximately +5 volts to 0, which is used to drive the function generator circuits. The ramp circuit is activated by the negative 400-millisecond pulse developed by monostable multivibrator A3 and inverted through dual gate A20-B. Figure 5 shows the basic ramp generator circuitry.

The ramp generator is essentially an analog integrator, whose reference input

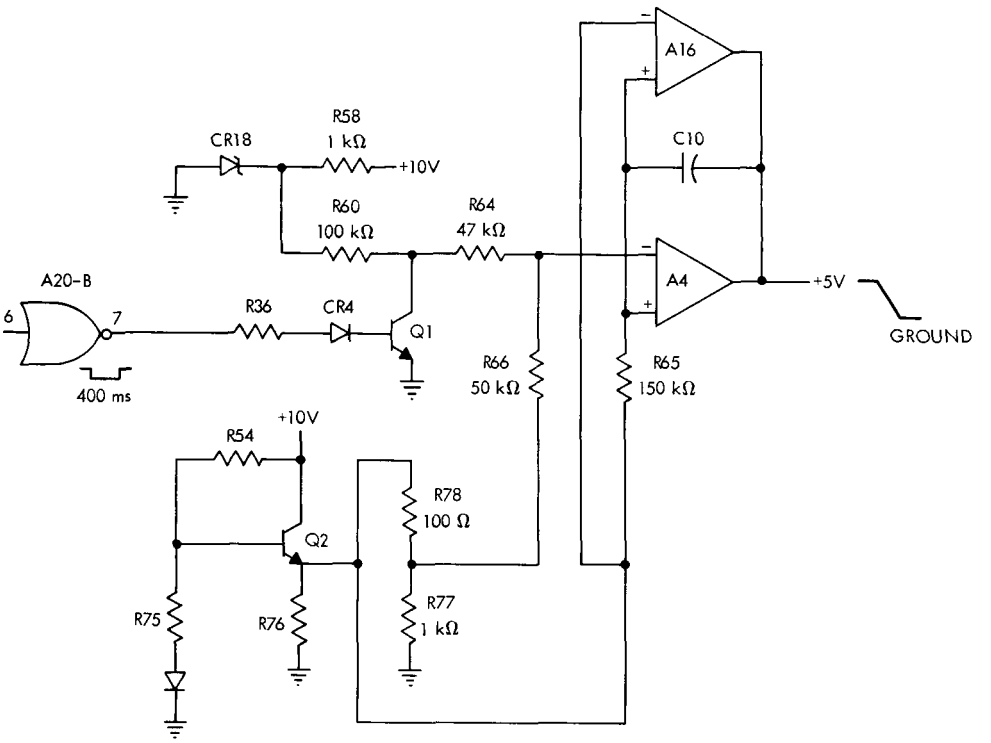


Figure 5. Ramp Generator

voltage is derived from the zener diode CR18. This diode is always maintained in the ON condition to reduce the effects of turn-on transients and short-term heating effects. The reference input voltage is removed from the amplifier input by grounding the center of the input resistors R60 and R64 through transistor Q1. The gating of Q1 is controlled by the 400-millisecond pulse from A20-B. Diode CR4 guarantees turn-off of Q1, and R36 limits Q1 base current to approximately 1 milliampere.

During the standby condition, the ramp generator output is driven to the positive limit of the boundary circuit A16 by the potential across R78, a select-at-test resistor. This potential is developed as a differential input across R66 and R65. Transistor Q2 is used as a low-impedance voltage reference to hold the quiescent d-c level within the common mode range of A4.

With the cut-off of Q1 by the 400-millisecond pulse from A20-B, the amplifier drives a constant current into capacitor C10 based on the constant voltage (V_Z) from CR18 and the time constant of the input resistors and C10.

$$i_{cap} = \frac{V_Z - \epsilon}{R} = \text{a constant for the ramp generated}$$

where ϵ = amplifier offset.

Therefore, the output of the ramp generator changes as follows:

$$V(t) = \frac{1}{C} \int \frac{V_Z - \epsilon}{R} \, dt = \frac{V_Z - \epsilon}{CR} \, t$$

$$V_{out} = V_{bound} - V(t)$$

The ramp generator is limited in its positive and negative excursion by a bounding circuit that limits the amplifier to its linear region of operation. This technique guarantees that the amplifier saturation storage problems can be ignored and that the limits will be repeatable with any input signal. The best overall performance from a bounding circuit is through the combination of a passive bound circuit and a leakage-current suppression circuit.

The passive bound circuit is shown in Figure 6. With the amplifier V_O at null, there is no potential difference between V_O and the common mode neutral, and the bounding circuit is in a quiescent state. In this mode there is a bias current between the two supplies that causes both matched zeners, ZA and ZB, to be activated. This zener action places EA at the zener potential above null and EB at the zener potential below null. At this time both diodes DA and DB are reverse-biased, so that no error current flows and their common point "M" is at the common mode neutral position. Therefore, with both ends of resistor RT at the same potential, no voltage is developed across it and no error signal is injected into the inverting input. If a negative signal is applied at the inverting input, the output will start

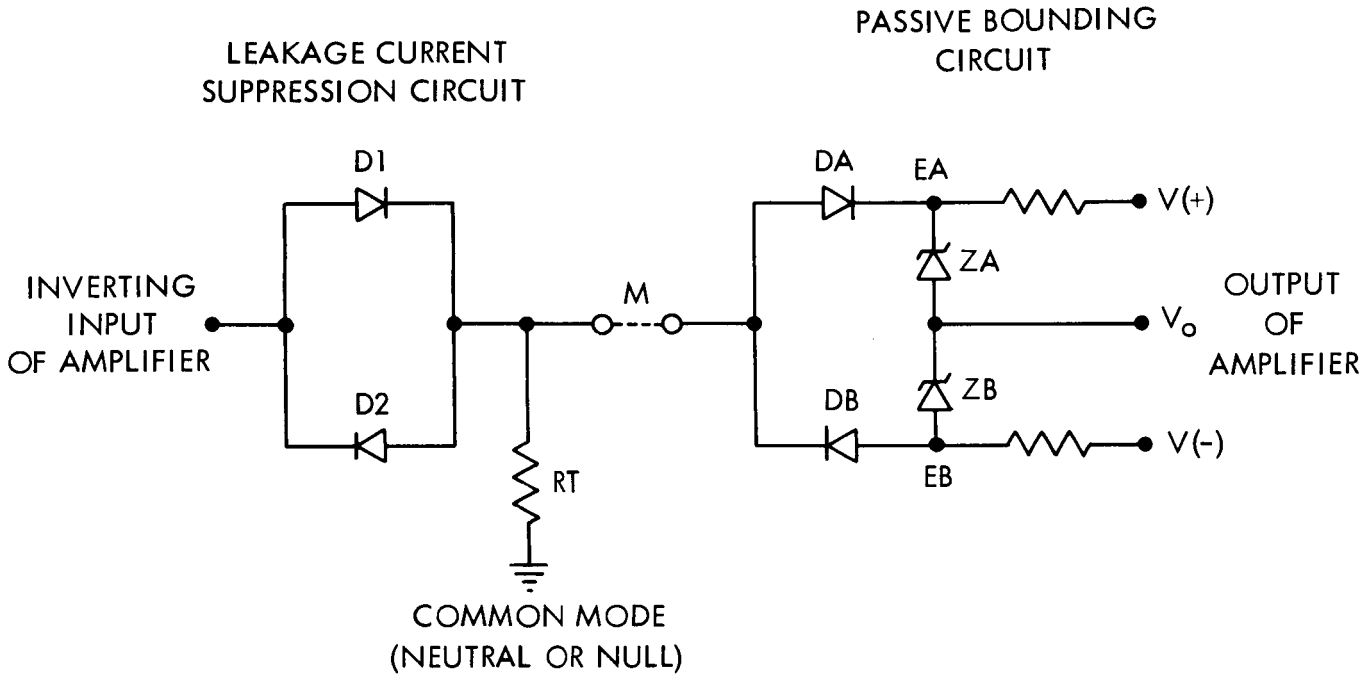


Figure 6. Bounding Circuit

positive. The zener ZA will go out of zener regulation as soon as V(+) - V_o is less than V_{ZA}. The point EA will approach the positive supply and diode VA will be reverse-biased to a larger amount. Diode DA must not break down. The point EB will also start positive. The zener ZB will stay in regulation and will lift the point EB to track the output. The point EB will always be less than V_o by the zener drop of ZB. When the output exceeds the zener potential of ZB, the point EB is lifted above the common mode neutral and diode DB becomes forward-biased. This error signal is fed across RT and into the inverting input through the forward-biased diode D2, which will inhibit the output swing. For a positive input the reciprocal action occurs with point EA being pulled more negative than the common mode neutral and forward biasing DA and D1. The bounding limits are set by the

two zener diodes ZA and ZB, and the influence of the diode drop of steering diodes DA, DB, and the leakage diodes D1 and D2.

The leakage-current suppression circuit, shown in Figure 6, functions as follows. The point "M" could be connected to the inverting input without negating the preceding explanation. The purpose of RT, D1, and D2 is to prevent the leakage currents of DA and DB which are, of course, functions of temperature and voltage and doping levels, from generating correcting signals that are not functions of the output level. The purpose of RT is to provide a leakage current path to ground that does not act as an injected error signal through the input stage transistors. Basically the signal at point M will see the resistor RT in parallel with diodes D1 and D2, since the intrinsic offset voltage between the inverting and non-inverting inputs is on the order of millivolts. Therefore, RT must be small enough to absorb all the leakage currents at high temperatures without the corallary of sinking all of the feedback drive signal currents.

2. Function Generator

The function generator consists of 24 double-ended limit switches, which are cascaded so that each is activated in a preset order, with the turn-off of one being the turn-on signal for the next one in the sequence. The 24 switches are driven by ramp generator A4. Figure 7 shows a simplified schematic of the basic function generator circuitry.

The μA 711 integrated comparator is used as the double-ended limit switch or "window generator." The period of operation on ON-time is established by the difference in magnitude between the reference level voltages set into it and the ramp dV/dT. When the input ramp voltage amplitude equals that of the upper reference voltage, the amplifier switches from +3.5 volts to -0.5 volt and remains there until the ramp voltage equals or exceeds the lower reference voltage set into the amplifier. At that time the amplifier output switches back to +3.5 volts. The upper

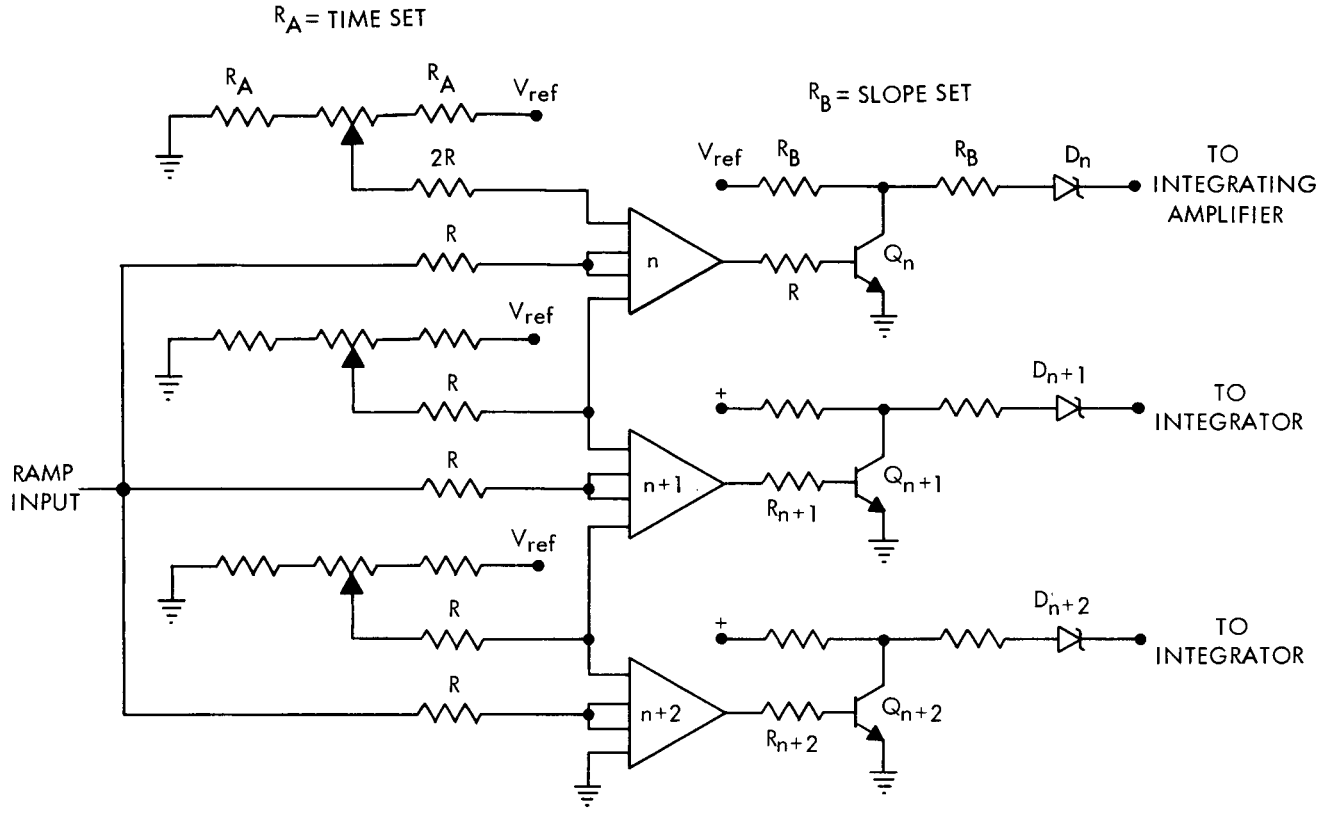


Figure 7. Function Generator

limit for one switch is the lower limit for the next switch, so that a series of 24 continuous time segments or windows is generated whose total time is equal to that of the generated input ramp voltage (400 milliseconds). The settings of the reference level voltage inputs to the amplifier switches are adjustable and are set according to the function being generated.

The output of each amplifier switch drives a transistor which is normally operating in saturation, but is cut off during the time period that the switch output is at -0.5 volt. Each μA 711 transistor pair when cut off permits a precision reference voltage to be applied to an integrating amplifier through a precision input resistor

network that is associated with each μA 711 transistor pair. Thus, the OFF period of a transistor, as determined by the -0.5 volt period of its amplifier switch, defines a line segment period. The value of the precision reference voltage to the integrator determines the charging rate or "slope" of the line segment. The polarity of the slope of each line segment depends upon which integrator it is associated with in the current.

3. Summing Circuits

Figure 8 shows a simplified block schematic of the integrators and summing amplifiers associated with the function generator circuitry.

The assignment of switch amplifier outputs to integrator A8 or A9 is dependent upon the desired polarity for the line segment that each represents. Integrator A8 holds negative segments for 400 milliseconds and A9 holds positive segments for 400 milliseconds. The output from A9 is inverted through A15 and summed in amplifier A10 with the output from integrator A8. The output of A10 thus represents the complete generated function with an inverse polarity to the actual function. The reference voltage to the two integrators is controlled by Q3, which is disabled except for the 400 millisecond function generation period, which prevents a function being generated during the reset of the ramp generator. Figure 9 shows the generation of a sample function starting with time pulses through to the output of A10.

D. DIFFERENCING CIRCUIT

The differencing circuit is a standard summing amplifier circuit using a feedback amplifier in which the output of the loop under test and the inverse of the generated function are added together. When properly calibrated, the output of the differencing amplifier, A11, represents the instantaneous mismatch of the generated and actual loop response at any time during the 400 millisecond test cycle. The gain of function amplifier A10 and the timing of the monostable miltivibrator A6 are

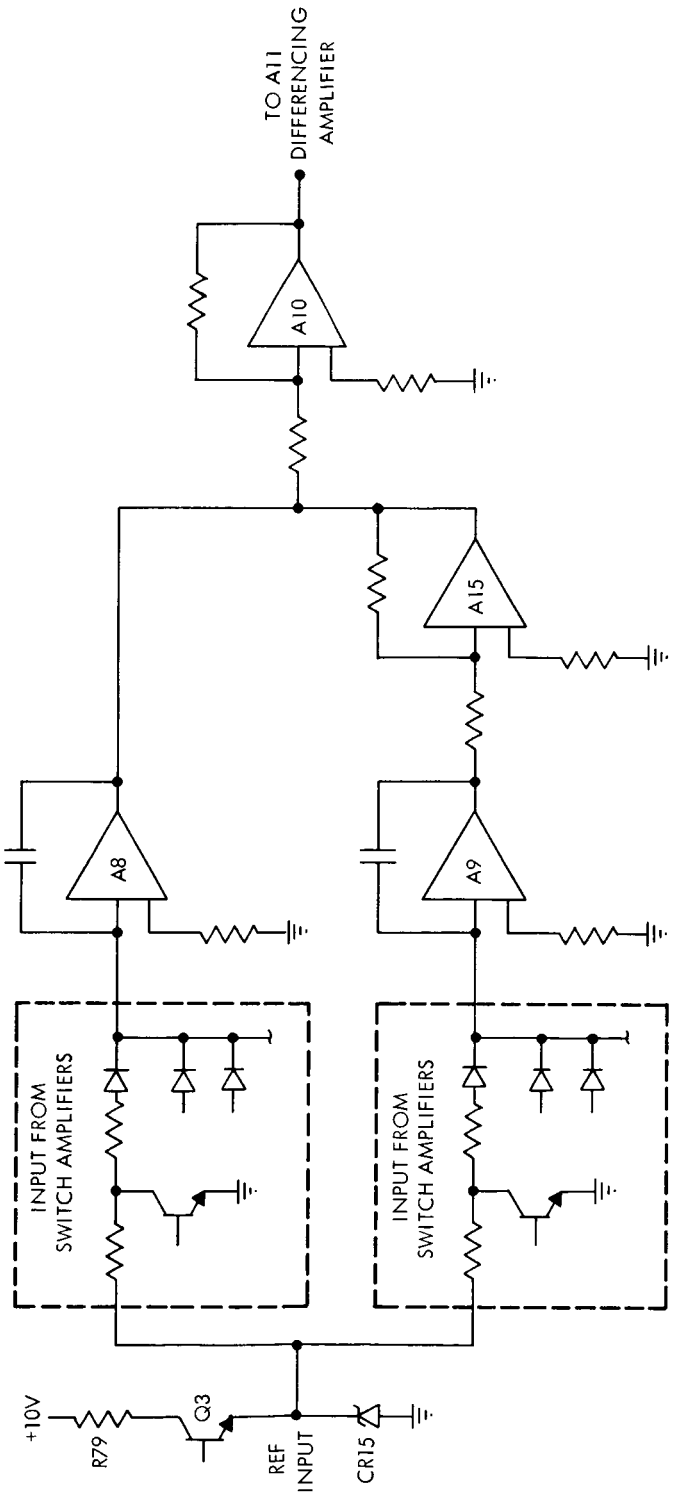


Figure 8. Integrators and Summing Amplifiers

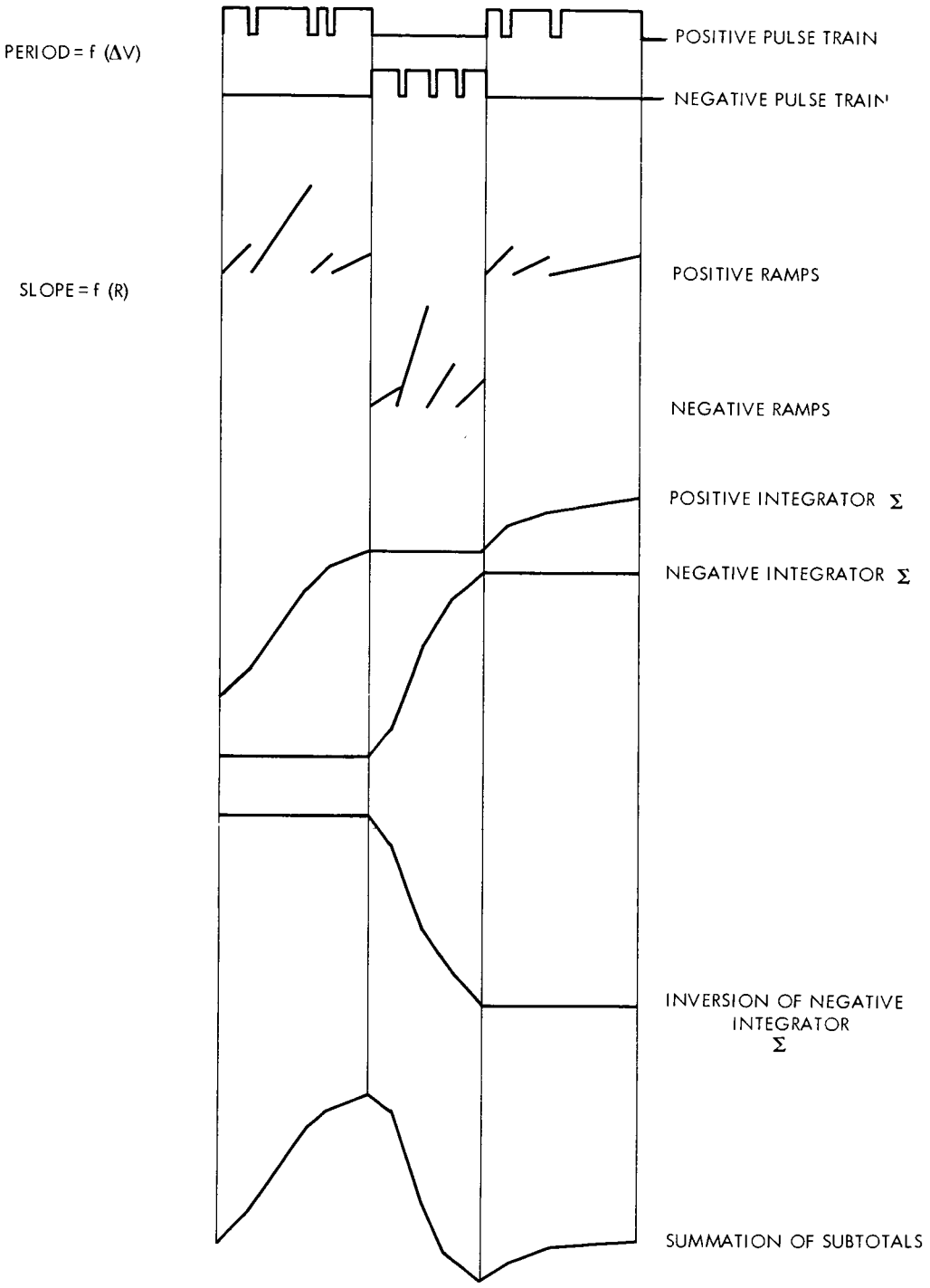


Figure 9. Sample of a Complete Generated Function

calibrated during setup to achieve time and amplitude synchronization with the response of the loop under test.

E. ABSOLUTE VALUE FUNCTION

The absolute value function makes use of the classical technique of analog computers for absolute value. The error function is doubled in gain inside the feedback loop of A12. Amplifier A12 has two feedback loops and an inversion at the output of the input signal. All positive excursions are inverted, doubled, and passed through CR12; all negative error excursions are inverted, doubled, passed through CR13, and brought out. This function is then added to the original function, canceling the negative excursions in a manner that gives them an equal positive excursion. Thus

$$F(t) = (-\epsilon) - 2(-\epsilon) = -\epsilon + 2\epsilon = +\epsilon$$

is generated without modification of the positive-going excursion. This forms basically a full-wave rectification. Of course either option was available, a positive absolute value or a negative absolute value. Also, during construction R108 is selected during test to obtain a true full-wave rectification and thus delete the contribution of the CR13 voltage drop. This "full-wave rectified" error function (all positive excursions) is integrated by A13 to establish a fixed value for the summation of all the spread out incremental errors. A fixed value can be established during setup by adjusting C30 for the particular error acceptable for the calibrated actual system. Any greater discontinuity would then increase this voltage and would establish the amount of deviation. With the maximum deviation established, the one-shot A14 is set using R110 and R113 to trip at maximum permissible error as it appears on analog output E14.

SECTION III. TEST AND EVALUATION

In the absence of an actual servo loop with the response characteristic matching the single response function provided by MSFC, it was necessary to devise an alternate test procedure which would give a valid indication of the operation and repeatability of the two prototypes.

This was accomplished by programming the two systems to generate the MSFC-supplied response function. The function generated by each system was then fed into the actual system-under-test response input of the other. Thus each prototype developed an error output using the generated function of the other as the actual loop-under-test response. A comparison of the outputs of both differencing circuits was then made and always found to be repeatable to better than 1 percent.

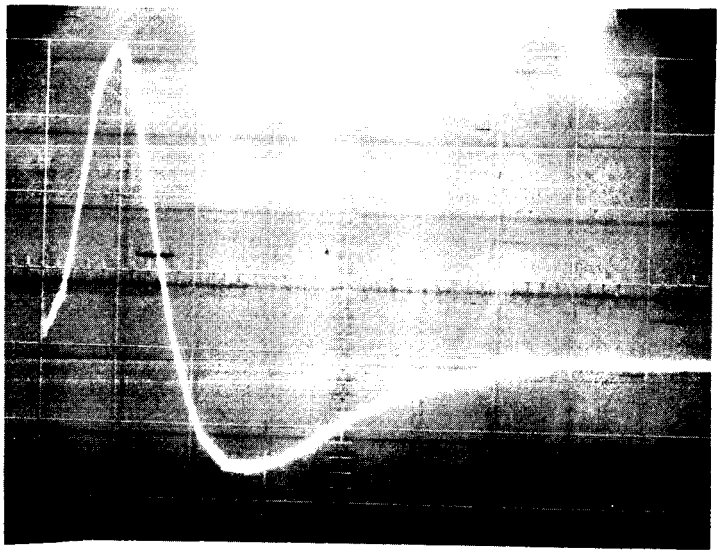
Starting at the difference circuit, the amplitudes of the output signals in the testers are functions of the scale factors built into the difference circuit, absolute value function, and the error function integrator. The absolute value functions were adjusted to yield a true full-wave rectification of the error signal. The values of the other two function scale factors were chosen arbitrarily from the cross-coupled responses to yield a significant error voltage magnitude for accurate reading.

The prototypes were tested and evaluated under controlled laboratory conditions. The magnitude of the error from the actual system could saturate the error integrator and the scale factors would then require modification.

The actual loop responses for the two prototype testers were recorded on film and are shown in Figure 10.

SYSTEM 1

Vertical - 1 volt/div
Horizontal - 50 ms/div



SYSTEM 2

Vertical - 1 volt/div
Horizontal - 50 ms/div

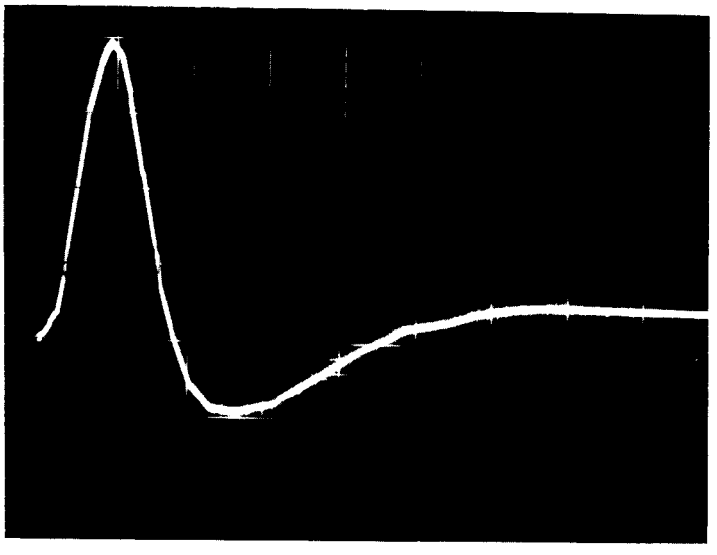


Figure 10. Loop Responses

SECTION IV. CONCLUSIONS AND RECOMMENDATIONS

The analog concept of flight check-out circuitry developed under this contract performs the essential functions required of it within acceptable limits. Although the circuitry was packaged conventionally to facilitate experimentation, the circuit design is adaptable to various degrees of miniature packaging, depending upon the amount of flexibility in function setting desired. For example, with a fixed function the flight check-out circuitry as presently conceived could be packaged in a 3 by 3 by 1 inch module.

By applying the experience gained in designing the present circuitry and a knowledge of new devices and advancements in the state of the art, a number of improvements could be made in future models, resulting in fewer components and/or better performance. Some of these possibilities are listed below.

(1) Convert the logic to use high-voltage Amelco, which would eliminate the level shifting networks on the outputs of the monostable multivibrators.

(2) Obtain more stable reference voltages by the use of Fairchild μA 726 integrated circuits for the reference zener diodes.

(3) Obtain better ramp linearity by using the μA 726 as a preamplifier for the μA 709 preamplifier in the ramp generator circuit.

(4) Convert the μA 709 monostable multivibrators to a conventional integrated circuit approach, which would eliminate the roll-off networks for the μA 709's.

(5) Replace the discrete capacitor-diode-resistor spiking circuits with additional integrated gating circuitry to achieve a size reduction.

(6) Replace the discrete resistor-transistor switches driven by the μA 711 circuit with J-FET switches similar to the Amelco analog gating circuits.

Further improvements in the timing precision might be achieved through greater utilization of digital techniques. For example, all general timing functions could be performed by MOS countdown circuits referenced to either an internal or external precision clock. Digital techniques might also be extended to timing the function increments. One approach could be to divide the function period into 40 equal periods through the use of count-down and flip-flop circuits. This would provide a 40-segment function generator where only the integrator summing resistors are analog in nature. This would fix the number and period of function increments, but still permit selection of the slope and polarity of each segment. This approach could be carried one step further by completely digitizing the generation of the function, but this would have the disadvantage of requiring a unique set of circuitry for each loop response generated.

APPENDIX A. FUNCTION GENERATION PROCEDURE

1. The function to be reproduced should be overdrawn with a maximum of 24 straight-line approximations that have a maximum total period of less than 400 milliseconds.

2. Each segment should be evaluated serially from t = 0 to T = max to determine the Δt of the segment and the ΔV of the segment. The units are not important as long as the same scale factor is used in measuring each segment.

3. A figure of merit for each segment is now generated by the ratio of $\Delta t/\Delta V$, which will be used to compute that segment's contribution to the total function.

4. To develop the function magnitudes within the capability of the tester integrators, the $\Delta t/\Delta V$ ratios are weighted to guarantee that within the time the segment is active, it can lift the integrator the required additional voltage. Since the largest resistors available for the integrators are one megohm each, the smallest contributor of charge or the largest $\Delta t/\Delta V$ number will be considered to be equal to 2 megohms. Thus if the largest figure of merit were 12,

   2.0 meg = 12 figure of merit
   1.0 meg = 6 figure of merit
   0.5 meg = 3 figure of merit

   All of the resistors for the slope card are thus defined. In some cases this value cannot be obtained by the sum of two equal-value resistors. For the center clamping, two resistors as close as possible to this value should be used.

   The first increment at t = 0 is defined by the series sum of R401 and R402 on

the slope card. The remaining segments are internally connected so that R403 - R404 is the next segment evaluated, etc.

5. The period of integration for a segment is defined by the input ramp. This ramp is bounded on both ends and has a fixed period of t = 400 milliseconds. The function ramp voltage swing and period are both measured, and a calibrated construction factor of volts per millisecond is obtained. For a given segment period the ramp volts per millisecond construction factor is multiplied by the period of the segment to develop the ΔV or voltage between the double-ended limiters. Thus

   5V/400 ms = 1/80 volts/ms

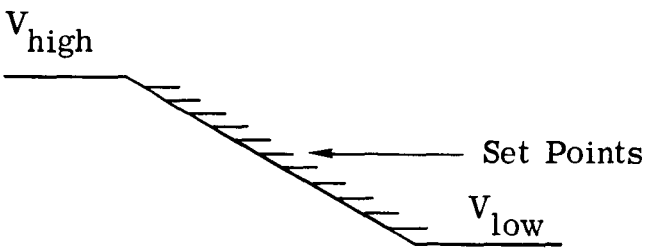
   segment "n" = 100 ms

   Therefore, the segment limit differential = 100/80 or 1.25 volts.

   This means that the lower double-ended limit should be 1.25 volts less than the upper double-ended limit to develop a gate out of the μA 711 of 100-millisecond duration.

   This voltage is developed by the ratio of two series resistors whose sum should be approximately 10 kilohms. When the resistor timing card is properly connected, a one kilohm built-in trim potentiometer is connected between each divider to provide a 10 percent trim adjustment of the center tap.

   One word of warning. Consider the ramp:



If the trim potentiometer on segment one is too high, it will activate the first segment on standby. Thus the absolute value of the turn-on voltage for the period of the first segment should be less than the peak voltage of the ramp on standby. This criterion also applies to the last segment. To guarantee turn off, the turn-off voltage must be less than the lowest ramp voltage or the last segment never stops integrating.

6. The breadboard function was based on the response shown in Figure 11. Table I records the ΔV and Δt and the calculated figure of merit, and gives the ideal slope resistances and time set voltages.

   Actual resistance values used on the timer and slope plug-in cards are documented on GAC drawings 315N002-003 and 315N002-004.

Table I. Calculation of Resistor Values for Function Boards

Increment	ms/volt	Figure of Merit	Slope Resistance (ohms)	Control Pot.	Set Voltage Level (at 9mV/ms)
1	3.2/ 0.14	22.85	6.55×10^4	R201	5.150
2	4.4/ 0.2	22	6.28×10^4	R202	5.122
3	4.4/ 0.54	8.15	2.33×10^4	R203	5.083
4	11.0/ 2.02	5.45	1.56×10^4	R204	5.044
5	7.0/ 0.62	11.3	3.23×10^4	R205	4.933
6	3.6/ 0.21	17.15	4.9×10^4	R206	4.305
7	4.4/ 0.15	29.35	8.55×10^4	R207	4.273
8	6.0/-0.15	-40.0	11.45×10^4	R208	4.234

Table I. Calculation of Resistor Values for Function Boards (Continued)

Increment	ms/volt	Figure of Merit	Slope Resistance (ohms)	Control Pot.	Set Voltage Level (at 9mV/ms)
9	5.6/-0.43	-13.02	-3.72×10^4	R209	4.180
10	12.4/-1.28	-9.69	-2.76×10^4	R210	4.129
11	16.4/-1.62	-10.15	-2.9×10^4	R211	4.011
12	11.6/-0.8	-14.5	-4.15×10^4	R212	3.869
13	10.8/-0.62	-17.4	-4.97×10^4	R213	3.764
14	12.8/-0.3	-42.6	-12.2×10^4	R214	3.657
15	16.4/-0.05	-328.0	-93.7×10^4	R215	3.542
16	28.6/+0.14	206.0	58.9×10^4	R216	3.396
17	27.8/ 0.33	84.3	24.0×10^4	R217	3.139
18	24.4/ 0.32	76.7	21.9×10^4	R218	2.889
19	19.2/ 0.18	106.5	30.4×10^4	R219	2.667
20	12.8/ 0.15	85.4	24.4×10^4	R220	2.494
21	26.0/ 0.09	289.0	82.6×10^4	R221	2.379
22	26.0/ 0.16	162.5	46.5×10^4	R222	2.145
23	25.8/ 0.07	369.0	105.5×10^4	R223	1.911
24	21.0/ 0.03	700.0	200×10^4	R224	1.679
				R225	1.470

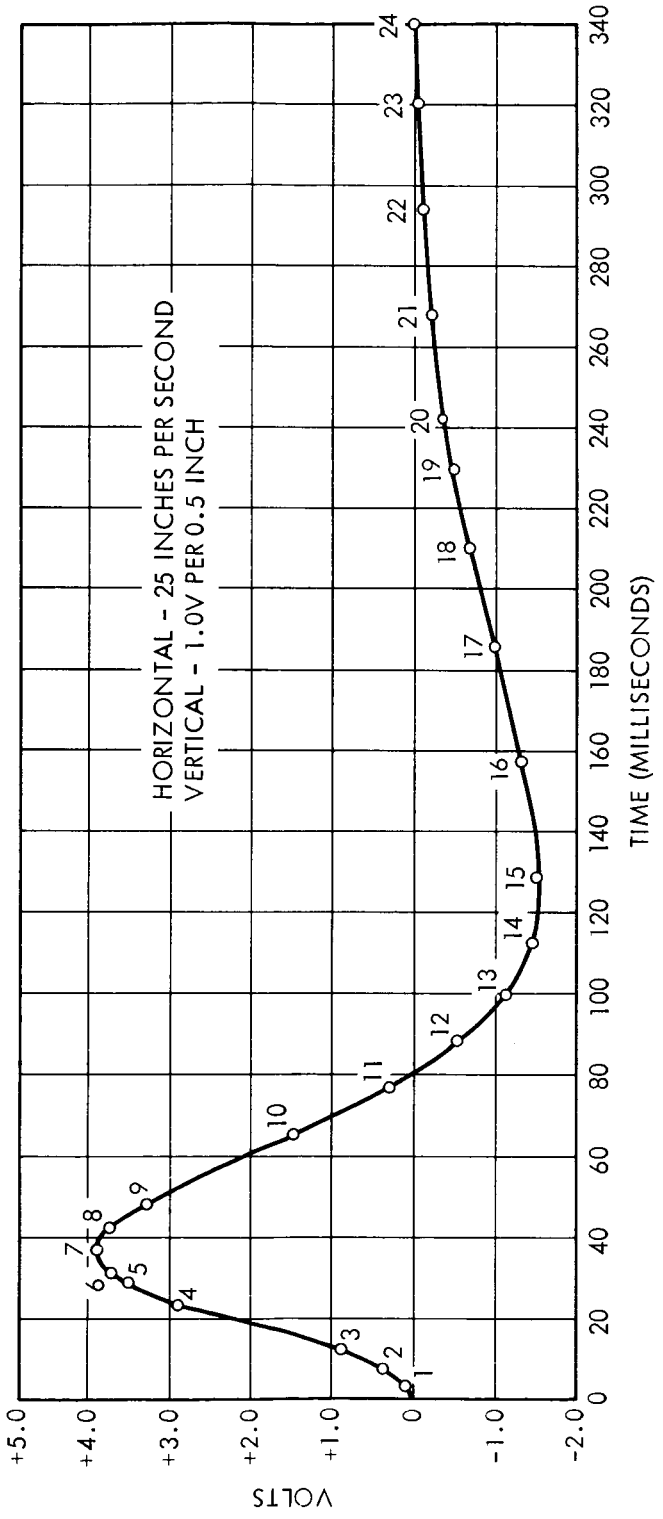


Figure 11. System Response

APPENDIX B. LIST OF DRAWINGS

315N002-001	Final Assembly, In-Flight Tester
315N002-002	Printer Wiring Assembly, Function Generator
315N002-003	Printed Wiring Assembly, Slope Function Card
315N002-004	Printed Wiring Assembly, Timer Function Card
315N002-005	Printed Wiring Assembly, Control & Evaluation
315N002-012	Electrical Schematic, Function Generator
315N002-013	Electrical Schematic, Slope Function Card
315N002-014	Electrical Schematic, Timer Function Card
315N002-015	Electrical Schematic, Control & Evaluation