NASA TECH BRIEF

Parallel-to-Serial Biphase-Data Converter

Register Sequence For All True
Loading And Inverting With Shift
Register

n   . . . c b a
n+1 . . . d̄c̄b̄
n+2 . . . e d c

Register Sequence For Alternate True/False
Loading And Direct Shifting

n   . . . c̄b̄a
n+1 . . . d̄c̄b̄
n+2 . . . e d̄c

Note: Shift Register And Frequency
Divider Change On Same
Polarity Of Slope.
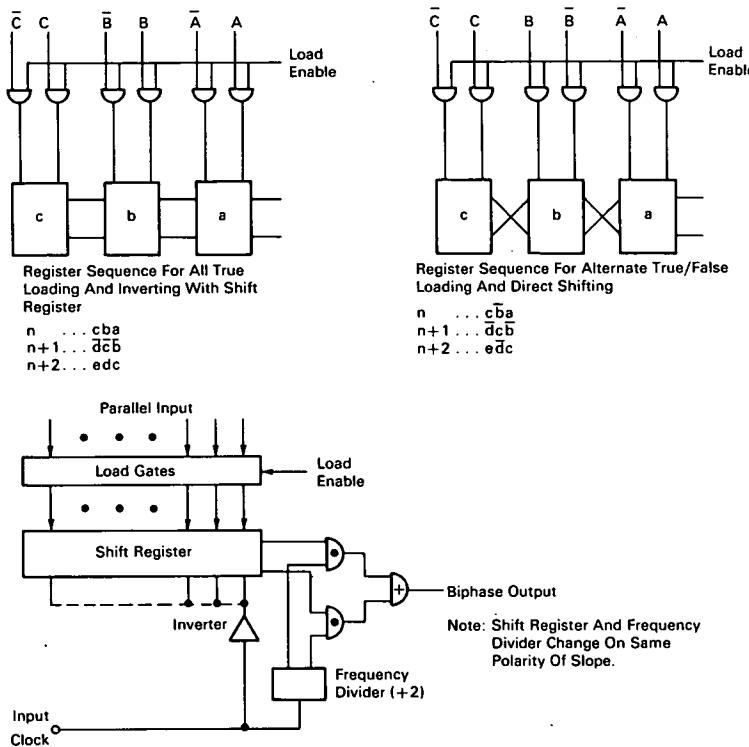
A data converter has been designed to produce a serial biphase output signal from parallel input data. Alternate bits are loaded into a shift register in complement form so that the bits appear at the end of the shift register in a true-complement form sequence. Use of a simple "exclusive-or" and a frequency divider generates the biphase signal with no timing "race" conditions. The logic illustrated generates biphase by (1) causing an output midbit voltage transition for each frequency divider change by forcing a change in

comparison state of the "exclusive-or" output gates, and (2) causing the shift register output stage to change state (hence comparison state) for two sequential bits of the same state and to remain the same (no comparator change) to generate a change in output bit state.

The shift register and frequency divider flip-flops change state on the same polarity of input slope. With an inverter placed between the frequency divider input and shift register input, the frequency divider

(continued overleaf)

changes states one-half bit period before the shift register receives a clock pulse. Both frequency divider and shift register are closed at the input clock rate.

Notes:

1. Logical state of a bit is decided by either (a) loading the parallel data alternately true and false, or (b) coupling shift stages so that a stage assumes the logical inverse of the preceding stage for each shift pulse. Shift operation occurs on one clock pulse slope while the count operation occurs on the other.

2. Inquiries concerning this innovation may be directed to:

Technology Utilization Officer
Manned Spacecraft Center
Houston, Texas 77058
Reference: B68-10241

Patent status:

No patent action is contemplated by NASA.

Source: R. D. Truelove
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